

Contact Information	School of Computing KAIST 291 Daehak-ro, Yuseong-gu Daejeon, South Korea, 34141	E-mail: jongse@kaist.ac.kr URL: https://jongse-park.github.io
Research Interests	Computer architecture, hardware acceleration, machine learning, distributed systems, approximate computing technologies.	
Employment	Assistant Professor. KAIST Product Engineer. Bigstream Solutions Inc.	Dec. 2019–date Jun. 2018–Nov. 2019
Education	Ph.D. in Computer Science. Georgia Institute of Technology • Advisor: Dr. Hadi Esmaeilzadeh • Dissertation: <i>Breaking the Abstractions for Productivity and Performance in the Era of Specialization</i>	Aug. 2013–Aug. 2018
	M.S. in Computer Science. KAIST • Advisor: Dr. Seungryoul Maeng • Thesis: <i>Dynamic Resource Reconfiguration on the Cloud for Improving Data Locality</i> • GPA: 3.71/4.30 (93.4%)	Feb. 2012
	B.E. in Computer Science and Engineering. Sogang University • GPA: 3.74/4.30 (93.4%) • Graduated with Honors	Feb. 2010
Honors and Awards	Distinguished paper award. IEEE Symposium on High Performance Computer Architecture. “TABLA: A Unified Template-Based Framework for Accelerating Statistical Machine Learning”	2016
	Honorable Mention in IEEE Micro Top Picks from 2014 Computer Architecture Conferences. “General-Purpose Code Acceleration with Limited-Precision Analog Computation”	2015
	Kwanjeong Foundation Scholarship, Kwanjeong Educational Foundation (KEF)	2013–2018
	National Full Scholarship, KAIST	2010–2012
	Dean's Honored Graduate, Ranked 3 rd among graduates of the class of 2010	2010
	DMC General Management Track Scholarship, Samsung Electronics Co., Ltd	2009
	Academic Scholarship, Sogang University, 7 semesters	2004–2009
Refereed Conference Papers	<ol style="list-style-type: none"> Y. Li, J. Park, M. Alian, Y. Yuan, Q. Zheng, P. Pan, R. Wang, A. Schwing, H. Esmaeilzadeh, N. Kim, “A Network-Centric Hardware/Algorithm Co-Design to Accelerate Distributed Training of Deep Neural Networks,” <i>The 50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)</i>, October 2018. H. Sharma, J. Park, B. Samynathan, B. Robotmili, S. Mirkhani, H. Esmaeilzadeh, “From Tensors to FPGAs: Accelerating Deep Learning,” <i>A Symposium on High Performance Chips (Hot Chips)</i>, August 2018. H. Sharma, J. Park, N. Suda, L. Lai, B. Chau, J. Kim, V. Chandra, H. Esmaeilzadeh, “Bit Fusion: Bit-Level Dynamically Composable Architecture for Accelerating Deep Neural Networks,” <i>International Symposium on Computer Architecture (ISCA)</i>, June 2018. J. Park, H. Sharma, D. Mahajan, J. Kim, P. Olds, H. Esmaeilzadeh, “Scale-Out Acceleration for Machine Learning,” in <i>The 50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)</i>, October 2017. 	

5. **J. Park**, E. Amaro, D. Mahajan, B. Thwaites, H. Esmaeilzadeh, "AXGAMES: Towards Crowdsourcing Quality Target Determination in Approximate Computing," in *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2016.
6. H. Sharma, **J. Park**, D. Mahajan, E. Amaro, J. Kim, C. Shao, A. Mishra, H. Esmaeilzadeh "From High-Level Deep Neural Models to FPGAs," in *The 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October 2016.
7. D. Mahajan, **J. Park**, E. Amaro, H. Sharma, A. Yazdanbakhsh, J. Kim, H. Esmaeilzadeh, "TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning," in *The 22nd IEEE Symposium on High Performance Computer Architecture (HPCA)*, March 2016.
(Distinguished Paper Award)
8. D. Mahajan, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, "Towards Statistical Guarantees in Controlling Quality Tradeoffs in Approximate Acceleration," in *International Symposium on Computer Architecture (ISCA)*, June 2016.
9. A. Yazdanbakhsh, **J. Park**, H. Sharma, P. Lotfi-Kamran, H. Esmaeilzadeh, "Neural Acceleration for GPU Throughput Processors," in *The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2015.
10. **J. Park**, H. Esmaeilzadeh, X. Zhang, M. Naik, W. Harris, "FLEXJAVA: Language Support for Safe and Modular Approximate Programming," in *The 10th Joint Meeting of the European Software Engineering Conference and the ACM SIGSOFT Symposium on the Foundations of Software Engineering (FSE)*, September 2015.
11. A. Yazdanbakhsh, D. Mahajan, B. Thwaites, **J. Park**, A. Nagendrakumar, S. Sethuraman, K. Ramkrishnan, N. Ravindran, R. Jariwala, A. Rahimi, H. Esmaeilzadeh, K. Bazargan, "AXILOG: Language Support for Approximate Hardware Design," in *Design Automation and Test in Europe (DATE)*, March 2015.
12. R. S. Amant, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, A. Hassibi, L. Ceze, D. Burger, "General-Purpose Code Acceleration with Limited-Precision Analog Computation," in *The 41th International Symposium on Computer Architecture (ISCA)*, June 2014.
(Nominated for CACM Research Highlights; Honorable Mention in IEEE Micro Top Picks)
13. B. Thwaites, G. Pekhimenko, A. Yazdanbakhsh, **J. Park**, G. Mururu, H. Esmaeilzadeh, O. Mutlu, T. Mowry, "Rollback-Free Value Prediction with Approximate Loads," in *The 24th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, August 2014.
14. J. Choi, **J. Park**, J. Seol, and S. Maeng, "Isolated Mini-domain for Trusted Cloud Computing," in *The 13th International Symposium on Cluster, Cloud, and Grid Computing (CCGrid)*, May 2013.
15. **J. Park**, D. Lee, B. Kim, J. Huh, S. Maeng, "Locality-aware Dynamic VM Reconfiguration on MapReduce Clouds," in *The 21st International ACM Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, June 2012.

Refereed Journal Articles

1. D. Mahajan, K. Ramkrishnan, R. Jariwala, A. Yazdanbakhsh, **J. Park**, B. Thwaites, A. Nagendrakumar, A. Rahimi, H. Esmaeilzadeh, K. Bazargan, "AXILOG: Abstractions for Approximate Hardware Design and Reuse," in *IEEE Micro, special issue on Alternative Computing Designs and Technologies*, October 2015.

Refereed Workshop Papers

1. H. Sharma, **J. Park**, E. Amaro, B. Thwaites, P. Kotha, A. Gupta, J. Kim, A. Mishra, H. Esmaeilzadeh, "DNNWEAVER: From High-Level Deep Network Models to FPGA Acceleration," in *The Second Workshop on Cognitive Architectures (CogArch) in conjunction with ASPLOS*, April 2016.
2. D. Mahajan, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, "Prediction-Based Quality Control for Approximate Accelerators," in *The Second Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2015.

3. **J. Park**, K. Ni, X. Zhang, H. Esmaeilzadeh, M. Naik, "Expectation-Oriented Framework for Automating Approximate Programming," in *The First Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2014.
4. A. Yazdanbakhsh, B. Thwaites, **J. Park**, H. Esmaeilzadeh, "Methodical Approximate Hardware Design and Reuse," in *The First Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2014.
5. A. Yazdanbakhsh, R. Amant, B. Thwaites, **J. Park**, H. Esmaeilzadeh, A. Hassibi, L. Ceze, D. Burger, "Toward General-Purpose Code Acceleration with Analog Computation," in *The First Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2014.
6. B. Thwaites, A. Yazdanbakhsh, **J. Park**, H. Esmaeilzadeh, "Bio-Accelerators: Bridging Biology and Silicon for General-Purpose Computing," in *Wild and Crazy Ideas (WACI) in conjunction with ASPLOS*, March 2014.

Research Experience	Research Assistant. Alternative Computing Technology (ACT) Lab <ul style="list-style-type: none"> Georgia Institute of Technology Advisor: Dr. Hadi Esmaeilzadeh 	Aug. 2013–Aug. 2018
	Visiting Researcher. Alternative Computing Technology (ACT) Lab <ul style="list-style-type: none"> University of California, San Diego Advisor: Dr. Hadi Esmaeilzadeh 	Jan. 2018–Aug. 2018
	Research Intern. Architecture Research Group (ARG) <ul style="list-style-type: none"> NVIDIA Research Mentors: Dr. Arslan Zulfiqar and Dr. Eiman Ebrahimi Manager: Dr. Steve Keckler 	May 2017–Aug. 2017
	Research Intern. Catapult team <ul style="list-style-type: none"> Microsoft Research Mentor: Dr. Eric Chung Manager: Dr. Doug Burger 	Jan. 2016–May 2016
	Research Assistant. Computer Architecture (CA) Lab <ul style="list-style-type: none"> Korea Advanced Institute of Science and Technology (KAIST) Advisor: Dr. Seungryoul Maeng 	Feb. 2010–Jul. 2013
Teaching Experience	Teaching Assistant. <ul style="list-style-type: none"> CS3220: Processor Design Georgia Institute of Technology Fall 2016 CS3220: Processor Design Georgia Institute of Technology Fall 2014 CS8803: Alternative Computing Technology Georgia Institute of Technology Spring 2014 CS211: Digital System and Lab. KAIST Spring 2011 CS311: Embedded Computer Systems. KAIST Fall 2010 	
Technical Skills	Programming languages: C/C++, Java, Python, CUDA, Verilog, Bash, JavaScript, HTML Development Tools: Tensorflow, Amazon EC2, Spark, Hadoop, Chord, LLVM	
References Available to Contact	Hadi Esmaeilzadeh. Associate Professor, UCSD <ul style="list-style-type: none"> 9500 Gilman Drive, La Jolla, CA 92093 	hadi@eng.ucsd.edu +1 (206) 658-3952
	Doug Burger. Distinguished Engineer, Microsoft Research <ul style="list-style-type: none"> 1 Microsoft Way, Redmond, WA 98052 	dburger@microsoft.com
	Stephen W. Keckler. Vice President, NVIDIA Research <ul style="list-style-type: none"> 11001 Lakeline Blvd, Austin, TX 78717 	skeckler@nvidia.com

Eric Chung. Senior Researcher, Microsoft Research

- 1 Microsoft Way, Redmond, WA 98052

erchung@microsoft.com

+1 (408) 477-5435

Eiman Ebrahimi. Senior Research Scientist, NVIDIA Research

- 11001 Lakeline Blvd, Austin, TX 78717

eebrahimi@nvidia.com

+1 (215) 573-1856

Mayur Naik. Associate Professor, University of Pennsylvania

- 3330 Walnut St, Philadelphia, PA 19104

mhnaik@cis.upenn.edu

+1 (215) 573-1856

Maysam Lavasani, CEO, Bigstream Solutions Inc.

- 1975 W El Camino Real #300, Mountain View, CA 94040, United States

maysam@bigstream.co

+1 (512) 632-5758