CS.50100 Computer Architecture (Spring 2026)

Course:	CS.50100 Computer Architecture
Instructor:	Jongse Park E3-5 405 Phone: 042-350-3580 jspark@casys.kaist.ac.kr
Teaching Assistants	TBA
Class Meetings	MW 14:30-15:45PM
Textbook	**Computer Architecture: A Quantitative Approach, Fifth Edition, Morgan Kaufmann, 2011,** John L Hennessy and David A. A set of research papers
Course Objectives	Computer architecture is a fast-evolving area with interesting new techniques added in every generation of processors. Recently, the area is facing a new phase of evolution with billions of transistors on a chip and multicores techniques. This course will cover various aspects of high-performance microprocessors, which include pipelining, front-end design, out-of-order execution, and caches. As multiprocessor/multicore technologies are used in all levels of computing from laptops to supercomputers, the course will cover topics in multiprocessor and GPU technologies. This course will also cover recent advances in computer architecture on AI accelerators.
Prerequisites	You need reasonable understanding of computer architecture and operating systems from undergraduate courses.
Assignments	There will be a set of projects.
Evaluation	TBD
Late submission policy	• Assignments will be due at 11:59pm on the specified due date. • You will lose 30% of the grade on the first late day. After the first late day, your submission will not be accepted.
Academic conduct	• You are encouraged to discuss course material with your classmates. However, collaboration on assignments is prohibited. Academic misconduct will have a heavy penalty. • Possession and/or use of another group's code is strictly prohibited. It is also the student's responsibility to protect his or her work from unauthorized access. • We will be using a sophisticated automated program to correlate projects to find copied codes.

Spring 2026 Tentative Schedule

Week	Topic
1	Pipelining and ISA
2	Memory Hierarchies
3	Cache Optimization
4	Instruction-Level Parallelism I
5	Instruction-Level Parallelism II
6	Out-of-Order Execution
7	Multithreading
8	Midterm Exam
9	Cache Coherence and Memory Consistency I
10	Cache Coherence and Memory Consistency II
11	Parallel Programming and Synchronization
12	SIMD and GPU I
13	SIMD and GPU II
14	Accelerators I
15	Accelerators II
16	Final Exam