Jongse Park

November 2019

Contact Information

School of Computing
KAIST
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Research Interests

Computer architecture, hardware acceleration, machine learning, distributed systems, approximate computing technologies.

Employment

Assistant Professor. **KAIST** Dec. 2019–date
Product Engineer. **Bigstream Solutions Inc.** Jun. 2018–Nov. 2019

Education

Ph.D. in Computer Science. Georgia Institute of Technology Aug. 2013–Aug. 2018

- Advisor: Dr. Hadi Esmaeilzadeh
- Dissertation: *Breaking the Abstractions for Productivity and Performance in the Era of Specialization*

M.S. in Computer Science. KAIST Feb. 2012

- Advisor: Dr. Seungryoul Maeng
- Thesis: *Dynamic Resource Reconfiguration on the Cloud for Improving Data Locality*
- GPA: 3.71/4.30 (93.4%)

B.E. in Computer Science and Engineering. Sogang University Feb. 2010

- GPA: 3.74/4.30 (93.4%)
- Graduated with Honors

Honors and Awards

Distinguished paper award. IEEE Symposium on High Performance Computer Architecture. 2016
"TABLA: A Unified Template-Based Framework for Accelerating Statistical Machine Learning"

Honorable Mention in IEEE Micro Top Picks from 2014 Computer Architecture Conferences. 2015
"General-Purpose Code Acceleration with Limited-Precision Analog Computation"

Kwanjeong Foundation Scholarship, Kwanjeong Educational Foundation (KEF) 2013–2018

National Full Scholarship, KAIST 2010–2012

Dean's Honored Graduate, Ranked 3^{rd} among graduates of the class of 2010 2010

DMC General Management Track Scholarship, Samsung Electronics Co., Ltd 2009

Academic Scholarship, Sogang University, 7 semesters 2004–2009

Refereed Conference Papers

1. Y. Li, **J. Park**, M. Alian, Y. Yuan, Q. Zheng, P. Pan, R. Wang, A. Schwing, H. Esmaeilzadeh, N. Kim, "A Network-Centric Hardware/Algorithm Co-Design to Accelerate Distributed Training of Deep Neural Networks," *The 50th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, October 2018.
2. H. Sharma, **J. Park**, B. Samynathan, B. Robatmili, S. Mirkhani, H. Esmaeilzadeh, "From Tensors to FPGAs: Accelerating Deep Learning," *A Symposium on High Performance Chips (**Hot Chips**)*, August 2018.
3. H. Sharma, **J. Park**, N. Suda, L. Lai, B. Chau, J. Kim, V. Chandra, H. Esmaeilzadeh, "Bit Fusion: Bit-Level Dynamically Composable Architecture for Accelerating Deep Neural Networks," *International Symposium on Computer Architecture (**ISCA**)*, June 2018.
4. **J. Park**, H. Sharma, D. Mahajan, J. Kim, P. Olds, H. Esmaeilzadeh, "Scale-Out Acceleration for Machine Learning," in *The 50th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, October 2017.

5. **J. Park**, E. Amaro, D. Mahajan, B. Thwaites, H. Esmaeilzadeh, "AxGames: Towards Crowdsourcing Quality Target Determination in Approximate Computing," in *International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, April 2016.

6. H. Sharma, **J. Park**, D. Mahajan, E. Amaro, J. Kim, C. Shao, A. Mishra, H. Esmaeilzadeh "From High-Level Deep Neural Models to FPGAs," in *The 49th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, October 2016.

7. D. Mahajan, **J. Park**, E. Amaro, H. Sharma, A. Yazdanbaksh, J. Kim, H. Esmaeilzadeh, "Tabla: A Unified Template-based Framework for Accelerating Statistical Machine Learning," in *The 22nd IEEE Symposium on High Performance Computer Architecture (**HPCA**)*, March 2016.

   (Distinguished Paper Award)

8. D. Mahajan, A. Yazdanbaksh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, "Towards Statistical Guarantees in Controlling Quality Tradeoffs in Approximate Acceleration," in *International Symposium on Computer Architecture (**ISCA**)*, June 2016.

9. A. Yazdanbakhsh, **J. Park**, H. Sharma, P. Lotfi-Kamran, H. Esmaeilzadeh, "Neural Acceleration for GPU Throughput Processors," in *The 48th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, December 2015.

10. **J. Park**, H. Esmaeilzadeh, X. Zhang, M. Naik, W. Harris, "FlexJava: Language Support for Safe and Modular Approximate Programming," in *The 10th Joint Meeting of the European Software Engineering Conference and the ACM SIGSOFT Symposium on the Foundations of Software Engineering (**FSE**)*, September 2015.

11. A. Yazdanbakhsh, D. Mahajan, B. Thwaites, **J. Park**, A. Nagendrakumar, S. Sethuraman, K. Ramkrishnan, N. Ravindran, R. Jariwala, A. Rahimi, H. Esmailzadeh, K. Bazargan, "Axilog: Language Support for Approximate Hardware Design," in *Design Automation and Test in Europe (**DATE**)*, March 2015.

12. R. S. Amant, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, A. Hassibi, L. Ceze, D. Burger, "General-Purpose Code Acceleration with Limited-Precision Analog Computation," in *The 41th International Symposium on Computer Architecture (**ISCA**)*, June 2014.

    (Nominated for CACM Research Highlights; Honorable Mention in IEEE Micro Top Picks)

13. B. Thwaites, G. Pekhimenko, A. Yazdanbakhsh, **J. Park**, G. Mururu, H. Esmaeilzadeh, O. Mutlu, T. Mowry, "Rollback-Free Value Prediction with Approximate Loads," in *The 24th International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, August 2014.

14. J. Choi, **J. Park**, J. Seol, and S. Maeng, "Isolated Mini-domain for Trusted Cloud Computing," in *The 13th International Symposium on Cluster, Cloud, and Grid Computing (**CCGrid**)*, May 2013.

15. **J. Park**, D. Lee, B. Kim, J. Huh, S. Maeng, "Locality-aware Dynamic VM Reconfiguration on MapReduce Clouds," in *The 21st International ACM Symposium on High-Performance Parallel and Distributed Computing (**HPDC**)*, June 2012.

Refereed Journal Articles

1. D. Mahajan, K. Ramkrishnan, R. Jariwala, A. Yazdanbakhsh, **J. Park**, B. Thwaites, A. Nagendrakumar, A. Rahimi, H. Esmaeilzadeh, K. Bazargan, "Axilog: Abstractions for Approximate Hardware Design and Reuse," in ***IEEE Micro**, special issue on Alternative Computing Designs and Technologies*, October 2015.

Refereed Workshop Papers

1. H. Sharma, **J. Park**, E. Amaro, B. Thwaites, P. Kotha, A. Gupta, J. Kim, A. Mishra, H. Esmaeilzadeh, "DnnWeaver: From High-Level Deep Network Models to FPGA Acceleration," in *The Second Workshop on Cognitive Architectures (**CogArch**) in conjunction with ASPLOS*, April 2016.

2. D. Mahajan, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, "Prediction-Based Quality Control for Approximate Accelerators," in *The Second Workshop on Approximate Computing Across the System Stack (**WACAS**) in conjunction with ASPLOS*, March 2015.

3. **J. Park**, K. Ni, X. Zhang, H. Esmaeilzadeh, M. Naik, "Expectation-Oriented Framework for Automating Approximate Programming,", in *The First Workshop on Approximate Computing Across the System Stack (**WACAS**) in conjunction with ASPLOS*, March 2014.

4. A. Yazdanbakhsh, B. Thwaites, **J. Park**, H. Esmaeilzadeh, "Methodical Approximate Hardware Design and Reuse," in *The First Workshop on Approximate Computing Across the System Stack (**WACAS**) in conjunction with ASPLOS*, March 2014.

5. A. Yazdanbakhsh, R. Amant, B. Thwaites, **J. Park**, H. Esmaeilzadeh, A. Hassibi, L. Ceze, D. Burger, "Toward General-Purpose Code Acceleration with Analog Computation," in *The First Workshop on Approximate Computing Across the System Stack (**WACAS**) in conjunction with ASPLOS*, March 2014.

6. B. Thwaites, A. Yazdanbakhsh, **J. Park**, H. Esmaeilzadeh, "Bio-Accelerators: Bridging Biology and Silicon for General-Purpose Computing," in *Wild and Crazy Ideas (**WACI**) in conjunction with ASPLOS*, March 2014.

Research Experience

Research Assistant. Alternative Computing Technology (ACT) Lab — Aug. 2013–Aug. 2018
- Georgia Institute of Technology
- Advisor: Dr. Hadi Esmaeilzadeh

Visiting Researcher. Alternative Computing Technology (ACT) Lab — Jan. 2018–Aug. 2018
- University of California, San Diego
- Advisor: Dr. Hadi Esmaeilzadeh

Research Intern. Architecture Research Group (ARG) — May 2017–Aug. 2017
- NVIDIA Research
- Mentors: Dr. Arslan Zulfiqar and Dr. Eiman Ebrahimi
- Manager: Dr. Steve Keckler

Research Intern. Catapult team — Jan. 2016–May 2016
- Microsoft Research
- Mentor: Dr. Eric Chung
- Manager: Dr. Doug Burger

Research Assistant. Computer Architecture (CA) Lab — Feb. 2010–Jul. 2013
- Korea Advanced Institute of Science and Technology (KAIST)
- Advisor: Dr. Seungryoul Maeng

Teaching Experience

Teaching Assistant.

• CS3220:	Processor Design	Georgia Institute of Technology	Fall 2016
• CS3220:	Processor Design	Georgia Institute of Technology	Fall 2014
• CS8803:	Alternative Computing Technology	Georgia Institute of Technology	Spring 2014
• CS211:	Digital System and Lab.	KAIST	Spring 2011
• CS311:	Embedded Computer Systems.	KAIST	Fall 2010

Technical Skills

Programming languages: C/C++, Java, Python, CUDA, Verilog, Bash, JavaScript, HTML
Development Tools: Tensorflow, Amazon EC2, Spark, Hadoop, Chord, LLVM

References Available to Contact

Hadi Esmaeilzadeh. Associate Professor, UCSD — hadi@eng.ucsd.edu
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Doug Burger. Distinguished Engineer, Microsoft Research — dburger@microsoft.com
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