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<b>Research Interests</b>	Computer architecture, hardware acceleration, machine learning, distributed systems, approximate computing technologies.	
<b>Employment</b>	Assistant Professor. <b>KAIST</b> Product Engineer. <b>Bigstream Solutions Inc.</b>	Dec. 2019–date Jun. 2018–Nov. 2019
<b>Education</b>	<b>Ph.D. in Computer Science. Georgia Institute of Technology</b> • Advisor: <a href="#">Dr. Hadi Esmaeilzadeh</a> • Dissertation: <i>Breaking the Abstractions for Productivity and Performance in the Era of Specialization</i> <b>M.S. in Computer Science. KAIST</b> • Advisor: <a href="#">Dr. Seungryoul Maeng</a> • Thesis: <i>Dynamic Resource Reconfiguration on the Cloud for Improving Data Locality</i> <b>B.E. in Computer Science and Engineering. Sogang University</b> • Graduated with Honors	Aug. 2013–Aug. 2018          Feb. 2012          Feb. 2010
<b>Honors and Awards</b>	Distinguished paper award. IEEE Symposium on High Performance Computer Architecture. 2016 “TABLA: A Unified Template-Based Framework for Accelerating Statistical Machine Learning” Honorable Mention in IEEE Micro Top Picks from 2014 Computer Architecture Conferences. 2015 “General-Purpose Code Acceleration with Limited-Precision Analog Computation” Kwanjeong Foundation Scholarship, Kwanjeong Educational Foundation (KEF) 2013–2018 National Full Scholarship, KAIST 2010–2012 Dean’s Honored Graduate, Ranked 3 <sup>rd</sup> among graduates of the class of 2010 2010 DMC General Management Track Scholarship, Samsung Electronics Co., Ltd 2009 Academic Scholarship, Sogang University, 7 semesters 2004–2009	
<b>Refereed Journal Articles</b>	1. J. Park, S. Kang, S. Lee, T. Kim, <b>J. Park</b> , Y. Kwon, and J. Huh, “Hardware Hardened Sandbox Enclaves for Trusted Serverless Computing” in <i>IEEE Transactions on Architecture and Code Optimization (TACO)</i> , 2023. 2. S. Noh, J. Koo, S. Lee, <b>J. Park</b> , and J. Kung, “FlexBlock: A Flexible DNN Training Accelerator with Multi-Mode Block Floating Point Support” in <i>IEEE Transactions on Computers (TC)</i> , 2023. 3. S. Lee, R. Hwang, <b>J. Park</b> , and M. Rhu, “HAMMER: Hardware-friendly Approximate Computing for Self-attention with Mean-redistribution and Linearization” in <i>IEEE Computer Architecture Letters (CAL)</i> , 2023. 4. W. Seo, S. Cha, Y. Kim, J. Huh, and <b>J. Park</b> , “SLO-aware Inference Scheduler for Heterogeneous Processors in Edge Platforms” in <i>Transactions on Architecture and Code Optimization (TACO)</i> , 2021. 5. D. Mahajan, K. Ramkrishnan, R. Jariwala, A. Yazdanbakhsh, <b>J. Park</b> , B. Thwaites, A. Nagendrakumar, A. Rahimi, H. Esmaeilzadeh, K. Bazargan, “AXILOG: Abstractions for Approximate Hardware Design and Reuse,” in <i>IEEE Micro, special issue on Alternative Computing Designs and Technologies</i> , October 2015.	

1. M. Kim, J. Hwang, G. Heo, S. Cho, D. Mahajan, **J. Park**, "Accelerating String-key Learned Index Structures via Memoization-based Incremental Training" in *International Conference on Very Large Data Bases (VLDB)*, August 2024 (To Appear).
2. S. Ghodrati, S. Kinzer, H. Xu, R. Mahapatra, Y. Kim, B. H. Ahn, D. K. Wang, L. Karthikeyan, A. Yazdanbakhsh, **J. Park**, N. S. Kim, H. Esmaeilzadeh, "Tandem Processor: Grappling with Emerging Operators in Neural Networks" in *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2024 (To Appear).
3. Sunho Lee, Seonjin Na, Jungwoo Kim, Jongse Park, and Jaehyuk Huh, "Tunable Memory Protection for Secure Neural Processing Units" in *The 40th IEEE International Conference on Computer Design (ICCD)*, October 2022.
4. Bokyeong Kim, Soojin Hwang, Sanghoon Cha, Chang Hyun Park, Jongse Park, and Jaehyuk Huh, "Supporting Dynamic Translation Granularity for Hybrid Memory Systems" in *The 40th IEEE International Conference on Computer Design (ICCD)*, October 2022.
5. Joon Kyung Kim, Byung Hoon Ahn, Sean Kinzer, Soroush Ghodrati, Rohan Mahapatra, Brahmen-dra Yatham, Dohee Kim, Parisa Sarikhani, Babak Mahmoudi, Divya Mahajan, Jongse Park, Hadi Esmaeilzadeh, "Yin-Yang: Programming Abstraction for Cross-Domain Multi-Acceleration", in *IEEE Micro, special issue on Compiling for Accelerators*, 2022.
6. Jinwoo Hwang, Minsu Kim, Daeun Kim, Seungho Nam, Yoonsung Kim, Dohee Kim, Hardik Sharma, Jongse Park, "CoVA: Exploiting Compressed-Domain Analysis to Accelerate Video Analytics", in *USENIX Annual Technical Conference (ATC)*, July 2022.
7. Seungbeom Choi, Sunho Lee, Yeonjae Kim, Jongse Park, Youngjin Kwon, and Jaehyuk Huh, "Serving Heterogeneous Machine Learning Models on Multi-GPU Servers with Spatio-Temporal Sharing", in *USENIX Annual Technical Conference (ATC)*, July 2022.
8. S. Lee, J. Kim, S. Na, **J. Park**, and J. Huh, "TNPU: Supporting Trusted Execution with Tree-less Integrity Protection for Neural Processing Unit" in *The 27th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February 2022. [To appear]
9. S. Na, S. Lee, Y. Kim, **J. Park**, and J. Huh, "Common Counters: Compressed Encryption Counters for Secure GPU Memory" in *The 27th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, February 2021.
10. S. Ghodrati, H. Sharma, S. Kinzer, A. Yazdanbakhsh, **J. Park**, N. Kim, D. Burger, and H. Esmaeilzadeh, "Mixed-Signal Charge-Domain Acceleration of Deep Neural Networks through Inter-leaved Bit-Partitioned Arithmetic" in *The 29th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2020.
11. Y. Li, **J. Park**, M. Alian, Y. Yuan, Q. Zheng, P. Pan, R. Wang, A. Schwing, H. Esmaeilzadeh, N. Kim, "A Network-Centric Hardware/Algorithm Co-Design to Accelerate Distributed Training of Deep Neural Networks," *The 50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October 2018.
12. H. Sharma, **J. Park**, B. Samynathan, B. Robatmili, S. Mirkhani, H. Esmaeilzadeh, "From Tensors to FPGAs: Accelerating Deep Learning," *A Symposium on High Performance Chips (Hot Chips)*, August 2018.
13. H. Sharma, **J. Park**, N. Suda, L. Lai, B. Chau, J. Kim, V. Chandra, H. Esmaeilzadeh, "Bit Fusion: Bit-Level Dynamically Composable Architecture for Accelerating Deep Neural Networks," *International Symposium on Computer Architecture (ISCA)*, June 2018.
14. **J. Park**, H. Sharma, D. Mahajan, J. Kim, P. Olds, H. Esmaeilzadeh, "Scale-Out Acceleration for Machine Learning," in *The 50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October 2017.
15. **J. Park**, E. Amaro, D. Mahajan, B. Thwaites, H. Esmaeilzadeh, "AXGAMES: Towards Crowdsourcing Quality Target Determination in Approximate Computing," in *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2016.

16. H. Sharma, **J. Park**, D. Mahajan, E. Amaro, J. Kim, C. Shao, A. Mishra, H. Esmaeilzadeh "From High-Level Deep Neural Models to FPGAs," in *The 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October 2016.
17. D. Mahajan, **J. Park**, E. Amaro, H. Sharma, A. Yazdanbakhsh, J. Kim, H. Esmaeilzadeh, "TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning," in *The 22nd IEEE Symposium on High Performance Computer Architecture (HPCA)*, March 2016.  
**(Distinguished Paper Award)**
18. D. Mahajan, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, "Towards Statistical Guarantees in Controlling Quality Tradeoffs in Approximate Acceleration," in *International Symposium on Computer Architecture (ISCA)*, June 2016.
19. A. Yazdanbakhsh, **J. Park**, H. Sharma, P. Lotfi-Kamran, H. Esmaeilzadeh, "Neural Acceleration for GPU Throughput Processors," in *The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2015.
20. **J. Park**, H. Esmaeilzadeh, X. Zhang, M. Naik, W. Harris, "FLEXJAVA: Language Support for Safe and Modular Approximate Programming," in *The 10th Joint Meeting of the European Software Engineering Conference and the ACM SIGSOFT Symposium on the Foundations of Software Engineering (FSE)*, September 2015.
21. A. Yazdanbakhsh, D. Mahajan, B. Thwaites, **J. Park**, A. Nagendrakumar, S. Sethuraman, K. Ramkrishnan, N. Ravindran, R. Jariwala, A. Rahimi, H. Esmaeilzadeh, K. Bazargan, "AXILOG: Language Support for Approximate Hardware Design," in *Design Automation and Test in Europe (DATE)*, March 2015.
22. R. S. Amant, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, A. Hassibi, L. Ceze, D. Burger, "General-Purpose Code Acceleration with Limited-Precision Analog Computation," in *The 41th International Symposium on Computer Architecture (ISCA)*, June 2014.  
**(Nominated for CACM Research Highlights; Honorable Mention in IEEE Micro Top Picks)**
23. B. Thwaites, G. Pekhimenko, A. Yazdanbakhsh, **J. Park**, G. Mururu, H. Esmaeilzadeh, O. Mutlu, T. Mowry, "Rollback-Free Value Prediction with Approximate Loads," in *The 24th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, August 2014.
24. J. Choi, **J. Park**, J. Seol, and S. Maeng, "Isolated Mini-domain for Trusted Cloud Computing," in *The 13th International Symposium on Cluster, Cloud, and Grid Computing (CCGrid)*, May 2013.
25. **J. Park**, D. Lee, B. Kim, J. Huh, S. Maeng, "Locality-aware Dynamic VM Reconfiguration on MapReduce Clouds," in *The 21st International ACM Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, June 2012.

#### Refereed Workshop Papers

1. H. Sharma, **J. Park**, E. Amaro, B. Thwaites, P. Kotha, A. Gupta, J. Kim, A. Mishra, H. Esmaeilzadeh, "DNNWEAVER: From High-Level Deep Network Models to FPGA Acceleration," in *The Second Workshop on Cognitive Architectures (CogArch) in conjunction with ASPLOS*, April 2016.
2. D. Mahajan, A. Yazdanbakhsh, **J. Park**, B. Thwaites, H. Esmaeilzadeh, "Prediction-Based Quality Control for Approximate Accelerators," in *The Second Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2015.
3. **J. Park**, K. Ni, X. Zhang, H. Esmaeilzadeh, M. Naik, "Expectation-Oriented Framework for Automating Approximate Programming," in *The First Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2014.
4. A. Yazdanbakhsh, B. Thwaites, **J. Park**, H. Esmaeilzadeh, "Methodical Approximate Hardware Design and Reuse," in *The First Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2014.
5. A. Yazdanbakhsh, R. Amant, B. Thwaites, **J. Park**, H. Esmaeilzadeh, A. Hassibi, L. Ceze, D. Burger, "Toward General-Purpose Code Acceleration with Analog Computation," in *The First Workshop on Approximate Computing Across the System Stack (WACAS) in conjunction with ASPLOS*, March 2014.

6. B. Thwaites, A. Yazdanbakhsh, **J. Park**, H. Esmaeilzadeh, “Bio-Accelerators: Bridging Biology and Silicon for General-Purpose Computing,” in *Wild and Crazy Ideas (WACI) in conjunction with ASPLOS*, March 2014.

<b>Research Experience</b>	<b>Research Assistant.</b> Alternative Computing Technology (ACT) Lab <ul style="list-style-type: none"> <li>Georgia Institute of Technology</li> <li>Advisor: Dr. Hadi Esmaeilzadeh</li> </ul>	Aug. 2013–Aug. 2018
	<b>Visiting Researcher.</b> Alternative Computing Technology (ACT) Lab <ul style="list-style-type: none"> <li>University of California, San Diego</li> <li>Advisor: Dr. Hadi Esmaeilzadeh</li> </ul>	Jan. 2018–Aug. 2018
	<b>Research Intern.</b> Architecture Research Group (ARG) <ul style="list-style-type: none"> <li>NVIDIA Research</li> <li>Mentors: Dr. Arslan Zulfiqar and Dr. Eiman Ebrahimi</li> <li>Manager: Dr. Steve Keckler</li> </ul>	May 2017–Aug. 2017
	<b>Research Intern.</b> Catapult team <ul style="list-style-type: none"> <li>Microsoft Research</li> <li>Mentor: Dr. Eric Chung</li> <li>Manager: Dr. Doug Burger</li> </ul>	Jan. 2016–May 2016
	<b>Research Assistant.</b> Computer Architecture (CA) Lab <ul style="list-style-type: none"> <li>Korea Advanced Institute of Science and Technology (KAIST)</li> <li>Advisor: Dr. Seungryoul Maeng</li> </ul>	Feb. 2010–Jul. 2013
<b>Teaching Experience</b>	<b>Instructor.</b> <ul style="list-style-type: none"> <li>CS610: Parallel Processing</li> <li>CS311: Computer Organization</li> <li>CS411: System for AI</li> <li>CS510: Computer Architecture</li> <li>CS230: System Programming</li> <li>CS311: Computer Organization</li> <li>CS230: System Programming</li> <li>CS492: Special Topic in Computer Science: System for Artificial Intelligence</li> <li>CS230: System Programming</li> <li>CS492: Special Topic in Computer Science: System for Machine Learning</li> </ul>	Spring 2024 Spring 2024 Fall 2023 Spring 2023 Fall 2022 Spring 2022 Fall 2021 Spring 2021 Fall 2020 Spring 2020
	<b>Teaching Assistant.</b> <ul style="list-style-type: none"> <li>CS3220: Processor Design</li> <li>CS3220: Processor Design</li> <li>CS8803: Alternative Computing Technology</li> <li>CS211: Digital System and Lab.</li> <li>CS311: Embedded Computer Systems.</li> </ul>	Georgia Institute of Technology Georgia Institute of Technology Georgia Institute of Technology KAIST KAIST Fall 2016 Fall 2014 Spring 2014 Spring 2011 Fall 2010
<b>Technical Skills</b>	Programming languages: C/C++, Java, Python, CUDA, Verilog, Bash, JavaScript, HTML Development Tools: Tensorflow, Amazon EC2, Spark, Hadoop, Chord, LLVM	
<b>References Available to Contact</b>	<b>Hadi Esmaeilzadeh.</b> Associate Professor, UCSD <ul style="list-style-type: none"> <li>9500 Gilman Drive, La Jolla, CA 92093</li> </ul>	<a href="mailto:hadi@eng.ucsd.edu">hadi@eng.ucsd.edu</a> +1 (206) 658-3952
	<b>Doug Burger.</b> Technical Fellow, Microsoft <ul style="list-style-type: none"> <li>1 Microsoft Way, Redmond, WA 98052</li> </ul>	<a href="mailto:dburger@microsoft.com">dburger@microsoft.com</a>
	<b>Stephen W. Keckler.</b> Vice President, NVIDIA Research <ul style="list-style-type: none"> <li>11001 Lakeline Blvd, Austin, TX 78717</li> </ul>	<a href="mailto:skeckler@nvidia.com">skeckler@nvidia.com</a>

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