Jonathan G. Tao

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Education

Ph.D. in Electrical and Computer Engineering March 2026 (Anticipated)
M.S. in Electrical and Computer Engineering March 2022
University of California, Santa Barbara - GPA: 3.96/4.00

B.S. in Electrical Engineering & B.S. in Computer Engineering March 2016
University of California, Davis - GPA: 3.86/4.00 with High Honors

Work

Graduate Student Researcher - UC Santa Barbara in Santa Barbara, CA September 2019 - Present

- Integrated circuits and packaging for receiver arrays above 100 GHz under direction of Professor James Buckwalter.

RFIC Engineer - Internship at HRL in Malibu, CA June 2022 - January 2023

- Phase shifter designs and layout at W-band in HRL T3 GaN, using ADS and Microwave Office.
- LNA design and layout at V-band in GlobalFoundries 45RFSOI using Cadence and EMX.

RFIC Engineer - Internship at SpaceX in Redmond, WA June - September 2021

- Circuit designs and layout for an RFIC in an Earth terminal for a satellite internet system (Starlink).
- Used Cadence and EMX to investigate on-chip Ku-band RF isolation and performance.

Product Support Engineer - Tesla, Inc. in Palo Alto, CA February 2017 - August 2019

- Validated and maintained Tesla's Superchargers, a global electric vehicle charging network.
- Created an automation platform for engineers with Python and Supercharger telemetry to replace manual diagnostics, leading to improved customer experience and enabling rapid expansion of the network.

NPI Electrical Engineer - Internship at Keysight Technologies in Santa Rosa, CA June - August 2015

Projects and Activities

D-band 4-Element Receiver Array with Dynamic LO Power Tradeoff - at UC Santa Barbara Present

- Designed an array IQ receiver chip for 110-170 GHz in 90-nm SiGe BICMOS to demonstrate LO power adaptation.
- Implemented antenna array and full module packaging with embedded controls to be driven with USB interface.

"A 170-260 GHz SiGe Frequency Doubler with ... 13-dB Input Power Range" EuMIC 2024

- Designed a doubler that demonstrates bias feedback to provide the optimum performance across power.

"A 185-GHz Low-Noise Amplifier Using a 35-nm InP HEMT Process" MWTL 2024

- Designed a LNA in a new technology using noise measure techniques and published the first compression measurements.

High Frequency Transistorized Function Generator - Personal Project January 2017

- Designed and fabricated a credit card-sized 40 MHz function generator made with 86 discrete transistors.

Formula SAE Student Electric - Race Car Design Team at UC Davis September 2013 - June 2015

Skills

Hardware

- Electronics design: mmWave RFIC, system packaging on PCB, and embedded systems.
- Use of oscilloscopes, signal generators, network analyzers, spectrum analyzers, etc. to verify circuits.
- Circuit design and layout with, Keysight ADS, Cadence Virtuoso, Microwave Office, Momentum, EMX, and HFSS.

Software

- Python, C/C++, BASH, MATLAB, SQL, Git, Docker.
- Software development for embedded systems, databases, and distributed compute.
- Software development with issue life-cycles, unit testing, continuous integration, and version control.