2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) | 979-8-3315-4124-8/24/$31.00 ©2024 IEEE | DOI: 10.1109/BCICTS59662.2024.10745700

A D-band SiGe Subharmonic Downconverter with Dynamic Conversion Gain and Fixed Input Compression

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***Abstract*—A fourth subharmonic downconverter operates with a bandwidth of 123-158 GHz and incorporates bias feedback to control the conversion gain over a large LO power range. A push-pull frequency multiplier achieves a high multiplication factor (X4) without sacrificing the additional area or power of a cascaded multiplier chain. Wide bandwidth is achieved by use of a sub-quarter-wavelength (SQWL) balun and an inductively-peaked transimpedance amplifier (TIA). The downconverter is realized in a 90-nm SiGe BiCMOS technology and has a peak conversion gain 7.5 dB at 155 GHz with -5 dBm of LO power at 35 GHz while consuming a maximum 55 mW of DC power and 0.196 mm^2 of area. The minimum 1-dB input compression power (P1dB) at 155 GHz is -15 dBm. Compared to earlier work, this paper demonstrates a higher LO multiplication factor with lower LO power requirements and over 20 dB of dynamic gain control while having the same peak power consumption and a 1.9 dB/dB conversion gain to LO power trade-off.**

***Index Terms*—D-band, millimeter wave, subharmonic mixer, feedback, frequency multiplier, power detection, silicon germanium (SiGe), BiCMOS, HBT**

I. Introduction

Wireless systems for sensing and communication networks are under increasing demand to provide the fusion of the radar and radio into a single hardware platform to cooperatively take advantage of the wide spectrum availability in the frequency bands from mm-wave up to THz [1]. The cooperation enhances communication by spatial localization and improves radar by distributed coordination in a dynamic channel environments with a MIMO system. However, the power consumption of transmit and receive arrays increases at higher frequency and becomes prohibitive in applications such as handsets where the power budget is limiting [2].

Fig. 1(a) illustrates a single receive channel of a MIMO array, which distributes LO power to each mixer with a variable-gain amplifier (VGA) in the intermediate frequency (IF). Millimeter-wave receiver circuitry typically consumes more power than circuits at lower frequencies. In addition to low noise amplifiers (LNA) having lower gain per stage above 100 GHz, the receiver needs large frequency multiplication factors with high local oscillator (LO) powers to drive the mixer, substantially contributing to power consumption. Conventional receiver arrays use a single saturating LO power to drive a mixer since the relationship between the input and output power of a conventional frequency multiplier circuit is nonlinear and difficult to control. This constant LO power assures relatively high DC power consumption.

This work was supported by the Semiconductor Research Corporation (SRC) under the JUMP 2.0 program, CogniSense, and pSemi Corporation.

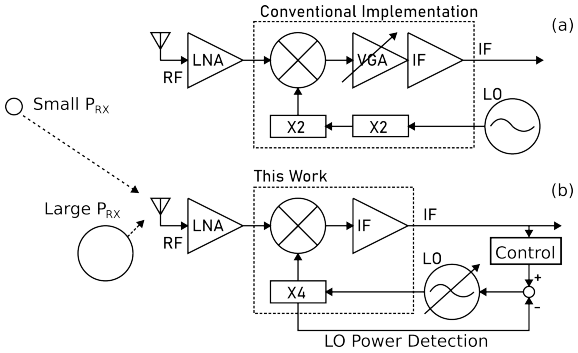
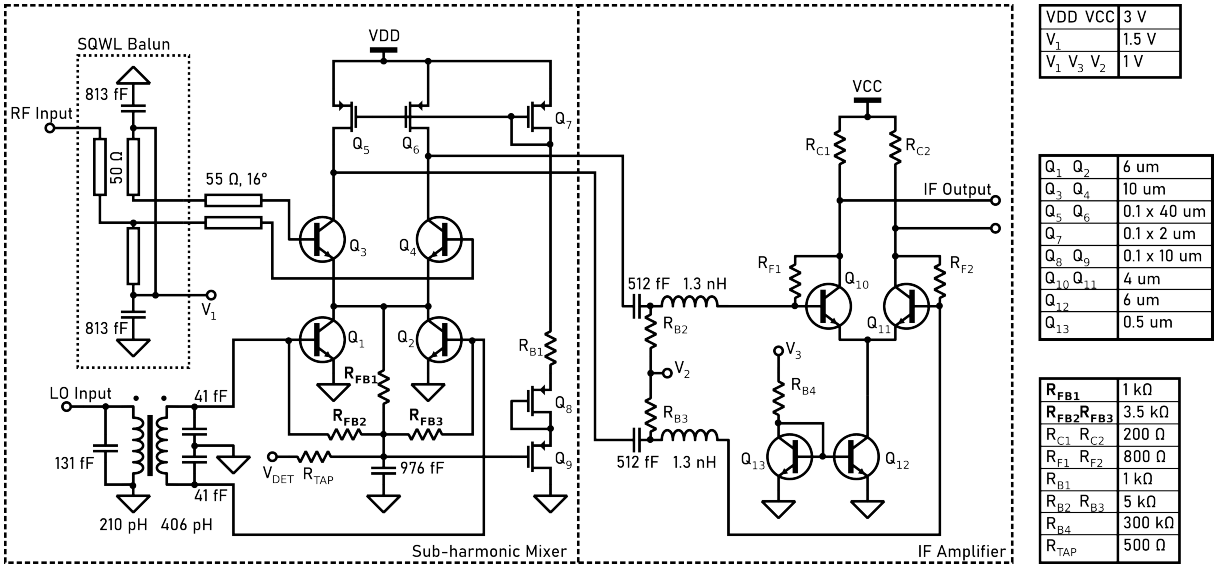


Fig. 1: (a) Conventional and (b) proposed downconversion system element in a dynamic channel environment.

This paper explores several circuit techniques that reduce power consumption in the LO chain to improve energy efficiency in the array receiver, especially for adapting to dynamic channel environments where the received power P_{RX} varies by target or transmitter distance. To accommodate high dynamic range of the received radar signal, the conversion gain of the mixer is adjusted by saving LO power, eliminating additional variable-gain amplifiers in the signal path and decreasing system power consumption and circuit area.

In this work, a subharmonic downconverter is realized in a 90-nm SiGe BiCMOS process for D-band (110-170 GHz), shown in Fig. 1(b). Bias-feedback circuitry adapts the LO current to enable gain control in the mixer through the LO power. The design adjusts the fourth harmonic content in a push-pull frequency multiplier to achieve a high multiplication factor without sacrificing additional area or power for a cascaded multiplier chain. Additionally, the design inherently contains an LO power detector to monitor and support closed-loop gain control in a system. Section II presents the subharmonic downconverter circuit and the details of the fourth harmonic push-pull circuit are presented in Section III. Section IV presents measurements of the wideband downconverter.



VDD VCC	3 V
V_1	1.5 V
V_1 V_3 V_2	1 V

Q_1 Q_2	6 um
Q_3 Q_4	10 um
Q_5 Q_6	0.1 x 40 um
Q_7	0.1 x 2 um
Q_8 Q_9	0.1 x 10 um
Q_{10} Q_{11}	4 um
Q_{12}	6 um
Q_{13}	0.5 um

R_{FB1}	1 kΩ
R_{FB2} R_{FB3}	3.5 kΩ
R_{C1} R_{C2}	200 Ω
R_{F1} R_{F2}	800 Ω
R_{B1}	1 kΩ
R_{B2} R_{B3}	5 kΩ
R_{B4}	300 kΩ
R_{TAP}	500 Ω

Fig. 2: Schematic of proposed downconverter with bias feedback and dynamic conversion gain.

II. Subharmonic-based Downconverter

The circuit of the downconverter is shown in Fig. 2 and is realized with a push-pull frequency multiplier generating a fourth harmonic to a single-balanced mixer. The RF input is split through a balun in the single balanced mixer.

The first proposed innovation is to replace the tail current source of the mixer with a push-pull frequency multiplier. With the active mixer directly attached the multiplier, the transistors form a cascode structure which increases conversion gain by suppressing the Miller effect and saves power by reusing the current for the multiplier in the mixer. The load of the mixer is a pair of saturated PFETs that are biased through a common mode connection to the frequency multiplier, with their drain bias point set by device parasitics.

The LO path includes a transformer balun that produces a differential LO to drive a pair of HBTs that generate the fourth harmonic. Since the LO is presented in the common mode in the mixer, it is suppressed by using differential mode in the RF path, through Q_3 and Q_4, and the IF path, though Q_{10} and Q_{11}. In the IF path, A differential wideband TIA with inductive peaking buffers and amplifies the converted signal from the mixer into difference voltage outputs.

The second proposed innovation is use of resistive feedback at the common node of the mixer to bias the multiplying transistors Q_1 and Q_2. The biasing supports frequency generation over a wide range of LO powers, enabling adjustable conversion gain at the mixer.

III. Dynamic Subharmonic Generation

A typical push-pull frequency multiplier or sub-harmonic mixer uses a second harmonic [3]. The proposed subharmonic mixer utilizes the fourth harmonic from a push-pull frequency multiplier implemented with transistors Q_1 and Q_2, shown in Fig. 2. The harmonic content of the combined collector currents I_C of Q_1 and Q_2 depend on the conduction cycle, which is controlled through their base voltage bias.

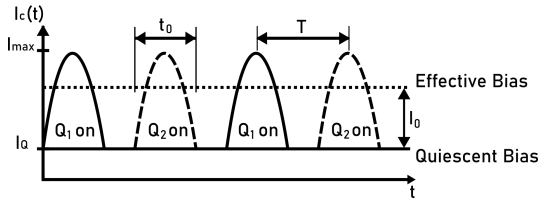


Fig. 3: Instantaneous output current from a push pull frequency multiplier stage and its time-average impact on bias.

Modeling the collector current as a half-wave rectified sinusoidal pulse train, illustrated in Fig. 3, the Fourier series expansion presents the current harmonics as in Eq. 1 [4] [5].

$$I_n = I_{max}\frac{4t_0}{\pi T}\begin{cases}1 & \text{, if } n=0\\ 2\cdot\left|\frac{\cos\left(\frac{n\pi t_0}{T}\right)}{1-\left(\frac{n\pi t_0}{T}\right)^2}\right| & \text{, if } n \text{ even}\\ 0 & \text{, if } n \text{ odd}\end{cases} \quad (1)$$

A maximum fourth harmonic current of $0.27\cdot I_{max}$ is obtained with conduction cycle $t_0/T = 0.17$. The ratio between the maximum harmonic current and generated DC current is $I_4/I_0 = 1.25$ for the maximum fourth harmonic. In this work, the conduction cycle is set by optimizing the combined resistance of $R_{FB1,2,3}$ for maximum conversion gain or fourth harmonic current. Despite the lower current in the fourth harmonic compared to the second, the ratio between the desired harmonic and generated DC current is fixed relative to the second or fourth harmonic. Thus, configuring a push-pull frequency multiplier for the fourth harmonic generation does not sacrifice DC power consumption.

In a typical multiplier, the bases of Q_1 and Q_2 are biased with a static voltage which is tuned for a particular LO input

power [4]. This method, however, does not provide the best bias across input powers. As shown by the DC current where $n = 0$ in Eq. (1), the average effective output current of Q_1 and Q_2 is $I_C = I_Q + I_0$, where I_Q is the quiescent bias current and I_0 is the additional current generated from the rectification of the input sinusoid. The additional current causes the transconductance to change with output power, a source of nonlinear gain in the multiplier.

To counteract the current variation, large feedback resistances, R_{FB1}, R_{FB2}, and R_{FB3}, from the collectors of Q_1 and Q_2 set the base bias and to compensate for the additional current created by the output waveform at DC. If we consider $V_{BE1,2} \approx V_{BE3,4}$, and $I_{C3,4} \approx I_{C1,2}$,

$$I_{C3,4} = \beta_{1,2} \frac{V_1 - 2V_{BE}}{R_{FB1} + R_{FB2} || R_{FB3}} \tag{2}$$

Thus, the feedback resistance reduces the influence from the additional rectified DC current. Although feedback compensates for the additional rectified current, the current change is not completely cancelled due to variations in the effective time-averaged $\beta_{1,2}$ over power variation. The feedback bias allows for a gradual change in gain over a wider range of LO input powers compared to the static bias approach, as shown in Fig. 4. The conversion gain remains higher over reduced LO power and improves the robustness of the circuit to LO power variation. With a -6 dB LO power backoff from peak conversion gain, the feedback biased circuit has 17 dB more gain than the static biased version. Additionally, the feedback network provides voltage V_{DET} corresponding to output current, enabling monitoring of conversion gain.

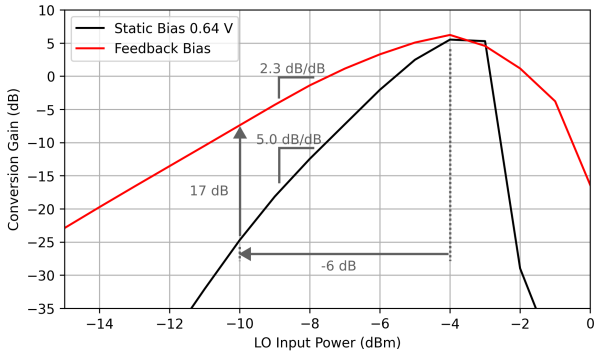


Fig. 4: Simulated effect of bias feedback in the downconverter, compared to a typical static bias approach.

IV. Measurement Results

Measurements were made on the subharmonic downconverter shown in Fig. 5 using a 3-V supply on VDD and VCC, with quiescent currents of 8.6 mA to the IF amplifier and 0.9 mA to the mixer. A VDI PM5B power meter was used as the power reference for calibrating the D-band extender as the RF input source, and output leveling was performed with an electronically controlled variable attenuator. DC blocks were used with an oscilloscope to measure the differential IF. The LO was directly provided by a signal generator.

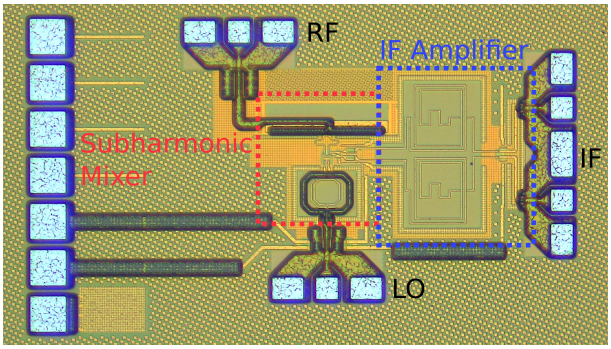


Fig. 5: Micrograph of downconverter with dimensions of 1.18 mm x 0.68 mm and core area of 0.56 mm x 0.35 mm.

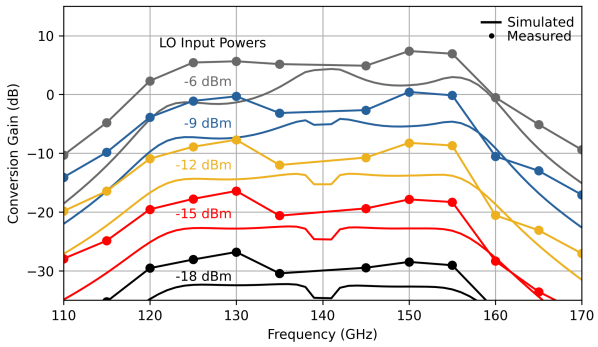
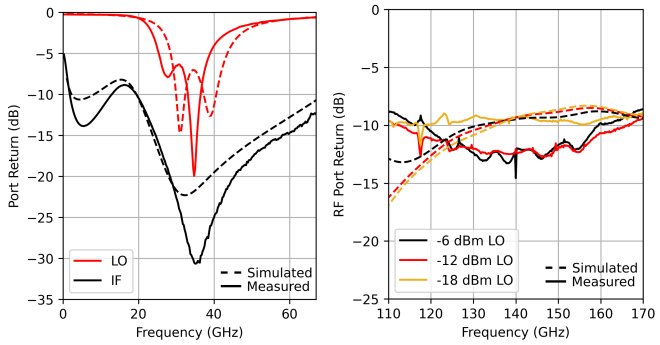


Fig. 6: Conversion gain over RF frequency across LO powers on a 140 GHz LO, with -24 dBm of RF input power.

The downconverter's conversion gain was measured across a range of LO powers across frequency with results in agreement with the simulation, shown in Fig. 6. The supplied RF input power was -24 dBm and the LO was supplied at 35 GHz for an effective 140 GHz LO at the mixer. With -6 dBm of LO power, the maximum gain across the band was 7.4 dB at 150 GHz with a 3-dB bandwidth of 35 GHz, spanning 123 GHz to 158 GHz. The measured gain of the down-converter is higher than simulated due to a frequency shift in the return loss of the LO, shown in Fig. 7a. The shift lead to a better match at the LO frequency and more delivered LO power. Additionally the RF return loss, shown in Fig. 7b, was close to simulation with slightly better return loss.

Measurements at 155 GHz with a 140 GHz LO confirming the relationship between LO power and resulting conversion gain are shown in Fig. 8. The downconverter's conversion gain was controlled with LO power at 1.9 dB/dB, leading to the ability to reliably trade off between conversion gain and power consumption. A maximum gain of 7.5 dB was observed at 155 GHz with -5 dBm of input power, while consuming 55 mW of DC power. By backing off LO power from -5 dBm to -11 dBm to decrease gain from the peak by 11.7 dB, DC power consumption was decreased by 19 mW, 35% less than consumption at peak gain.

The LO power detection voltage V_{DET} was measured to be close to simulation, shown in Fig. 9. The power detection



(a) (b)

Fig. 7: Port return S-parameters for (a) single-ended LO with differential IF and (b) RF port with varying LO powers.

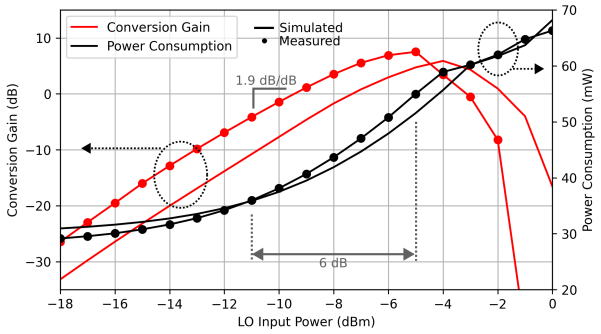


Fig. 8: Conversion gain and DC power consumption at 155 GHz RF and 140 GHz LO, with -24 dBm of RF input power.

is predictable and monotonic, making it suitable for use in system level control of LO power. With a 155 GHz RF and 140 GHz LO, the lowest demonstrated 1-dB input compression is -15 dBm, shown in Fig. 9. With less than -4 dBm LO power, the input compression remains fixed between -15 dBm and -10 dBm while the output compression changes with LO power.

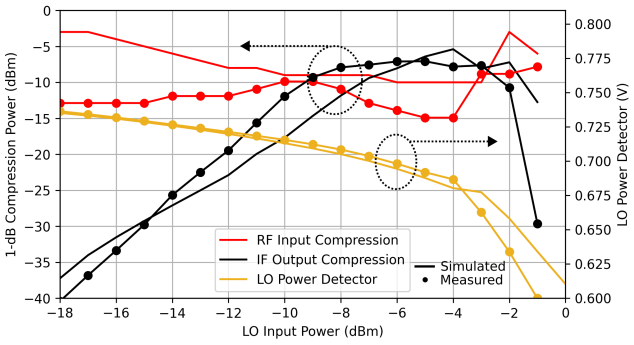


Fig. 9: 1-dB input and output power compression at 155 GHz RF and 140 GHz LO with LO power detection voltage (V_{DET}).

TABLE I: Comparison with Downconverters Above 100 GHz

Reference	This Work	[3]	[6]	[7]
Technology	90-nm SiGe	90-nm SiGe	130-nm SiGe	130-nm SiGe
Subharmonic	4	2	2	1
f_C (GHz)	140	136	121	140
BW_{3dB} (GHz)	35	38	>14	35
Gain (dB)	7.5	5.1	4	32
P_{i1dB} (dBm)	-15	-7	-	-41
Noise Figure (dB)	21.7*	-	23*	9.5
LO (dBm)	-5	2	7	-2
P_{DC} (mW)	55	51	89	65
Area (mm^2)	0.196†	0.450†	-	0.191†

* Simulated † Area without pads.

V. Conclusion

A wideband fourth subharmonic D-band downconverter is presented with bias feedback to enable adaptation of performance and power consumption through LO power. The circuit exploits the fourth harmonic content of a push-pull frequency multiplier to achieve a high multiplication factor without sacrificing additional area, power consumption, or LO power requirement for a cascaded multiplier chain, exemplified in Table I. The adaptation makes this circuit suitable for applications of joint radar and radio systems in dynamic environments.

Acknowledgment

This work was supported by the Semiconductor Research Corporation (SRC) under the JUMP 2.0 program CogniSense and pSemi Corporation. The authors appreciate the support of GlobalFoundries for access to the 9HP+ process technology.

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