A 170-260 GHz SiGe Frequency Doubler with 5-dBm Output Power and 13-dB Input Power Range

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Abstract — **A frequency doubler in a 90-nm SiGe BiCMOS technology operates over 170-260 GHz and incorporates bias feedback to maintain fixed gain over a wider input power range. With a peak conversion gain of -2.0 dB at 190 GHz, the doubler's bias feedback maintains conversion gain variation to less than 3 dB over a 13-dB input power range. The measured output power is greater than -3.3 dBm over 170-260 GHz, with a peak value of 5.8 dBm and 7.2% efficiency at 206 GHz. The total chip area is 0.074 mm^2 and is much more compact than typical doublers.**

Keywords — **G-band, millimeter wave, frequency multiplier, silicon germanium (SiGe), BiCMOS, HBT, feedback, linearization**

I. INTRODUCTION

Wireless backhaul networks are under increasing demand to provide fiber-like data rates, spurring interest for the wide spectrum availability in the 100-300 GHz frequency band [1]. However, the power consumption of transmit and receive arrays increases at higher frequency and the reduced area occupied by a single element creates a prohibitive thermal flux in small antenna apertures [2]. The LO chain, illustrated in Fig. 1, multiplies a reference frequency and amplifies the LO signal for frequency conversion. Based on the frequency multiplication factor and the LO power required to drive the mixer into saturation, the LO chain above 100 GHz places significant demands on the circuit power consumption. Circuit techniques that reduce power consumption in the LO chain support more energy efficiency in the transmitter and receiver.

As wireless link requirements change, the conversion gain of the mixer can be adjusted with LO power, eliminating other variable-gain amplifiers in beamforming applications, further decreasing system power consumption and area. A variable power frequency multiplier can adaptively respond to link and power requirements.

The basic frequency multiplier is illustrated in Fig. 1a and uses push-pull transistors operating in class B or C mode. To increase the conversion of the input frequency f_0 to a $2f_0$, the doubler might include a bypassed resistive degeneration or use a bypassed tail current [3] as shown in Fig. 1b. These methods consume voltage headroom, which require either higher voltage operation or sacrificing maximum output power in a low voltage system.

In this work, a G-band (170-260 GHz) frequency doubler is realized in a 90-nm SiGe BiCMOS process. Bias-feedback circuitry adapts the conversion gain over a wide range of input powers. At 190 GHz, the doubler has a peak gain of -2.0

dB and remains within 3 dB of the peak gain over a 13 dB input power range. The doubler without pads has compact dimensions of 95 μm x 135 μm, which makes it suitable for an LO chain in an array. In Section II, we review the operation of the push-pull frequency doubler to describe the sensitivity to input power variation. Section III describes the proposed bias-feedback circuit. Section IV presents the measurements between 170 and 260 GHz.
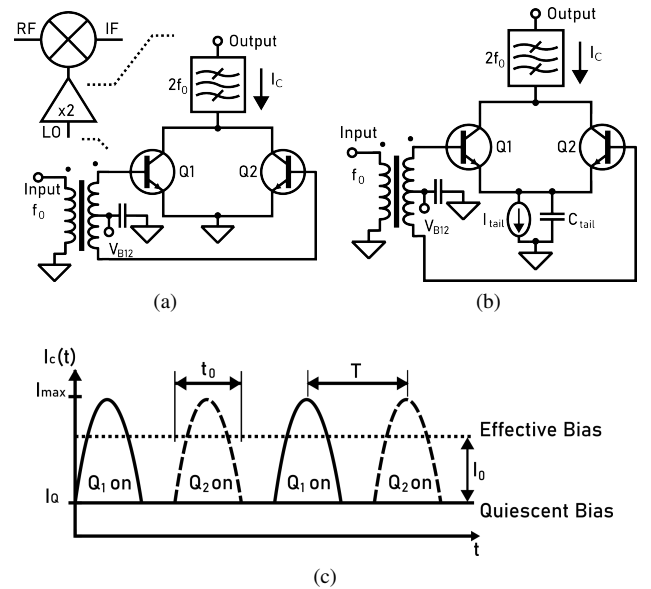

Fig. 1. Doublers using (a) static voltage biasing and (b) degenerated tail biasing with application in a frequency conversion system. (c) Instantaneous output current from a frequency doubler and its time-average impact on bias.

II. PUSH-PULL FREQUENCY DOUBLERS

The schematic of the doubler in this work is presented in Fig. 2. Heterojunction bipolar transistors (HBTs) Q1 and Q2 form an active push-pull doubler, while Q3 forms a common-base amplifier to buffer the current and to maintain bias conditions. The current flowing through Q3 is reused by the push-pull doubler, saving power compared to an AC-coupled connection to a power amplifier stage.

In a typical doubler, the bases of Q1 and Q2 are biased with a static voltage V_{B12}, shown in Fig. 1a. The frequency doubler creates an output waveform that contains the desired second harmonic of the sinusoidal input frequency by rectifying a balanced signal from the input balun. Using the Fourier series expansion of the output as a current cosine pulse train, we

observe that the output waveform creates additional DC current in addition to the output harmonics of interest [4][5]. The average effective output current is $I_C = I_Q + I_0$, where I_Q is the quiescent bias current and I_0 is the additional current generated from the rectification of the input sinusoid.

This additional current from the output waveform changes with input voltage v_i on the bases of Q1 and Q2. The AC output current can be estimated from the linearization of the small-signal collector current i_C, based on the DC collector current I_C through the devices, e.g. $i_C = G_m(I_C)v_i$, where G_m is the time average effective transconductance. The bias shift is calculated from

$$I_0 = \frac{4t_0}{\pi T} i_C = \frac{4t_0}{\pi T} G_m(I_Q + I_0)v_i. \quad (1)$$

Since the transistor transconductance is sensitive to additional rectified current, i.e. $G_m(I_Q + I_0)$, the inherently non-linear transconductance causes the conversion gain for a static bias doubler to change with the input power. The result is that the frequency multiplier would have high gain only within a narrow range of input powers, and the sensitivity to input power diminishes the ability to control and deliver a desired output power in a system. Using a bypassed tail current source on Q1 and Q2, as shown in Fig. 1b, can force the DC current to be constant at the expense of power consumption [3].
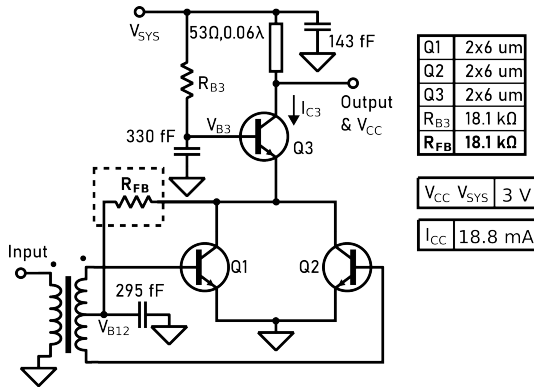

Fig. 2. Schematic of the frequency doubler in this work with bias-feedback adaptation resistor R_{FB}. V_{CC} is provided by an output bias tee for this test structure, while V_{SYS} would be the supply for system integration.

III. PROPOSED ADAPTIVE BIAS FEEDBACK

We propose a resistive feedback technique within frequency doublers to change base bias voltage (V_{B1} and V_{B2}), which mitigates the decrease in the bias current with decreasing input power to maintain gain. Transistor Q3 not only provides amplification but also output current detection, while resistor R_{FB} implements the feedback for adaptation. This technique does not have the drawback of increased power consumption from additional components for bias control.

The time average V_{BE3} decreases in response to a decrease in effective bias current I_C caused by the output waveform. The voltage signal from V_{BE3} is fed-back through resistor R_{FB} into the bases of Q1 and Q2 to compensate for the change in DC bias current. The AC component is not significantly

affected by the resistive feedback, because the feedback resistance is large compared to the emitter impedance of Q3. In the following DC analysis of the biasing system, Q1 and Q2 are combined into an equivalent Q12, because they are shorted together at DC. The Q3 base voltage, $V_{B3} = V_{CC} - \frac{I_{C3}}{\beta_3}R_{B3}$, changes with the collector current. In this work, V_{B3} is set to 2.2 V to maximize output voltage swing. If we consider $V_{BE3} \approx V_{BE12}$ and $I_{C3} \approx I_{C12}$,

$$I_{C3} = \beta_{12}\frac{V_{B3} - 2V_{BE}}{R_{FB}} = \frac{V_{CC} - 2V_{BE}}{R_{FB}/\beta_{12} + R_{B3}/\beta_3}. \quad (2)$$

In this manner, the bias current for the frequency doubler is set by V_{CC} and a selection of R_{FB} and R_{B3}, reducing the influence from the additional rectified DC current through V_{BE}. Instead of being dependent on a non-linear $G_m(I_Q + I_0)$, the gain with resistive feedback is dependent on $G_m(I_{C3})$.

The effect of the input power on gain with this bias-feedback adaptation is illustrated in Fig. 3, where the conversion gain varies by less than 3 dB from the peak value over a 14-dB input power range, compared to only 6-dB input power range in the static biasing case illustrated in the black curves. Fig. 4 plots the output power variation and DC current for the static and bias-feedback doubler circuit. While the static biasing produces similar peak output power as the feedback case, static biasing is strongly dependent on the input power with rapidly changing current consumption. The proposed bias-feedback circuit maintains bias current across a large input power range and delivers the same saturated power as a static-bias circuit with a bias tuned for a particular input power to deliver maximum power.
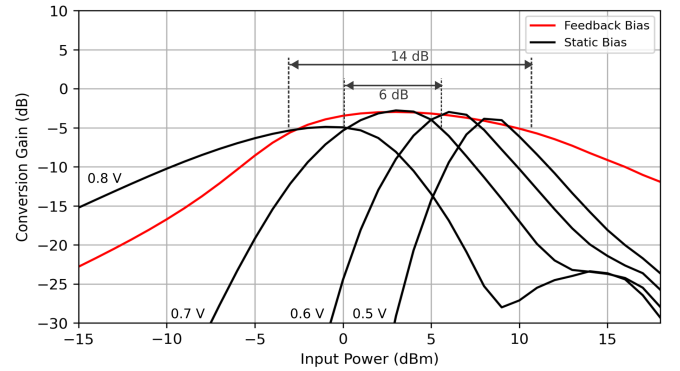

Fig. 3. Simulated comparison on conversion gain between feedback biased and static biased frequency doubler at 210 GHz. Static bias voltages are applied at V_{B12} with no feedback resistor, as shown in Fig 1a.

IV. MEASUREMENTS AND RESULTS

Measurements were made on the bias-feedback frequency doubler with a 3-V supply through an output probe bias tee, supplying 14.4 mA of quiescent current on V_{CC}, while V_{SYS} is open and not implemented for this test structure. Because of the wide output bandwidth of the doubler, the measurement was split into two frequency ranges. Fig. 5 shows the power measurement setup at the higher D-band input range with the
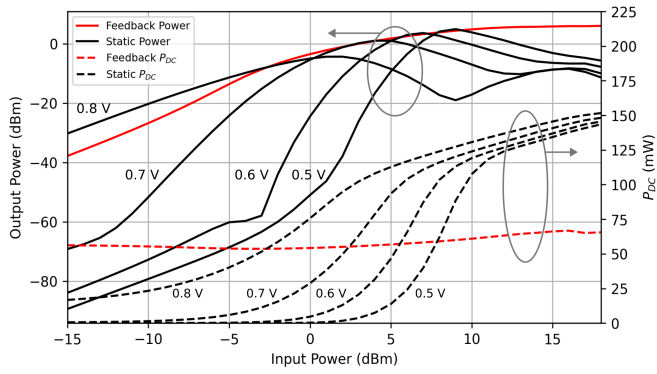
Fig. 4. Simulated comparison on output power and power consumption between feedback biased and static biased frequency doubler at 210 GHz.
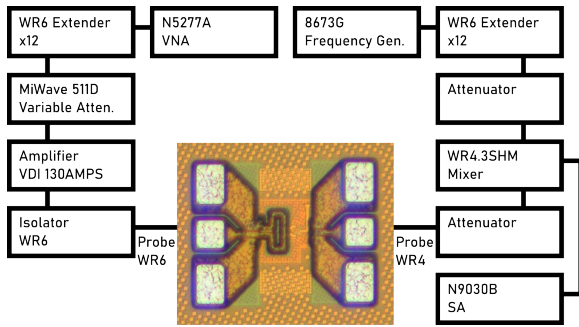

Fig. 5. Measurement setup with D-band input and micrograph of G-band doubler with dimensions 0.095 mm x 0.135 mm without pads and 0.303 mm x 0.243 mm with pads.
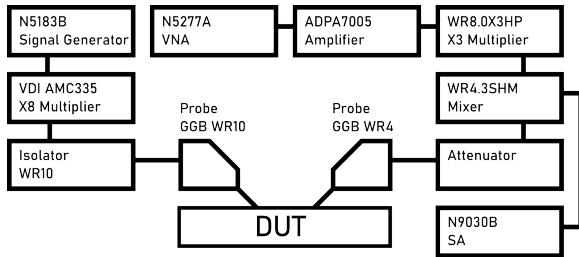

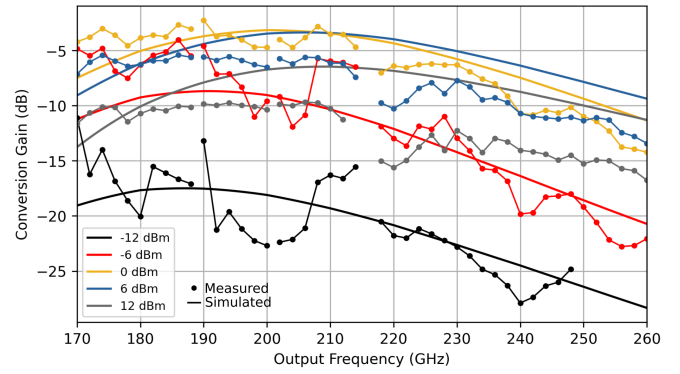Fig. 6. Measurement setup with W-Band input

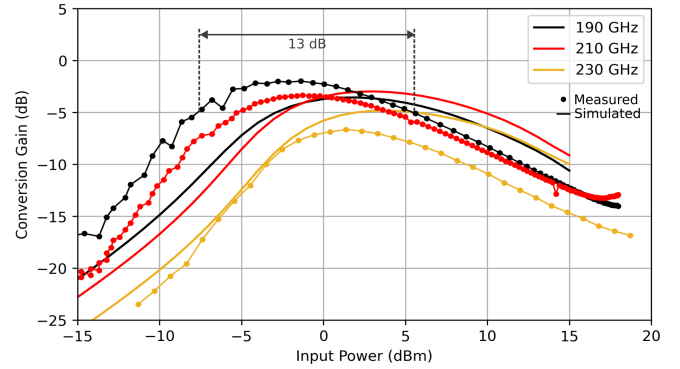Fig. 7. Measured gains over frequency with a selected range of input powers.

Fig. 8. Measured gains across input powers.

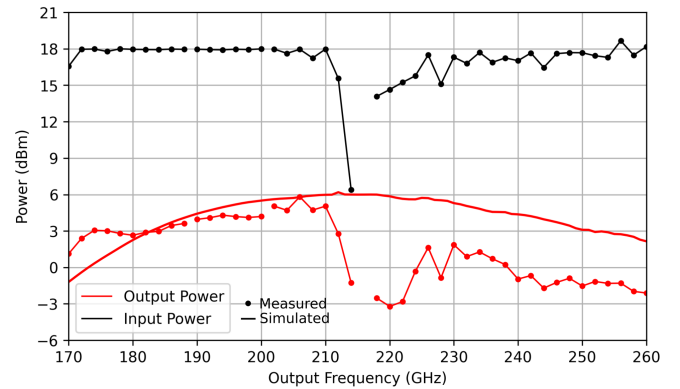Fig. 9. Maximum measured output power with associated input power across frequency.

chip micrograph, while Fig. 6 shows setup at the lower W-band input range. The setup is calibrated with a VDI PM5B power meter for the input source across its power range and the output detection. The output is measured by down-converting the output spectrum of the doubler to a spectrum analyzer. The detected narrow-band power is adjusted by using the power meter as the primary calibration reference.

The doubler's output gain is measured across a range of input powers across frequency with results in agreement with simulation as shown in Fig. 7. In Fig. 8, the frequency doubler exhibits the predicted gain flatness across a wide range of input powers. At 190 GHz, the doubler has 13.0 dB of 3-dB input power range, where the gain is within 3 dB of the peak gain at -2.0 dB, exemplifying the primary effect of adapting the bias of the doubler. Fig. 9 shows that saturated output power relationship is close to simulation, despite being limited by

equipment input power. The gain bandwidth with a 12 dBm input is 170-218 GHz. The peak output power is 5.8 dBm, an equivalent 1.2 V_{PP} on 50 Ω, at 206 GHz with 18.0 dBm of input power. The doubler delivers more than -3.3 dBm over 170-260 GHz.

Fig. 10 shows a trend of flatness in power consumption, indicating that the bias feedback is controlling bias current across a wide range of input powers, despite an offset from simulation. The target quiescent current was 18.8 mA while the measured current was 14.4 mA. The current discrepancy could be due to poor tolerance of the small, high sheet resistance

Table 1. Performance Summary of Frequency Multipliers Above 100 GHz

Ref.	This Work	[6]	[7]	[8]	[9]	[10]
Technology	90-nm SiGe BiCMOS	55-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	90-nm SiGe BiCMOS	45-nm SOI CMOS
Type	Doubler + Amplifier	Doubler + Amplifier	Doubler + Amplifier	Doubler	Doubler	Doubler
Output Frequency (GHz)	206	245	152	204	228	150
BW_{3dB} (GHz)	170-218 ‡	220-260	138-170	165-230	200-245	135-160
Peak Gain (dB)	-2.0 §	10.9	4.9	-8.6	-15	-3
P_{sat} (dBm)	5.8	5.5	5.6	-2.6	2	3.5
P_{DC} (mW)	53	240	36	39	35	25
Efficiency (%)	7.2	9.5	10.9	1.4	4.5	9.0
Area (mm^2)	0.013†, 0.074	0.253	0.485	0.090	0.246	0.441
3-dB Gain Input Range (dB)	13.0 §	6 *	9 *	>7 *	>6 *	11 *

* Estimated from plot. † Area without pads. ‡ Lower end limited by G-band measurement, with 12 dBm input. § At 190 GHz.

polysilicon resistors in the design, in addition to some V_{BE} variation. With peak output power at 206 GHz the collector efficiency is 7.2%, while DC consumption is 53 mW. As shown by Table 1, the bias adaptation in this work enables higher output power over a wide input power range without significant sacrifice of other performance attributes.
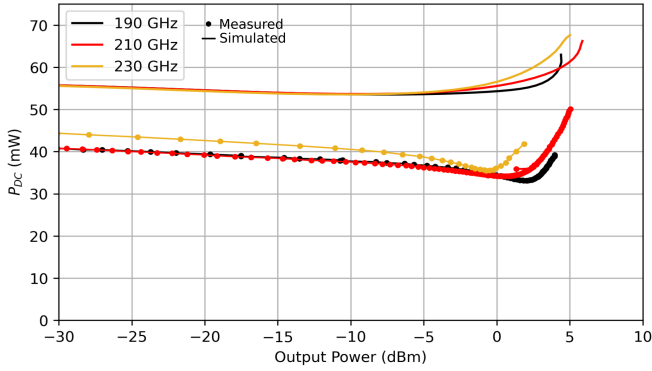

Fig. 10. Measured DC supply power consumption across output power

V. CONCLUSION

A G-band frequency doubler in 90-nm SiGe BiCMOS technology with a novel resistive feedback adaptation is presented. With a peak gain of -2.0 dB measured at 190 GHz and a 13-dB input power range defined by the 3-dB gain variation, this doubler demonstrates the benefit of the adaptive biasing with no penalty in power consumption, area, or output power. The doubler delivers more than -3.3 dBm over 170-260 GHz, with a peak of 5.8 dBm. These results strongly support the potential for implementing efficient LO multiplier chains in adaptive transceivers that can take advantage of variable LO power.

ACKNOWLEDGMENT

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