A 185-GHz Low-Noise Amplifier Using a 35-nm InP HEMT Process

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***Abstract*— We present a four-stage, 185-GHz indium phosphide (InP) high electron mobility transistor (HEMT) low-noise amplifier (LNA) implemented with coplanar waveguide (CPW) inductive degeneration and designed with a procedure using noise measure. At 194 GHz, the LNA exhibits a peak 19.6 dB of gain with an input 1-dB compression point (P1dB) of −23.7 dBm at 190 GHz. To our knowledge, this is the first P1dB measurement over frequency for this technology. Over a frequency range covering 175 to 200 GHz, the LNA exhibits noise figure (NF) ranging from 9.8 to 11.4 dB. The amplifier consumes 22 mW of power and 0.77 mm^2 of area. Additionally, a novel figure of merit (FoM) based on noise measure is proposed to evaluate designs across technologies independent of the number of stages.**

***Index Terms*— 1-DB compression point (P1DB), figure of merit (FoM), *G*-band, high electron mobility transistor (HEMT), indium phosphide (InP), low-noise amplifier (LNA), millimeter wave.**

I. Introduction

WIRELESS backhaul networks are under increasing demand to provide fiber-rate data rates driven by emerging 5G systems at 3.5 and 6 GHz, and millimeter-wave bands. Following this trend, research interest has been high in developing the next generation of communication, imaging, and detection systems that will take advantage of the spectrum and ability to perform array scaling at 100–300 GHz. For long-range communication links, it is attractive to combine CMOS with external low-noise amplifiers in technologies such as indium phosphide (InP) high electron mobility transistor (HEMT) for better receiver sensitivity and reduced demand for transmit power [1].

In this work, a 185-GHz InP HEMT low-noise amplifier (LNA) is presented with compact form suitable for heterogenous integration with CMOS in a multichannel system as illustrated in Fig. 1(a). The LNA design procedure uses noise measure based on inductive degeneration for simultaneous noise and gain matching. With dimensions of 1285×600 μm, it can be tiled along its width to fit under the free-space half-wavelength at 210 GHz, which is 714 μm. This article presents the design procedure based on noise measure, noise measurements, and the first P1dB measurements across frequency for this technology.

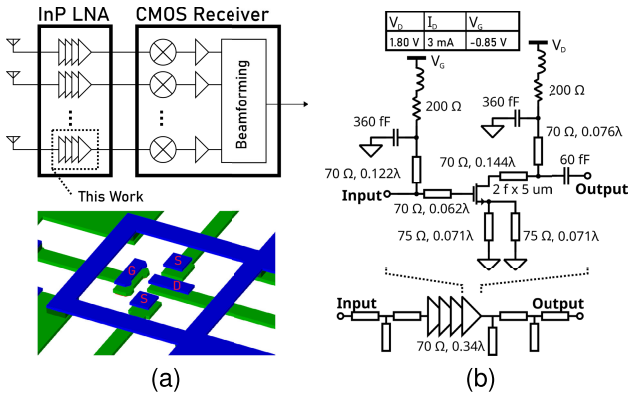

Fig. 1. (a) Diagram of heterogenous integration between an InP LNA and a CMOS receiver in a multichannel system and transistor layout with (b) schematic of a single stage of this work's four-stage LNA. All stages in the amplifier are identical.

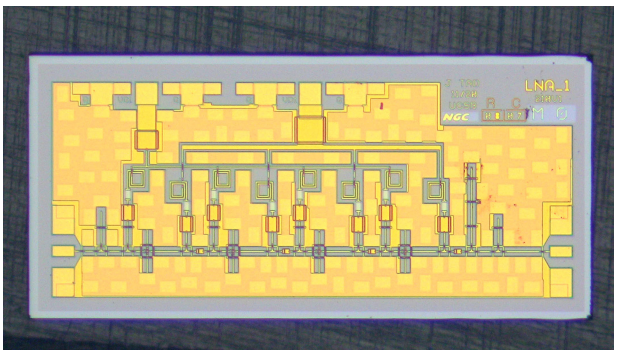

Fig. 2. Micrograph of the four–stage low-noise amplifier. The total die dimensions are 1285×600 μm with a total area of 0.77 mm^2.

II. Design

The LNA, shown in Fig. 2, was designed and fabricated based on a Northrop Grumman 35-nm InP HEMT process. The process has a single metal layer for interconnect with a top air-bridge metal. Resistors are available as thin films at 20 and 100 Ω/□ with 600 pF/mm^2 capacitors. At 300 mA/mm, the HEMT has a maximum 866-GHz unity power gain frequency (f_{max}) under a nominal drain voltage of 1.2 V. With a substrate thickness of 51 μm, the coplanar layout was chosen over the microstrip alternative to achieve practical line impedance and compatibility with packaging [2].

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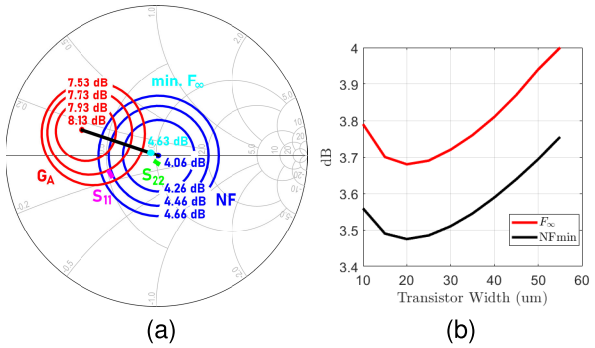

Fig. 3. (a) Minimum noise measure impedance match with a single LNA stage in simulation at 210 GHz. (b) Minimum F_∞ over two-finger transistor widths at 300 mA/mm.

A. Noise Measure Design Procedure

A minimum noise measure technique was used to optimize and perform simultaneous power and noise matching. Noise measure M is defined by

$$M = \frac{F-1}{1-1/G_A} \tag{1}$$

where G_A is the available gain and F is the noise factor of the amplifier [3]. The upper bound for an infinite cascade of LNA stages can be represented with noise measure as

$$F_\infty = F + \sum_{k>=1}^{\infty} \frac{(F-1)}{G_A^k} = \frac{F-1}{1-1/G_A} + 1 = M + 1. \tag{2}$$

F_∞ is intrinsic to the underlying transistor since any passive, lossless, and reciprocal additions to implement the transistor into a circuit do not affect this metric [3]. It is more relevant in most applications since a low-noise stage with a low gain is unable to buffer the noise contributions of subsequent stages.

The optimum source impedance to achieve minimum F_∞ was approximately determined in Keysight ADS by finding the impedance between the G_A and noise figure (NF) circle centers that yield the minimum F_∞ as illustrated in Fig. 3(a) using an algorithm from [4]. The external source is matched to present the impedance of minimum F_∞ to the input of the transistor, while the output of the transistor is power matched to the external impedance. In implementation, the input match for the best noise measure is different from a conjugate match, so techniques such as inductive degeneration in this work are used to reduce the gain effects of this difference to achieve the ability to cascade stages while maintaining noise measure performance.

B. Circuit Implementation

In this design, the minimum F_∞ of the chosen two-finger 10 μm transistor at 210 GHz is 3.8 dB. Although the scalable fixed-bias transistor models showed that other sizes had slightly better F_∞, as shown in Fig. 3(b), lossy matching applied to the transistor outweighed the small variations in F_∞ by width. Transistor width was chosen for the matching topology with inductive degeneration, shown in Fig. 1(b). Fig. 3(a) shows that the implementation of the transistor into a single stage of the LNA degrades the F_∞ from 3.8 to 4.6 dB, and then to 5.2 dB with cascade and addition of matched pads in layout.

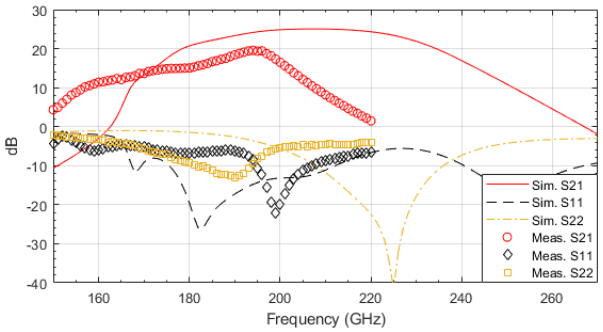

Fig. 4. Measured and simulated S-parameters of the LNA.

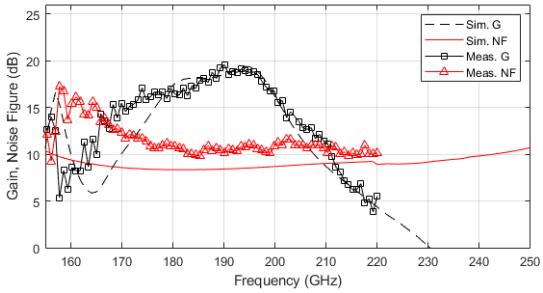

Fig. 5. Measured amplifier noise with adjusted simulation.

III. Measurements and Results

Measurements for gain, power, and noise were made on the LNA with transistor current density at 300 mA/mm, set with a gate voltage of −0.85 V. The transistor in each stage, with a periphery of 10 μm split across two gate fingers, draws 3 mA. The drain bias is set through a ballast resistor that drops the 1.8 V supply to 1.2 V at the transistor. The LNA consumes a total of 12 mA at 1.8 V, resulting in 21.6 mW of dc power consumption.

A. S-Parameter Measurement

S-parameters were measured using a Keysight N5277A network analyzer with 140–220-GHz OML frequency extender modules with WR4 GGB probes. The measured S-parameters are shown in Fig. 4, and the peak small signal gain was 19.6 dB at 194 GHz. Between the simulated and measured S-parameters, a reduction in gain and a downward frequency shift of about 15% from the design was observed. The simulation can be adjusted to approximate measurement by reducing g_m by 5%, increasing R_i by 30 times, reducing R_{DS} by 50%, reducing R_G, R_D, and R_S by 30%, raising C_{gd} by 100%, and adding 8 pH in series to both the gate and the drain of the transistor. The extra inductance may be caused by the removal of the ground plane immediately next to the transistor to fit the coplanar waveguide (CPW) degeneration lines. The impact of this simulation adjustment is shown in Fig. 5. The sample yield is 8.3%, indicating high process variation.

B. Power Measurement

Power measurements were made with a Keysight E8267D signal generator and a VDI WR4.3SGX-M extender, and then the output with a VDI PM5B power meter. From 170 to 210 GHz, the measured gain, shown in Fig. 6(a), was in agreement with the measured S-parameters. The 1-dB

TABLE I
COMPARISON OF RECENTLY PUBLISHED LNA ABOVE 100 GHz

Ref.	Technology	Freq. (GHz)	Gain (dB)	Stages	NF (dB)	Pi1dB (dBm)	P_{DC} (mW)	F_∞ * (dB)	$1/MP_{DC,Stage}$ † (mW^{-1})
[4]	250 nm InP HBT	196-216	13	4	6.8-7.6	-19.1	19.2	7.4	0.047
[4]	250 nm InP HBT	196-216	14.5	2	6.7-8.1	-17.5	9.2	7.5	0.047
[5]	50 nm InP mHEMT	220-325	31	8	5.6-7	-29.3	56	6.3	0.044
[6]	50 nm InP mHEMT	178-185	24.5	5	3.5-4.5	-	24	4.0	0.137
[7]	25 nm InP HEMT	215-225	36	-	3.9-4.5	-	-	4.2	-
[8]	75 nm InP HEMT	180-270	12.5	2	5.3-7	-	18	6.3	0.034
[9]	35 nm InP HEMT	158-220	22	4	4.8-5.2	-	-	5.0	-
[9]	35 nm InP HEMT	164-220	25	3	4.8-5.6	-	-	5.2	-
This work	35 nm InP HEMT	175-200	19.6	4	9.8-11.4	-23.7	22	10.6	0.017

* Calculated with insertion gain $||S_{21}||^2$ and average of the reported range of noise figures.
† Calculated with power consumption per stage, $P_{DC,Stage}$.

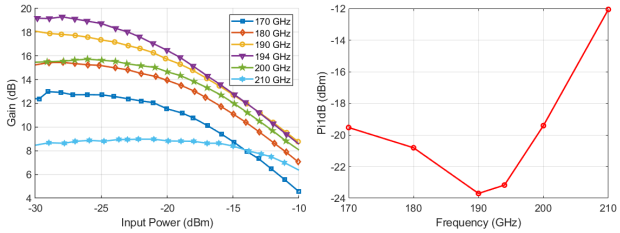

Fig. 6. (a) Measured gain across input power with frequency. (b) Measured 1-dB input power compression point over frequency.

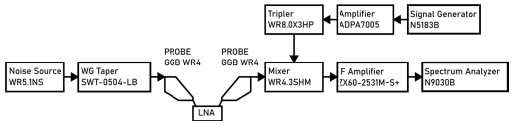

Fig. 7. Noise measurement setup.

input power compression points are plotted in Fig. 6(b). The lowest compression point of −23.7 dBm was measured at 190 GHz with the highest $P_{1\ dB}$ was −12 dBm at 210 GHz. To our knowledge, this is the first P1dB measurement over frequency for this 35-nm InP HEMT technology.

C. Noise Measurement

NF was measured using a VDI WR5.1NS hot-cold noise source and a down-conversion chain, as shown in Fig. 7. Effects of measured probe loss were removed by calculation, since the calibrated reference planes are set to the output of the noise source and input to the down-conversion, using noise source manufacturer excess noise ratio (ENR) data. The noise source has ENRs ranging from 6.0 to 10.9 dB.

The results of the noise measurement are shown in Fig. 5 with the gain and noise from a simulation with the adjusted transistor parameters. The gain derived from the Y-factor noise measurement is close to that of the S-parameter measurements and adjusted simulation. Over 175 to 200 GHz, the amplifier demonstrates NF ranging from 9.8 to 11.4 dB, with the point of lowest noise occurring at 185 GHz. In spite of the adjustment device model to correct the S-parameters, our noise measurements remained significantly higher than the NF predicted from the device model.

Table I compares the current work against the state of the art. F_∞ and $1/MP_{dc,stage}$ are computed using the average NF. Performance is quantified with a novel $1/MP_{dc,stage}$ as a figure of merit (FoM). The FoM represents the noise performance capability of the underlying technology through M and the power consumed to achieve that noise performance through $P_{dc,stage}$. This metric is invariant with the number of stages and is supported by the design theory with noise measure M, used by the design procedure in this work.

IV. CONCLUSION

A four-stage 185-GHz InP HEMT LNA suitable was designed and fabricated. In the first P1dB measurements across frequency for this technology, the amplifier exhibits a P1dB of −23.7 dBm at 190 GHz. Over 175 to 200 GHz, the amplifier demonstrated NFs ranging from 9.8 to 11.4 dB. The amplifier shows a peak 19.6 dB of gain at 194 GHz. The circuit consumes 22 mW of dc power. With dimensions of 1285 × 600 μm, it is suitable for multichannel arrays.

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