

A 5.4 mW G-Band Phase Shifter in 90-nm SiGe HBT With One-Hot Encoding

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Abstract—We present a compact, low-power G-band phase shifter for beamforming and/or MIMO arrays with large numbers of elements. The active phase shifter is based on a one-hot selection where the state of the phase shifter is selected from four phases. The low resolution (2-bit) per element minimizes per channel complexity and power consumption as well as supporting high switching bandwidth. A subquarter wavelength balun and broadside coupler allow compact implementation covering most of G-band. The phase shifter is implemented in a 90-nm SiGe HBT process ($f_{\max} = 375$ GHz) and measured from 150 to 220 GHz with -8.7 dB average gain and a -5.7 dBm input 1-dB gain compression at 180 GHz. It consumes 5.4 mW DC power and occupies only 0.02 mm^2 core area. The root-mean-square error of gain and phase were, respectively, 0.68 – 1.48 dB and 12 – 16.7° across the range.

Index Terms—BiCMOS, G-band, millimeter-wave, one-hot encoding, phase shifter, SiGe, vector-sum.

I. INTRODUCTION

G-band (140–220 GHz) communication offers tremendous bandwidth to support high throughput backhaul links or high-resolution imaging. G-band requires RF circuits to operate close to the maximum oscillation frequency (f_{\max}) of the transistor, which means the transistor cannot offer high gain and efficiency in the circuit. A large number of phased arrays in the G-band escalates the system gain and efficiency in the spatial domain and overcomes the harsh channel characteristics as well as the poor electrical performance of the transmitter. However, the G-band arrays would place a premium on power consumption and area per element. With a half-wavelength spacing of 0.7 mm , hundreds of elements could occupy an array aperture of only 1 cm^2 . A large number of elements requires new architectures that leverage low resolution per element to constrain the overall power consumption and area requirement.

A phase shifter with a small footprint and low-power consumption is important for efficient massively scaled arrays. A vector-sum active phase shifter is a candidate and has been reported around 200 GHz frequency [1], [2], [3], [4], [5], [6], [7]. However, vector summing is sensitive to the nonlinear transconductance of amplifiers, resulting in unpredictable gain and phase shift as a function of control voltage. The control resolution must be finer than the operational resolution through a lookup table that calibrates the gain and phase. The control

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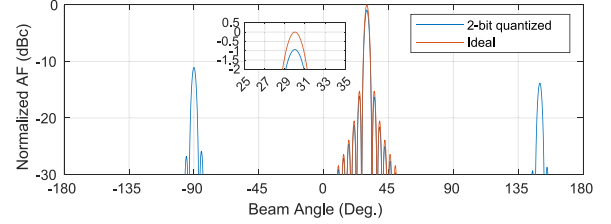


Fig. 1. Array factor comparing a 2-bit phase shifter and ideal phase shifter for 100 channels at a 30° incident angle.

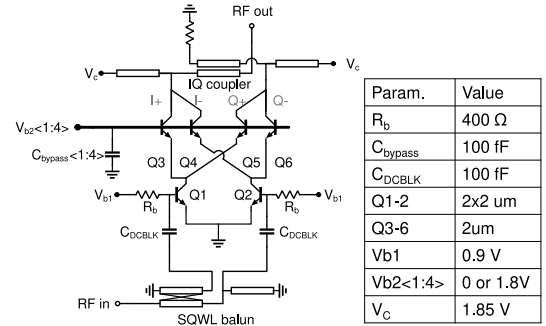


Fig. 2. Schematic of proposed active phase shifter using an HBT technology.

bits and lookup tables become a burden as the frequency of operation scales.

For a large number of array elements, gain, and phase error can be tolerated due to the averaging across a large number of elements [8], [9], [10]. Fig. 1 shows an example array factor of a 100-element phased array with 2-bit phase shifters. In the quantized phased array, the phase shift level of each channel is chosen as the closest phase to the desired phase-shift levels that each channel requires. The 2-bit quantized phased array only gives 0.94 dB loss at the main beam, while a quantization side lobe is produced at -11 dB from the main beam.

Here, we present a compact, wideband 2-bit active phase shifter as an alternative to complex operation of the vector-sum phase shifters. One-hot encoding, where one of four paths is instantaneously active, selects the phase shift through one of the paths rather than by vector summing. Therefore, the gain error is minimized if all four paths are identical and the quadrature error is determined through the accuracy of the quadrature coupler. The footprint of the phase shifter is minimized with subquarter wavelength (SQWL) design of the phase generation components.

In Section II, we discuss the operation principle and the SQWL designs of phase generation components. The measured results of the phase shifter are presented in Section III. The phase shifter exhibits an exceptionally wideband performance from 150 to 220 GHz at 5.4 mW.

II. CIRCUIT DESIGN

Fig. 2 provides a schematic of the proposed active phase shifter and the detailed design parameters. At the input, the SQWL balun

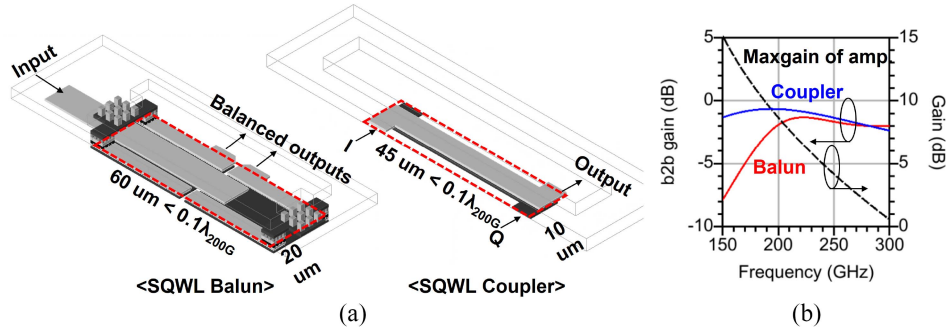


Fig. 3. Subquarter-wavelength balun and coupler (a) layout and (b) simulated back-to-back losses.

TABLE I
LOGIC TABLE OF THE PHASE SHIFTER WITH ONE-HOT ENCODING

State	Amp. 1		Amp. 2	
	Q3	Q5	Q4	Q6
I+	1	0	0	0
Q+	0	1	0	0
I-	0	0	1	0
Q-	0	0	0	1

produces differential signals that drive a differential pair (Q1/Q2). Q1 and Q2 are sized to produce around a $25\ \Omega$ base impedance which is matched with balance ports of the balun for a wide-band input matching. It has $16.1 - j3.6\ \Omega$ of base impedance at 180 GHz. The differential currents generated by the differential pair provide a 180° phase shift and are introduced to the quad cell of HBT current switches. One of four HBTs (Q3–Q6) is selected to be active at any time for phase selection. This one-hot encoding is limited to 2 bits and operates according to Table I. Two differential paths are connected to the I coupler port and the other two differential paths are connected to the Q coupler port. Each differential path is matched to $50\ \Omega$ through series and short stub biasing transmission line. An output SQWL directional IQ coupler determines the 90° phase shift. Therefore, the phase error is related to the 180° error in the input SQWL and the 90° error in the output coupler. Since one HBT is selected at a time but the signal path shares the same elements, the gain error is intrinsically lower than a conventional vector-sum phase shifter. This operation allows the phase shifter to be insensitive to the nonlinear transconductance of the transistors and mainly be determined by the phase generation components with the reduced power consumption from the Gilbert cell. The phase shifter has top-metal ground plane and the transmission line is implemented in inverted microstrip line. Top-metal ground provides large continuous ground without discontinuity when accessing the transistors [11].

Fig. 3(a) shows the proposed passive phase generation elements. The SQWL balun allows a compact implementation based on a triaxial microstrip environment [12]. The SQWL can absorb the input capacitance of the base-emitter junctions (Q1/Q2) into the inherent inductive impedance of the balanced ports to match the input or output parasitic capacitance. The input balun length is shortened to $60\ \mu\text{m}$ to absorb the capacitance, whereas the quarter wavelength at 200 GHz is $190\ \mu\text{m}$. Similarly, the IQ directional coupler is also designed using SQWL approach with $45\text{-}\mu\text{m}$ length along the broadside coupling.

Fig. 3(b) shows simulated back-to-back loss of the designed balun and IQ coupler. The loss of the input balun and coupler are centered around 200 GHz to equalize against the gain response of the

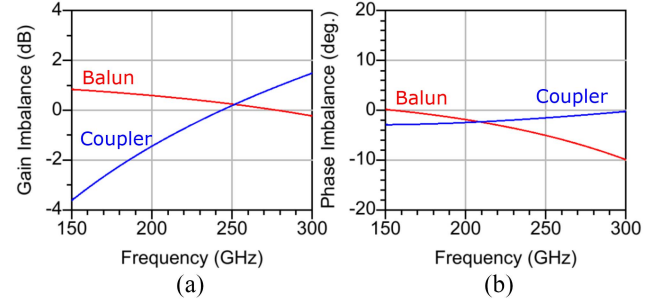


Fig. 4. Imbalance of (a) gain and (b) phase of the balun and coupler.

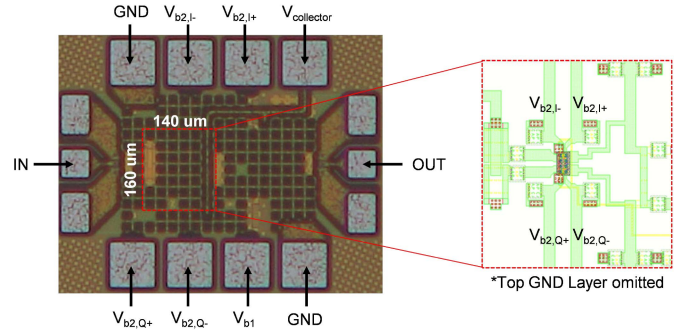


Fig. 5. Chip photograph and core layout of proposed active phase shifter. (core/chip area: $0.02/0.24\ \text{mm}^2$).

amplifier from 150 GHz. From the back-to-back insertion loss simulation, insertion losses per balun or coupler excluding the dividing loss are derived. The lowest insertion losses per component among G-band were 0.75 dB at 220 GHz for the balun and 0.35 dB at 200 GHz for the coupler.

The simulated gain and phase imbalance of the balun and coupler are shown in Fig. 4. The load impedance is set to $25\ \Omega$ for balanced port of the balun and rest of the ports are set to $50\ \Omega$. To offset the relatively high gain imbalance in the SQWL design of the coupler, the coupler is intended to compensate with a composite imbalance that flattens out. Similarly, the total phase imbalance is also intended to cancel out at the output of the phase shifter. Actual complementary imbalance equalization is monitored and fine tuned after the simulation with gain cell.

III. MEASUREMENTS

The proposed active phase shifter is implemented in the GlobalFoundries 90-nm SiGe BiCMOS process ($f_{\text{max}} = 375\ \text{GHz}$). Fig. 5 shows the implemented chip photograph and core layout inside the inverted microstrip line. The core area occupies only $0.02\ \text{mm}^2$,

TABLE II
COMPARISON TABLE OF THE PHASE SHIFTERS OPERATES AROUND 200 GHz

Ref.	Process	Phase Range	Resolution	Freq. (GHz)	Avg. Gain (dB)	RMSE Gain (dB)	RMSE Phase ($^{\circ}$)	IP1dB (dBm)	P_{DC} (mW)	Core Area (mm ²)
[1]	250 nm InP DHBT	90 $^{\circ}$	Cont.	260–320	8.8	n.a.	n.a.	n.a.	113.9	0.20*
[2]	130 nm SiGe $f_{max} = 500$ GHz	360 $^{\circ}$	Cont.	220–245	-6	n.a.	n.a.	n.a.	10.5	n.a.
[3]	250 nm InP DHBT $f_{max} = 650$ GHz	360 $^{\circ}$	Cont.	220–320	-13.7	n.a.	n.a.	-0.7	21.8–42.0	0.14
[4]	50 nm GaAs mHEMT	360 $^{\circ}$	4 bits / Cont.**	240–270	-4.5	<1.8**	<12.5**	n.a.	13.7	0.64*
[5]	130 nm SiGe $f_{max} = 450$ GHz	360 $^{\circ}$	Cont.	160–200	-9.5	n.a.	n.a.	-8.4 (sim.)	8.6	0.08
[6]	130 nm SiGe $f_{max} = 500$ GHz	360 $^{\circ}$	Cont.	140–200	3.5	n.a.	n.a.	n.a.	<28	0.26
[7]	130 nm SiGe $f_{max} = 450$ GHz	360 $^{\circ}$	4 bits / Cont.**	162–190	-6.2	<1**	<8**	-13.5 (sim.)	12.4	0.07
This work	90 nm SiGe $f_{max} = 375$ GHz	360 $^{\circ}$	2 bits	150–220 150–211 (3-dB GBW)	-8.7	<1.5	<16.2	-5.7	5.4	0.02

* Estimated. ** Continuously controlled and extracted for quantized bits.

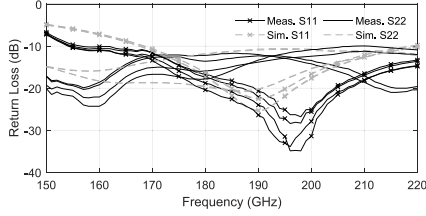


Fig. 6. Measured return losses of the phase shifter.

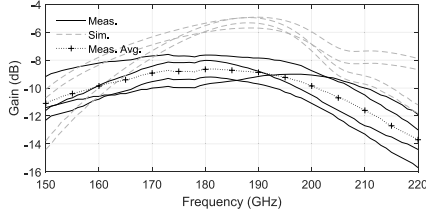


Fig. 7. Simulated and measured small-signal gain.

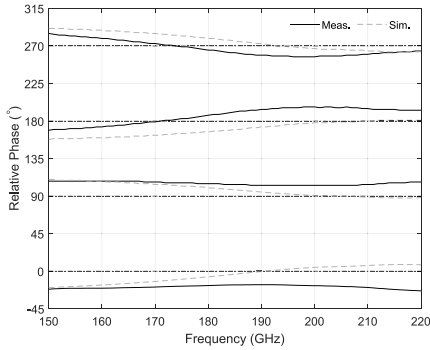


Fig. 8. Simulated and measured relative phase for the states.

and the chip consumes 5.4 mW of DC power (P_{DC}) under the 1.85 V collector voltage.

The S -parameters were measured from 150 to 220 GHz with an OML G-band extender with calibration using on-chip custom TRL patterns where the simulated loss per pad is 0.18 dB at 220 GHz. Fig. 6 shows the measured return loss of the phase shifter for all four states across 150 to 220 GHz.

The measured gain and phase response are shown in Figs. 7 and 8, respectively. The phase shifter exhibited an average -8.7 dB gain at 180 GHz, which is roughly 2 dB worse than expected from simulation.

The phase error of each state, i is calculated by the following equation:

$$\text{err}_{\theta,i} (^{\circ}) = \theta_i - \mu(\Delta\theta_i) \quad (1)$$

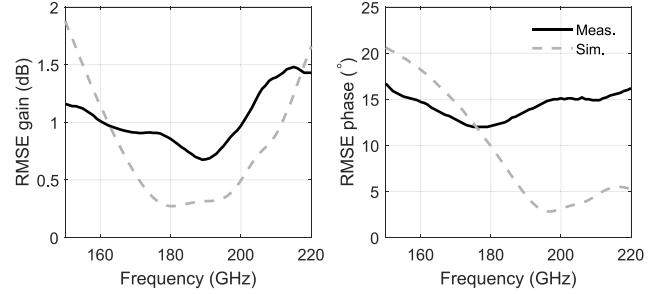


Fig. 9. Simulated and measured RMSE of (left) gain and (right) phase.

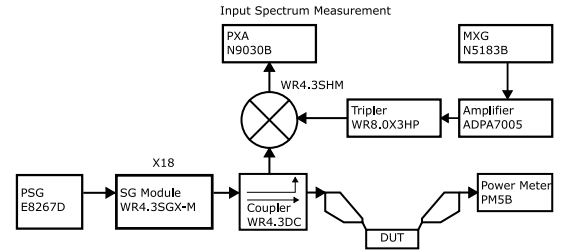


Fig. 10. Single-tone linearity measurement setup.

where θ_i is a relative phase of the i th state, and $\Delta\theta_i$ is the difference between the relative phase and ideal phase of the i th state. Based on these measurements, root-mean-square error (RMSE) of gain and phase are calculated and shown in Fig. 9. The measured RMSE of gain and phase were minimum 0.68 to maximum 1.48 dB across the 70 GHz range and minimum 12.0 to maximum 16.2 $^{\circ}$ in the measured frequency, respectively. The phase error at 185 GHz only gives 0.23 dB loss to the main beam of the quantized array factor under same computation condition to Fig. 1.

Single-tone linearity measurements of the phase shifter were performed from 170 to 200 GHz. The setup is shown in Fig. 10. The incident signal into an input probe was measured with a Keysight spectrum analyzer (N9030B) by coupling and down mixing the signal with a wave-guide direction coupler and a sub-harmonic mixer. The output signal from the output probe was measured with a VDI power meter (PM5B). The probe losses were de-embedded by measuring the 50 Ω thru line. Fig. 11 shows the measured linearity of the phase shifter. The measured peak input 1 dB gain compression point (IP1dB) was -5.7 dBm at 180 GHz.

Table II compares the proposed active phase shifter with other state-of-the-art that operate around 200 GHz. To the best of author's knowledge, the proposed phase shifter operates over the widest

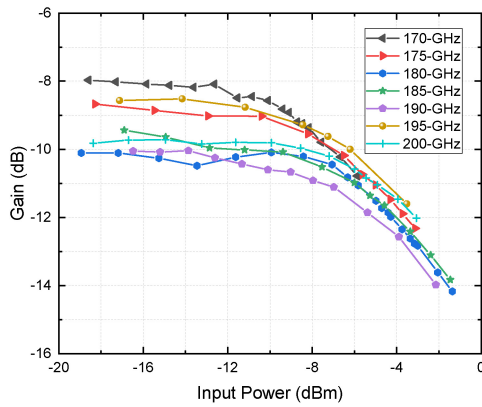


Fig. 11. Measured gain according to the input power.

bandwidth while occupying the smallest core area and operating at the lowest P_{DC} compared to earlier works. The gain and IP1dB results are comparable to earlier works. Improvements in adjusting the coupler phase shift can reduce the phase error systematically across the entire band.

IV. CONCLUSION

We present a G-band phase shifter with 0.02 mm^2 area and $5.4 \text{ mW } P_{DC}$ for future use in G-band phased arrays. It operates from 150 to 220 GHz and has -8.7 dB average gain with a -5.7 dBm input 1 dB gain compression point at 180 GHz. To the best of author's knowledge, it has the smallest implementation with low P_{DC} compared to the other phase shifters operating around 200 GHz.

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