An Ultra-compact D-band SiGe Low Noise Amplifier for Array Integration

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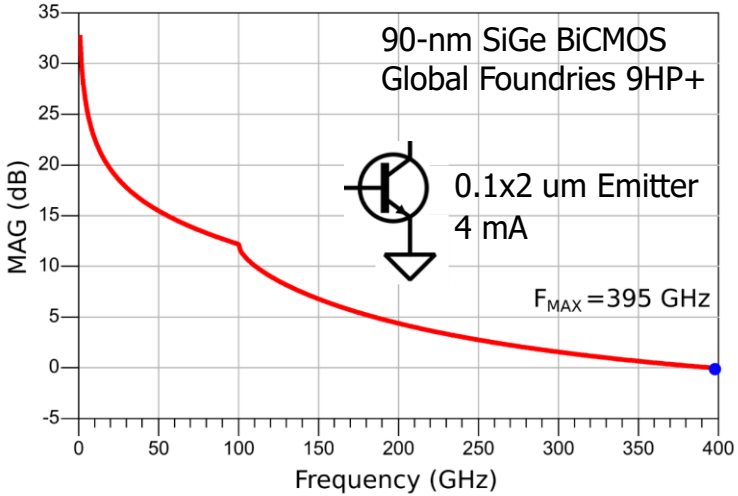
Outline

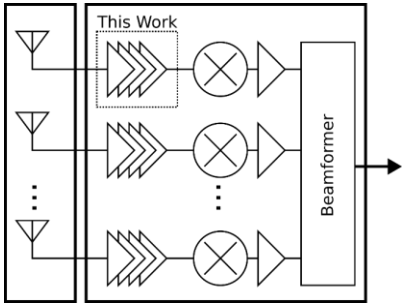
- Motivation
- Design
- Results
- Conclusion

Motivation

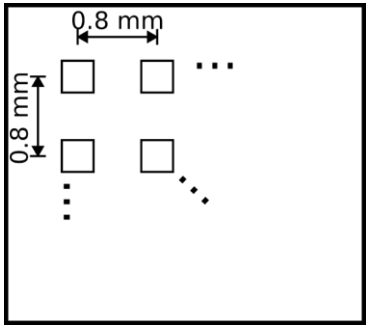
- Wide spectrum availability in frequency bands from 30 GHz to 300 GHz

- Want a compact LNA to cover D-band (110-170 GHz) that fits in array receiver system





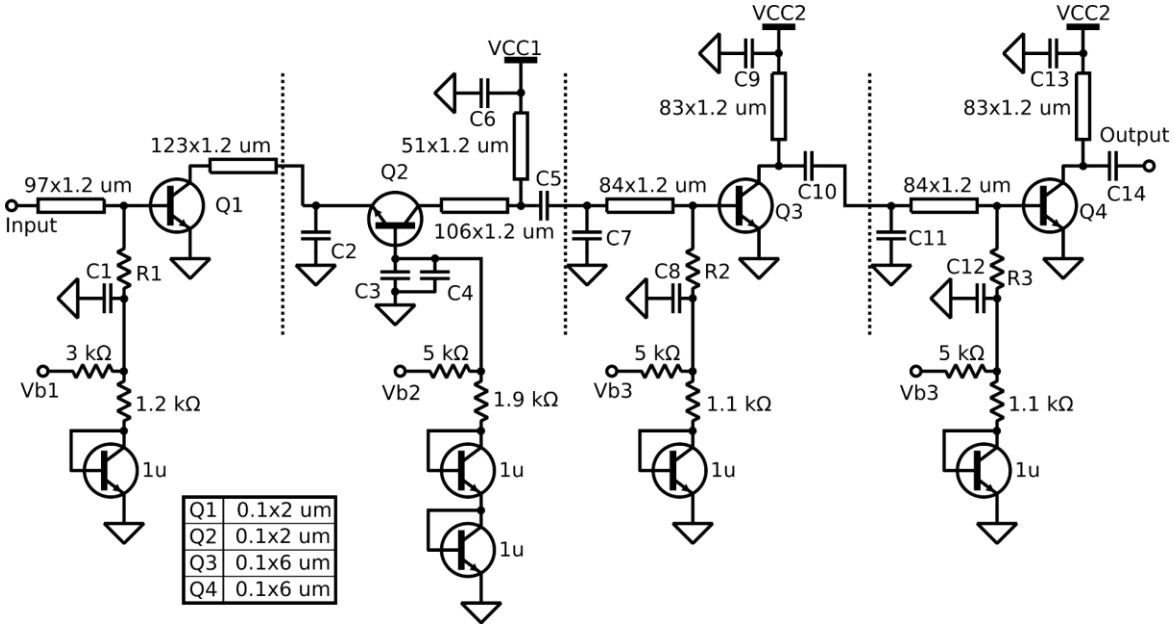
Array receiver system for integration



Half-wavelength tiling at 170 GHz

Schematic

- Proposed 4-stage LNA
- 90-nm SiGe BiCMOS (Global Foundries 9HP+)



Q1	0.1x2 um
Q2	0.1x2 um
Q3	0.1x6 um
Q4	0.1x6 um

R1	25 kΩ
C1	246 fF
C2	11 fF
C3	322 fF
C4	299 fF
C5	58 fF
C6	1.13 pF
C7	28 fF
R2	6.4 kΩ
C8	54 fF
C9	648 fF
C10	100 fF
C11	28 fF
R3	6.4 kΩ
C12	54 fF
C13	648 fF
C14	100 fF

VCC1	2.4 V
VCC2	1.2 V
Vb1	2 V
Vb2	3 V
Vb3	2 V

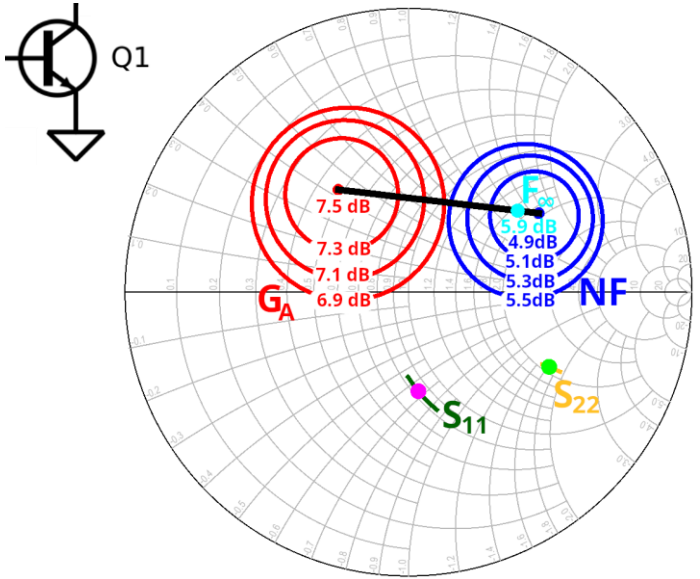
Design

- First Stage (Common Emitter):
  - Design for best noise performance and broadband input matching
  - Sized to get base impedance 42.8- j59.6 Ω at 140 GHz for easy input matching
  - Use noise measure (as F_∞) for matching

$$M = \frac{F-1}{1-1/G_A}$$

$$F_\infty = F + \sum_{k\geq 1}^{\infty} \frac{(F-1)}{G_A^k} = \frac{F-1}{1-1/G_A} + 1 = M + 1$$

  - 4 mA collector current (2 um emitter)

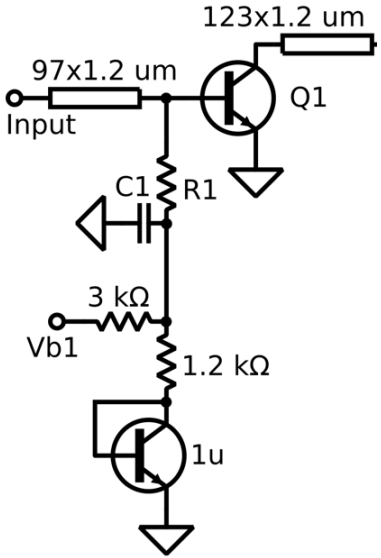


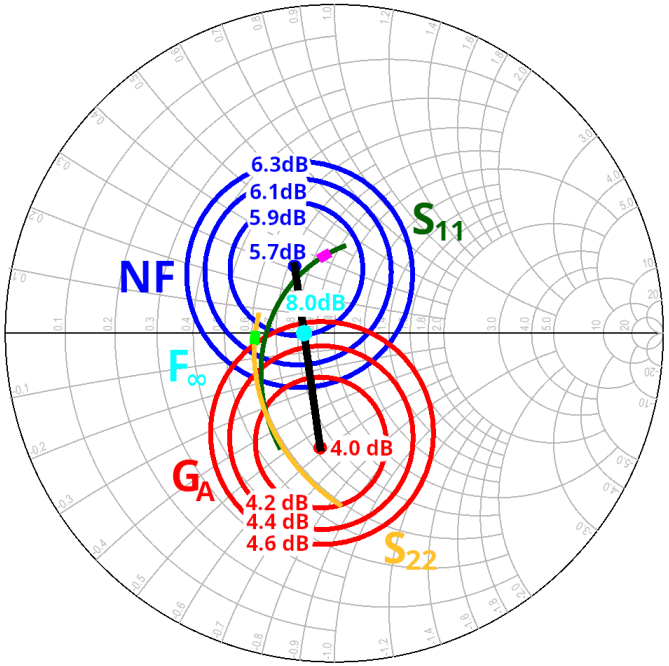
Impedances of Unmatched First Stage Transistor (140 GHz)

Design: First Stage Noise and Gain

- Minimum noise measure impedance match at 158 GHz.
- Match at higher frequency to make the most of lower gain and higher noise
- Stagger tuning between S11 and S22 for next stage to peak the gain at higher frequencies

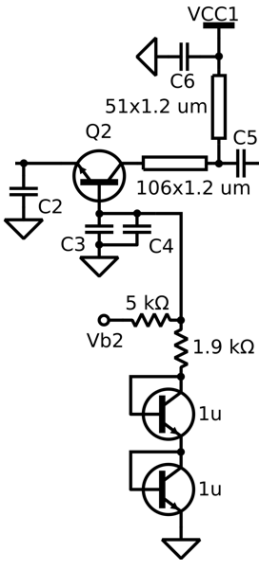
- Input and output impedances are shown from 110-170 GHz with 158 GHz marked.



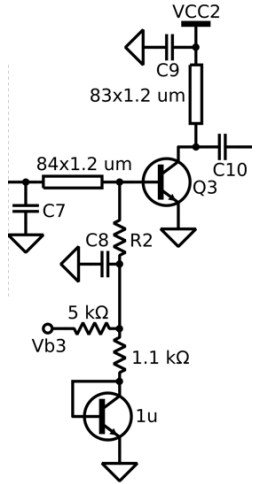


Design

- Second Stage (Common Base):
  - Design for high frequency gain peaking with staggered match at high frequency
  - Reuses current provided to first stage without DC block to save space and power
  - 4 mA collector current (2 um emitter)

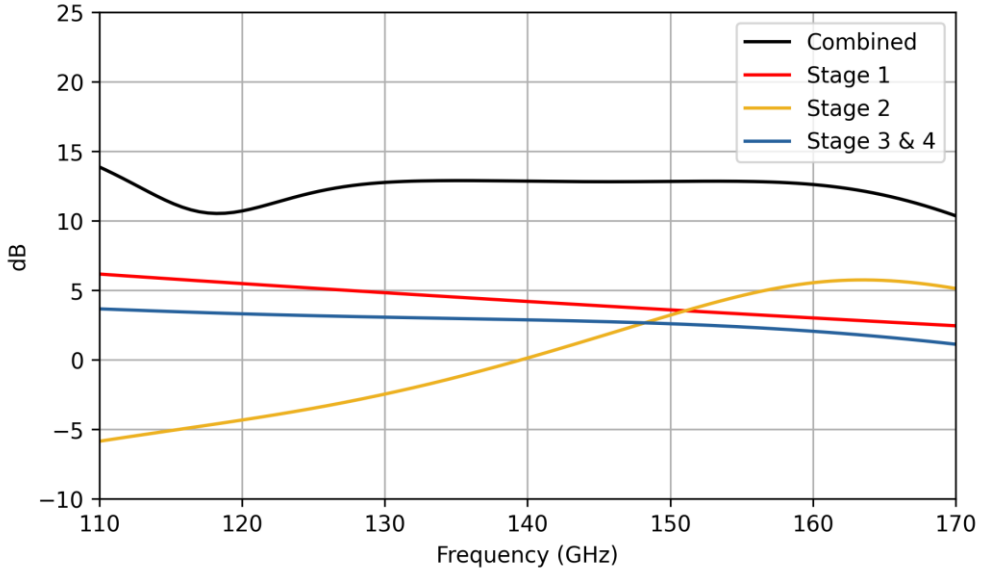


- Third/Fourth Stage (Common Emitter):
  - Designed to increase output power and to provide additional gain with available space
  - 9.4 mA collector current (6 um emitter)



Design: Gain per Stage

- Simulated gain per stage contributions with staggered tuning and combined gain of full 4-stage LNA.

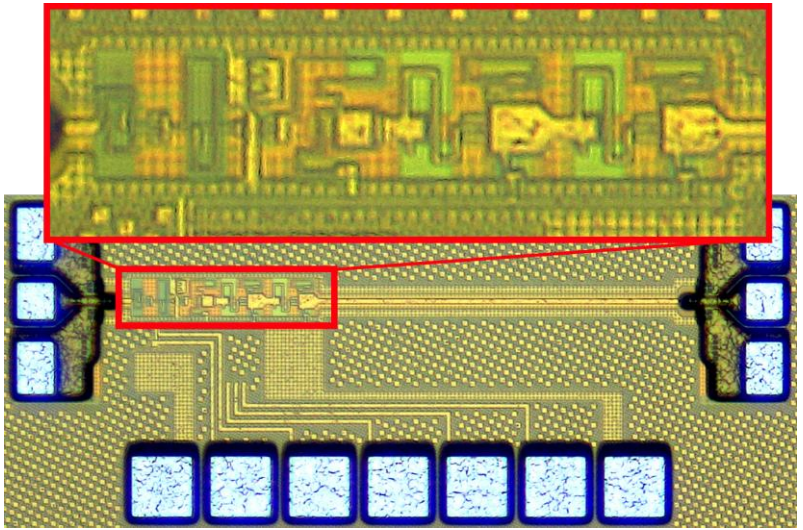


Micrograph

- LNA test structure with output extension
  - Includes 450 um line for probe clearance
  - Not de-embedded from measurements
  - Measured loss ranges from 0.5 dB to 1.7 dB, and return loss > 14.6 dB

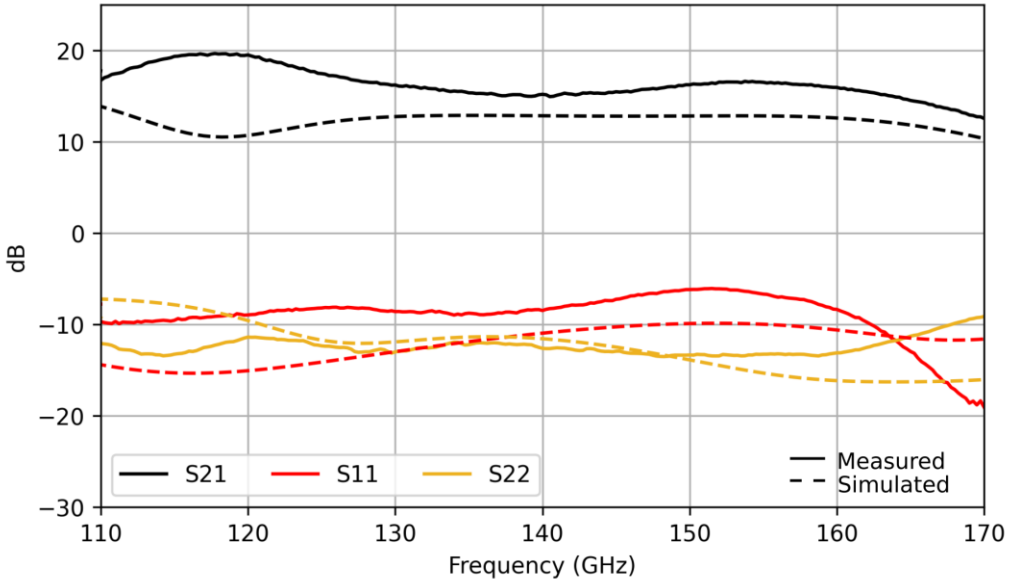
- Chip dimensions:
  - 395 um x 975 um

- **LNA core dimensions:**
  - **60 um x 245 um**
  - **0.015 mm^2**



Results: S-Parameters

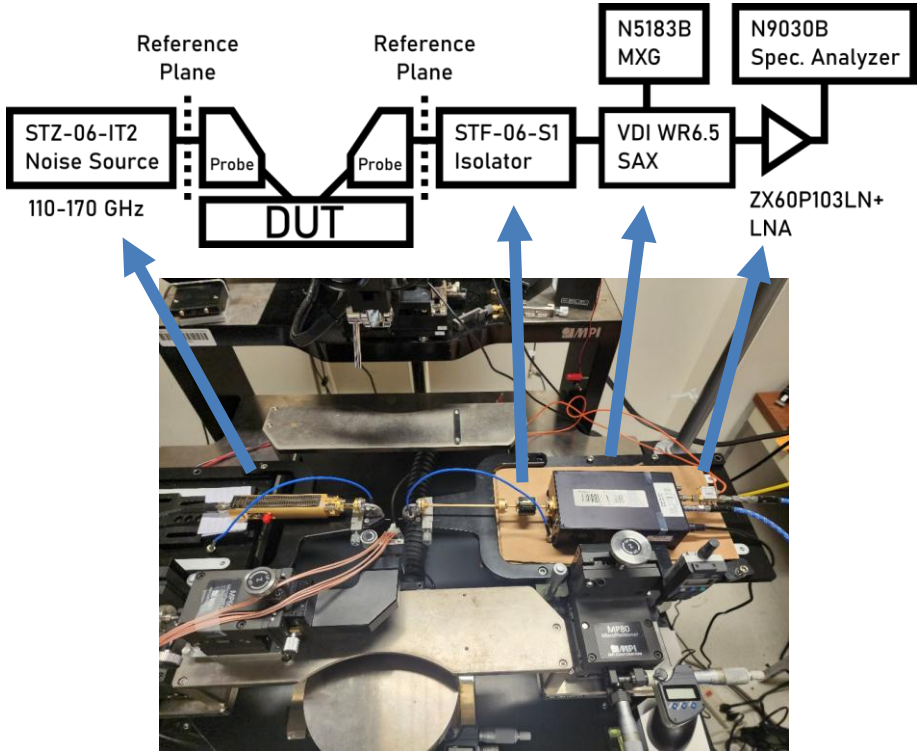
- Gain > 12 dB across D-Band
- Maximum gain: 19.7 dB at 118 GHz
- 3-dB Bandwidth from 123 GHz to 164 GHz



Noise Measurement Setup

- Y-factor measurement
  - ENR ~15 dB
  - 1 GHz IF with 240 kHz RBW

- Probes loss was removed from noise measurement by calculation
- Probe loss was obtained with back-to-back scalar measurement

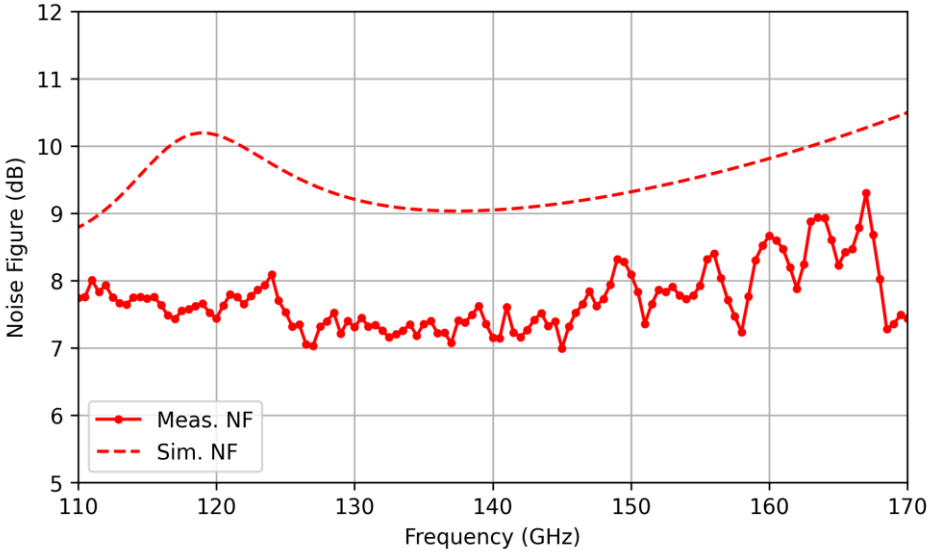


Results: Noise Figure

- NF < 9.3 dB across D-band
- Lowest NF: 7.0 dB at 145 GHz

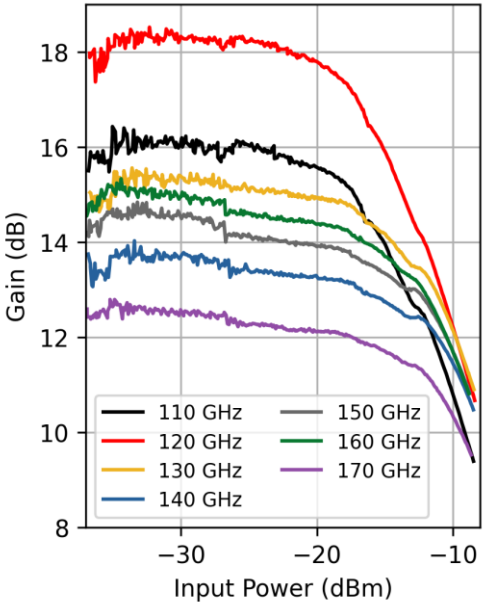
- Monte Carlo on variation with noise figure (140 GHz):
  - Standard Deviation: 0.4 dB

- Noise Measurement Uncertainty (140 GHz):
  - 0.7 dB over 2σ

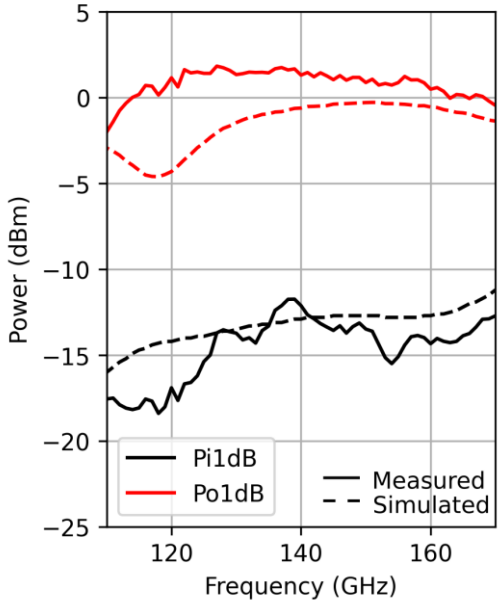


Results: Power

- Small signal gain is consistent with S-parameter measurements
- 1-dB input compression ranges from -18.4 dBm to -11.7 dBm



Input Power Sweep



Compression Points

Conclusion

- The LNA uses staggered tuning with optimum noise measure matching to achieve performance in record area consumption.
- Its small size of 0.015 mm^2 makes it suitable for highly scaled receiver systems.

Reference	**This Work**	[4]	[5]	[6]	[7]	[8]
Technology	90-nm SiGe	90-nm SiGe	90-nm SiGe	55-nm SiGe	130-nm SiGe	130-nm SiGe
Freq. (GHz)	144	139.8	140	140	140	140
BW_{3dB} (GHz)	41	37.6	28	70	52	23.2
Max. Gain (dB)	19.7	26.5	30	23	32.6	32.8
P_{i1dB} (dBm)	-13.4	-31	-	-21.3	-37.6	-28.6
NF (dB)	7.0-9.3	7.2	6.2	5-6.5	4.8-6.1	7.8*
P_{DC} (mW)	37.6	20.6	45	60	28	39.6
Core Area (mm^2)	0.015	0.69 †	0.11	0.109	0.6	0.075†

* Simulated † Die Area

Acknowledgements

- This work was supported by the Semiconductor Research Corporation (SRC) under the JUMP program, Cognisense

- The authors appreciate the support of GlobalFoundries for access to the 9HP+ process.

Comparison Table References

- [4] A. Moradinia, S. G. Rao, and J. D. Cressler, “A sige hbt d-band lna utilizing asymmetric broadside coupled lines,” IEEE Microwave and Wireless Technology Letters, vol. 33, no. 6, pp. 707–710
- [5] R. B. Yishay, E. Shumaker, and D. Elad, “A 122-150 ghz lna with 30 db gain and 6.2 db noise figure in sige bicmos technology,” in 2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2015
- [6] G. D. Filippi, L. Piotto, and A. Mazzanti, “A d-band lna exploiting ultrawideband sixth-order matching networks in sige bicmos,” in 2024 IEEE European Solid-State Electronics Research Conference (ESSERC), 2024
- [7] E. Turkmen, A. Burak, A. Guner, I. Kalyoncu, M. Kaynak, and Y. Gurbuz, “A sige hbt d -band lna with butterworth response and noise reduction technique,” IEEE Microwave and Wireless Components Letters, vol. 28, no. 6, pp. 524–526,
- [8] E. Aguilar, A. Hagelauer, D. Kissinger, and R. Weigel, “A low-power wideband d-band lna in a 130 nm bicmos technology for imaging applications,” in 2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2018

Power Measurement Setup

- Use variable attenuator to change power level
  - Better extender performance at saturated power
  - Better linear control over power level
- Calibrate input powers at all frequencies and attenuations with power meter
- Use calibrated input chain to calibrate down-conversion