Lab 01

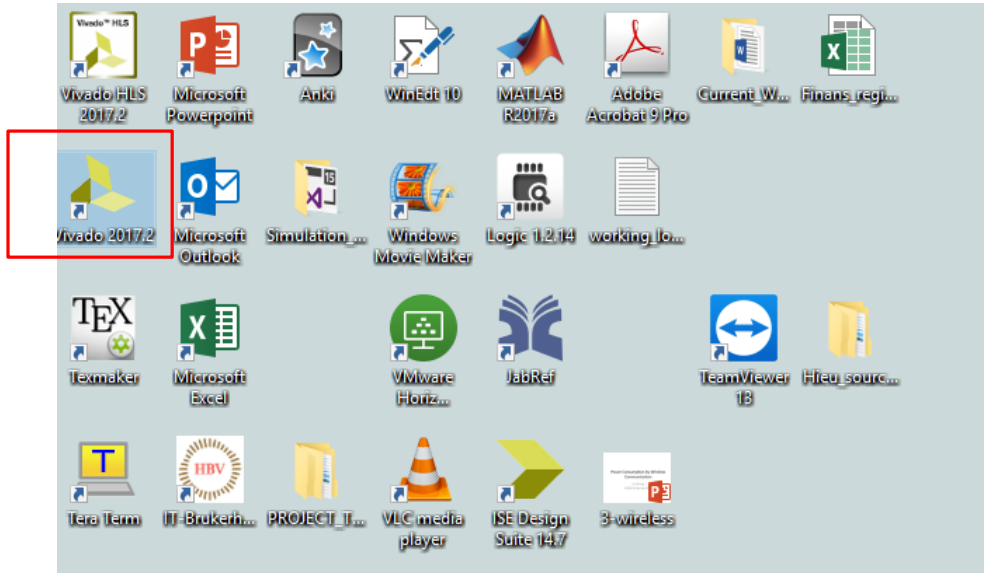
HIEU NGUYEN

Lab 01-Part I

In this lab, students use the 1-bit comparator and two bit comparator to simulate the behavior of the circuit

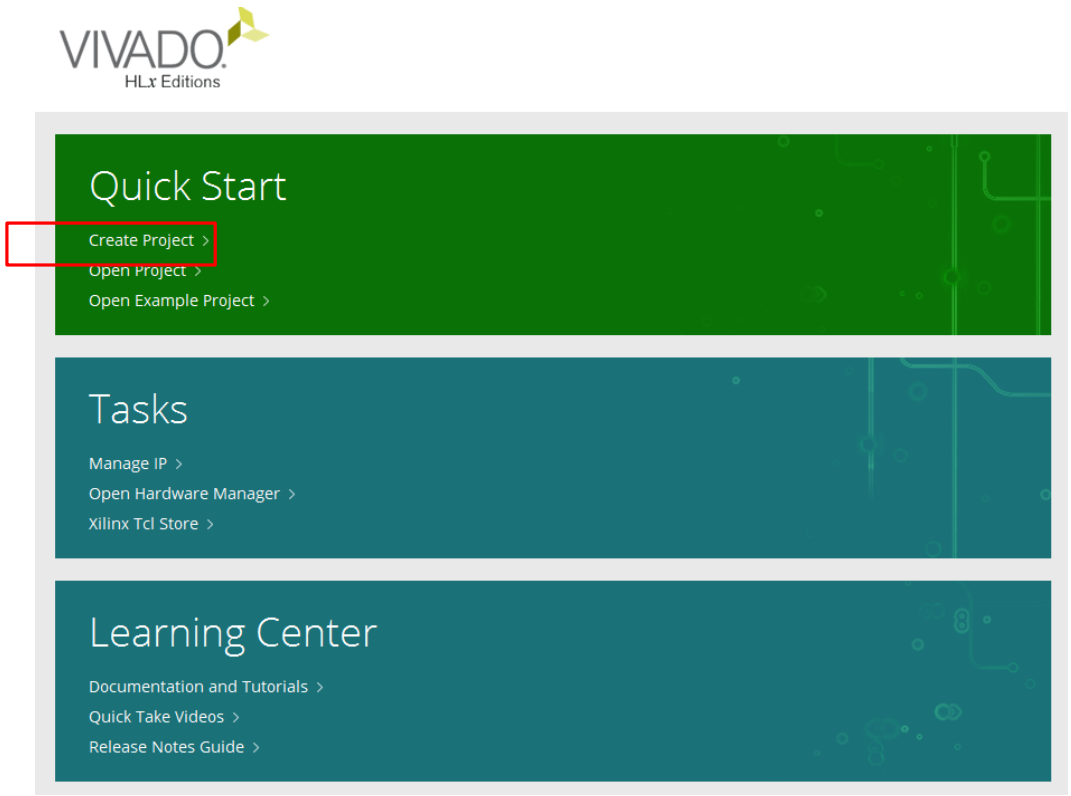
Lab 01-Part I

- Step 1: Create a folder on your computer with your own name (for example: Lab01)
- Step 2: Click on Vivado 2017.x on the desktop to open Vivado



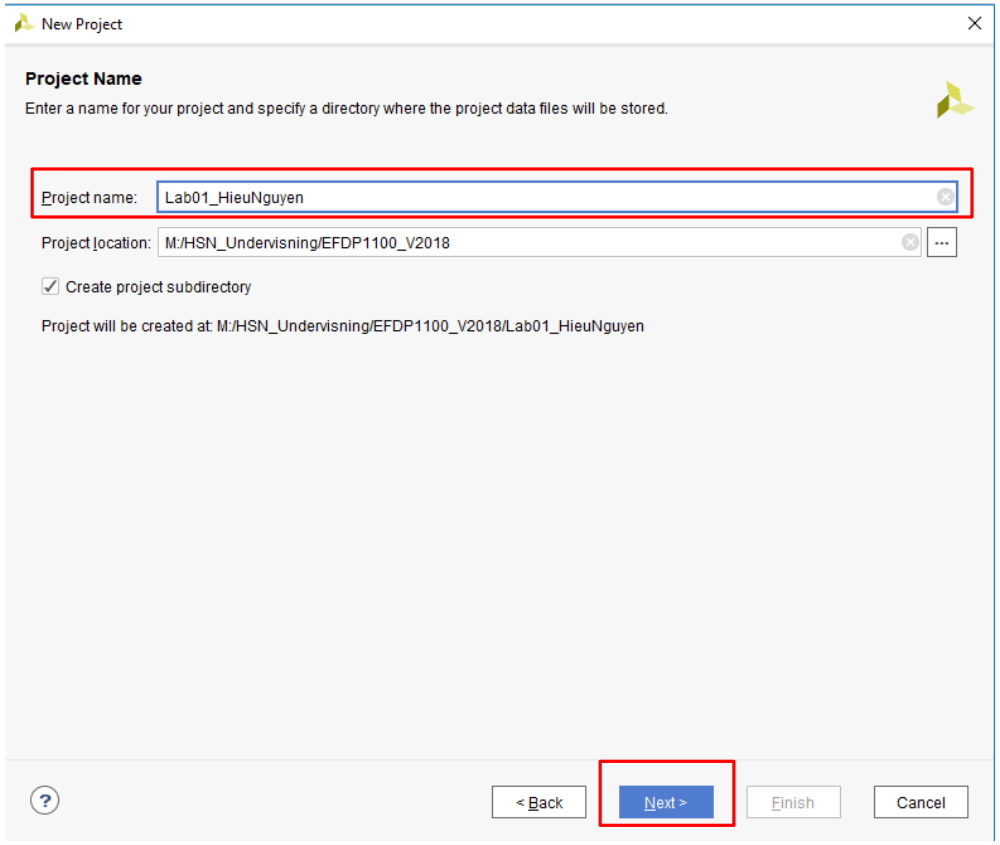
Lab 01-Part I

- Step 3: Under quick start, click on Create project, then click Next



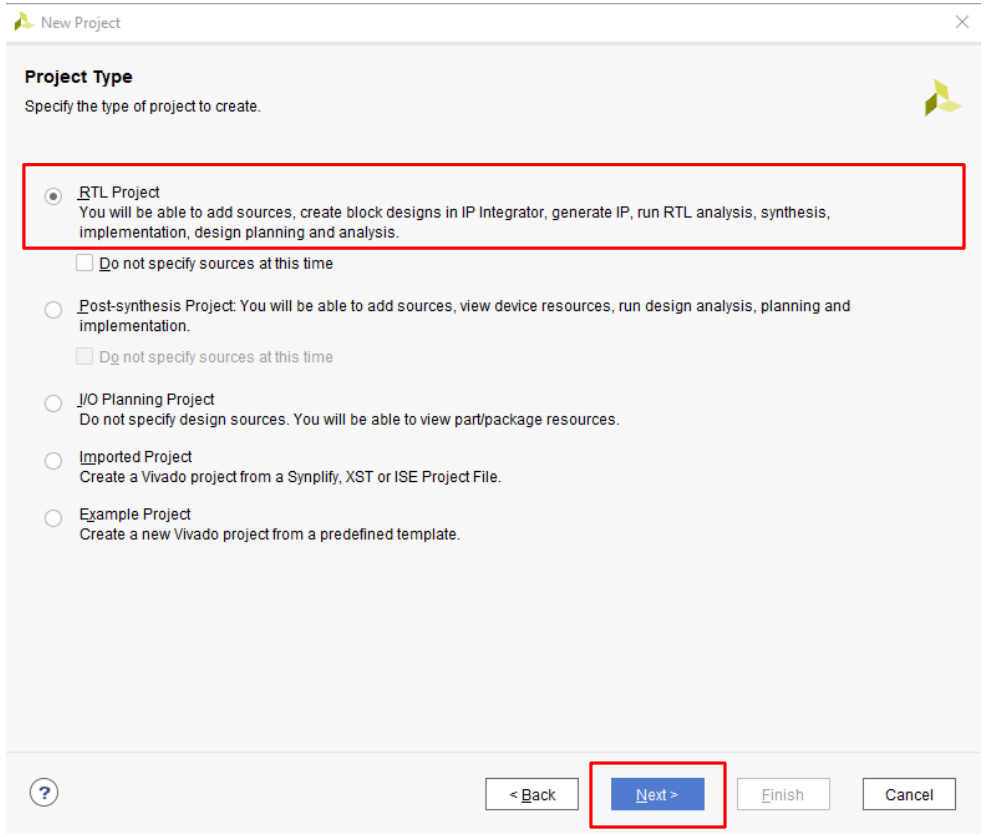
Lab 01-Part I

- Step 4: Choose project Name: Lab01_YourName, then click next



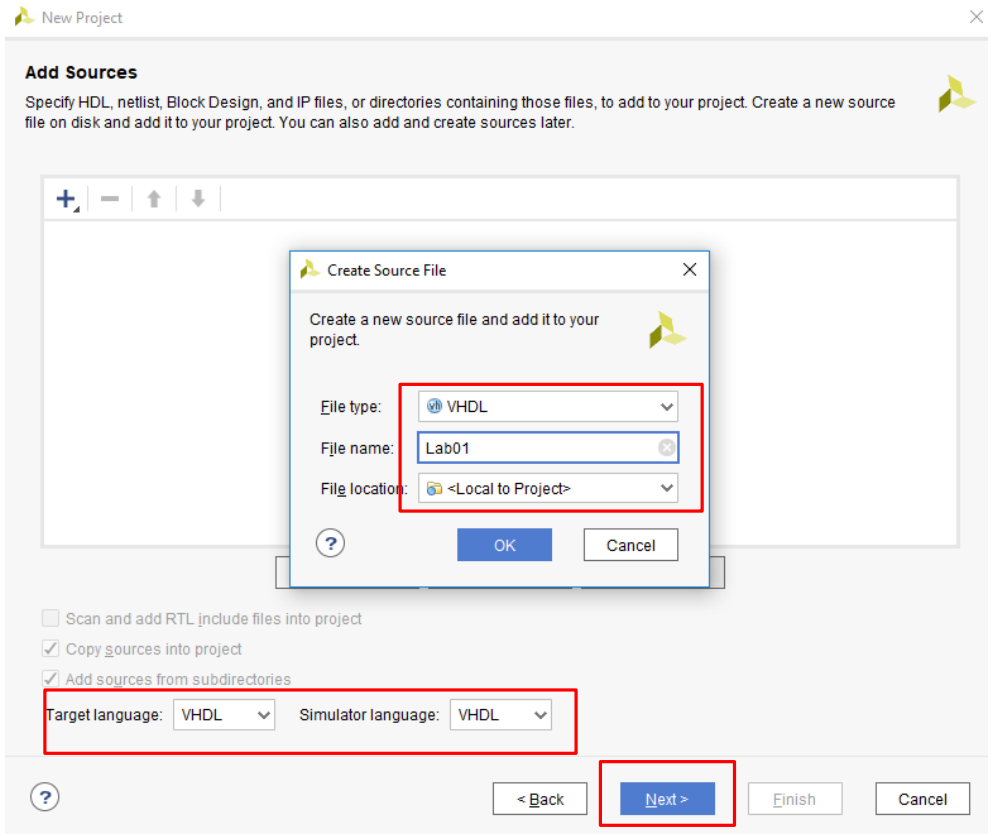
Lab 01-Part I

- Step 5: Choose RTL Project and click Next



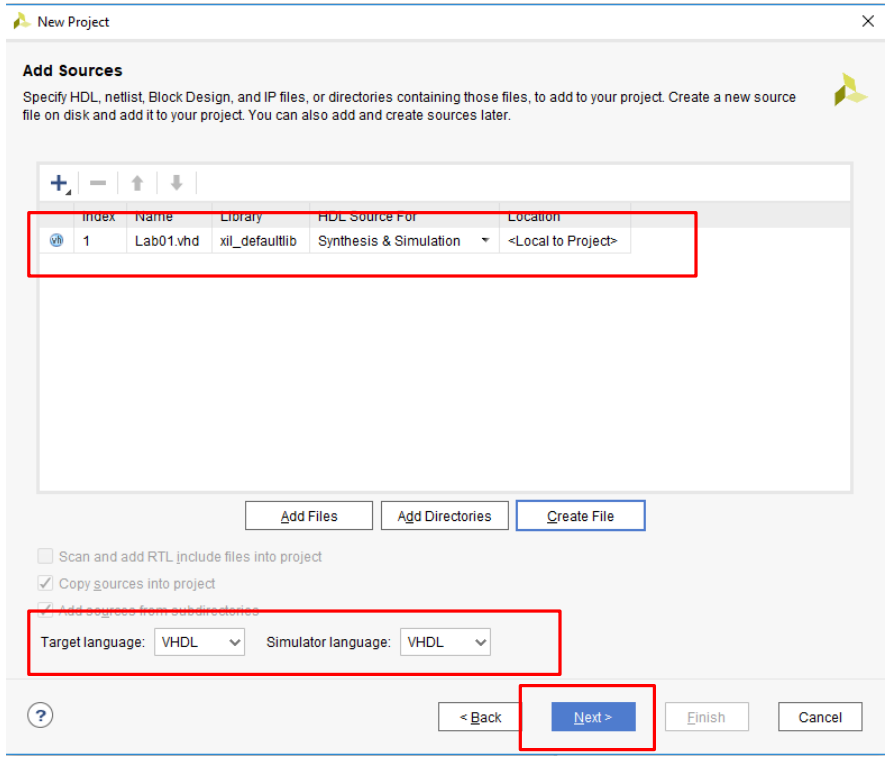
Lab 01-Part I

- Step 7: Choose the file name (For example: Lab01). Then click OK. Rememer to choose File Type as VHDL



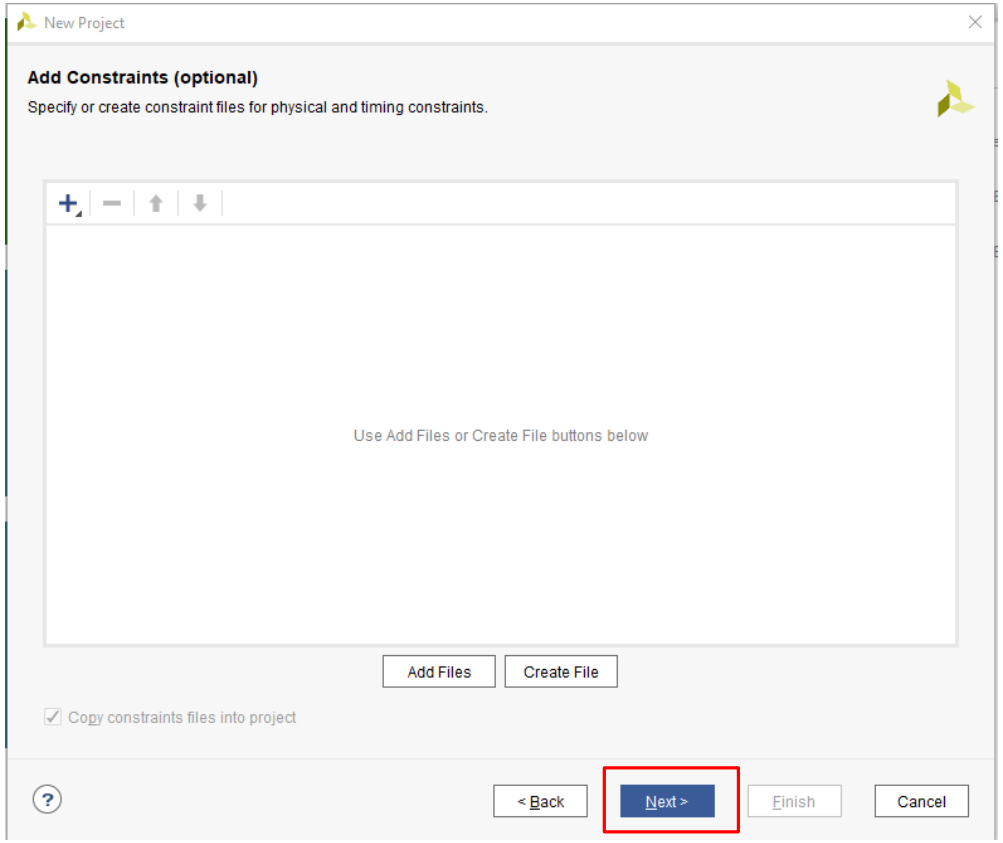
Lab 01-Part I

- Step 8: Check to guarantee that Target language is set to VHDL and Simulator language is VHDL. Then click NEXT



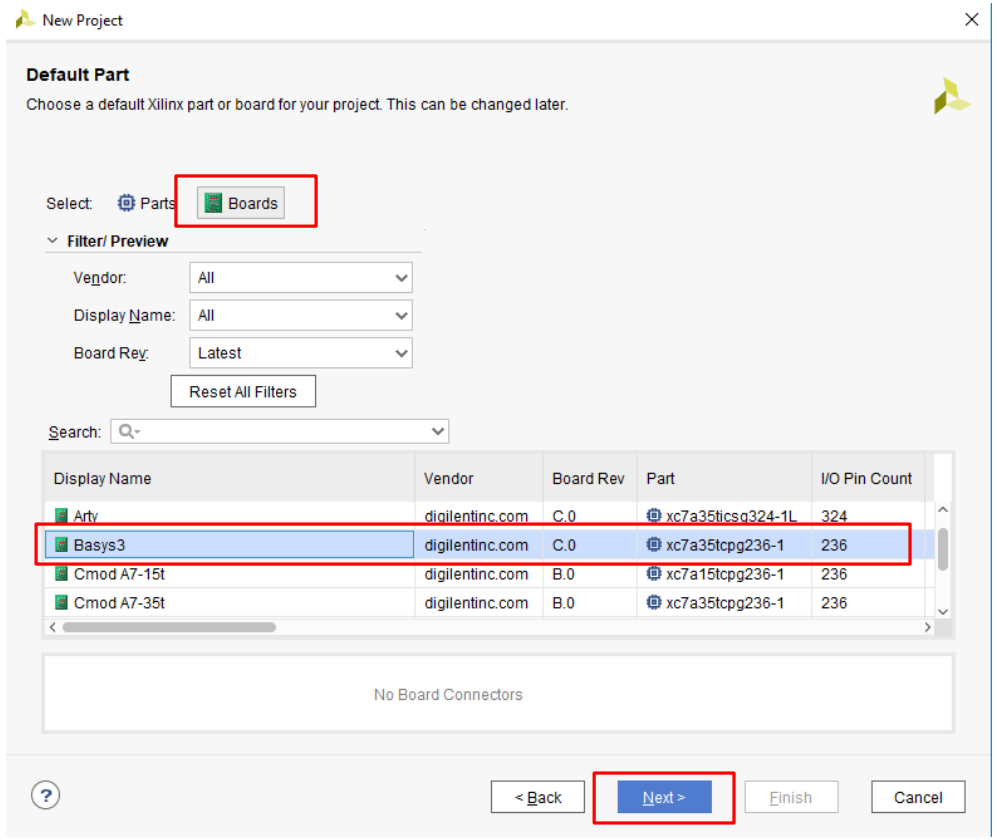
Lab 01-Part I

- Step 9: Click NEXT (We don’t use Constraint yet)



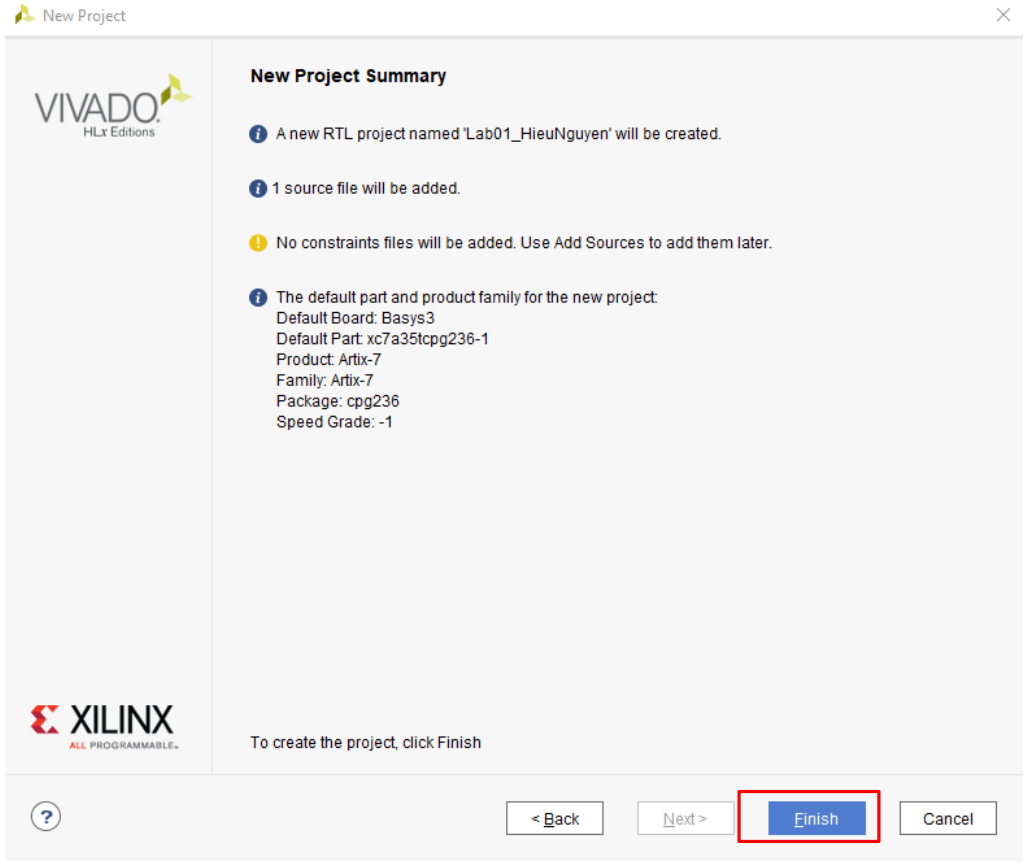
Lab 01-Part I

- Step 10: Choose equipment and click NEXT



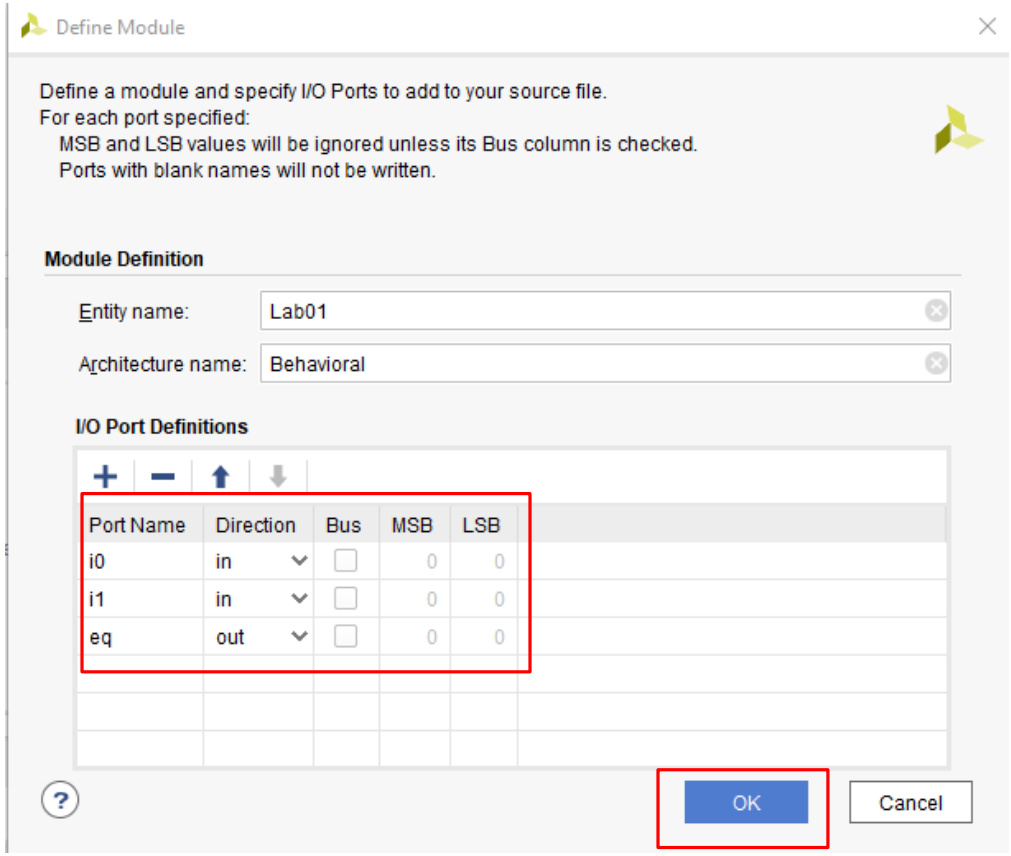
Lab 01-Part I

- Project summary: Click NEXT



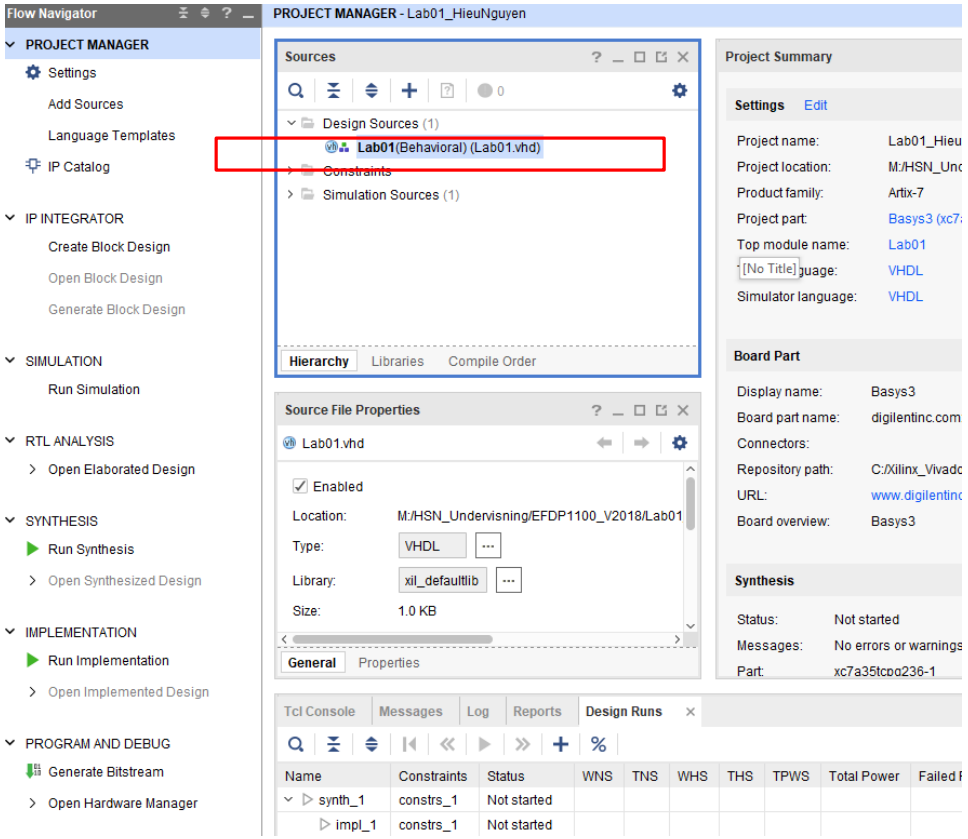
Lab 01-Part I

- Step 11: Define the input and output signals (i0, i1, eq) and click OK



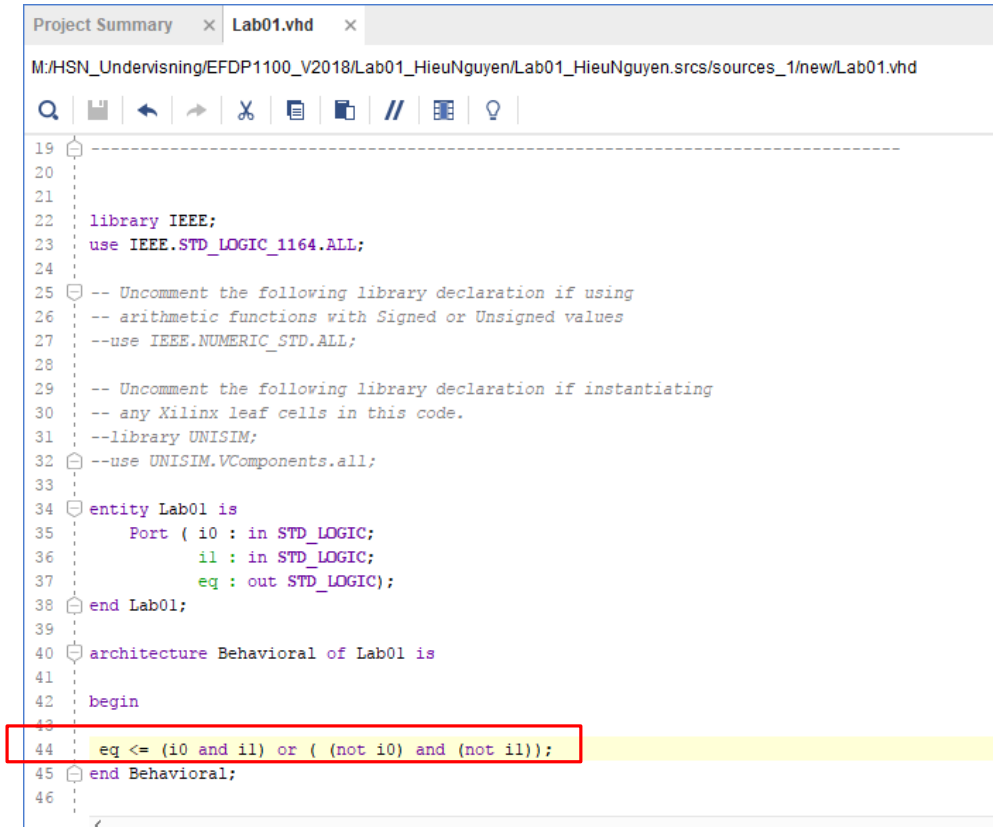
Lab 01-Part I

- Step 12: Click on Lab01 under Design Sources to open Lab01.vhd



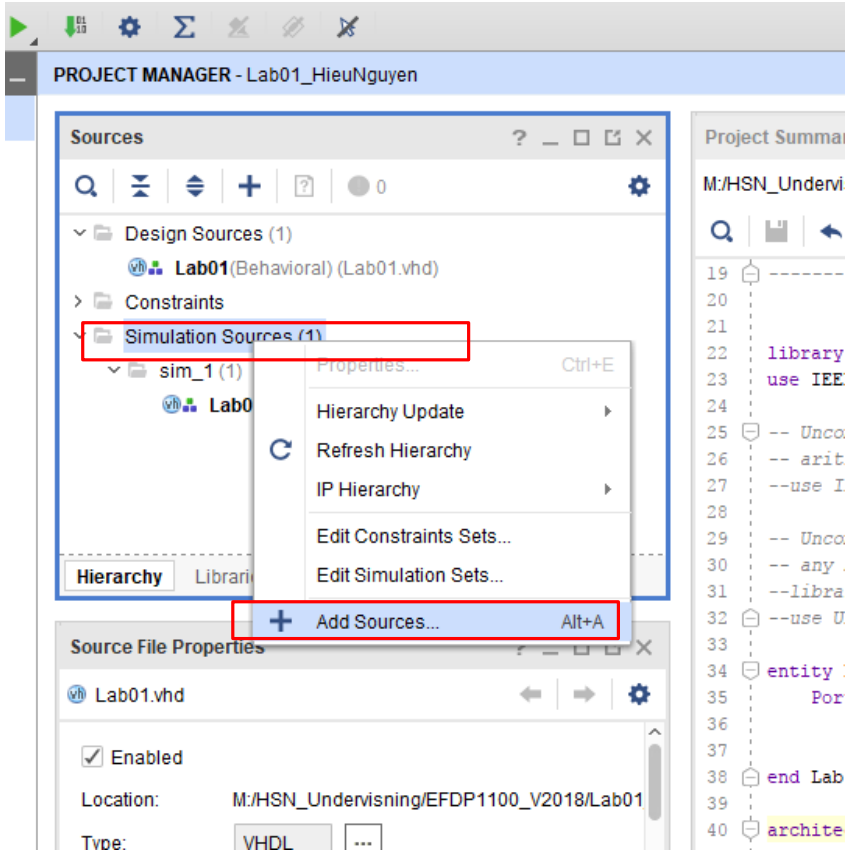
Lab 01-Part I

- Step 13: Edit the text in window next to Sources



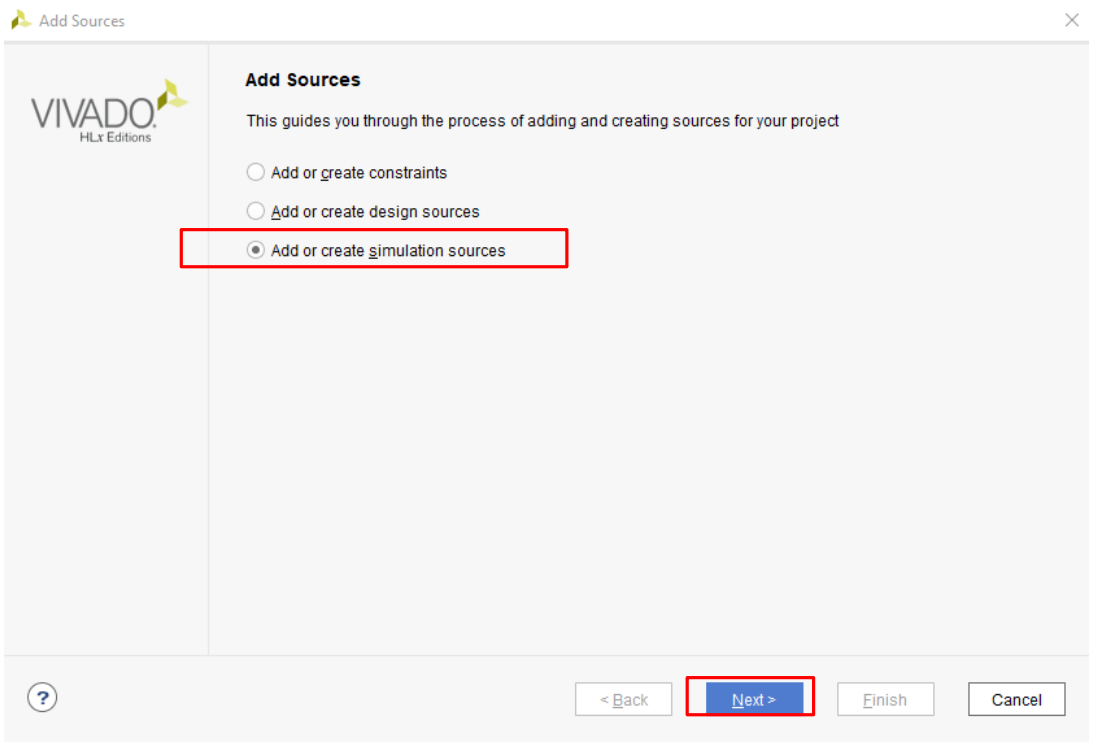
Lab 01-Part I

- Step 14: Create Testbench. Right click on Simulation Sources and choose Add Sources



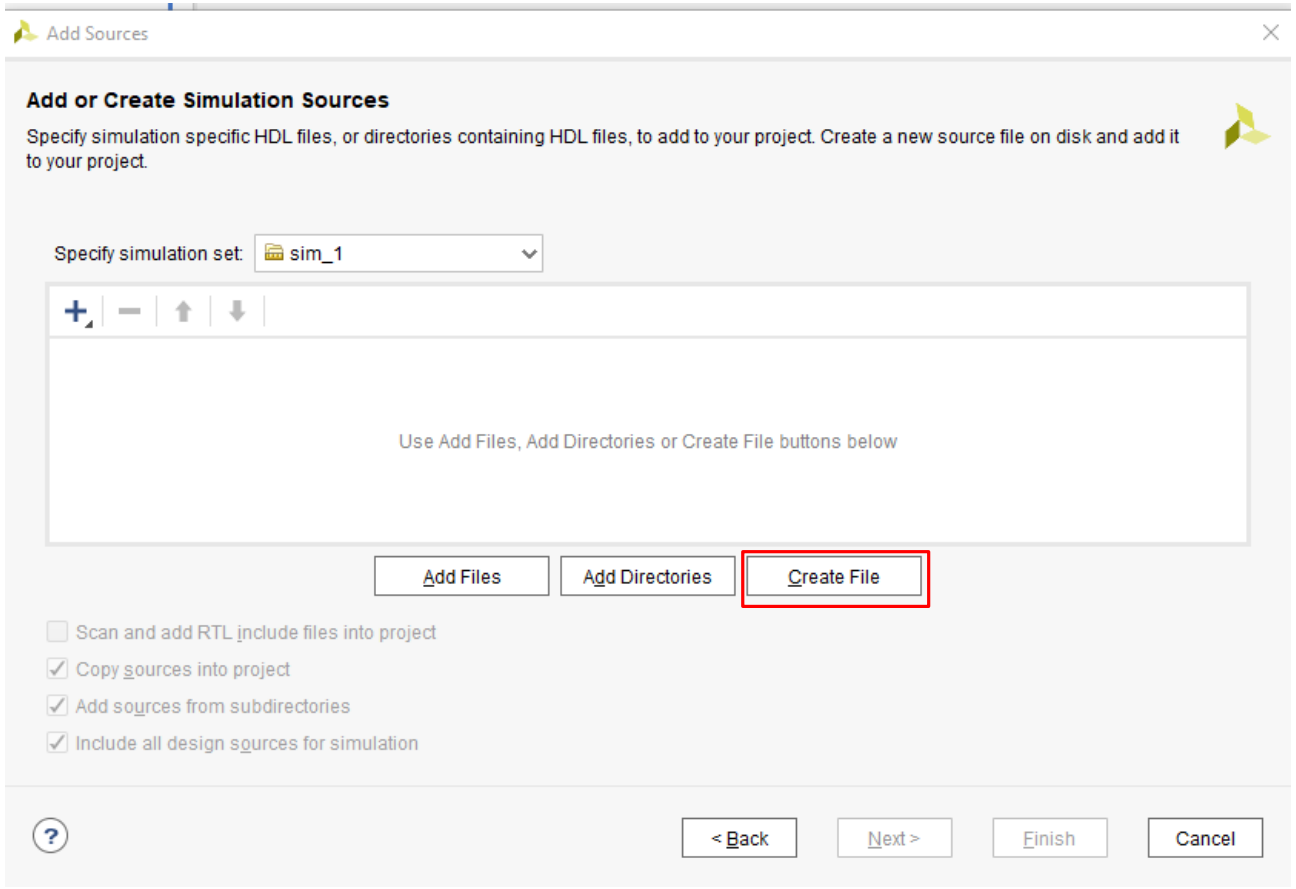
Lab 01-Part I

- Choose Add or create simulation sources. Then click NEXT



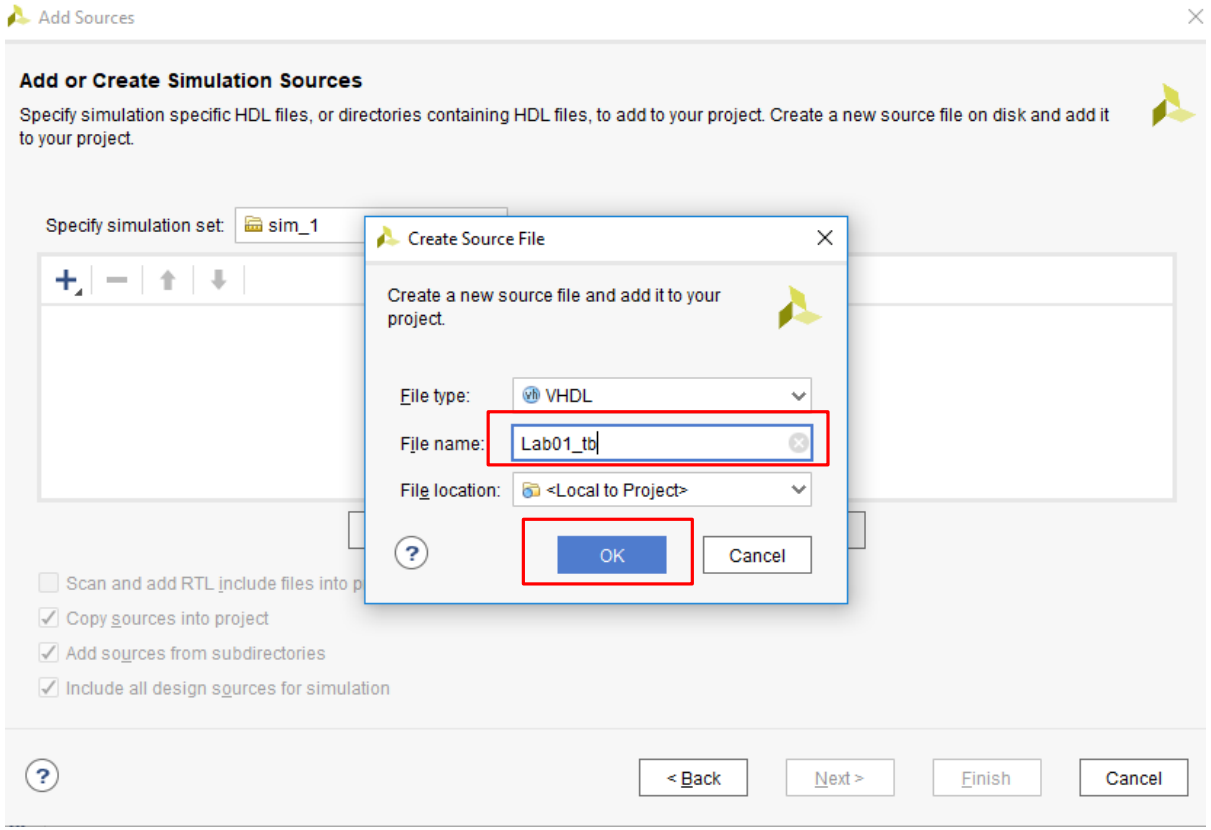
Lab 01-Part I

- Choose Create File



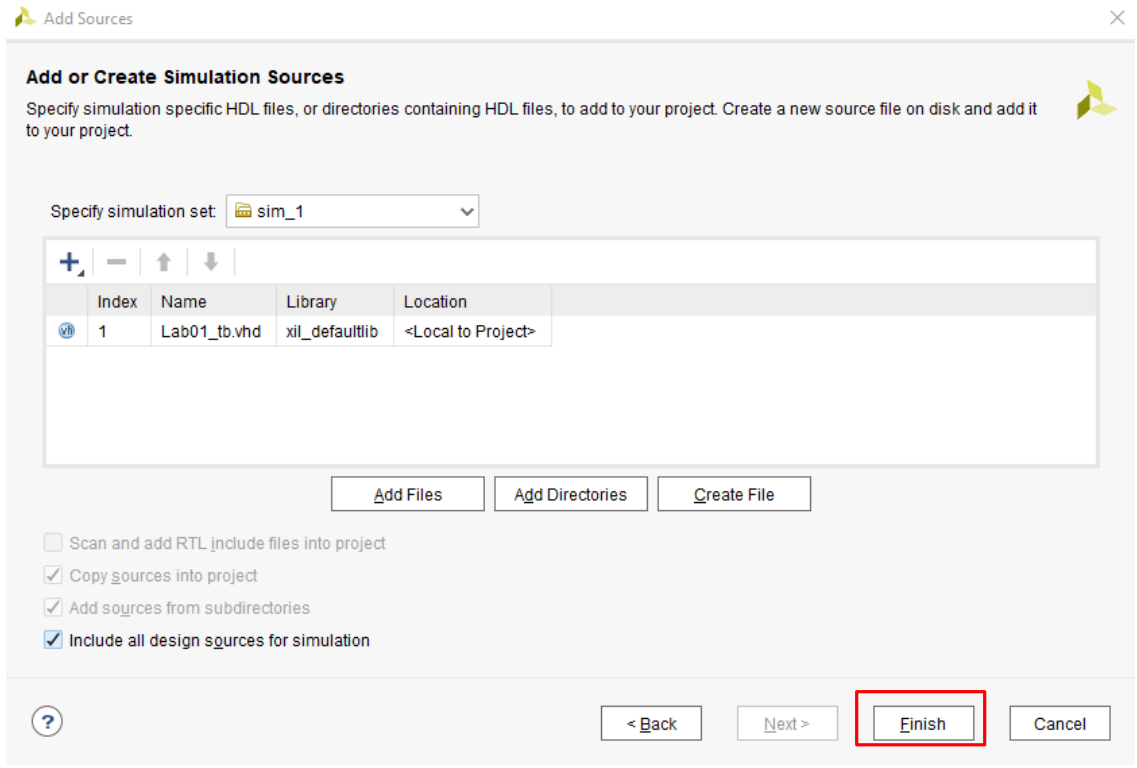
Lab 01-Part I

- Choose File Name for example Lab01_tb. Then click OK



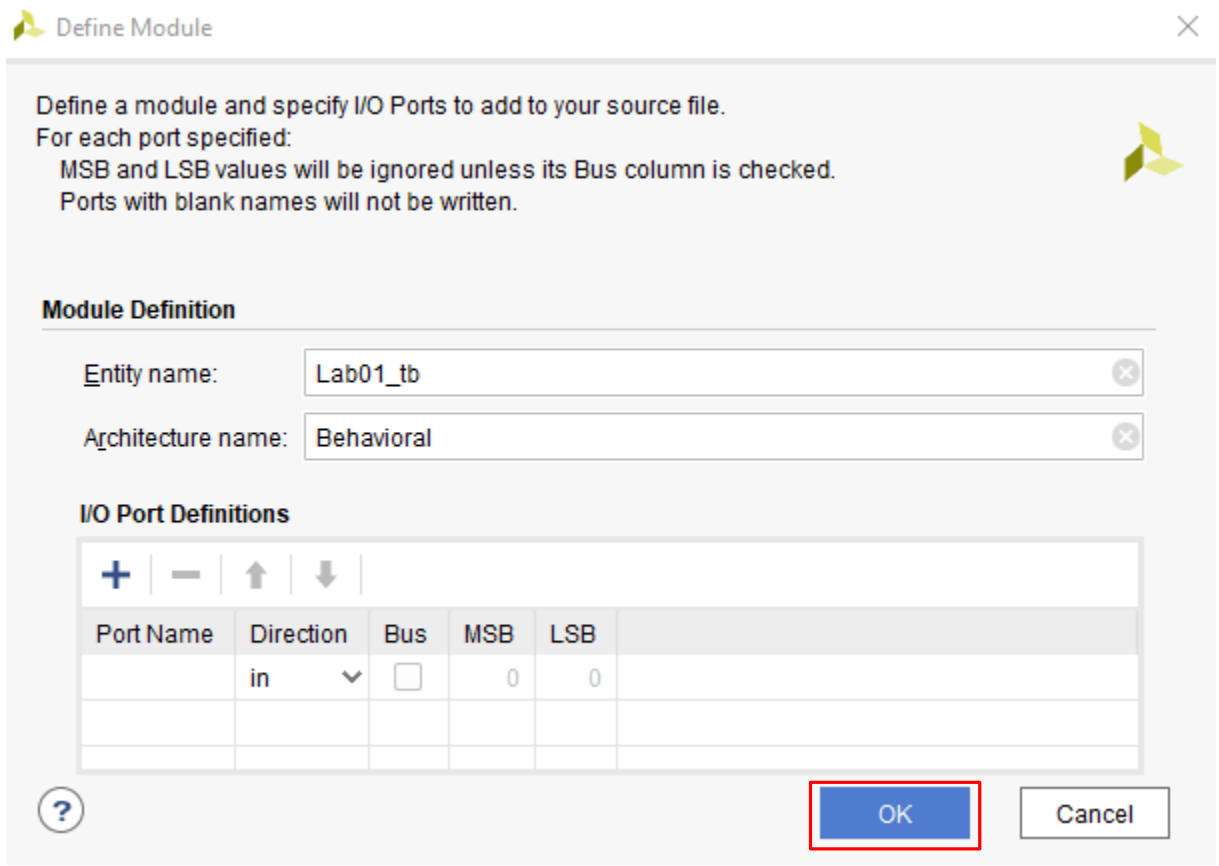
Lab 01-Part I

- Click Finish



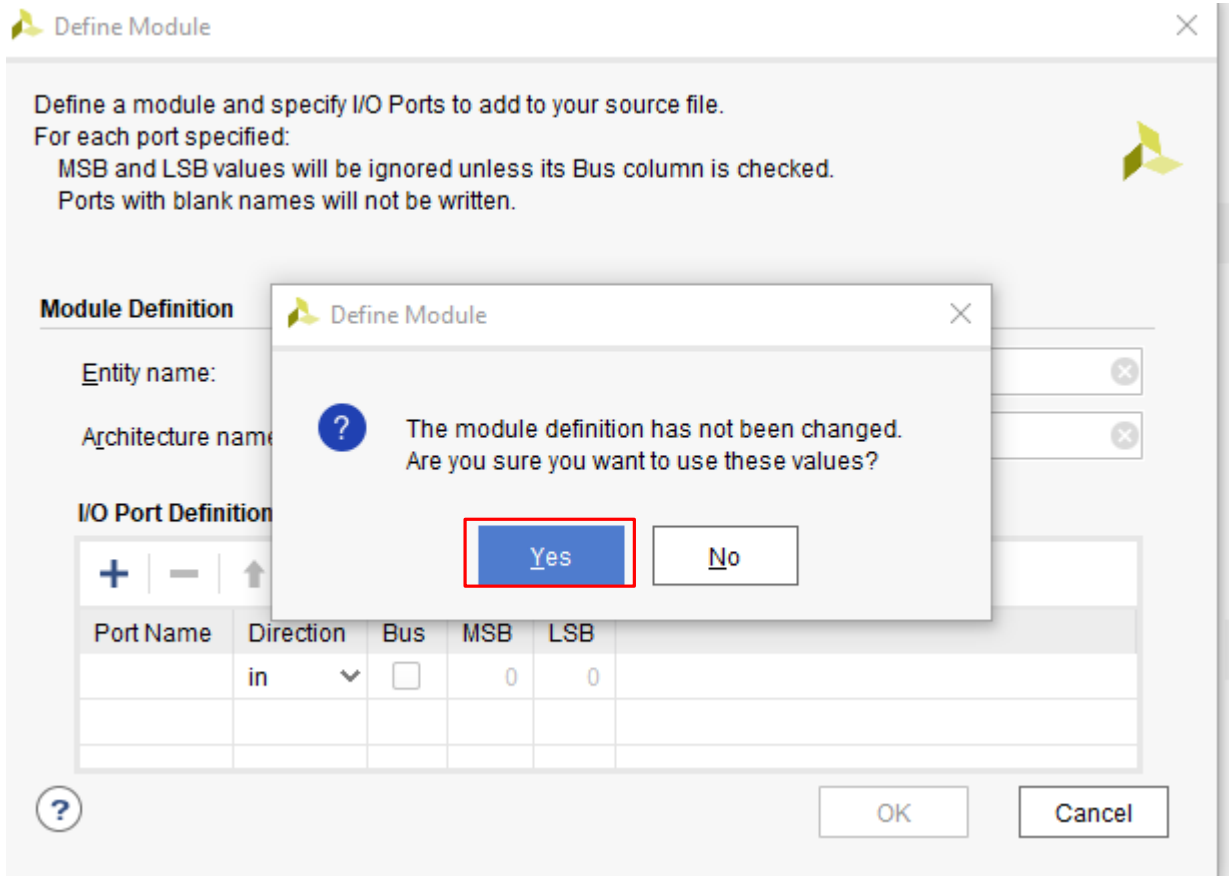
Lab 01-Part I

- Click OK



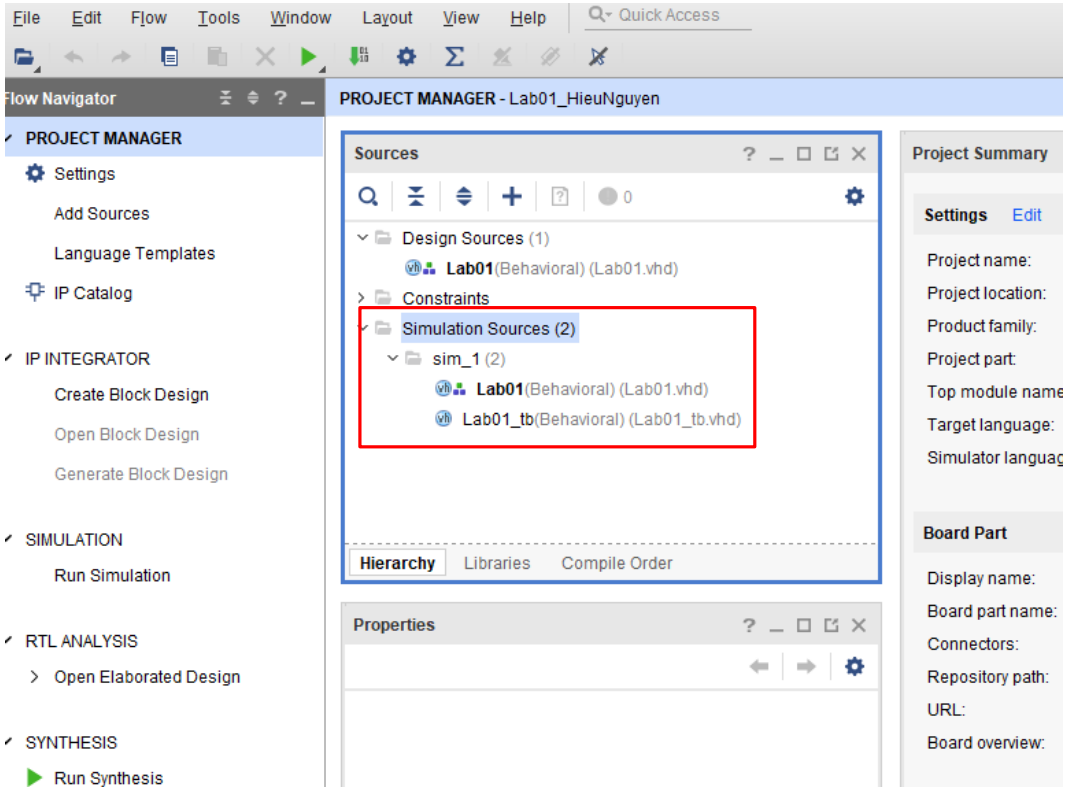
Lab 01-Part I

- Click Yes



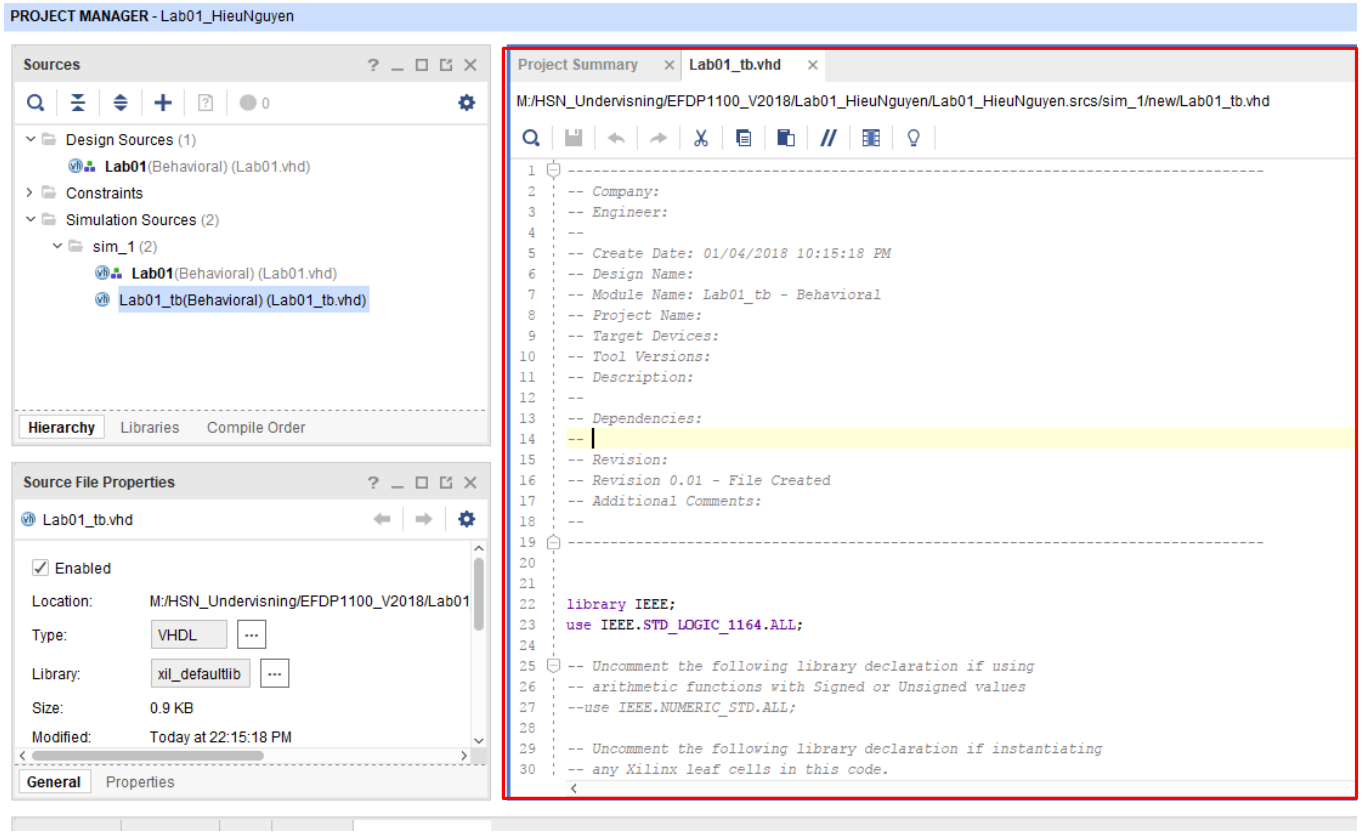
Lab 01-Part I

- Now we have testbench file under Simulation Sources



Lab 01-Part I

- Double click on Lab01_tb to open the text editor



Text editor

Lab 01-Part I

- Component declaration

```
34  entity Lab01_tb is
35  --  Port ( );
36  end Lab01_tb;
37
38  architecture Behavioral of Lab01_tb is
39
40  //--------------Declare  component here
41  component Lab01
42      Port ( i0 : in STD_LOGIC;
43             i1 : in STD_LOGIC;
44             eq : out STD_LOGIC);
45  end component Lab01;
46  begin
47
48
49  end Behavioral;
50
```

Lab 01-Part I

- Internal Singal Declaration

Lab01_tb.vhd | Lab01.vhd | Untitled 1

M:/HSN_Undervisning/EFDP1100_V2018/Lab01_HieuNguyen/Lab01_HieuNguyen.srcs/sim_1/new/Lab

```
26      -- arithmetic functions with Signed or Unsigned values
27      --use IEEE.NUMERIC_STD.ALL;
28
29      -- Uncomment the following library declaration if instantiating
30      -- any Xilinx leaf cells in this code.
31      --library UNISIM;
32      --use UNISIM.VComponents.all;
33
34      entity Lab01_tb is
35      --  Port ( );
36      end Lab01_tb;
37
38      architecture Behavioral of Lab01_tb is
39
40      -------------Declare  component here
41      component Lab01
42          Port ( i0 : in STD_LOGIC;
43                 i1 : in STD_LOGIC;
44                 eq : out STD_LOGIC);
45      end component Lab01;
46
47      ---------- Internal Singal Declaration----
48      signal i0_tb: std_logic;
49      signal i1_tb: std_logic;
50      signal eq_tb: std_logic;
51
52      begin
53
54      UUT: Lab01
55      port map (i0 => i0_tb,i1 => i1_tb, eq => eq_tb);
56
57      process
58          begin
59              ---------------vector 1--------
```

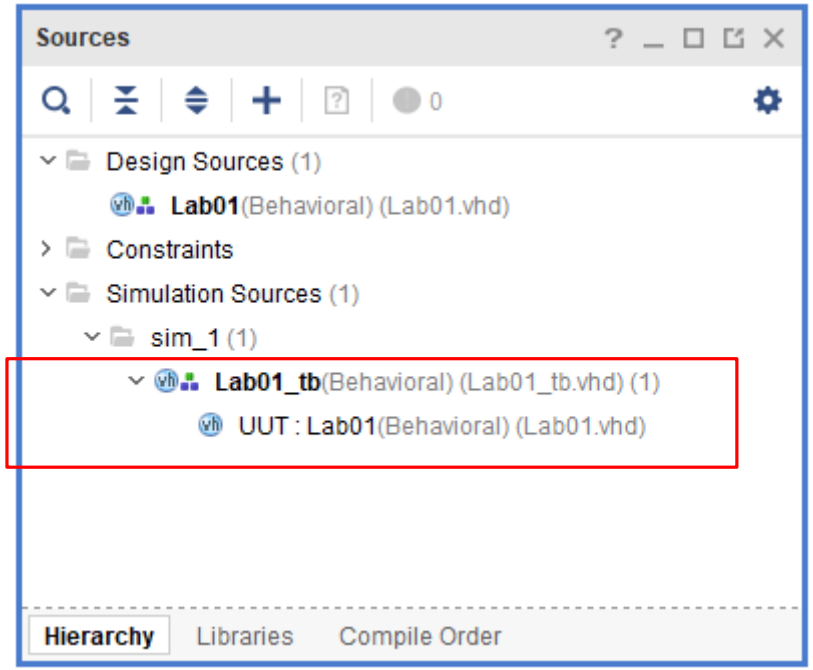
Lab 01-Part I

- Component Instantiation

Lab01_tb.vhd | Lab01.vhd | Untitled 1

M:/HSN_Undervisning/EFDP1100_V2018/Lab01_HieuNguyen/Lab01_HieuNguyen.srcs/sim_1/new/Lat

```
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Lab01_tb is
35  --  Port ( );
36  end Lab01_tb;
37
38  architecture Behavioral of Lab01_tb is
39
40  -------------Declare  component here
41  component Lab01
42      Port ( i0 : in STD_LOGIC;
43             i1 : in STD_LOGIC;
44             eq : out STD_LOGIC);
45  end component Lab01;
46
47  ---------- Internal Singal Declaration----
48  signal i0_tb: std_logic;
49  signal i1_tb: std_logic;
50  signal eq_tb: std_logic;
51
52  begin
53
54  UUT: Lab01
55  port map (i0 => i0_tb,i1 => i1_tb, eq => eq_tb);
56
57  process
58      begin
59          ---------------vector 1--------
```



Lab 01-Part I

- Generate Test Vectors

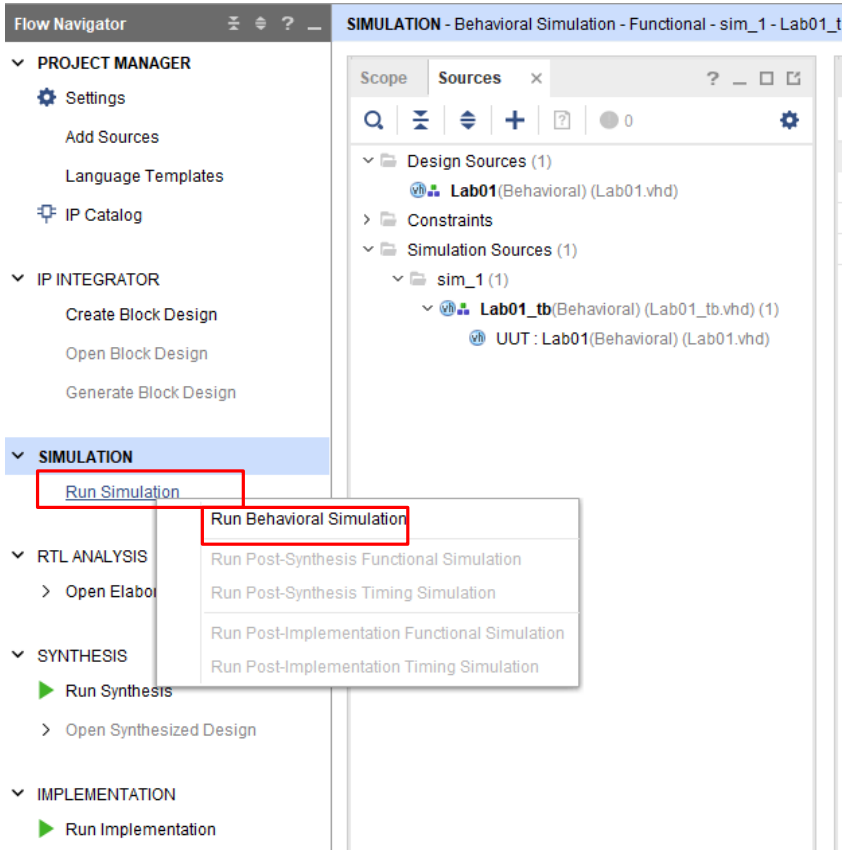
Lab01_tb.vhd | Lab01.vhd | Untitled 1

M:/HSN_Undervisning/EFDP1100_V2018/Lab01_HieuNguyen/Lab01_HieuNguyen.srcs/sim_1/new/Lal

```
47      ---------- Internal Singal Declaration----
48      signal i0_tb: std_logic;
49      signal il_tb: std_logic;
50      signal eq_tb: std_logic;
51
52      begin
53
54      UUT: Lab01
55      port map (i0 => i0_tb,il => il_tb, eq => eq_tb);
56
57      process
58          begin
59              ---------------vector 1--------
60              i0_tb <= '0';
61              il_tb <= '0';
62              wait for 40 ns;
63
64              --------vector 2---------------
65              i0_tb <= '0';
66              il_tb <= '1';
67              wait for 40 ns;
68
69               --------vector 3---------------
70              i0_tb <= '1';
71              il_tb <= '0';
72              wait for 40 ns;
73              --------vector 3---------------
74              i0_tb <= '1';
75              il_tb <= '1';
76              wait;
77          end process;
78
79      end Behavioral;
80
```

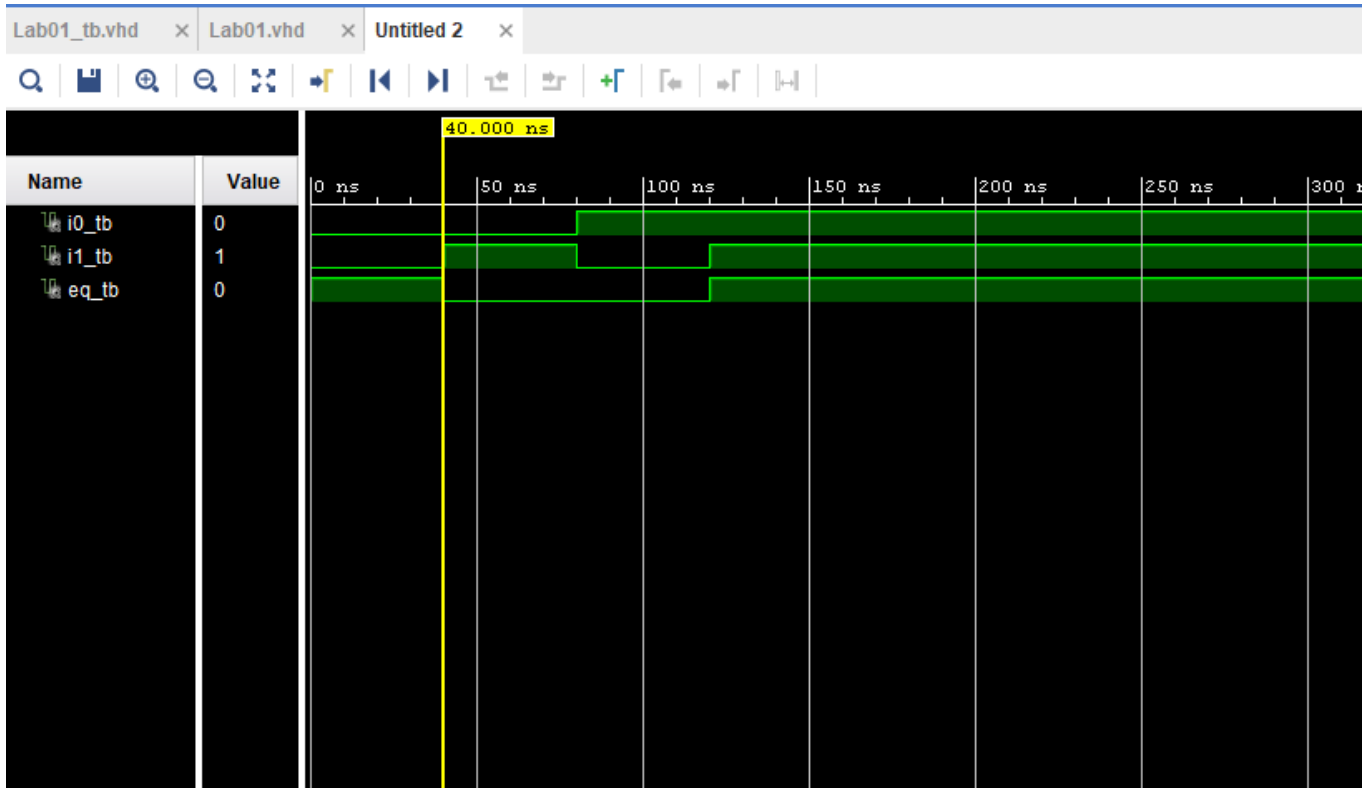
Lab 01-Part I

- Click on Run Simulation and then choose Run Behavioral Simulation



Lab 01-Part I

- We will se the simulation waveform



Lab 01-Part I

Send your design file and testbench file to report for part I

Lab 01- Part II: Students do following tasks

- Follow the steps in Part I to create a project for 2-bit comparator
- Create a design for 2-bit comparator in your project
- Create the testbench to test 2-bit comparator
- Run behavioral simulation
- Send your 2-bit comparator design and testbench to report for your lab