

Lab 01

HIEU NGUYEN

Lab 01-Part I

In this lab, students use the 1-bit comparator and two bit comparator to simulate the behavior of the circuit

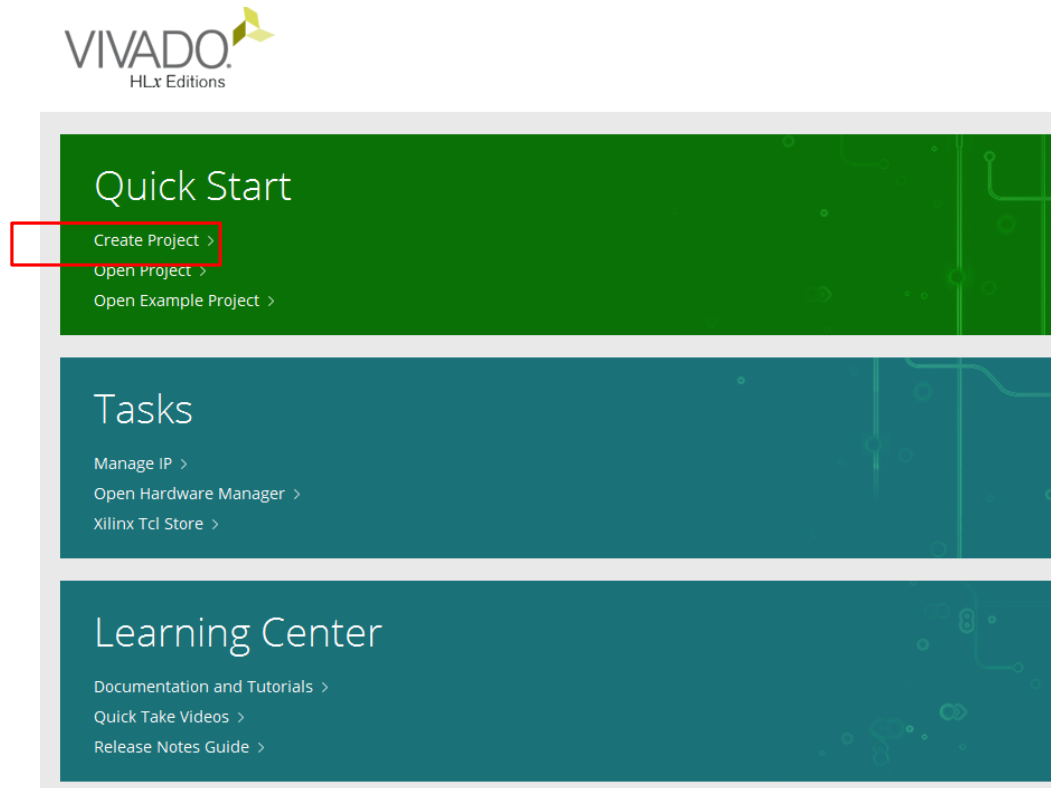
Lab 01-Part I

- Step 1: Create a folder on your computer with your own name (for example: Lab01)
- Step 2: Click on Vivado 2017.x on the desktop to open Vivado



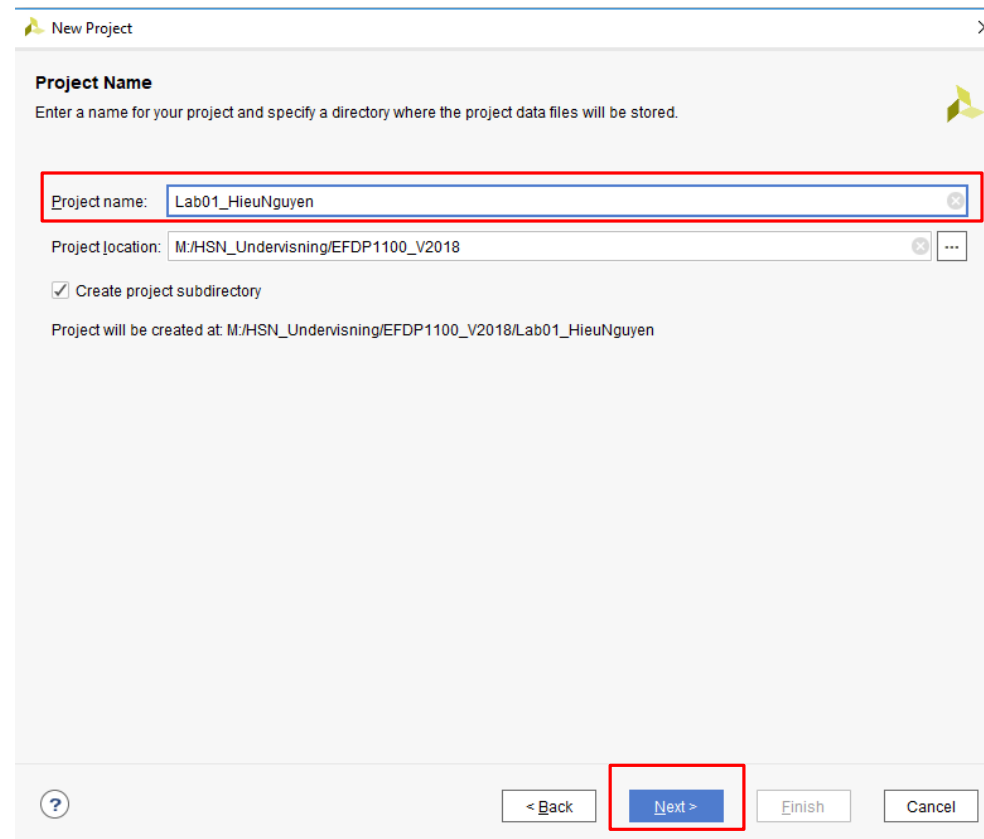
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- Step 3: Under quick start, click on Create project, then click Next



Lab 01-Part I

- Step 4: Choose project Name: Lab01_YourName, then click next



New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: Lab01_HieuNguyen

Project location: M:/HSN_Undervisning/EFDP1100_V2018

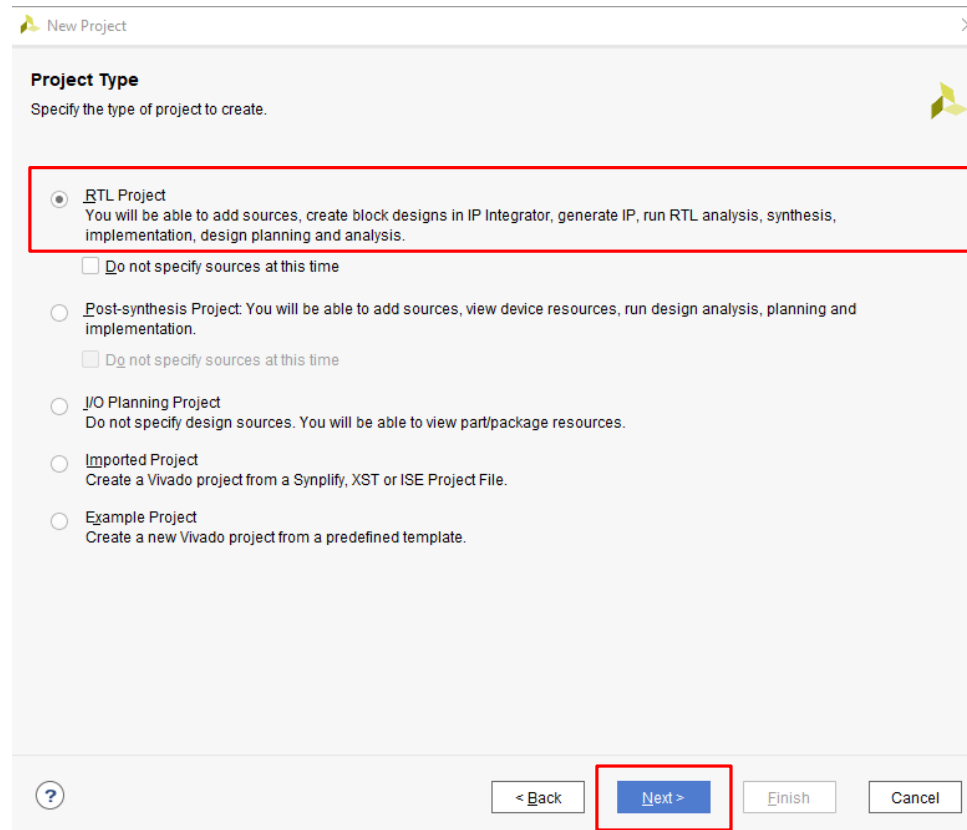
☒ Create project subdirectory

Project will be created at: M:/HSN_Undervisning/EFDP1100_V2018/Lab01_HieuNguyen

< Back Next > Finish Cancel

Lab 01-Part I

- Step 5: Choose RTL Project and click Next



New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time



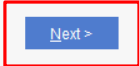


☐ **Post-synthesis Project**: You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

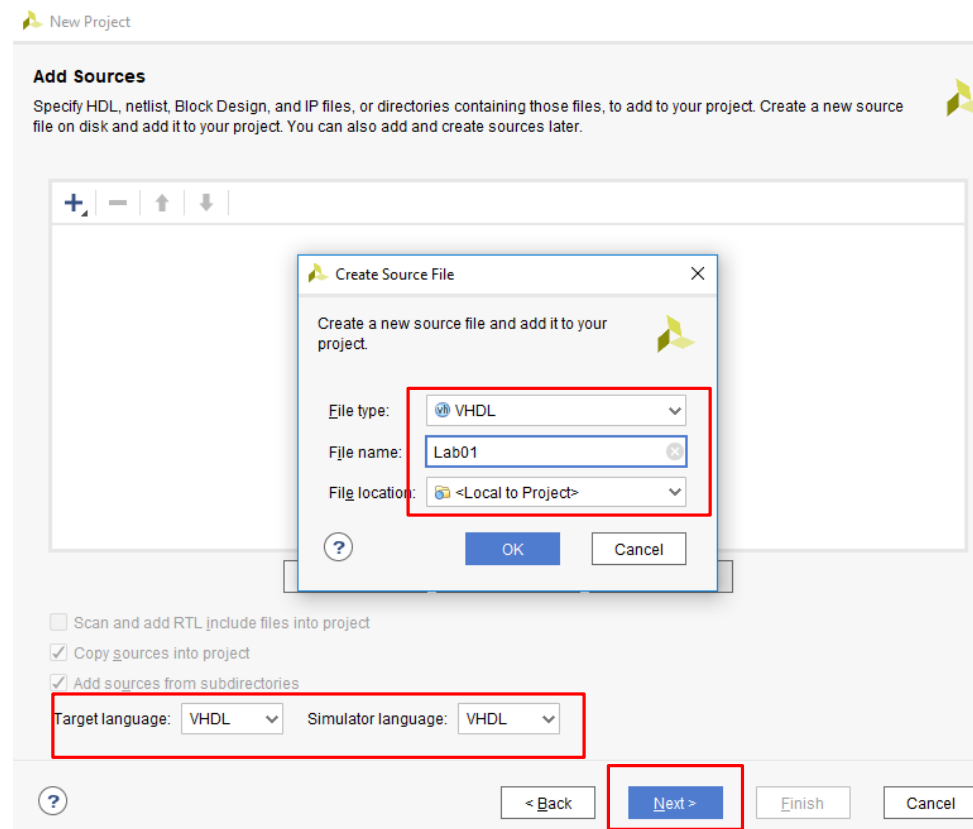
☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

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- Step 7: Choose the file name (For example: Lab01). Then click OK. Remember to choose File Type as VHDL



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- Step 8: Check to guarantee that Target language is set to VHDL and Simulator language is VHDL. Then click NEXT

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Index	Name	Library	HDL Source For	Location
1	Lab01.vhd	xil_defaultlib	Synthesis & Simulation	<Local to Project>

Add Files Add Directories Create File

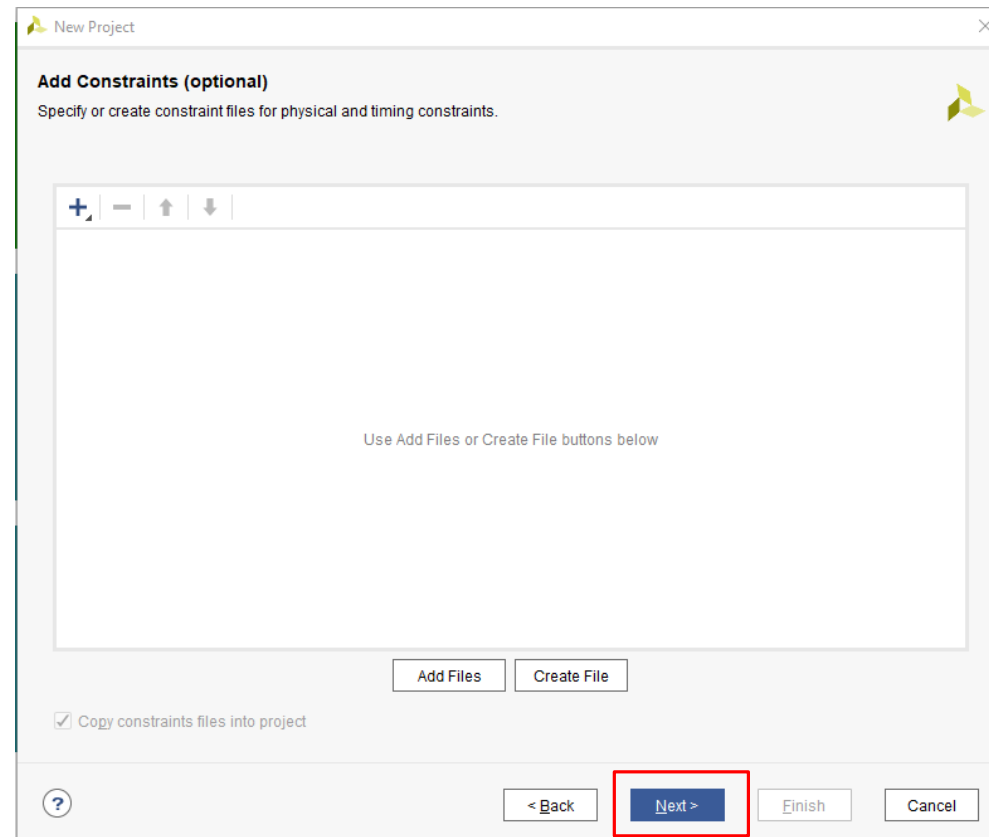
☐ Scan and add RTL include files into project
☒ Copy sources into project
☒ Add sources from subdirectories

Target language: VHDL Simulator language: VHDL

< Back Next > Finish Cancel

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- Step 9: Click NEXT (We don't use Constraint yet)



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- Step 10: Choose equipment and click NEXT

New Project

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Select: ☐ Parts ☒ Boards

Filter/Preview

Vendor: All
Display Name: All
Board Rev: Latest
Reset All Filters

Search:

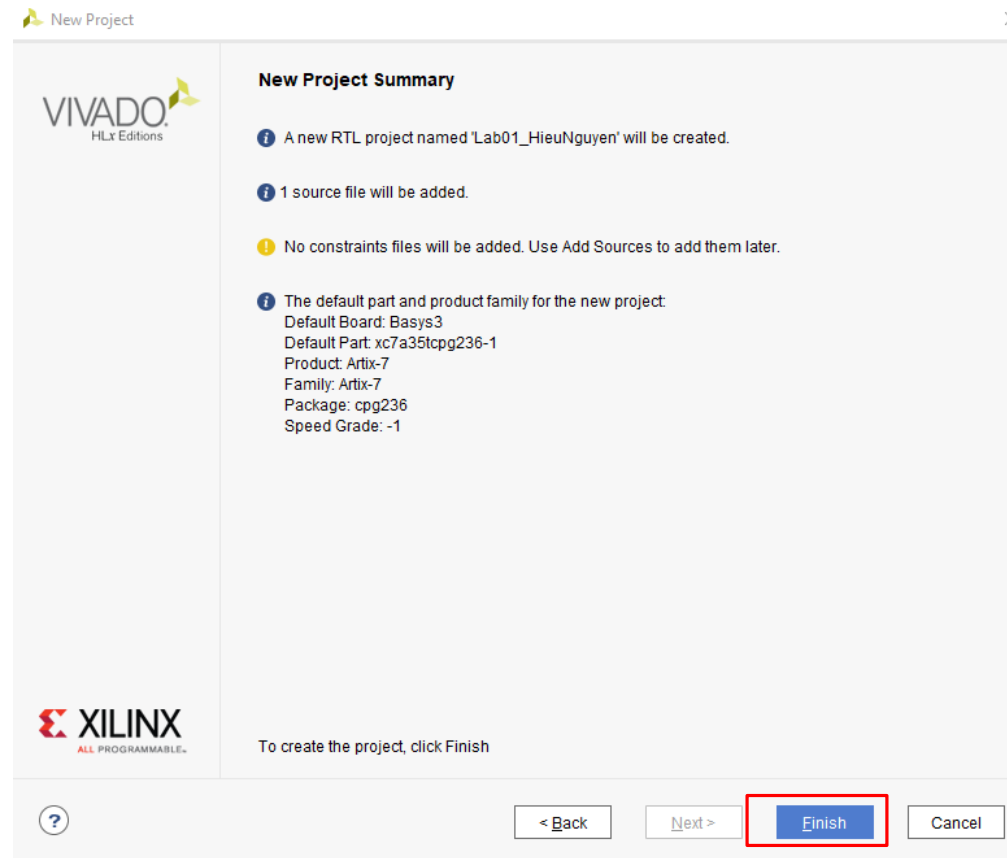
Display Name	Vendor	Board Rev	Part	I/O Pin Count
Arty	digilentinc.com	C.0	xc7a35ticsq324-1L	324
Basys3	digilentinc.com	C.0	xc7a35tcpq236-1	236
Cmod A7-15t	digilentinc.com	B.0	xc7a15tcpq236-1	236
Cmod A7-35t	digilentinc.com	B.0	xc7a35tcpq236-1	236

No Board Connectors

< Back Next > Finish Cancel

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- Project summary: Click NEXT



Lab 01-Part I

- Step 11: Define the input and output signals (i0, i1, eq) and click OK

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Entity name: Lab01

Architecture name: Behavioral

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
i0	in	<input type="checkbox"/>	0	0
i1	in	<input type="checkbox"/>	0	0
eq	out	<input type="checkbox"/>	0	0

?

OK Cancel

Lab 01-Part I

- Step 12: Click on Lab01 under Design Sources to open Lab01.vhd

The screenshot displays the Xilinx IDE interface. On the left, the 'Flow Navigator' pane shows the project structure. The 'PROJECT MANAGER' pane is active, showing the 'Sources' tab. A red rectangle highlights the 'Lab01(Behavioral) (Lab01.vhd)' file under 'Design Sources (1)'. The 'Source File Properties' window is open, showing the following details for 'Lab01.vhd':

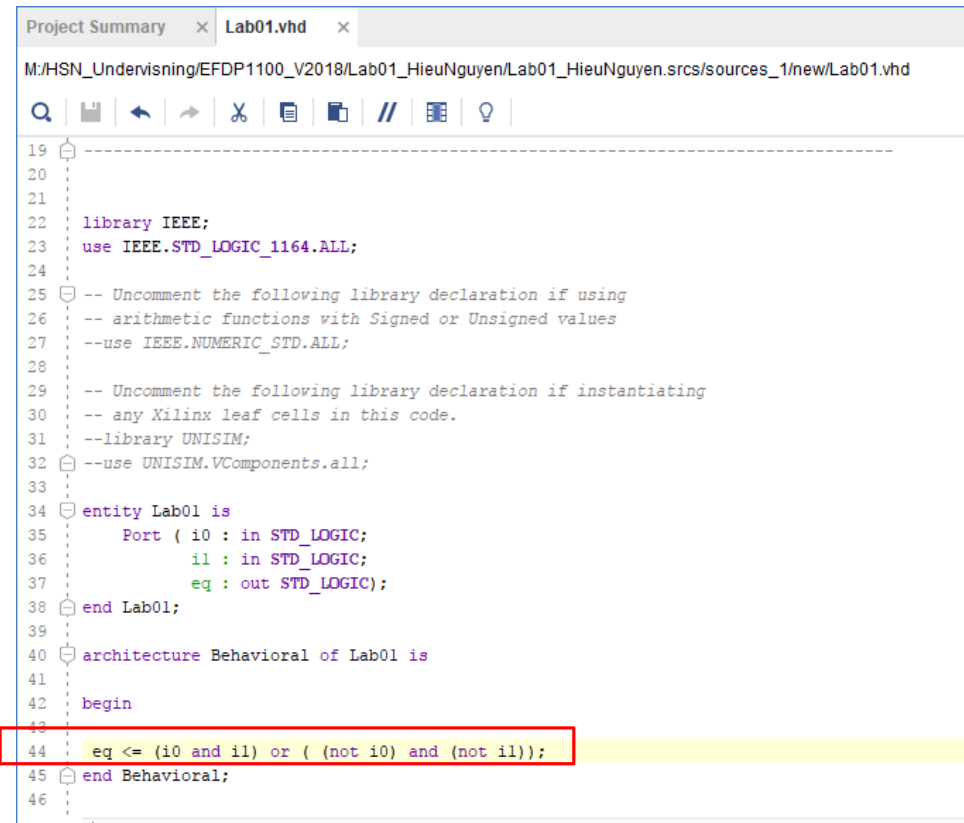
- Enabled: ☒
- Location: M:/HSN_Undervisning/EFDP1100_V2018/Lab01
- Type: VHDL
- Library: xil_defaultlib
- Size: 1.0 KB

The 'Design Runs' table at the bottom shows the status of synthesis and implementation:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed f
synth_1	constrs_1	Not started							
impl_1	constrs_1	Not started							

Lab 01-Part I

- Step 13: Edit the text in window next to Sources

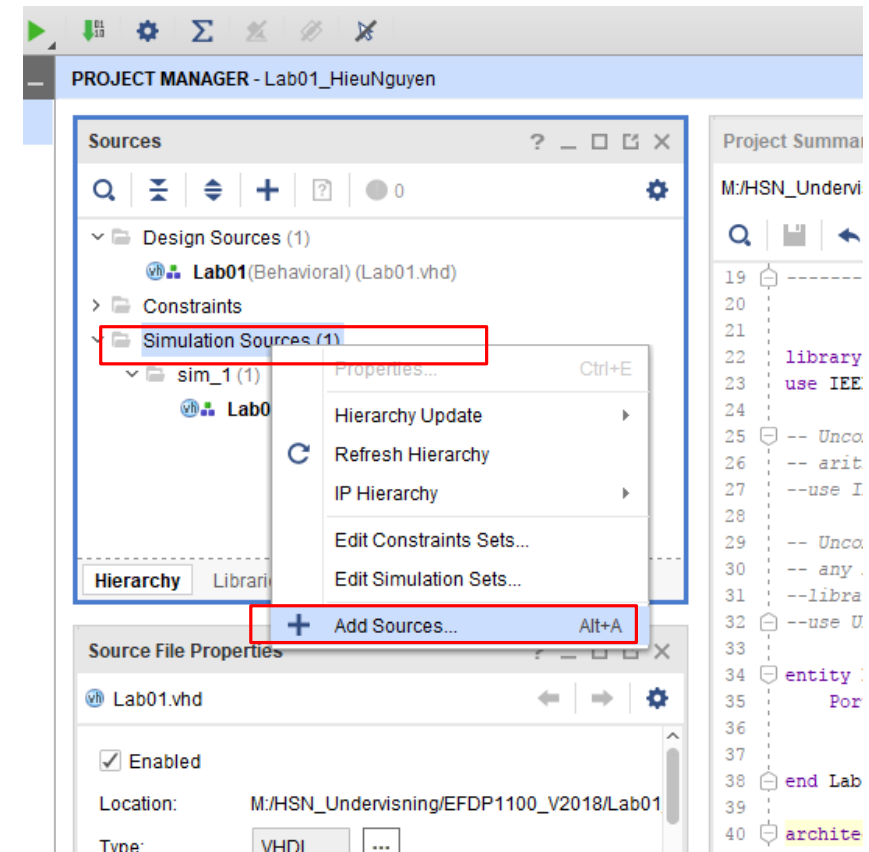


```
Project Summary x Lab01.vhd x
M:/HSN_Undervisning/EFDP1100_V2018/Lab01_HieuNguyen/Lab01_HieuNguyen.srscs/sources_1/new/Lab01.vhd

19 -----
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity Lab01 is
35     Port ( i0 : in STD_LOGIC;
36           i1 : in STD_LOGIC;
37           eq : out STD_LOGIC);
38 end Lab01;
39
40 architecture Behavioral of Lab01 is
41
42 begin
43
44     eq <= (i0 and il) or ( (not i0) and (not il));
45 end Behavioral;
46
```

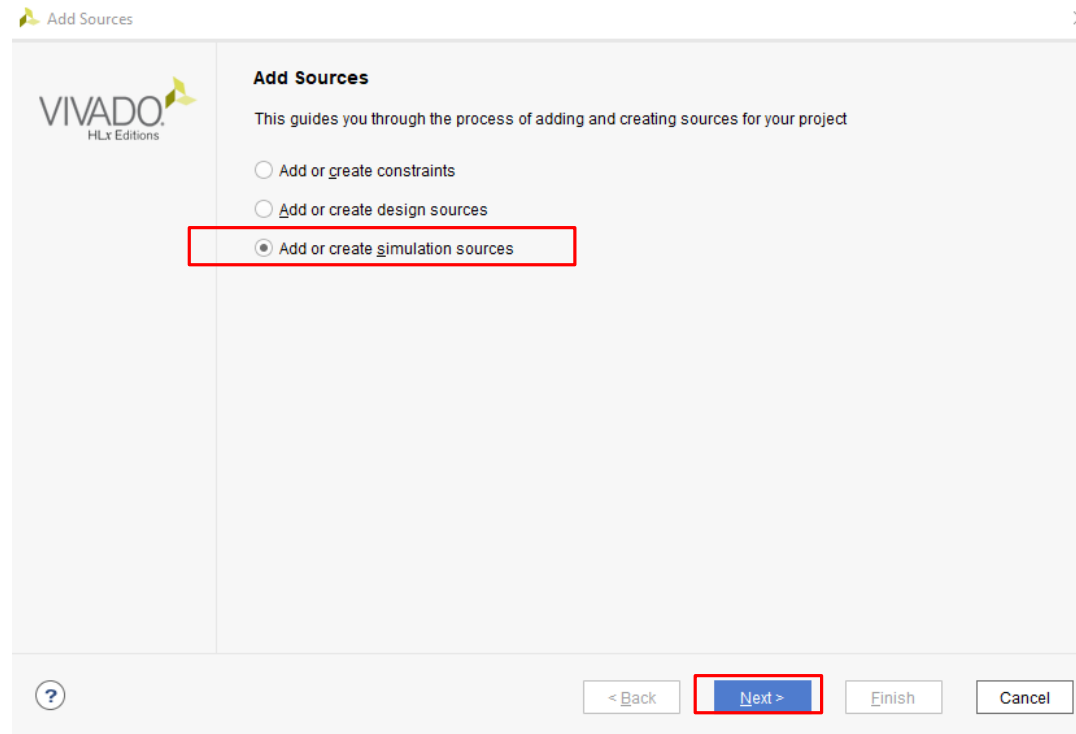
Lab 01-Part I

- Step 14: Create Testbench. Right click on Simulation Sources and choose Add Sources



Lab 01-Part I

- Choose Add or create simulation sources. Then click NEXT



Lab 01-Part I

- Choose Create File

Add Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

Use Add Files, Add Directories or Create File buttons below

Add Files Add Directories Create File

☐ Scan and add RTL include files into project

☒ Copy sources into project

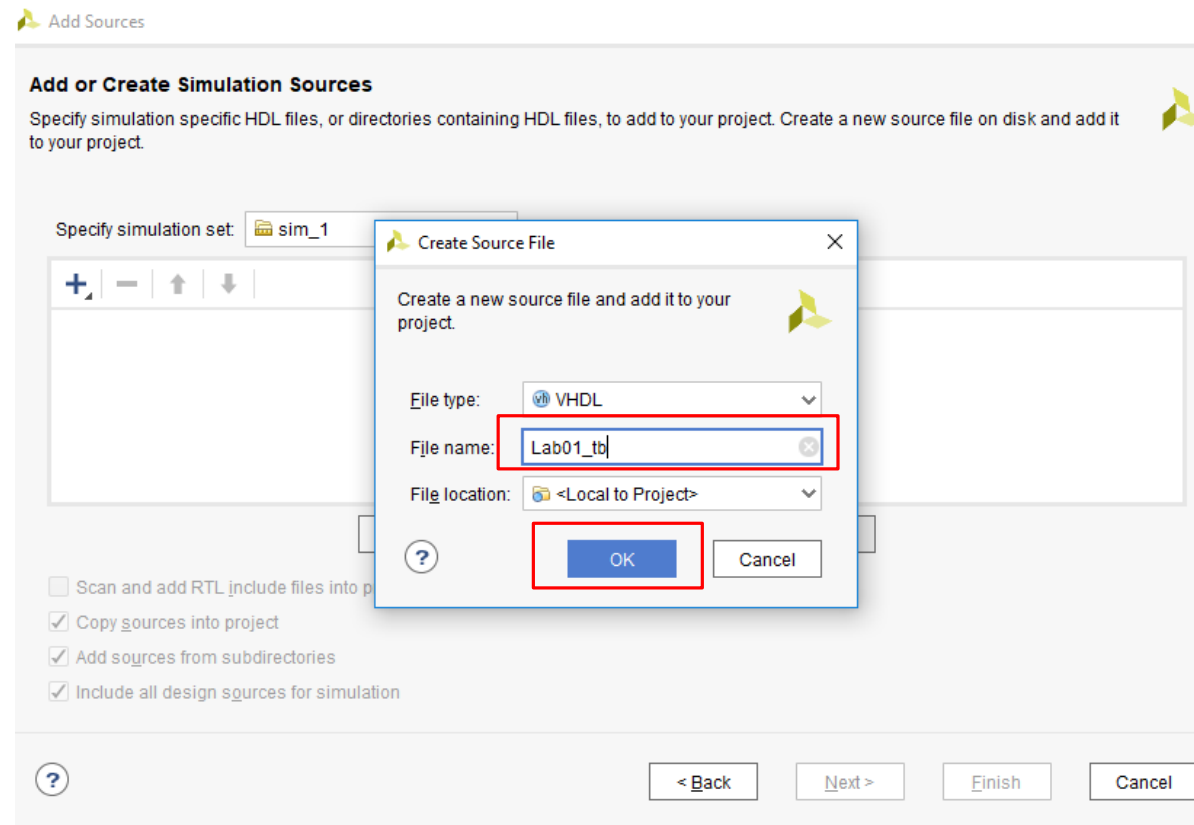
☒ Add sources from subdirectories

☒ Include all design sources for simulation

? < Back Next > Finish Cancel


Lab 01-Part I

- Choose File Name for example Lab01_tb. Then click OK




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- Click Finish




 Add Sources ✕

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set:  sim_1 ▼

	Index	Name	Library	Location
	1	Lab01_tb.vhd	xil_defaultlib	<Local to Project>


  

☐ Scan and add RTL include files into project

☒ Copy sources into project

☒ Add sources from subdirectories

☒ Include all design sources for simulation

 < Back Next > Finish Cancel

Lab 01-Part I

- Click OK

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Entity name:

Architecture name:

I/O Port Definitions

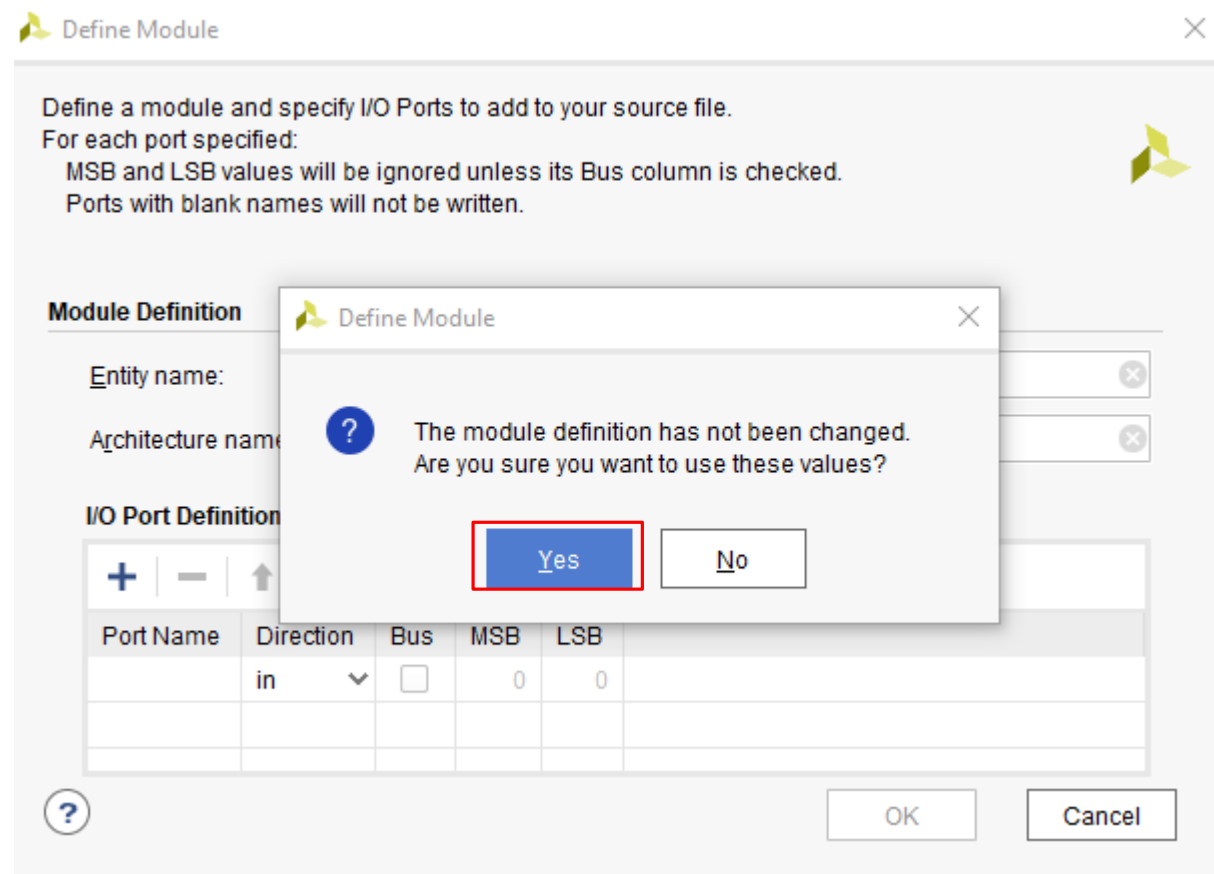
Port Name	Direction	Bus	MSB	LSB
	in	<input type="checkbox"/>	0	0

?

OK Cancel

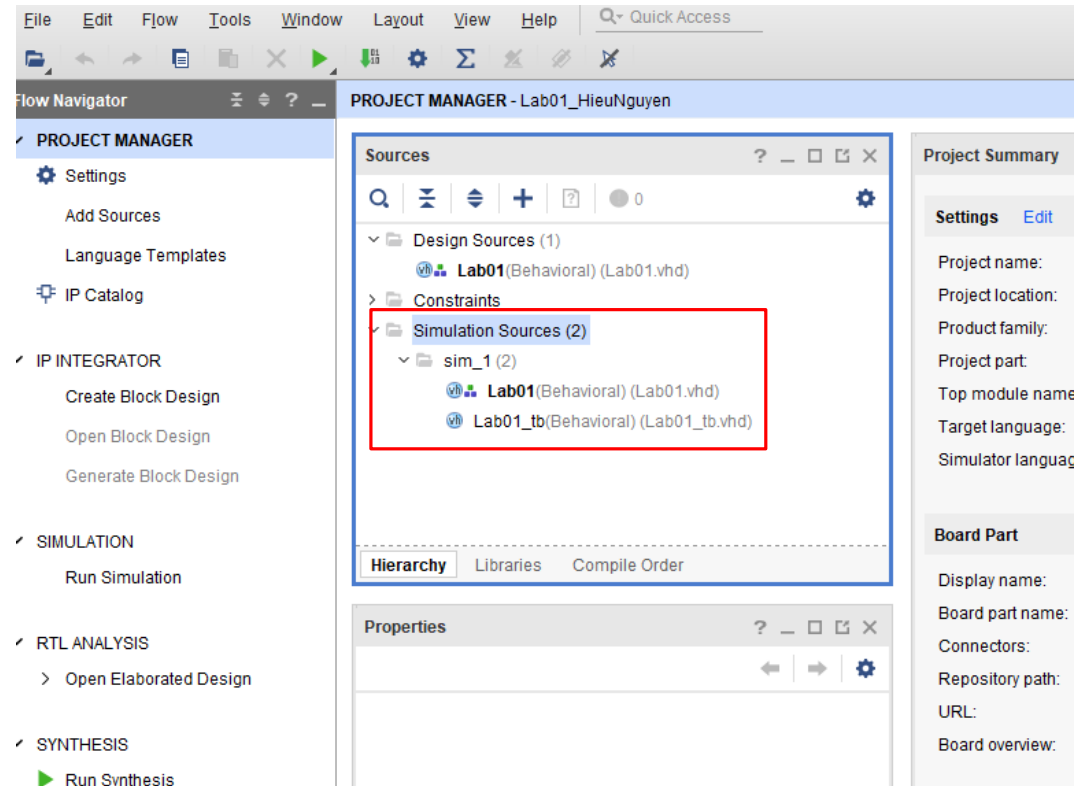
Lab 01-Part I

- Click Yes



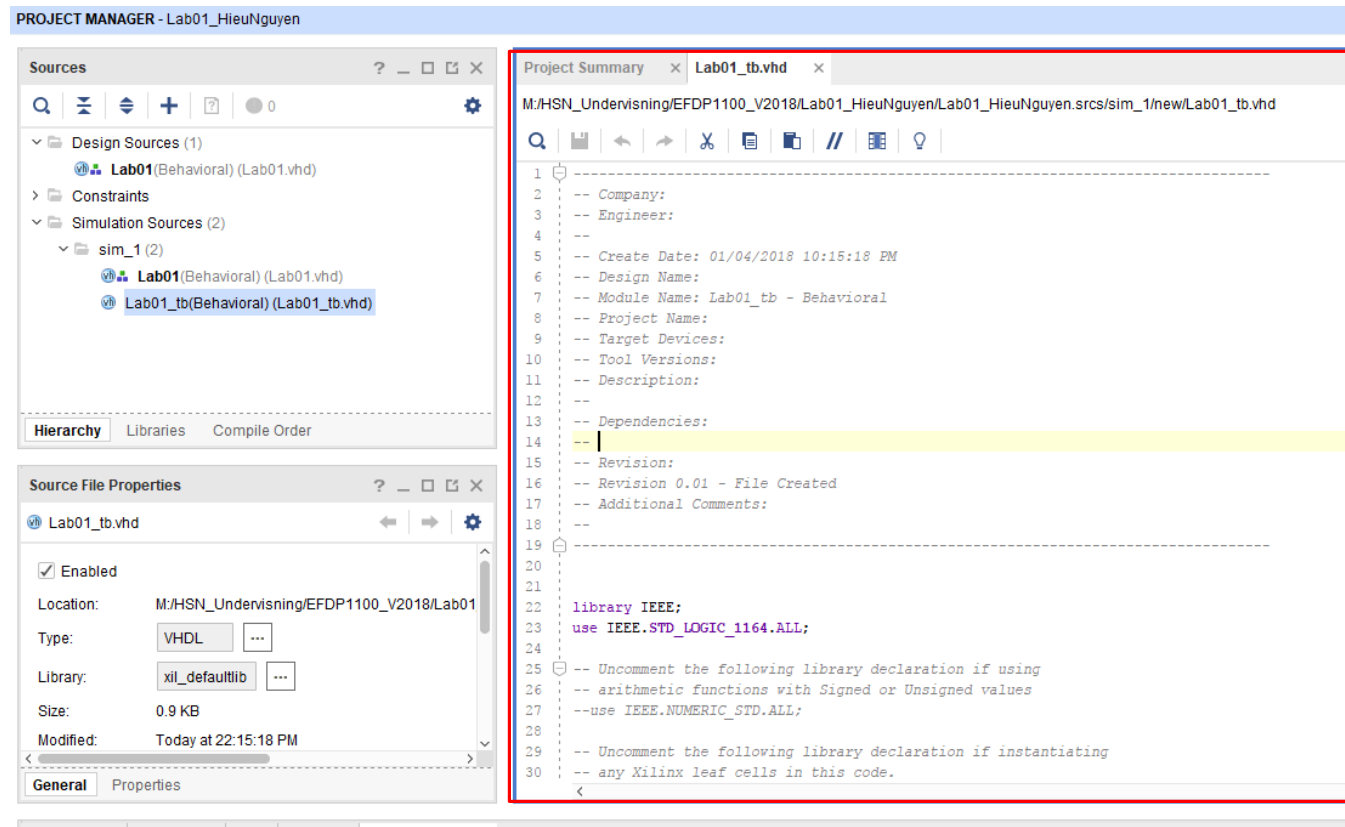
Lab 01-Part I

- Now we have testbench file under Simulation Sources



Lab 01-Part I

- Double click on Lab01_tb to open the text editor



Text editor

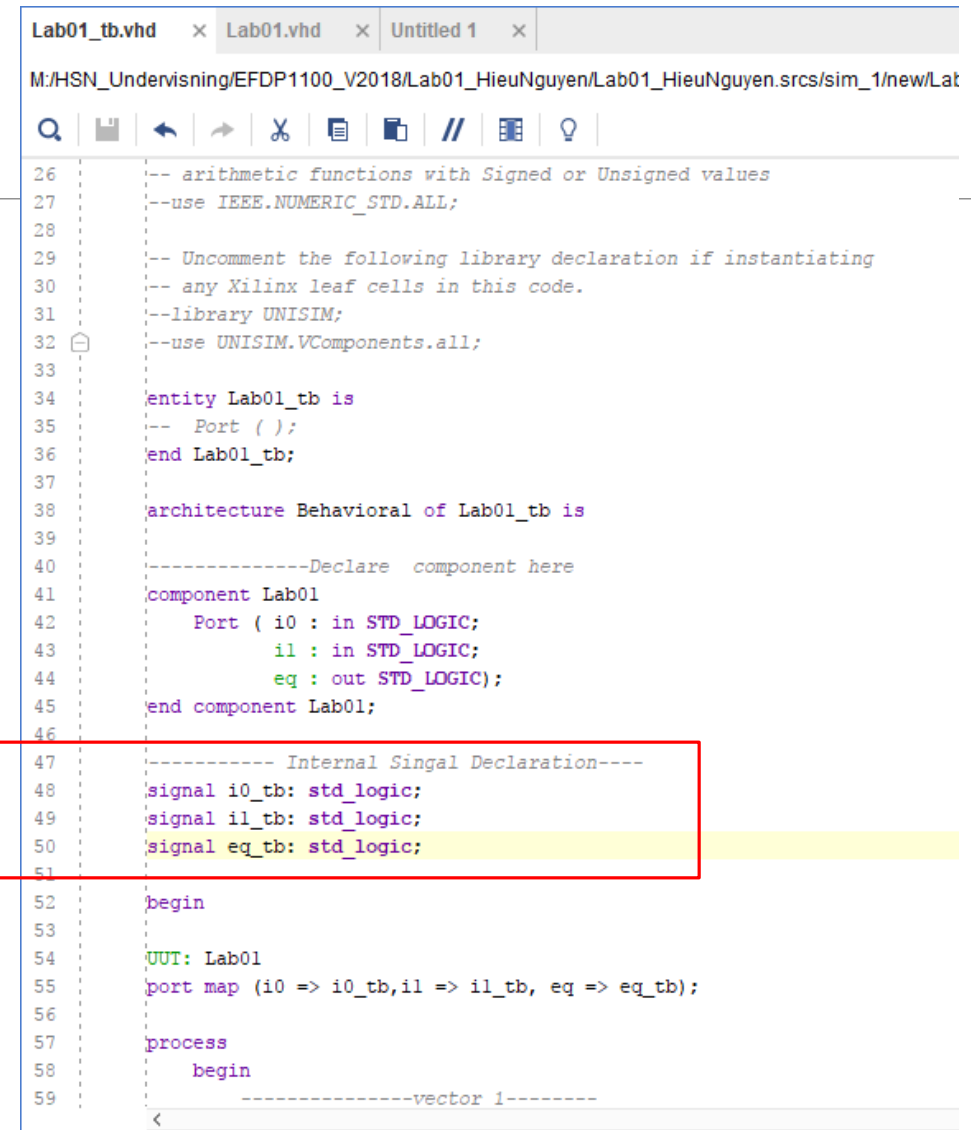
Lab 01-Part I

- Component declaration

```
34  entity Lab01_tb is
35  -- Port ( );
36  end Lab01_tb;
37
38  architecture Behavioral of Lab01_tb is
39
40  //-----Declare component here
41  component Lab01
42      Port ( i0 : in STD_LOGIC;
43            i1 : in STD_LOGIC;
44            eq : out STD_LOGIC);
45  end component Lab01;
46  begin
47
48
49  end Behavioral;
50
```


Lab 01-Part I

- Internal Singal Declaration



The screenshot shows a VHDL code editor with three tabs: Lab01_tb.vhd, Lab01.vhd, and Untitled 1. The file path is M:/HSN_Undervisning/EFDP1100_V2018/Lab01_HieuNguyen/Lab01_HieuNguyen.srcs/sim_1/new/Lat. The code is as follows:

```
26      -- arithmetic functions with Signed or Unsigned values
27      --use IEEE.NUMERIC_STD.ALL;
28
29      -- Uncomment the following library declaration if instantiating
30      -- any Xilinx leaf cells in this code.
31      --library UNISIM;
32      --use UNISIM.VComponents.all;
33
34      entity Lab01_tb is
35      -- Port ( );
36      end Lab01_tb;
37
38      architecture Behavioral of Lab01_tb is
39
40      -----Declare component here
41      component Lab01
42      Port ( i0 : in STD_LOGIC;
43            i1 : in STD_LOGIC;
44            eq : out STD_LOGIC);
45      end component Lab01;
46
47      ----- Internal Singal Declaration-----
48      signal i0_tb: std_logic;
49      signal i1_tb: std_logic;
50      signal eq_tb: std_logic;
51
52      begin
53
54      UUT: Lab01
55      port map (i0 => i0_tb,i1 => i1_tb, eq => eq_tb);
56
57      process
58      begin
59      -----vector 1-----
```

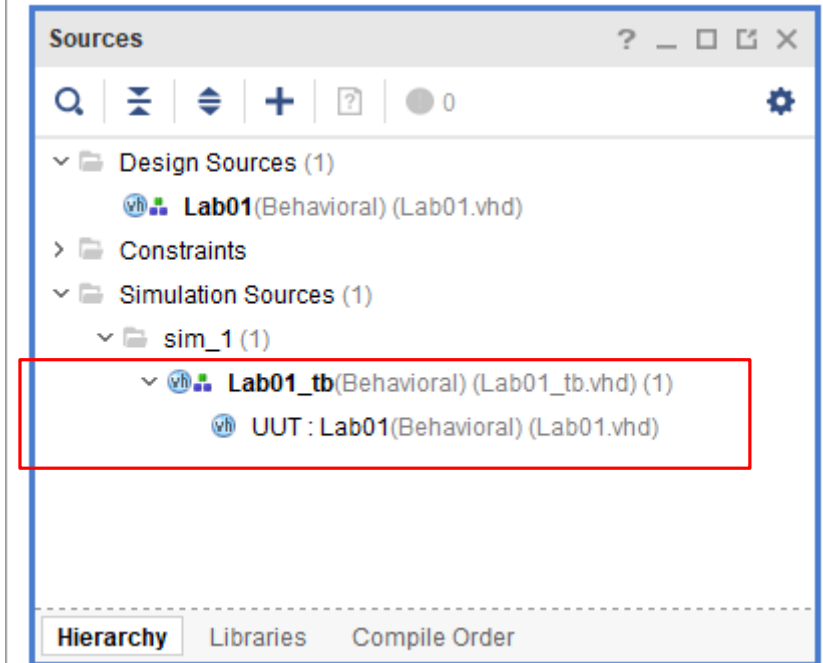
The internal signal declaration section (lines 47-50) is highlighted in yellow and enclosed in a red box. The signals declared are i0_tb, i1_tb, and eq_tb, all of type std_logic.

Lab 01-Part I

■ Component Instantiation

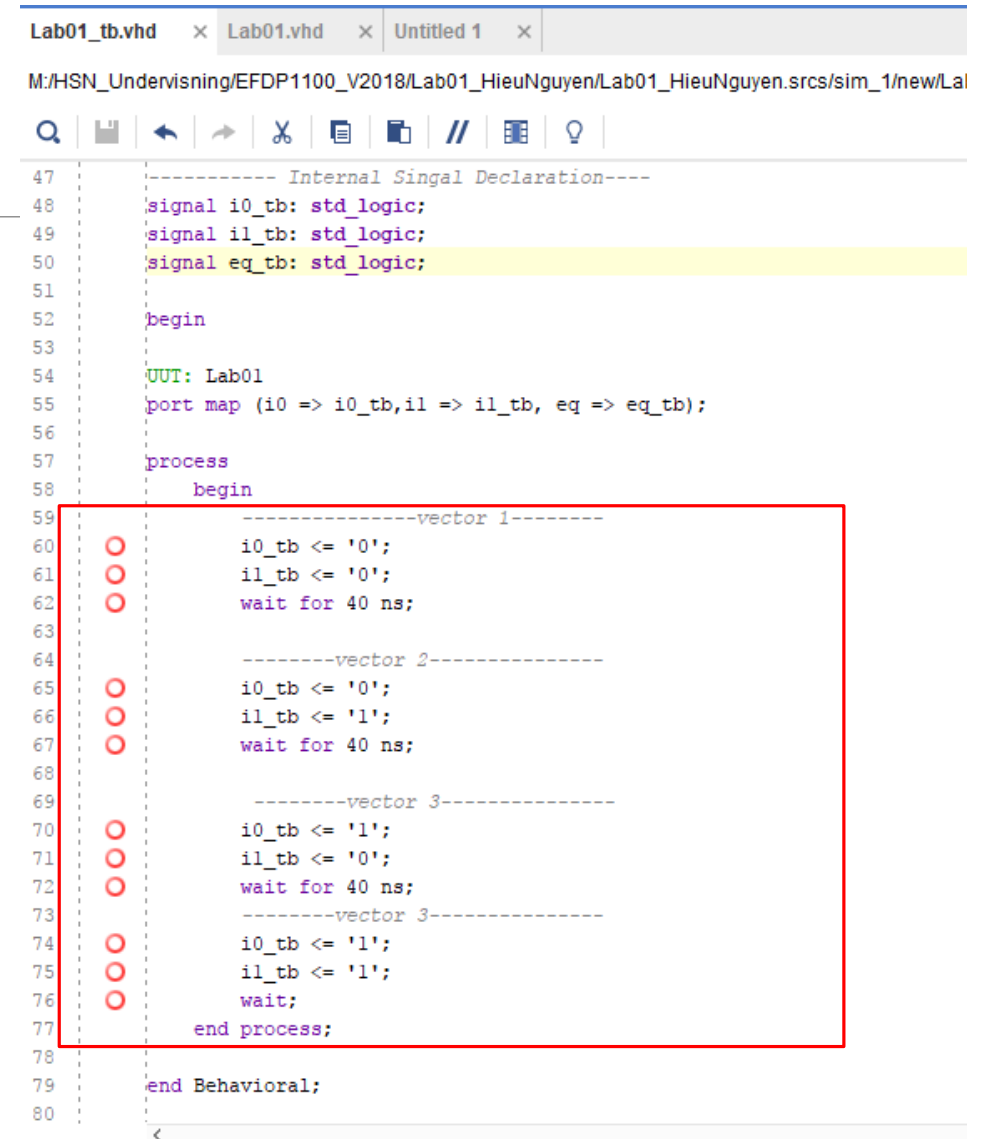
```
Lab01_tb.vhd x Lab01.vhd x Untitled 1 x
M:/HSN_Undervisng/EFDP1100_V2018/Lab01_HieuNguyen/Lab01_HieuNguyen.srcs/sim_1/new/Lat

26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Lab01_tb is
35  -- Port ( );
36  end Lab01_tb;
37
38  architecture Behavioral of Lab01_tb is
39
40  -----Declare component here
41  component Lab01
42  Port ( i0 : in STD_LOGIC;
43        i1 : in STD_LOGIC;
44        eq : out STD_LOGIC);
45  end component Lab01;
46
47  ----- Internal Singal Declaration-----
48  signal i0_tb: std_logic;
49  signal i1_tb: std_logic;
50  signal eq_tb: std_logic;
51
52  begin
53
54  UUT: Lab01
55  port map (i0 => i0_tb,i1 => i1_tb, eq => eq_tb);
56
57  process
58  begin
59  -----vector 1-----
60
```



Lab 01-Part I

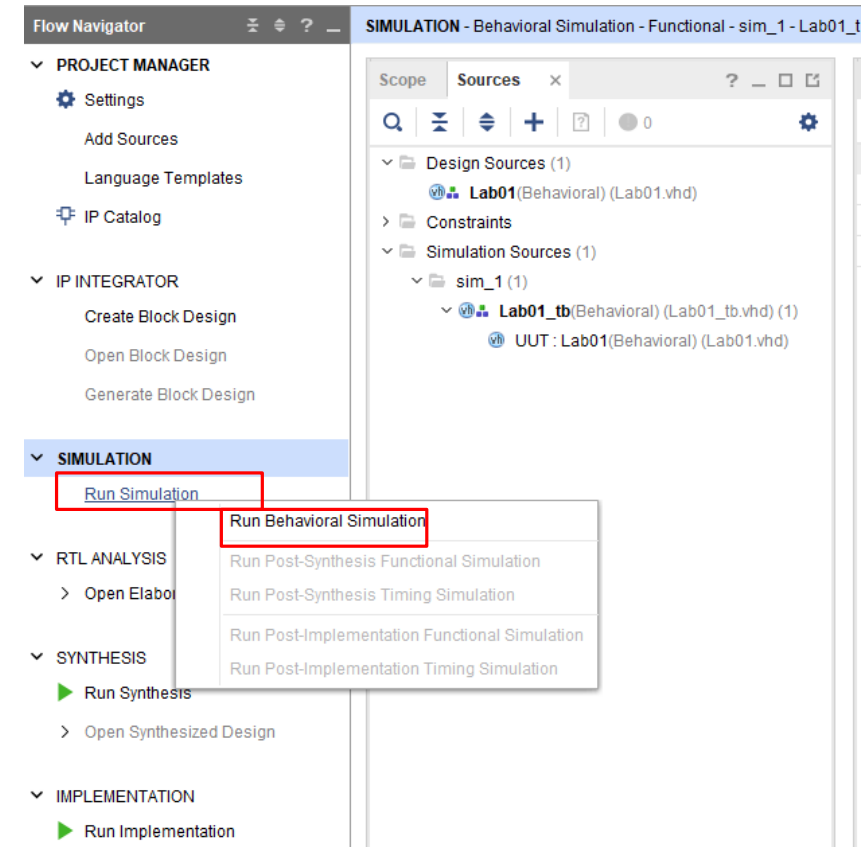
- Generate Test Vectors



```
Lab01_tb.vhd x Lab01.vhd x Untitled 1 x
M:/HSN_Undervisning/EFDP1100_V2018/Lab01_HieuNguyen/Lab01_HieuNguyen.srcs/sim_1/new/Lab01_tb.vhd
47 ----- Internal Singal Declaration-----
48 signal i0_tb: std_logic;
49 signal il_tb: std_logic;
50 signal eq_tb: std_logic;
51
52 begin
53
54 UUT: Lab01
55 port map (i0 => i0_tb, il => il_tb, eq => eq_tb);
56
57 process
58     begin
59         -----vector 1-----
60         i0_tb <= '0';
61         il_tb <= '0';
62         wait for 40 ns;
63
64         -----vector 2-----
65         i0_tb <= '0';
66         il_tb <= '1';
67         wait for 40 ns;
68
69         -----vector 3-----
70         i0_tb <= '1';
71         il_tb <= '0';
72         wait for 40 ns;
73         -----vector 3-----
74         i0_tb <= '1';
75         il_tb <= '1';
76         wait;
77     end process;
78
79 end Behavioral;
80
```

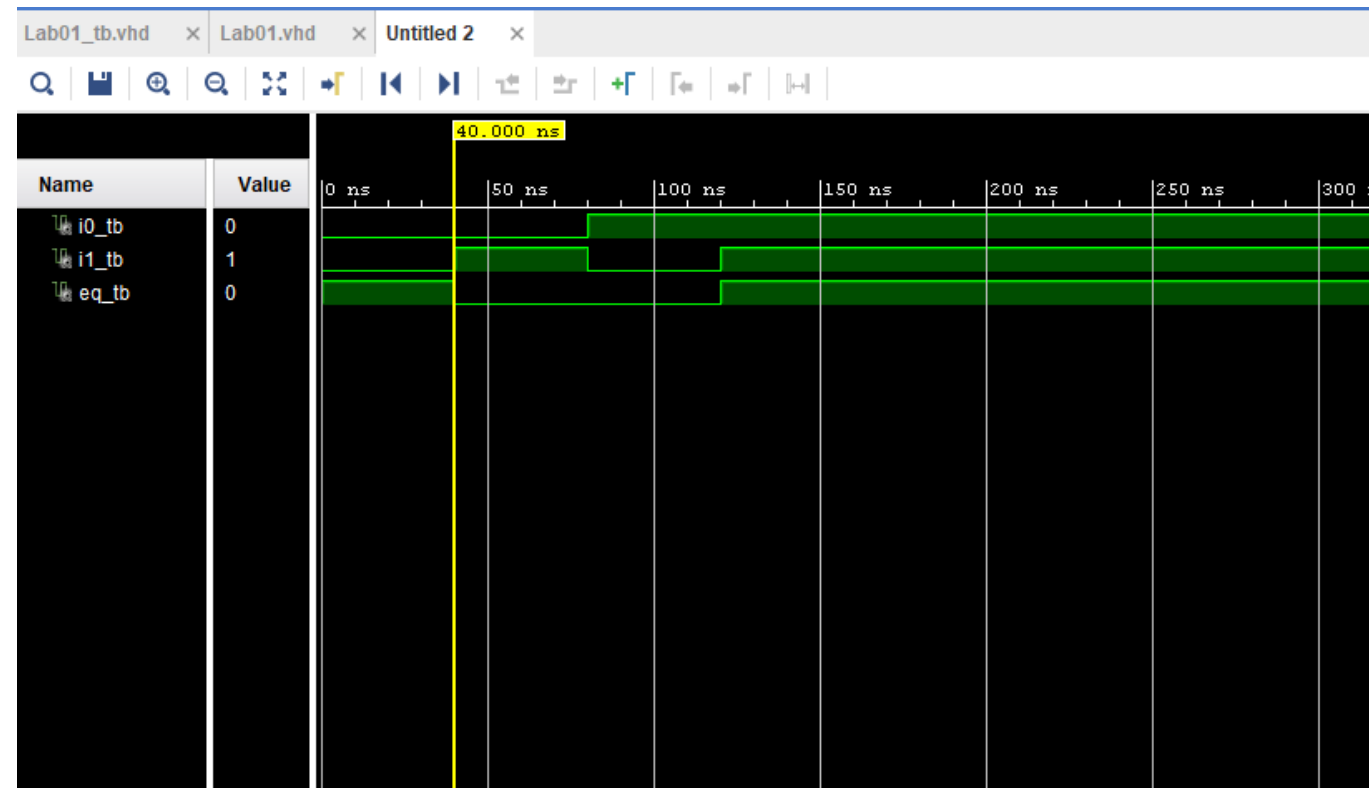
Lab 01-Part I

- Click on Run Simulation and then choose Run Behavioral Simulation



Lab 01-Part I

- We will see the simulation waveform



Lab 01-Part I

Send your design file and testbench file to report for part I

Lab 01- Part II: Students do following tasks

- Follow the steps in Part I to create a project for 2-bit comparator
- Create a design for 2-bit comparator in your project
- Create the testbench to test 2-bit comparator
- Run behavioral simulation
- Send your 2-bit comparator design and testbench to report for your lab