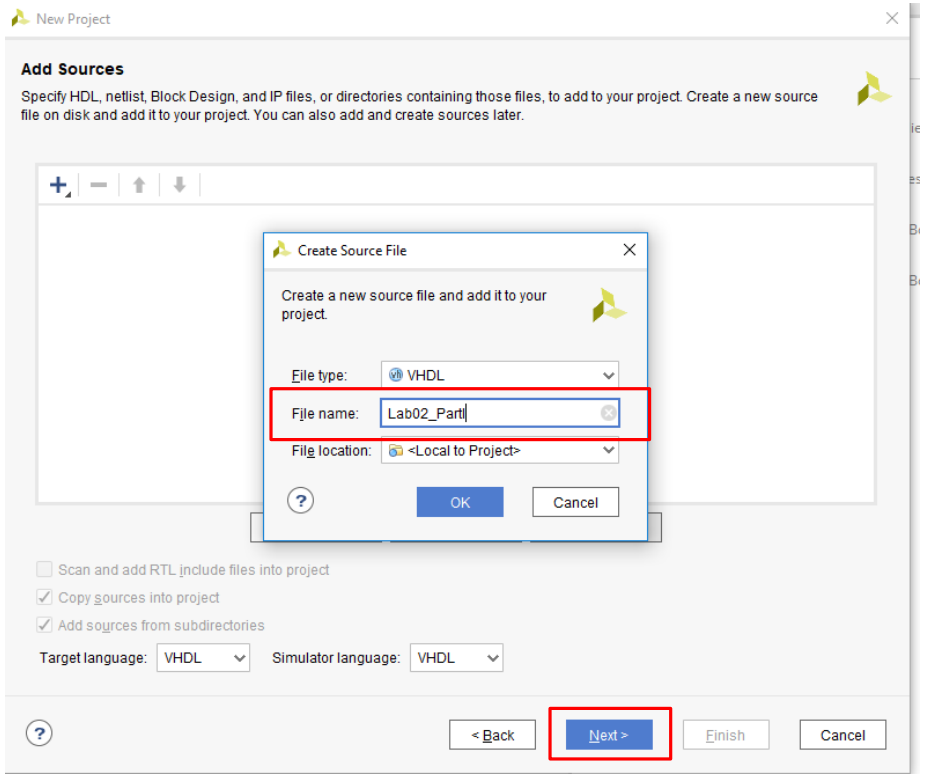
Lab 02

HIEU NGUYEN

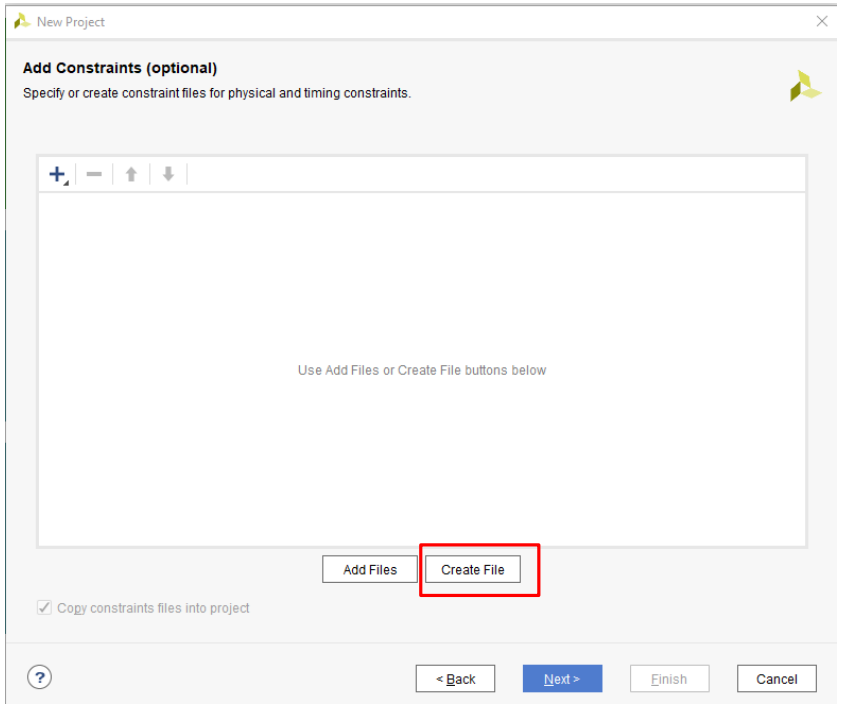
Lab 02-Part I

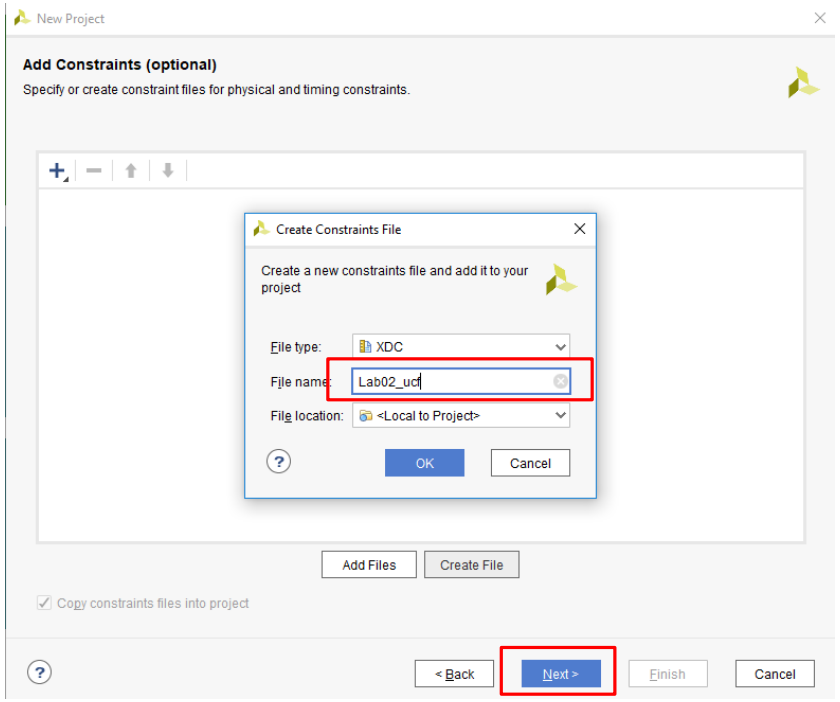
- Create a folder for your lab 02 (See Lab01 for more detail)
- Launch Vivado 2017.x (See Lab01 for more detail)
- Create a new project with name: Lab02_YourName
- Create a new VHDL-design file with the name: Lab02_partI



Lab 02-Part I

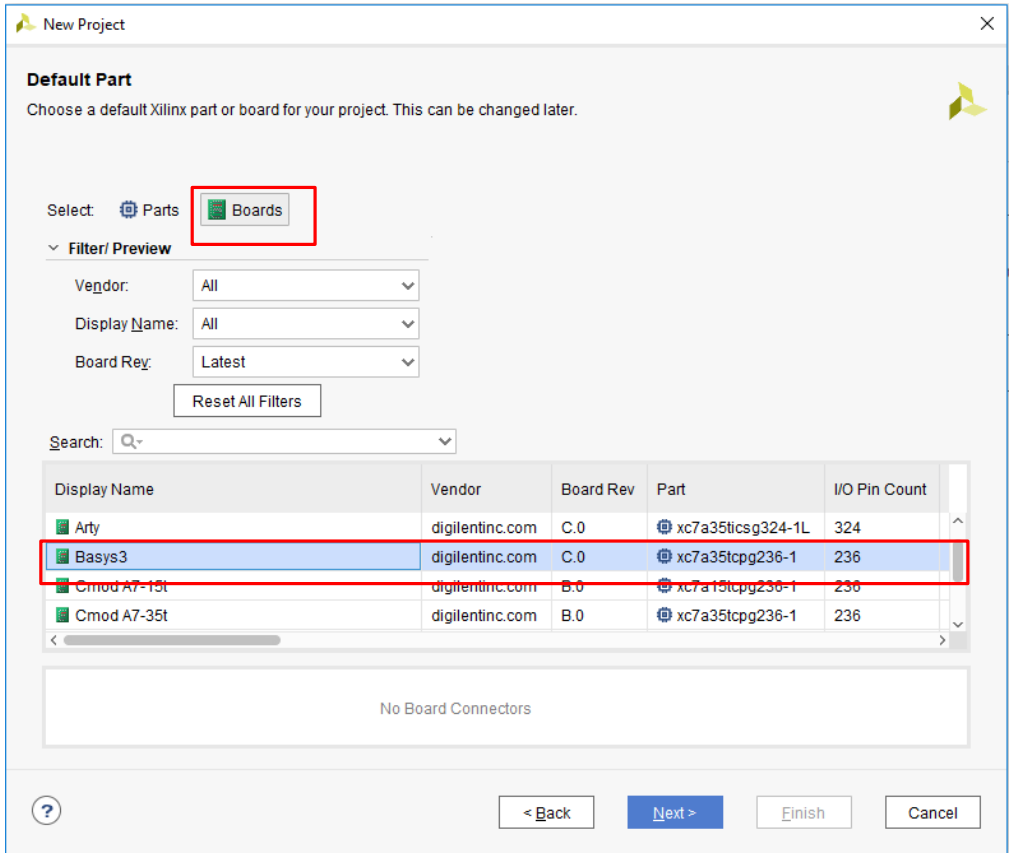
- Click on «Create File» to create constraint file with name: Lab02_ucf. Then click OK and then NEXT





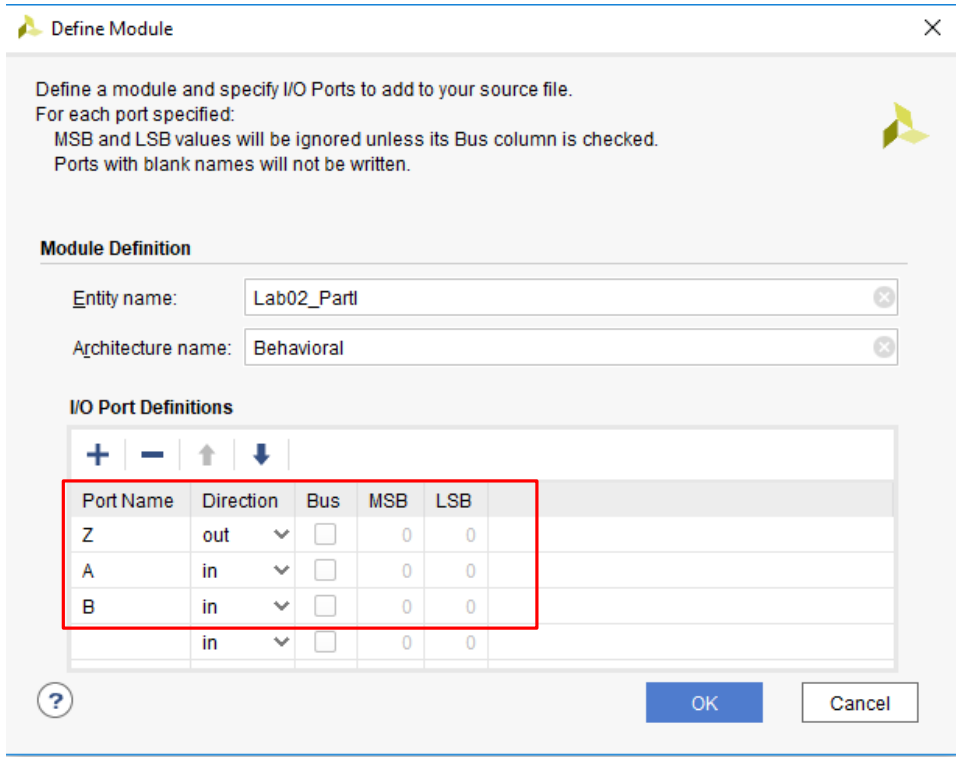
Lab 02-Part I

- Choose the board (Basys-3) as bellow



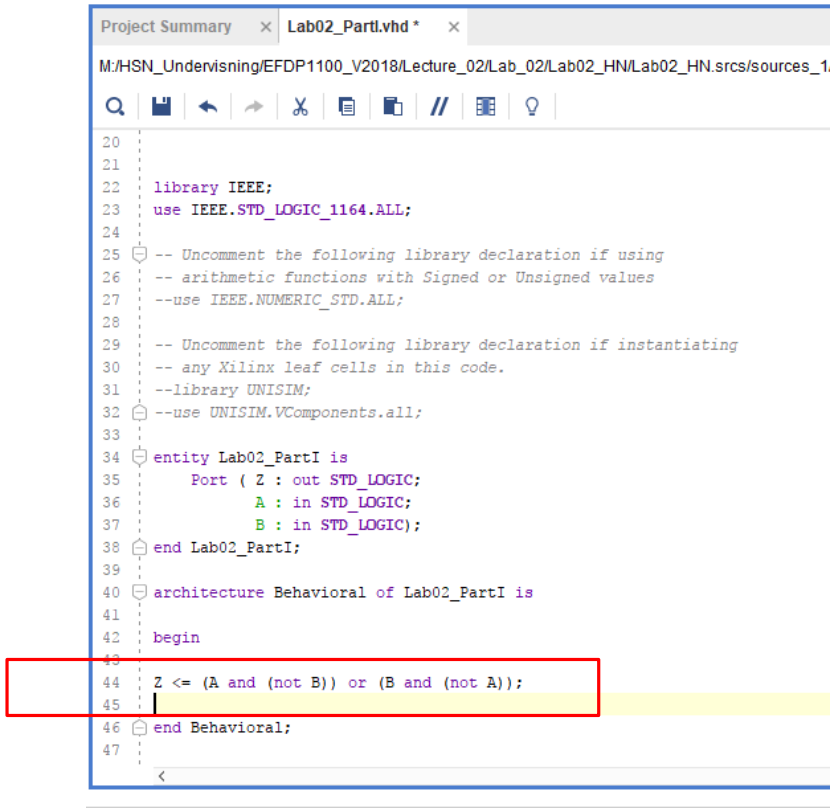
Lab 02-Part I

- Define input and output ports as below. Then click OK



Lab 02-Part I

- Edit Lab02_PartI by adding the following statement

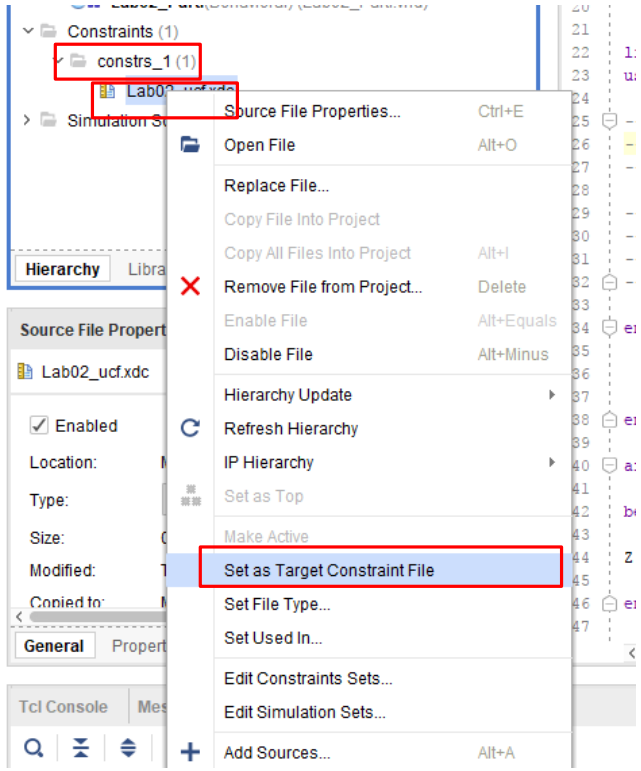


Lab 02-Part I

- Create the test bench with the name: Lab02_PartI_tb and generate the test vectors for this design (See Lab01 for more detail)
-

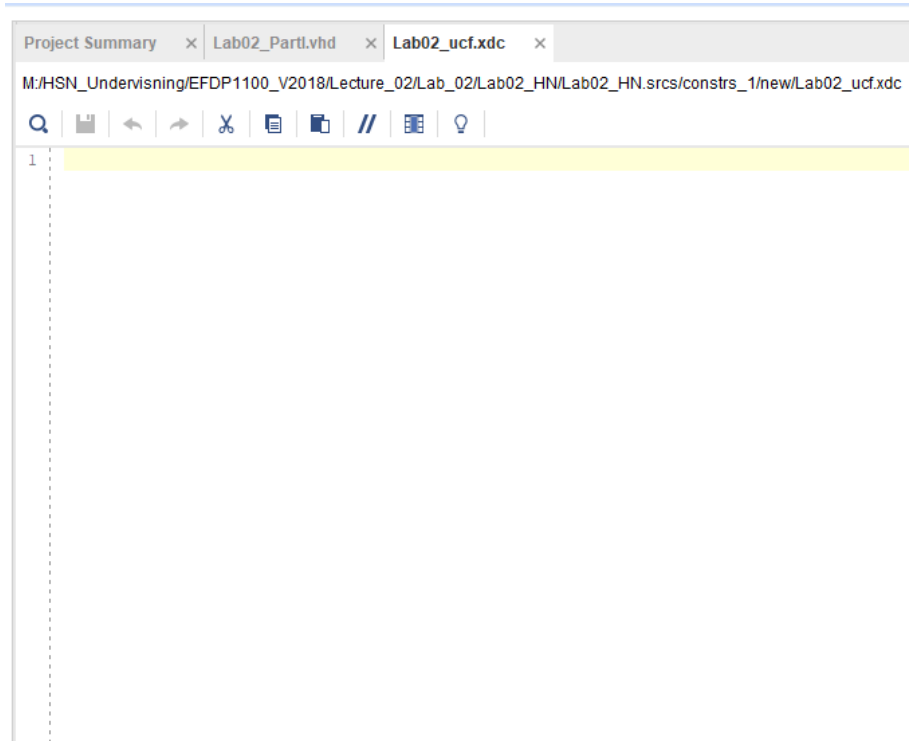
Lab 02-Part I

- Click on constrs_1 and then right click on Lab02_ucf and choose «Set target constraint file»



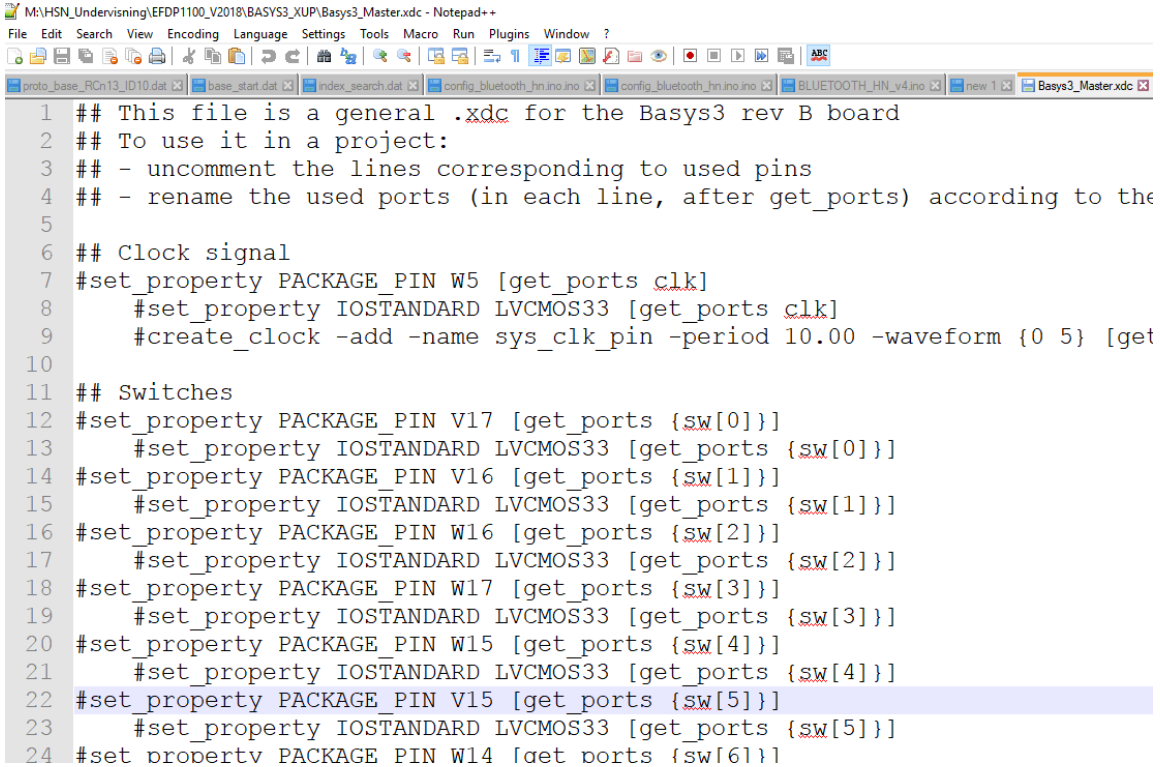
Lab 02-Part I

- Click on Lab02_ucf to edit the this file. Now the ucf-file is empty.



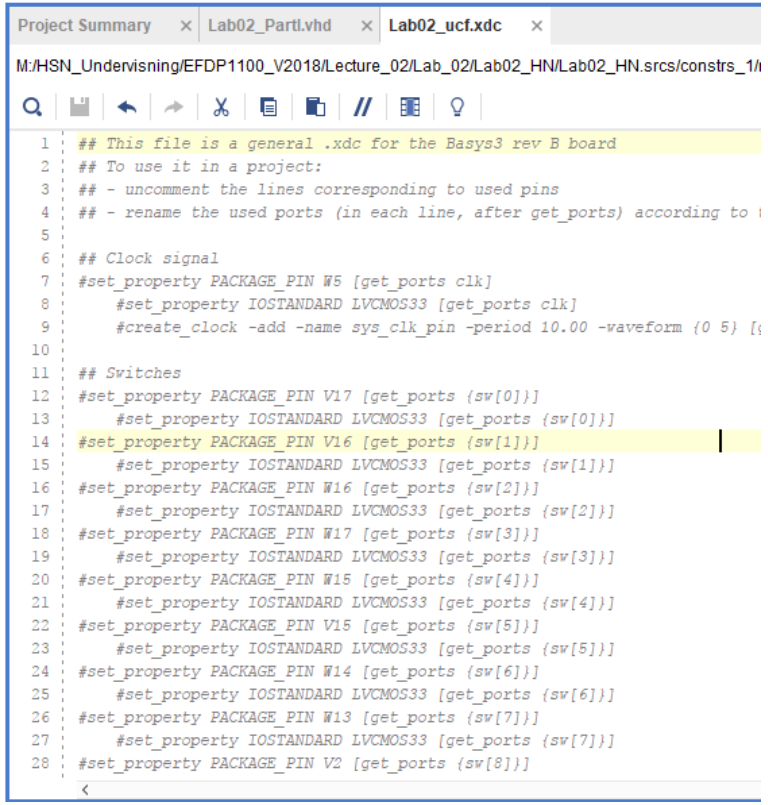
Lab 02-Part I

- Open xdc file from Digilent with notepad



Lab 02-Part I

- Copy all the content of xdc file from Digilent and paste in Lab02_ucf.dxc



Lab 02-Part I

- Enable line 12 and line 13 to use Switch 0 for input signal A
- Enable line 14 and line 15 to use Switch 1 for input signal B

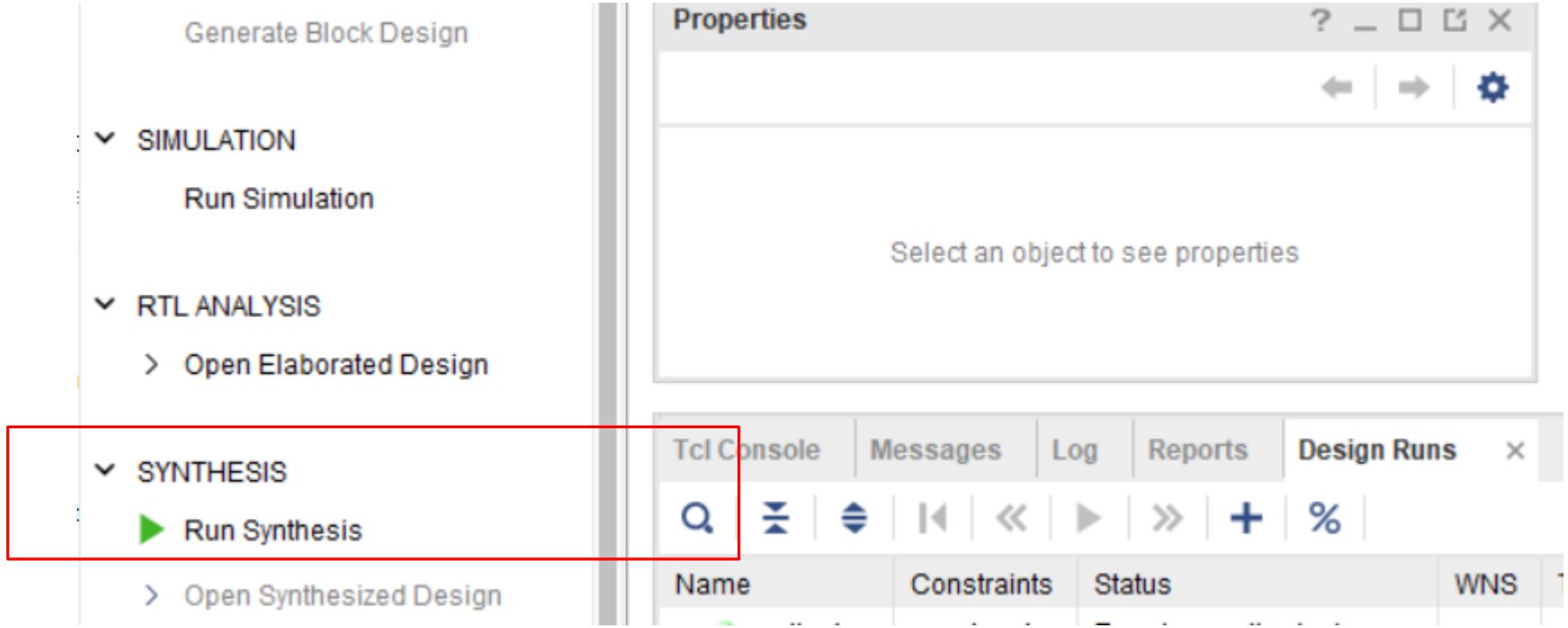
```
11  ## Switches
12  set_property PACKAGE_PIN V17 [get_ports {A}]
13      set_property IOSTANDARD LVCMOS33 [get_ports {A}]
14  set_property PACKAGE_PIN V16 [get_ports {B}]
15      set_property IOSTANDARD LVCMOS33 [get_ports {B}]
16  #set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
17      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
18  #set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
19      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
20  #set_property PACKAGE_PIN W15 [get_ports {sw[4]}]
```

- Enable line 47 and line 48 to use Led0 for output signal Z

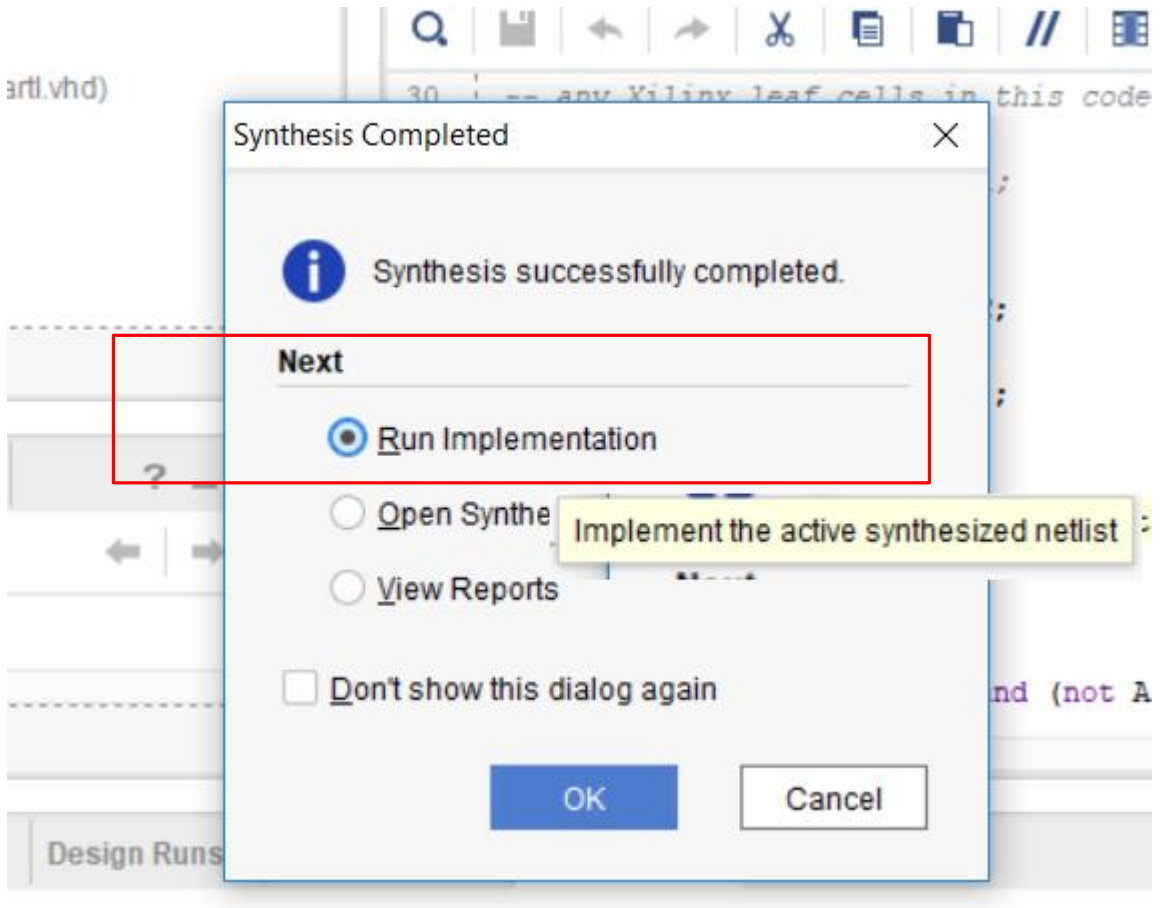
```
45
46  ## LEDs
47  set_property PACKAGE_PIN U16 [get_ports {Z}]
48      set_property IOSTANDARD LVCMOS33 [get_ports {Z}]
49  #set_property PACKAGE_PIN E19 [get_ports {led[1]}]
50      #set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]
51  #set_property PACKAGE_PIN U19 [get_ports {led[2]}]
52      #set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]
53  #set_property PACKAGE_PIN V19 [get_ports {led[3]}]
54      #set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]
```

Lab 02-Part I

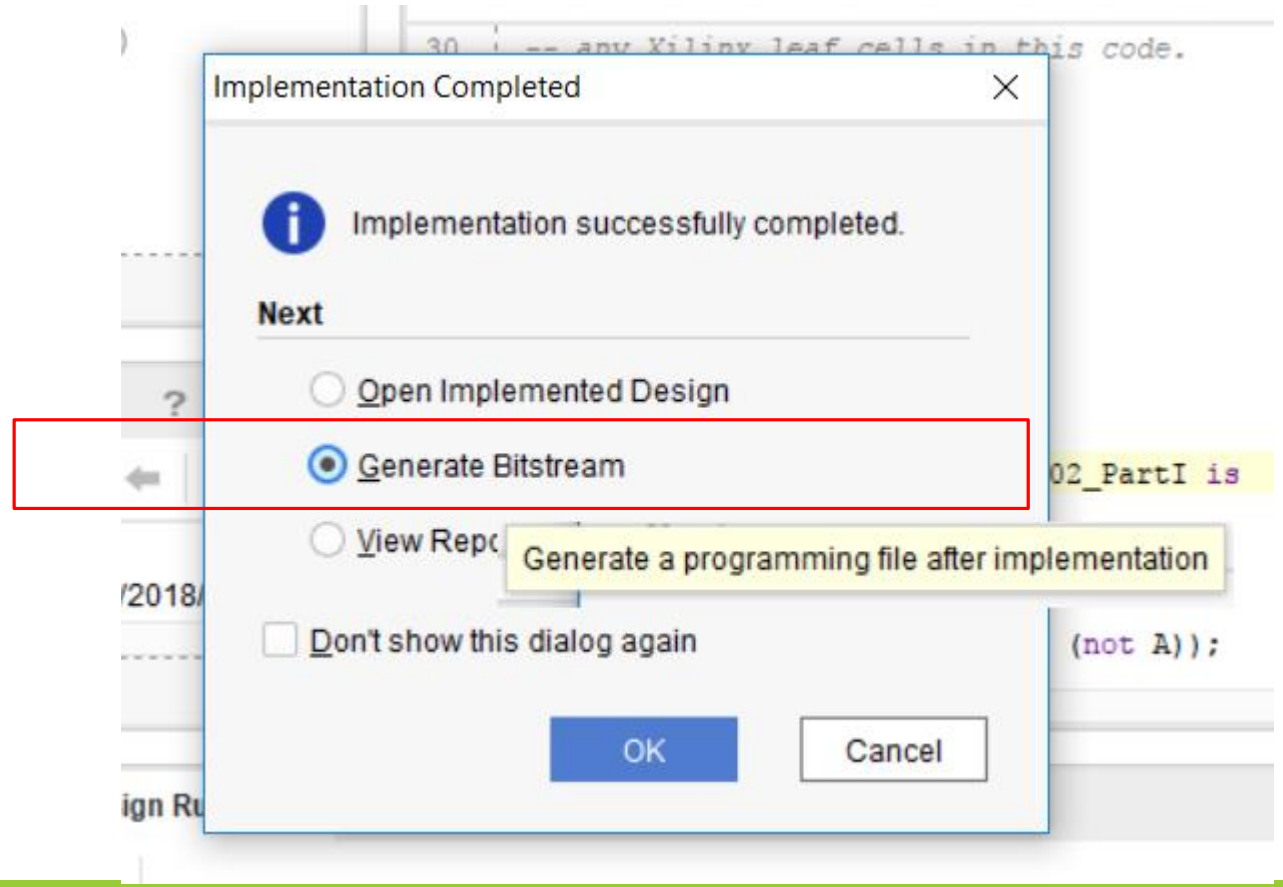
- Click on Run Synthesis



Lab 02-Part I

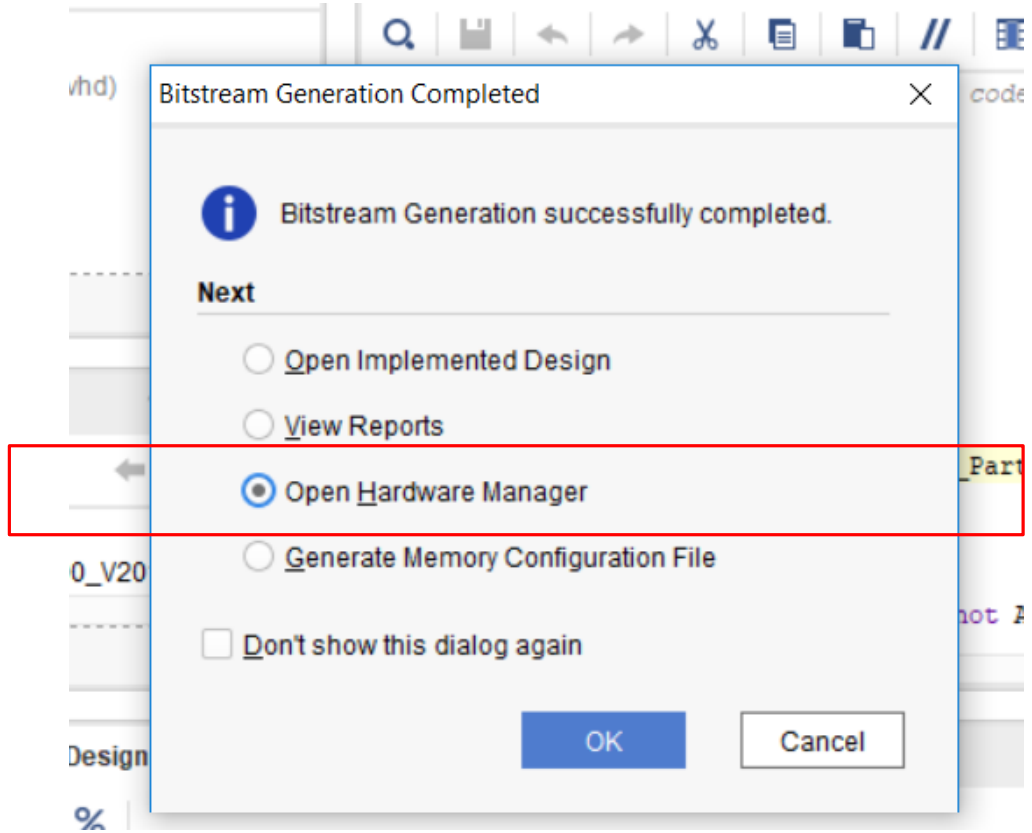

Synthesis Completed
Synthesis successfully completed.
Next
Run Implementation
Open Synthe
View Reports
Implement the active synthesized netlist
Don't show this dialog again
OK
Cancel
Design Runs

Lab 02-Part I


Implementation Completed
Implementation successfully completed.
Next
Open Implemented Design
Generate Bitstream
View Repo
Generate a programming file after implementation
Don't show this dialog again
OK
Cancel
02_PartI is
(not A));

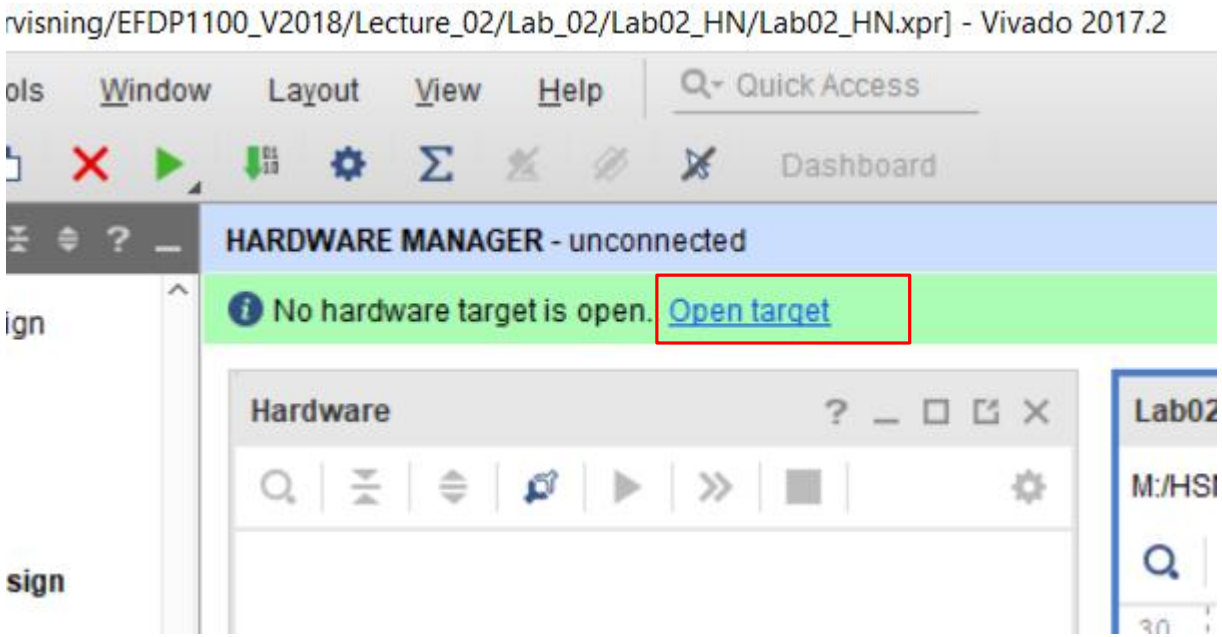
Lab 02-Part I

- Connect BASYS-3 to your computer using USB port and choose Open Hardware Manager



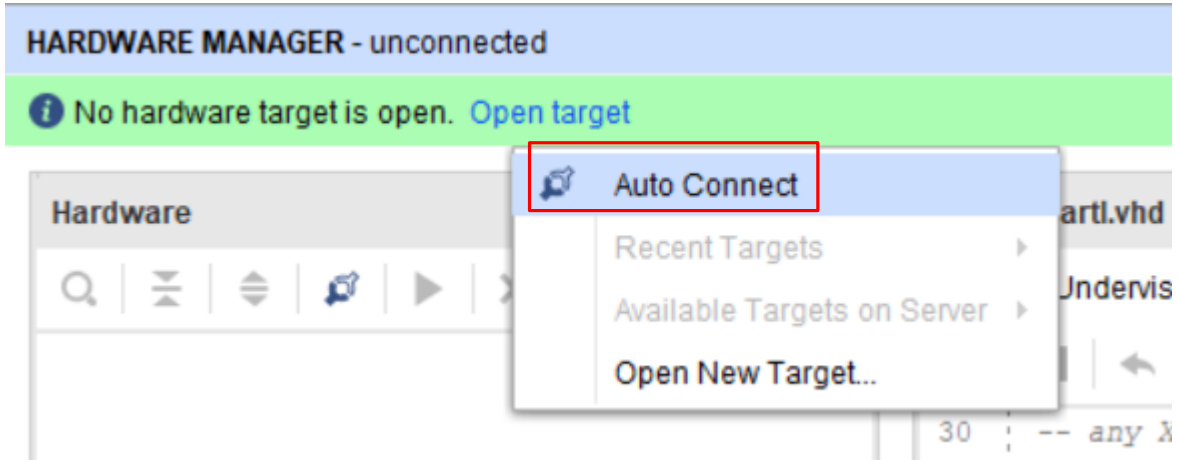
Lab 02-Part I

- Click on Open target



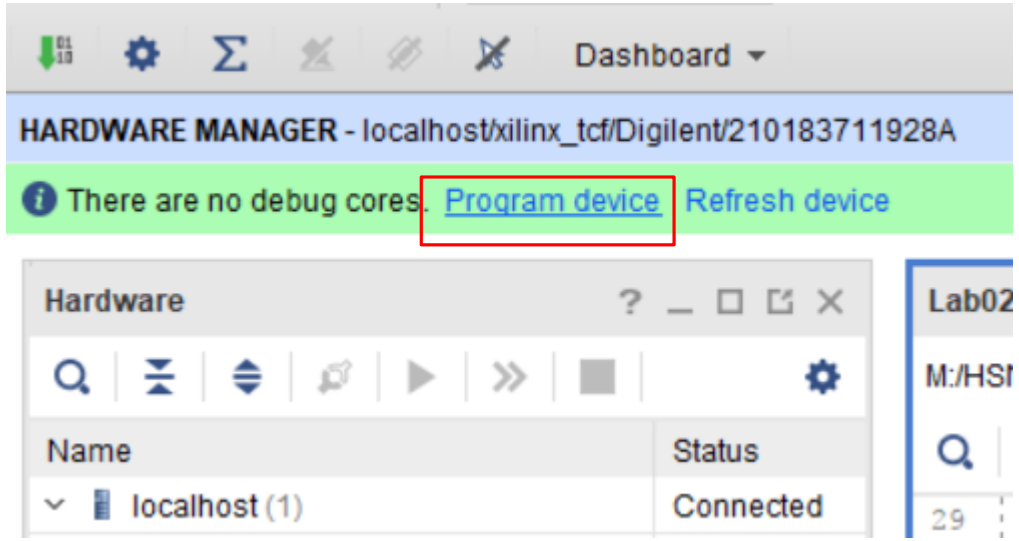
Lab 02-Part I

Choose Auto Connect



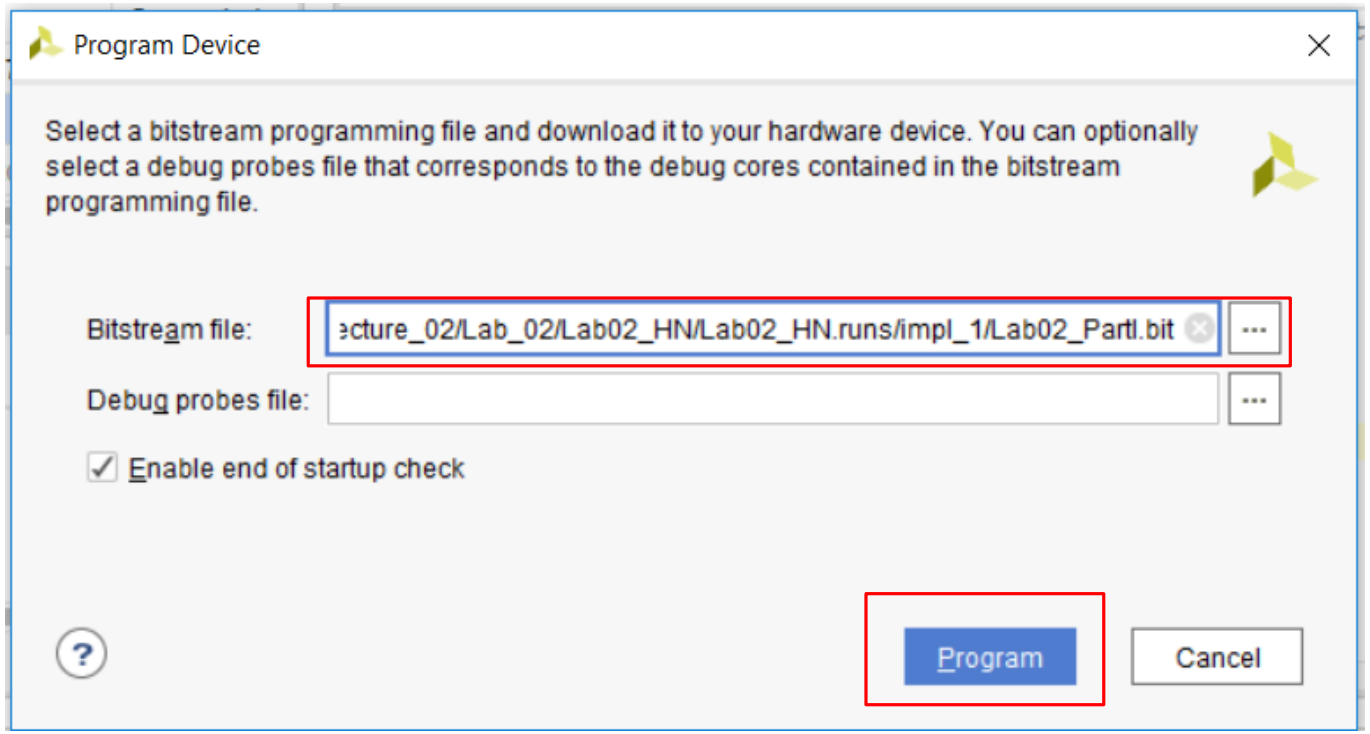
Lab 02-Part I

Click on Program device



Lab 02-Part I

Check if the bit-file with name of your project is in the Bitstream-file box. Then click Program



Lab 02-Part I

- Change the state of two switches Sw0 and Switch 1 and Observe the Led0

Switch 0 (A)	Swith 1(B)	Led0 (Z)
OFF	OFF	
OFF	ON	
ON	OFF	
ON	ON	

Send the table above and vhdl for your design, testbench and ucf as the report of lab 02 part I

Lab 02- Part II

- In this part, you will design one-bit full adder (See your previous home work). Student should report your testing result including
  - VHDL code for one-bit full adder
  - VHDL test bench for such one-bit full adder
  - Simulation waveform for behavior of one bit adder
  - Follow the procedure to generate *.bit file and download your bit-file to your BASYS-3 and test. Following is suggestion about pin-mapping for input and output signals

Signal	Pin
A	SW0
B	SW1
Cin	SW2
Sum	LED0
Cout	LED1

Send your vhdl for design, testbench and ucf as a report for Lab02-partII