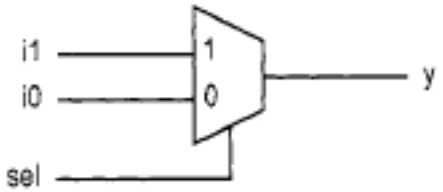
Lab 03

Part I: In this part, students require to experiment the 2-to-1 multiplexer circuit



sel	y
0 (false)	i0
1 (true)	i1

(a) Diagram of a 2-to-1 multiplexer

1. Create a folder to store your design files in this lab
2. Create a project in Vivado design suite (See Lab 01 and Lab 02 in case you need it)
3. Create a new VHDL design file
4. Write concurrent statement for the truth table above either using when-else statement or with-select statement
5. Create a template for test bench and add in your own test vectors
6. Simulate the behavior of the circuit
7. Capture the simulation waveform for lab report
8. Assign input signals to switch pins and the output is a led on BASYS-3 board
9. Generate bit file and download to your BASYS-3 board.
10. Send zip-file as report.

Part II: In this part, students require to experiment priority encoder

1. Create VHDL design for this priority encoder (see lecture note). Use when-else statement to implement this circuit.
2. Write VHDL test bench to verify your design
3. Using switches for input signals and leds for the output signals to experiment the circuit on BASYS-3 board
4. Send zip-file as report.

Part III: In this part of the lab, students should experiment the 2-to-4 decoder circuit

1. Create VHDL design for this encoder (see lecture note). Use with-select statement to implement this circuit
2. Write VHDL test bench to verify that your design
3. Using switches for input signals and leds for the output signals to experiment the circuit on BASYS-3 board
4. Send zip-file as report.