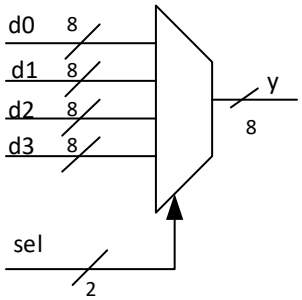
VHDL Programmering
Oppgave 04
Foreleser: Hieu Nguyen
Kontakt: hieu.nguyen@usn.no
Innleveringsfristen: Ingen

Ex 01: Given a combination circuit with truth table as

X (2 downto 0)	Y(1 downto 0)
000	01
001	01
010	11
011	11
100	00
101	00
110	11
111	10

a. Write VHDL code for such combinational circuit using if—else routing statement
b. Write VHDL code for such combinational circuit using case routing statement
c. Write VHDL test bench to simulate your designs and compare the result

Ex 02: A 4-to-1 multiplexer is shown in the figure below



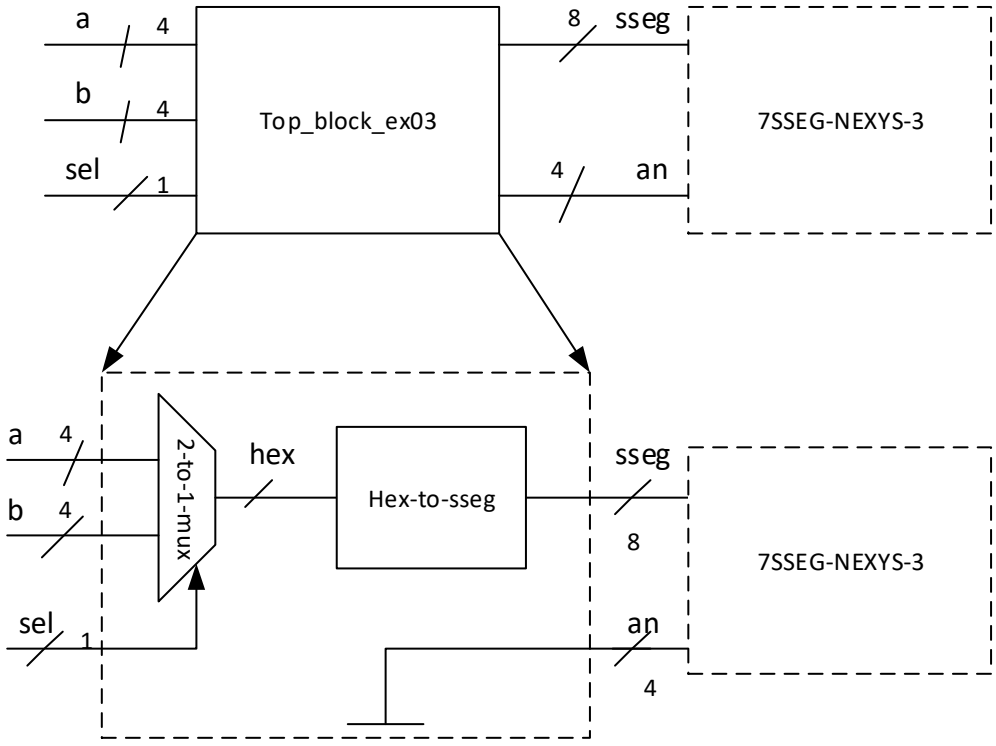
The truth table is given

Sel	Y
00	d0
01	d1
10	d2
11	d3

a. Write VHDL code for such circuit using if-else routing statement

b. Write VHDL code for such circuit using case routing statement
c. Write VHDL test bench to verify the behaviour of the circuit

Ex-03: In this exercise, students use the structural design method to implement the circuit shown in the figure below



a. Develop VHDL-codes 2-to-1-multiplexer and the test bench to test this sub-block.
b. Develop VHDL-codes for hex-to-sseg and the test bench for this sub-block.
c. Create the top_block_ex03 to integrate the two sub-blocks as shown in the above figure.
d. Create the XDC-file where switches 0 to 3 are used for signal a, switches 4 to 7 are used for signal b, center push button is used for sel signal and the sseg and an are connected to sseg and an of the 7-led-segments
e. Synthesize and implement the top-block-ex03 and download the bit-file to BASYS-3 for testing