

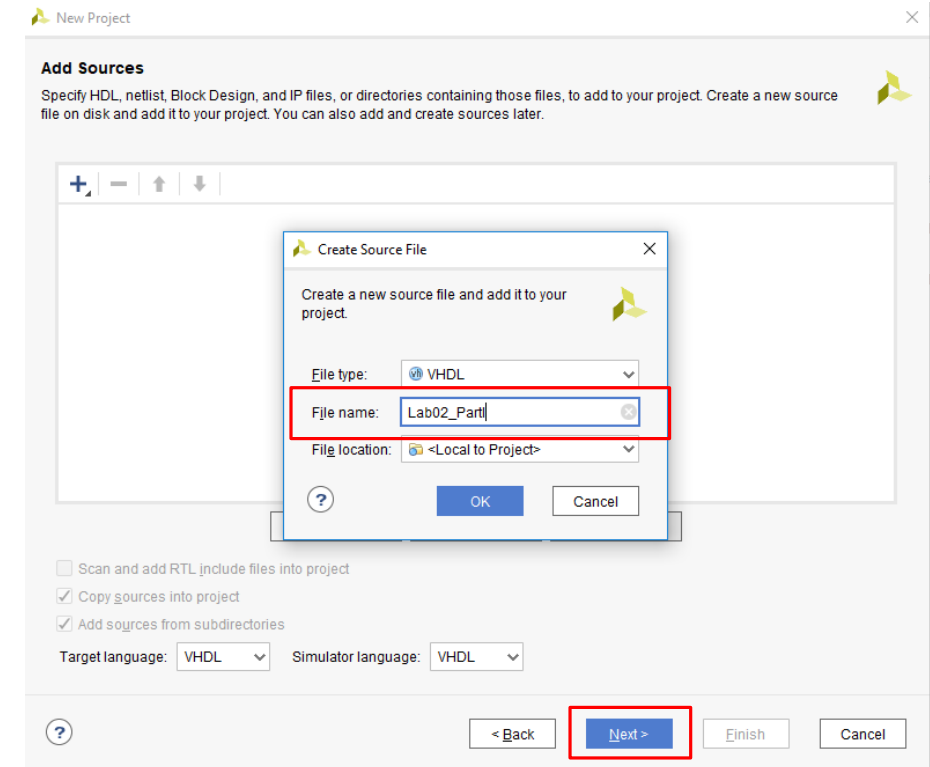
Lab 02

HIEU NGUYEN



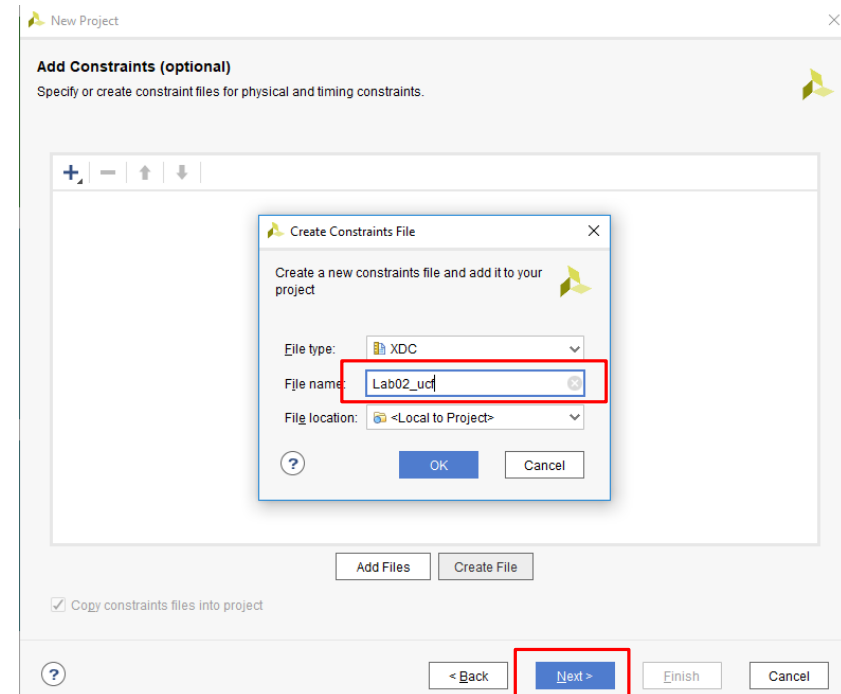
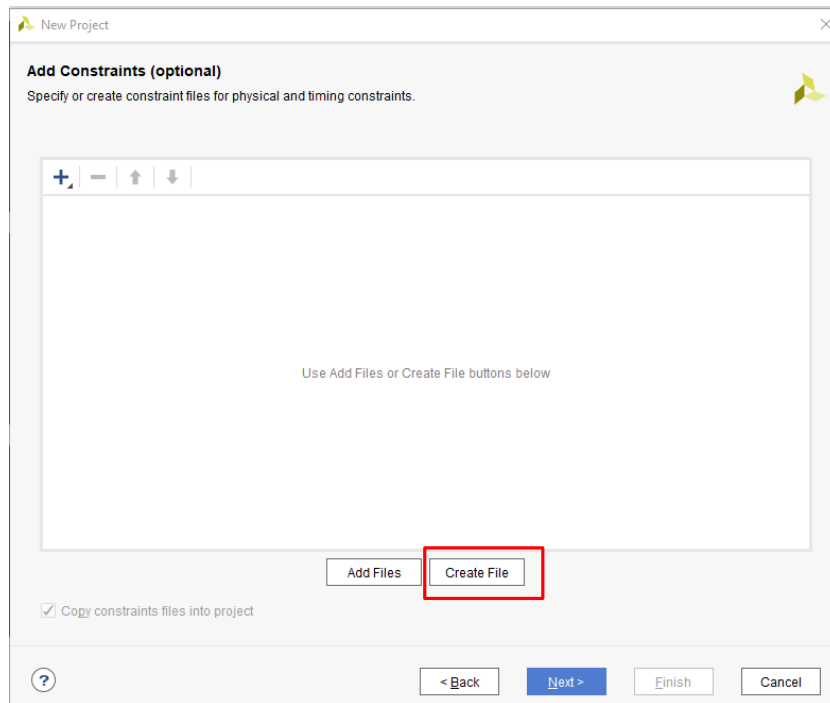
Lab 02-Part I

- Create a folder for your lab 02 (See Lab01 for more detail)
- Launch Vivado 2017.x (See Lab01 for more detail)
- Create a new project with name: Lab02_YourName
- Create a new VHDL-design file with the name: Lab02_partI



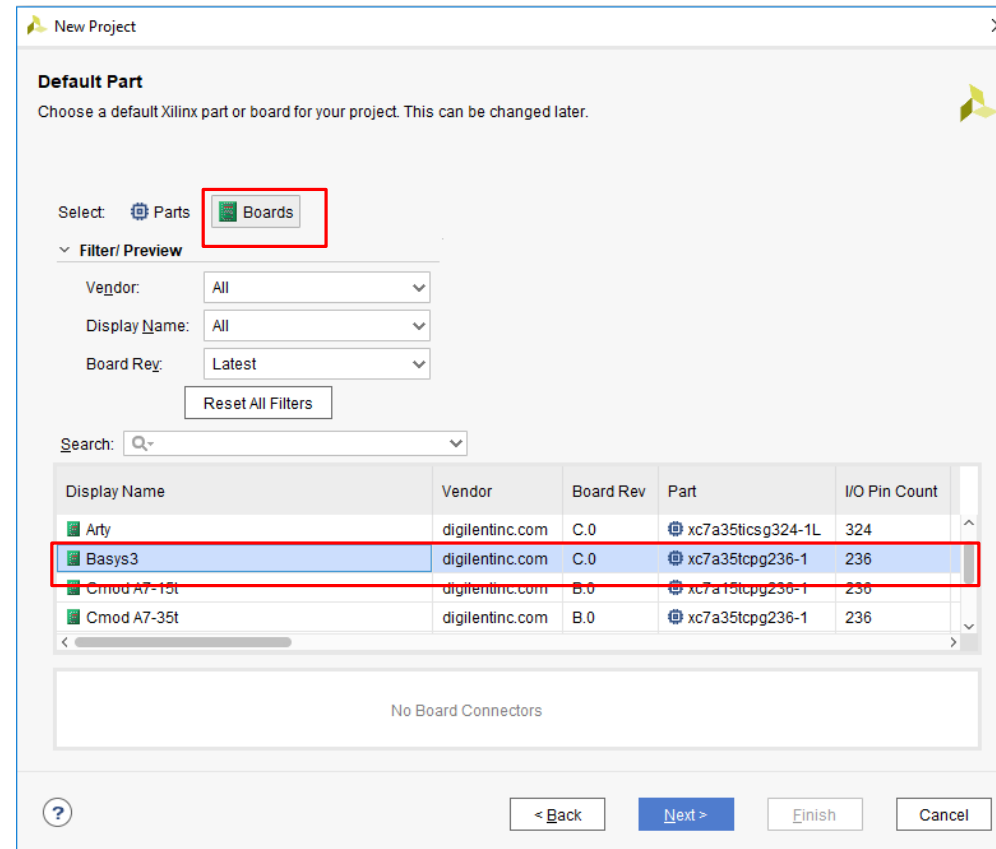
Lab 02-Part I

- Click on «Create File» to create constraint file with name: Lab02_ucf. Then click OK and then NEXT



Lab 02-Part I

- Choose the board (Basys-3) as bellow



New Project

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Select: ☐ Parts ☒ Boards

Filter/ Preview

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

Search:

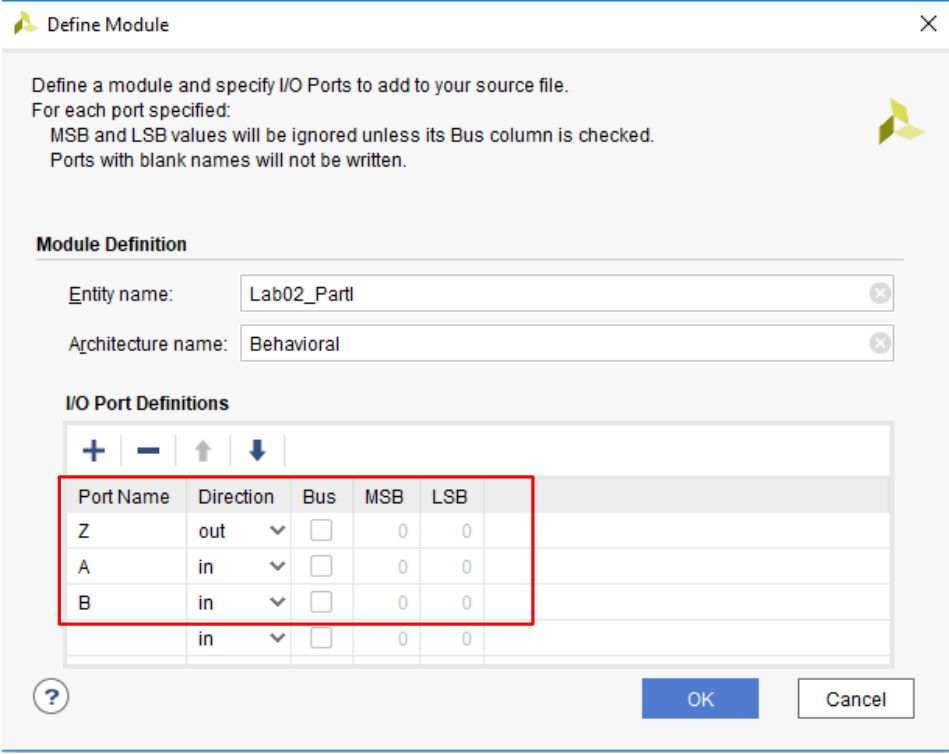
Display Name	Vendor	Board Rev	Part	I/O Pin Count
Arty	digilentinc.com	C.0	xc7a35ticsg324-1L	324
Basys3	digilentinc.com	C.0	xc7a35tcpg236-1	236
Cmod A7-15t	digilentinc.com	B.0	xc7a15tcpg236-1	236
Cmod A7-35t	digilentinc.com	B.0	xc7a35tcpg236-1	236

No Board Connectors

< Back Next > Finish Cancel

Lab 02-Part I

- Define input and output ports as below. Then click OK



Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Entity name:

Architecture name:

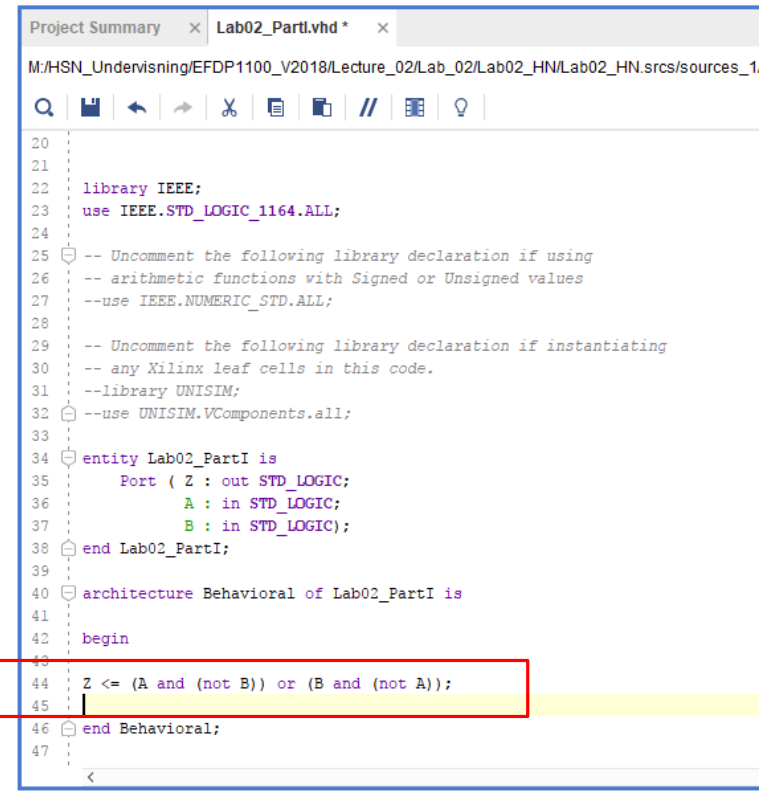
I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
Z	out	<input type="checkbox"/>	0	0
A	in	<input type="checkbox"/>	0	0
B	in	<input type="checkbox"/>	0	0
	in	<input type="checkbox"/>	0	0

Buttons: ? OK Cancel

Lab 02-Part I

- Edit Lab02_PartI by adding the following statement



```
Project Summary x Lab02_PartI.vhd * x
M:/HSN_Undervisning/EFDP1100_V2018/Lecture_02/Lab_02/Lab02_HN/Lab02_HN.srscs/sources_1

20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity Lab02_PartI is
35     Port ( Z : out STD_LOGIC;
36           A : in STD_LOGIC;
37           B : in STD_LOGIC);
38 end Lab02_PartI;
39
40 architecture Behavioral of Lab02_PartI is
41
42 begin
43
44 Z <= (A and (not B)) or (B and (not A));
45
46 end Behavioral;
47
```

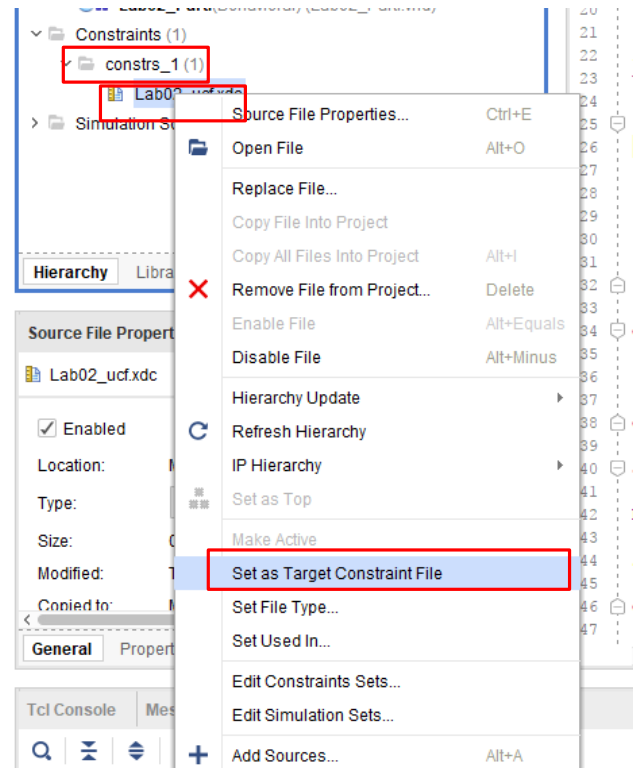
Lab 02-Part I

- Create the test bench with the name: Lab02_PartI_tb and generate the test vectors for this design (See Lab01 for more detail)

-

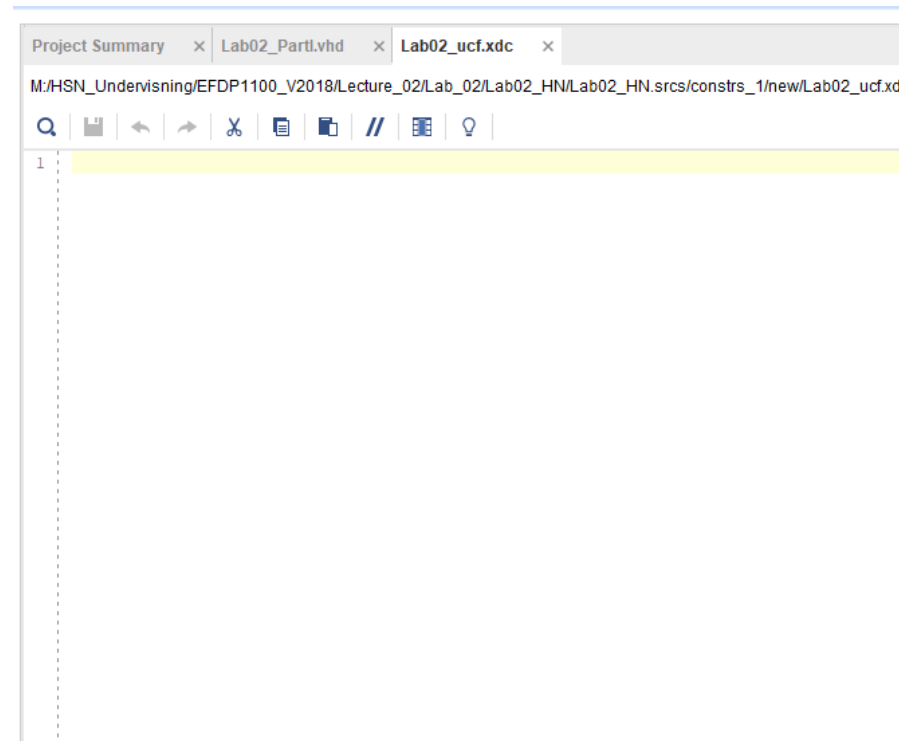
Lab 02-Part I

- Click on constrs_1 and then right click on Lab02_ucf and choose «Set target constraint file»



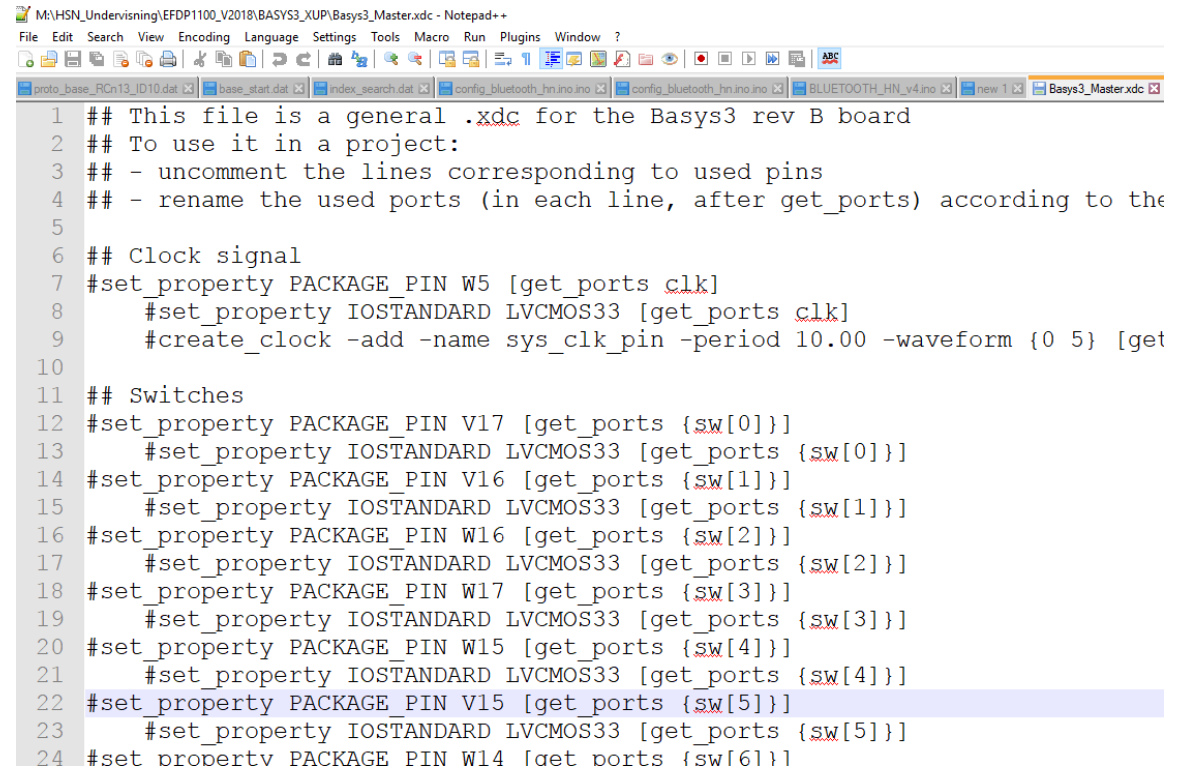
Lab 02-Part I

- Click on Lab02_ucf to edit the this file. Now the ucf-file is empty.



Lab 02-Part I

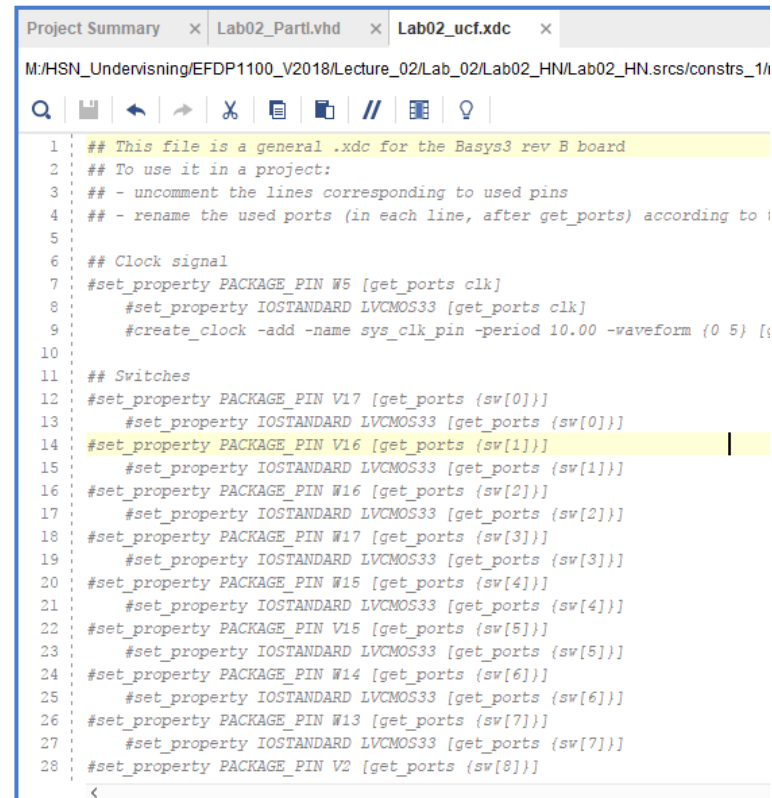
- Open xdc file from Digilent with notepad



```
M:\HSN_Undervising\EFDP1100_V2018\BASYS3_XUP\Basys3_Master.xdc - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
proto_base_RCh13_ID10.dat base_start.dat index_search.dat config_bluetooth_hn.ino config_bluetooth_hn.ino BLUETOOTH_HN_v4.ino new 1 Basys3_Master.xdc
1 ## This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used ports (in each line, after get_ports) according to the
5
6 ## Clock signal
7 #set_property PACKAGE_PIN W5 [get_ports clk]
8     #set_property IOSTANDARD LVCMOS33 [get_ports clk]
9     #create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get
10
11 ## Switches
12 #set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
13     #set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
14 #set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
15     #set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
16 #set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
17     #set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
18 #set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
19     #set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
20 #set_property PACKAGE_PIN W15 [get_ports {sw[4]}]
21     #set_property IOSTANDARD LVCMOS33 [get_ports {sw[4]}]
22 #set_property PACKAGE_PIN V15 [get_ports {sw[5]}]
23     #set_property IOSTANDARD LVCMOS33 [get_ports {sw[5]}]
24 #set_property PACKAGE_PIN W14 [get_ports {sw[6]}]
```

Lab 02-Part I

- Copy all the content of xdc file from Digilent and paste in Lab02_ucf.dxc



```
1  ## This file is a general .xdc for the Basys3 rev B board
2  ## To use it in a project:
3  ## - uncomment the lines corresponding to used pins
4  ## - rename the used ports (in each line, after get_ports) according to
5
6  ## Clock signal
7  #set_property PACKAGE_PIN W5 [get_ports clk]
8      #set_property IOSTANDARD LVCMOS33 [get_ports clk]
9      #create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [
10
11  ## Switches
12  #set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
13      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
14  #set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
15      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
16  #set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
17      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
18  #set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
19      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
20  #set_property PACKAGE_PIN W15 [get_ports {sw[4]}]
21      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[4]}]
22  #set_property PACKAGE_PIN V15 [get_ports {sw[5]}]
23      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[5]}]
24  #set_property PACKAGE_PIN W14 [get_ports {sw[6]}]
25      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[6]}]
26  #set_property PACKAGE_PIN W13 [get_ports {sw[7]}]
27      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[7]}]
28  #set_property PACKAGE_PIN V2 [get_ports {sw[8]}]
```

Lab 02-Part I

- Enable line 12 and line 13 to use Switch 0 for input signal A
- Enable line 14 and line 15 to use Switch 1 for input signal B

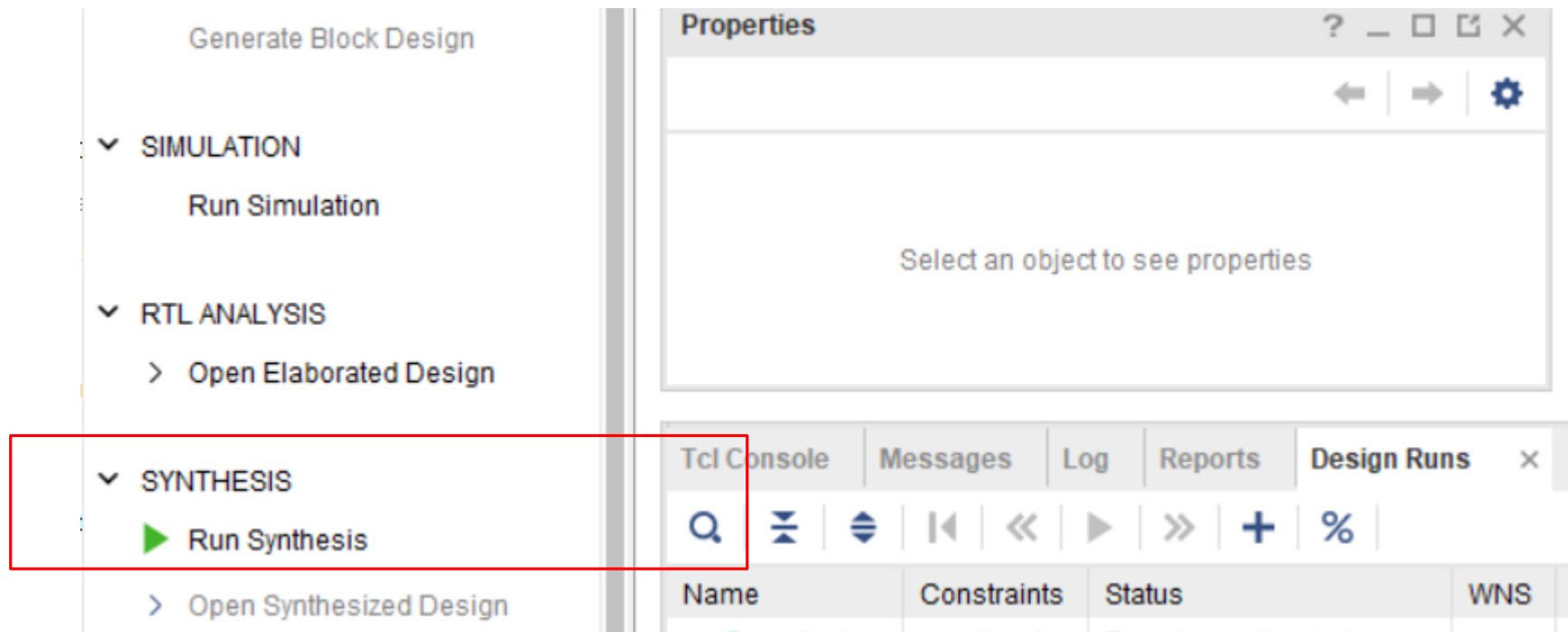
```
11  ## Switches
12  set_property PACKAGE_PIN V17 [get_ports {A}]
13      set_property IOSTANDARD LVCMOS33 [get_ports {A}]
14  set_property PACKAGE_PIN V16 [get_ports {B}]
15      set_property IOSTANDARD LVCMOS33 [get_ports {B}]
16  #set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
17      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
18  #set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
19      #set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
20  #set_property PACKAGE_PIN W15 [get_ports {sw[4]}]
```

- Enable line 47 and line 48 to use Led0 for output signal Z

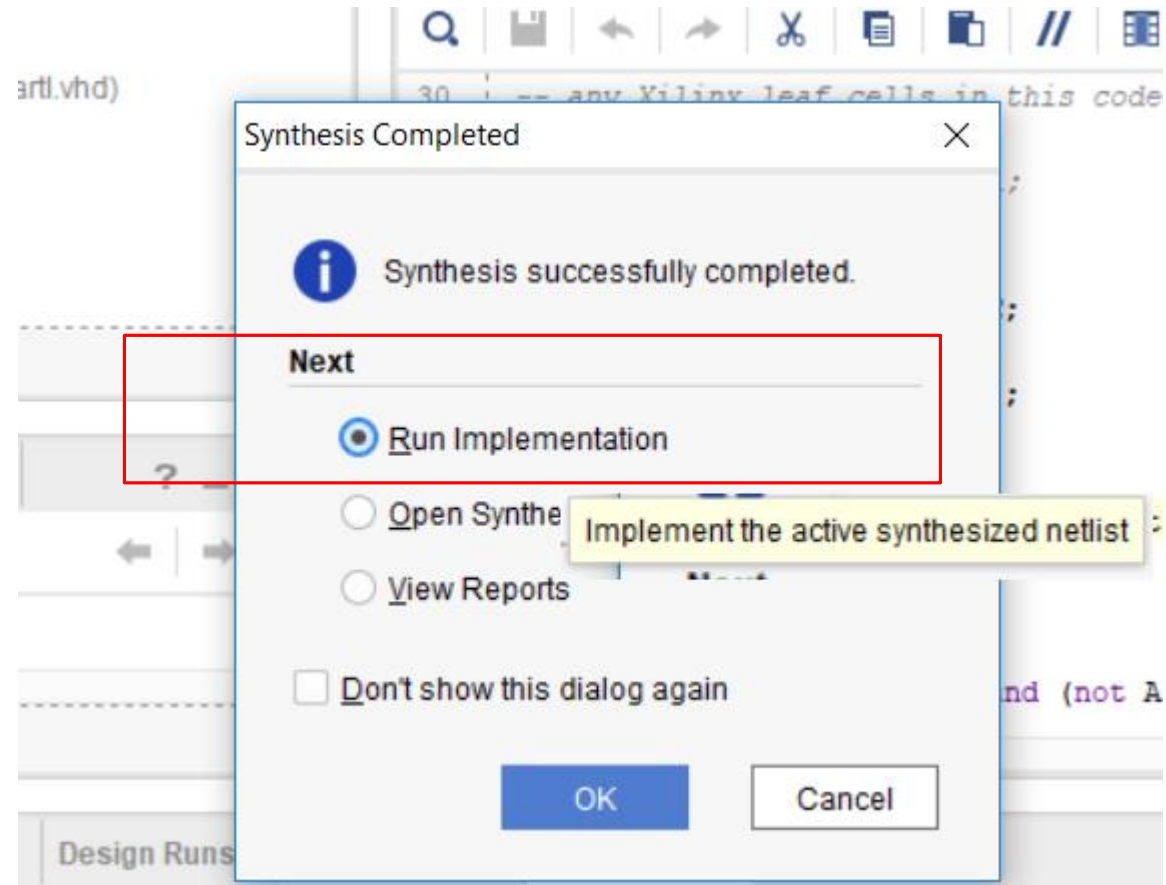
```
45
46  ## LEDs
47  set_property PACKAGE_PIN U16 [get_ports {Z}]
48      set_property IOSTANDARD LVCMOS33 [get_ports {Z}]
49  #set_property PACKAGE_PIN E19 [get_ports {led[1]}]
50      #set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]
51  #set_property PACKAGE_PIN U19 [get_ports {led[2]}]
52      #set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]
53  #set_property PACKAGE_PIN V19 [get_ports {led[3]}]
54      #set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]
```

Lab 02-Part I

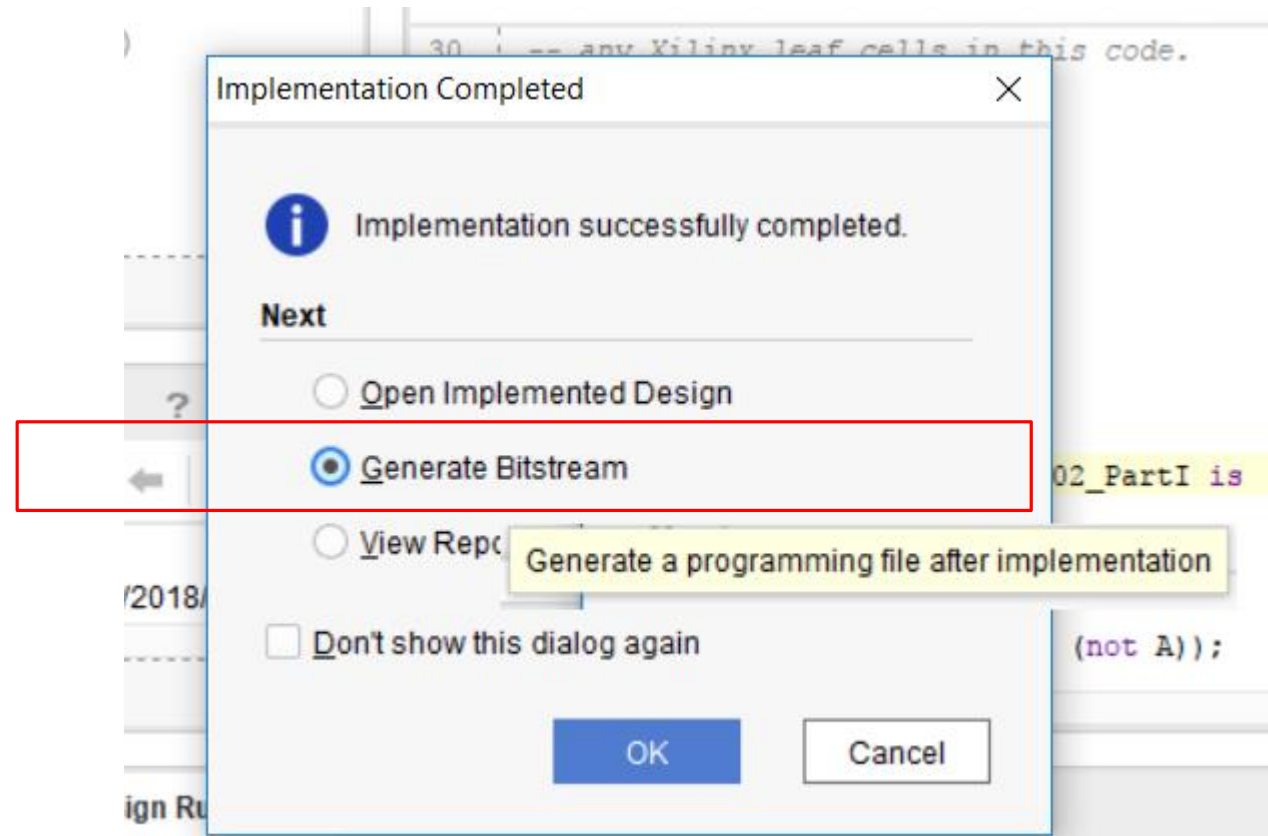
- Click on Run Synthesis



Lab 02-Part I

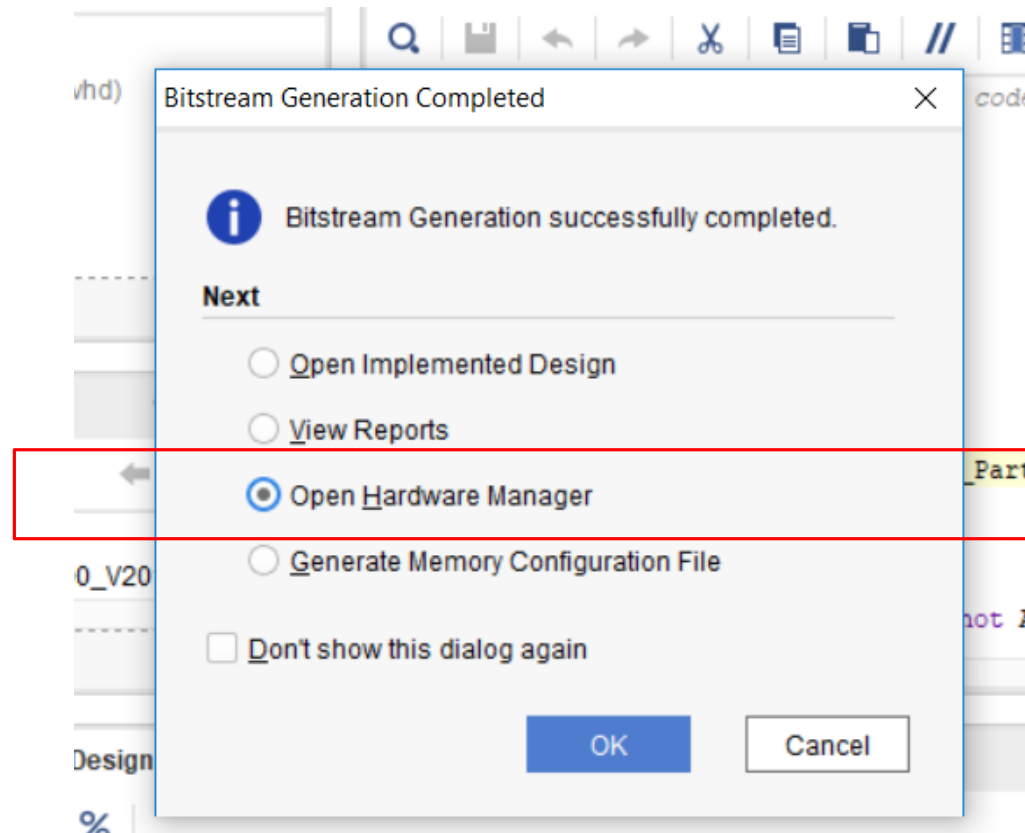


Lab 02-Part I



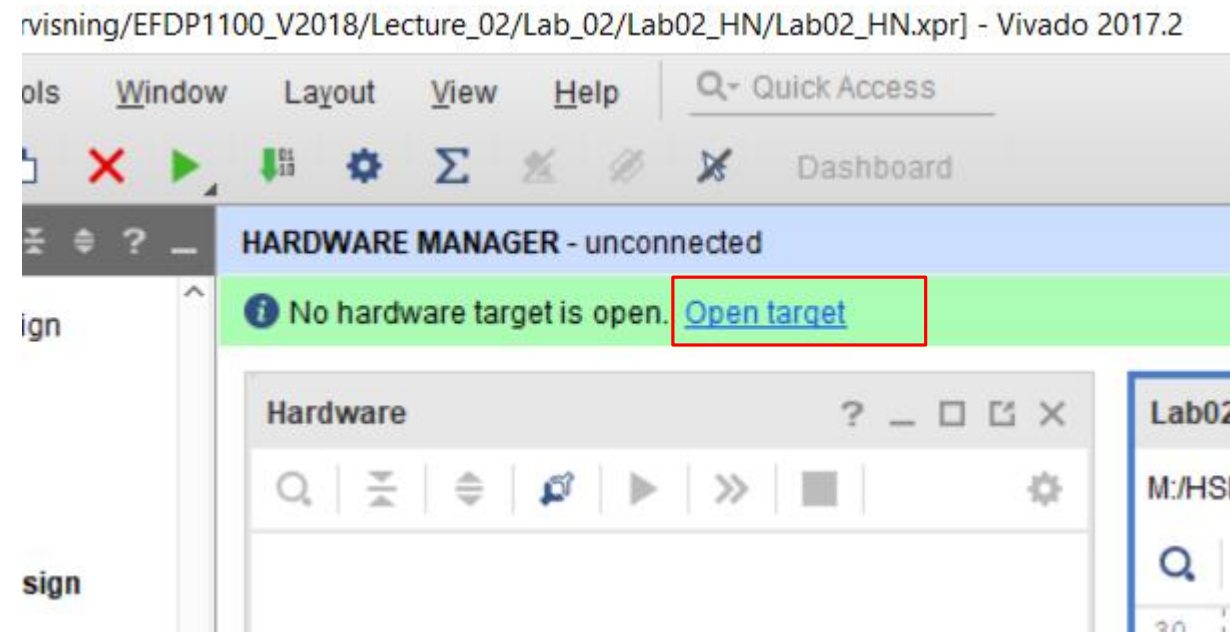
Lab 02-Part I

- Connect BASYS-3 to your computer using USB port and choose Open Hardware Manager



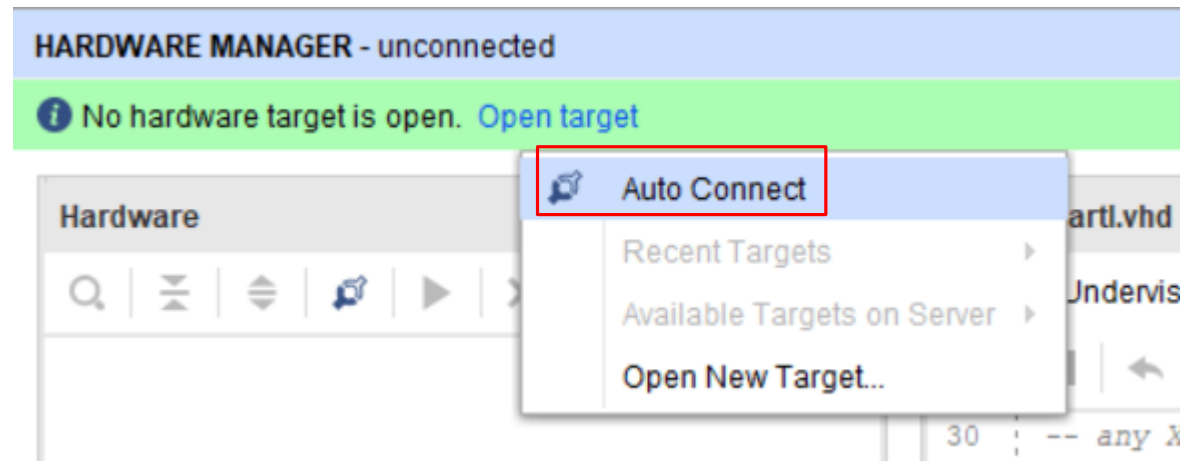
Lab 02-Part I

- Click on Open target



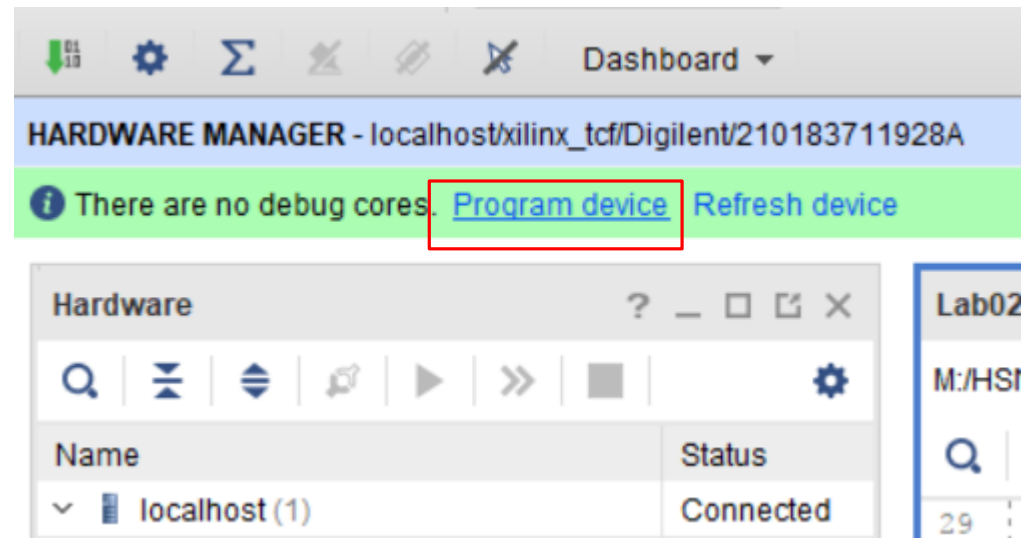
Lab 02-Part I

Choose Auto Connect



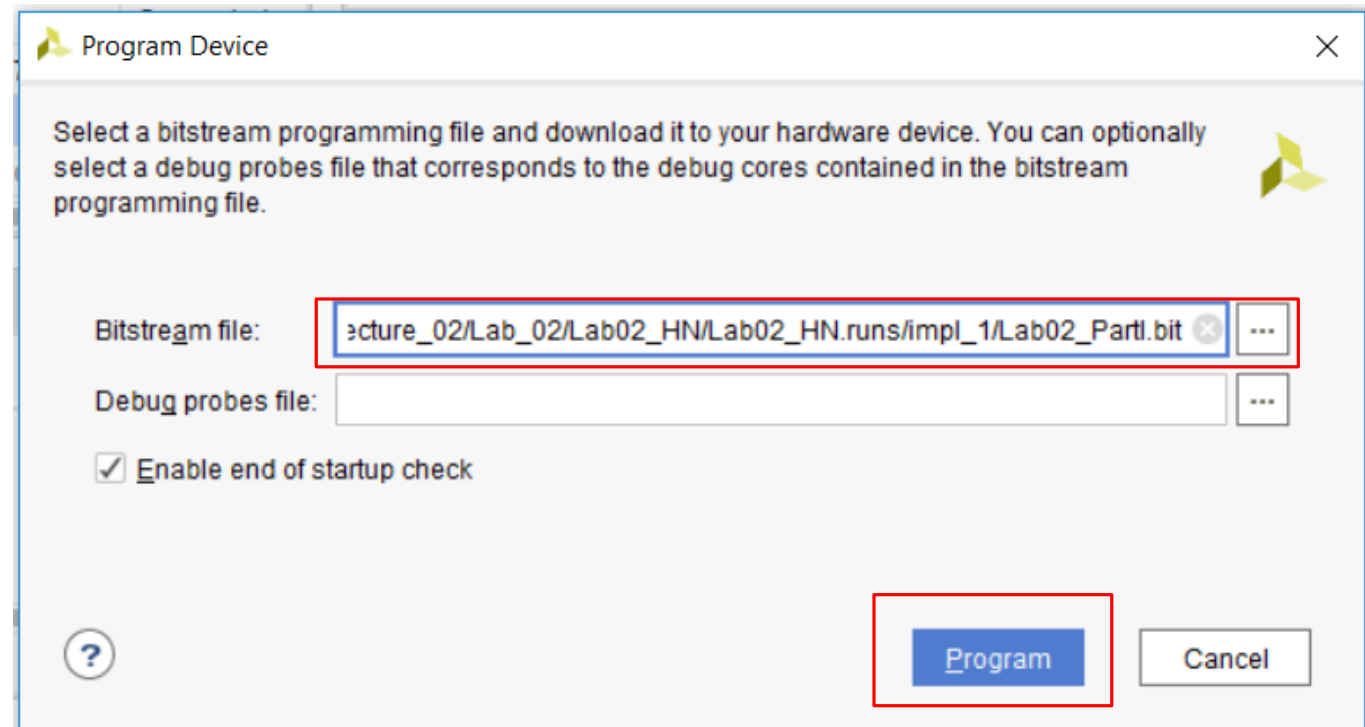
Lab 02-Part I

Click on Program device



Lab 02-Part I

Check if the bit-file with name of your project is in the Bitstream-file box. Then click Program



Lab 02-Part I

- Change the state of two switches Sw0 and Switch 1 and Observe the Led0

Switch 0 (A)	Swith 1(B)	Led0 (Z)
OFF	OFF	
OFF	ON	
ON	OFF	
ON	ON	

Send the table above and vhdl for your design, testbench and ucf as the report of lab 02 part I

Lab 02- Part II

- In this part, you will design one-bit full adder (See your previous home work). Student should report your testing result including
 - VHDL code for one-bit full adder
 - VHDL test bench for such one-bit full adder
 - Simulation waveform for behavior of one bit adder
 - Follow the procedure to generate *.bit file and download your bit-file to your BASYS-3 and test. Following is suggestion about pin-mapping for input and output signals

Signal	Pin
A	SW0
B	SW1
Cin	SW2
Sum	LED0
Cout	LED1

Send your vhdl for design, testbench and ucf as a report for Lab02-partII