ELEC 451 Lab Report 2

Dynamic NAND Gate

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In-Lab Results

The following tables summarize the data collected during the lab session. Some configurations were not measured on the dynamic NOR gate due to time restrictions.

Static NAND (1 Chip)

A (pin6)	B (pin 10)	T_f (fall time)	T_r (rise time)
1	clk	100 ns	72 ns
clk	1	106 ns	72 ns
clk	clk	106 ns	38 ns

Table 1: Static NAND delay times using one CD4007UBE chip.

Static NAND (2 Chips)

A	B	T_f	T_r
clk	1	58 ns	84 ns
1	clk	70 ns	80 ns
clk	clk	70 ns	45 ns

Table 2: Static NAND delay times using two CD4007UBE chips.

Dynamic NAND (1 Chip)

A	B	T_f	T_r
clk	1	98 ns	76 ns
clk	clk	108 ns	72 ns
1	clk	96 ns	74 ns

Table 3: Dynamic NAND delay times using one CD4007UBE chip.

Dynamic NOR (1 Chip)

A	B	T_f	T_r
clk	1	64 ns	76 ns

Table 4: Dynamic NOR delay times using one CD4007UBE chip.

Post-Lab Results

The two-input static and dynamic NAND gate layouts shown in Figure 1 were generated using the Electric software. An effort was made during the design of these layouts to make them as clear and readable as possible. If minimizing the rising and falling times was a greater concern, reducing the amount of excess metal 1 (in blue), especially near the output, would improve the results. All figures and tables may be shared anonymously.

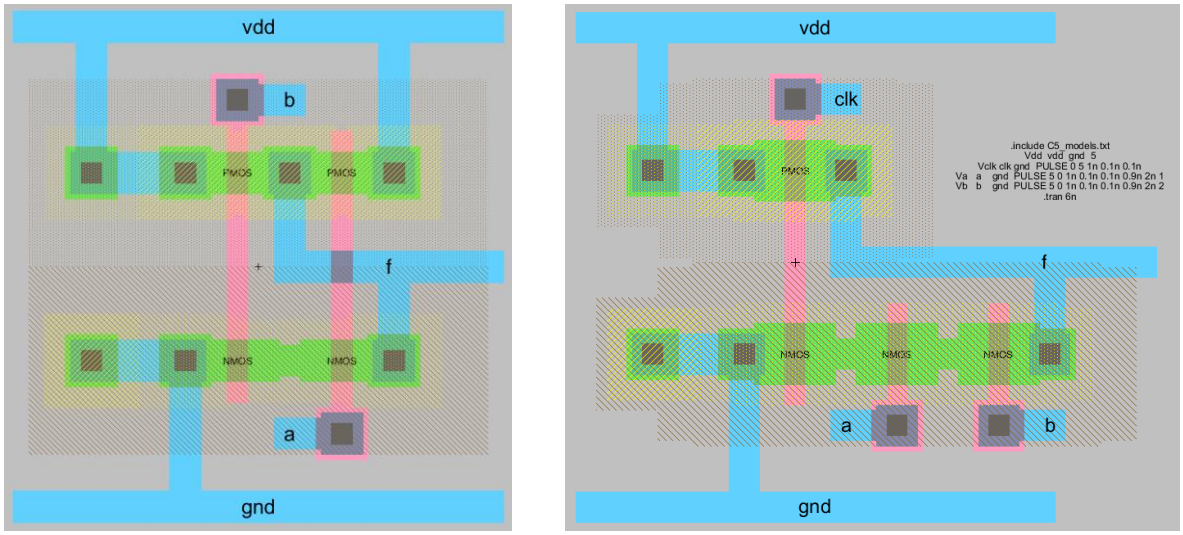

Figure 1: Screenshots of a two-input static (left) and dynamic (right) NAND gate layout in Electric.

The LTSpice code for generating the input voltages is shown in Figure 1. The inputs transition as follows, where the bits are in the order clock, A, B: 111 → 011 → 111 → 001 → 111 → 010 → 111 → 000 → 111. Note that this covers all 8 relevant transitions for a standard two-input dynamic setup. All input traces as well as the output trace are displayed in Figure 2.

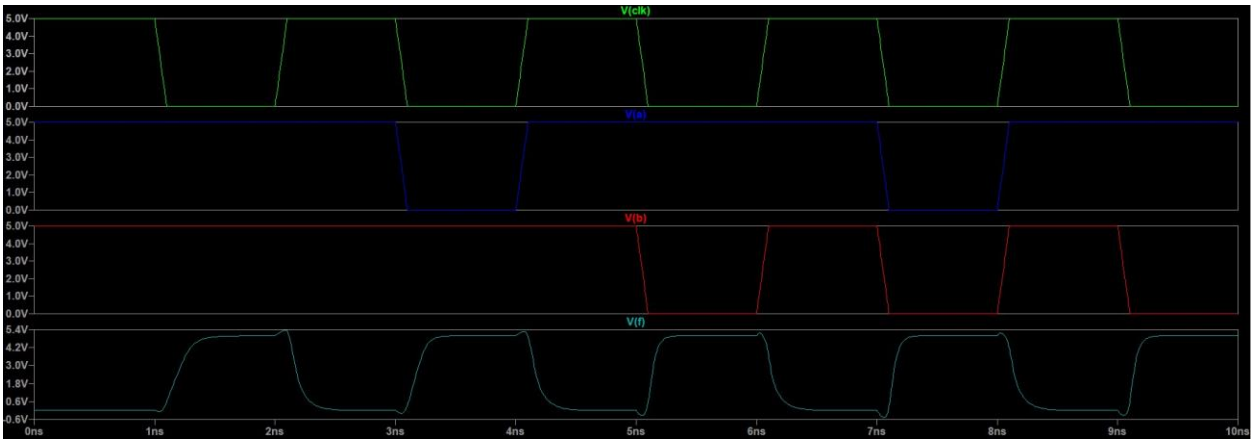

Figure 2: Oscilloscope readings of the simulated dynamic NAND gate's input and output voltage traces.

Table 5 and Table 6 summarize the data collected from the simulated and implemented NAND gates respectively. They aim to compare the advantages and disadvantages of using a static versus a dynamic setup. Note that the additional metrics of maximum and minimum voltages were added to Table 5 to compare the voltage spikes and dips in the output which occur immediately before each transition.

Layouts	Static	Dynamic	% Difference	Winner
Worst T_r	0.154602 ns	0.143886 ns	7.677 %	Dynamic
Best T_r	0.072368 ns	0.048916 ns	47.943 %	Dynamic
Worst T_f	0.142539 ns	0.129628 ns	9.960 %	Dynamic
Best T_f	0.113242 ns	0.072935 ns	55.264%	Dynamic
Worst Delay	0.154602 ns	0.143886 ns	7.677%	Dynamic
Layout Area	1584 λ^2	1696 λ^2	7.071%	Static
Max Output	5.2 V	5.37 V	3.270%	Static
Min Output	-0.313 V	-0.465 V	48.562%	Static

Table 5: Time delay, layout area and Output results from simulated NAND and dynamic NAND gates.

Comparing simulation results seen in Table 5, it is apparent that the dynamic NAND gate achieves more desirable rise and fall times in both the best- and worst-case scenarios. The worst-case rise and fall times are comparable as both gates travel through the same number of transistors. The best-case rise time was significantly better for the dynamic NAND gate which occurred when clk, A and B began high (1) and B switched to low(0), turning the NAND gate on. The reason why this transition yielded strong results was because of B's position with respect to the output. The static NAND gate preformed better when comparing the maximum and minimum voltage outputs as they are generally better in terms of power consumption and complexity.

Physical	Static	Dynamic	2Static	NOR
Worst T_r	72 ns	76 ns	84 ns	76 ns
Best T_r	38 ns	72 ns	45 ns	76 ns
Worst T_f	106 ns	108 ns	70 ns	64 ns
Best T_f	100 ns	96 ns	58 ns	64 ns
Worst Delay	106 ns	108 ns	84 ns	76 ns

Table 6: Time delay results from the physical gates built using the CD700UBE chip(s).

As the results in Table 6 suggest, a dynamic NOR gate will have faster fall times than a dynamic NAND gate built from the same chip. This is because a NOR gate places the NFETs in parallel, compared to the NAND gate's series configuration, which leads to a shorter and less resistive path to ground. The rise times are comparable since both gates use only a single PFET to pull the output voltage to VDD.

ELEC 451 Lab 1 Lab Report

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Due on: Oct 19th, 2023

Nand Gate Layout Using Electric

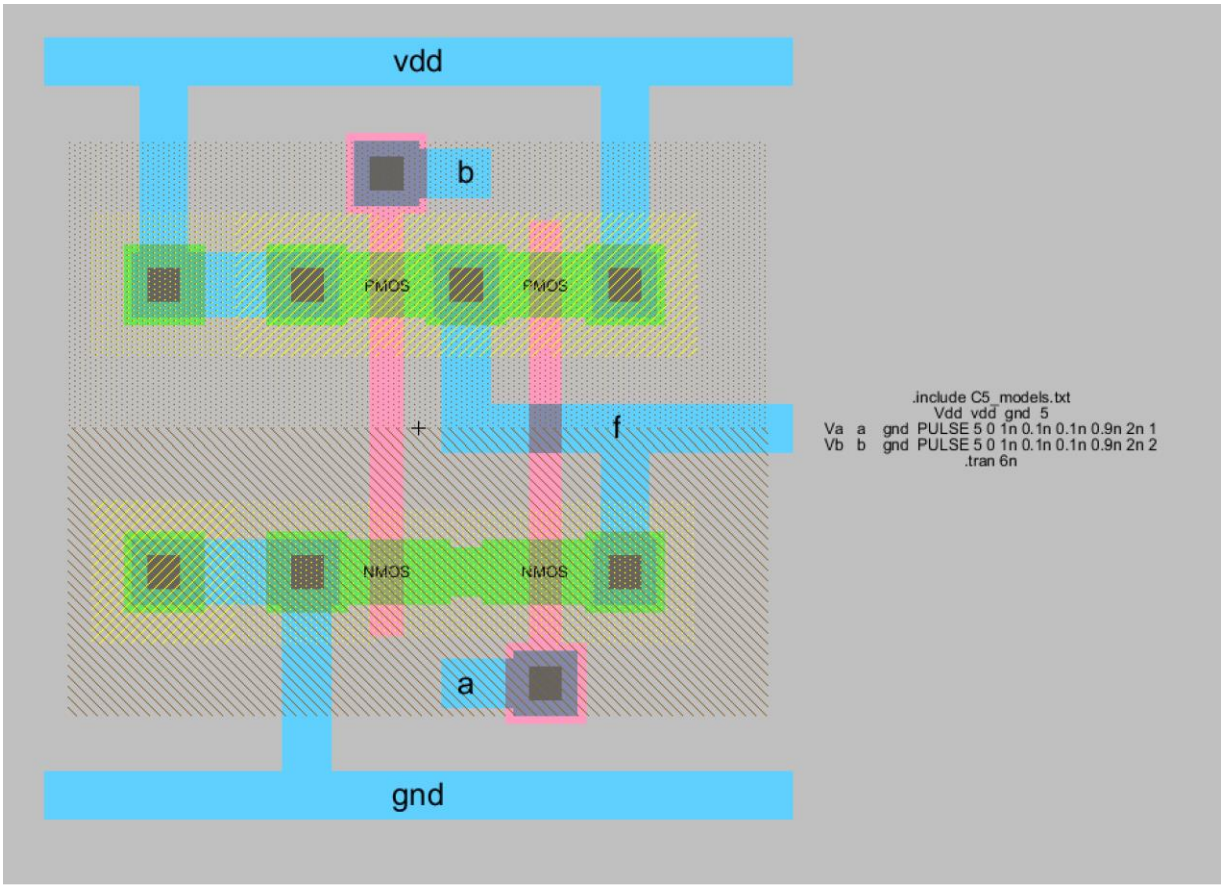

Figure 1: Electric diagram of the NAND gate.

Time Delay Plots for all transitions

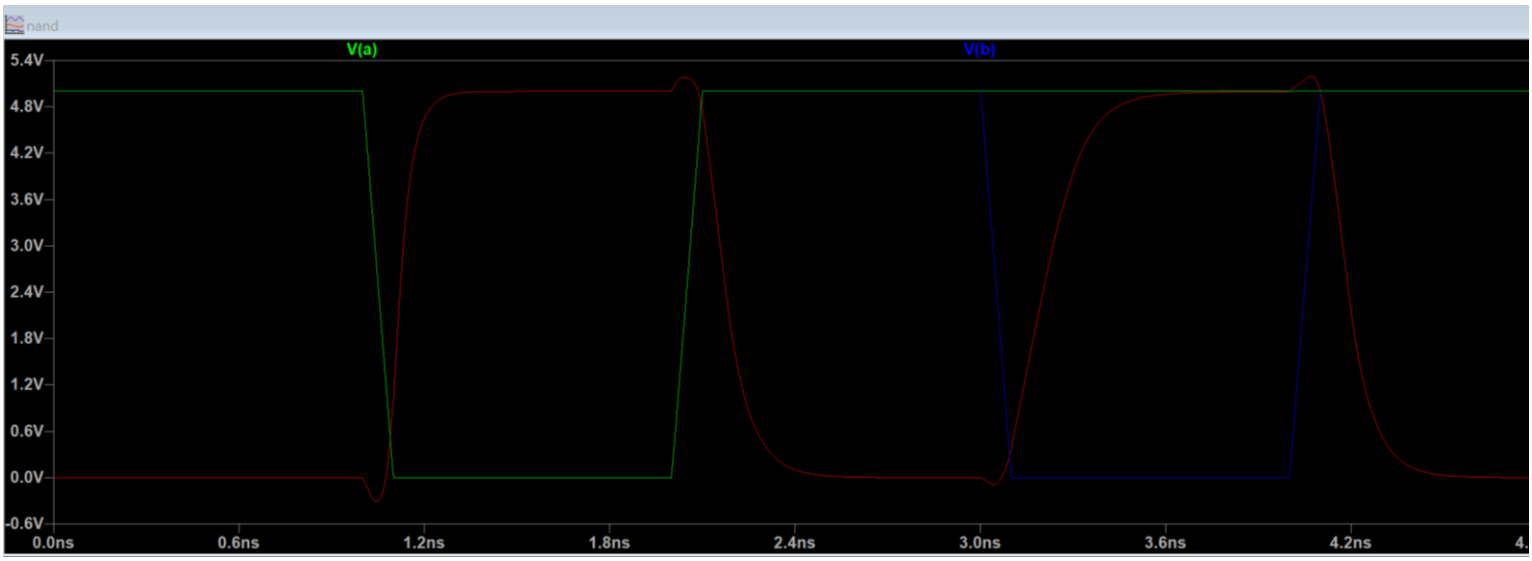

Figure 2: Rise and Fall times from with V(a) in green, V(b) in blue and V(f) in red.

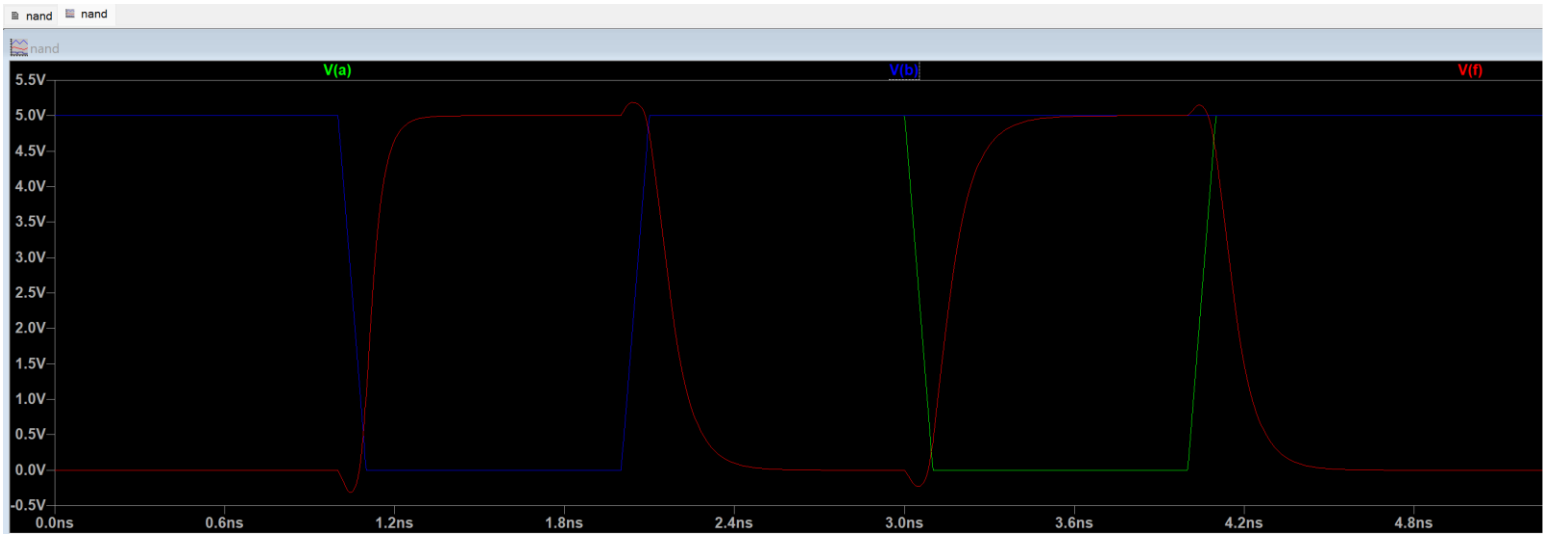

Figure 3: Rise and Fall times from with V(a) in green, V(b) in blue and V(f) in red.

Post Lab Questions

Q) Explain the Reasoning behind your setup choice for worst delay time.

The worst delay times were determined experimentally by testing every state transition. In order to find the slowest fall time, the following three transitions were setup to measure the delay from: 00→11, 01→11, and 10→11. It was found that the worst-case rise time was the 11→10 transition, and the worst-case fall time was the 10→11 transition.

In fact, switching the second bit, "bit B", would result in the slowest delay times by analysis. As shown in Figure 1 above, the N-FET associated with bit B is located furthest from the output. This slight difference explains the slower transitions than those resulting from switching bit A which is significantly closer to the output.

Q) Compare your worst-case delay time(s) to your best-case delay time(s).

The best-case rise times were observed when transitioning from 11 to 00. This can be explained by examining the P-FETs. Because these transistors are in parallel, when they are both active, the total resistance of the path up to V_{DD} is halved. It follows, then, that the rise time should be approximately half of that for a single bit transition. Table 1 confirms that the best-case rise time is 46.8% of the worst-case.

Table 1: Delay times for each two-bit transition.

Transition	Delay Time [ps]	Rise/Fall
11 → 00	72.368421	Rise
11 → 10	154.60526	Rise
11 → 01	111.84211	Rise
00 → 11	123.4375	Fall
10 → 11	142.53906	Fall
01 → 11	113.24219	Fall

The difference in fall times is not as significant since both P-FETs activate for each transition. Table 1 shows that the best-case fall time is only 79.4% of the worst-case.

Q) If you were to make a NOR gate the schematic would be different, but what would you change in the W_n, W_p choices for your design?

NOR gates require that the P-FETs be placed in series and that the N-FETs be placed in parallel. These changes would require that W_p/W_n be equal to 4 increases the size of the gate. In practice, the best solution would be to double W_p and to halve W_n. In the case of this lab, that would mean setting W_p to 8 and W_n to 2.