MCP3201

2.7V 12-Bit A/D Converter with SPI™ Serial Interface

Features

- 12-bit resolution
- ±1 LSB max DNL
- ±1 LSB max INL (MCP3201-B)
- ±2 LSB max INL (MCP3201-C)
- On-chip sample and hold
- SPI™ serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100ksps max. sampling rate at V_{DD} = 5V
- 50ksps max. sampling rate at V_{DD} = 2.7V
- Low power CMOS technology
- 500 nA typical standby current, 2 µA max.
- 400 µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- 8-pin MSOP, PDIP, SOIC and TSSOP packages

Applications

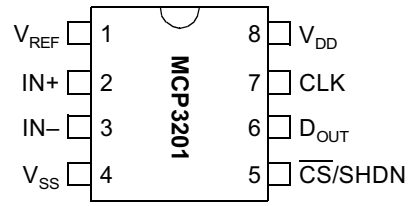
- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

Description

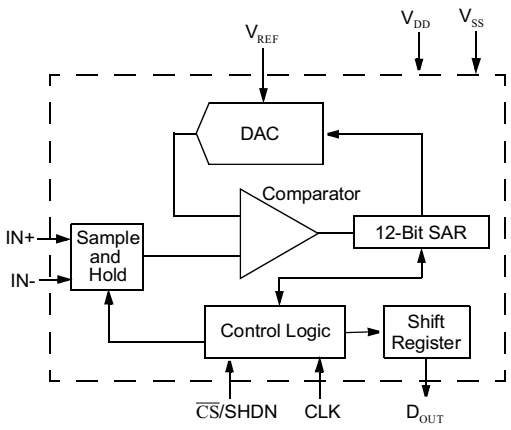
The Microchip Technology Inc. MCP3201 is a successive approximation 12-bit Analog-to-Digital (A/D) Converter with on-board sample and hold circuitry. The device provides a single pseudo-differential input. Differential Nonlinearity (DNL) is specified at ±1 LSB, and Integral Nonlinearity (INL) is offered in ±1 LSB (MCP3201-B) and ±2 LSB (MCP3201-C) versions. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of sample rates of up to 100 ksps at a clock rate of 1.6 MHz. The MCP3201 operates over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500 nA and 300 µA, respectively. The device is offered in 8-pin MSOP, PDIP, TSSOP and 150 mil SOIC packages.

Package Types

MSOP, PDIP, SOIC, TSSOP



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD}.....7.0V

All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{DD} +0.6V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-65°C to +125°C

ESD protection on all pins (HBM).....> 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{DD}	+2.7V to 5.5V Power Supply
V_{SS}	Ground
IN+	Positive Analog Input
IN-	Negative Analog Input
CLK	Serial Clock
D_{OUT}	Serial Data Out
$\overline{CS}$/SHDN	$\overline{Chip\ Select}$/Shutdown Input
V_{REF}	Reference Voltage Input

ELECTRICAL CHARACTERISTICS

All parameters apply at V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 100 ksps, and f_{CLK} = 16*f_{SAMPLE} unless otherwise noted.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Conversion Rate:						
Conversion Time	t_{CONV}	—	—	12	clock cycles	
Analog Input Sample Time	t_{SAMPLE}		1.5		clock cycles	
Throughput Rate	f_{SAMPLE}	—	—	100 50	ksps ksps	V_{DD} = V_{REF} = 5V V_{DD} = V_{REF} = 2.7V
DC Accuracy:						
Resolution			12		bits	
Integral Nonlinearity	INL	— —	±0.75 ±1	±1 ±2	LSB LSB	MCP3201-B MCP3201-C
Differential Nonlinearity	DNL	—	±0.5	±1	LSB	No missing codes over temperature
Offset Error		—	±1.25	±3	LSB	
Gain Error		—	±1.25	±5	LSB	
Dynamic Performance:						
Total Harmonic Distortion	THD	—	-82	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Signal to Noise and Distortion (SINAD)	SINAD	—	72	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Spurious Free Dynamic Range	SFDR	—	86	—	dB	V_{IN} = 0.1V to 4.9V@1 kHz
Reference Input:						
Voltage Range		0.25	—	V_{DD}	V	**Note 2**
Current Drain		— —	100 .001	150 3	µA µA	 $\overline{CS}$ = V_{DD} = 5V
Analog Inputs:						
Input Voltage Range (IN+)	IN+	IN-	—	V_{REF}+IN-	V	
Input Voltage Range (IN-)	IN-	V_{SS}-100		V_{SS}+100	mV	
Leakage Current		—	0.001	±1	µA	
Switch Resistance	R_{SS}	—	1K	—	W	See Figure 4-1
Sample Capacitor	C_{SAMPLE}	—	20	—	pF	See Figure 4-1

Note 1: This parameter is established by characterization and not 100% tested.

2: See graph that relates linearity performance to V_{REF} level.

3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

ELECTRICAL CHARACTERISTICS (CONTINUED)

All parameters apply at V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_{AMB} = -40°C to +85°C, f_{SAMPLE} = 100 ksps, and f_{CLK} = 16*f_{SAMPLE} unless otherwise noted.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Digital Input/Output:						
Data Coding Format			Straight Binary			
High Level Input Voltage	V_{IH}	0.7 V_{DD}	—	—	V	
Low Level Input Voltage	V_{IL}	—	—	0.3 V_{DD}	V	
High Level Output Voltage	V_{OH}	4.1	—	—	V	I_{OH} = -1 mA, V_{DD} = 4.5V
Low Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1 mA, V_{DD} = 4.5V
Input Leakage Current	I_{LI}	-10	—	10	µA	V_{IN} = V_{SS} or V_{DD}
Output Leakage Current	I_{LO}	-10	—	10	µA	V_{OUT} = V_{SS} or V_{DD}
Pin Capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	—	10	pF	V_{DD} = 5.0V **(Note 1)** T_{AMB} = 25°C, f = 1 MHz
Timing Parameters:						
Clock Frequency	f_{CLK}	— —	— —	1.6 0.8	MHz MHz	V_{DD} = 5V **(Note 3)** V_{DD} = 2.7V **(Note 3)**
Clock High Time	t_{HI}	312	—	—	ns	
Clock Low Time	t_{LO}	312	—	—	ns	
$\overline{CS}$ Fall To First Rising CLK Edge	t_{SUCS}	100	—	—	ns	
CLK Fall To Output Data Valid	t_{DO}	—	—	200	ns	See Test Circuits, Figure 1-2
CLK Fall To Output Enable	t_{EN}	—	—	200	ns	See Test Circuits, Figure 1-2
$\overline{CS}$ Rise To Output Disable	t_{DIS}	—	—	100	ns	See Test Circuits, Figure 1-2 **(Note 1)**
$\overline{CS}$ Disable Time	t_{CSH}	625	—	—	ns	
D_{OUT} Rise Time	t_R	—	—	100	ns	See Test Circuits, Figure 1-2 **(Note 1)**
D_{OUT} Fall Time	t_F	—	—	100	ns	See Test Circuits, Figure 1-2 **(Note 1)**
Power Requirements:						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	— —	300 210	400 —	µA µA	V_{DD} = 5.0V, D_{OUT} unloaded V_{DD} = 2.7V, D_{OUT} unloaded
Standby Current	I_{DDS}	—	0.5	2	µA	$\overline{CS}$ = V_{DD} = 5.0V
Temperature Ranges:						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistance:						
Thermal Resistance, 8L-PDIP	q_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	q_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	q_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-TSSOP	q_{JA}	—	124	—	°C/W	

Note 1: This parameter is established by characterization and not 100% tested.

2: See graph that relates linearity performance to V_{REF} level.

3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See Section 6.2 for more information.

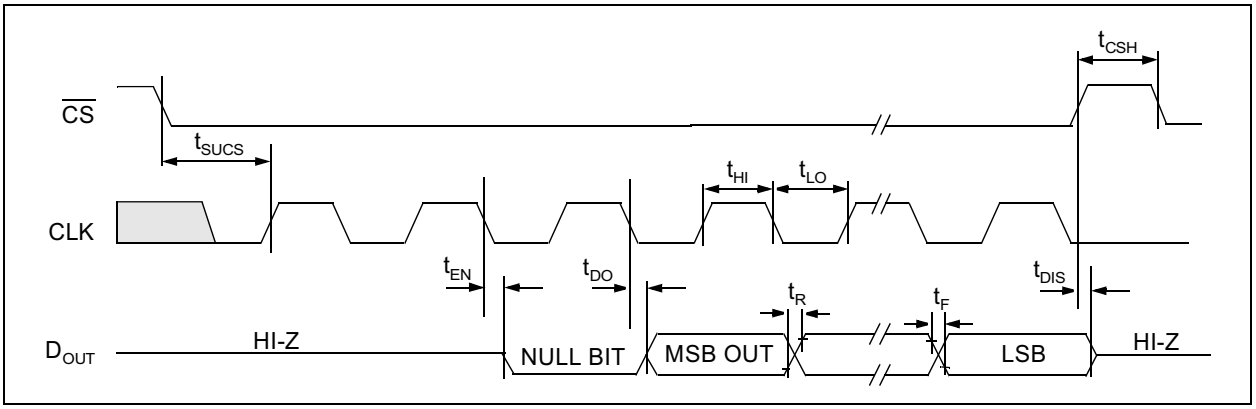
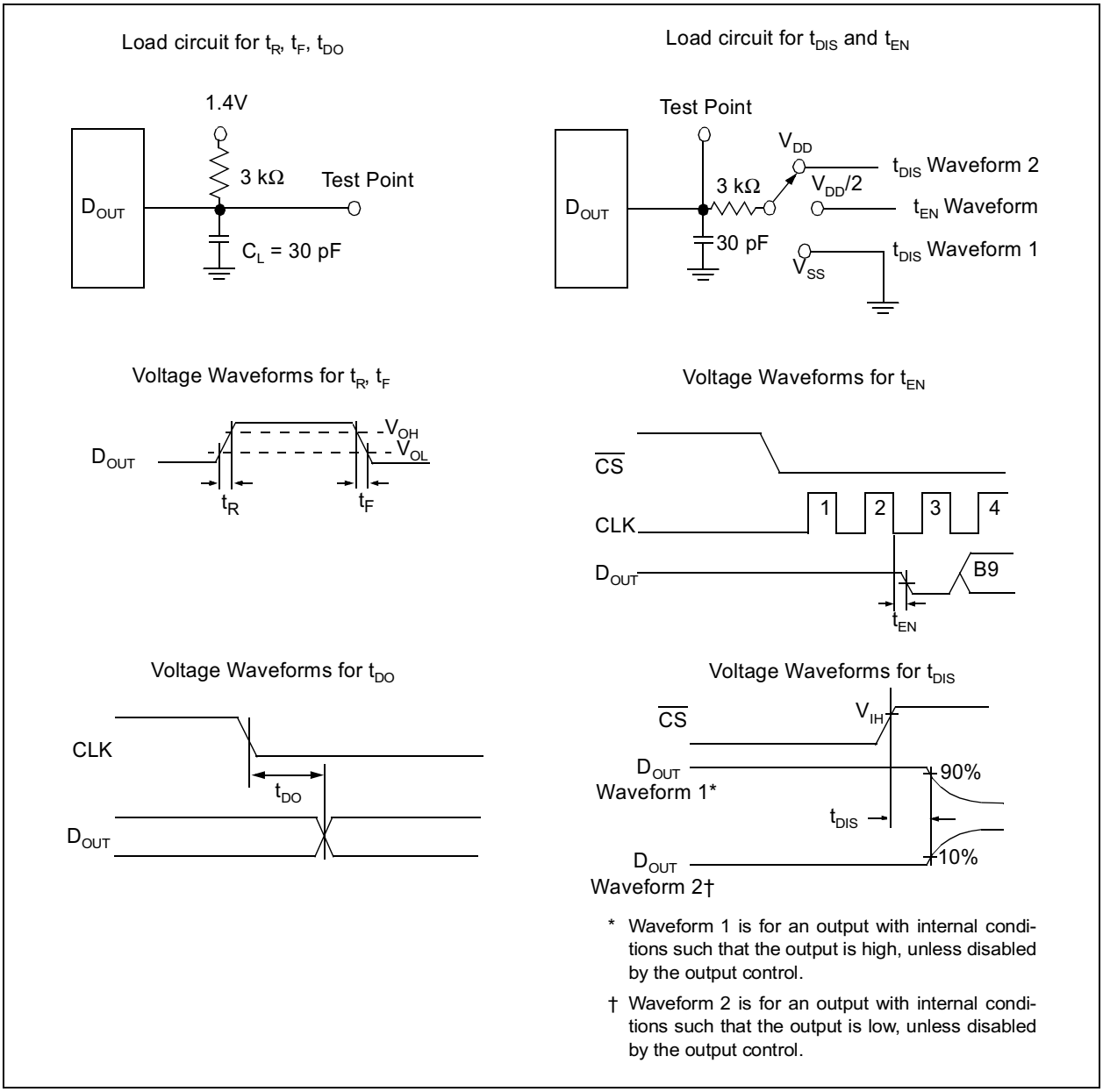


FIGURE 1-1: *Serial Timing.*



* Waveform 1 is for an output with internal conditions such that the output is high, unless disabled by the output control.

† Waveform 2 is for an output with internal conditions such that the output is low, unless disabled by the output control.

FIGURE 1-2: *Test Circuits.*

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = 25°C$

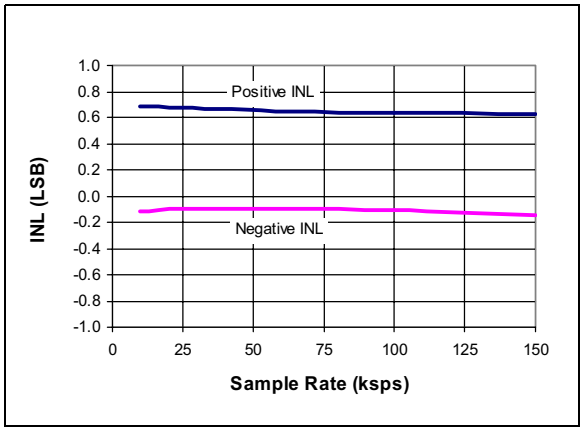


FIGURE 2-1: *Integral Nonlinearity (INL) vs. Sample Rate.*

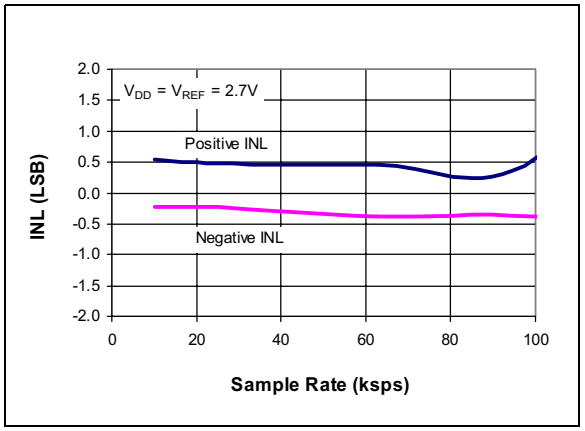


FIGURE 2-4: *Integral Nonlinearity (INL) vs. Sample Rate (V_{DD} = 2.7V).*

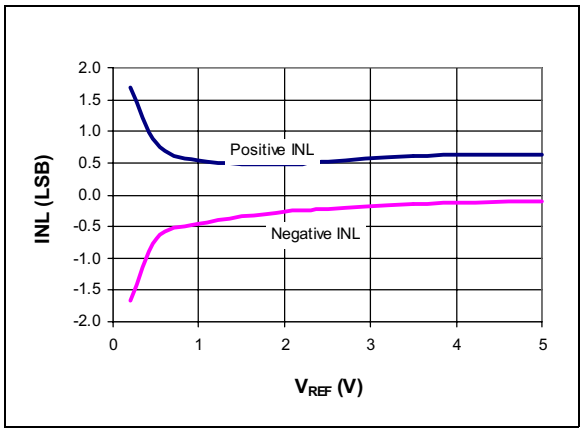


FIGURE 2-2: *Integral Nonlinearity (INL) vs. V_{REF}.*

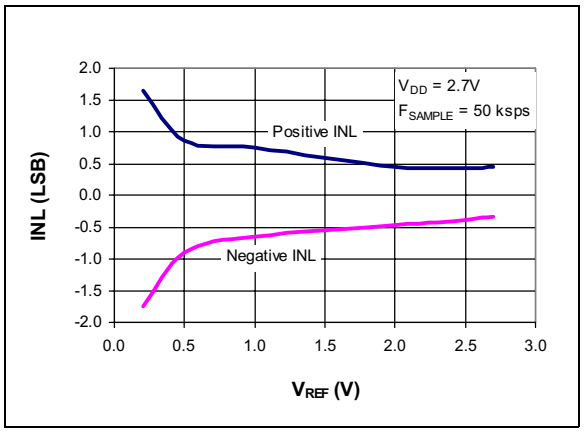


FIGURE 2-5: *Integral Nonlinearity (INL) vs. V_{REF} (V_{DD} = 2.7V).*

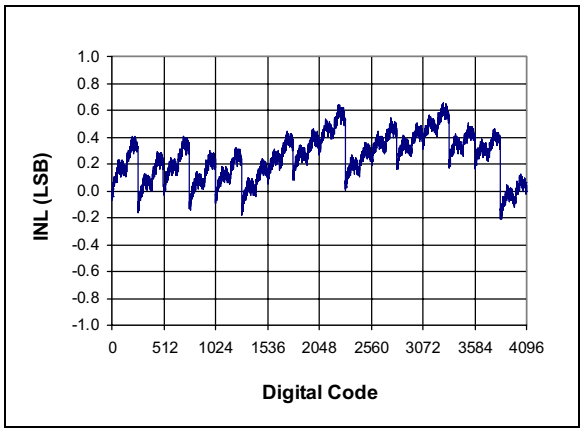


FIGURE 2-3: *Integral Nonlinearity (INL) vs. Code (Representative Part).*

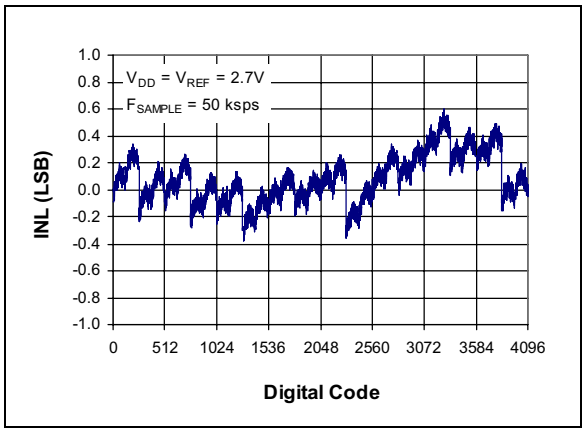


FIGURE 2-6: *Integral Nonlinearity (INL) vs. Code (Representative Part, V_{DD} = 2.7V).*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = 25°C$

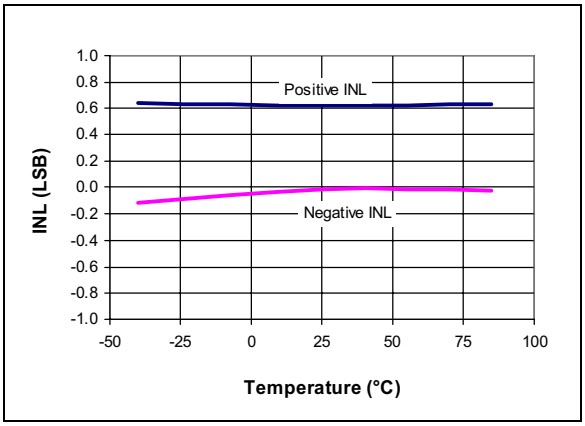


FIGURE 2-7: *Integral Nonlinearity (INL) vs. Temperature.*

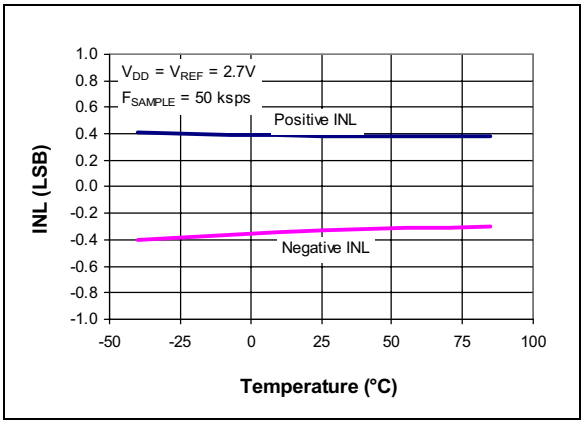


FIGURE 2-10: *Integral Nonlinearity (INL) vs. Temperature (V_{DD} = 2.7V).*

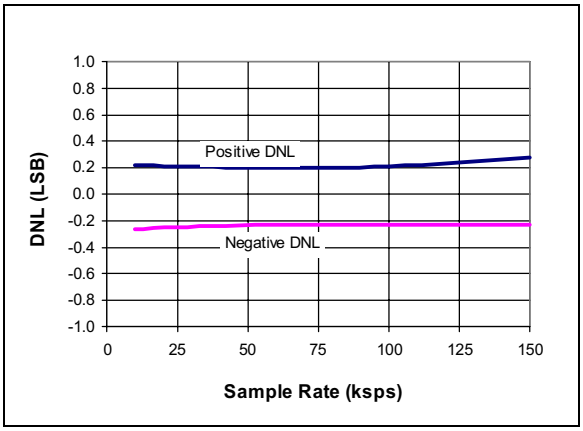


FIGURE 2-8: *Differential Nonlinearity (DNL) vs. Sample Rate.*

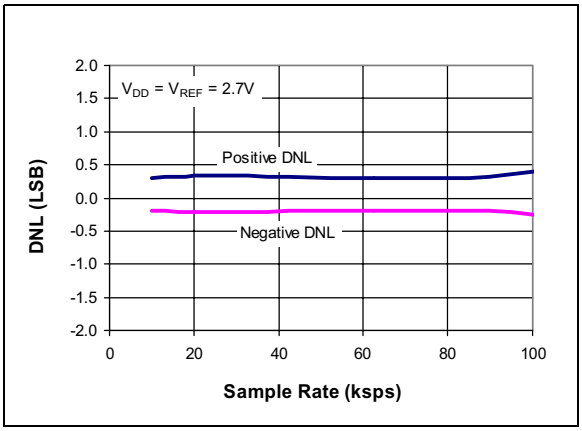


FIGURE 2-11: *Differential Nonlinearity (DNL) vs. Sample Rate (V_{DD} = 2.7V).*

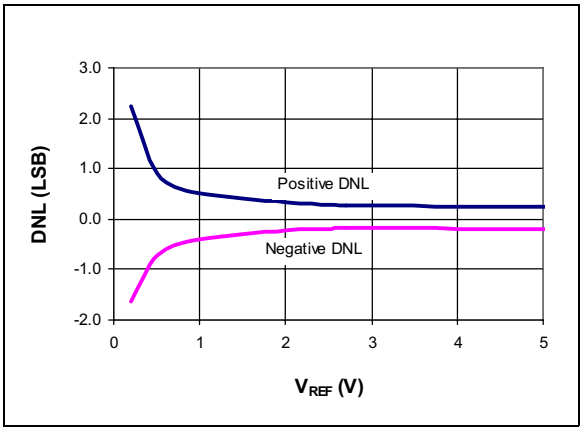


FIGURE 2-9: *Differential Nonlinearity (DNL) vs. V_{REF}.*

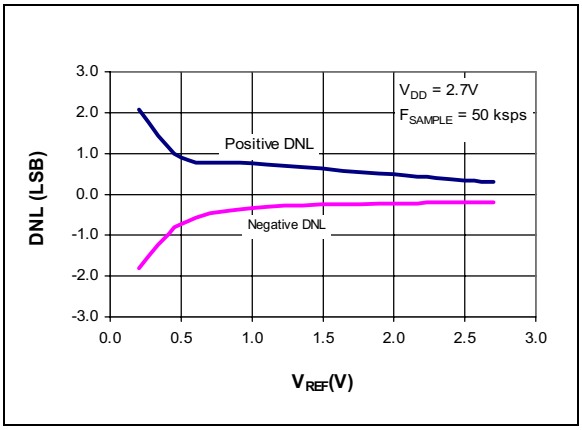


FIGURE 2-12: *Differential Nonlinearity (DNL) vs. V_{REF} (V_{DD} = 2.7V).*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = 25°C$

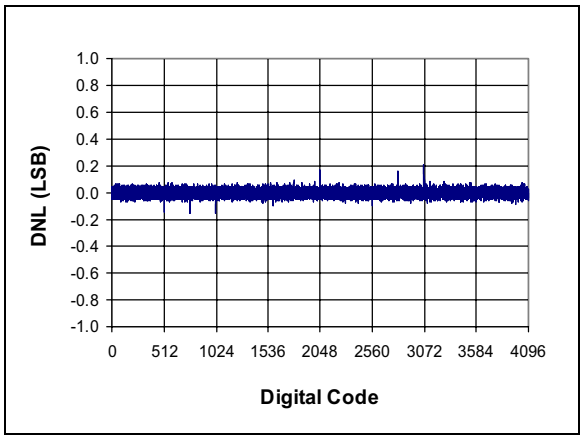


FIGURE 2-13: *Differential Nonlinearity (DNL) vs. Code (Representative Part).*

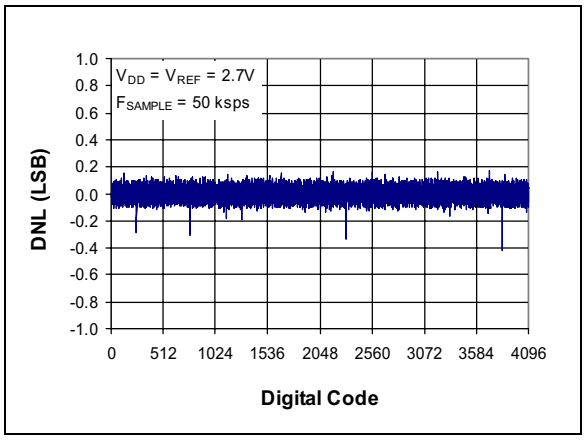


FIGURE 2-16: *Differential Nonlinearity (DNL) vs. Code (Representative Part, $V_{DD} = 2.7V$).*

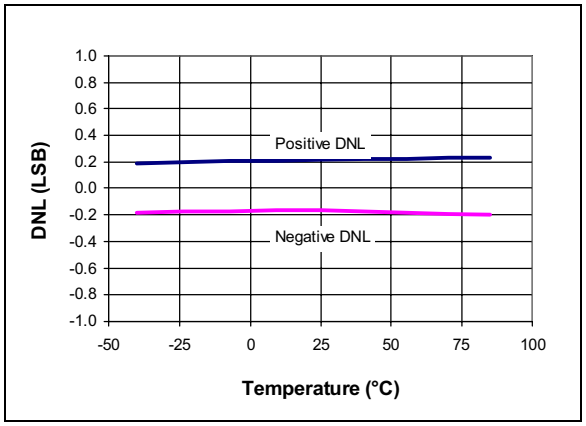


FIGURE 2-14: *Differential Nonlinearity (DNL) vs. Temperature.*

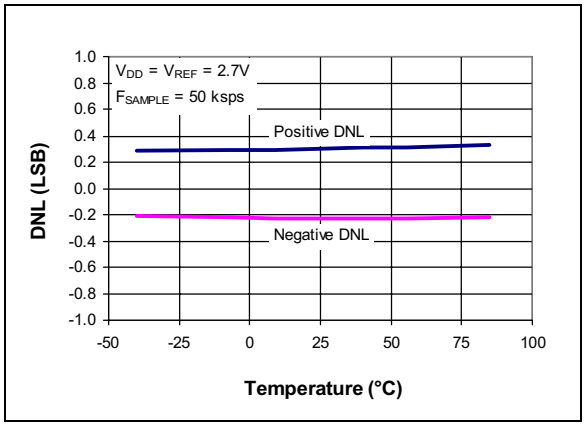


FIGURE 2-17: *Differential Nonlinearity (DNL) vs. Temperature ($V_{DD} = 2.7V$).*

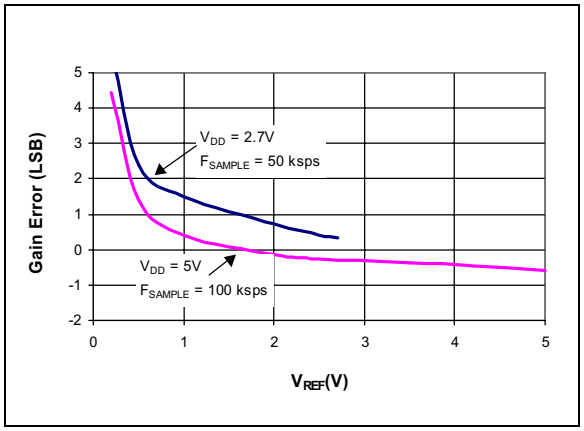


FIGURE 2-15: *Gain Error vs. V_{REF}.*

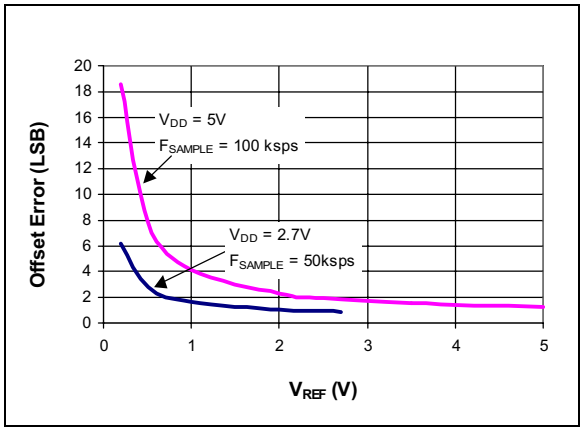


FIGURE 2-18: *Offset Error vs. V_{REF}.*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = 25°C$

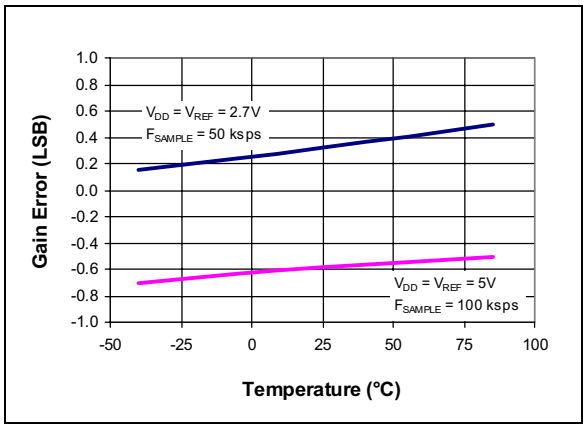


FIGURE 2-19: *Gain Error vs. Temperature.*

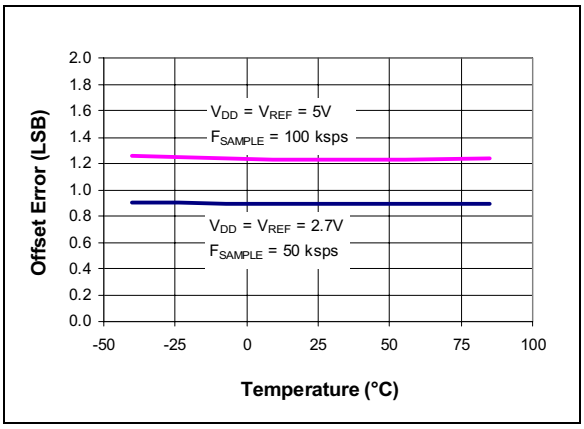


FIGURE 2-22: *Offset Error vs. Temperature.*

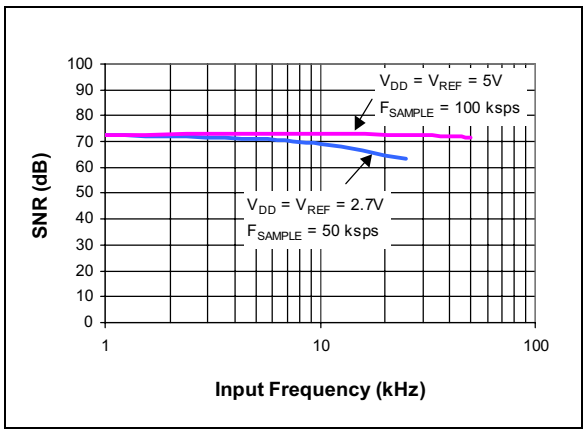


FIGURE 2-20: *Signal to Noise Ratio (SNR) vs. Input Frequency.*

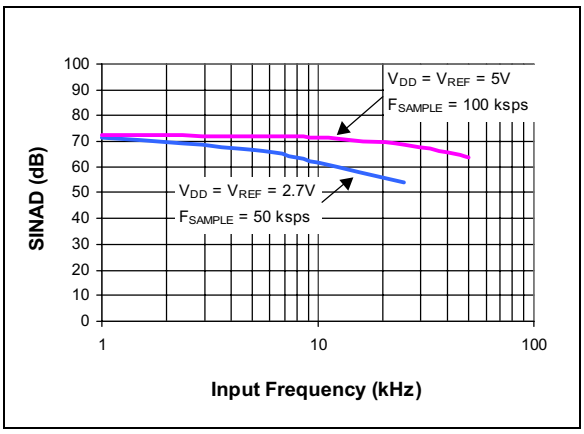


FIGURE 2-23: *Signal to Noise and Distortion (SINAD) vs. Input Frequency.*

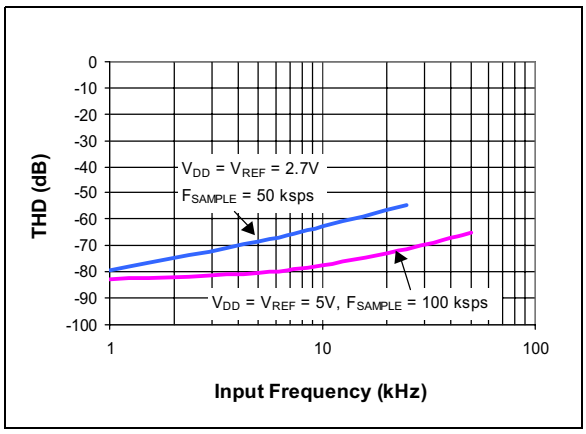


FIGURE 2-21: *Total Harmonic Distortion (THD) vs. Input Frequency.*

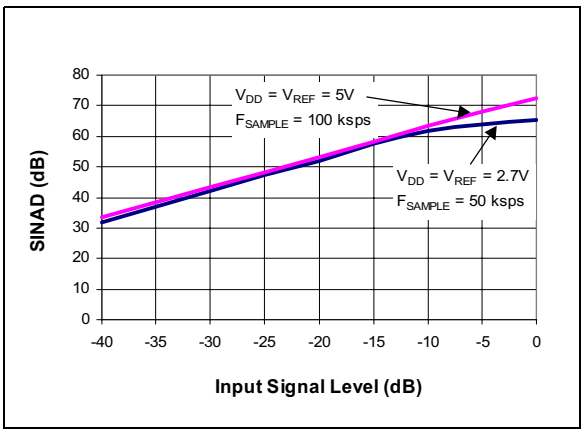


FIGURE 2-24: *Signal to Noise and Distortion (SINAD) vs. Input Signal Level.*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = 25°C$

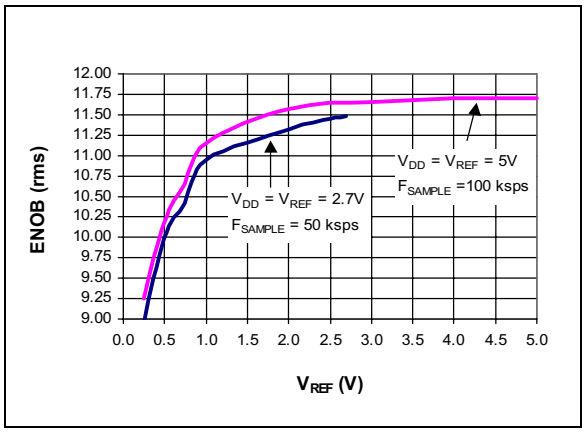


FIGURE 2-25: *Effective Number of Bits (ENOB) vs. V_{REF}.*

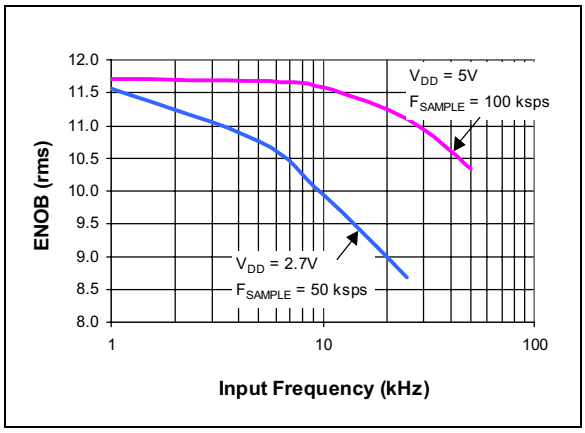


FIGURE 2-28: *Effective Number of Bits (ENOB) vs. Input Frequency.*

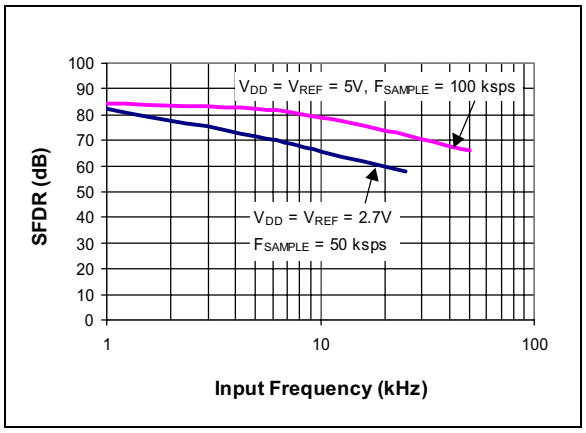


FIGURE 2-26: *Spurious Free Dynamic Range (SFDR) vs. Input Frequency.*

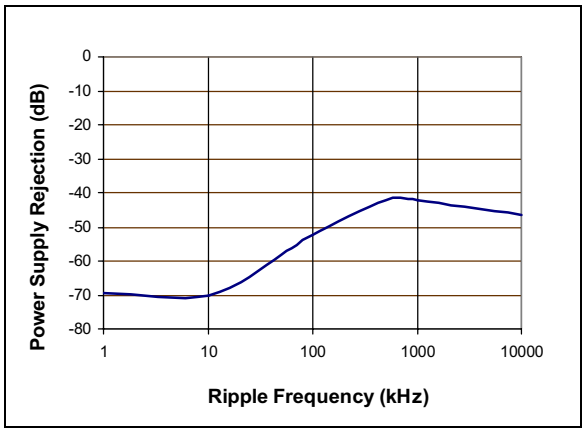


FIGURE 2-29: *Power Supply Rejection (PSR) vs. Ripple Frequency.*

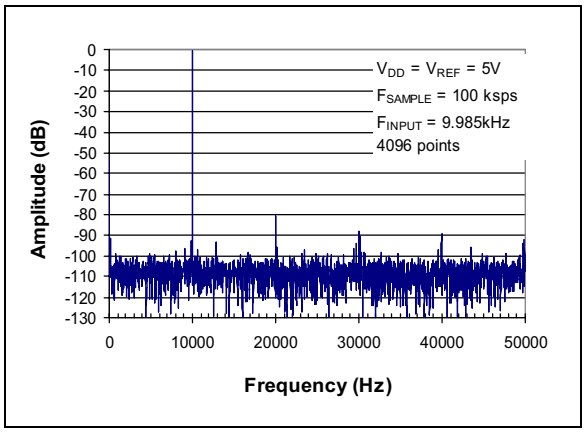


FIGURE 2-27: *Frequency Spectrum of 10 kHz input (Representative Part).*

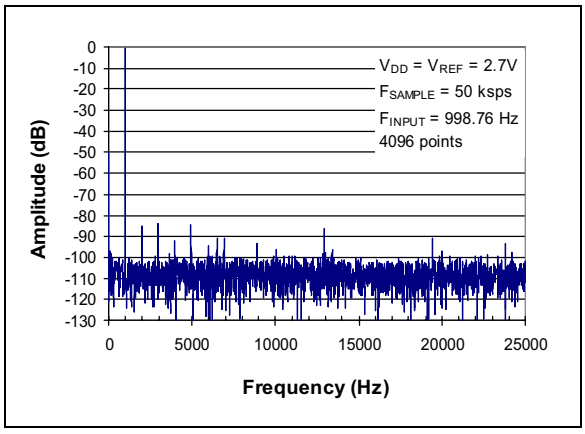


FIGURE 2-30: *Frequency Spectrum of 1 kHz input (Representative Part, $V_{DD} = 2.7V$).*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = 25°C$

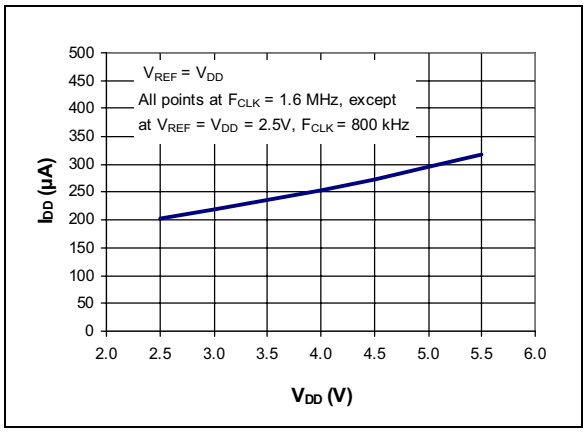


FIGURE 2-31: *I_{DD} vs. V_{DD}.*

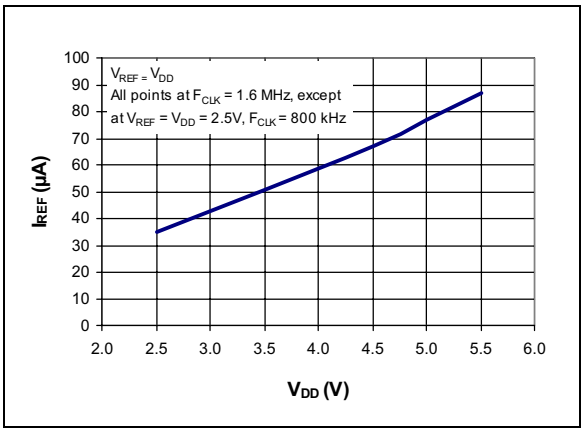


FIGURE 2-34: *I_{REF} vs. V_{DD}.*

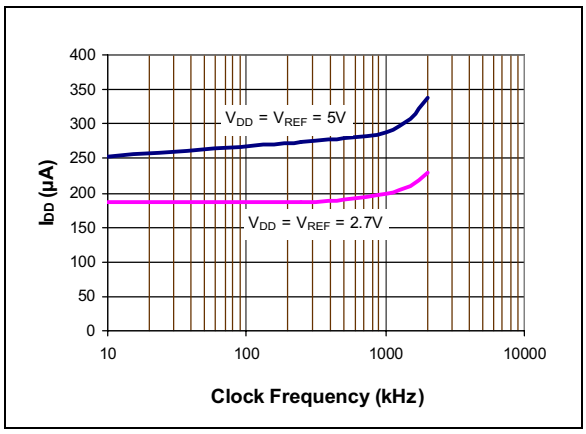


FIGURE 2-32: *I_{DD} vs. Clock Frequency.*

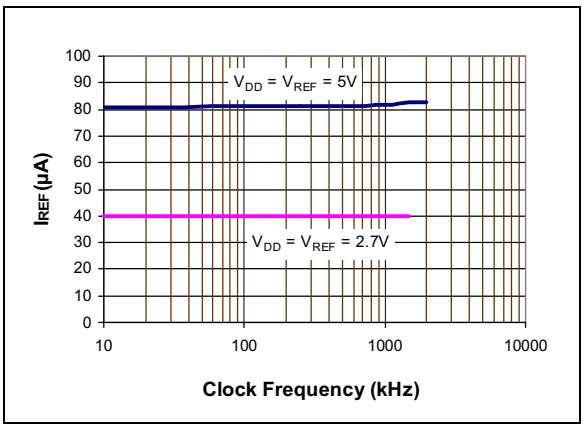


FIGURE 2-35: *I_{REF} vs. Clock Frequency.*

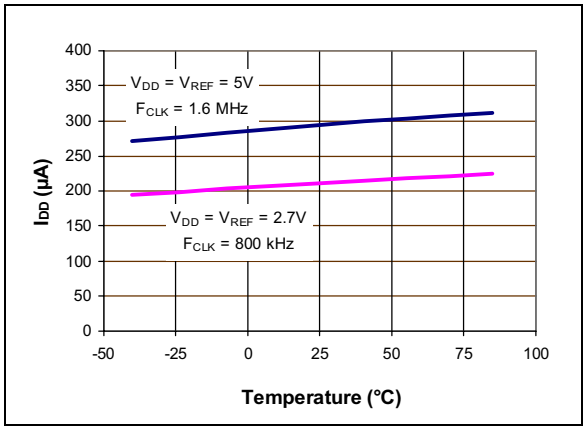


FIGURE 2-33: *I_{DD} vs. Temperature.*

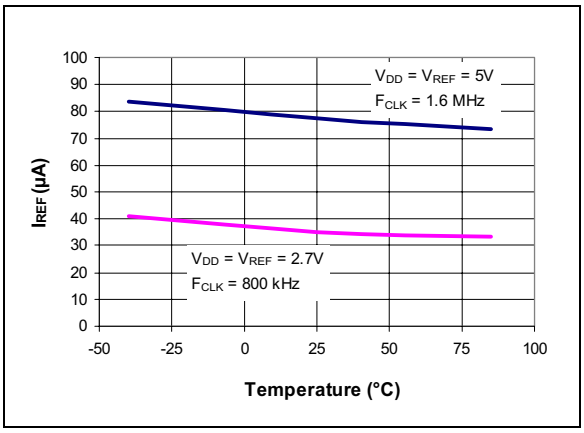


FIGURE 2-36: *I_{REF} vs. Temperature.*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = 25°C$

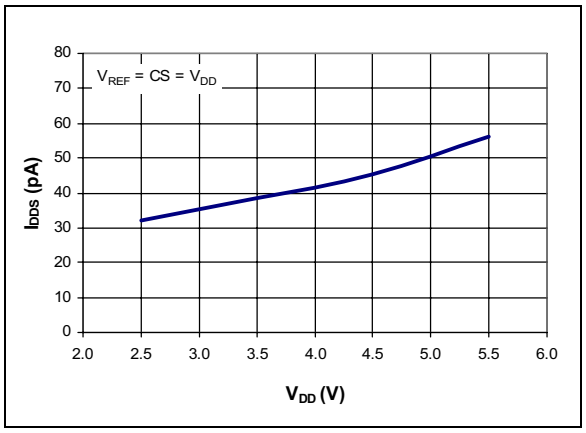


FIGURE 2-37: *I_{DDS} vs. V_{DD}.*

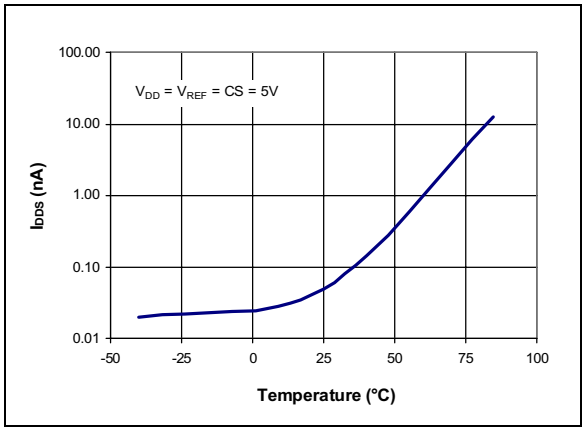


FIGURE 2-38: *I_{DDS} vs. Temperature.*

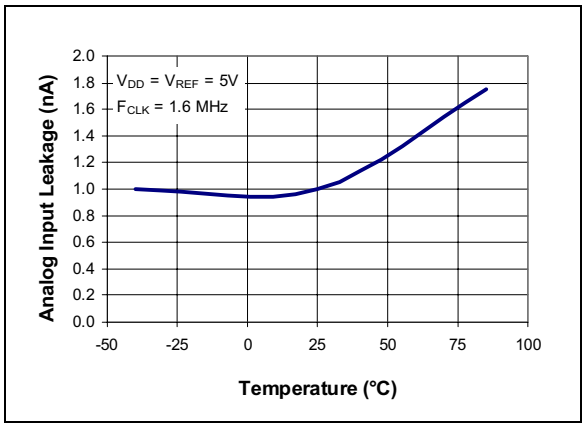


FIGURE 2-39: *Analog Input Leakage Current vs. Temperature.*

3.0 PIN DESCRIPTIONS

3.1 IN+

Positive analog input. This input can vary from IN- to V_{REF} + IN-.

3.2 IN-

Negative analog input. This input can vary ±100 mV from V_{SS}.

3.3 Chip Select/Shutdown ($\overline{CS}$/SHDN)

The $\overline{CS}$/SHDN pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The $\overline{CS}$/SHDN pin must be pulled high between conversions.

3.4 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed.

3.5 Serial Data Output (DOUT)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

4.0 DEVICE OPERATION

The MCP3201 A/D Converter employs a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the first rising edge of the serial clock after $\overline{CS}$ has been pulled low. Following this sample time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100 ksps are possible on the MCP3201. See Section 6.2 for information on minimum clock rates. Communication with the device is done using a 3-wire SPI-compatible interface.

4.1 Analog Inputs

The MCP3201 provides a single pseudo-differential input. The IN+ input can range from IN- to V_{REF} (V_{REF} +IN-). The IN- input is limited to ±100 mV from the V_{SS} rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

For the A/D Converter to meet specification, the charge holding capacitor (C_{SAMPLE}) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram, it is shown that the source impedance (R_S) adds to the internal sampling switch (R_{SS}) impedance, directly affecting the time that is required to charge the capacitor (C_{SAMPLE}). Consequently, a larger source impedance increases the offset, gain, and integral linearity errors of the conversion.

Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP601, which has a closed loop output impedance of tens of ohms. The adverse affects of higher source impedances are shown in Figure 4-2.

If the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than {[V_{REF} + (IN-)] - 1 LSB}, then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below V_{SS}, then the voltage level at the IN+ input will have to go below V_{SS} to see the 000h output code. Conversely, if IN- is more than 1 LSB above Vss, then the FFFh code will not be seen unless the IN+ input level goes above V_{REF} level.

4.2 Reference Input

The reference input (V_{REF}) determines the analog input voltage range and the LSB size, as shown below.

$$LSB\ Size = \frac{V_{REF}}{4096}$$

As the reference input is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is a function of the analog input signal and the reference input as shown below.

$$Digital\ Output\ Code = \frac{4096 * V_{IN}}{V_{REF}}$$

where:

V_{IN} = *analog input voltage = V(IN+) - V(IN-)*

V_{REF} = *reference voltage*

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the A/D Converter.

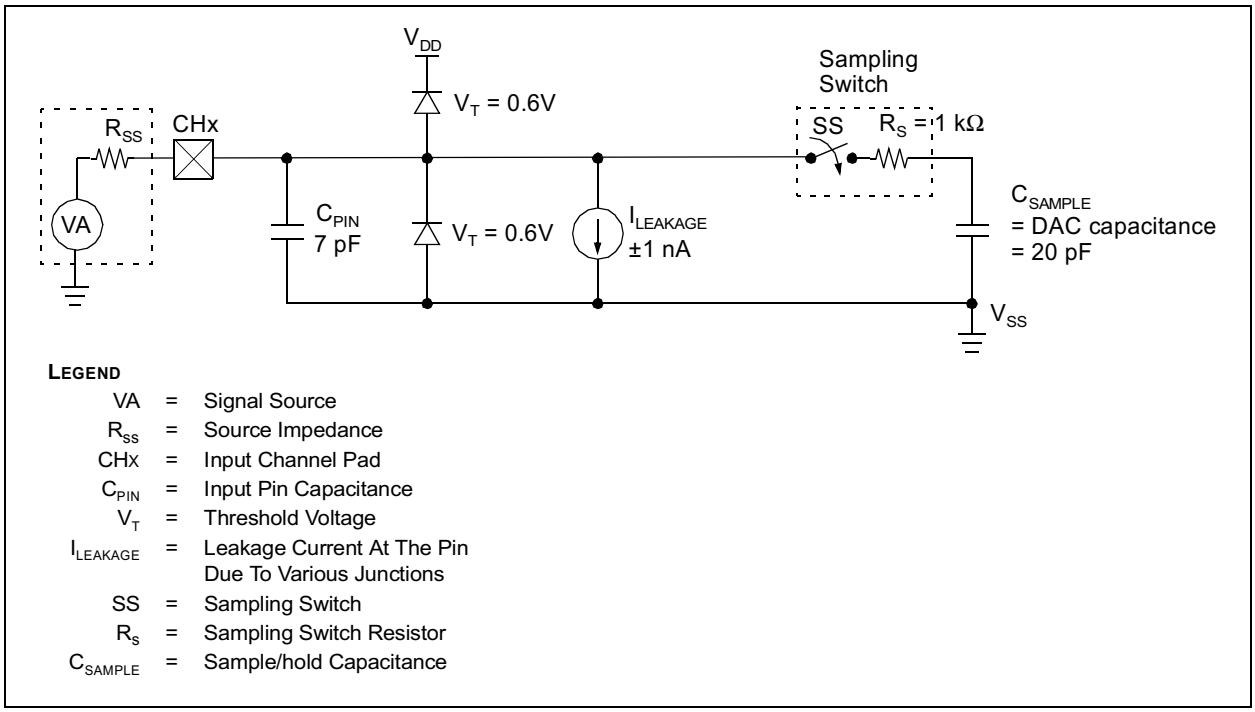


FIGURE 4-1: *Analog Input Model.*

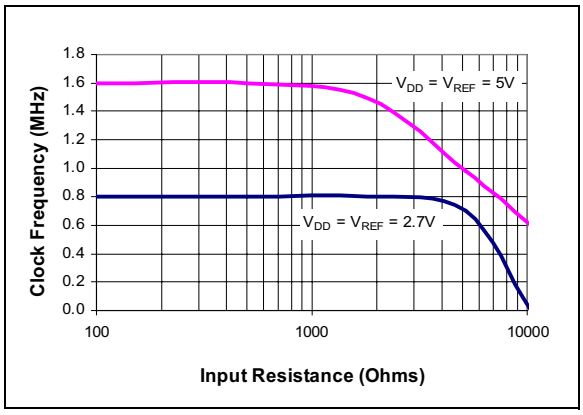
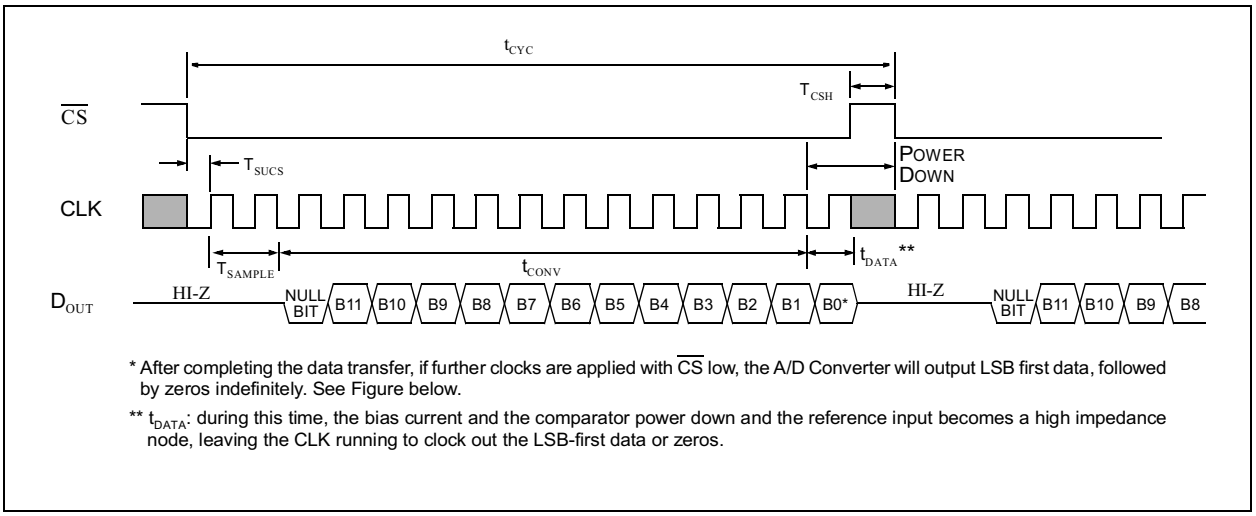


FIGURE 4-2: *Maximum Clock Frequency vs. Input Resistance (R_S) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.*

5.0 SERIAL COMMUNICATIONS

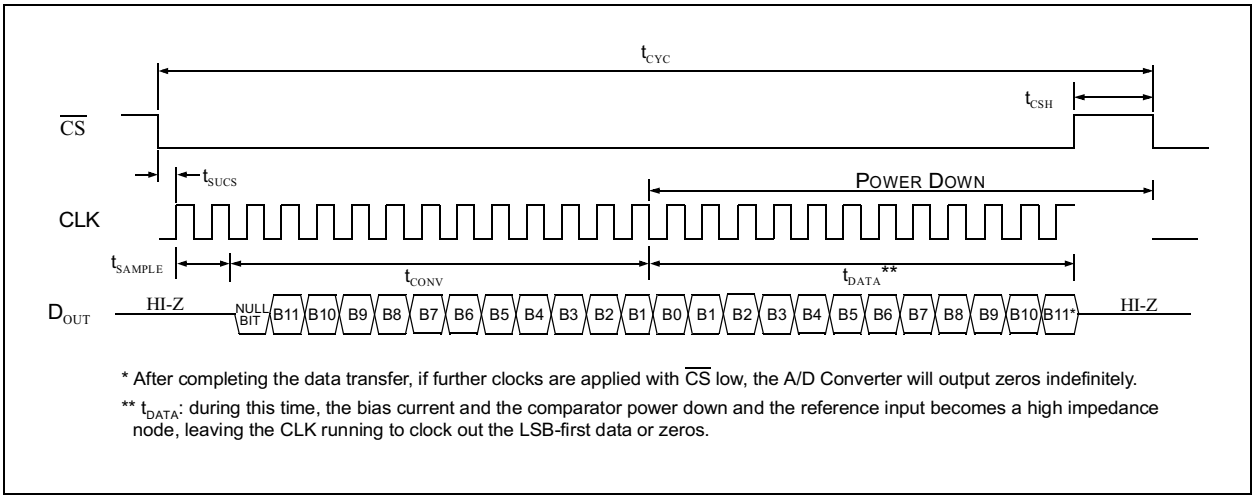
Communication with the device is done using a standard SPI-compatible serial interface. Initiating communication with the MCP3201 begins with the $\overline{CS}$ going low. If the device was powered up with the $\overline{CS}$ pin low, it must be brought high and back low to initiate communication. The device will begin to sample the analog input on the first rising edge after $\overline{CS}$ goes low. The sample period will end in the falling edge of the second clock, at which time the device will output a low null bit. The next 12 clocks will output the result of the conversion with MSB first, as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the $\overline{CS}$ is held low, the device will output the conversion result LSB first, as shown in Figure 5-2. If more clocks are provided to the device while $\overline{CS}$ is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output LSB first data, followed by zeros indefinitely. See Figure below.

** t_{DATA}: during this time, the bias current and the comparator power down and the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-1: *Communication with MCP3201 using MSB first Format.*



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output zeros indefinitely.

** t_{DATA}: during this time, the bias current and the comparator power down and the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-2: *Communication with MCP3201 using LSB first Format.*

6.0 APPLICATIONS INFORMATION

6.1 Using the MCP3201 with Microcontroller SPI Ports

With most microcontroller SPI ports, it is required to clock out eight bits at a time. If this is the case, it will be necessary to provide more clocks than are required for the MCP3201. As an example, Figure 6-1 and Figure 6-2 show how the MCP3201 can be interfaced to a microcontroller with a standard SPI port. Since the MCP3201 always clocks data out on the falling edge of clock, the MCU SPI port must be configured to match this operation. SPI Mode 0,0 (clock idles low) and SPI Mode 1,1 (clock idles high) are both compatible with the MCP3201. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the CLK from the microcontroller idles in the 'low' state. As shown in the diagram, the MSB is clocked out of the A/D Converter on the falling edge of the third clock pulse. After the first eight clocks have been sent to the device, the microcontroller's receive buffer will contain two unknown bits (the output is at high impedance for the first two clocks), the null bit and the highest order five bits of the conversion. After the second eight clocks have been sent to the device, the MCU receive register will contain the lowest order seven bits and the B1 bit repeated as the A/D Converter has begun to shift out LSB first data with the extra clock. Typical procedure would then call for the lower order byte of data to be shifted right by one bit to remove the extra B1 bit. The B7 bit is then transferred from the high order byte to the lower order byte, and then the higher order byte is shifted one bit to the right as well. Easier manipulation of the converted data can be obtained by using this method.

Figure 6-2 shows the same thing in SPI Mode 1,1 which requires that the clock idles in the high state. As with mode 0,0, the A/D Converter outputs data on the falling edge of the clock and the MCU latches data from the A/D Converter in on the rising edge of the clock.

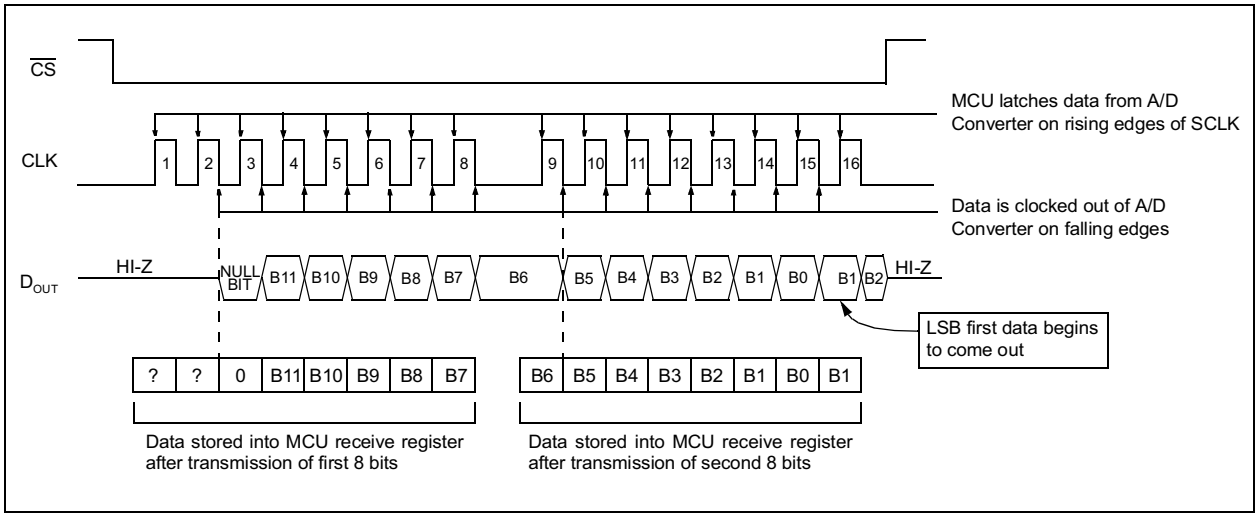


FIGURE 6-1: *SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).*

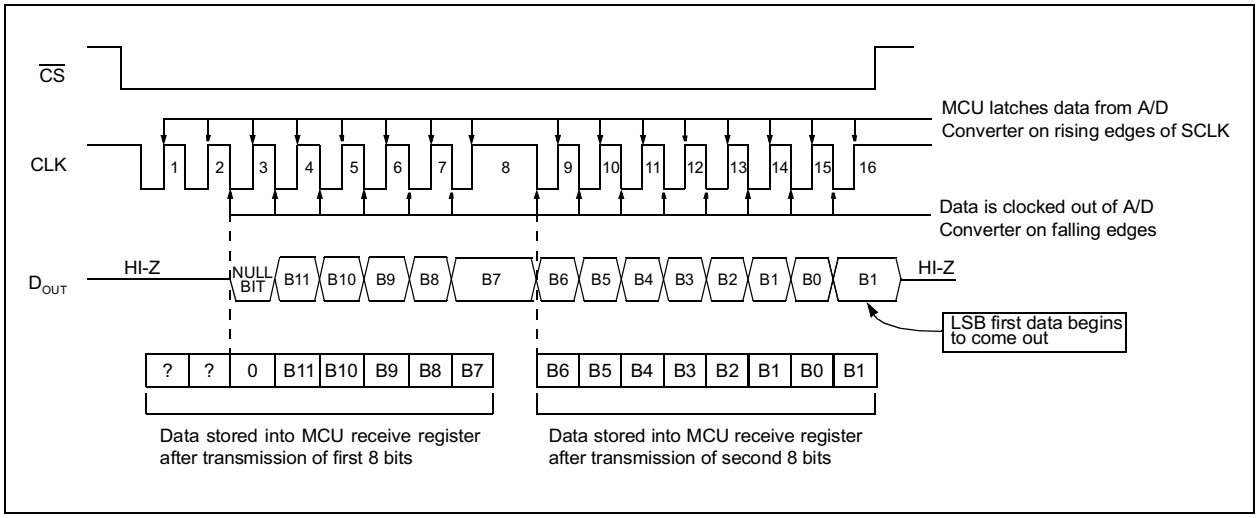


FIGURE 6-2: *SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).*

6.2 Maintaining Minimum Clock Speed

When the MCP3201 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criteria may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D Converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D Converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur. See Figure 4-2. It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results. This is illustrated in Figure 6-3 where an op amp is used to drive the analog input of the MCP3201. This amplifier provides a low impedance source for the converter input and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab™ software. FilterLab will calculate capacitor and resistor values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 *"Anti-Aliasing Analog Filters for Data Acquisition Systems."*

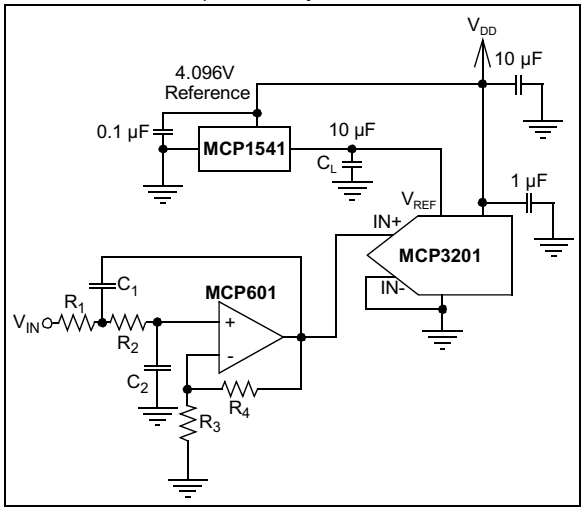


FIGURE 6-3: *The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3201.*

6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D Converter, refer to AN688 *"Layout Tips for 12-Bit A/D Converter Applications"*.

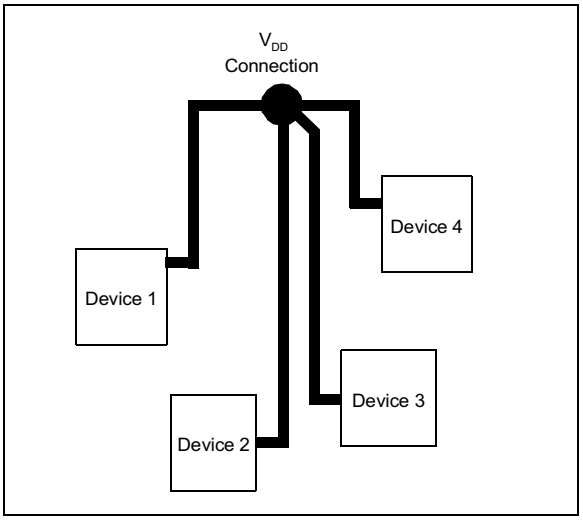
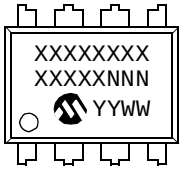


FIGURE 6-4: *V_{DD} traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.*

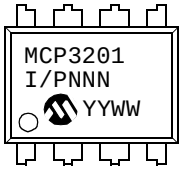
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

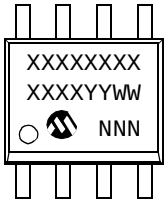
8-Lead PDIP (300 mil)



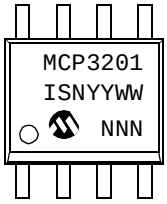
Example:



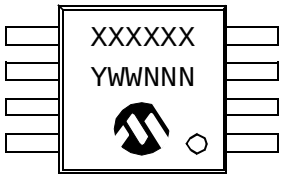
8-Lead SOIC (150 mil)



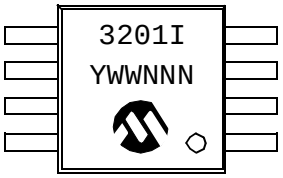
Example:



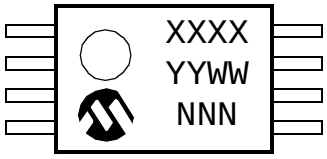
8-Lead MSOP



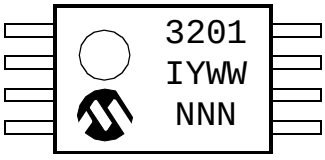
Example:



8-Lead TSSOP



Example:

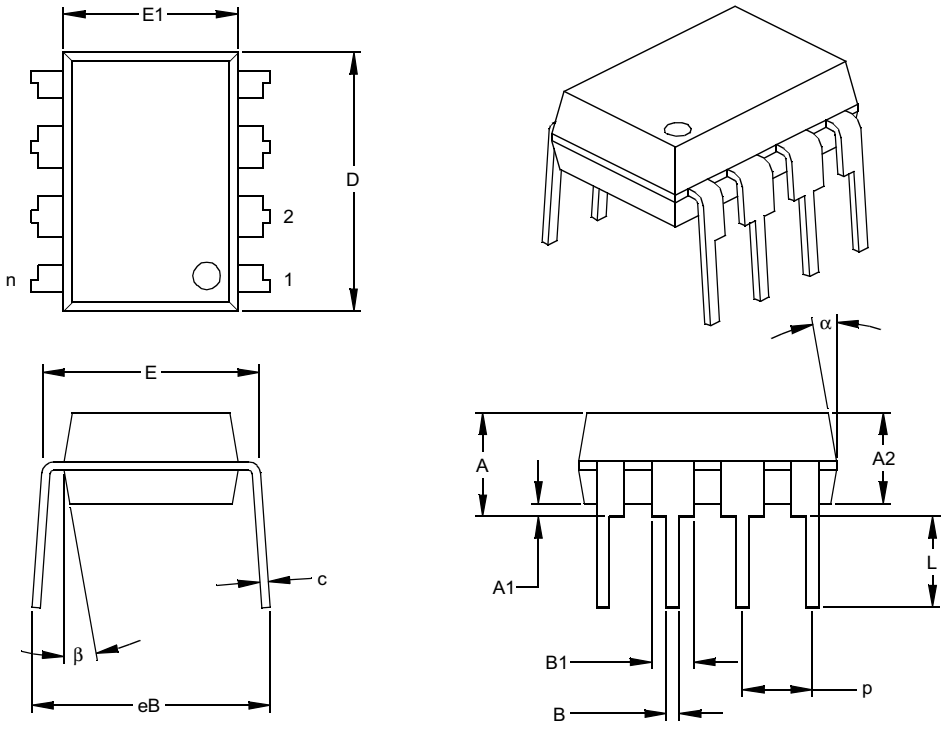


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard device marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

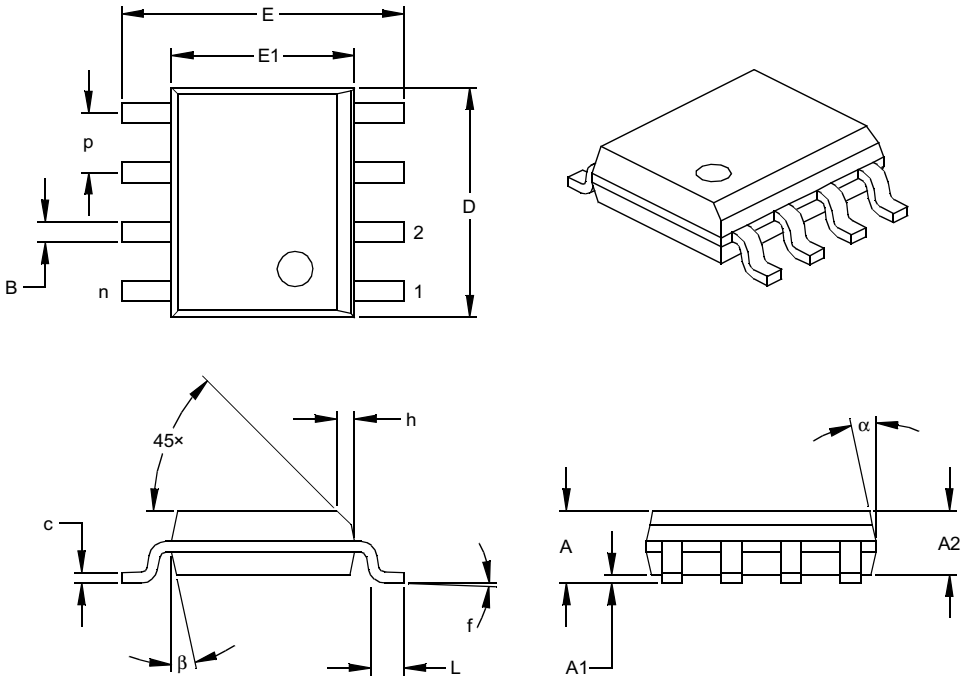


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

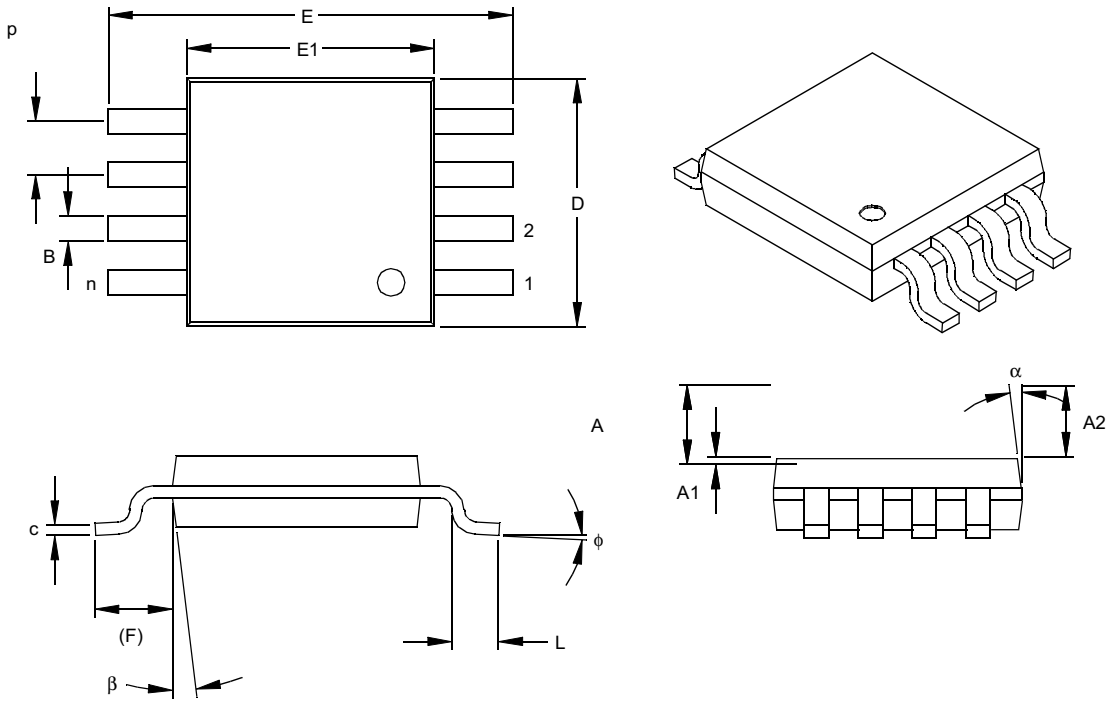


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

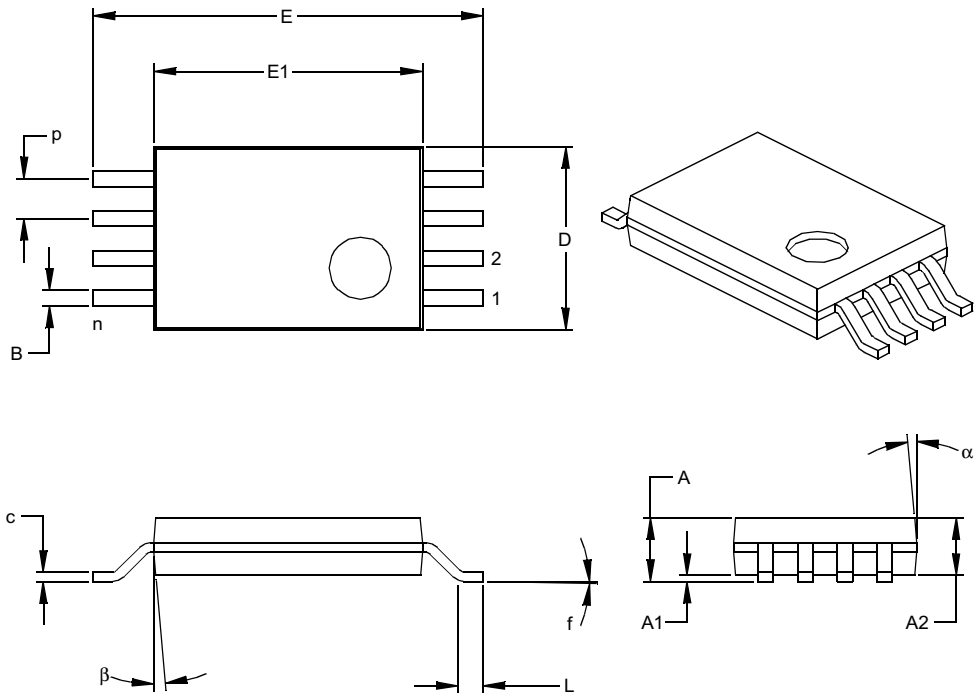
*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits.The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

013001

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager Total Pages Sent

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: **MCP3201** Literature Number: **DS21290C**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP3201:	12-Bit A/D Converter w/SPI Interface
	MCP3201T:	12-Bit A/D Converter w/SPI Interface (Tape and Reel) (SOIC and TSSOP only)
Temperature Range:	I =	-40°C to +85°C
Package:	MS =	Plastic Micro Small Outline (MSOP), 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	ST =	Plastic TSSOP (4.4 mm), 8-lead

Examples:

a) MCP3201-I/P: Industrial Temperature, PDIP package.

b) MCP3201-I/SN: Industrial Temperature, SOIC package.

c) MCP3201-I/ST: Industrial Temperature, TSSOP package.

d) MCP3201-I/MS: Industrial Temperature, MSOP package.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microID, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rfPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Term Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

Printed on recycled paper.

DNV Certification, Inc. USA
ANSI-RAB QMS ACCREDITED
DNV
DNV MSC The Netherlands Accredited by the RvA
ISO 9001 / QS-9000 REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton
Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Rm. 531, North Building
Fujian Foreign Trade Center Hotel
73 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7557563 Fax: 86-591-7557572

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

10/01/01

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

MCP3201-BI/SN MCP3201-BI/P MCP3201-CI/ST MCP3201-CI/SN MCP3201-CI/MS MCP3201-CI/P MCP3201T-CI/ST MCP3201T-CI/SN MCP3201T-BI/SN