



AHEAD OF WHAT'S POSSIBLE™

# Intro to ADRV9009:

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MAY, 2019

[WWW.ANALOG.COM/RADIOVERSE](http://WWW.ANALOG.COM/RADIOVERSE)



# Agenda

- ▶ Zero intermediate frequency (ZIF) radios vs. Super-Heterodyne radios
- ▶ Catalina (AD9361), Mykonos (AD9371), and Talise (ADRV9009) high-level overviews
- ▶ ADRV9009
  - Unboxing and using the ADRV9009
  - Evaluation Software Overview
  - Details on the ADRV9009's operation

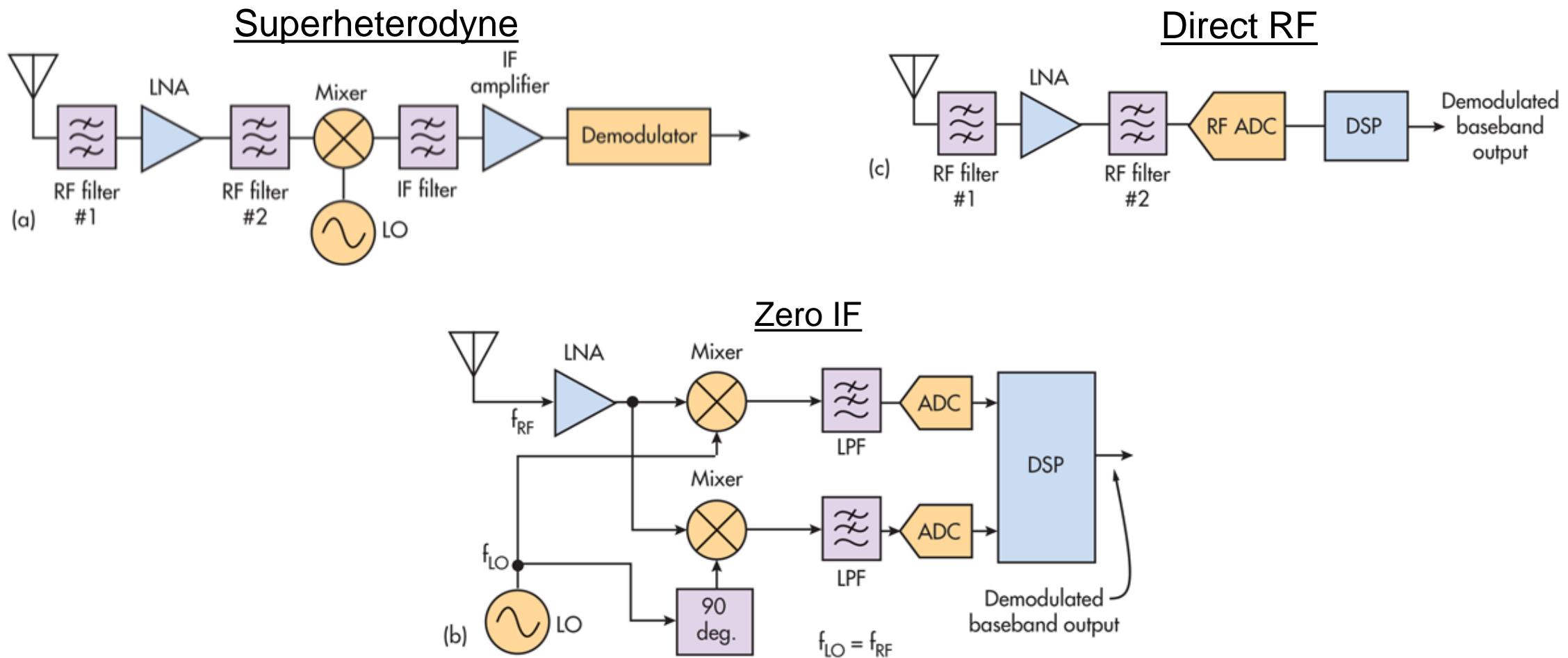


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# ZIF Transceivers

COMPARISON TO SUPER-HETERODYNE

# Tranceiver Topologies

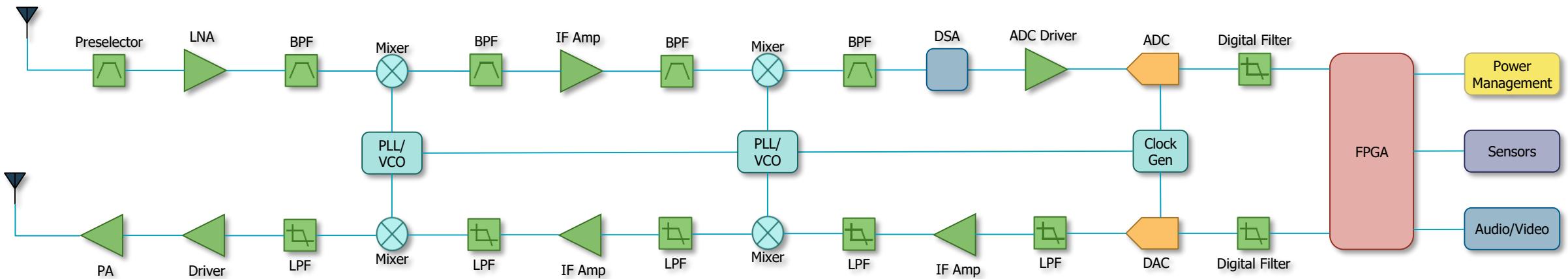


<https://www.electronicdesign.com/adc/high-speed-rf-sampling-adc-boosts-bandwidth-dynamic-range>

Lou Frenzel | Feb 22, 2017

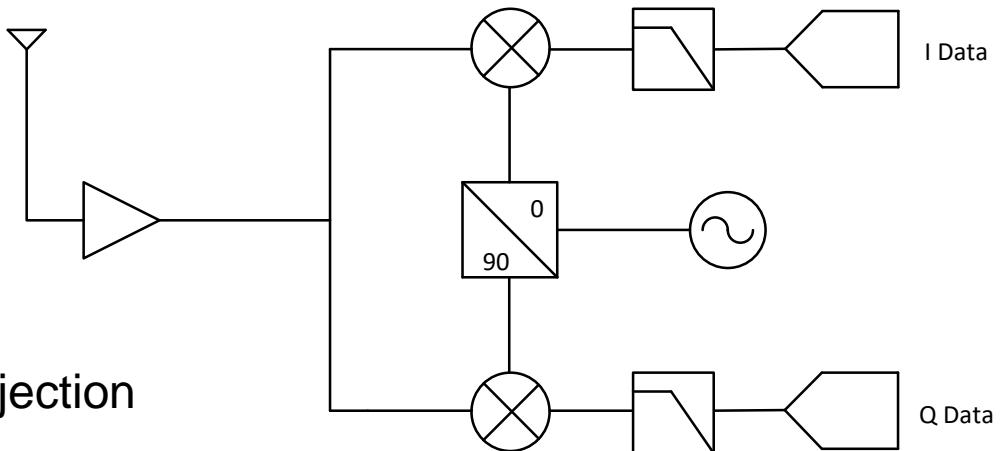
# Super-Heterodyne Overview

- Introduced 100 years ago
  - Still dominates most designs, in radar and MILCOM/EW/SIGINT
  - Trusted technique, allows for incremental improvements across devices
- High performance at the sacrifice of large size and power
  - Filters, especially in the IF strips, drive this



# Direct Conversion Overview

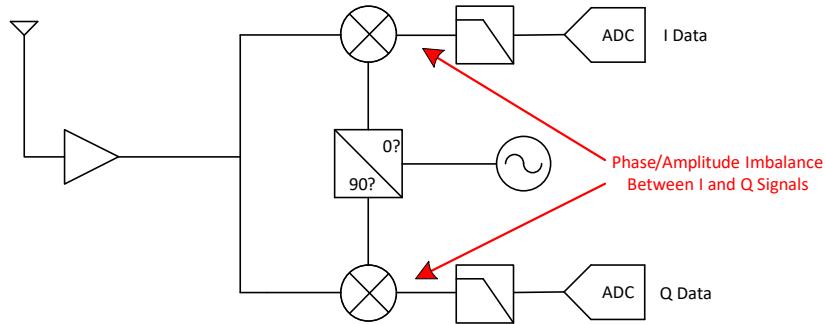
- ▶ Direct conversion attempts to simplify the super-heterodyne
- ▶ One mixing stage
  - LO = RF
    - Rx goes directly to baseband
    - Tx goes directly to the desired RF frequency
- ▶ Removes filtering complexity in the design
  - Filtering takes place at baseband
  - But dependent on mixer performance for LO and image rejection
- ▶ Has numerous advantages over the superhet architecture
  - Filtering requirements less stringent
  - Significant reduction in power consumption
    - Resulting from reduced component count and reduced sample rate
  - Significant cost reduction
    - Resulting from reduced component count and filtering requirements



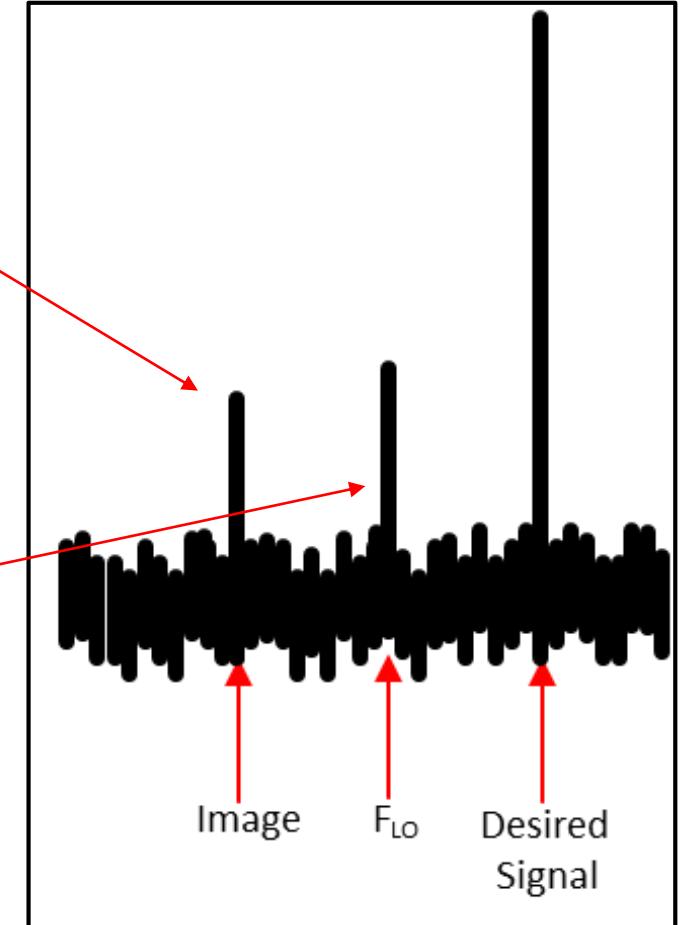
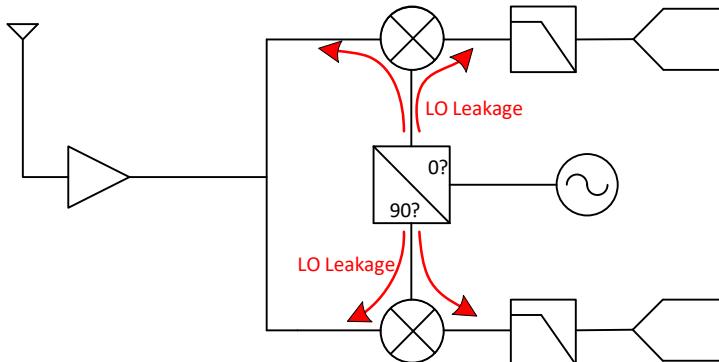
# ZIF Architecture Problems

- Disadvantages over Superhet architecture

- I/Q phase/amplitude imbalance degrades image rejection



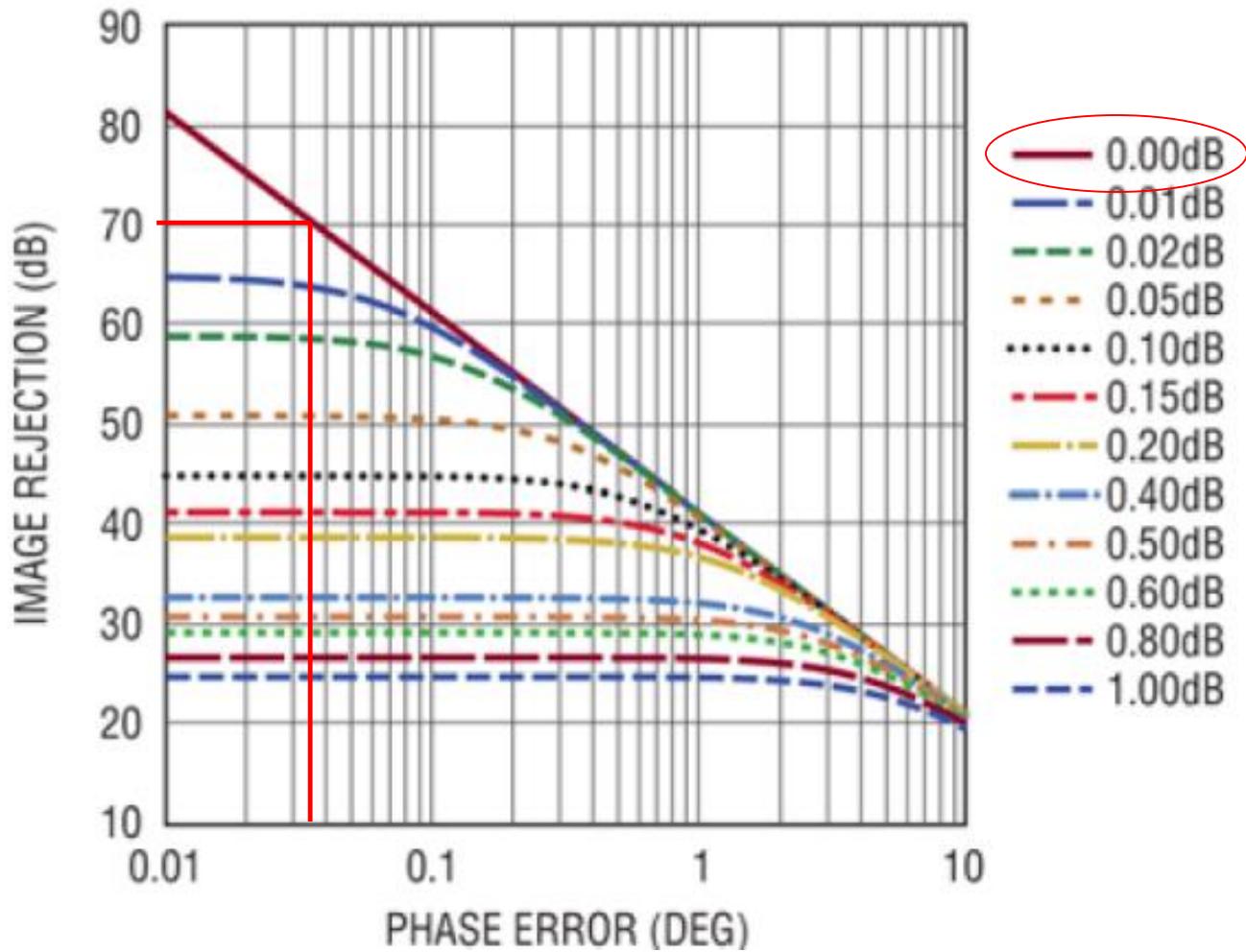
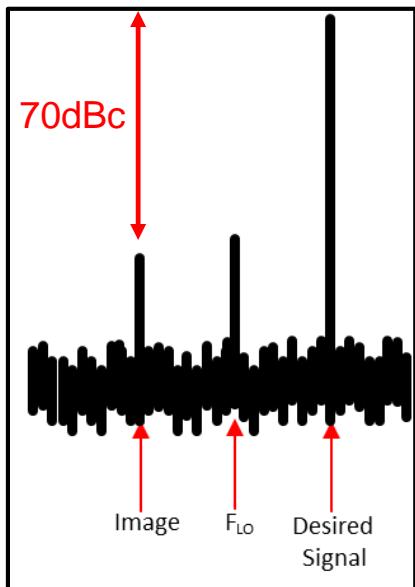
- Poor LO isolation passes LO to RF (LO Leakage) and baseband (DC Offset)



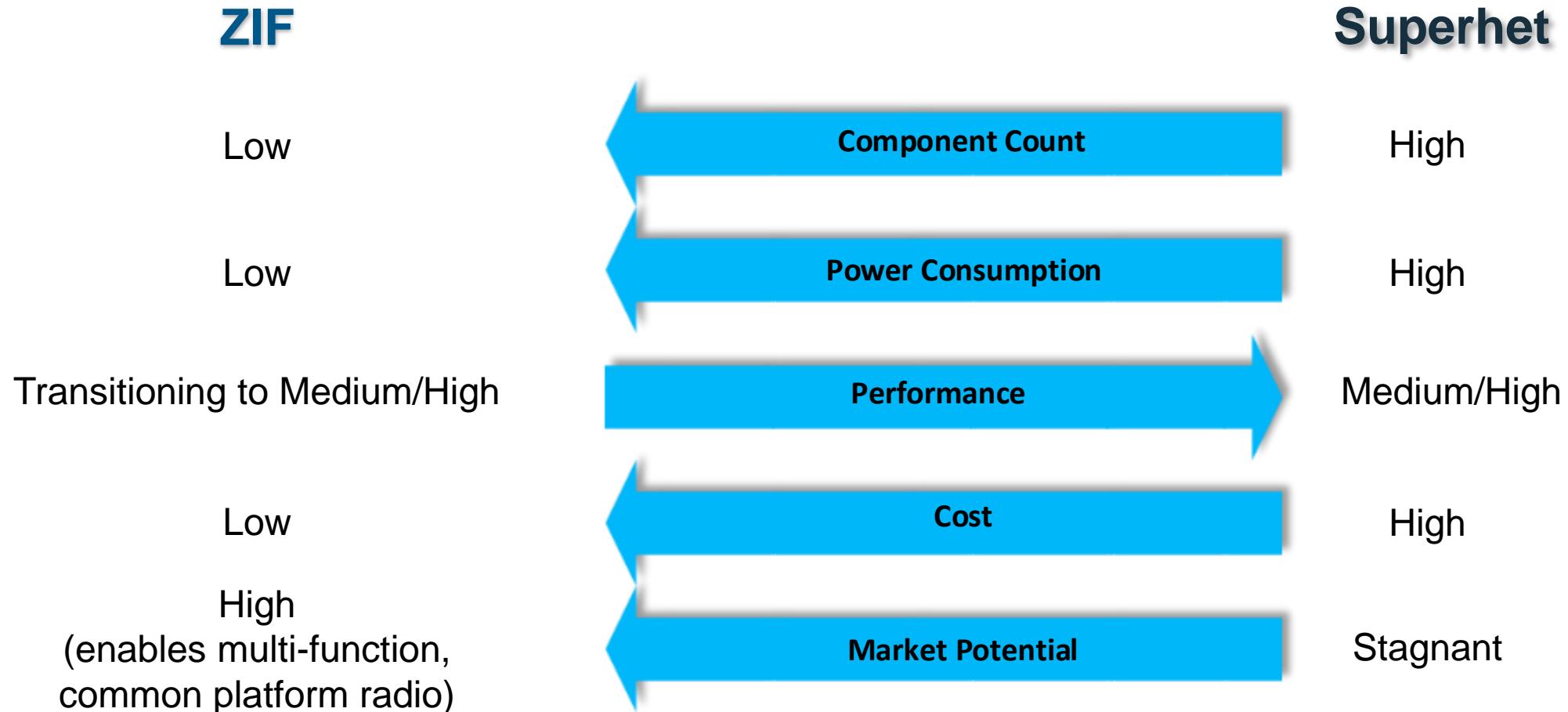
# Image Rejection Challenges

## ► How hard is 70dB image rejection?

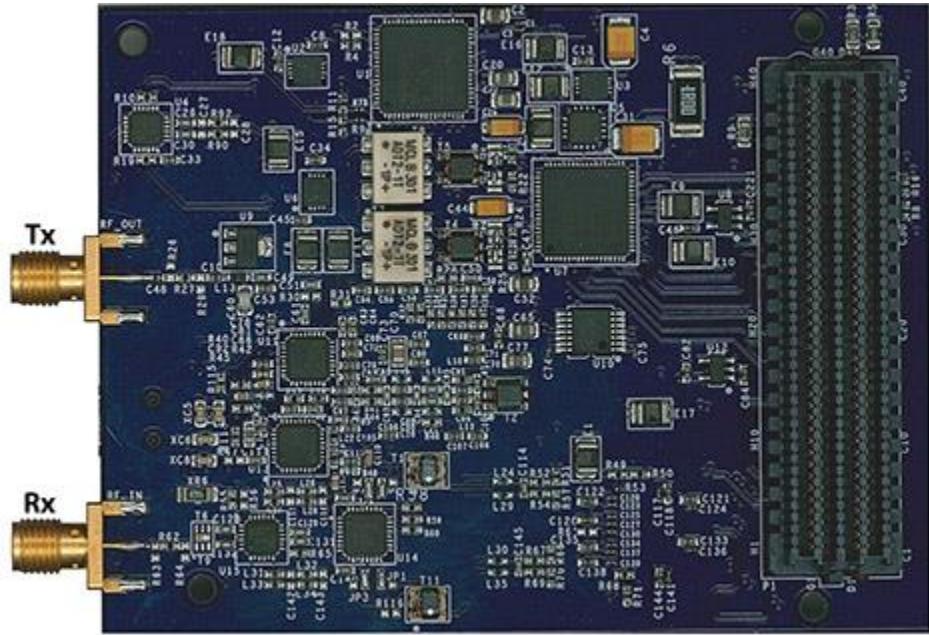
- 0.005dB I/Q gain error (11b matching)
- 0.035 deg phase error
  - ~ 30fs LO delay mismatch 4GHz
  - ~1ps LPF group delay matching



# Summary of ZIF Architecture Comparison To Superhet

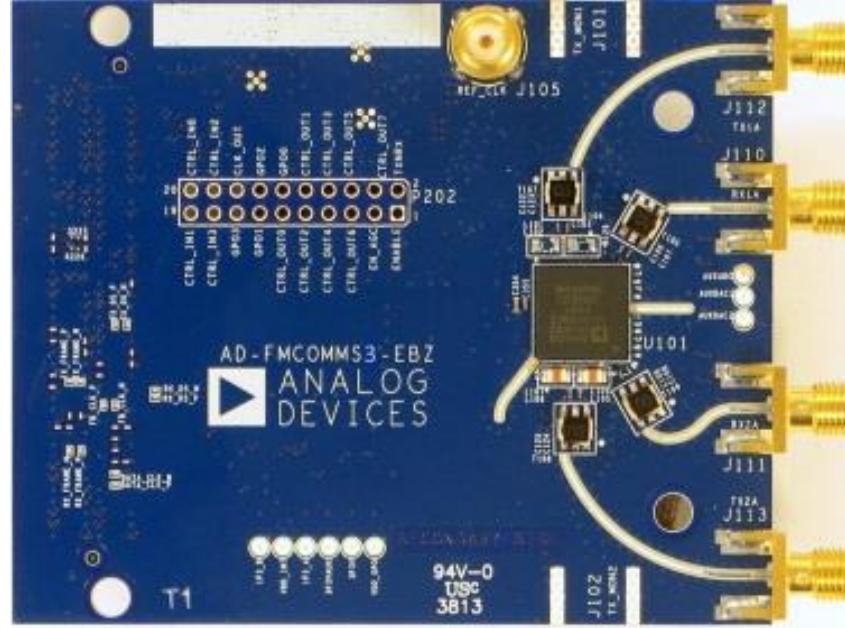


# Size and Power of Two ZIF Solutions



## AD-FMCOMMS1

- Discrete ZIF, direct RF
- 1Rx, 1Tx
- 400 MHz – 4GHz tuning range
- 200+ MHz channel bandwidth
- Power, Clocks, ADC (AD9625), DAC (AD9162), PLL, DVGA
- Radio Power Consumption=4.5W



## AD-FMCOMMS3

- AD9361 Integrated
- 2 x Rx, 2 x Tx
- 70 MHz – 6GHz tuning range
- 200kHz - 56 MHz channel bandwidth
- Power, AD9361
- Radio Power Consumption=0.7W



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## Overview of ADI's Zero IF SDR Transceivers

**Catalina (AD936x)**

**Mykonos (AD9371)**

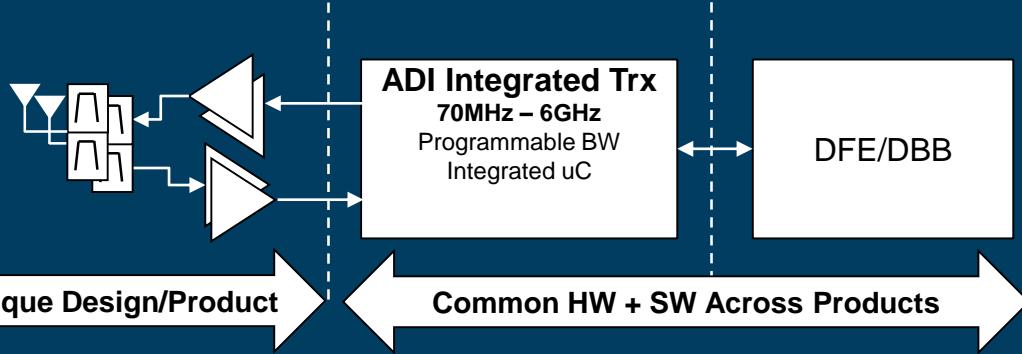
**Talise (ADRV9008/9)**

HIGH-LEVEL OVERVIEWS

# Wideband RF Transceiver Benefits

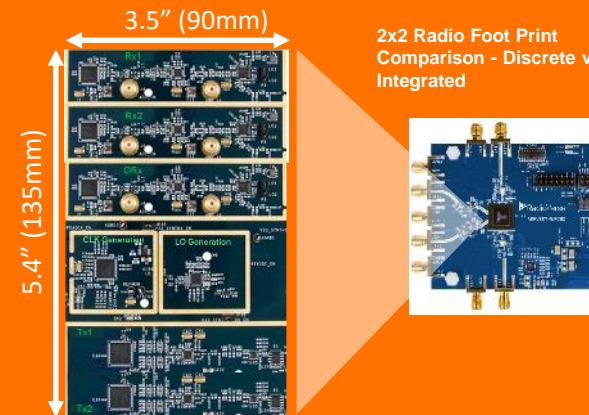
## Highly Reconfigurable

Enables reduced time to market through common HW & SW  
Small Signal Radio Platform



## Highest Level of Integration

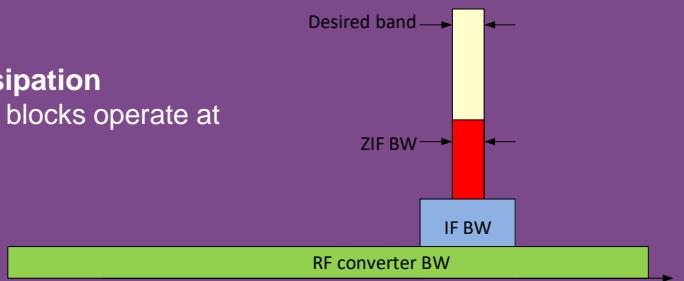
Enables higher density radio architectures e.g. M-MIMO



## Lowest Power Consumption

Reduce thermal density, enable lower SWAP radios

- Lowest possible power dissipation**
- Highest power consumption blocks operate at minimum bandwidth



## Lowest System Cost

### Re-use of architecture used in handsets

- Components such as IF filters are eliminated
- RF filters are simplified enabled by the elimination of out-of-band images or aliases

# AD9361: 2Rx/2Tx Integrated RF Transceiver (Catalina)

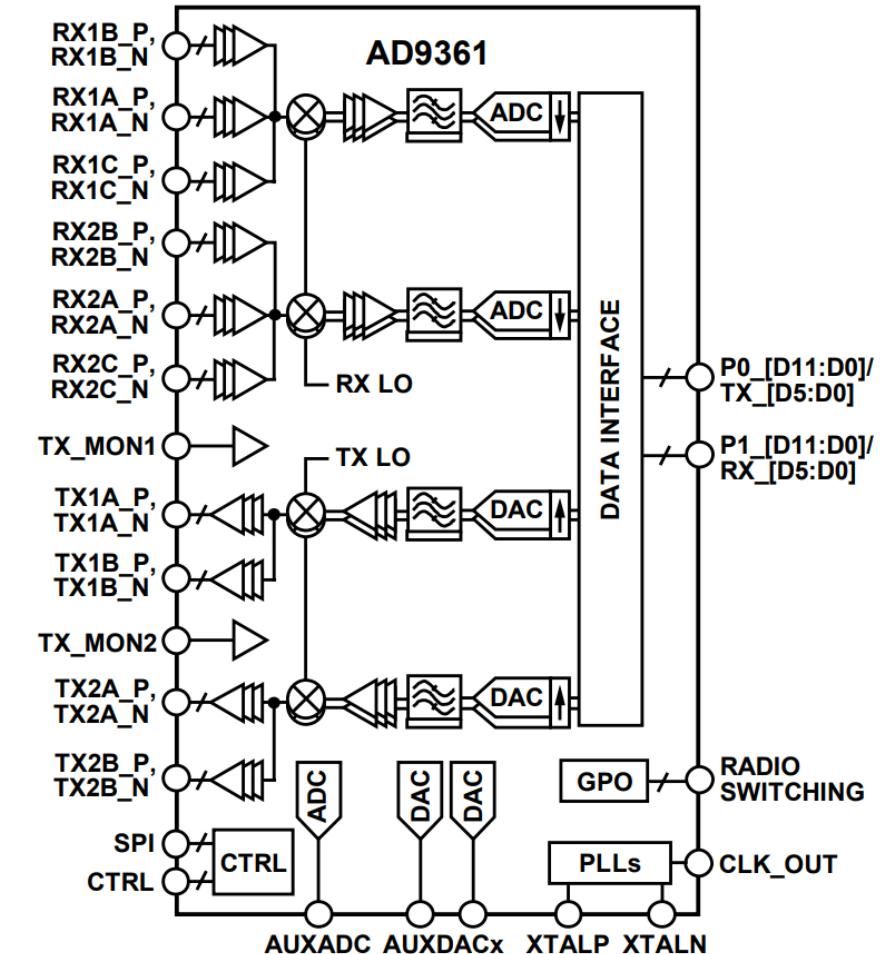
- 2Rx / 2Tx integrated RF transceiver
  - Tuning range: 70 MHz to 6GHz
  - Tunable channel BW: 200KHz to 56MHz
  - FDD/TDD operation



- Performance and power
  - Rx: 2.5dB NF
  - Tx: < -42dB Tx EVM
  - Tx Noise < -157dBm/Hz noise @ 70 MHz offset
  - Tx monitor: > 66dB dynamic range with 1dB accuracy
  - 12 bit ADCs/DACs
  - Phase noise: 0.25° @ 2.5 GHz

- Digital features
  - Rx: DC offset correction, quadrature calibration, AGC, programmable FIR filters
  - Tx: quadrature calibration, programmable FIR filters

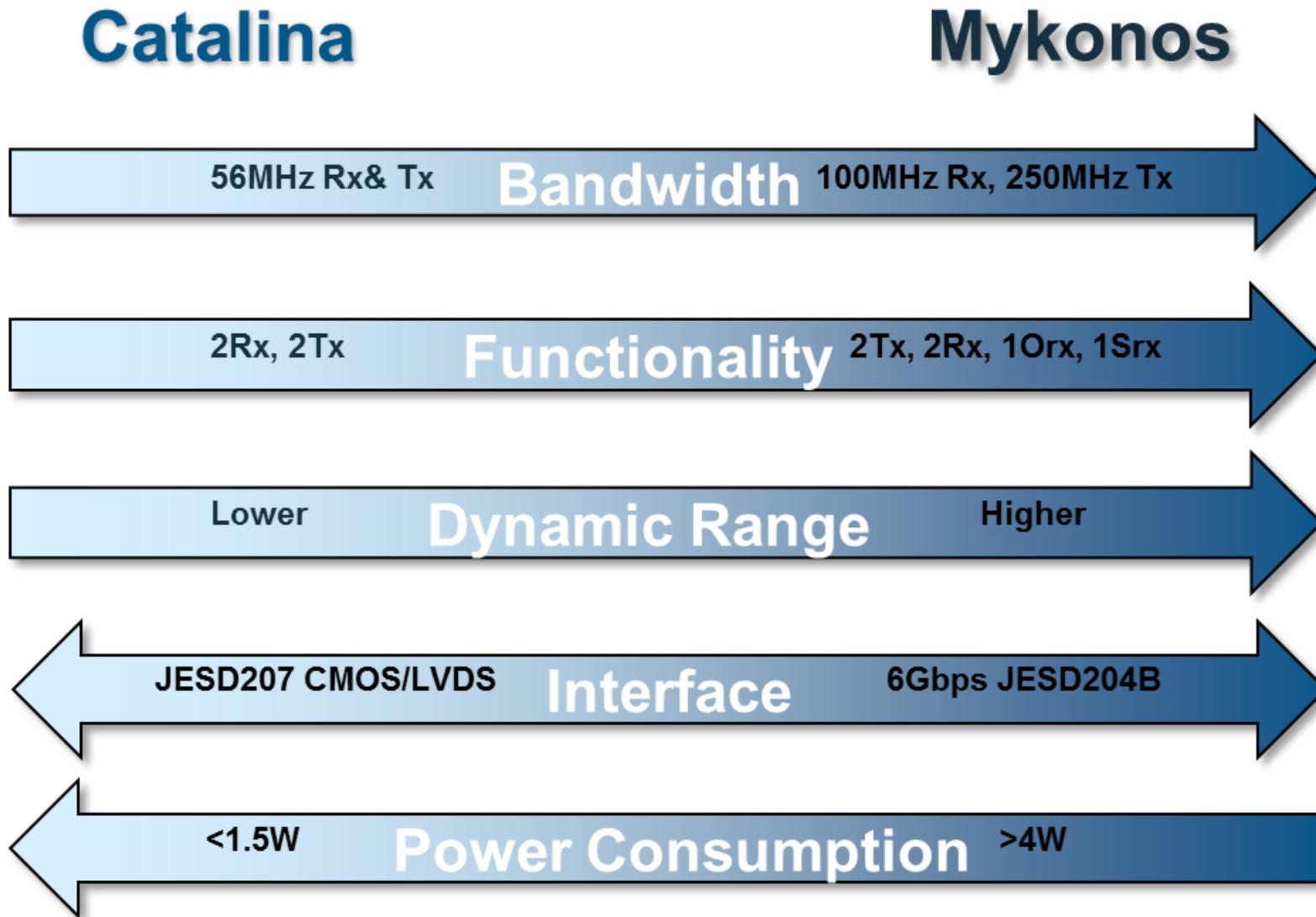
- Typical power: 800-1100 mW
  - 2Rx & 2Tx, 20 MHz BW, 0 dBm Tx power



Temp
-40°C – +85°C

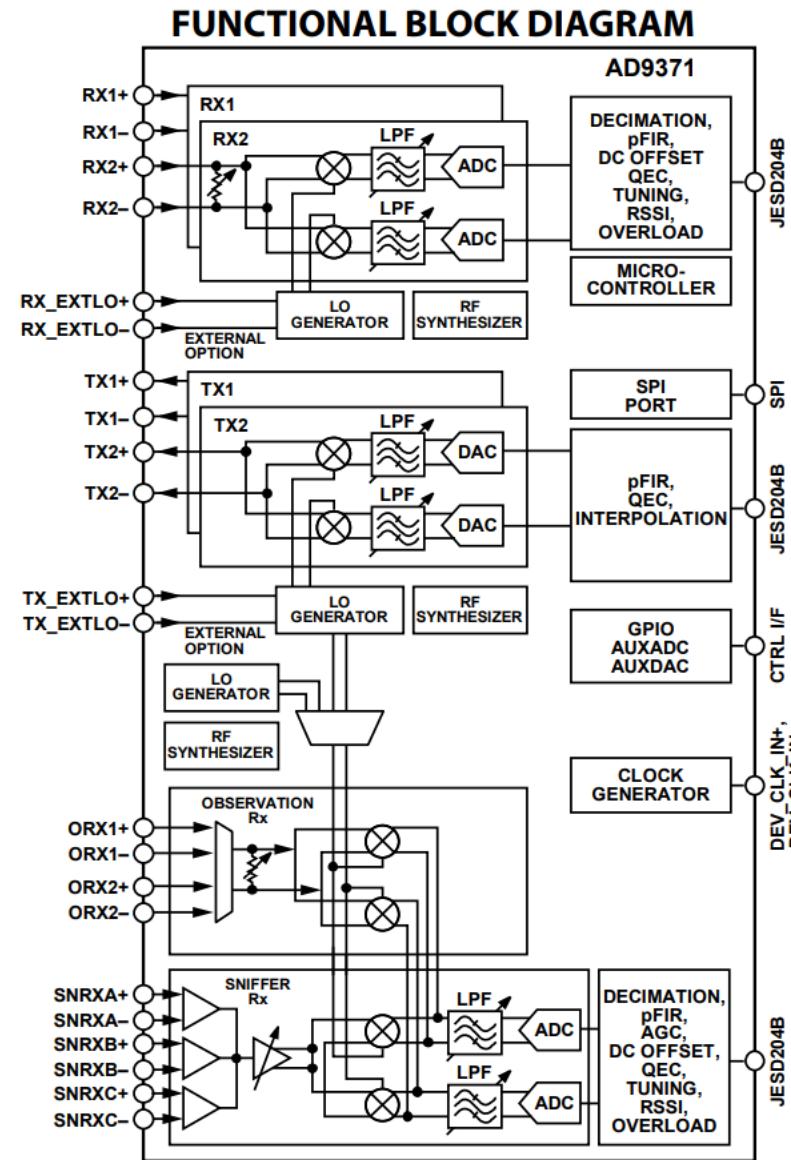
Package
144- CSP_BGA (10x10mm) Pb-Free

# AD9361 (Catalina) vs AD9371 (Mykonos)



# AD9371 Integrated, Dual RF Transceiver With Observation Path (Mykonos)

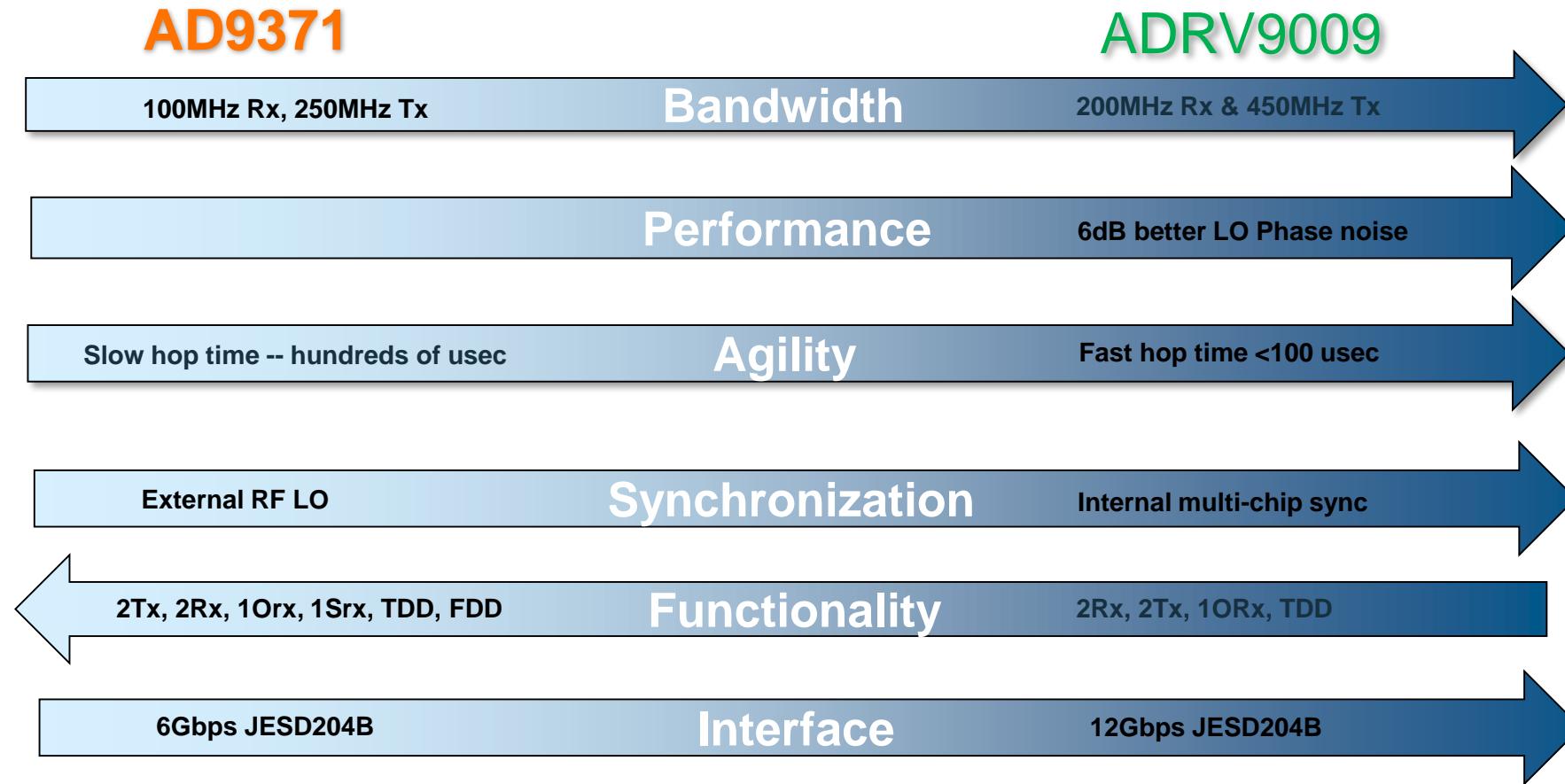
- Integrated dual-traffic Rx and Tx
  - Tuning range:  $300\text{MHz} < F_c < 6\text{GHz}$
  - FDD/TDD operation
- Receiver
  - Max Rx BW = 100MHz
  - NF: 12dB
  - IIP<sub>3</sub>: 22dBm
  - IIP<sub>2</sub>: 65dBm
  - Gain range/step (dB): 30/0.5
- Transmitter
  - Max Tx BW = 250MHz
  - 64dB ACLR (4 UMTS Carriers)
  - OIP3: 27dBm (5dB atten)
  - Gain range/step (dB): 42/0.05
- Integrated observation and sniffer Rx
  - Max ORx BW = 250MHz
    - 2 inputs
  - Max SRx BW = 20MHz
    - Contains LNA
    - Dedicated LO
    - 3 inputs
- Total power (@ max bandwidth)
  - 2x Rx = 2.7W
  - 2x Tx = 3.7W
  - 2x Rx, 2x Tx, ORx = 4.86W
- Digital features
  - Tx/Rx QEC, DC offset, LO leakage
  - 6GSPS JESD204-B interface



Package  
196- CSP\_BGA  
(12x12mm) Pb-Free



# AD9371 vs ADRV9009

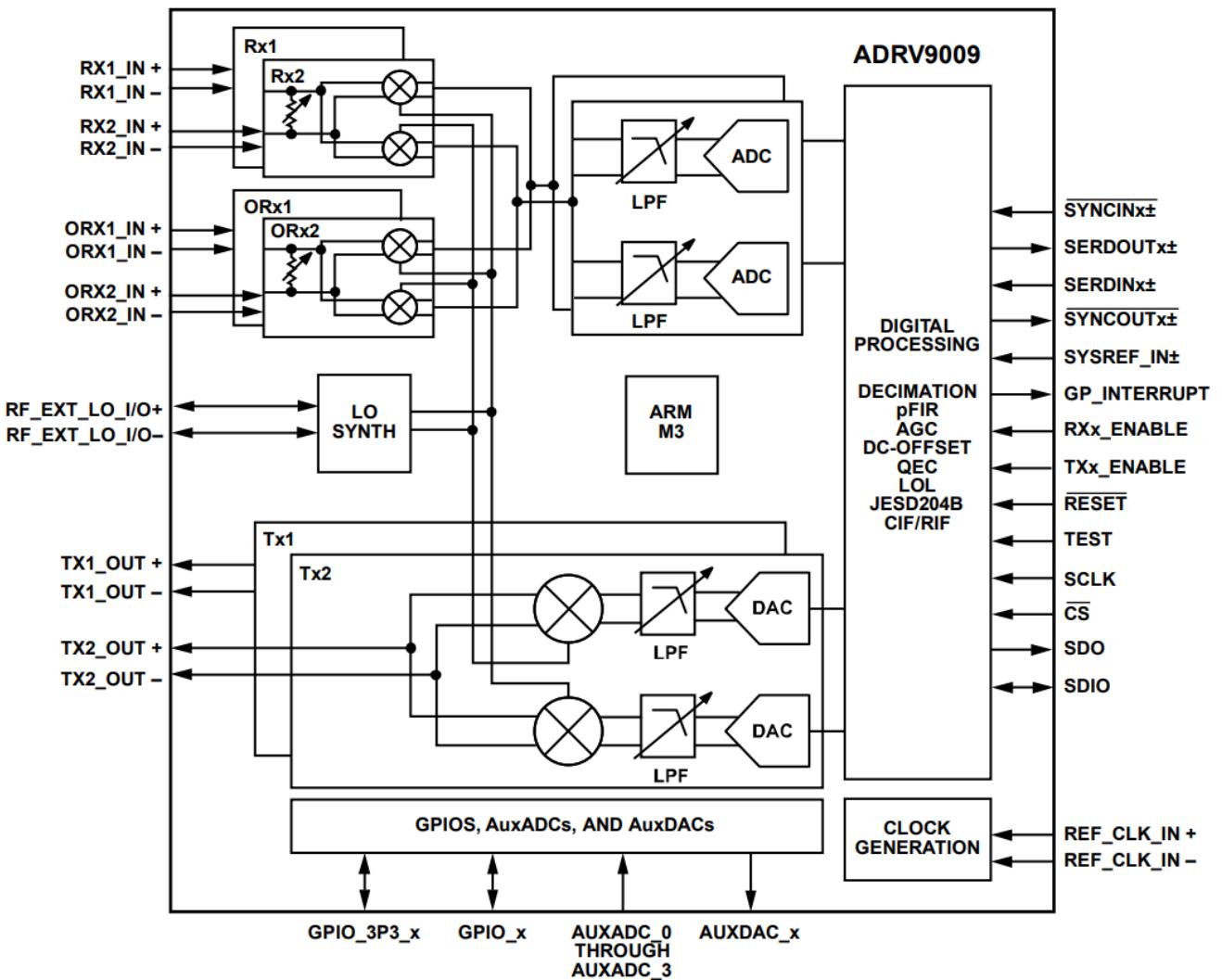


- Widest bandwidth, highest performance integrated radio solution from 75MHz to 6GHz
- Common platform design for 2G/3G/4G/5G base stations
- Supports multi-chip LO phase synchronization
- Enhanced frequency agility with fast frequency hopping and precalibration profiles

# ADRV9009 Functionality & Block Diagram

- **TDD operation**
  - **Bandwidth:** 200 MHz receiver,  
450 MHz transmitter and observation receiver
  - **Integration:** dual transmitters, dual receivers and  
observation receivers with shared input
  - **Tuning Range:** 75MHz to 6GHz
  - **Interface:** 12 Gbps JESD204B
  - **Power Consumption:** 4.6W\*
  - **Multi-chip LO phase synchronization**
  - **Package:** 12x12 BGA

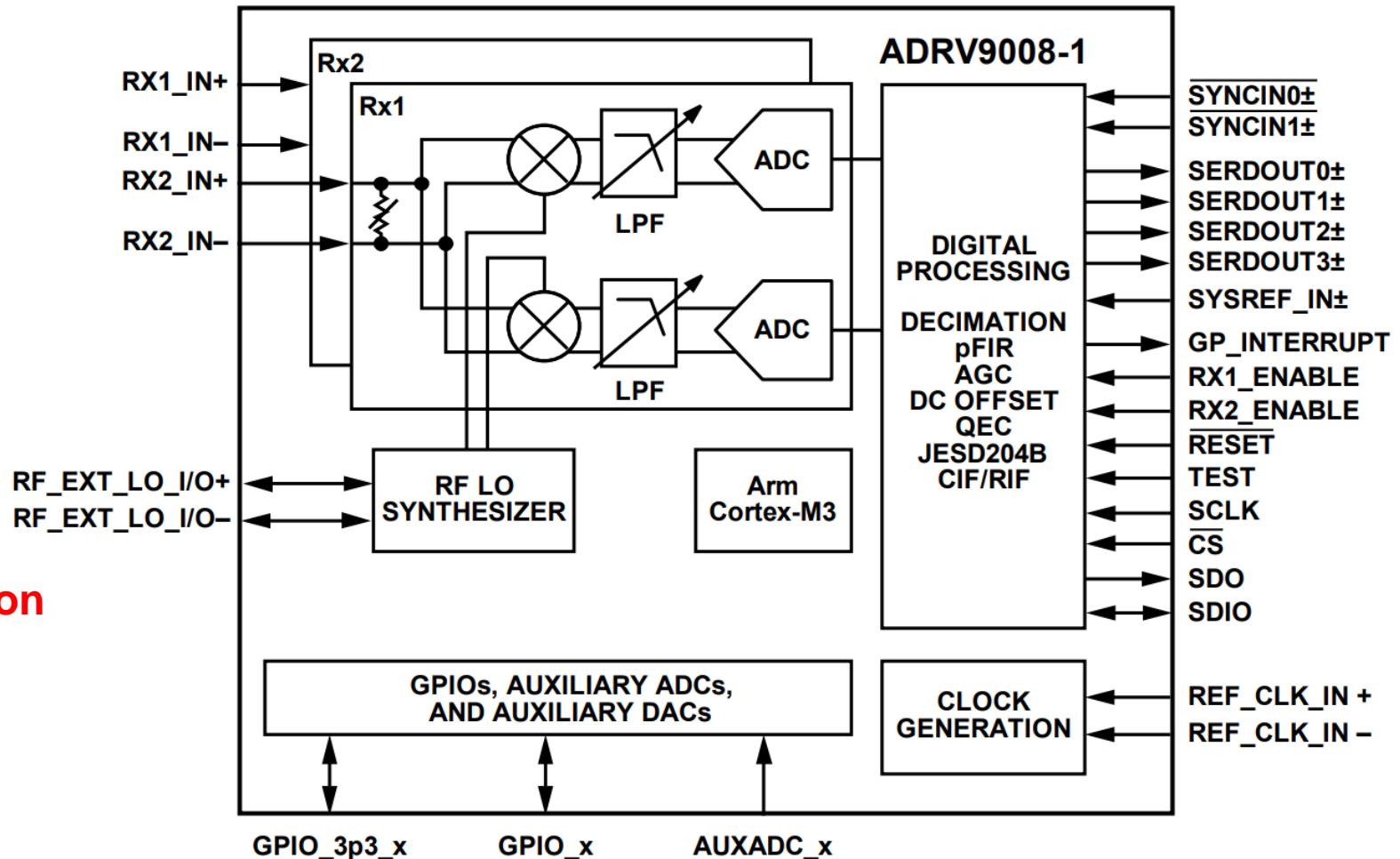
\*For 50% Rx/Tx Duty Cycle, Orx on, 200MHz/450MHz BW, 0dB attenuation



# ADRV9008-1 Functionality & Block Diagram

- **FDD Rx operation**
- **Bandwidth:** 200 MHz receiver
- **Integration:** dual receivers
- **Tuning Range:** 75MHz to 6GHz
- **Interface:** 12 Gbps JESD204B
- **Power Consumption:** 2.48W\*
- **Multi-chip LO phase synchronization**
- **Package:** 12x12 BGA
- Pin compatible with ADRV9009

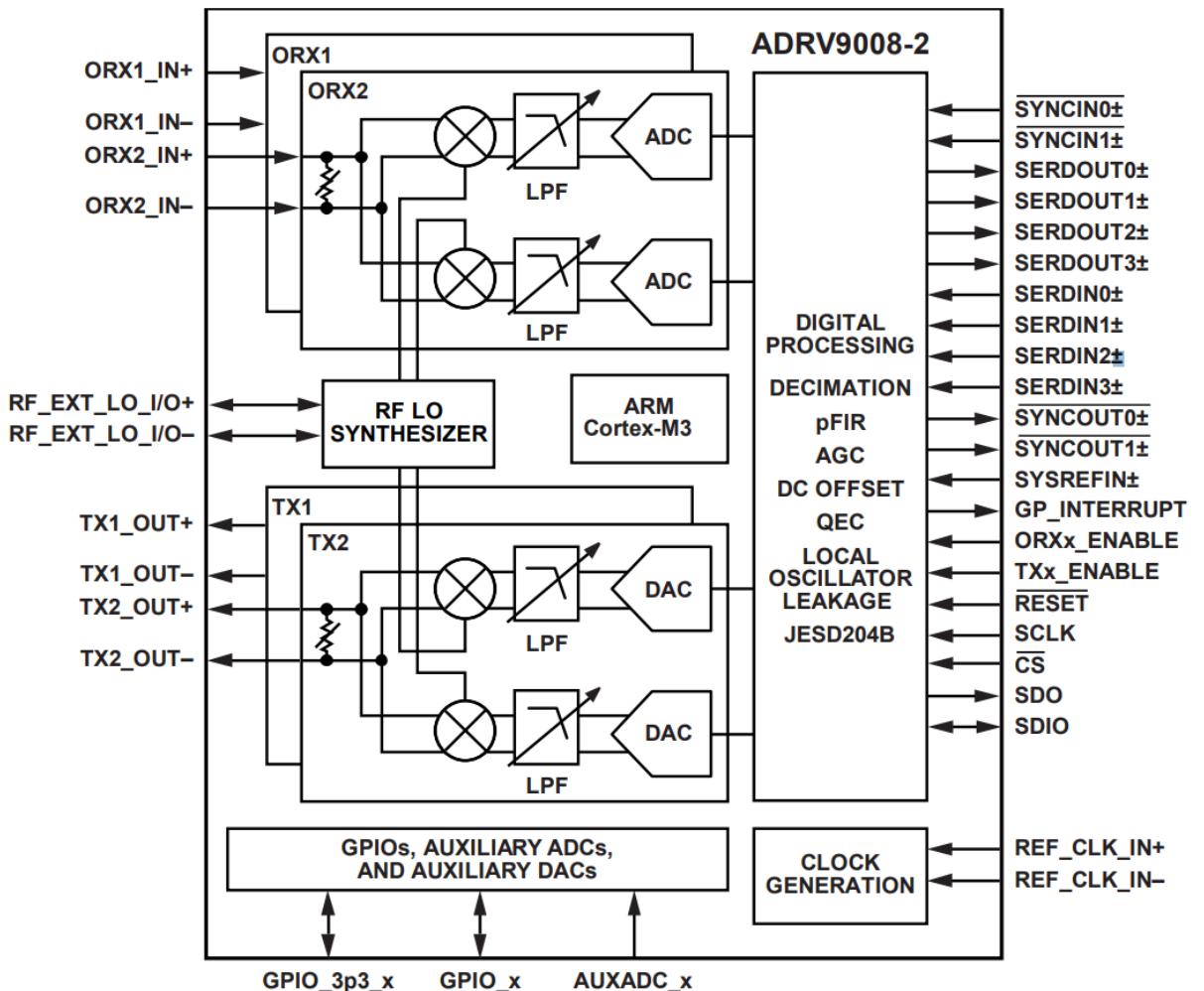
\*For 2Rx, 200MHz BW



# ADRV9008-2 Functionality & Block Diagram

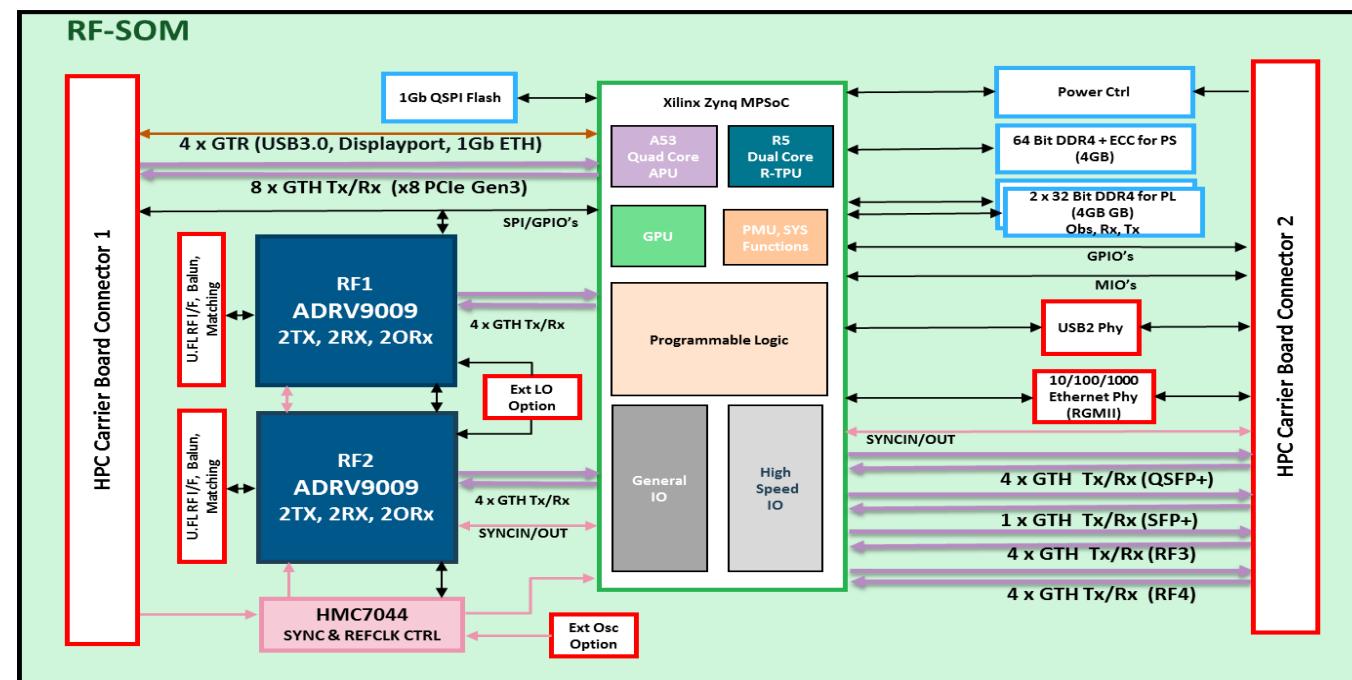
- **FDD Tx/Orx operation**
- **Bandwidth:** 450 MHz transmitter and observation receiver
- **Integration:** dual transmitters, observation receiver with dual inputs
- **Tuning Range:** 75MHz to 6GHz
- **Interface:** 12 Gbps JESD204B
- **Power Consumption:** 4.34W Tx, 1.25W Orx \*
- **Multi-chip LO phase synchronization**
- **Package:** 12x12 BGA
- Pin compatible with ADRV9009

\*For 450MHz BW, 0dB attenuation

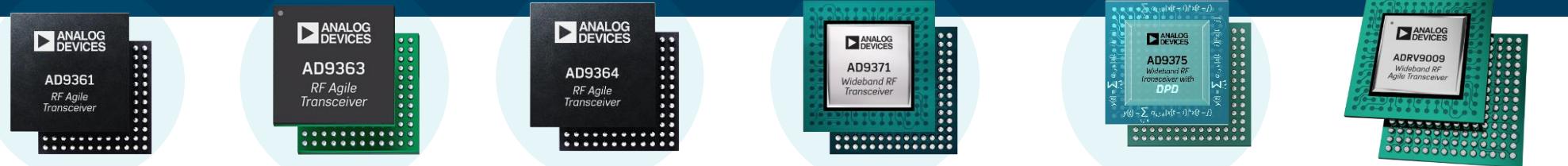


# New ADRV9009 System-on-Module (RF-SOM)

- ▶ Supports up to 4x ADRV9009 that can be synced in Freq & Phase
- ▶ Scalable with multiple RF-SOM's synced together
- ▶ I/O connector: USB 3.0, 10Gb Ethernet, PCIe x8
- ▶ Approx. size: 96mm x 160mm
- ▶ Comes with open source code support package hosted on GitHub
- ▶ Qualified 'production ready' module to speed up prototyping and integration into final production.
- ▶ Allows customers to focus on their own areas of differentiation
- ▶ Broad range of applications in cellular infrastructure, radar, portable defence and instrumentation



# Wideband RF Transceiver Portfolio Released on RadioVerse™



Part # (Family)	Applications	Bandwidth	Functionality	RF Tuning Range	Rx Image Rejection*	Rx NF/IIP3**	Tx OIP3*	EVM	Package Size	Data Interface	Price
AD9361 (Catalina)	3G/4G Picocell, SDR, Pt-Pt, Satcom, IoT Aggregator	56 MHz	2 Rx, 2 Tx	70 MHz to 6 GHz	50B	3dB/-14dBm	+19dBm	-40 dB	10 mm x 10 mm	CMOS/LVDS	\$175
AD9364 (Catalina)	3G/4G Picocell, SDR	56 MHz	1 Rx, 1 Tx	70 MHz to 6 GHz	50dB	3dB/-14dBm	+19dBm	-40 dB	10 mm x 10 mm	CMOS/LVDS	\$130
AD9363 (Catalina)	3G/4G Femtocell, UAV, Wireless Surveillance	20 MHz	2 Rx, 2 Tx	325 MHz to 3.8 GHz	50dB	3dB/-14dBm	+19dBm	-34 dB	10 mm x 10 mm	CMOS/LVDS	\$80
AD9371 (Mykonos)	3G/4G Macro BTS, Massive MIMO, SDR	100MHz Rx, 250MHz Tx	2Tx, 2Rx Orx & SnRx	300 MHz to 6GHz	75dB	1.6dB/+2dBm	+27dBm	-40 dB	12 mm x 12 mm	6GHz JESD204B	\$245
AD9375 (Mykonos)	3G/4G Small Cell, 3G/4G Massive MIMO PreDistortion (DPD)	100MHz Rx, 250MHz Tx	2Tx, 2Rx Orx & SnRx	300 MHz to 6GHz	75dB	1.6dB/+2dBm	+27dBm	-40 dB	12 mm x 12 mm	6GHz JESD204B	\$325
ADRV9009 (Talise)	3G/4G/5G <b>TDD</b> macro cell, Massive MIMO, Phased array radar	200MHz Rx, 450MHz Tx	2Tx, 2Rx Orx	75 MHz to 6GHz	75dB	1.6dB/+2dBm	+27dBm	-43 dB	12 mm x 12 mm	12GHz JESD204B	\$319
ADRV9008-1 (Talise)	3G/4G/5G <b>FDD</b> macro cell, Massive MIMO, Phased array radar	200MHz Rx	2Rx	75 MHz to 6GHz	75dB	1.6dB/+2dBm	--	--	12 mm x 12 mm	12GHz JESD204B	\$210
ADRV9008-2 (Talise)	3G/4G/5G <b>FDD</b> macro cell, Massive MIMO, Phased array radar	450MHz Tx	2Tx, Orx	75 MHz to 6GHz	--	--	+27dBm	-43 dB	12 mm x 12 mm	12GHz JESD204B	\$239

\* typical performance @ 2.6GHz

\*\* AD9371 cascaded analysis with external LNA NF = 1.1dB, Gain = 19.5dB, IIP3 = 33dB (HMC8175A broadband LNA). Typical Performance @ 2.6GHz

\*\* AD9361 assumes internal LNA, typical performance @ 2.6GHz

# ADI's Hardware Prototyping Environment

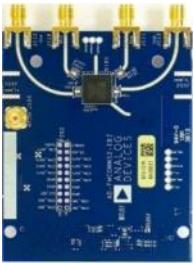
## ADALM-PLUTO

- AD9363
- 1 x Rx, 1 x Tx
- 325 MHz – 3.8GHz
- 200kHz – 20 MHz channel bandwidth



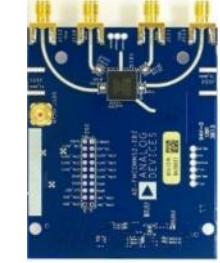
## AD-FMCOMMS2

- AD9361
- 2 x Rx, 2 x Tx
- *tuning range*
  - 2.2 GHz – 2.6GHz
  - 70 MHz – 6GHz
- 200kHz – 56 MHz channel bandwidth



## AD-FMCOMMS3

- AD9361
- 2 x Rx, 2 x Tx
- *tuning range*
  - 2.2 GHz – 2.6GHz
  - 70 MHz – 6GHz
- 200kHz – 56 MHz channel bandwidth



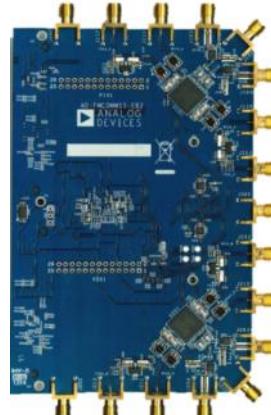
## AD-FMCOMMS4

- *AD9364*
- 1 x Rx, 1 x Tx
- 70 MHz – 6GHz tuning range
- 200kHz - 56 MHz channel bandwidth
- Shipping Now!



## ARRADIO

- AD9361
- HSMC, not FMC
- 2 x Rx, 2 x Tx
- *2.2 GHz – 2.6GHz tuning range*
- 200kHz - 56 MHz channel bandwidth
- Shipping Now!



## AD-FMCOMMS5

- 2 x *AD9361*
- 4 x Rx, 4 x Tx
- *Synchronized RF tuning range*
- 70 MHz – 6GHz tuning range
- 200kHz - 56 MHz channel bandwidth
- Shipping Now!



## ADRV9371-N/PCBZ ADRV9371-W/PCBZ

- *AD9371*
- 2 x Rx, 2 x Tx, 2 x Obs, 1x Sniffer
- tuning range
  - 1.8GHz – 2.6GHz
  - 300MHz – 6GHz
- Tx synthesis bandwidth 250 MHz
- Rx BW: 8 MHz to 100 MHz



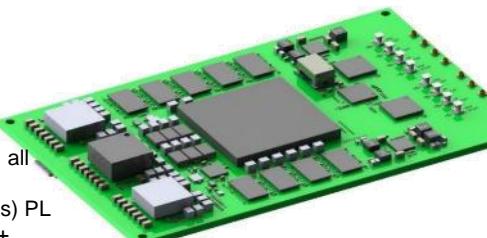
## ADRV9375-N/PCBZ ADRV9375-W/PCBZ

- *AD9375*
- 2 x Rx, 2 x Tx, 2 x Obs, 1x Sniffer
- tuning range
  - 1.8GHz – 2.6GHz
  - 300MHz – 6GHz
- *DPD actuator and adaptation engine for PA linearization*



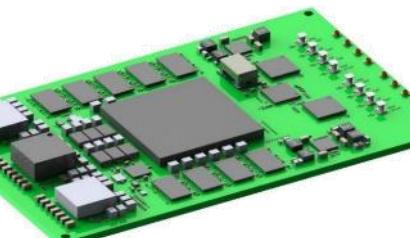
## ADRV9008-1W/PCBZ (Rx) ADRV9008-2W/PCBZ (Tx/Obs)

- *ADRV9008-1, ADRV9008-2, ADRV9009*
- 2 x Rx, 2 x Tx, 2 x Obs, 1x Sniffer
- 75MHz – 6GHz tuning range
- Tx synthesis bandwidth 450 MHz
- Rx BW to 200 MHz



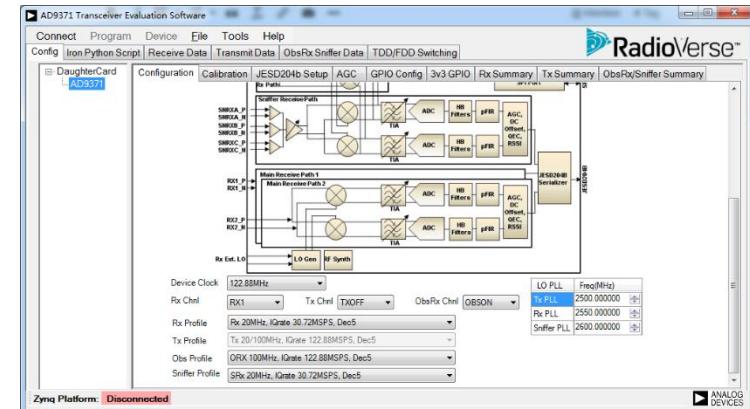
## ADRV9009-ZU11EG

- 2 x *ADRV9009 + Zynq Ultrascale*
- 75MHz to 6GHz tuning range
- Rx BW 200MHz
- Tx synthesis bandwidth 450 MHz
- Integrated LO and Phase synch between all channels and Modules
- 4G x64 w/ECC PS; 4G (2Gb x32 x2Banks) PL
- USB3, USB2, PCIe 3.0 x8, QSFP+, SFP+, 1Gb Ethernet x2, and CPRI



# ADI's Software Prototyping Environment: 4 Main Tools

- IIO Oscilloscope
  - Built on the IIOLIB Linux Drivers
  - Data Visualization Application
  - Graphical Configuration Application
- TES GUI
  - For the AD937x and ADRV9008/9 products
  - Evaluation and Python Scripting
- GNU Radio
  - Free Linux Based Graphical Communications Toolbox
  - Great intro to concepts and algorithm development
  - Pluto and AD936x products supported, not AD937x or ADRV9008/9
  - But for prototype and production, better to move to Matlab
- Matlab / Simulink
  - All ADI Transceivers Supported in Matlab
  - Evaluation → Verification → Detailed Design → Prototype
  - See Next Slide for Seminar Details

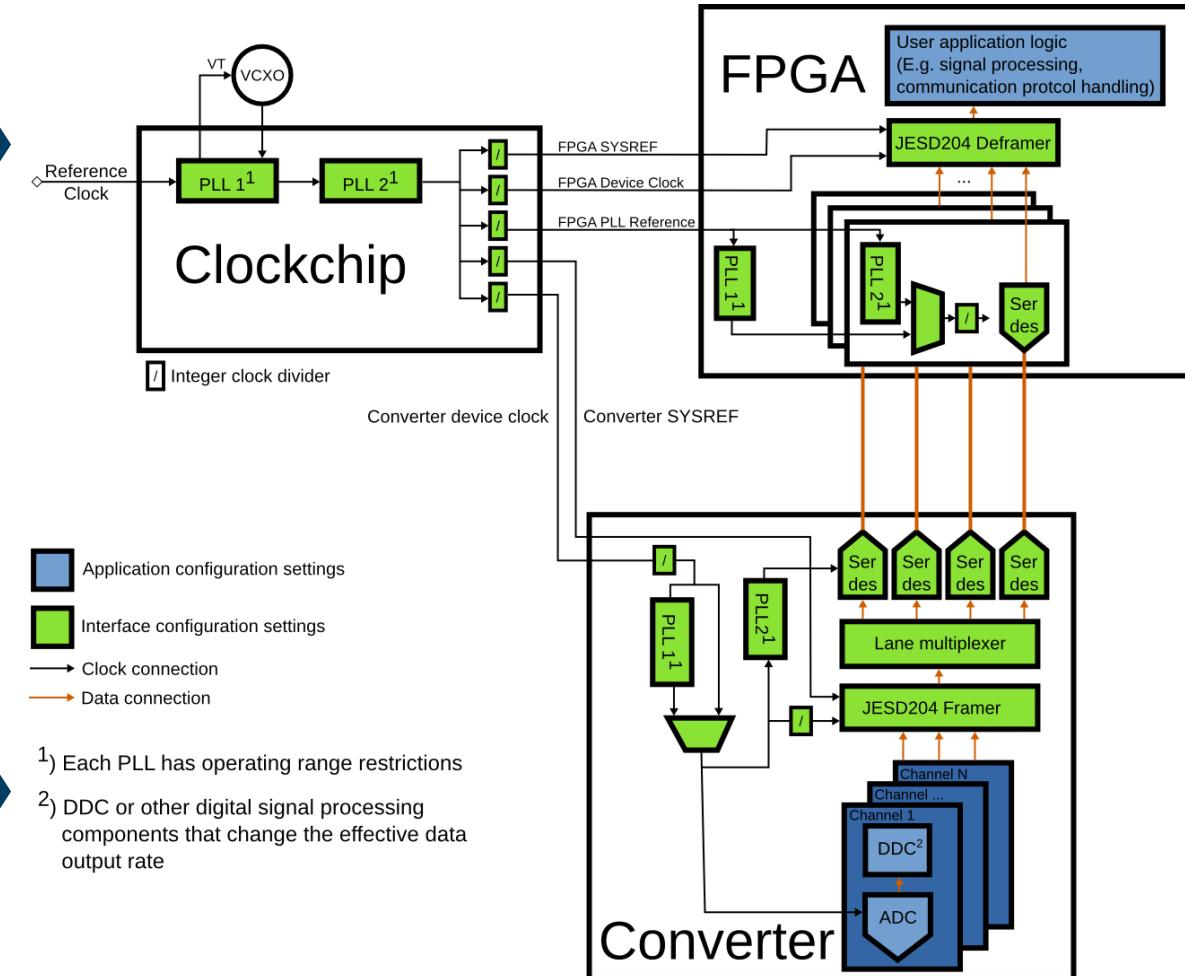


# ADI provides complete JESD204B integration solution

## JESD204B Interface Framework

- Open-source HDL and software drivers (Linux & No-OS) for ADI CVT, TRX, CLK solutions
- Support Xilinx and Altera FPGAs
- \$5000 for commercial license and one-on-one support

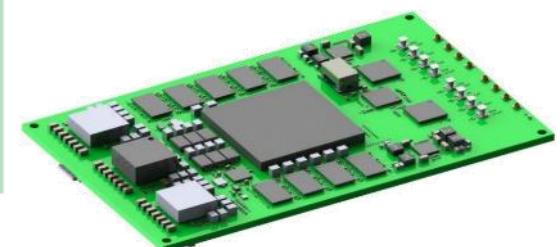
Includes interoperability report with Altera FPGA and Xilinx FPGA



# Talise Evaluation and Prototyping Options

The table below outlines the full set of software and hardware tools available from ADI for evaluation, prototyping, and reference design.

	FMC Mezzanine Cards	Carrier Boards	Software and Driver	
Evaluation System	<ul style="list-style-type: none"> <li>▶ ADRV9009-W/PCBZ</li> <li>▶ ADRV9008-1W/PCBZ</li> <li>▶ ADRV9008-2W/PCBZ</li> </ul>	<ul style="list-style-type: none"> <li>▶ EVAL-TPG-ZYNQ3</li> </ul>	<ul style="list-style-type: none"> <li>▶ Operating system-agnostic API source in ANSI C</li> <li>▶ Windows GUI for transceiver configuration and data capture</li> </ul>	<ul style="list-style-type: none"> <li>▶ Binary/image provided, uses Xilinx® JESD204B IP</li> </ul>
Prototyping Platform	<ul style="list-style-type: none"> <li>▶ ADRV9009-W/PCBZ</li> <li>▶ ADRV9008-1W/PCBZ</li> <li>▶ ADRV9008-2W/PCBZ</li> </ul>	<ul style="list-style-type: none"> <li>▶ Xilinx Zynq UltraScale+ MPSoC ZCU102 evaluation kit</li> <li>▶ Intel® Arria® 10 SoC development kit</li> </ul>	<ul style="list-style-type: none"> <li>▶ Open-source Linux® driver</li> <li>▶ Open-source Linux IIO scope for data capture</li> <li>▶ Compatible with MATLAB® and Simulink®</li> </ul>	<ul style="list-style-type: none"> <li>▶ Compatible with GNU radio</li> <li>▶ Publicly available reference design on GitHub, uses ADI JESD204B interface framework</li> </ul>
System on Module (Available 2018 Q4)	<ul style="list-style-type: none"> <li>▶ ADRV9009-ZU11EG</li> </ul>		<ul style="list-style-type: none"> <li>▶ Dual ADRV9009 connected to a Zynq UltraScale+ MPSoC</li> <li>▶ Quad-core ARM® Cortex®-A53 MPCore™</li> <li>▶ 4 synchronized transmit channels</li> </ul>	<ul style="list-style-type: none"> <li>▶ 4 synchronized receive channels</li> <li>▶ USB 3 and PCIe back to host PC</li> <li>▶ 653k system logic cells and 2928 DSP slices for custom IP development</li> </ul>





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## ADRV9009 Operation Details and Evaluation Results

# ADRV9009 Operation Details and Evaluation Results

- ▶ ADRV9009 Evaluation Software and Unboxing
- ▶ ADRV9009 Tx Details:
  - QEC Correction
  - DC Offset Calibration
  - Demo of effect of enabling the calibrations
- ▶ ADRV9009 Rx Details
  - Calibration
  - Demo of monitoring calibrations
  - Automatic Gain Control
  - AGC Demo
- ▶ ADRV9009 LO Generation
  - Phase Synchronization
- ▶ ADRV9009 Configuration Tool
- ▶ ADRV9009 JESD204 Details
- ▶ ADRV9009 API Details

# ADRV9009 Evaluation Setup

# ADRV9009 Software

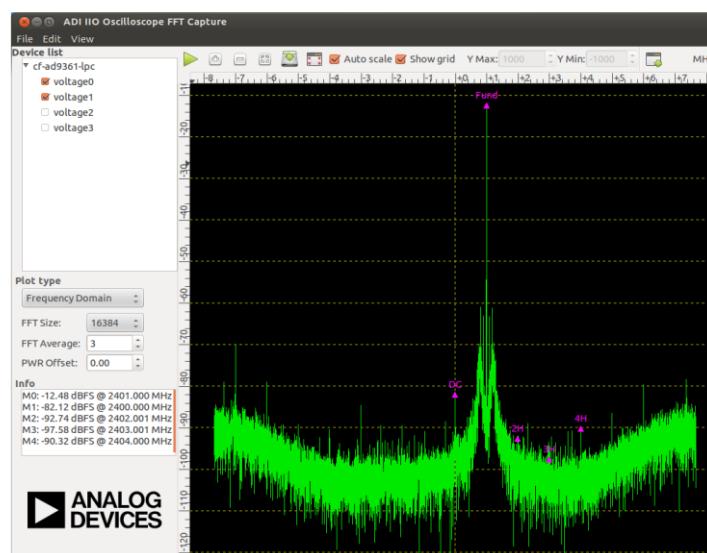
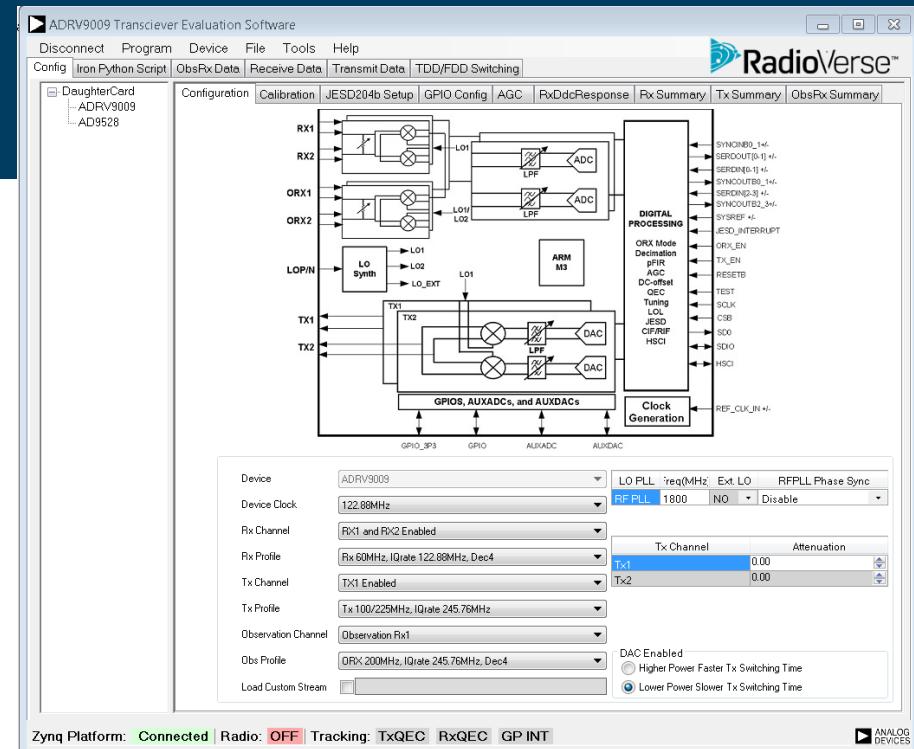
- There are two Software options

- One is the “**Evaluation Software**”

- Command/control and data capture via Windows GUI
    - Runs API
    - Automated testing via any .net enabled application such as C#, MATLAB, etc.
    - Works with ZC706 (JESD204 lane rate restrictions) or ZYNQ3 (max JESD lanes) FPGA
  - OS- and platform-agnostic API source
    - Integrate into customer system
    - Used to characterize IC performance

- The other is the “**Prototyping Software**”

- Works with various Xilinx and Altera motherboards
    - Only ZCU102 FPGA works with supplied SD card
  - FPGA source on GitHub, verified with Xilinx and Altera JESD204B cores
  - Open-source GUI, Windows, Linux, OS-X
  - Open-source Linux IIO driver
  - Streams data to GNU Radio, MATLAB, Simulink
  - <https://wiki.analog.com/resources/eval/user-guides/adrv9009>



# FMC Evaluation Board

**“Wideband”** supports the entire 100 MHz to 6 GHz LO range

- Wide range Balun has higher loss, especially at frequency extremes
- Won’t meet all data sheet specs such as NF, sensitivity, or power output
- Allows for functional verification or software development at any supported LO frequency
- ADRV9009-W/PCBZ
- Comes with 2 SD cards: one for Windows based TES (evaluation software), one for Linux IIO Oscilloscope (prototyping software)
- Download the Design Package here:
  - [https://form.analog.com/Form\\_Pages/Catalina/CatalinaDesign.aspx?prodid=ADRV9009](https://form.analog.com/Form_Pages/Catalina/CatalinaDesign.aspx?prodid=ADRV9009)
  - Please read the user guide! It is 250 pages, but it is really really really helpful!



# ADRV9009 Evaluation Software: “TES”

- ▶ Download and Install ADRV9009 Transceiver Evaluation Software
  - <https://www.analog.com/en/products/adrv9009.html#product-evaluationkit>
  - Install IronPython and .NET tools from the installer options



The image shows the ADRV9009-W/PCBZ evaluation kit, which is a blue printed circuit board (PCB) with various electronic components, connectors, and RF ports.

**EVAL-ADRV9008/9**

[View Detailed Evaluation Kit Information](#)

The ADRV9009-W/PCBZ is a radio card designed to showcase the ADRV9009, the widest bandwidth, highest performance RF integrated transceiver. The radio card provides a single 2x2 transceiver platform for device evaluation and rapid prototyping of radio solutions. All peripherals necessary for the radio card to operate including a high efficiency switcher only power supply solution, and a high performance clocking solution are populated on the board. The ADRV9009-W/PCBZ is a single-chip TDD solution of dual receivers, dual transmitters with observation receiver.

The ADRV9009-W/PCBZ operates over a wide tuning range 75MHz – 6GHz,

**Features & Benefits**

- Complete Radio Card for evaluation
  - ADRV9009-W/PCBZ: Evaluation kit for ADRV9009 (Dual RF Rx/Tx/Otx Evaluation Board)
  - ADRV9008-1W/PCBZ: Evaluation kit for ADRV9008-1 (Dual RF Rx Evaluation Board)
  - ADRV9008-2W/PCBZ: Evaluation kit for ADRV9008-2 (Dual RF Tx/Otx Evaluation Board)
- Wide band RF operation over 75MHz - 6GHz frequency range
- Complete with high efficiency power supply solution and clocking solution
- FMC connector to Xilinx motherboard ([EVAL-TPG-ZYNQ3](#))
- Powered from single FMC connector
- Includes schematics, layout, BOM, HDL, drivers and application software

**Resources**

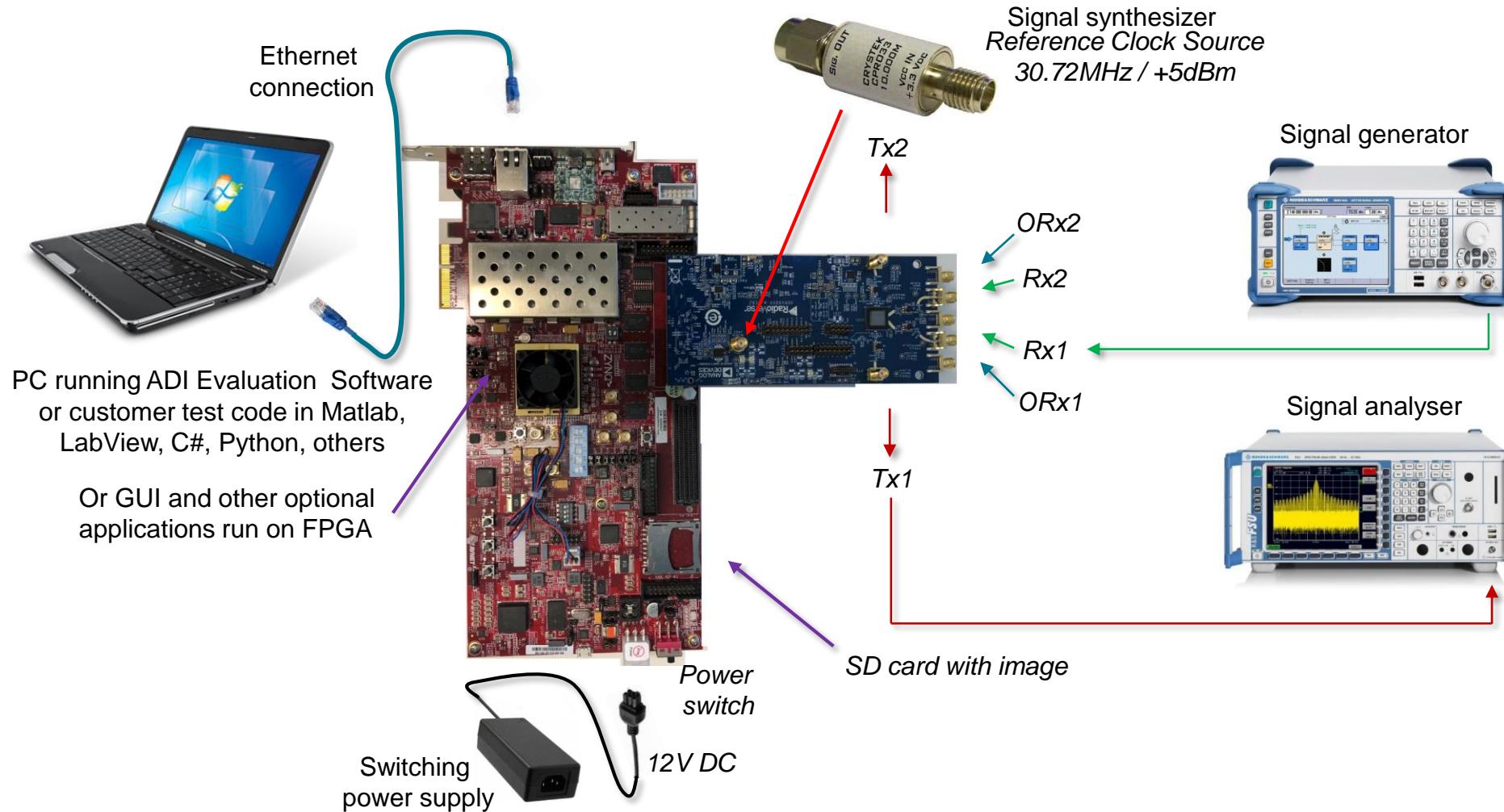
-  [ADRV9009 Prototyping Platform User Guide](#)
-  [SDR Integrated Transceiver Design Resources](#)

**Software**

-  [Wideband RF Transceiver Evaluation Software](#)
-  [JESD204 Interface Framework](#)

A thick red arrow points from the bottom right towards the 'Software' section of the product page, highlighting the download links for the evaluation software.

# ADRV9009 Eval Hardware Setup



# Reference Clock Source Options

- The ADRV900x boards need a reference clock.
  - 30.72 MHz is the default value, but this could be changed (i.e. 61.44MHz) if required.
- A signal source works great, of course.
- But an easier solution is the Crystek CPR033-30.72 SMA oscillator.
- These are not expensive, but they are hard to find, so here's the part's list for that option:

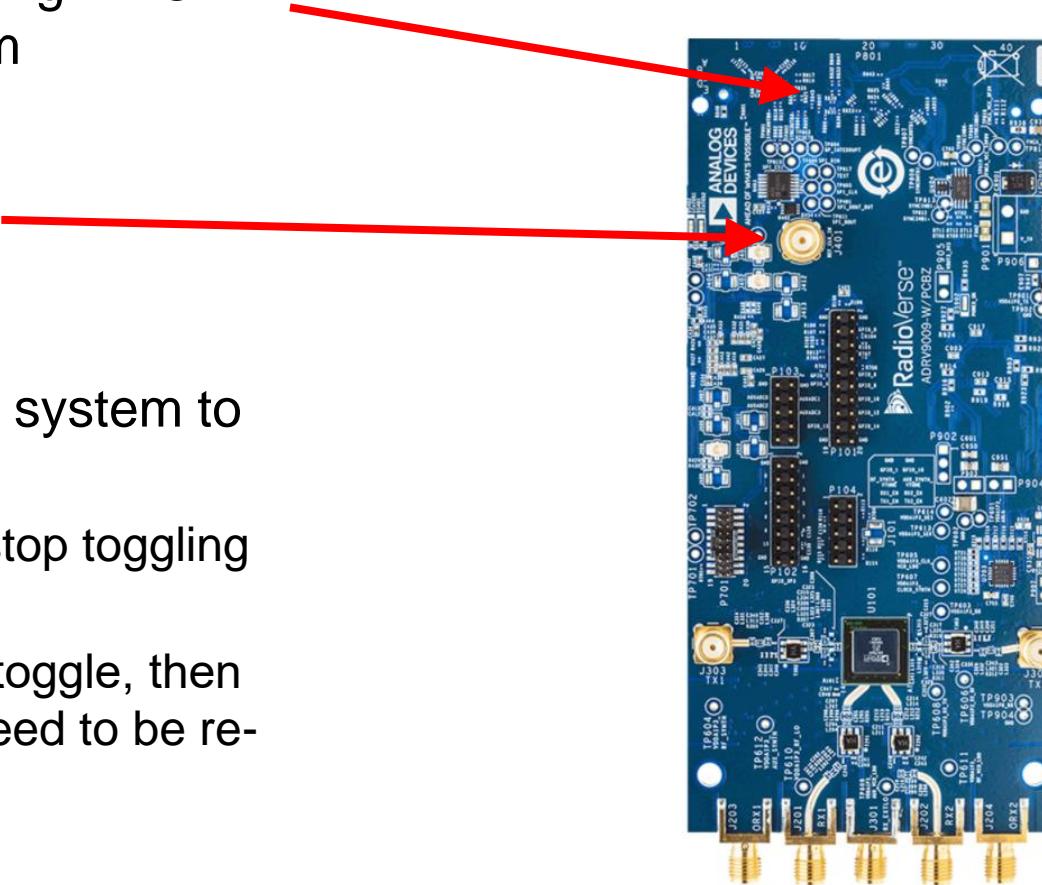
SMA 30.72 MHz clock source for the AD9371 and ADRV9008/9 boards:

Oscillator	CPR033-30.72	<a href="https://www.digikey.com/products/en?keywords=CPR033-30.72">https://www.digikey.com/products/en?keywords=CPR033-30.72</a>
SMA to barrel adapter		<a href="https://www.digikey.com/products/en?keywords=CCADP-MM-6">https://www.digikey.com/products/en?keywords=CCADP-MM-6</a>
3.3V power wall wart	2.1/5.5mm barrel	<a href="https://www.digikey.com/product-detail/en/kaga-electronics-usa/KTPS05-03315U-VI-P1/62-1234-ND/5820199">https://www.digikey.com/product-detail/en/kaga-electronics-usa/KTPS05-03315U-VI-P1/62-1234-ND/5820199</a>



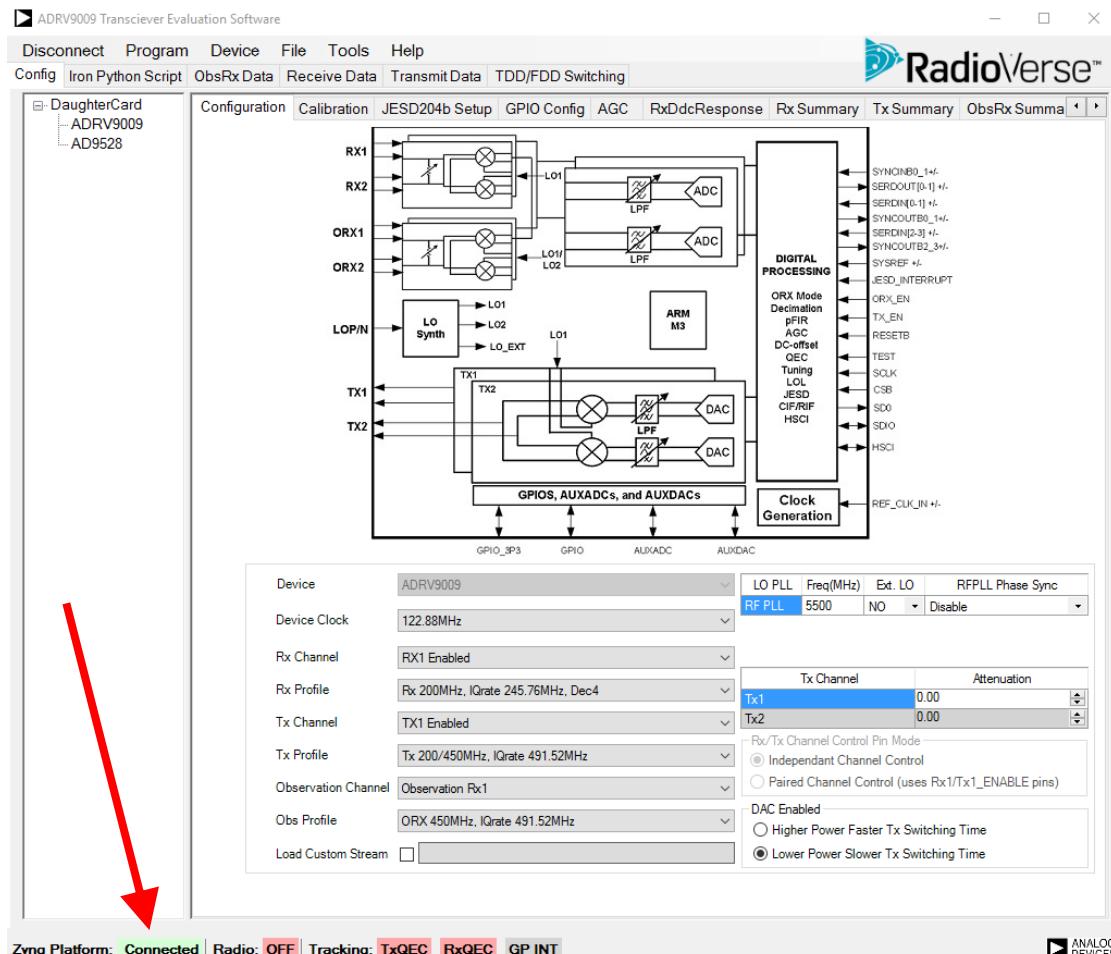
# ADRV9009 Hardware Setup

- ▶ Connect ADRV9009 evaluation board using FMC connector J37 on ZC706/ZYNQ3 platform
- ▶ Connect clock source to J401
- ▶ Flip SW1 on ZC706 platform and wait for system to boot
  - Finished when 4 LEDs near power switch stop toggling ON/OFF
  - If these LEDs don't stop toggling, or never toggle, then there is an issue with the SD card. It will need to be re-imaged.



# ADRV9009 TES

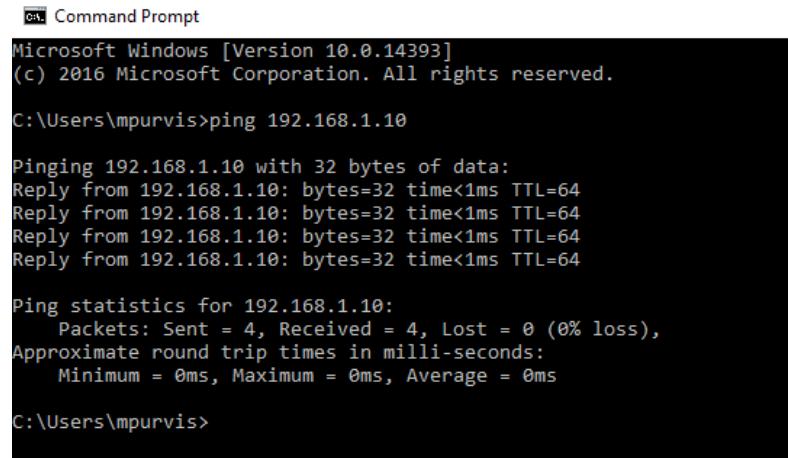
- Launch application
- Click ‘Connect’ to make TCPIP connection to ZC706 platform



# ADRV9009 TES Connection Troubleshooting

## ► Common Connection Issues

- Ethernet connection
  - ping 192.168.1.10 from command line and verify response
- Verify command server is running on FPGA
  - Connect to FPGA platform via SSH using terminal application like PuTTY or TeraTerm
    - Username: root Password: analog
  - Run ps -e | grep cmd\_server to show cmd\_server process



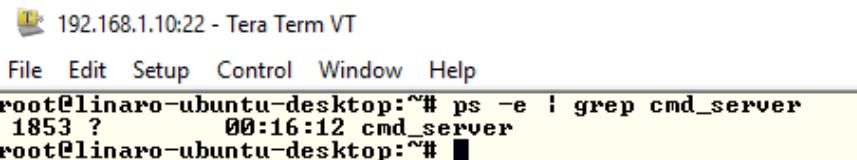
```
Microsoft Windows [Version 10.0.14393]
(c) 2016 Microsoft Corporation. All rights reserved.

C:\Users\mpurvis>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:
Reply from 192.168.1.10: bytes=32 time<1ms TTL=64

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip times in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0ms

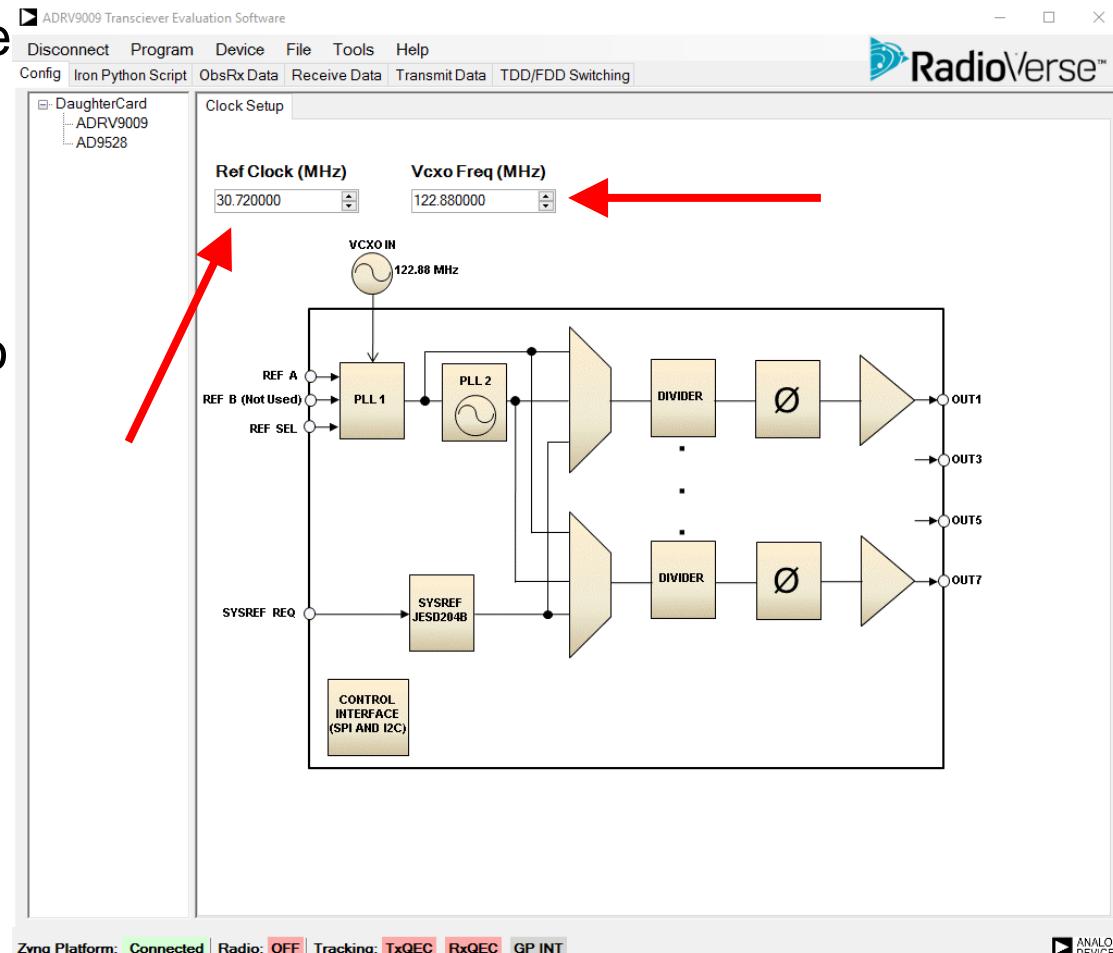
C:\Users\mpurvis>
```



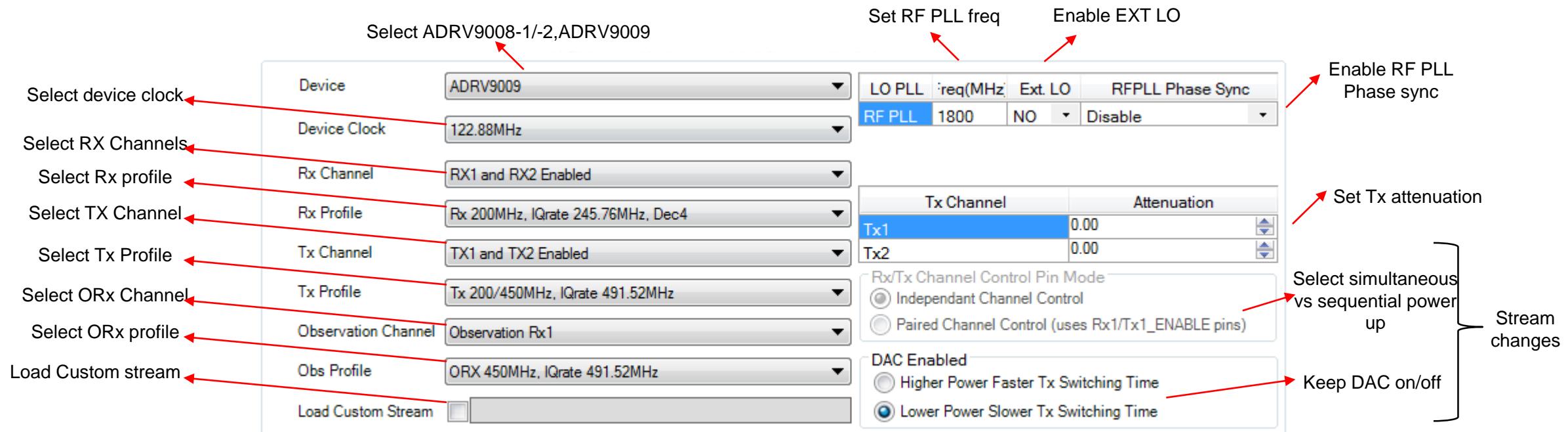
```
192.168.1.10:22 - Tera Term VT
File Edit Setup Control Window Help
root@linaro-ubuntu-desktop:~# ps -e | grep cmd_server
1853 ?        00:16:12 cmd_server
root@linaro-ubuntu-desktop:~#
```

# AD9528 Configuration

- Ref Clock field should match clock source we supply at J401
  - 30.72Mhz in this exercise
- VCXO frequency should be 122.88Mhz to match VCXO source on evaluation board
  - CVHD-950



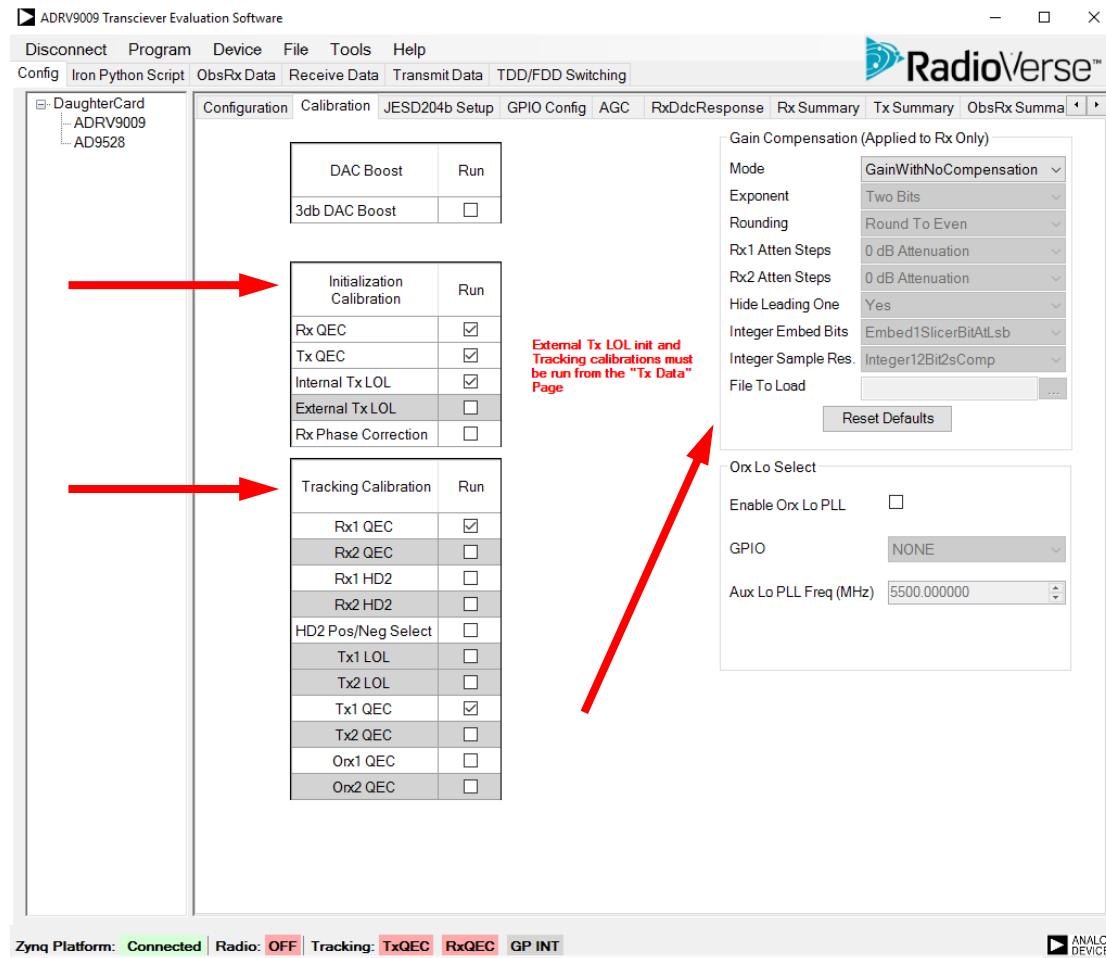
# AD9009 Configuration – Device Profile



- Select Device Clock frequency for desired profile
- Enable RX, TX, and ORX channels
- Select RX, TX, and ORX profiles (BW, IQ Rate)
- Set RF PLL Frequency
  - Can also setup EXT LO and PLL phase sync

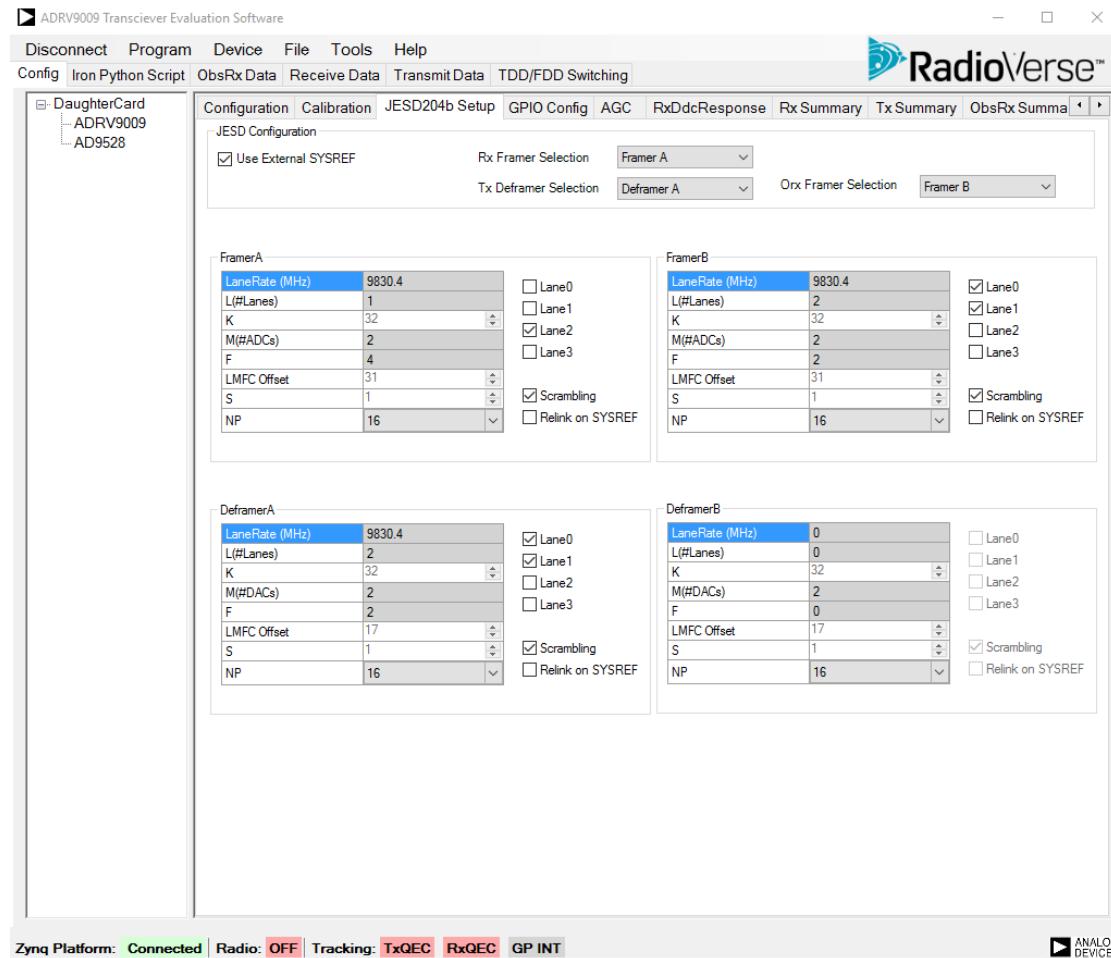
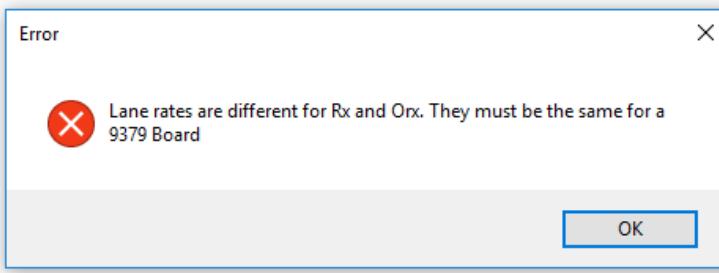
# AD9009 Configuration – Calibrations

- ▶ Select desired initialization calibrations
- ▶ Select desired tracking calibrations
- ▶ RX gain compensation and ORX LO select are also configurable
- ▶ We'll discuss calibrations in detail later in this presentation

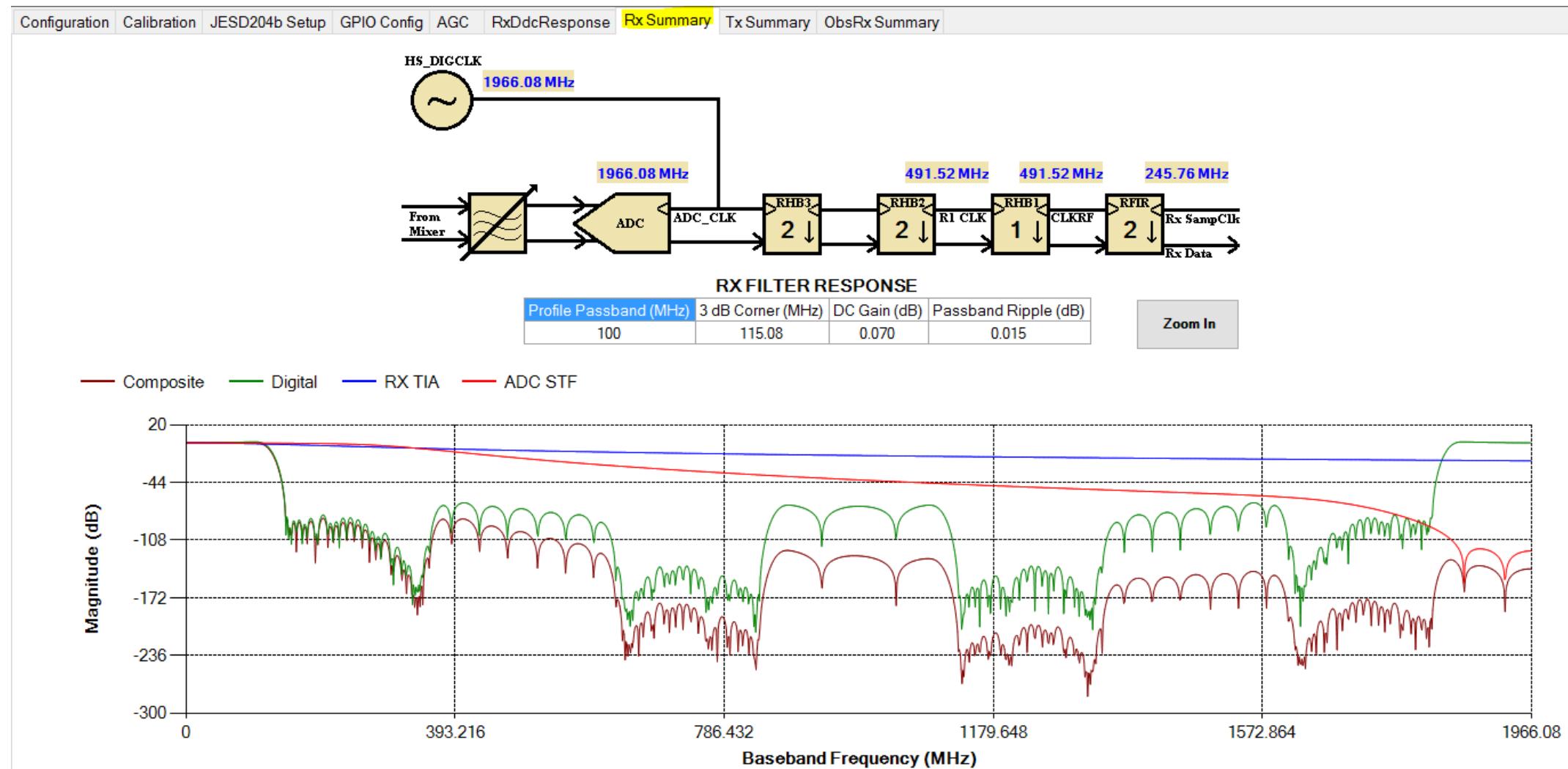


# AD9009 Configuration – JESD204b

- Framer and Deframer settings should auto configure based on profile settings on Configuration tab
- # of Lanes used may need to be adjusted based “Configuration” tab sample rates

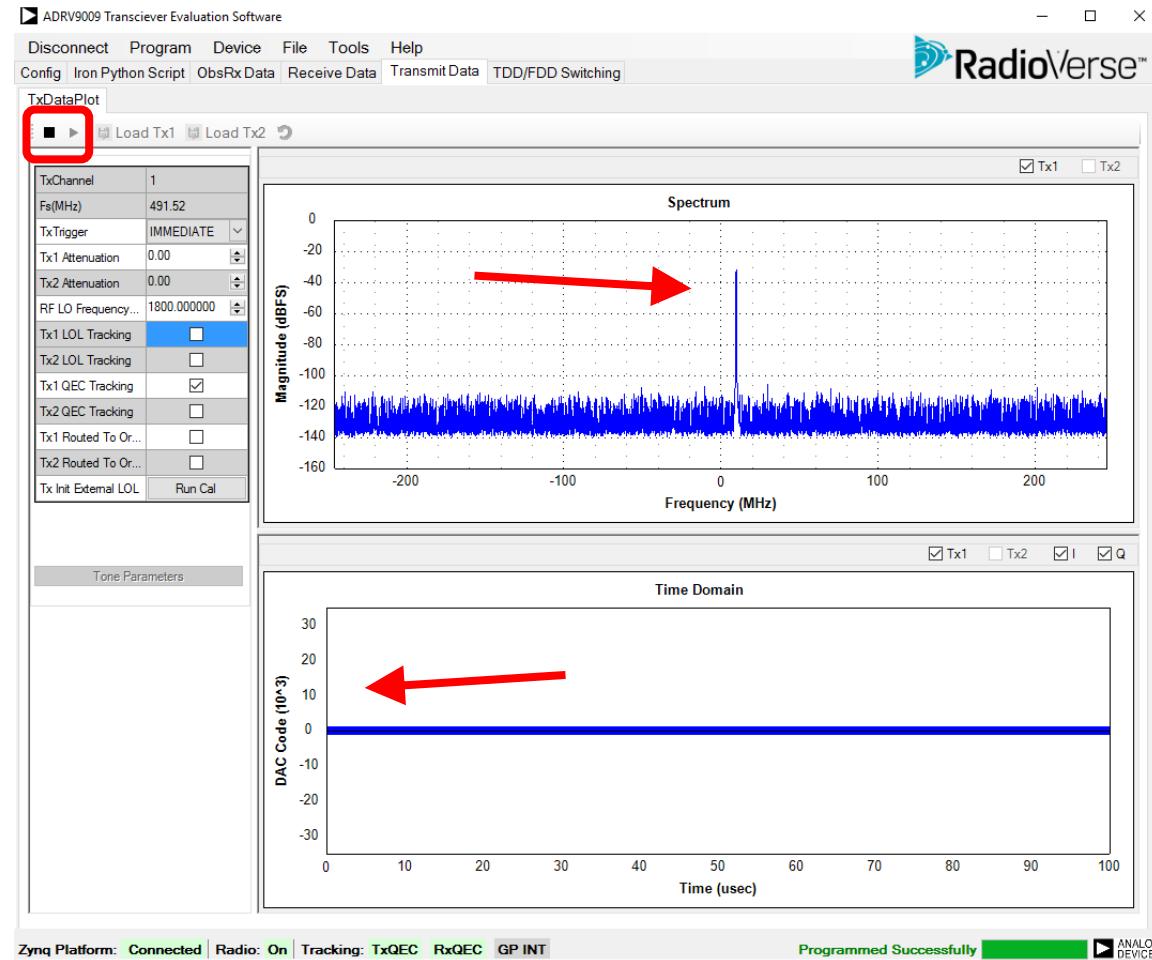


# AD9009 Configuration – Signal Path Summary



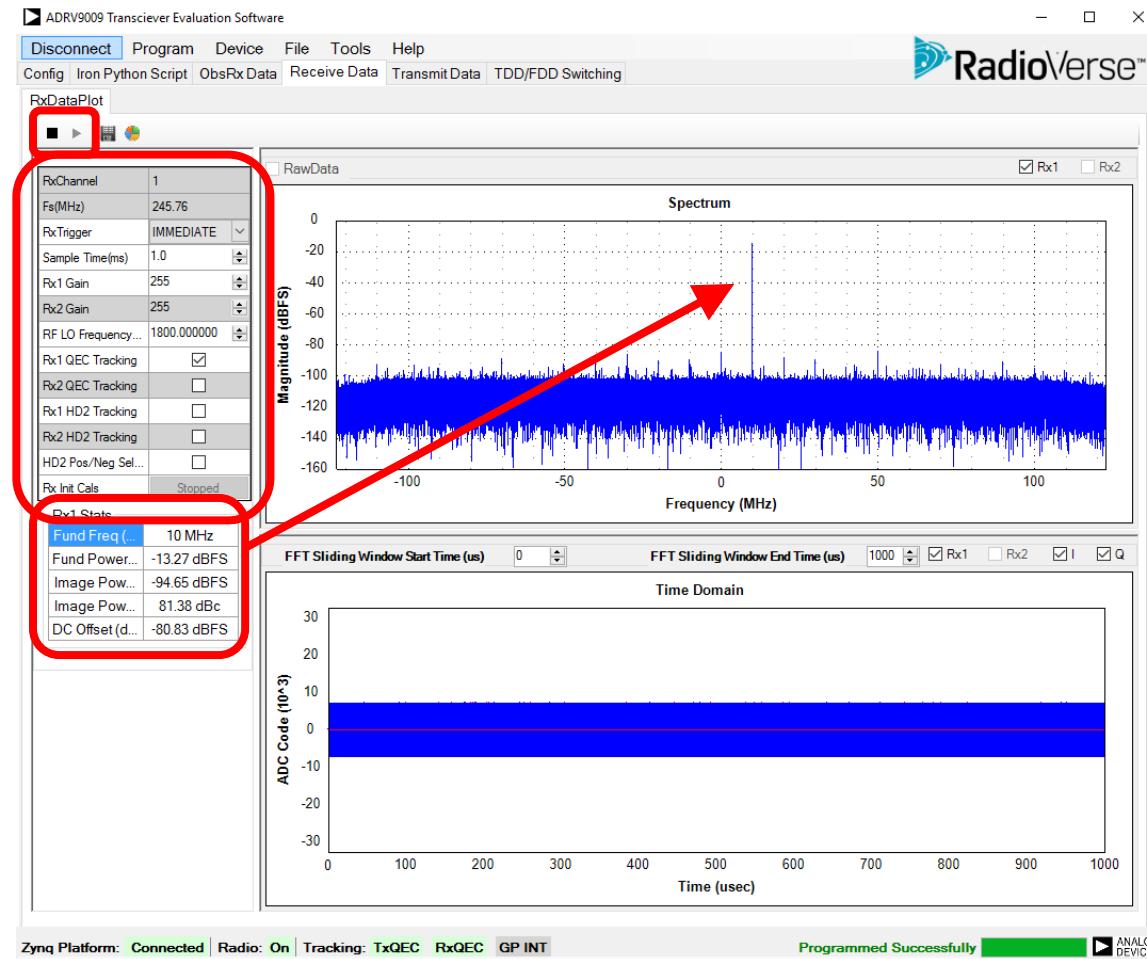
# AD9009 Operation – Transmit Data

- ▶ Use to operate transmitters
- ▶ Load custom waveforms
- ▶ Configure internal CW tone generator
- ▶ Configure tracking calibration, TX attenuation, trigger, and LO frequency
- ▶ Press ‘Play’ to enable transmitter(s)
- ▶ Frequency and time domain representations of transmitted data displayed



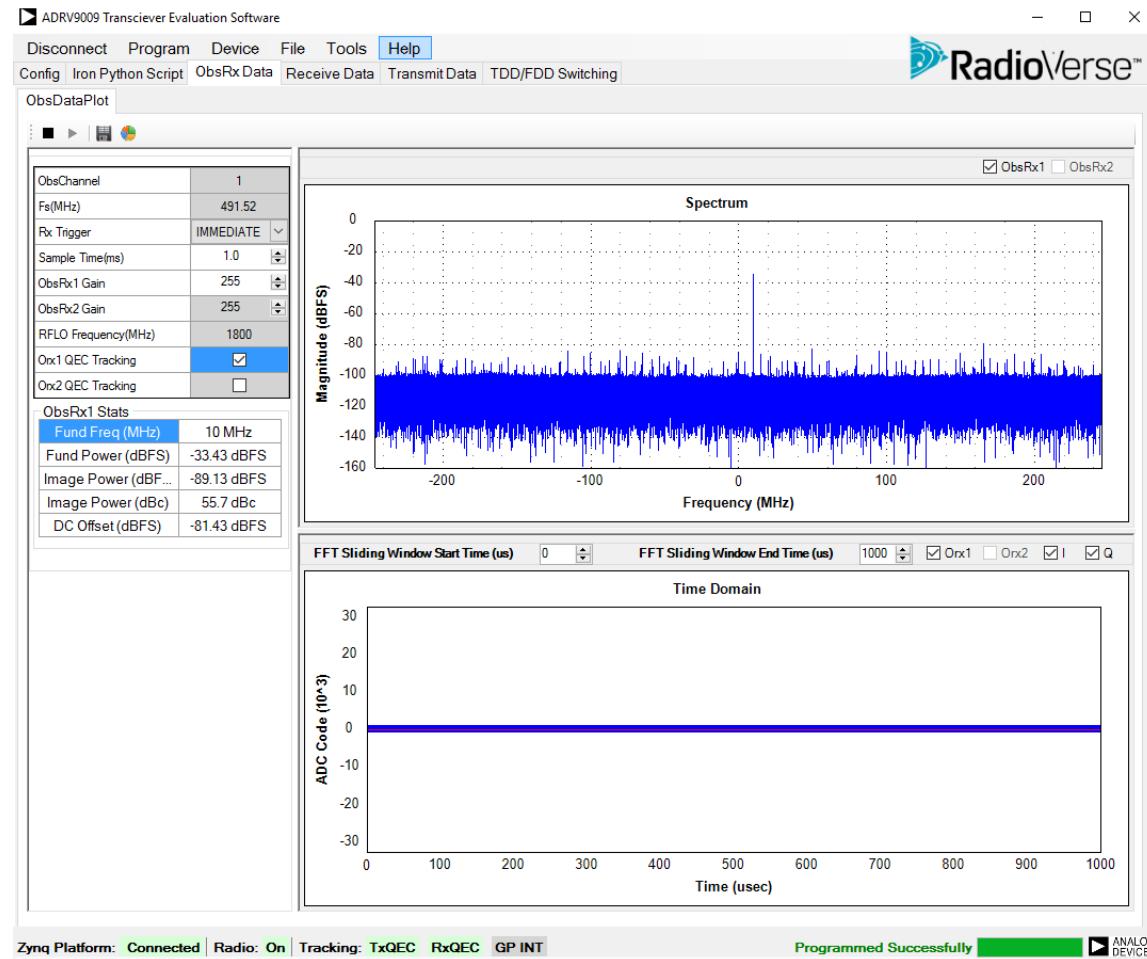
# AD9009 Operation – Receive Data

- ▶ Use to operate receivers
- ▶ Configure tracking calibrations, RX gain, trigger source, and LO frequency
- ▶ Press ‘Play’ to enable receiver(s)
- ▶ Click pie chart icon for signal statistics
- ▶ Frequency and time domain of received data displayed



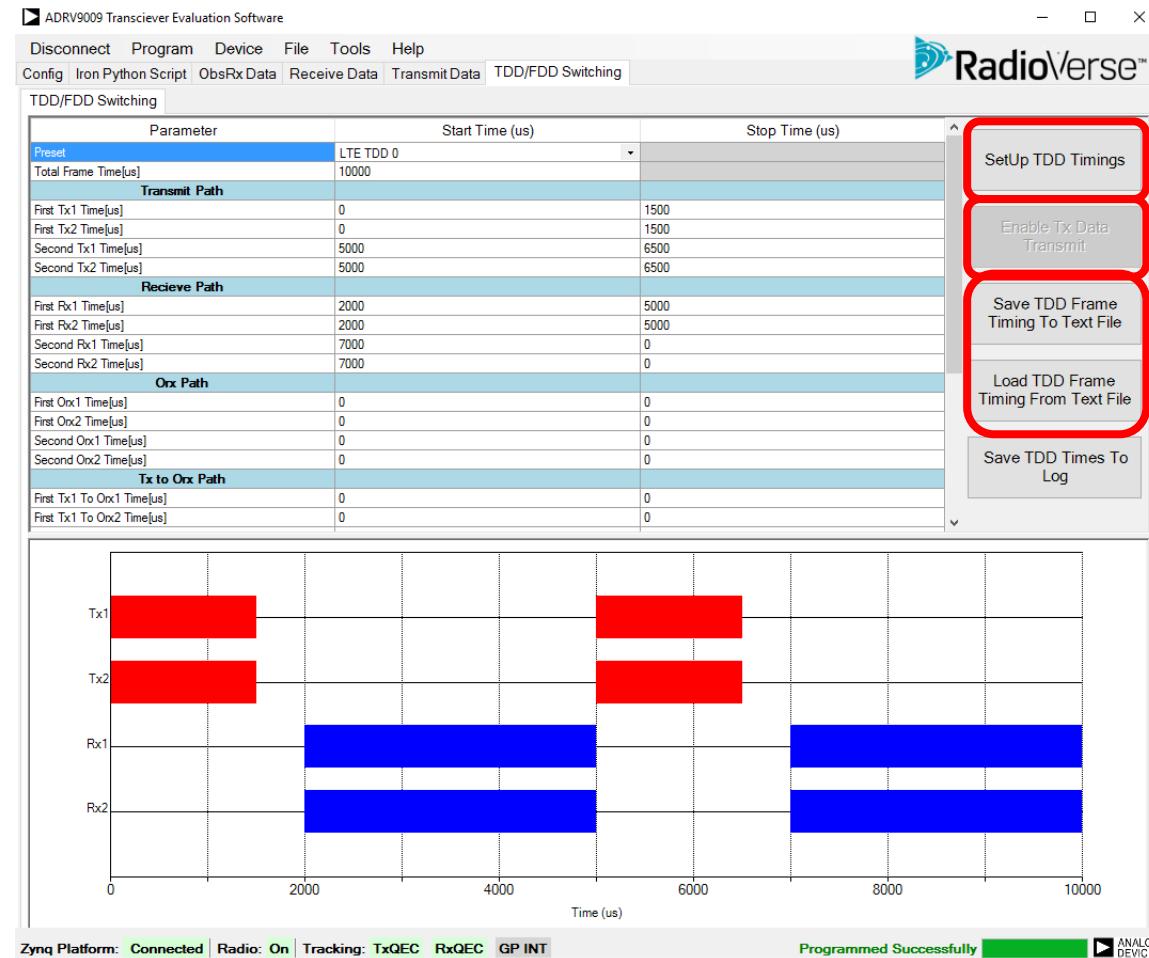
# AD9009 Operation – ObsRx Data

- ▶ Use to operate ObsRx
- ▶ Similar to RX control tab
- ▶ Press ‘Play’ to enable observation receiver(s)
- ▶ LO is set to TX LO unless otherwise configured
- ▶ Click pie chart icon to display signal statistics
- ▶ Frequency and time domain of received data displayed



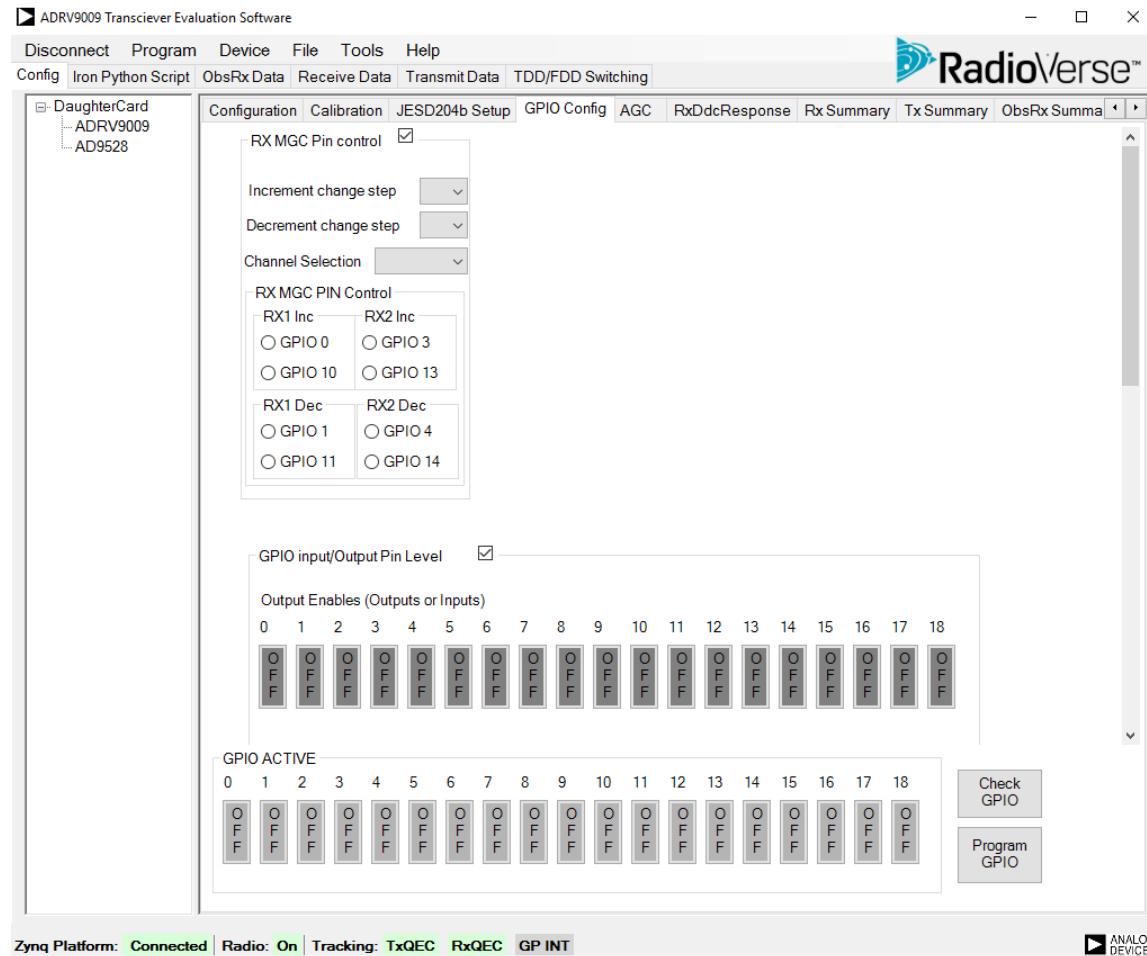
# AD9009 Operation – TDD Switching

- ▶ Use to configure TDD state machine for time domain RX/TX switching
- ▶ Timings can be loaded from file or save to file
- ▶ Click SetUp TDD timings to configure TDD state machine
- ▶ Ensure TX and RX are triggered from ‘TDD\_SM\_PULSE’
- ▶ Click Enable TX Data Transmit



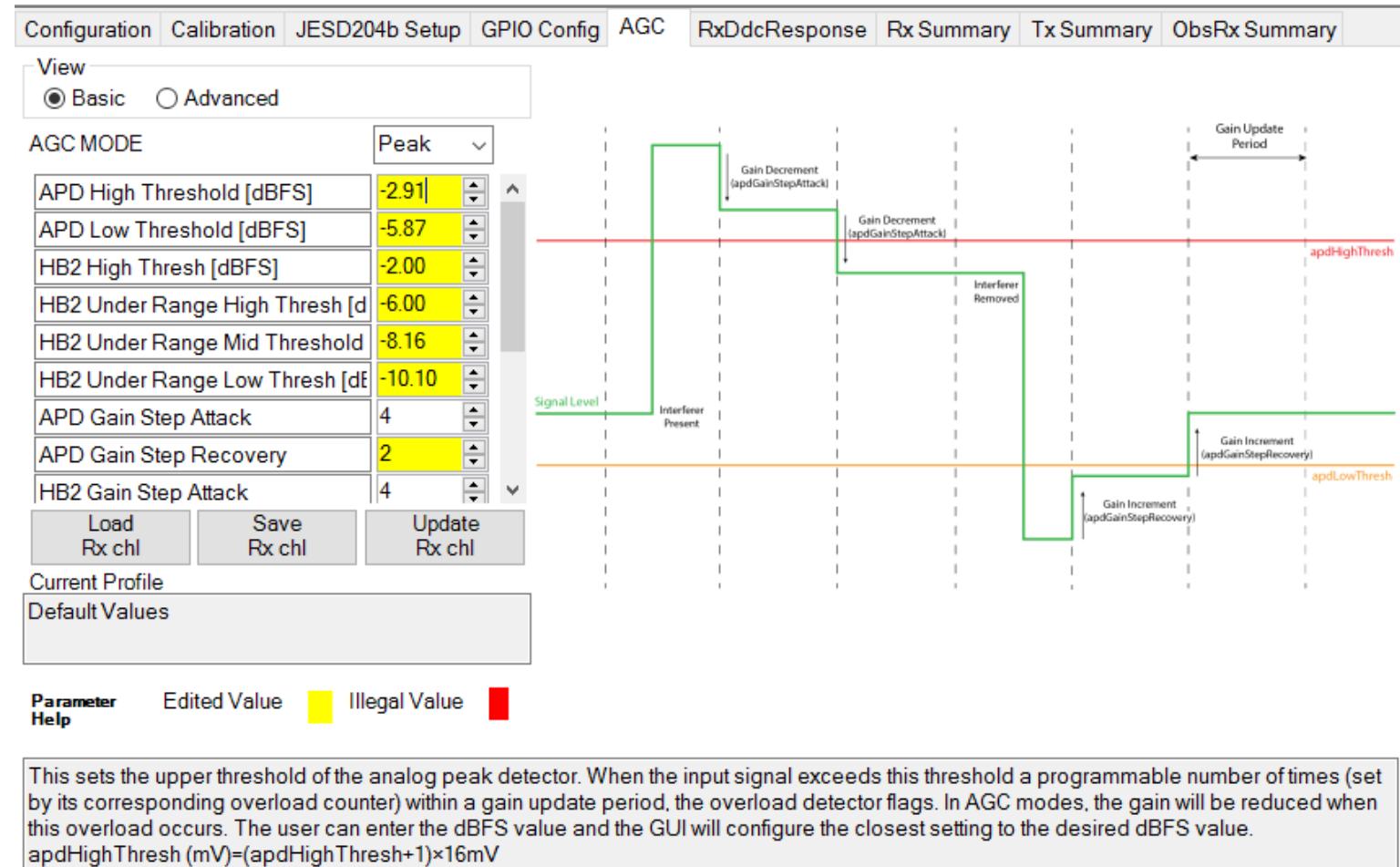
# AD9009 Operation – GPIO Configuration

- ADRV9009 TES supports:
  - RX AGC Configuration
  - GPIO Input/Output bitbang
  - GPIO Monitor Selection



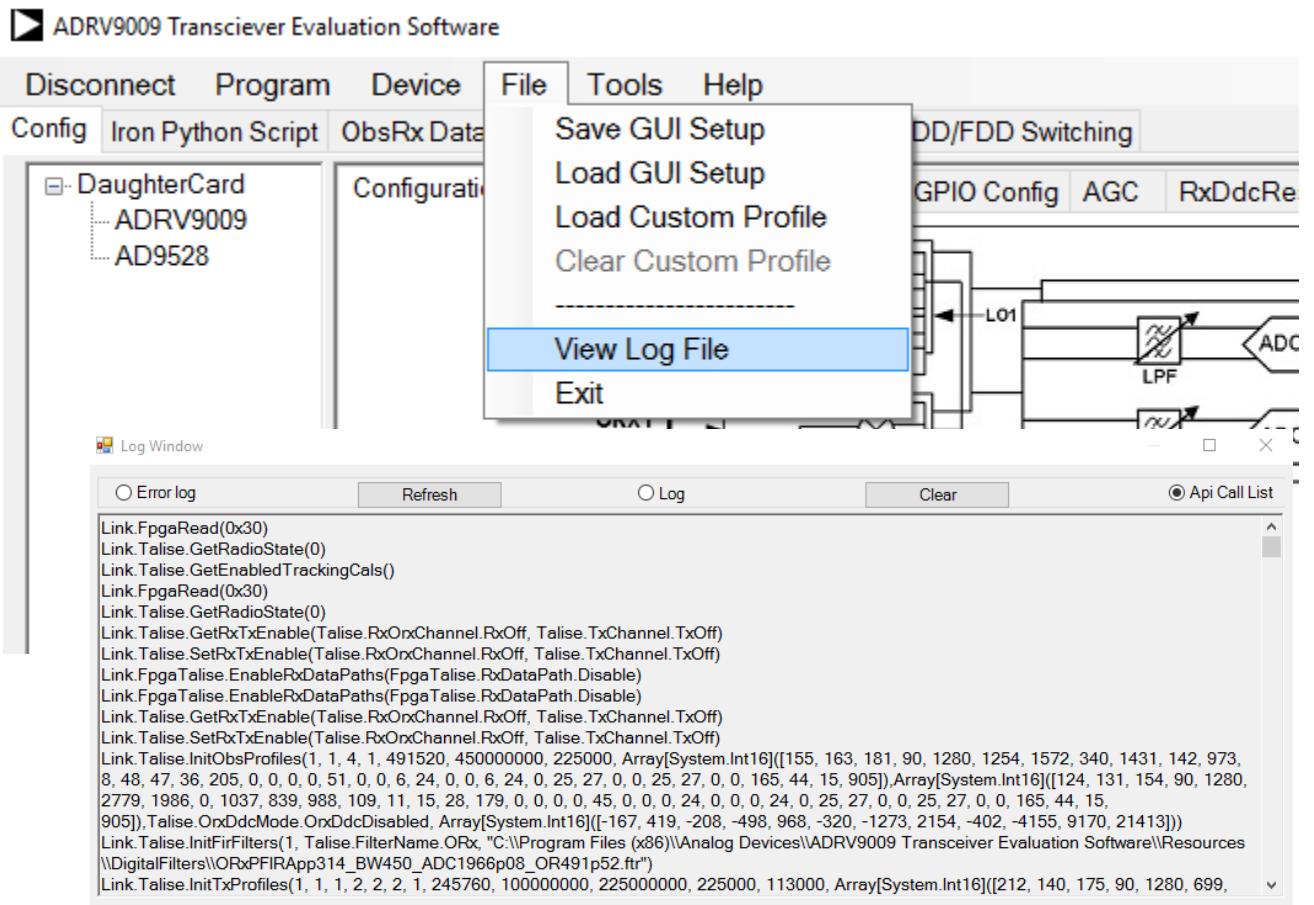
# AD9009 Operation – Automatic Gain Control Configuration

- ADRV9009 TES supports:
  - Manual Gain Control
    - Use GPIO inputs to gain index
    - Use GPIO outputs to monitor overrange
  - Automatic Gain Control
    - Lots of programmable settings...
    - More on that later in this presentation



# AD9009 GUI Debug and Log File

- Log File Contains:
  - Error Log
  - Log
  - API Call List
- General Purpose Interrupt Status is polled by the GUI every 2 seconds and reported in the status bar.
- API errors are logged to the Error logging window
- Device Radio state is shown in the GUI status bar
- Tracking cal enable information is shown in the status bar

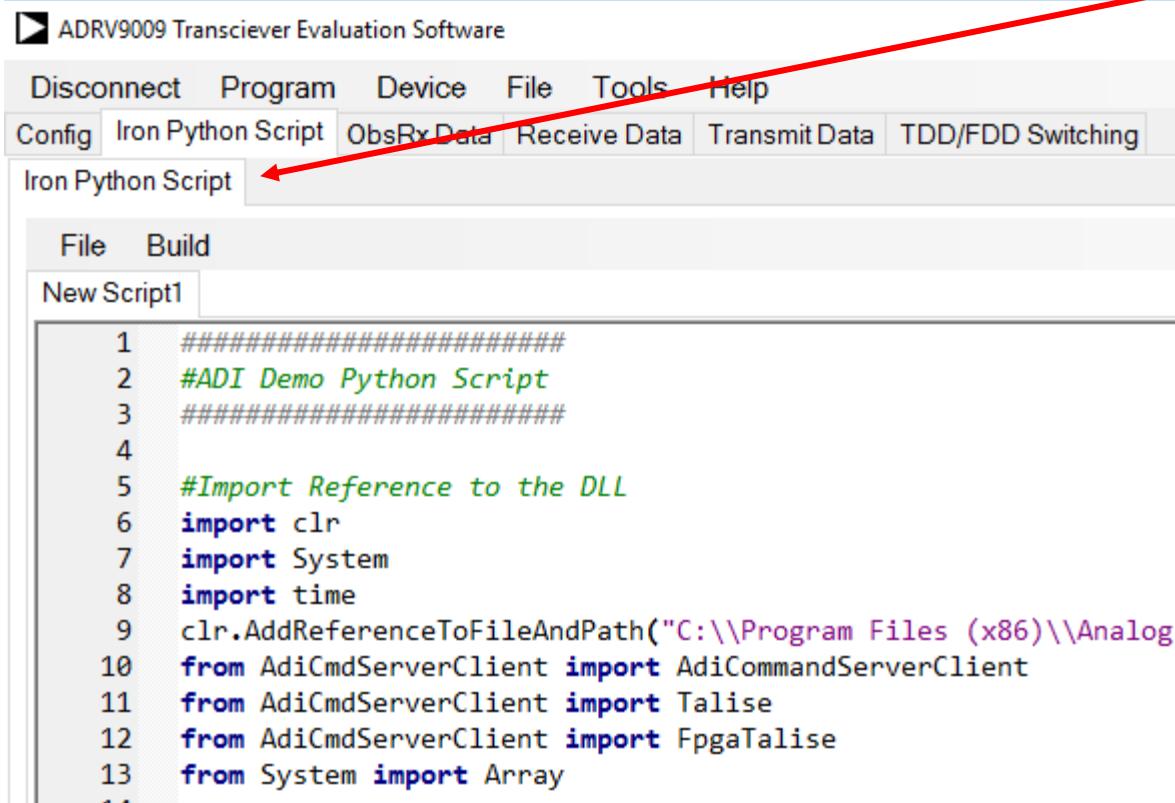


Zynq Platform: Connected | Radio: On | Tracking: TxQEC RxQEC GP INT

Programmed Successfully  ANALOG DEVICES

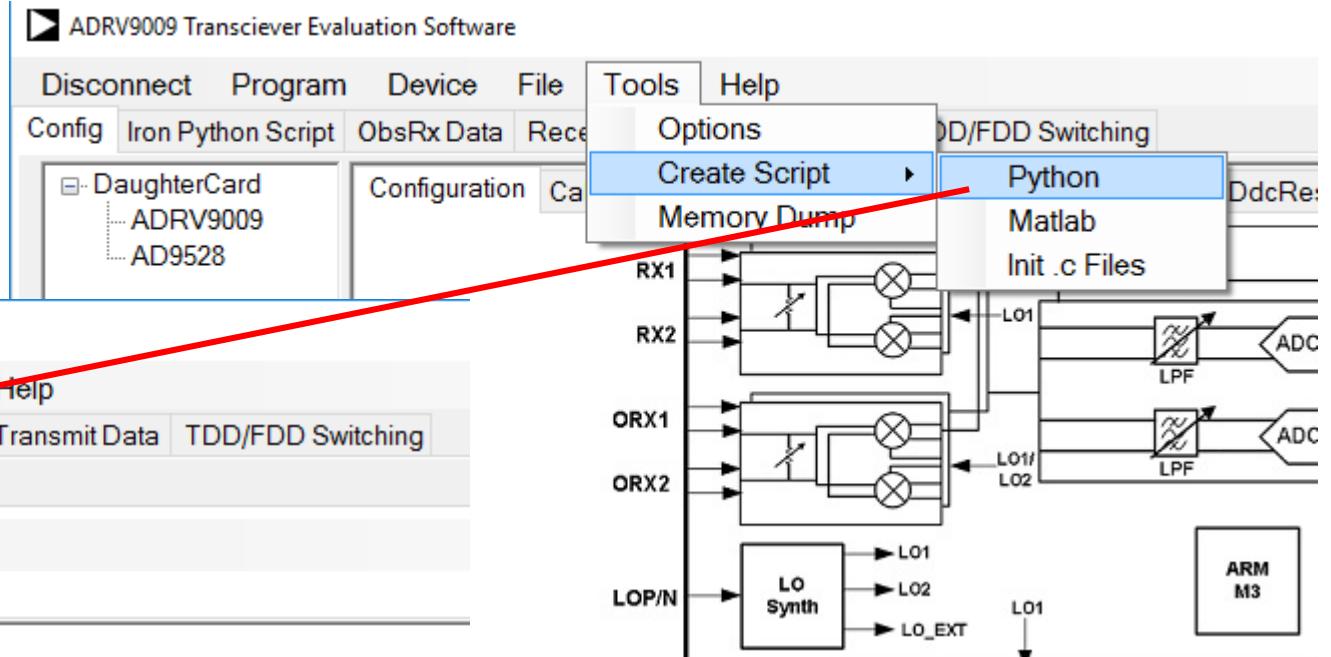
# Create Scripts

- TES will output setup parameters to
  - Python
  - C Program
  - Matlab



The screenshot shows the software interface for the ADRV9009 Transceiver Evaluation Software. The window title is "ADRV9009 Transceiver Evaluation Software". The menu bar includes Disconnect, Program, Device, File, Tools, Help, Config, Iron Python Script, ObsRx Data, Receive Data, Transmit Data, and TDD/FDD Switching. The "Iron Python Script" tab is currently selected. Below the tabs, there is a toolbar with File and Build buttons. A text editor window titled "New Script1" contains the following Python code:

```
1 #####  
2 #ADI Demo Python Script  
3 #####  
4  
5 #Import Reference to the DLL  
6 import clr  
7 import System  
8 import time  
9 clr.AddReferenceToFileAndPath("C:\\Program Files (x86)\\Analog  
10 from AdiCmdServerClient import AdiCommandServerClient  
11 from AdiCmdServerClient import Talise  
12 from AdiCmdServerClient import FpgaTalise  
13 from System import Array  
14
```



# Automation of the ADI evaluation hardware

- Talise GUI has a scripting tab – IronPython
  - GUI will generate an Iron Python script of the init sequence.
- All API and hardware calls are accomplished by calling a .Net DLL
  - Any language that supports .Net DLLs can control the hardware

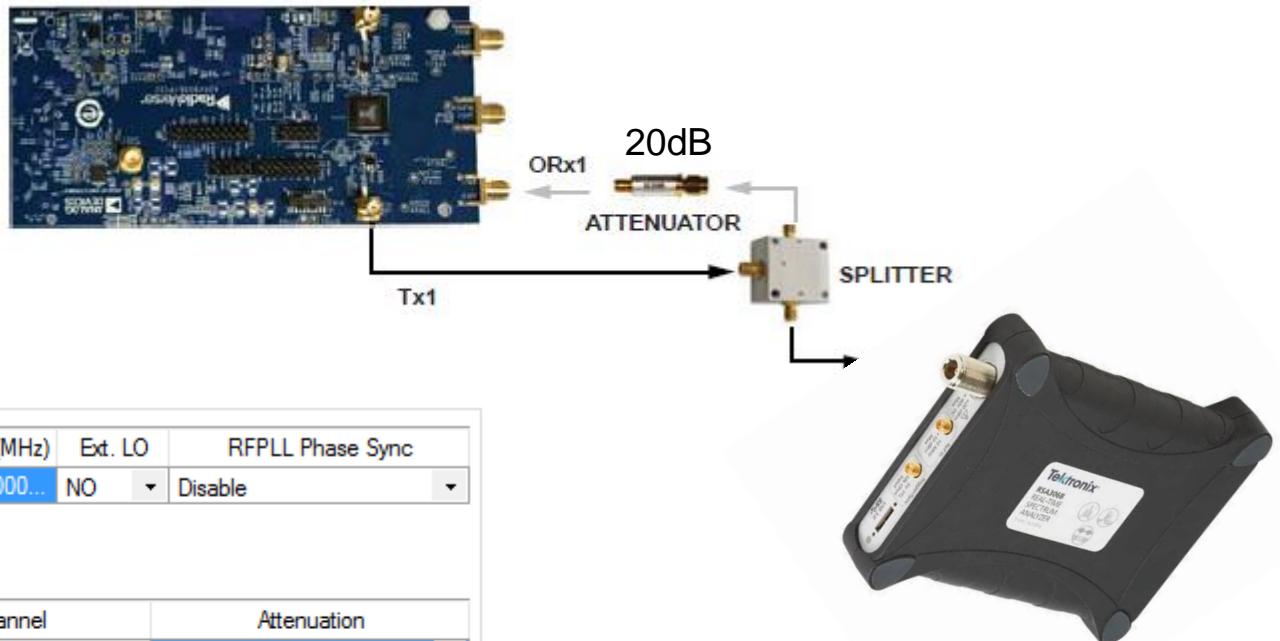
- Matlab
- Labview
- Iron Python
- C#, VB .Net, etc

```
12 #####
73 # Program Talise
74 #####
75 Link.Talise.ResetDevice()
76 Link.Talise.Initialize()
77 Link.Talise.SetDacFullScale(Talise.DacFullScale.DacFs0dB)
78 pllStatus = Link.Talise.GetPllsLockStatus()
79 print 'Talise pllStatus = ', hex(pllStatus)
80 Link.Talise.EnableMultichipSync(0x1, 0x0)
81 Link.Ad9528.RequestSysref(1)
82 Link.Ad9528.RequestSysref(1)
83 Link.Ad9528.RequestSysref(1)
84 Link.Ad9528.RequestSysref(1)
85 time.sleep(0.1)
86 mcsStatus = Link.Talise.EnableMultichipSync(0x0, 0x0)
87 print 'MCS Status = ', hex(mcsStatus)
88
89 Link.FpgaTalise.SetupJesd204bOversampler(FpgaTalise.FpgaDeframerSelect.DeframerB, FpgaTalise.FpgaSampleDecimation.DecimateBy1)
90 Link.SetLogLevel(0)
91 if pllStatus & 0x01:
92     Link.Talise.InitArm()
93     Link.Talise.LoadStreamProcessor("C:\\\\Users\\\\doates\\\\AppData\\\\Local\\\\Temp\\\\TaliseStream.bin")
94     Link.Talise.LoadArm("C:\\\\Program Files (x86)\\\\Analog Devices\\\\Talise Transceiver Evaluation Software\\\\Resources\\\\TaliseTDDArmFirmware.bin")
95     isArmGood = Link.Talise.VerifyArmChecksum()
96     print 'isArmGood = ', hex(isArmGood)
97     if isArmGood & 1:
98         print "ARM Loaded Successfully"
99     else:
100        print "ARM File not loaded correctly"
101 else:
102    print "pll Lock Status is Incorrect"
103 Link.Talise.GetArmVersion()
104 Link.SetLogLevel(63)
105 Link.Talise.SetRfPllFrequency(Talise.PllName.Rfp11, 20000000001
```

# ADRV9009 Tx

# Effect of Calibration on the Eval Board

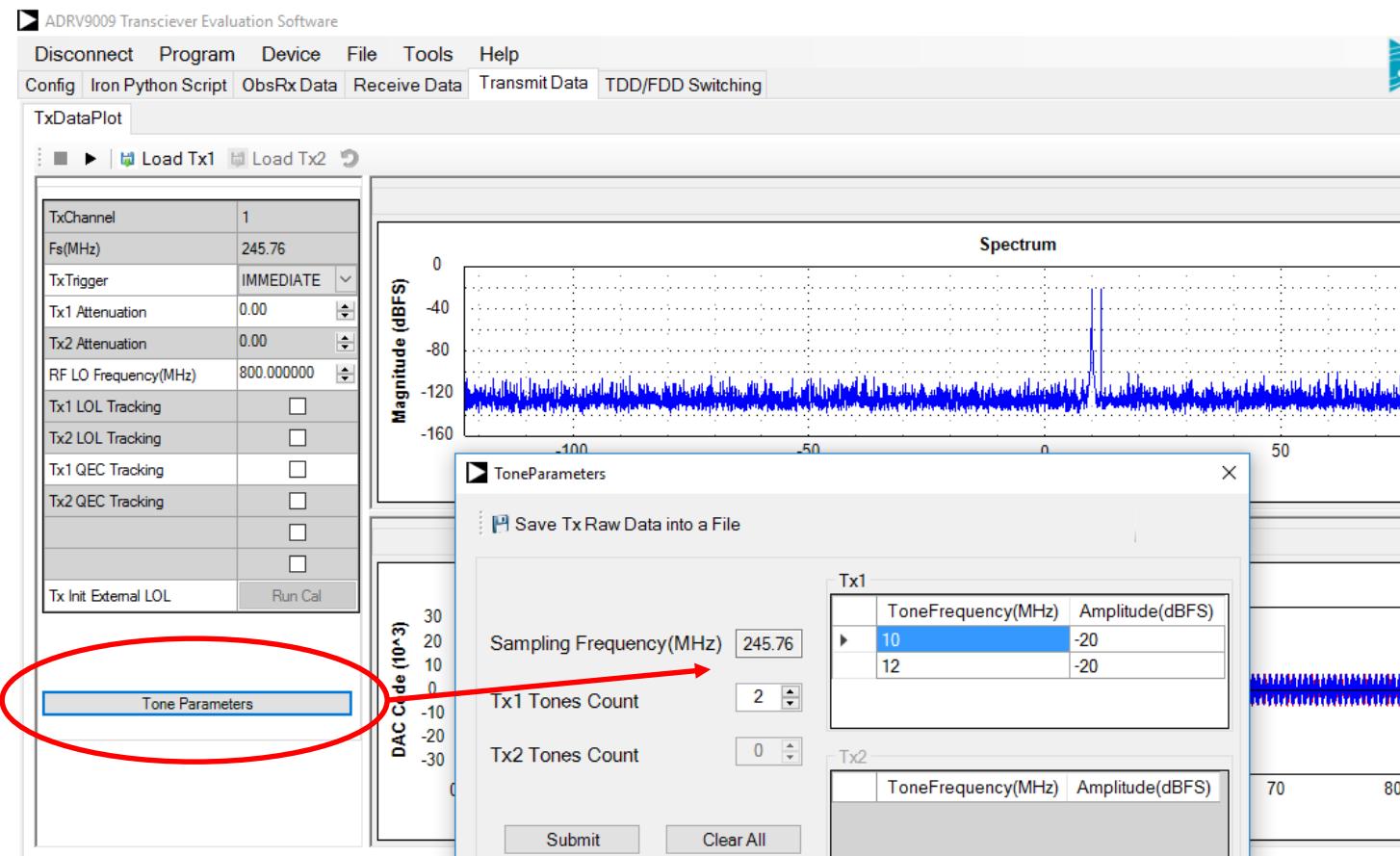
- Let's experiment with the effect of various calibrations.
- First set the eval board and TES like this:



	GPO_GPS	GPO	AUXADC	AUXDAC	
Device	ADRV9009				LO PLL Freq(MHz) Ext. LO RFPLL Phase Sync
Device Clock	122.88MHz				RF PLL 800.000... NO Disable
Rx Channel	RX1 Enabled				Tx Channel Attenuation
Rx Profile	Rx 200MHz, IQrate 245.76MHz, Dec4				Tx1 0.00
Tx Channel	TX1 Enabled				Tx2 0.00
Tx Profile	Tx 100/225MHz, IQrate 245.76MHz				Rx/Tx Channel Control Pin Mode
Observation Channel	Observation Off				<input checked="" type="radio"/> Independant Channel Control
Obs Profile	ORX 200MHz, IQrate 245.76MHz, Dec4				<input type="radio"/> Paired Channel Control (uses Rx1/Tx1_ENABLE pins)
Load Custom Stream	<input type="checkbox"/>				DAC Enabled
					<input type="radio"/> Higher Power Faster Tx Switching Time
					<input checked="" type="radio"/> Lower Power Slower Tx Switching Time

# Effect of Calibration on the Eval Board

- Then use the FPGA to construct a dual tone on TX1



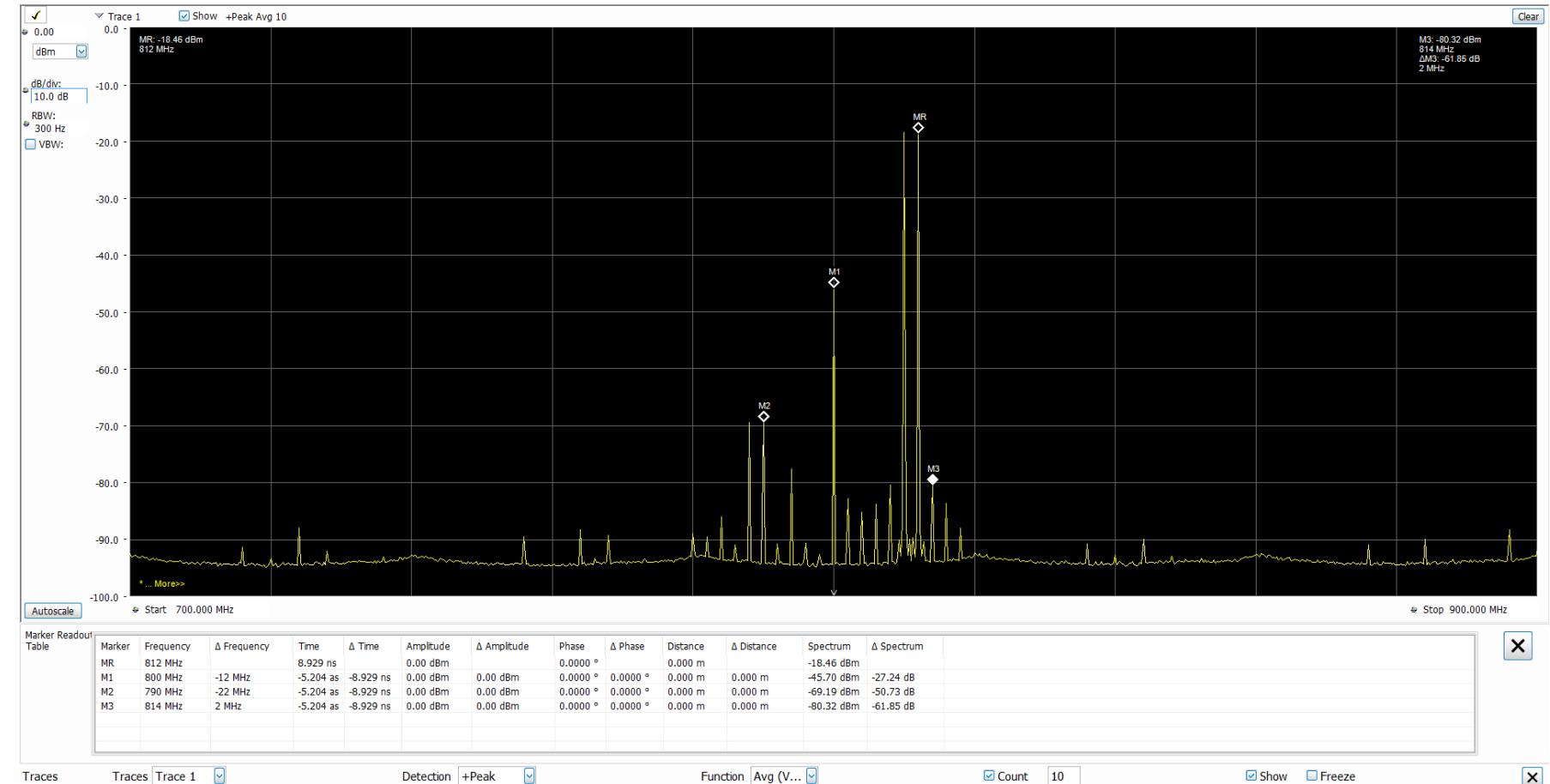
# Effect of Calibration on the Eval Board

- First, make sure all calibrations are off, and observe the spectrum:

DAC Boost	Run
3db DAC Boost	<input checked="" type="checkbox"/>

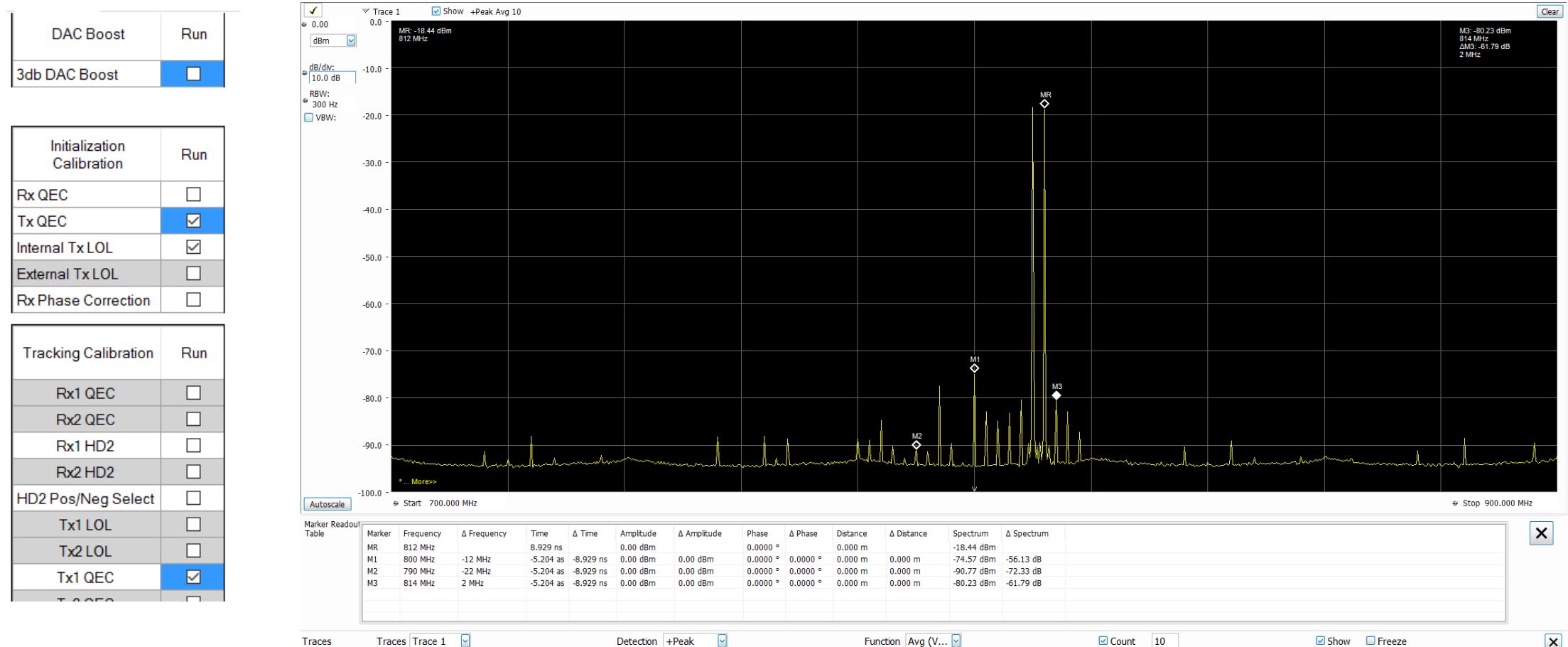
Initialization Calibration	Run
Rx QEC	<input type="checkbox"/>
Tx QEC	<input type="checkbox"/>
Internal Tx LOL	<input checked="" type="checkbox"/>
External Tx LOL	<input type="checkbox"/>
Rx Phase Correction	<input type="checkbox"/>

Tracking Calibration	Run
Rx1 QEC	<input type="checkbox"/>
Rx2 QEC	<input type="checkbox"/>
Rx1 HD2	<input type="checkbox"/>
Rx2 HD2	<input type="checkbox"/>
HD2 Pos/Neg Select	<input type="checkbox"/>
Tx1 LOL	<input type="checkbox"/>
Tx2 LOL	<input type="checkbox"/>



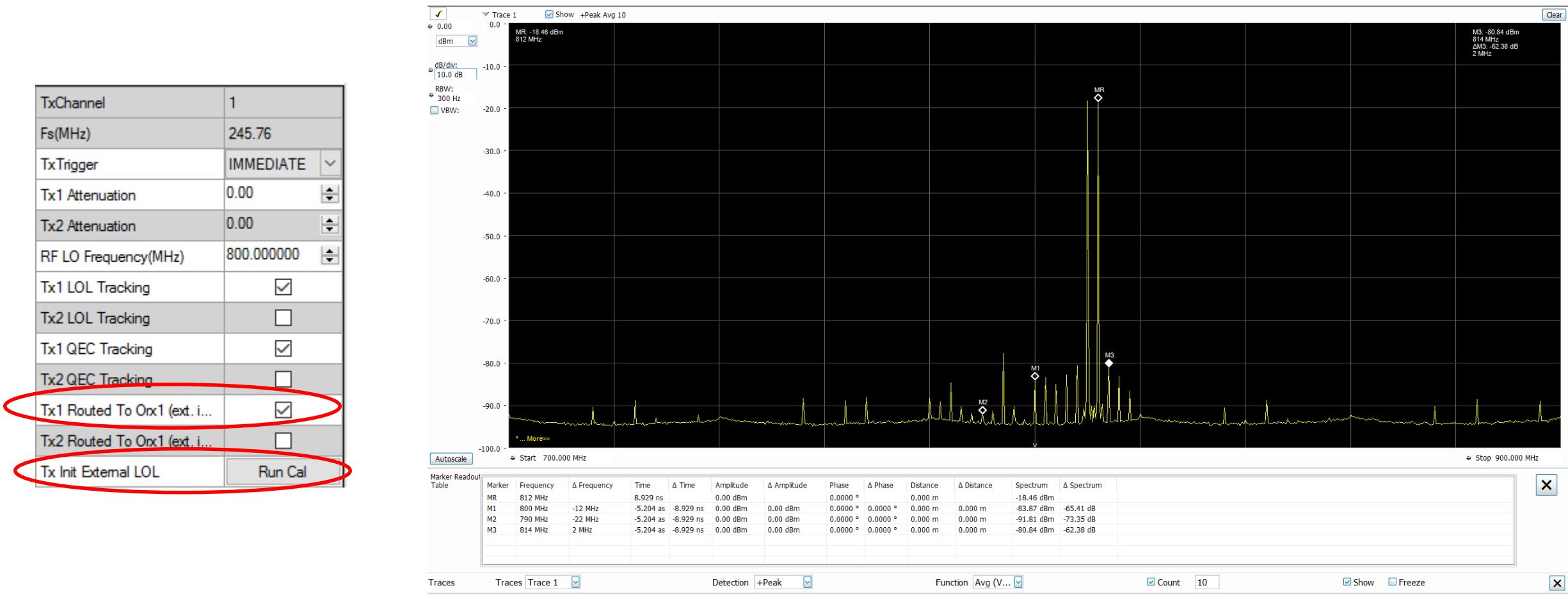
# Effect of Calibration on the Eval Board

- Now, let's turn on the internal cals, and observe the change to image and LO leakage:



# Effect of Calibration on the Eval Board

- Now, let's enable the ORx path to enable External Tx LO leakage calibration



# ADRV9009 Rx

# Let's Monitor Our Calibrations!

- Turn on the Rx calibrations and the Tx internal LOL calibration

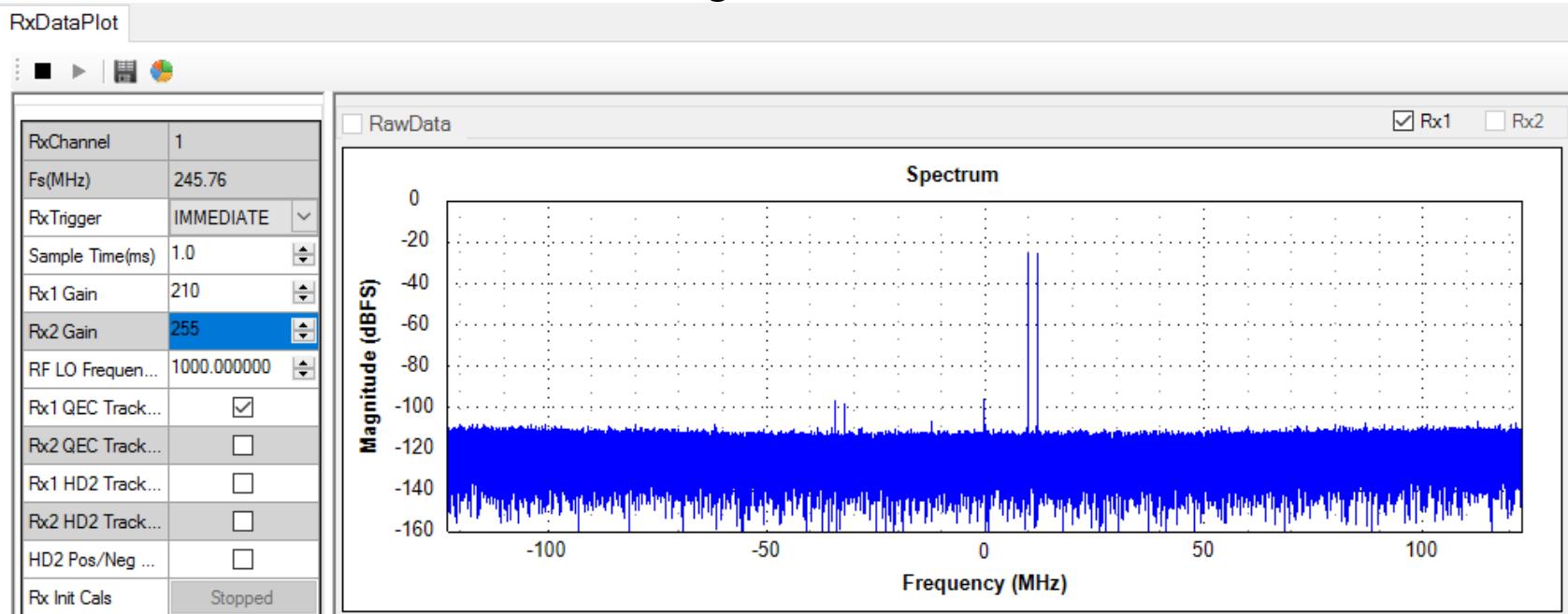
Configuration Calibration JESD204b Setup G

DAC Boost	Run
3db DAC Boost	<input type="checkbox"/>

Initialization Calibration	Run
Rx QEC	<input checked="" type="checkbox"/>
Tx QEC	<input checked="" type="checkbox"/>
Internal Tx LOL	<input checked="" type="checkbox"/>
External Tx LOL	<input type="checkbox"/>
Rx Phase Correction	<input type="checkbox"/>

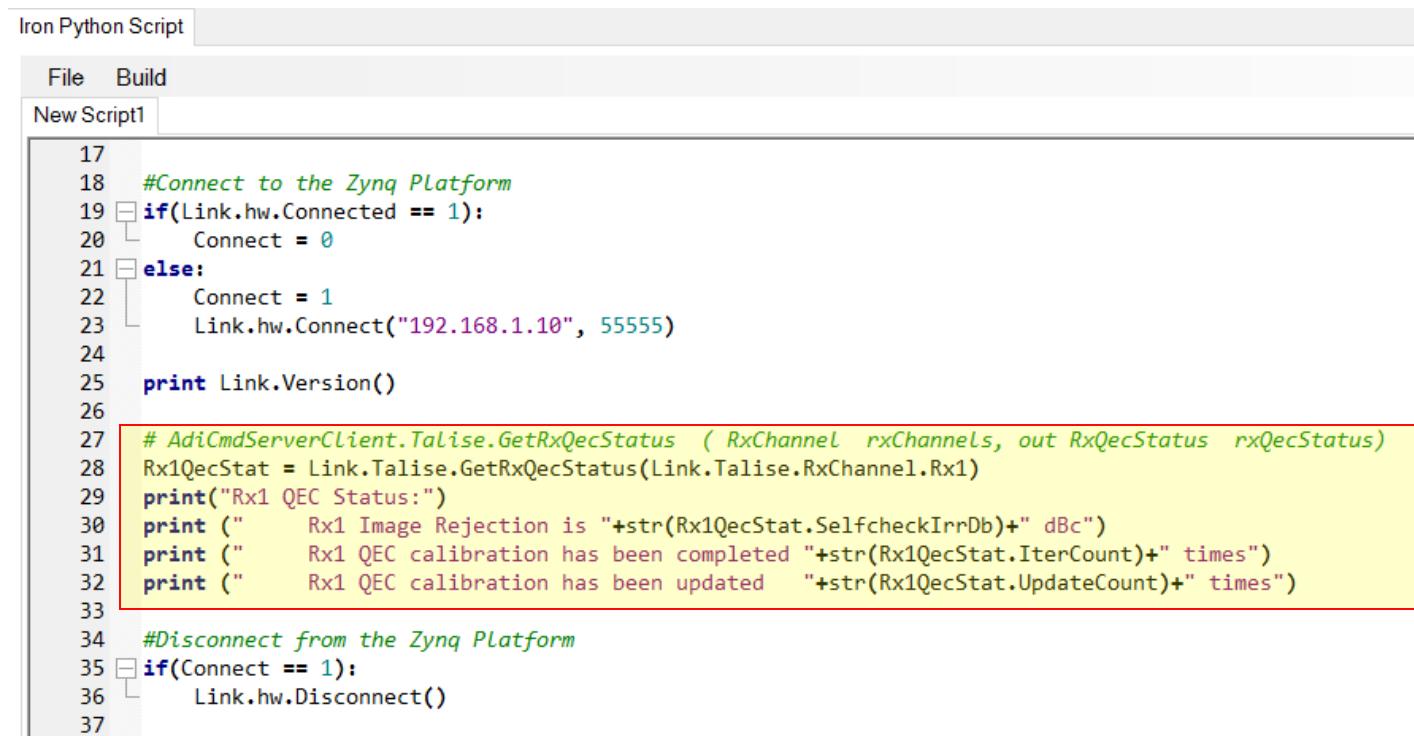
Tracking Calibration	Run
Rx1 QEC	<input checked="" type="checkbox"/>
Rx2 QEC	<input type="checkbox"/>
Rx1 HD2	<input type="checkbox"/>
Rx2 HD2	<input type="checkbox"/>
HD2 Pos/Neg Select	<input type="checkbox"/>
Tx1 LOL	<input type="checkbox"/>
Tx2 LOL	<input type="checkbox"/>
Tx1 QEC	<input checked="" type="checkbox"/>
Tx2 QEC	<input type="checkbox"/>
Onx1 QEC	<input type="checkbox"/>
Onx2 QEC	<input type="checkbox"/>

- Use an SMA cable to connect TX1 to RX1
- Play data on TX1 and Observe RX1
- Make sure Rx1 QEC Tracking is Enabled



# Let's Monitor Our Calibrations!

- The TES GUI doesn't give us the hooks for all diagnostic calibration info.
- But we can still access it via a simple Python script
- Go to the Iron Python Script Tab
  - Select File → New to load the default script
  - Add the code (lines 27-32) below to the default script:



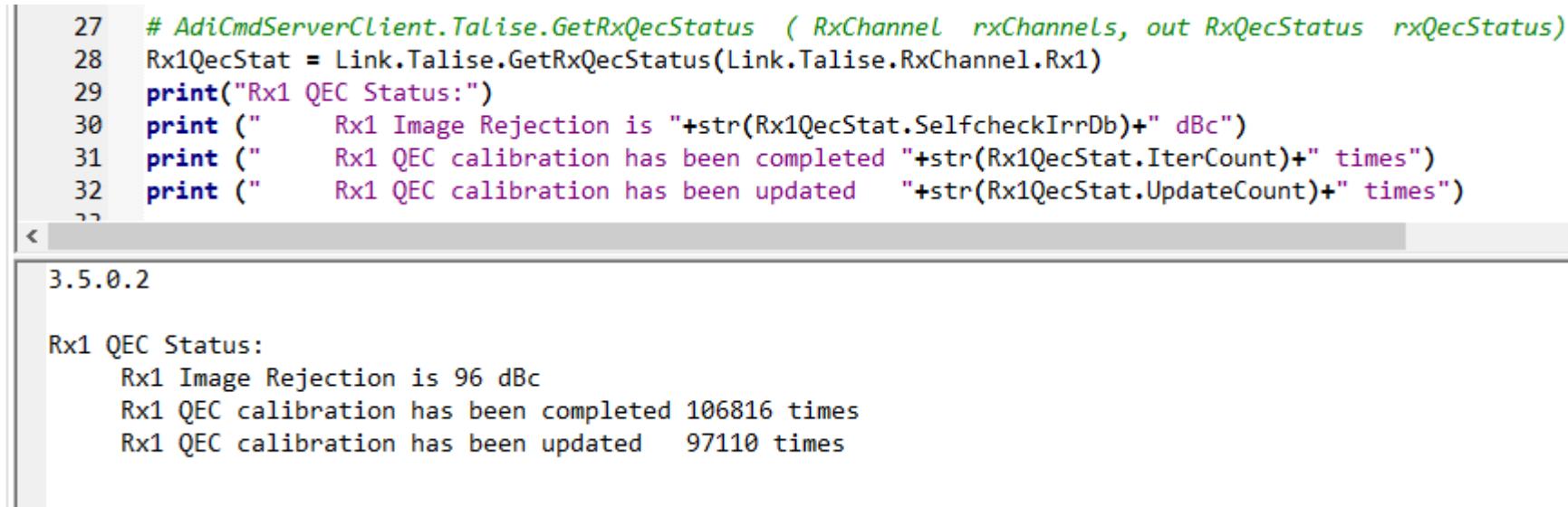
The screenshot shows a software interface titled "Iron Python Script". The menu bar includes "File" and "Build". The tab bar shows "New Script1". The main code area contains the following Python script:

```
17
18 #Connect to the Zynq Platform
19 if(Link.hw.Connected == 1):
20     Connect = 0
21 else:
22     Connect = 1
23     Link.hw.Connect("192.168.1.10", 55555)
24
25 print Link.Version()
26
27 # AdiCmdServerClient.Talise.GetRxQecStatus ( RxChannel rxChannels, out RxQecStatus rxQecStatus )
28 Rx1QecStat = Link.Talise.GetRxQecStatus(Link.Talise.RxChannel.Rx1)
29 print("Rx1 QEC Status:")
30 print ("    Rx1 Image Rejection is "+str(Rx1QecStat.SelfcheckIrrDb)+" dBc")
31 print ("    Rx1 QEC calibration has been completed "+str(Rx1QecStat.IterCount)+" times")
32 print ("    Rx1 QEC calibration has been updated   "+str(Rx1QecStat.UpdateCount)+" times")
33
34 #Disconnect from the Zynq Platform
35 if(Connect == 1):
36     Link.hw.Disconnect()
37
```

Lines 27 through 32 are highlighted with a yellow background and a red border, indicating they are the specific code to be added.

# Let's Monitor Our Calibrations!

- Now go to Build → Run (F5)
- You will see the following output:



```
27 # AdiCmdServerClient.Talise.GetRxQecStatus ( RxChannel rxChannels, out RxQecStatus rxQecStatus)
28 Rx1QecStat = Link.Talise.GetRxQecStatus(Link.Talise.RxChannel.Rx1)
29 print("Rx1 QEC Status:")
30 print ("    Rx1 Image Rejection is "+str(Rx1QecStat.SelfcheckIrrDb)+" dBc")
31 print ("    Rx1 QEC calibration has been completed "+str(Rx1QecStat.IterCount)+" times")
32 print ("    Rx1 QEC calibration has been updated   "+str(Rx1QecStat.UpdateCount)+" times")
33
```

3.5.0.2

Rx1 QEC Status:  
Rx1 Image Rejection is 96 dBc  
Rx1 QEC calibration has been completed 106816 times  
Rx1 QEC calibration has been updated 97110 times

- Talise gives its estimate of our Image Rejection (use this just for diagnostic purposes)
- And tells us how many times Rx1 QEC calibration has been run, and updated.

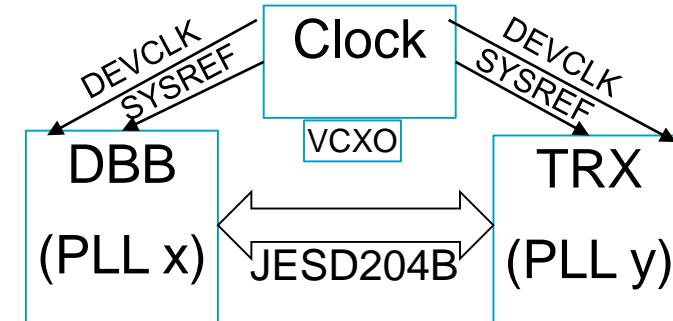
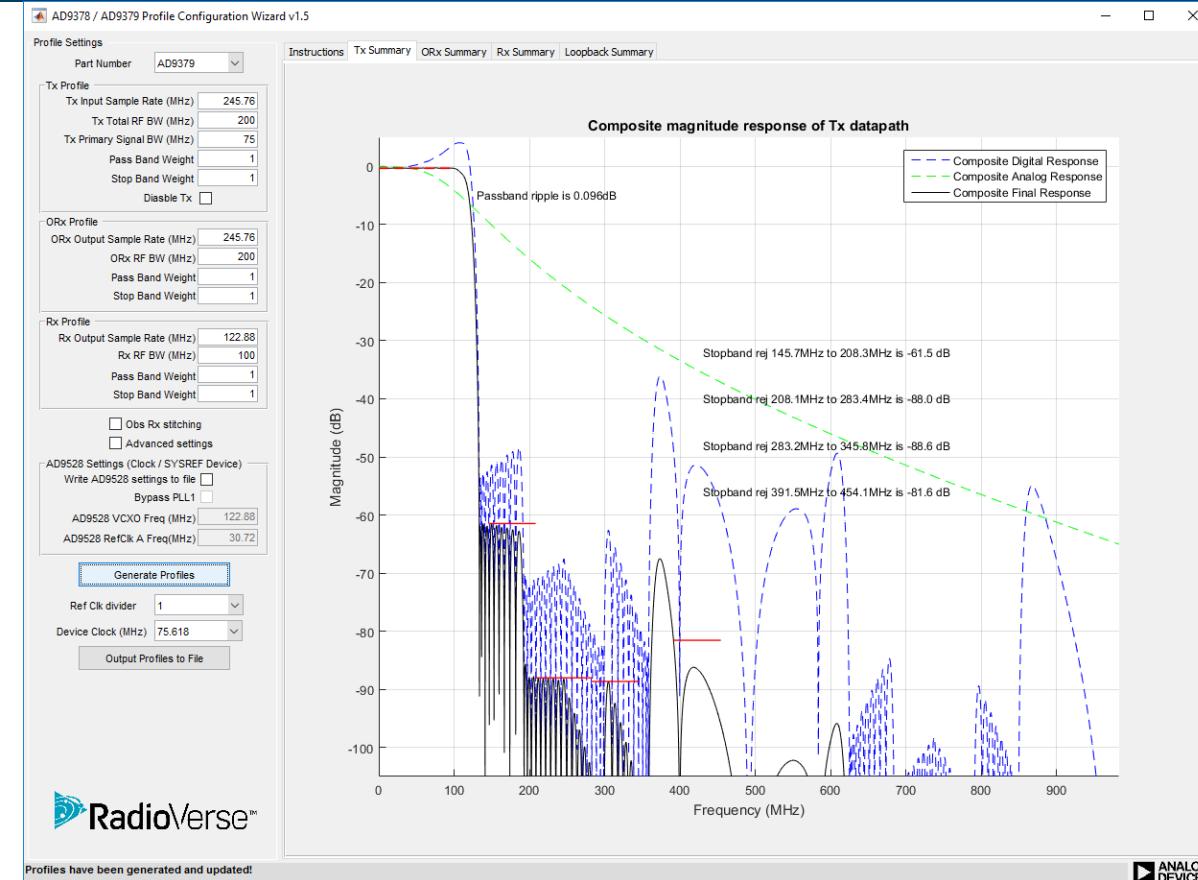


AHEAD OF WHAT'S POSSIBLE™

# ADRV9009 Configuration Wizard

# The ADRV9008-x, ADRV9009 Wizard

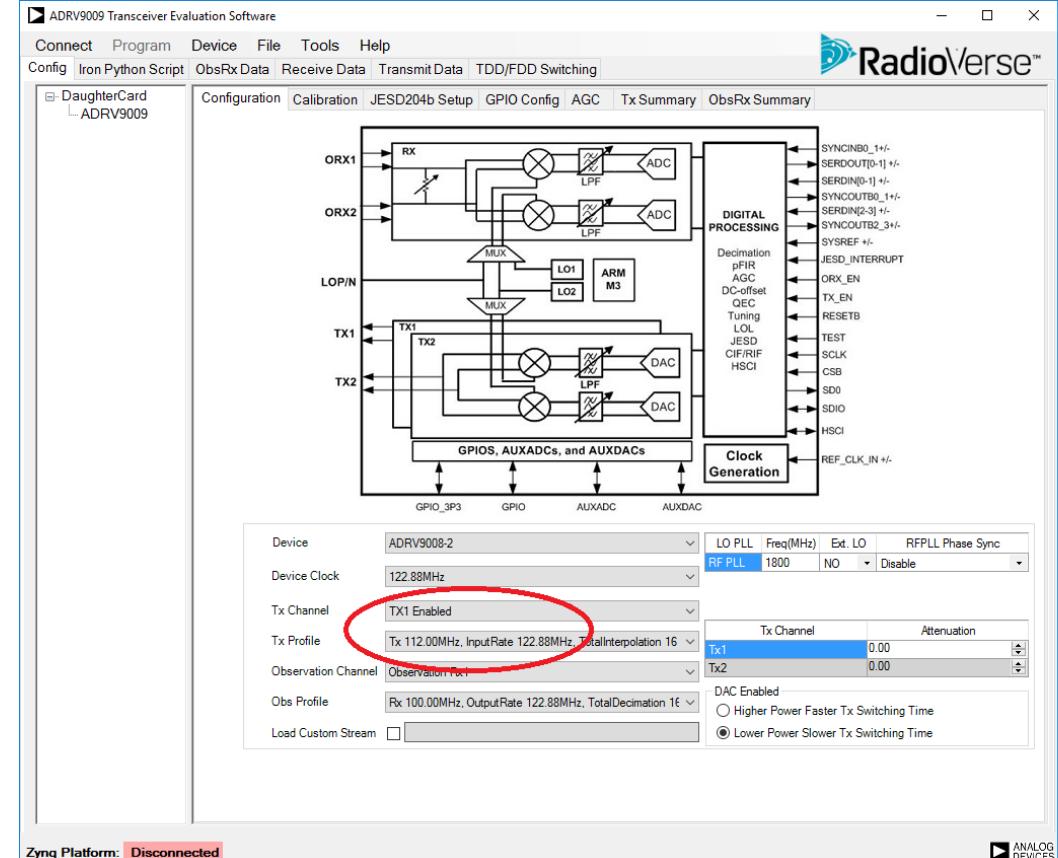
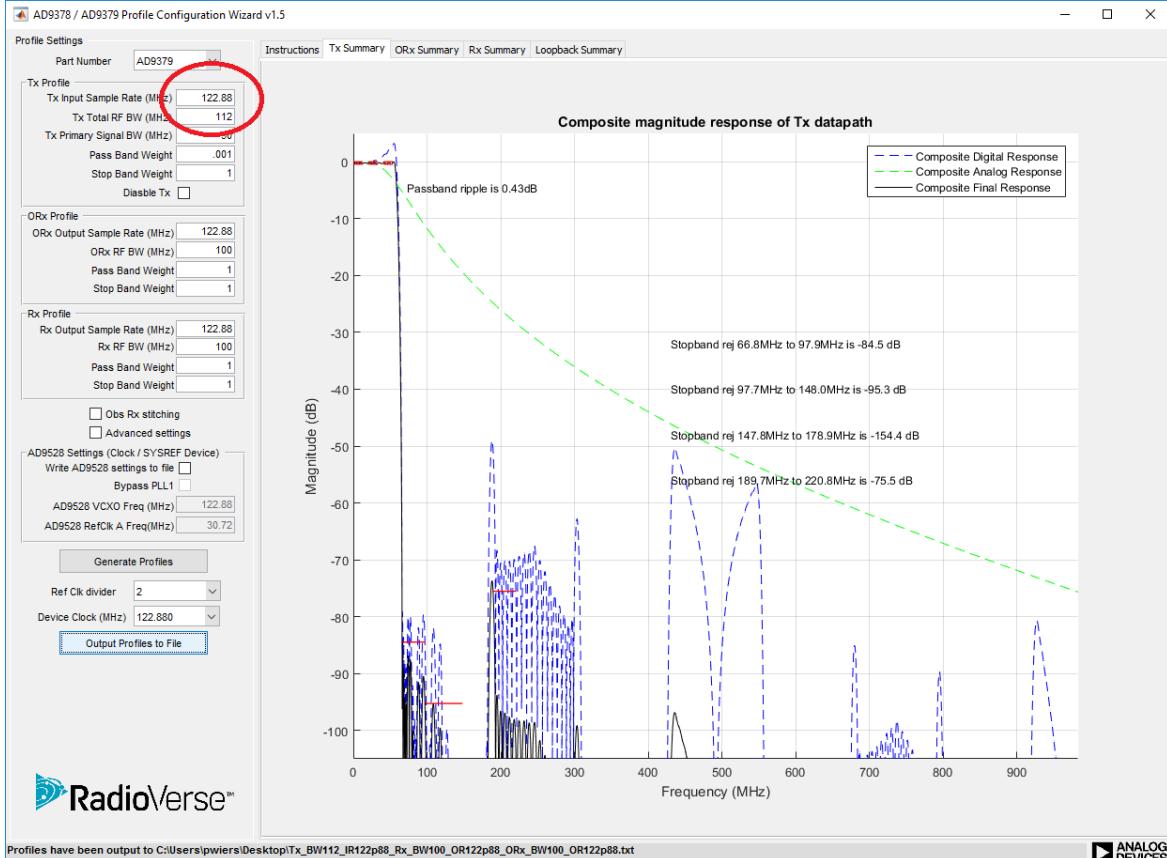
- ▶ Purposes
  - FIR filter generation
  - Profile generation—BW can affect ARM calibrations
    - Limitations on BW vs. sampling rate
  - ADC coefficient generation
- ▶ Note addition of a *Part Number Selection Box*
- ▶ Filter design parameters specified differently
  - BW and weighting—*ratio* is the critical parameter, not the absolute numbers
  - RF BW is total BW (both sides of LO)
- ▶ JESD204B ties data rate to DEVCLK rate
  - Embedded clock—same rate at both ends
  - Exactly same PLL rate (data rate) must be generated and used by both TRX and DBB
  - ClockPLL operates in integer mode
  - Multiplying/dividing DEVCLK generates options
    - 153.6 MSPS data rate can use 122.88 MHz DEVCLK
  - Customer may use any method to provide clock (and SYSREF)
- ▶ Source, MATLAB App, or exe options



# Using the Wizard Output with the TES GUI

- ▶ Use the Wizard to generate the desired profile(s)
- ▶ Verify that the clock settings (divider & frequency) are as desired
- ▶ Press the “Output Profiles to File” button and select a destination; change the filename if needed
- ▶ On the GUI, select “File” and then “Load Custom Profile”
- ▶ Browse to the file
  - There will be four of them
    - Select the file without “lpbkadc\_stf” (ADC signal transfer functions used to plot filter responses)
- ▶ Verify that the profile loads correctly, including the device clock frequency
- ▶ Adjust JESD, AGC, GPIO settings as needed, program, and proceed as usual
  - If the AD9528 VCXO frequency was set  $\neq$  122.88 MHz, verify that the EVB is configured correctly

# Using the Wizard Output with the TES GUI

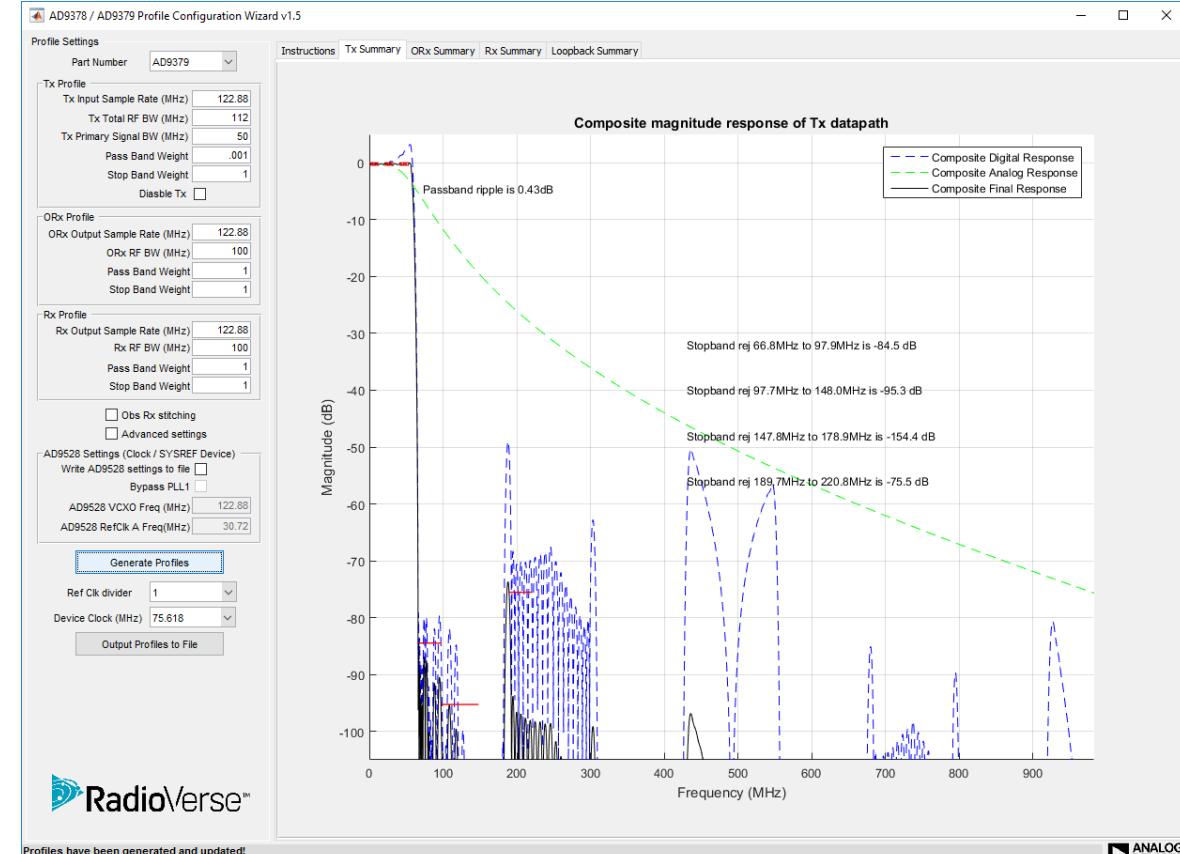
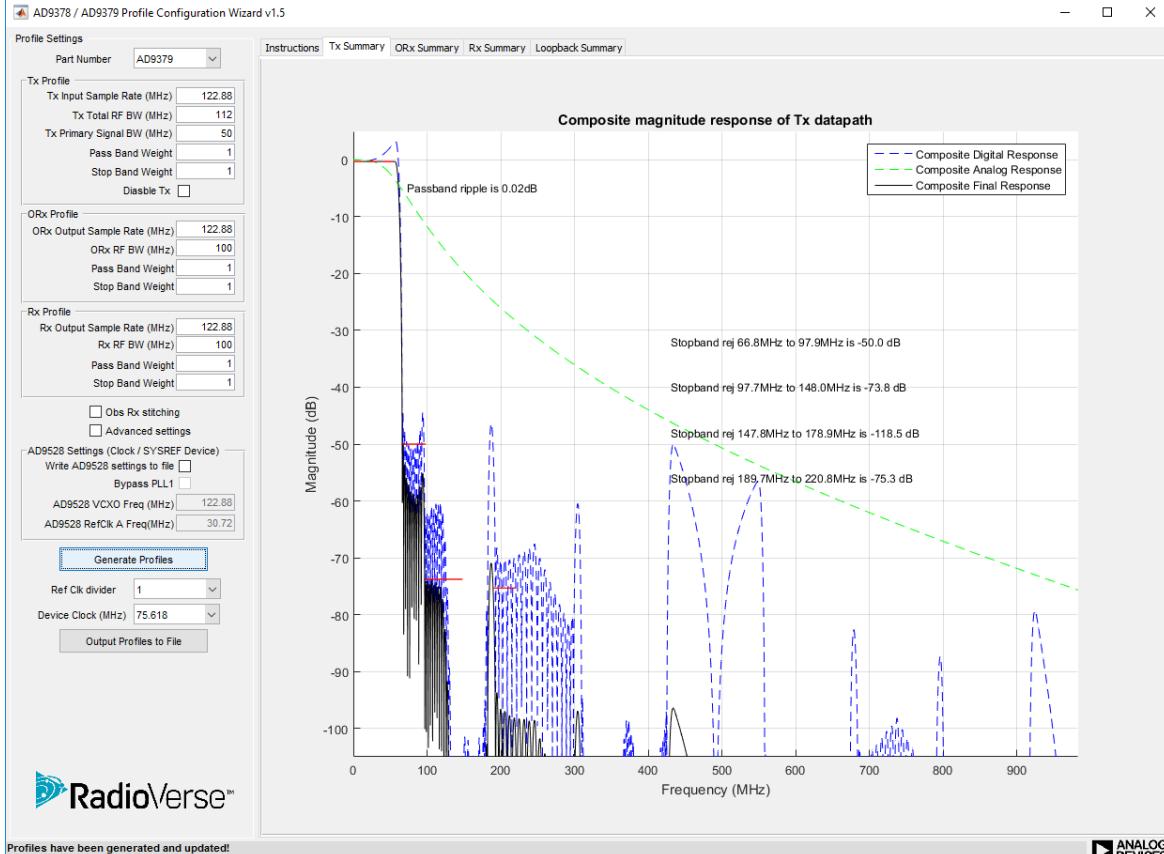


# How to Use Pass Band and Stop Band Weights

- Weights are used as a ratio to let the Wizard determine how much emphasis to place on reducing pass band ripple vs. improving out of band rejection
- Effectiveness is most easily demonstrated when the number of available FIR taps is not enough to achieve both excellent flatness and rejection
  - Most standard profiles achieve both but very low oversampling ratios will force the wizard to compromise one or both performance aspects
  - Change the ratio to provide more emphasis on one of the two aspects
  - The next slide uses two slides to demonstrate the use of weighting

# How to Use Pass Band and Stop Band Weights

(changing the ratio from 1:1 to 0.001:1, emphasizing stop band rejection)



# ADRV9009 Power Solution

# ADRV9009 Power and Clock Block Diagram

Note: ADRV9009 supply domains have been combined for clarity

Ferrite Beads are recommended to isolate aggressive nodes from sensitive nodes

## Choice of Two Power Management Solutions:

### ► ADP5054 Solution:

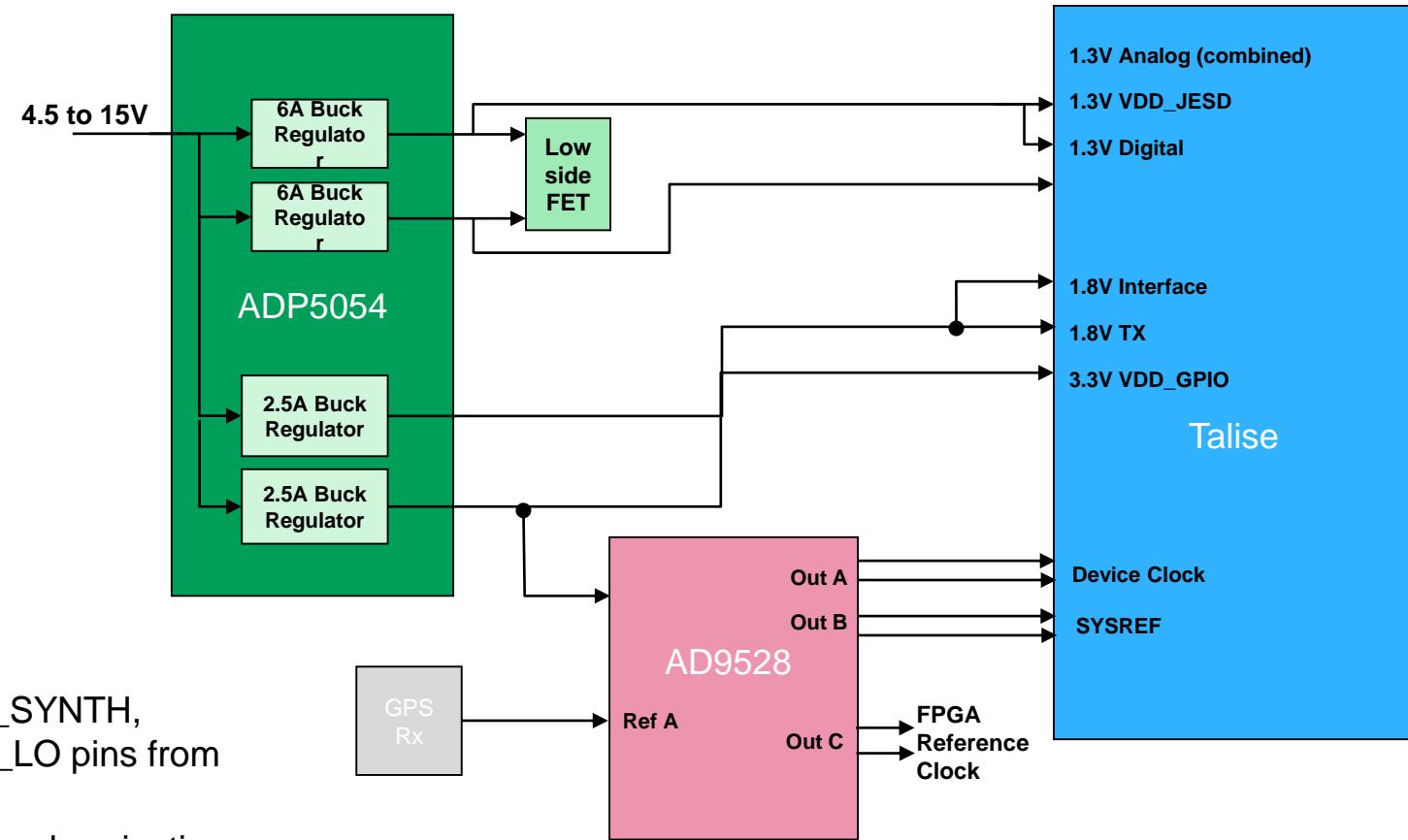
- Low Noise Buck
- Programmable Sequencing
- **Up to 15V Input**
- Higher current, can **power 2 ADRV9009**

### ► ADP5014 Solution:

- Low Noise Buck
- Programmable Sequencing
- **Up to 6V Input**
- Lower current, **power 1 ADRV9009**

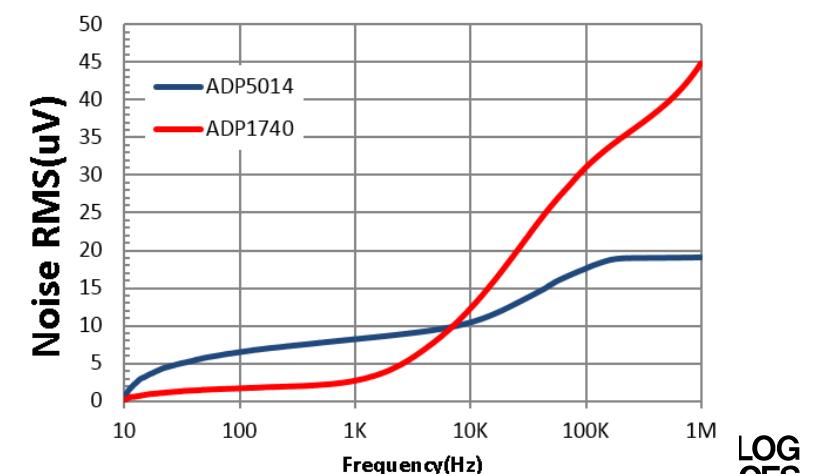
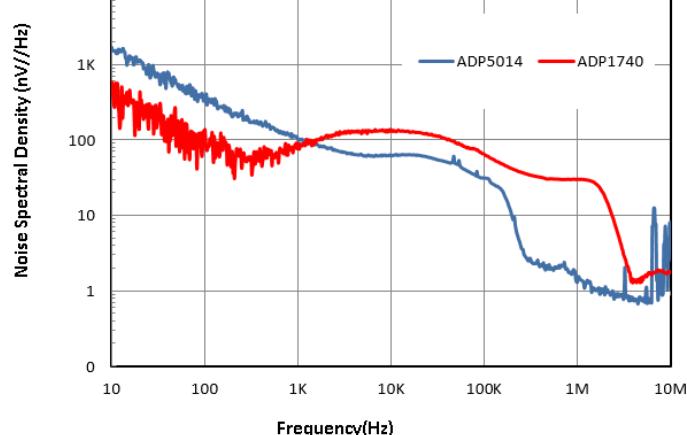
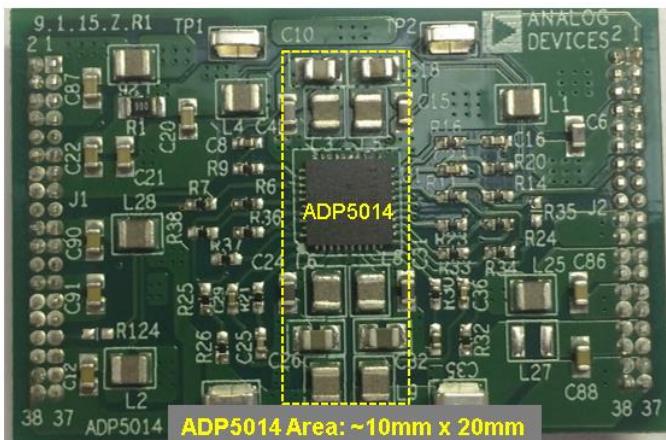
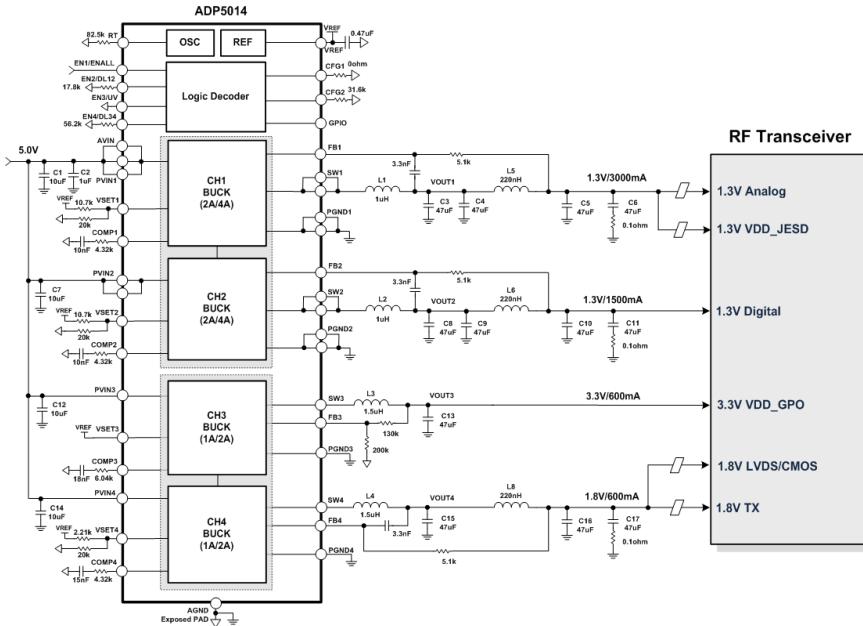
### ► If using Multi Chip Synchronization (MCS):

- Care must be taken to isolate the VDDA1P3\_RF\_SYNTH, VDDA1P3\_CLOCK\_SYNTH, and VDDA1P3\_RF\_LO pins from the VDDA\_1P3\_ANALOG supply.
- This isolation is critical to achieving best phase synchronization performance.



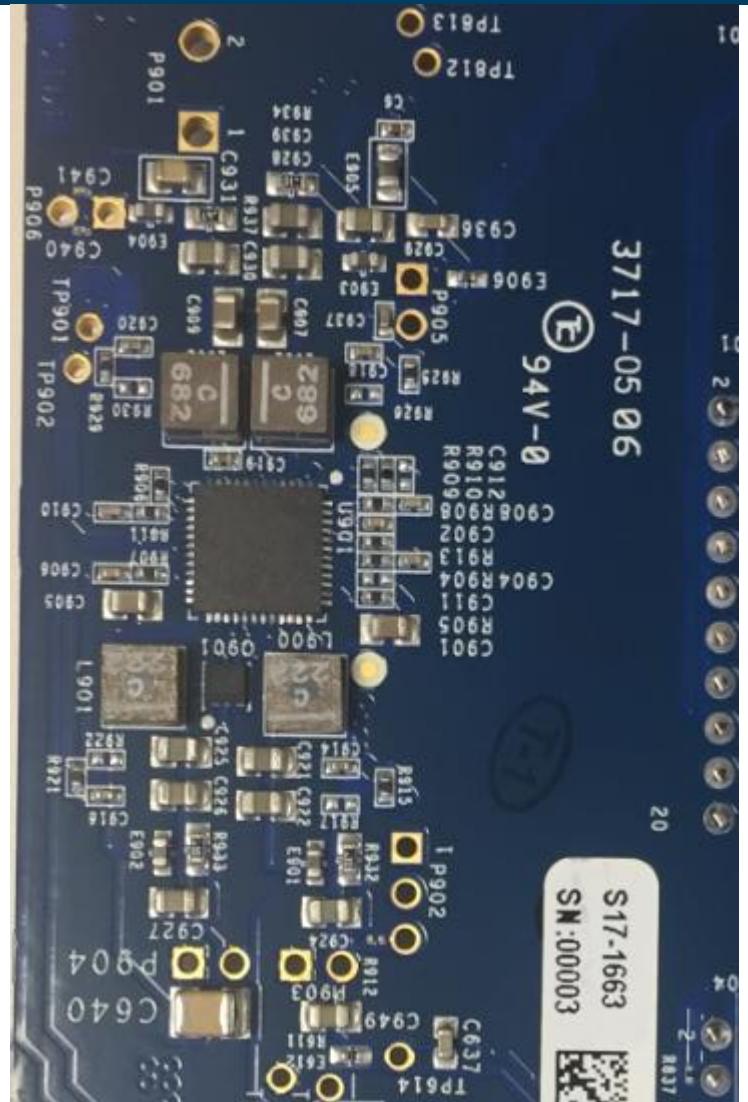
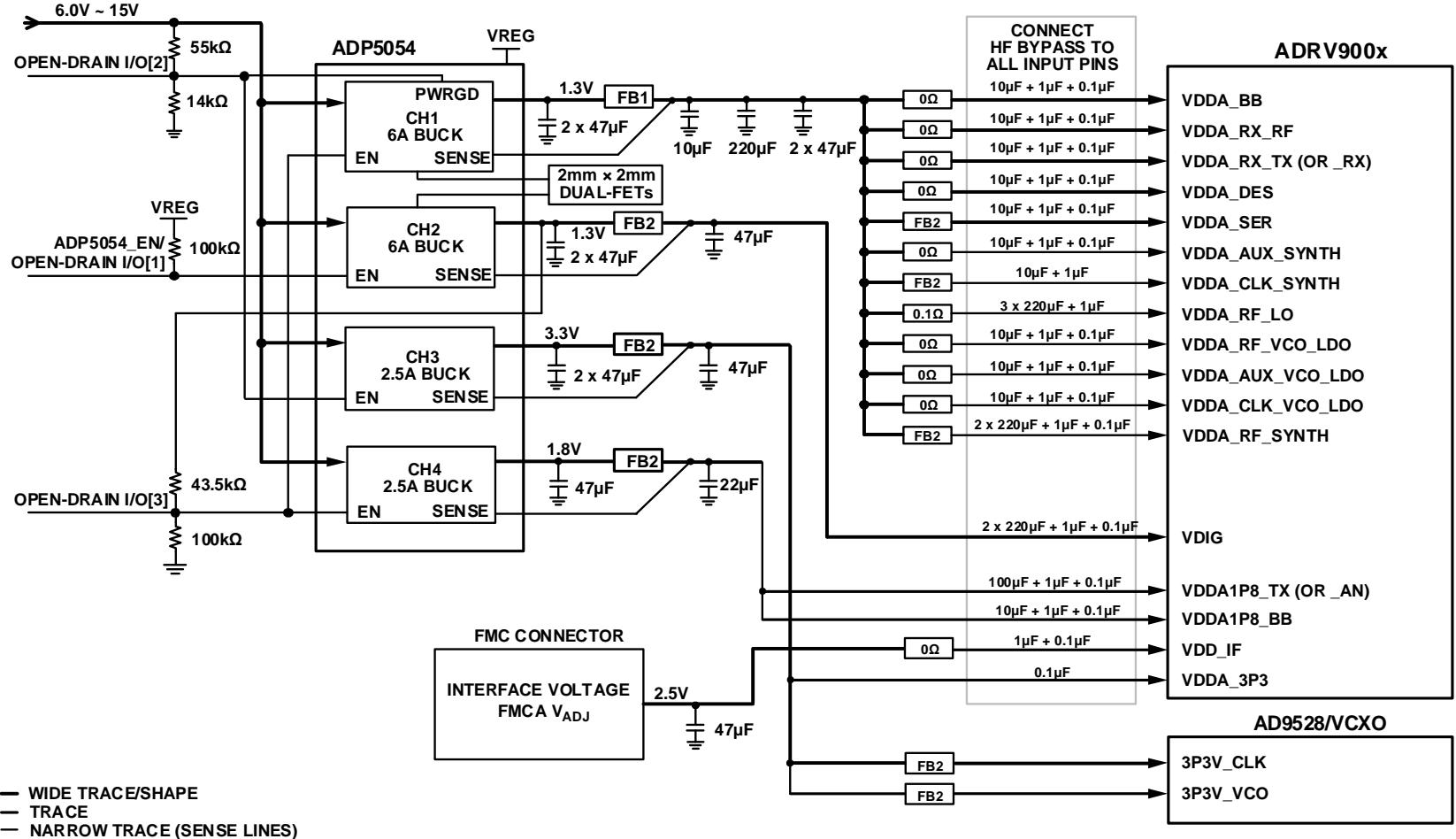
# ADP5014 to Power Up RF Transceiver (Mykonos/Talise)

## - “Low 1/f Noise” Buck Architecture

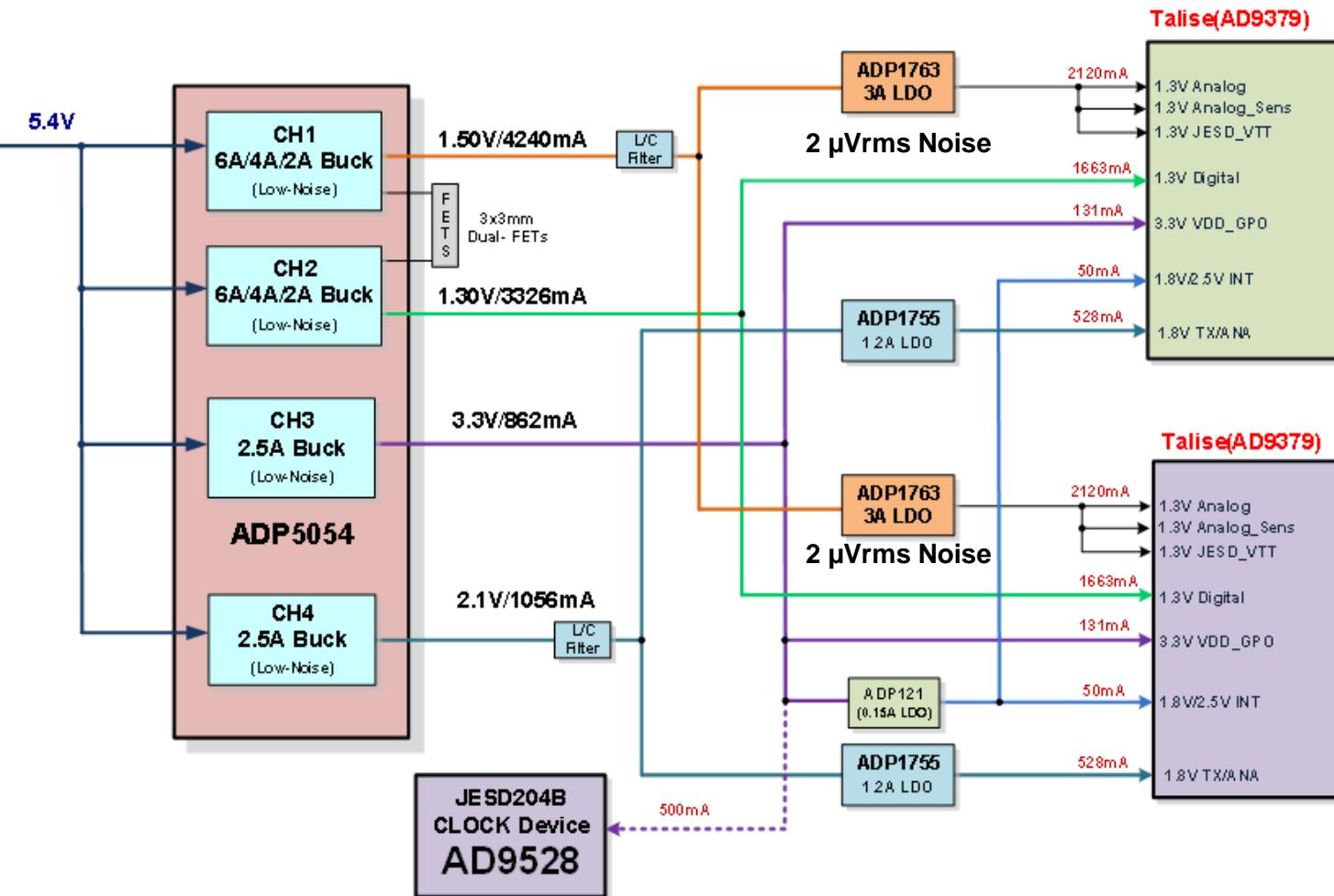


- ADP5014 provide excellent wideband noise
  - ~25 $\mu$ Vrms Noise with 2<sup>nd</sup> L/C filter
  - Better than ADP1740 (LDO) 1/f Noise
- Programmable Sequence Mode
  - 1V3\_DIG -> 1V3\_ANA -> 1.8V\_VDDA/3V3\_GPO
- Small Solution Size
- “1-to-1” attach to Mykonos/Talise

# Focus on ADRV9009 Individual Supply Domains



# uPMU + LDOs for Multiple RF TRX, e.g. 2x Talise/ADRV9009



- ADP1763 (3A Low-Noise LDO) to power up 1.3V analog, analog sensitive, JESD VTT rail
  - Careful ferrite isolation required for each sensitive pin
  - Please refer to Talise reference design
- Suggest to use individual LDO - ADP1755 for isolate each 1.8V TX/ANA at this moment
- Combine and supply 3.3V VDD GPO and 1.8V/2.5V Interface supply
- Sequence Implementation & Phase Synchronized in ADP5054
  - 1.3V DIG -> 1.3V ANA -> 1.8V\_TX/3.3V\_GPO