Design of Digital Systems Laboratory

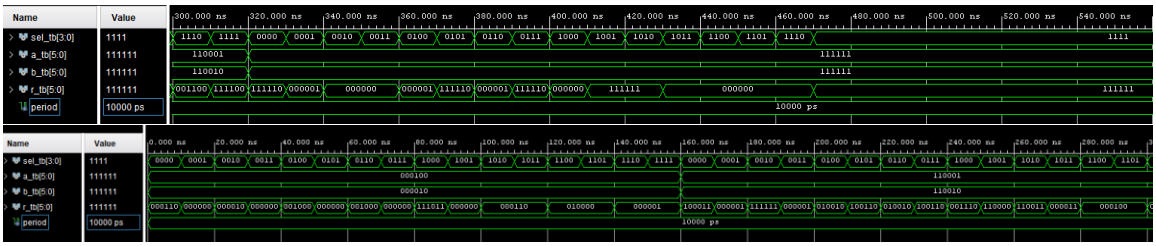
Lab 3

Jonathan Mazurkiewicz

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

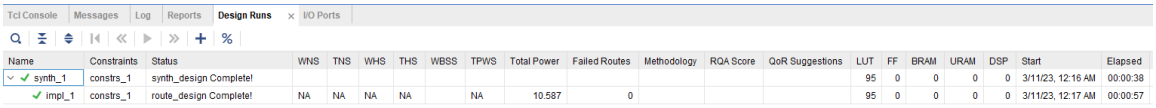
Your Signature: Jonathan Mazurkiewicz

Simulation Results



This lab is an Arithmetic Logic Unit (ALU). Using hardware, it is capable to perform adding, subtracting (both with or without carry), bitwise multiplication, bitwise Not, And, Or, and Xor, SLL, SRL, and SRA. By changing the value of select, we can determine which one of the operations we want to use.

Area Implementation



Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed
synth_1	constrs_1	synth_design Complete!												95	0	0	0	0	3/11/23, 12:16 AM	00:00:38
impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA		NA	10.587	0				95	0	0	0	0	3/11/23, 12:17 AM	00:00:57

Timing Implementation

n/a

Video Explanation

https://youtu.be/RpFWmpQyUb4