Design of Digital Systems Laboratory

Lab 4

Jonathan Mazurkiewicz

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: Jonathan Mazurkiewicz

Simulation Results

```
# }
WARNING: Simulation object /mult_tb/MULT_FILE was not traceable in the design for the following reason:
Vivado Simulator does not yet support tracing of VHDL variables.
# run 100000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'mult_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 100000ns
launch_simulation: Time (s): cpu = 00:00:01 ; elapsed = 00:00:06 . Memory (MB): peak = 1560.730 ; gain = 0.000
run all
Note: Simulation complete
Time: 1310720 ns  Iteration: 0  Process: /mult_tb/tb  File: C:/Users/jonma/OneDrive - Florida Atlantic University/Desktop/CDA 4240C/lab_4/lab_4.srcs/sim_1/new/mult_tb.vhd
```

This lab takes two 8 bit inputs, implements a carry save multiplier, and outputs a 16 bit result. The 16 switches are the inputs and the 16 LEDs are the output.

Area Implementation

Tcl Console | Messages | Log | Reports | **Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed
synth_1	constrs_1	synth_design Complete!												109	32	0	0	0	4/2/23, 2:25 PM	00:00:35
impl_1	constrs_1	Running write_bitstream...	2.308	0.000	0.303	0.000		0.000	0.136	0	32 Warn			109	32	0	0	0	4/2/23, 2:26 PM	00:01:02

Timing Implementation

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.733 ns	Worst Hold Slack (WHS):	0.191 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	16	Total Number of Endpoints:	16	Total Number of Endpoints:	33

All user specified timing constraints are met.

Video Explanation

https://youtu.be/yfTE1AtAJqE