Design of Digital Systems Laboratory

Lab 2

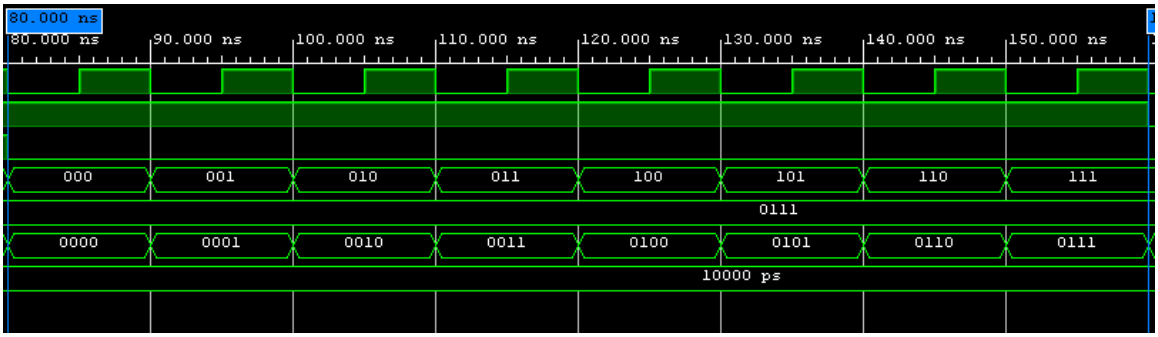
Jonathan Mazurkiewicz

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

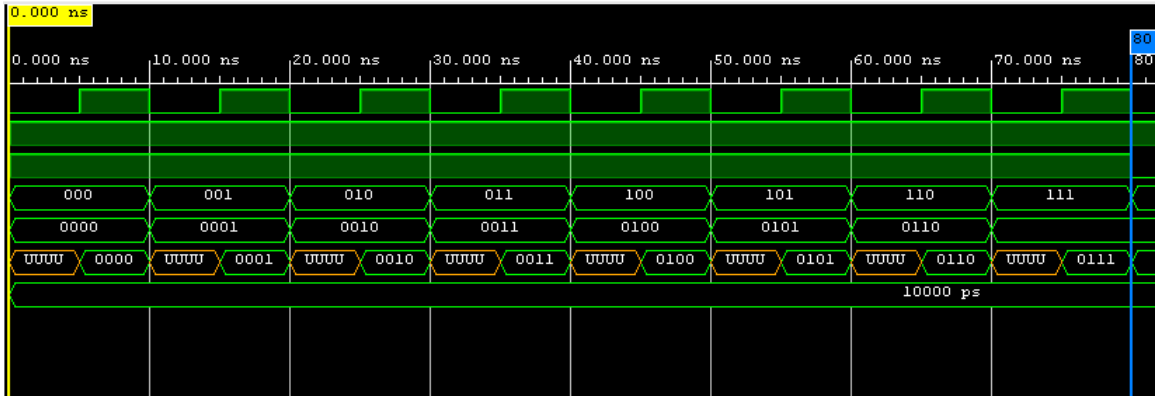
Your Signature: Jonathan Mazurkiewicz

Simulation Results

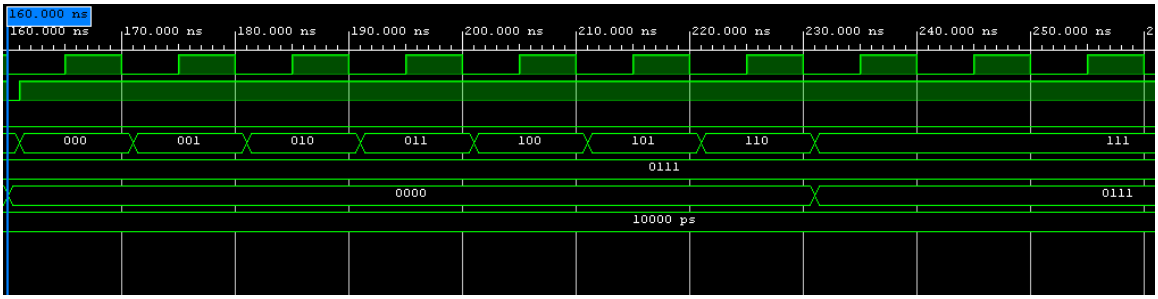
--Read



--Write



--Reset



This lab is a register file. It contains 8 separate registers that have the capability to store data of 4 bits. (Generics were used to change the size of each register at a later time). Write enable allows writing to be done, otherwise, we will read from the registers. An address of 3 bits is fed into a decoder that selects which register will be accessed. Then, whichever address is selected along with the data from the register can be used to read from the registers. Reset clears all registers.

Area Implementation

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed
✓ synth_1	constrs_1	synth_design Complete!												17	32	0	0	0	2/16/23, 11:29 AM	00:00:36
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA		NA	4.426	0	32 CW			17	32	0	0	0	2/16/23, 11:31 AM	00:01:04

Timing Implementation

n/a

Video Explanation

https://youtu.be/sJmkrrj4DsQ