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A Novel Hybrid CMOS-Memristor Based 2-Bit Magnitude Comparator using Memristor Ratioed Logic Universal Gate for Low Power Applications

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***Abstract* — In recent years, memristor-based digital circuit design has become one of the prime focuses for low power, area-efficient VLSI design. A comparator is a combinational circuit used in complex ALU for the comparison of n-bit numbers. The unique hybrid 2bit CMOS-based comparator with Memristor Ratioed Logic Universal Gates has been implemented in this study (MRLUG). The proposed 2-bit magnitude comparator is verified by theoretical analysis and SPICE simulations. The area on-chip and power analysis are performed and the results are compared with conventional CMOS logic and threshold logic-based magnitude comparator. The feasibility of the proposed design is analyzed using LTSPICE and simulation results show an average power consumption of 39.92µW and 32.14% improvement in the area compared to resistive threshold logic (RTL).**

Keywords— Memristor, MRL, Comparator, SPICE

I. INTRODUCTION

Nowadays, due to increase in the usage of portable consumer electronics, low power designs become crucial. The market demand for chip design concentrates mainly on (i) Low power (ii) High speed (iii) Less area on-chip. Intensified research proves that memristors are one of the promising alternate solutions for nearing obsolesce of CMOS technology [1]. The binary comparator plays a major role in multiprocessing and parallel computing. In traditional CMOS method, the logic function is implemented using both PMOS and NMOS transistors, but the application of large number of inputs results in circuit complexity and degraded operating speed. Even though, the CMOS technology leads to the innovation of several logic design styles like Pass Transistor Logic (PTL), Pseudo NMOS logic style and Transmission Gates, the use of MOSFET is nearing its obsolence. A memristor is a non-volatile, 2-terminal nano sized alternative device for MOSFET with unique characteristics of computing and storing simultaneously for unconventional computational framework. The logic styles based on memristors like IMPLY logic, RTL [2] and MRL etc., is explored for the implementation of digital logic circuits. The proposed 2-bit comparator is designed based on hybrid CMOS-memristive logic based on MRL. The idea of hybrid CMOS-memristive logic based on Memristor Ratioed Logic (MRL) [3] implements AND and OR gates with only memristors, but NOT gate requires CMOS inverter. In MRL, the logic value is represented as voltage, whereas memristance is represented as logic value in IMPLY logic.

II. MEMRISTOR DEVICE MODEL

The proposed idea of memristor based basic logic gates and comparator circuit employs bipolar switching of memristor regulated with threshold voltage [4]. The model proposed has three characteristics namely, electron tunneling, non-linear drift for oxygen vacancy, and a voltage threshold for motion of state variable. The IV characteristics rely on internal state x(t) = (0,1) and x(t) directly impacts conductivity. The parameters a1, a2 and b have been set to fit the following condition:

$$I(t) = \begin{cases} a1x(t)sinh\left(b(V(t)\right), V(t) \geq 0 \\ a2x(t)sinh\left(b(V(t)\right), V(t) < 0 \end{cases}$$

The internal state variable satisfies the condition:

$$\frac{dx}{dt} = g(v)f(x)$$

$$g(v) = \begin{cases} Ap\left(e^{V(t)} - e^{Vp}\right), V(t) > Vp \\ -An\left(e^{-V(t)} - e^{Vn}\right), V(t) < Vn \\ 0, -Vn < V(t) < Vp \end{cases}$$

The function f(x) splits the variable movement into two areas dependent on the current state variable. The parameters x_p, x_n, α_p, and αn are needed for model to fit dynamics of few other types of devices.

$$f(x) = \begin{cases} e^{-\alpha p(x-x_p)}\omega_p(x, x_p), x \geq x_p \\ 1, x < x_p \end{cases}$$

$$f(x) = \begin{cases} e^{-\alpha n(x+x_n-1)}\omega_n(x, x_n), x \leq 1 - x_n \\ 1, x > 1 - x_n \end{cases}$$

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where,

$$\omega_p(x, x_p) = \frac{x_p - x}{1 - x_p} + 1$$

$$\omega_n(x, x_n) = \frac{x}{1 - x_n}$$

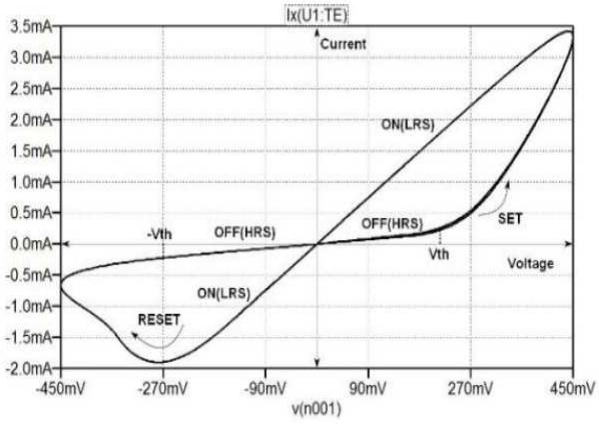

Fig. 1. IV characteristics of memristor

Fig. 3 is the IV characteristics of the aforementioned memristor model. If the voltage is higher than the positive voltage threshold Vp, the memory will move on from RHS (Resistance High State) to RLS (Resistance Low State). Likewise, the memorial shifts from RLS to RHS, when the voltage provided is larger compared to the adverse threshold voltage Vn.

III. MRL LOGIC

Memristor is the fourth passive component relating charge and flux. In MRL logic family [5], the input and output are represented as voltage levels which is compatible with conventional CMOS logic. The memristive components are exclusively used only for computing and not for saving the outputs as in IMPLY logic [6]. The MRL AND and OR gates are formed by two series memristor with opposite polarities as shown in Fig.3. An additional inverter is used to design NAND and NOR gates [7]. The drop between input voltages is zero for identical inputs and hence the output equals voltage of the input. For non-identical inputs, there is a current flow from top to bottom electrode with high voltage to low voltage, thus by altering the memristance of both devices.

In case of OR logic, if one input is logic 0(RHS) and other input is logic 1(RLS), at the computational end, the resistance of two devices is around R_{ON} and R_{OFF} respectively. The initial memristance has no out-turn on the end computation result.

Assume $R_{OFF} >> R_{ON}$, the resultant voltage of OR gate is set on by voltage divider rule in-between two memristive devices.

$$V_{out,or} = \frac{R_{off}}{R_{off} + R_{on}} V_{high} \approx V_{high}$$

In case of AND gate, the voltage output equation is

$$V_{out,and} = \frac{R_{on}}{R_{off} + R_{on}} V_{high} \approx 0$$

The static power consumption is approximately,

$$P_{Static} = \frac{V_{high}^2}{R_{off} + R_{on}}$$

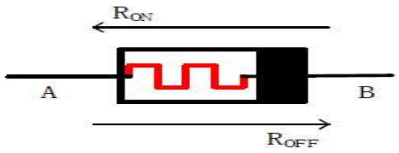

Fig. 2. Memristor symbol

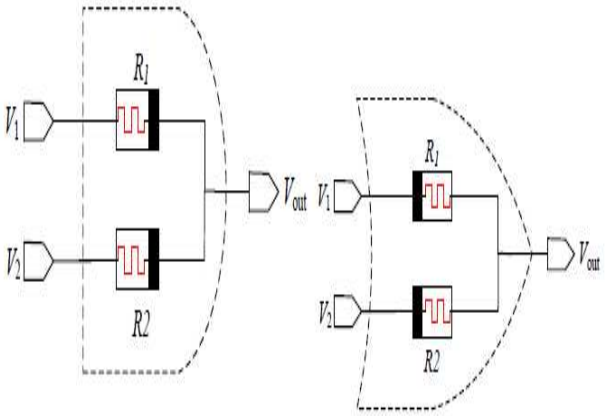

Fig.. 3. MRL AND and OR gates

IV. UNIVERSAL GATE

MRL Universal gate [9] is constructed from hybrid CMOS memristor concept with 4 memristors and a CMOS inverter. The source of PMOS is connected with MRL OR gate and MRL AND gate is connected to CMOS inverter input. The CMOS inverter output results in ex-or gate. Thus, MRL UG produces three output AND, OR, XOR [8]. Similarly, for XNOR gate, the source of NMOS is connected with MRL AND gate and input of the CMOS inverter is connected with MRL OR gate. The logic circuit and simulated results of XOR and XNOR are as follows:

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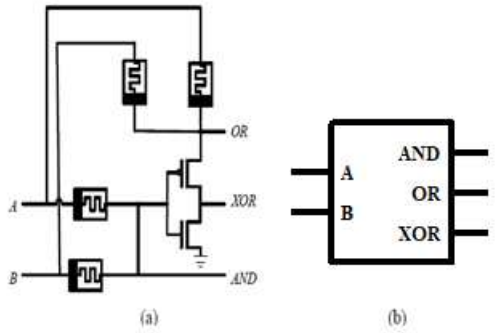

Fig. 4. MRL UG XOR gate

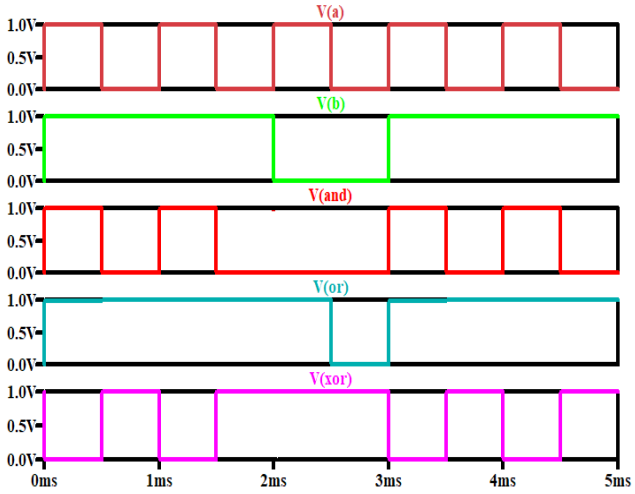

Fig. 5. Simulation results of MRL UG XOR gates

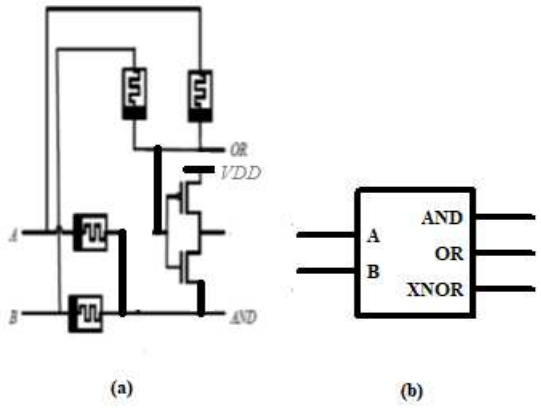

Fig. 6. MRL UG XNOR gate

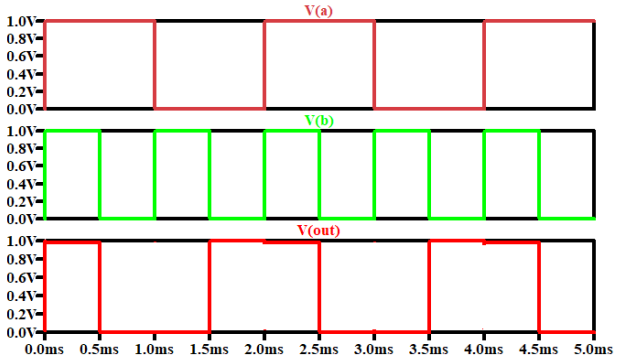

Fig. 7. Simulation results of MRL UG XNOR gates

V. MRL UG BASED 2-BIT MAGNITUDE COMPARATOR

Magnitude comparator is the fundamental block for ALU, where ALU is the basic functional unit of Digital Signal processor. To determine the Most Significant Bit, see if A>B, A<B or A=B (MSB). If MSB is different from both inputs, For example, when MSB is A = 1 and MSB is B = 0, output is A > B and the opposite is A < B. If both inputs have same MSB, move to the next bit, and then continue to compare the next input bits to LSB. If the inputs are identical, then the bits are A=B. The 2-bit digital comparator results are presented in TABLE 1, for several input combinations.

TABLE I. TRUTH TABLE OF 2-BIT MAGNITUDE COMPARATOR

Input Bits				Output Bits		
A2	A1	B2	B1	A=B (AEB)	A>B (AGB)	A<B (ALB)
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

The equations are as follows depending on the varied input conditions:

AGB := A2B2 + A1B1(A2 ʘ B2) := A2 B2 + A1B1(X2)
AEB := (A2 ʘ B2)(A1 ʘ B1) := X2 X1
ALB := A2B2 + A1B1(A2 ʘ B2):= A2B2 + A1B1(X2)
Where,
A2 ʘ B2 = X2
A1 ʘ B1 = X1

The block diagram of proposed hybrid CMOS memristor based 2-bit magnitude comparator is as follows:

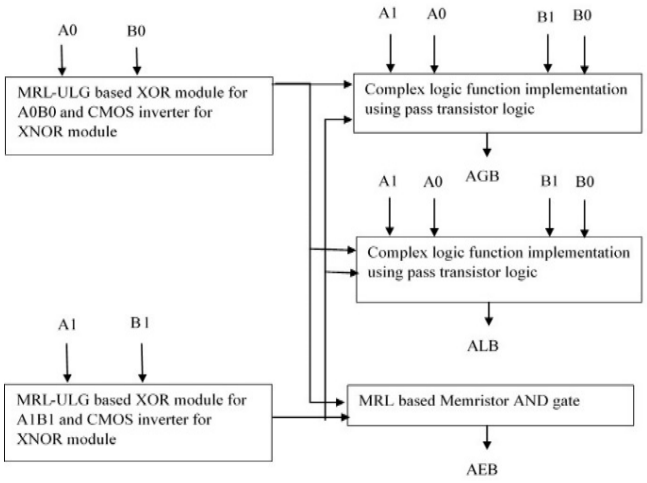

FIG. 8. Block diagram of proposed hybrid CMOS Memristor based 2-bit Magnitude Comparator

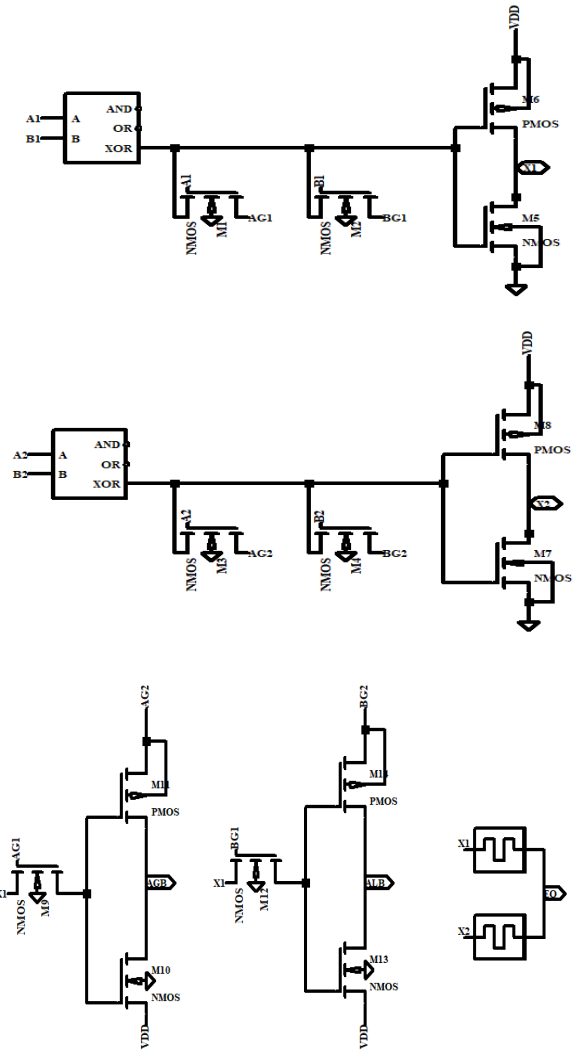

Fig. 9. Schematic diagram of 2-bit Digital Comparator

VI. SIMULATION SETUP

The proposed magnitude comparator is simulated using LTSPICE. The model described above has the following parameters. The model parameters are: Vp = 0.16V, Vn = 0.15V, Ap = 4000, An = 4000, xp = 0.3, xn = 0.5, αp = 1, a1 = 0.17, a2 = 0.17, b = 0.05, x0 = 0.11. V(A2), V(A1) , V(B2) and V(B1) are the input voltages. The output voltages are V(EQ) when all the inputs are equal. If A>B then V(AGB) is the voltage output and if A<B, then V(ALB) is voltage output.

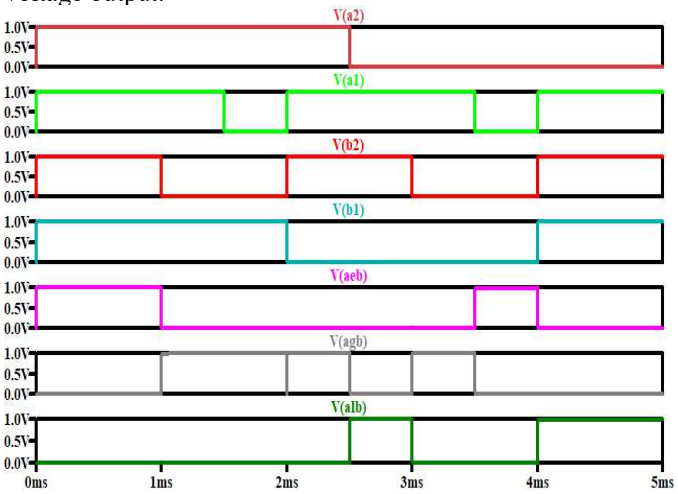

Fig. 10. Simulation waveform for 2-bit Magnitude Comparator

Using MRLUG the number of memristors are reduced and proposed design has 10 memristors and 18 transistors. The proposed magnitude comparator reduces power consumption, area and computational complexity. The memristor size is about 3 nm, while the size of the CMOS is 180 µm. The average static power consumption of proposed 2-bit comparator logic is tabulated as follows.

TABLE II. COMPARISON OF POWER DISSIPATION OF 2-BIT MAGNITUDE COMPARATOR

S.No	Logic Styles	Power
1.	Conventional CMOS Logic	49.125 µW
2.	Resistive Threshold logic [10]	154.26µW
3.	Proposed Hybrid CMOS Memristor logic	39.92 µW

Compared to resistive threshold logic, the proposed 2-bit magnitude comparator shows an improvement of 32.14% in area.

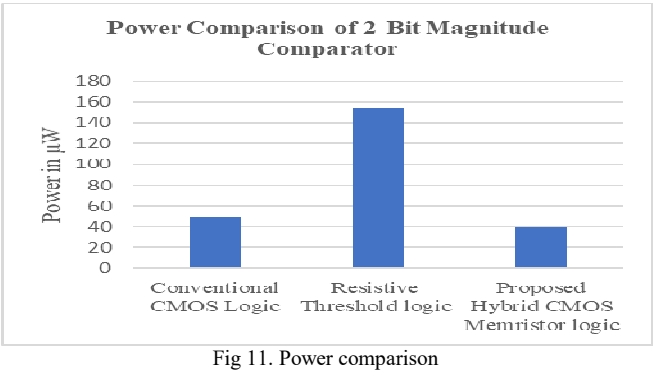

Fig 11. Power comparison

TABLE III. COMPARISON OF TRANSISTOR COUNTS FOR THREE DIFFERENT LOGIC STYLES

	No. of bits	Conventional CMOS Logic	Resistive Threshold logic [10]	Proposed Hybrid CMOS Memristor logic
No. of transistors	1	26	18	6
No. of memristors		Nil	15	4
No. of transistors	2	120	56	18
No. of memristors		Nil	55	10

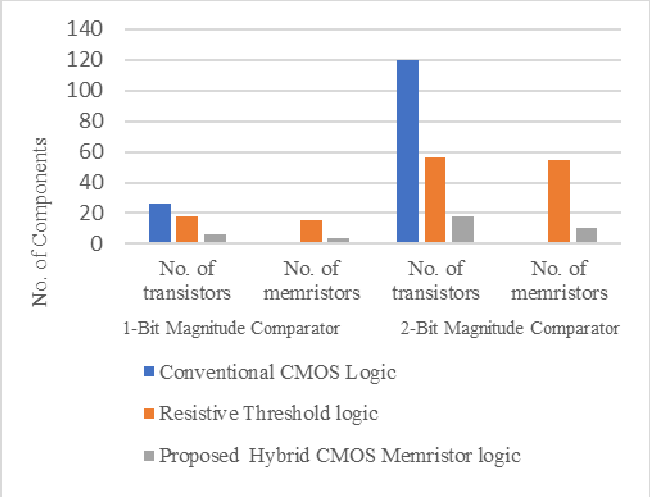

Fig 12. Comparison of transistor counts

VII. CONCLUSION

This work proposes a two-bit efficient, MRLUG-built CMOS-compatible digital comparator, consistent with the standard CMOS system. The design provided shows to be area and power efficient. The reduction in area results in less interconnect requirement which leads to reduced cross talk effect [11]. In addition, it is possible to increase the design to a comparator of multi- bit size. As the size of the comparator increases, there exists voltage degradation problem in complex cascaded structures [12]. The voltage degradation problem can be overcome by modifying our proposed design using multi-input MRL gate.

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