MOSFET-Based Memristor for High-Frequency Signal Processing

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***Abstract*— This research article proposes a floating memristor emulator configuration based on n-type MOSFETs only. The proposed memristor comprises three nMOS and an extra nMOS for an external grounded capacitor. Compared to the existing literature, the proposed floating MOS memristor enables a simple design without any sophisticated design complexity. The actual fingerprint of the memristor as a pinched hysteresis loop with different frequency domains and composite characteristics as incremental and decremental are well examined using computer simulation with 90-nm CMOS technology parameters for MOSFETs. The power consumed by the proposed circuit is 2.6 μW. In addition, an experimental test using off-the-shelf components is investigated to verify the theoretical and simulated results. Moreover, the proposed nMOS-memristor emulator application is suitable for the modulation and demodulation of binary frequency-shift keying (BFSK) and Boolean logic gates.**

***Index Terms*— Floating memristor emulator, frequency analysis, memristor, MOSFET, pinched hysteresis loop.**

I. Introduction

CHUA [1] first introduces the fourth circuit element after fundamental passive components in 1971, presenting the missing constitutive relation between charge and flux. After the invention of the memristor, the first successful fabrication of a fundamental nanoscale memristor by HP Labs came in 2008 [2]. The boost provided by HP lab for the memristor design is now a trend for the research community to implement high-performance memristor. An intensive investigation has been dedicated to complement memristor-based inherent applications as resistive random access memory (RRAM) [3]–[5], analog circuits [6], digital circuits [7], [8], chaotic circuits [9], [10], neural networks [11]–[13], and few more, but the memristor fabrication is still a challenging task due to very sophisticated design procedures and cost issues that limit the real-time applications. The Knowm memristor [14] is commercially available, but still, there is a scope for more research in this domain. Bio-inspired technologies have launched the world's first commercially accessible memristor [15] and are suitable only for specific circumstances to avoid irreversible damage. Therefore, memristor emulators are being designed to imitate its attributes using analog building blocks, such as second generation current conveyor (CCII) [16], [17], operational transconductance amplifier (OTA) [18], current feedback operational amplifier (CFOA) [19], differential difference current conveyor (DDCC) [20], current conveyor transconductance amplifier (CCTA) [21], and so on. A charged control emulator model for memristor and memcapacitor using CCIIs and an analog multiplier is reported in [22]. Another memristor emulator using electronically tunable DDCC, one multiplier, two resistors, and a grounded capacitor is also available, but [22] comes with a maximum number of component counts. Floating and grounded memristor emulators using differential voltage CCTA (DVCCTA), three resistors, and a capacitor have been reported [23]. A floating memristor is realized by employing a voltage differencing transconductance amplifier (VDTA), one multiplier, two resistors, and a capacitor with incremental and decremental configurations reported in [24]. The memristor emulator reported in [25] uses four CFOAs, two multipliers, and nine resistors that operate only up to 10-Hz frequency. Recently, a memristor emulator was reported using OTA, current differencing buffered amplifier (CDBA), and a capacitor that operates up to 1-MHz frequency [26]. The emulator presented in [27] and [28] can well imitate the features of the TiO_2 memristor. However, the circuits are complex and use an analog multiplier and several operational amplifiers, resistors, and MOS transistors.

By analyzing the available physical and performance characteristics, a summary of the proposed work with the earlier reported work as per Table I is illustrated below.

1) The passive component count is more in [18], [19], [23], [30]–[33], and [35]–[41].
2) The total number of transistors used in the proposed work is much less than in [19], [23]–[32], and [34]–[40].

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TABLE I
COMPARATIVE ANALYSIS OF THE PROPOSED WORK WITH PREVIOUSLY REPORTED WORK

Ref. (Fig. No.)	No. of Components	Transistor Count	Technology Used	Passive component Count	Floating/ Grounded	Operating Frequency	Power Consumption	Input voltage (peak to peak)	Experimental Results
[19] (Fig. 5)	DDCC-1, Multiplier-1	50	0.35µm CMOS	C-1,R-2	Floating	1MHz	74.5mW	50mV	No
[23] (Fig. 4)	DVCCTA-1	29	0.5µm CMOS	C-1, R-3	Grounded	1MHz	--	--	Yes
[29] (Fig. 2)	VDTA - 1, MOS-CAP-1	17	0.18µm CMOS	0	Grounded	50MHz	--	--	Yes
[30] (Fig. 1)	OTA-1, MOSFET-2	16	0.18µm CMOS	C-1	Floating	Few Hz	--	--	No
[31] (Fig. 1)	VDTA - 1, MOSFET- 2	19	0.18µm CMOS	C-1, R-1	Floating	50MHz	1.34mW	200mV	Yes
[32] (Fig. 1)	MOSFETs	7	0.18µm CMOS	C-1	Grounded	50MHz	--	--	Yes
[33] (Fig. 1)	MOSFETs	3	--	C-2, R-2	Grounded	Few kHz	--		Yes
[18] (Fig. 1)	OTAs - 3, CCIIs - 4	--	--	C-1, R-3	Floating	10kHz	1.2 µW	100mV	Yes
[34] (Fig. 2)	MOSFETs	7	0.13µm CMOS	--	Floating	1MHz	--	--	No
[35] (Fig. 1)	CFOA-2, OTA-1	>56	--	C-2,R-3	Grounded	Few KHz	260mW	2V	Yes
[36] (Fig. 1)	AD844-1, Multiplier-1	>40	--	C-1,R-3	Grounded	860kHz	204mW	2V	Yes
[37] (Fig. 13)	Subtractor-1, Adder-1	12	0.25µm CMOS	C-1, R-1, NR-1	Grounded	Few Hz	4.51mW	± 1.25V	No
[38] (Fig. 2)	MO-OTA-1, Multiplier-1	38	0.18µm TSMC CMOS	C-1,R-1	Grounded	Few kHz	--	100mV	Yes
[39] (Fig. 3)	CBTA-1, Multiplier	23	0.18µm TSMC CMOS	C-1,R-2	Grounded	460kHz	--	0.5V	No
[40] (Fig. 6)	OTA - 2	17	CNTFET	C-1	Both	10 MHz	--	0.3V	No
[41] (Fig. 2)	MOSFETs	3	0.18µm TSMC CMOS	C-1	Floating	13 MHz	6.725nW	1V	Yes
Proposed work (Fig. 1)	nMOS-3, MOS-CAP-1	4	90nm GPDK CMOS	0	Floating	50MHz	2.6 µW	1.3V	Yes

3) There is no experimental verification in [19], [30], [34], [37], [39], and [40].
4) The low operating frequency in [18], [19], and [23], [33]–[41] compared to the proposed work.
5) Power dissipation of the proposed work is small compared to the work reported in [19], [31], and [35]–[37].

This work presents a floating memristor emulator configuration that uses three nMOS and one nMOS for the grounded capacitor. The rest of this research article is structured as follows: a complete theoretical description of the proposed memristor emulator is presented in Section II. The performance evaluation of the proposed memristor is examined by both simulation and experimental tests in Section III. In addition to the viability test, Section IV includes the application perspective of the proposed memristor as modulation and demodulation of the BFSK process and logic gates. Finally, this article ends with a conclusion in Section V.

II. PROPOSED MEMRISTOR EMULATOR IMPLEMENTATION

A MOS-based realization of the proposed floating memristor emulator is shown in Fig. 1, which comprises three nMOS with one MOS capacitor. Body of the all nMOS transistors is connected to the drain for nonlinearity.

The differential input voltage $V_{\text{in}}(t) = V_1 - V_2$ is applied across the drain terminal of transistors $M1$ and $M2$, respectively, and the corresponding input voltage magnitude is considered as $V_1 = -V_2 = V_{\text{in}}(t)/2$. To evaluate the control voltage (V_0), the transistors are operating in the linear region with constant threshold voltage for all nMOS and metal oxide semiconductor field effect transistor-capacitance (MOS-CAP) functions as an ideal capacitor. The current (I_C) across the MOS-CAP can be approximated as

$$I_C = C\frac{dV_O}{dt}. \tag{1}$$

The gate voltage of $M3$ can be found by applying Kirchhoff's voltage law at nodes 1–3 as

$$\begin{aligned} &V_1 - V_{\text{DS}_1} - V_{\text{DS}_2} - V_2 = 0 \\ &V_1 - V_{\text{DS}_1} + V_{\text{SD}_2} - V_2 = 0 \\ &V_1 - (V_1 - V_3) + (V_3 - V_2) - V_2 = 0. \end{aligned} \tag{2}$$

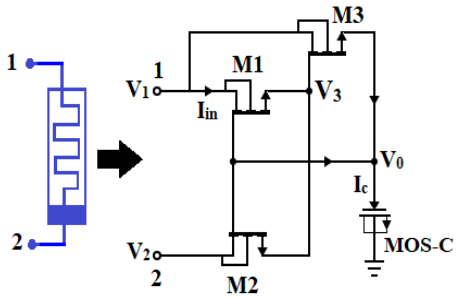

Fig. 1. Proposed memristor emulator using nMOS.

For simplification, that gives

$$V_3 = -\frac{V_{\text{in}}(t)}{2}. \tag{3}$$

The current (I_C) through the MOS-CAP in the saturation region ($M3$) is achieved by employing drain current equation at node V_0 in linear region and can be expressed as

$$I_C = \frac{K_3}{2}\left[\left(V_{\text{GS}_3} - V_t\right)^2\right]$$
$$I_C = \frac{K_3}{2}\left[(V_3 - V_0 - V_t)^2\right]. \tag{4}$$

Substituting (3) in (4), we get

$$I_C = \frac{K_3}{2}\left[\left(-\frac{V_{\text{in}}(t)}{2} - V_0 - V_t\right)^2\right]$$
$$I_C = \frac{K_3}{2}\left[\frac{V_{\text{in}}(t)^2}{4} + V_0^2 + V_t^2 + V_{\text{in}}(t)V_0 + 2V_0V_t + V_{\text{in}}(t)V_t\right] \tag{5}$$

where K_3 is the MOS transconductance parameter. For simplification purpose, the terms $(V_{\text{in}}(t)V_t)$, V_t^2, and $(V_{\text{in}}(t)^2/4)$ of (4) are discarded due to very small values and substituting (1) in (5). Hence, the current through MOS capacitor is approximated as

$$C\frac{dV_O}{dt} = \frac{1}{2}K_3\left[V_0^2 + V_{\text{in}}(t)V_0 + 2V_tV_0\right]$$
$$\Rightarrow V_0^{-2}\frac{dV_0}{dt} - V_0^{-1}\frac{K_3}{2C}(V_{\text{in}}(t) + V_t) = \frac{K_3}{2C}. \tag{6}$$

The comparative investigation of equation leads a first-order linear differential equation by substituting $V_0^{-1} = X$ with $V_t \approx 0$. The threshold voltage (V_t) can be approximated as a dc offset in the time-varying input signal $V_{\text{in}}(t)$. Therefore, the modified equation (6) can be simplified as

$$\left(\frac{dX}{dt}\right) + \underbrace{\frac{K_3}{2C}V_{in}(t)}_{G}X = -\underbrace{\frac{K_3}{2C}}_{H}$$
$$\left(\frac{dX}{dt}\right) - \left(\underbrace{-\frac{K_3}{2C}V_{in}(t)}_{G}X\right) = -\underbrace{\frac{K_3}{2C}}_{H}. \tag{7}$$

Equation (7) resembles a perfect first-order linear differential equation as (dX/dt)-$GX = -H$, whose solution with the integration constant (D) can be mathematically simplified as

$$Xe^{-\int G dt} = \int -He^{-\int G dt}dt + D$$
$$\Rightarrow Xe^{\int\left\{\frac{K_3}{2C}V_{\text{in}}(t)\right\}dt} = \int -He^{\int\left\{\frac{K_3}{2C}V_{\text{in}}(t)\right\}dt}dt + D$$
$$\Rightarrow X \approx De^{\int\left\{\frac{K_3}{2C}V_{\text{in}}(t)\right\}dt}. \tag{8}$$

Again by putting $V_0^{-1} = X$ in (8) results control voltage (V_0) as

$$V_0^{-1} \approx De^{\frac{K_3}{2C}f(t)}$$
$$\text{or } V_0 \approx \frac{1}{D} - \frac{K_3}{2DC}\phi(t). \tag{9}$$

The drain current flowing through the transistors $M1$ and $M2$ is equal. The expression of the drain current can be expressed as

$$I_D(t) = \frac{1}{2}K_1\left[2(V_0 - V_3 - V_t)\left(\frac{V_{\text{in}}(t)}{2} - V_3\right) - \left(\frac{V_{\text{in}}(t)}{2} - V_3\right)^2\right]. \tag{10}$$

Hence, substituting (3) in (10), the drain current can be reconstructed as

$$I_D(t) = \frac{1}{2}K_1\left[2\left(V_0 + \frac{V_{\text{in}}(t)}{2} - V_t\right)\left(\frac{V_{\text{in}}(t)}{2} + \frac{V_{\text{in}}(t)}{2}\right) - \left(\frac{V_{\text{in}}(t)}{2} + \frac{V_{\text{in}}(t)}{2}\right)^2\right]$$
$$\text{or } I_D(t) = \frac{1}{2}K_1\left[2\left(V_0 + \frac{V_{\text{in}}(t)}{2} - V_t\right) - V_{\text{in}}(t)\right]V_{\text{in}}(t)$$
$$I_D(t) = K_1[V_0 - V_t]V_{\text{in}}(t). \tag{11}$$

Finally, putting (9) in (11) gives

$$I_D(t) = K_1\left[\frac{1}{D} - \frac{K_3}{2DC}\phi(t) - V_t\right]V_{\text{in}}(t). \tag{12}$$

Hence, (12) informs the flux controlled memristor with inverse memristance value as

$$M^{-1}(\phi(t)) \approx K_1\left[\frac{1}{D} - \frac{K_3}{2DC}\phi(t) - V_t\right]. \tag{13}$$

From (13), it is observed that linear drain to source resistance is converted to time-dependent drain to source resistance that imitates the memristor linear time-varying resistor properties without external current bias sources [41]. In addition, the nonvolatile behavior of the memristor is analyzed when the capacitor starts to discharge, and then, it allows the current flow in $M2$ and $M1$.

III. Simulation and Experimental Verification

To substantiate the theoretical prediction of the memristor model (see Fig. 1), both simulation and experimental tests are performed in Cadence Virtuoso analog design tool and off-the-shelf electronic devices on a breadboard for experimental verification, respectively. The first verification for the proposed memristor model uses 90-nm generic process design kit (GPDK) CMOS technology with an aspect ratio of transistors $(W/L)_1 = 120/100$ nm, $(W/L)_2 = 1\ \mu$m/100 nm, and $(W/L)_3 = 240/100$ nm. To test the proposed floating memristor, a sinusoidal input signal of magnitude 1.3 V and frequency 100 kHz is given and reflects the overall transient response, as shown in Fig. 2. MOS-CAP and input voltage parameters are shown in Table II that shows the frequency range at different capacitor values. The prominent finger print of memristor is frequency analysis, which is observed in Fig. 3 at different frequencies (50 kHz, 100 kHz, 1 MHz, and 10 MHz). Let us consider a sinusoidal signal $V_{\text{in}} = A_m \sin(2\pi f_c t)$ for the examination of frequency dependency over pinched hysteresis

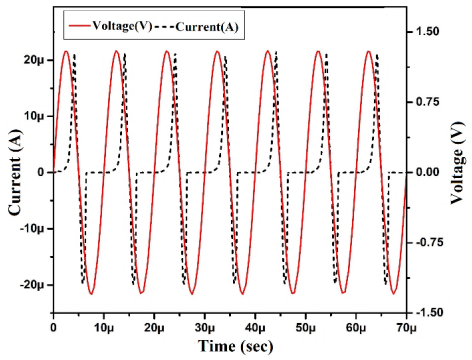

Fig. 2. Transient response of the proposed memristor emulator.

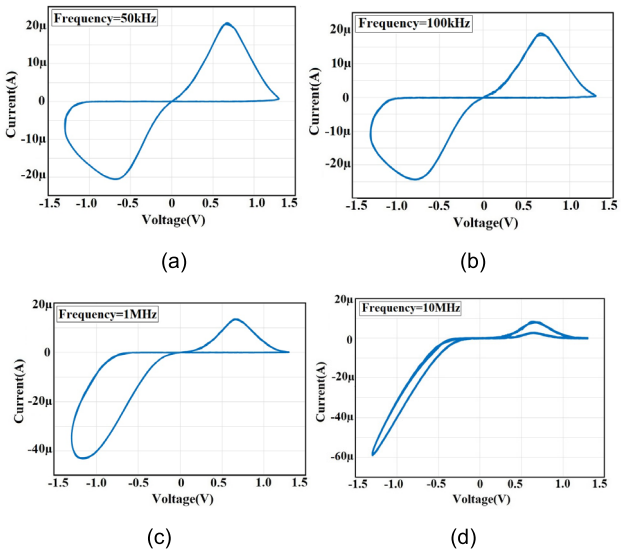

Fig. 3. Pinched hysteresis curve of the proposed floating memristor for frequencies of (a) 50 kHz, (b) 100 kHz, (c) 1 MHz, and (d) 10 MHz.

TABLE II
MOS-CAP PARAMETER AND FREQUENCY RANGE OF MEMRISTOR EMULATOR

Component	Value	Frequency range	Layout Area (W x L)
MOS-Cap* (nmoscap1v)	12.06 pF (W/L = 20µm / 20µm)	Up to 1MHz	41.16 x 28.48 µm
MOS-Cap (nmoscap1v)	301.6 fF (W/L = 5µm / 4µm)	1MHz to 5 MHz	8.24 x 7.21 µm
MOS-Cap (nmoscap1v)	150.8 fF (W/L = 5µm / 2µm)	5 MHz to 20 MHz	5.88 x 6.1 µm
MOS-Cap (nmoscap1v)	30.16 fF (W/L = 2µm / 1µm)	20 MHz to 50 MHz	3.98 x 4.2 µm

*Fingers of nmoscap1v is taken as two for getting this value.
V_1 = 800mV and V_2 = - 500mV

loop with amplitude as "A_m" and frequency as "f." Then, the ON-state memristance can be written as

$$M^{-1}(\phi(t)) \approx \frac{K_1 K_3}{2DC}\frac{A_m}{2\pi f}\cos(2\pi f t) \approx \frac{1}{\tau f} \tag{14}$$

where τ represents the time constant of the proposed emulator that controls the pinched hysteresis loop.

From the above equation, we can observe that as the signal frequency varies, the area of the pinched hysteresis loop depends upon the following cases.

Case 1: As frequency approached infinity ($f \rightarrow \infty$), we can observe that the ON-state inverse memristance tends to zero, which causes the degradation of pinched hysteresis loop characteristics to a linear resistance.

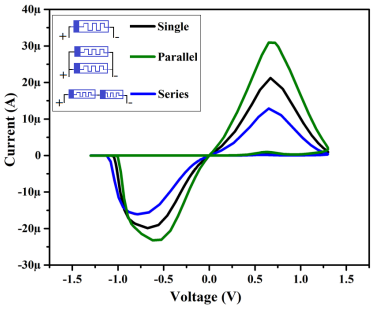

Fig. 4. Pinched hysteresis curve for different combinations of memristor.

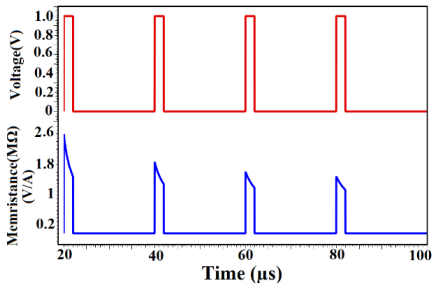

Fig. 5. Nonvolatility test of the proposed memristor.

Case 2: The maximum hysteresis loop area will be attained only when $\tau = 1/f$, so that the ON-state resistance will gain its maximum value.

Case 3: At certain conditions; there may be loss of pinched hysteresis loop when the memristance time constant falls below the signal frequency ($\tau \leq 1/f$).

Besides, an investigation of the proposed memristor emulator is also carried out for different connections. The resultant pinched hysteresis curve in Fig. 4 shows the behavior of the proposed floating memristor for single, series, and parallel connections. It indicates that the memristance value will be doubled and the current value will be decreased by half when similar memristors are connected in series with the same polarity, but in parallel connections, the memristance value will be reduced by half and the corresponding current value will be doubled.

The other scope of investigation in terms of nonvolatility property is also developed in Fig. 5, which illustrates the proposed configuration's memory performance. By applying a train of pulses having a period of 20 μs, the pulsewidth of 2 μs, and amplitude of 1 V is applied at the input terminal, this characteristic of memristor can be examined. It is observed that memristance decreases from 2.5 to 1.48 MΩ during the "ON" period of the first cycle of the input pulse, and it retains the value of memristance during the "OFF" period. For the "ON" period of the second cycle, memristance decreases from the previous memristance to 1.285 MΩ and retains its value of memristance during the "OFF" period. In the next cycle, the process repeats identically. Hence, it is concluded that while the input pulse is in the "OFF" state, the memristor emulator circuit remembers the previous value of memristance, and it can hold for a period of 18 μs. Also, the effect of

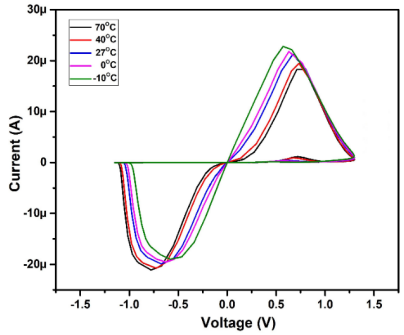

Fig. 6. Pinched hysteresis for different temperatures.

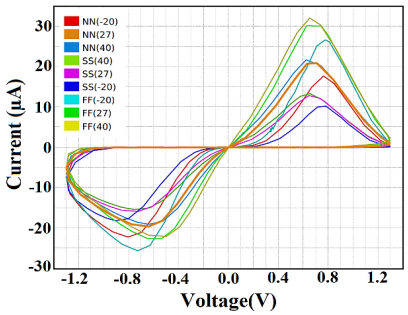

Fig. 7. Pinched hysteresis loops for various temperatures and process corners.

temperature on the proposed memristor emulator in Fig. 6 gives a hysteresis loop that shrinks with the increase in temperature. The temperature variation has a higher impact on drain to source resistance that in turn determines the maximum current rating. It is well known that the drain to source resistance has a positive temperature coefficient due to the reduction of carrier mobility with increment in temperature, which can be represented as

$$R_{\mathrm{DS(on)}}(T) = R_{\mathrm{DS(on)}}(25\ ^{\circ}\mathrm{C})\left(\frac{T}{300}\right)^{n} \tag{15}$$

where n and T represent the fitting parameter and absolute temperature. In case of the proposed memristor, the drain to source resistance plays a major role, and hence, there is a shrinking of pinched hysteresis loop with increase in temperature. Moreover, Fig. 7 depicts the pinched hysteresis loop performance of the proposed memristor at different process corners and temperatures. It can be observed that radical temperature variations and different process corners are slow–slow (SS), normal–normal (NN), and fast–fast (FF). The proposed memristor still operates even though its hysteresis loop varies marginally. It is worth mentioning that more current flows in the FF process corner while less current flows in the SS process corner as anticipated. The layout of the proposed floating memristor emulator is observed in Fig. 8. For a better understanding of the proposed memristor, a postlayout simulation is presented in Fig. 9.

In addition, the proposed floating memristor emulator by incorporating off-the-shelf components is tested experimentally using MOS transistor IRF840. The time-domain behavior

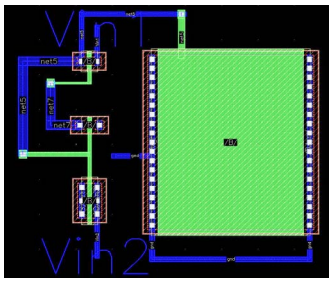

Fig. 8. Layout of the proposed memristor emulator with 59.41 μm^2 of chip area.

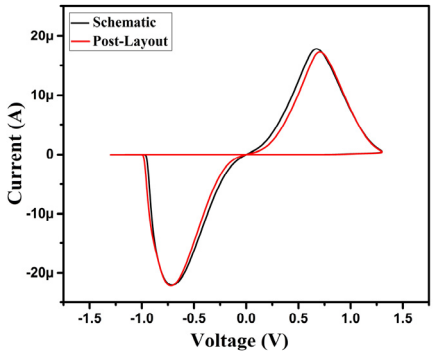

Fig. 9. Pinched hysteresis: layout versus schematic.

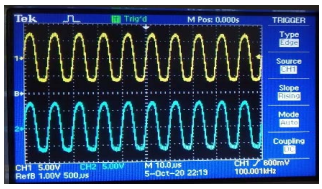

Fig. 10. Transient waveforms of the experimental verification.

of the proposed memristor is observed in the Tektronix DSO by employing a sinusoidal voltage signal with frequency 100 kHz and amplitude 5 V to the memristor emulator circuit. The transient waveforms are shown in Fig. 10, in which output current has been converted to voltage. The corresponding pinched hysteresis loop for three different frequencies (100 kHz, 1 MHz, and 6 MHz) using a capacitor value 22 nF is shown in Fig. 11. The pinched hysteresis lobe area decreases with an increase in frequency that describes the fundamental characteristics of the memristor. Hence, the laboratory confirmation validates the memristor model, and these results have similar characteristics as that of simulation outcomes.

IV. Application Possibility of the Proposed Memristor

In order to validate the workability of memristor, some signal processing circuits such as Binary Frequency-Shift Keying (BFSK) circuit, and logic gates are designed by employing the proposed memristor emulator.

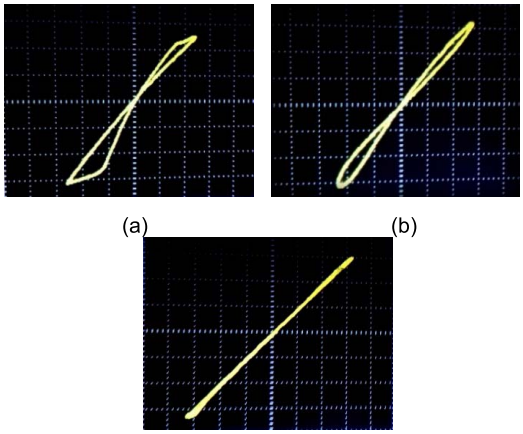

Fig. 11. Pinched hysteresis at different frequencies. (a) 100 kHz. (b) 1 MHz. (c) 6 MHz.

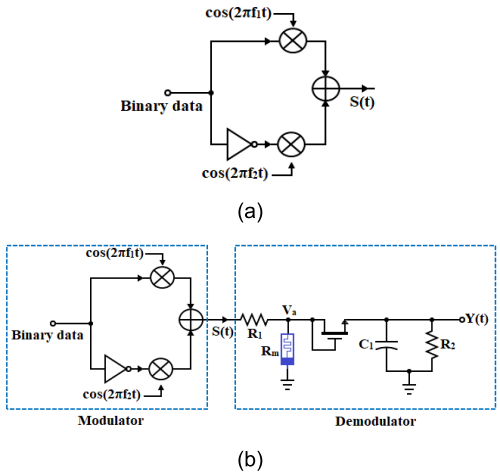

Fig. 12. Memristor-based circuit for BFSK. (a) Modulator. (b) Demodulator.

A. BFSK Modulation and Demodulation

The BFSK is the digital modulation scheme, where two different frequencies are used to modulate binary bits 0 and 1 [42], [43]. Fig. 12 shows the grounded memristor-based BFSK modulator and demodulator configurations. The signals transmitted for binary 1's and 0's are

$$m_1(t) = A\cos(2\pi f_1 t + \theta_c);\ 0 < t \leq T \tag{16}$$

$$m_2(t) = A\cos(2\pi f_2 t + \theta_c);\ 0 < t \leq T. \tag{17}$$

Here, the modulated signal, $S(t)$, changes between two discrete frequency levels. In BFSK, the carrier frequency is shifted by the binary input signal, which changes from a logic 0 to logic 1 and vice versa. The output signal changes between two frequencies. The input binary sequence and BFSK modulated output wave, $S(t)$, are shown in Fig. 13. The output of the modulator circuit $S(t)$ is applied as an input to the demodulator configuration that begins with a voltage divider employing a resistor (R_1) and a memristor. The memresistance (R_m) will increase with the increasing of frequency of input signal $S(t)$. So, the output voltage of the voltage divider

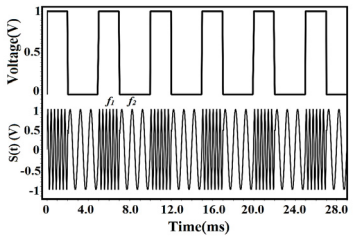

Fig. 13. BFSK input binary sequence and modulated waveform, $S(t)$.

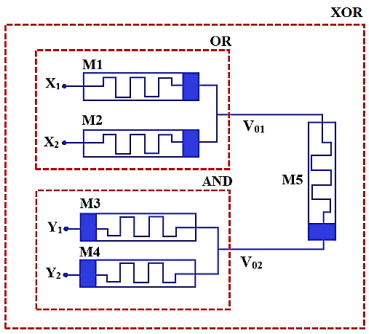

Fig. 14. Logical AND, OR, and XOR operations using memristor.

(V_a) increases. Similarly, V_a reduces with the decreasing of frequency of $S(t)$. After the voltage divider, a peak detector is used, and the diode of the peak detector is replaced by a MOSFET, as shown in Fig. 12. When the input voltage of the peak detector increases (that is higher frequency $S(t)$ signal is received), the capacitor (C_1) voltage is maintained high. Similarly, with the decreasing frequency of $S(t)$, the input voltage of the peak detector reduces. So, the MOSFET will be in cutoff region and capacitor (C_1) will discharge through R_2. The passive component values are $C_1 = 10\ \mu$F, $R_2 = 1$ MΩ, and $R_1 = 1$ kΩ.

B. Memristive Logic Gates

The viability of the proposed memristor design is executed as memristor-based fundamental Boolean logic gates to perform memory and logic operations. The variable resistance to the direction of current flow is a potent element for developing diverse computational design.

Fig. 14 presents a circuit diagram of memristor-based AND, OR, and XOR gate [44] configurations, and the corresponding truth table of the logic gates along with memristance value is well displayed in Table III. For the AND gate configuration, the current flows from higher to lower potential (V_{dd} to gnd); if any of the input is logic 1. When current transfers from memristor $M3$, the value of the memresistance will rise to R_{off}, and simultaneously, the memresistance value of $M4$ will reduce to R_{on} as well as current leaves through the node.

Furthermore, the memristor-based configuration is performed for OR gate, in which the polarities of the memristor are reversed. It can be observed from the table that the output signal will be high only if any or all input signals are at the higher potential. Here, if any input is logic 1 and other is

TABLE III
TRUTH TABLE FOR MEMRISTOR-BASED LOGIC GATES

Inputs		Outputs			Memristance Values		
X_1	X_2	AND (V_{02})	OR (V_{01})	XOR (V_{02}-V_{01})	AND	OR	XOR
0	0	0	0	0	R_{off} (1k)	R_{off} (1k)	R_{off} (1k)
0	1	0	1	1	R_{off} (1k)	R_{on} (5Ω)	R_{on} (5Ω)
1	0	0	1	1	R_{off} (1k)	R_{on} (5Ω)	R_{on} (5Ω)
1	1	1	1	0	R_{on} (5Ω)	R_{on} (5Ω)	R_{off} (5Ω)

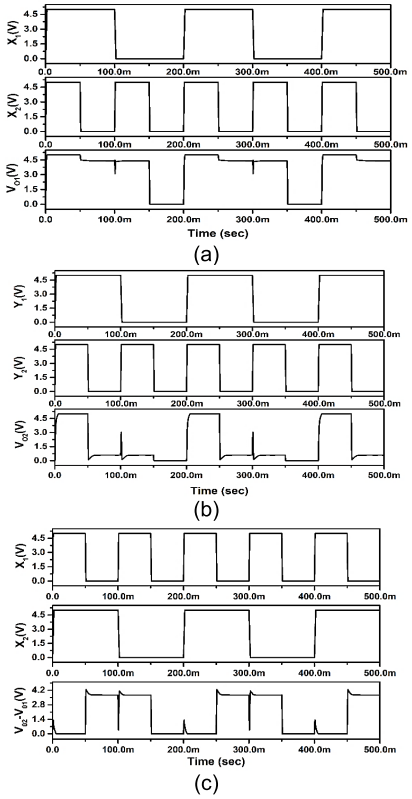

Fig. 15. Simulated results of (a) OR, (b) AND, and (c) XOR operations.

logic 0, i.e., $X_1 = 1$ and $X_2 = 0$, $X_1 = 0$ and $X_2 = 1$, then the current flows from V_{dd} to gnd. When current transfers from memristor $M1$, the value of the memresistance decreases R_{on}, and simultaneously, the memresistance value of $M2$ will increase to R_{off}. Hence, two memresistance values (R_{off} and R_{on}) are developed with different values. By considering the voltage divider rule, the output voltages V_{01} and V_{02} for OR and AND gates can be expressed as

$$V_{01} = \frac{R_{M1}}{R_{M1}+R_{M2}}X_2 + \frac{R_{M2}}{R_{M1}+R_{M2}}X_1 \tag{18}$$

$$V_{02} = \frac{R_{M3}}{R_{M3}+R_{M4}}X_2 + \frac{R_{M4}}{R_{M3}+R_{M4}}X_1. \tag{19}$$

Furthermore, memristor-based XOR configuration is implemented using both AND and OR gates, where Y_1 and Y_2 are the input voltages and X_1 and X_2 are the control voltages. The initial memristance value of $M5$ is R_{off} and its logic value is considered as an output. An influence of $M5$ in that configuration can be minimized by considering the larger value of R_{M5} compared to the other memristors used in the circuit. So, $M5$ acts as an open circuit, and the output voltage of XOR gate can be represented as

$$V_{02} - V_{01} \approx \left(\frac{R_{M3}}{R_{M3}+R_{M4}}Y_2 + \frac{R_{M4}}{R_{M3}+R_{M4}}Y_1\right) - \left(\frac{R_{M1}}{R_{M1}+R_{M2}}X_2 + \frac{R_{M2}}{R_{M1}+R_{M2}}X_1\right). \tag{20}$$

The above observation corresponds the behavior of XOR gate, in which any input becomes logic 1 and other logic 0. Then, the control voltages will be $X_1 = Y_1$ and $X_2 = Y_2$. For input voltages, the current flows from V_{dd} to gnd. The current will pass from $M3$, the memresistance of $M3$ decreases to R_{on}, the memresistance of $M4$ increases to R_{off}, and current leaves through output node. Memresistances of $M1$ and $M2$ are R_{on} and R_{off}, respectively. Two different values of memresistances R_{off} and R_{on} are developed. Hence, by employing the voltage divider rule, the output V_{02} is observed as 1. A similar proceeding is also applicable for V_{01} and found to be 0.

Fig. 15 shows the simulated input and output voltage waveforms with amplitude 5 V and pulsewidth of 50 ms for all the three configurations. The time periods for the first and second signals (X_1 and X_2) are 100 and 200 ms, respectively.

V. CONCLUSION

A simple floating memristor emulator using only three nMOS transistors without any passive element is designed in this research article. The proposed emulator design comes with less active and passive components, a high-operating frequency range, a floating circuit, and low power dissipation and is suitable for IC fabrication. The MOS-capacitor is employed rather than the standard capacitor to operate suitably in the high-frequency range. The entire structure of the memristor emulator circuit is integrated in the Cadence environment using GPDK 90-nm CMOS technology parameters. Each characteristic of the proposed memristor emulator is tested via circuit analysis and simulations. The theoretical analysis, simulation, and experimental results of memristor are obtained and found suitable to the theoretical expectation. To verify the usage of the proposed memristor, the demonstration of applications such as modulation and demodulation of the BFSK process and memristive logic gates is presented for the viability of the proposed memristor design.

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