A MOS-DTMOS Implementation of Floating Memristor Emulator for High-Frequency Applications

Ananda Y. R., Nehal Raj, and Gaurav Trivedi, *Member, IEEE*

***Abstract*— The work presented in this article focuses on designing a floating MOS-dynamic threshold voltage MOSFET (DTMOS)-based circuit to emulate a memristor. The proposed circuit consists of four transistors, including a DT-MOSFET and an external capacitor, which helps obtain high-frequency operations up to 3 MHz. This facilitates easier integration of the devices and monolithic IC fabrication. The correctness of the proposed emulator is validated by conducting various parametric analyses at different operating frequencies and process corners, and it generates acceptable pinched hysteresis loops (PHLs) at various frequencies. Furthermore, pre- and post-layout validation of the proposed emulator are also performed using Cadence Virtuoso with Taiwan Semiconductor Manufacturing Company (TSMC) 180-nm process design kits (PDKs) to prove its effectiveness as a memristor. The area and power consumption of the proposed emulator are 157.48 μm^2 and 8.24 μW, respectively. The physical experiment of the proposed memristor emulator is performed using ALD1106 *n*-channel MOSFETs to characterize its functionality as a real-life memristor. It is also used in designing a memristor-based application to showcase its applicability in power and area optimal circuit design.**

***Index Terms*— ALD1106, cadence Virtuoso, dynamic threshold voltage MOSFET (DTMOS), memristor emulator, pinched hysteresis loop (PHL).**

I. Introduction

THE novel fundamental circuit element memristor was conceptualized by Chua [1], based on the missing relationship between charge (q) and flux (ϕ). The term memristor is used due to its characteristic as a memory and a resistor. It holds the previous resistance value without an applied electric field, showcasing its nonvolatile property. The first physical memristor fabricated by HP Labs in 2008 [2] consists of bilayered TiO_2 sandwiched between two platinum electrodes. The memristor drew the attention of the research community after its first physical fabrication, and various experiments on memristors have been conducted in the recent past to study their nonlinear and nonvolatile properties applicable in diverse applications, such as resistive RAM (ReRAM) [3], neuromorphic computation [4], [5], amplifiers [6], oscillators [7], filters [8], cellular neural network (CNN) [9], mrFPGA [10], approximate computing [11], programmable analog circuits [12], [13], and numerous bio-inspired applications [14], [15]. Furthermore, the design and implementation of any of these applications require a physical memristor, but the fabrication complexities incurred in developing nanostructured memristive devices impact its commercialization [16] and wide usage. As we know, solid-state memristors are commercialized by KNOWM [17]. However, commercial memristors have strict operational conditions, especially dc and ac responses, which limit their general acceptance. Therefore, many memristor models [18], [19], [20], [21] have been developed aiming to implement it in various real-life applications and are analyzed numerically.

One of the most promising methods to circumvent this limitation is the physical realization of a memristor (or emulation) using discrete components, such as MOSFETs. The technique of realizing the behavior of a memristor using the existing components is termed as memristor emulation [12]. The key principle mechanism of memristor emulation is to exhibit three important fingerprints [38], viz.: 1) I–V characteristic exhibiting pinched hysteresis loop (PHL); 2) lobe area of PHL increases when frequency decreases; and 3) lobe area shrinks as frequency increases and I–V curve becomes linear at the maximum frequency. The memristor emulator designed by Pershin and di Ventra [12] includes a microcontroller, an ADC, and a digital potentiometer. The operating frequency of this emulator is limited to 50 Hz, and the circuit complexity restricts this emulator from being used with other circuit elements operating at a high frequency. The memristor emulator proposed by Kim et al. [23] consists of several discrete elements, such as an operational amplifier, analog multiplier, transistors, and resistors. However, this emulator is unsuitable for monolithic integration due to many discrete components and a large ON-chip area. Similarly, there are many memristor emulators available in the literature which use second-generation current conveyors (CCIIs) and passive elements [24], [25], differential difference current conveyor (DDCC) [33], current feedback operational amplifiers (CFOAs) and operational transconductance amplifier (OTA) [22], current backward transconductance amplifier (CBTA) [29], differential voltage current conveyor transconductance amplifier (DVCCTA) [34], etc. Note that

Manuscript received 18 July 2022; revised 6 November 2022; accepted 2 December 2022. Date of publication 13 December 2022; date of current version 24 February 2023. *(Corresponding author: Ananda Y. R.)*

Ananda Y. R. and Gaurav Trivedi are with the Department of Electronics and Electrical Engineering, IIT Guwahati, Guwahati, Assam 781039, India (e-mail: yrananda@iitg.ac.in; trivedi@iitg.ac.in).

Nehal Raj is with the Department of Electronics and Communication Engineering, Bhusanayana Mukundadas Sreenivasaiah College of Engineering (BMSCE), Bengaluru, Karnataka 560019, India (e-mail: nehalraj3599@gmail.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TVLSI.2022.3227201.

Digital Object Identifier 10.1109/TVLSI.2022.3227201

TABLE I
SUMMARY OF EXISTING MEMRISTOR EMULATORS

Ref., Year	Components used	Hardware Implementation	Power Consumption	Operating Frequency
[22], 2014	1OTA, 2CFOA, 3R, 2C	Complex	High	Low
[23], 2012	2OPAMPs, 1Multiplier, 2R, 1C			
[24], 2015	4CCIIs, 1Multiplier, 2R, 1C			
[25], 2014	4CCIIs, 1Multiplier, 1OPAMP, 8R, 1C			
[26], 2015	2CCII, 1Multiplier, 2R, 1C			
[27], 2017	1CCII, 1Multiplier, 1R, 1C			
[28], 2017	1MO-OTA, 1Multiplier, 1R, 1C			
[29], 2017	1CBTA, 1Multiplier, 2R, 1C			
[30], 2014	3CFOAs, 4R, 2C, 1D			
[31], 2016	3OTAs, 4CCIIs, 6R, 1C	Complex	Moderate	Low
[32], 2017	1OTA, 2Transistors, 1C			
[33], 2014	1DDCC, 1 Multiplier, 2R, 1C	Complex	High	High
[34], 2017	1 DVCCTA, 1OTA, 3R, 1C			
[35], 2018	CCTA, CCII, 3R, 1C	Complex	-	High
[36], 2018	1VDTA, 1Multiplier, 2R, 1C			
[37], 2020	1OTA, 1CDTA, 1C			

Here, "-" represents no data available for the references given.

memristor emulators having discrete circuit elements are available in the form of analog ICs [22], [26], [27], [28], [31], [35] for commercial use. However, Babacan et al. [39] presented a grounded memristor emulator using four MOSFETs with a maximum operating frequency of 100 MHz. Since this emulator is of the grounded type, one of its terminals is always connected to the ground. It also requires an external dc supply making its usage complex in practical applications [40]. In contrast, our proposed emulator does not require any external dc supply, which reduces its complexity and power consumption compared with [39]. The memristor emulators presented in the literature exhibit limitations in monolithic integration due to the complexity involved in their topology. A summary of the existing memristor emulators is depicted in Table I for ready reference. It can be seen in Table I that the need of the hour is to design a simple and efficient memristor emulator for its wider applicability in low- to high-frequency applications. Thus, it is imperative to use a minimum number of the existing nonlinear discrete devices with as few passive elements as possible to mimic the behavior of a memristor. Not only will this enable optimizing the area, power, and delay of the memristor emulator but also it will increase the feasibility of its integration with other circuit elements. The increasing demand for high-performance and low-power devices motivated us to propose a novel memristor emulator using four metal–oxide–semiconductor field-effect transistors and an external capacitor. The novelty of the proposed emulator is depicted below.

The key features of the proposed emulator are listed as follows.

1) It needs four n-channel MOSFETs, which makes it suitable for monolithic IC fabrication.
2) It is more area-efficient than other emulators reported in the literature.
3) The simplicity of the proposed emulator facilitates easy integration with other circuits/devices for designing potential applications to exploit the key properties of the memristor.
4) Unlike other emulators, the proposed emulator works without external bias.

Numerical analyses of the proposed emulator for various parameters are conducted using the cadence Virtuoso EDA framework and Taiwan Semiconductor Manufacturing Company (TSMC) 180-nm technology. In addition, the post-layout simulation is performed to validate the correctness of the proposed memristor emulator. Furthermore, the efficacy of the proposed memristor emulator is validated by implementing memristor-based applications. Note that the proposed memristor emulator is realized physically using ALD1106 n-channel MOSFETs, which generates a PHL as per our expectation at various frequencies. This further corroborates the correctness of the proposed memristor emulator topology.

The structure of the article is organized as follows. Section II presents detailed circuit analysis and mathematical formulation of the proposed memristor emulator. Section III describes the performance analysis of the proposed emulator. Applications of our emulator are discussed in Section IV. Finally, Section V concludes the article.

II. PROPOSED MOS-DTMOS MEMRISTOR EMULATOR

The main objective of this work is to realize the behavior of the memristor using MOS transistors and an external capacitor. The proposed memristor emulator also incorporates a dynamic threshold voltage MOSFET (DTMOS), which is formed by connecting body of a MOSFET to its gate terminal. The circuit configuration and mathematical analysis of the proposed memristor emulator are discussed in this section.

A. DTMOS Transistor

A MOSFET should ideally have a high threshold voltage V_t at $V_{GS} = 0$ to achieve low leakage and low V_t at $V_{GS} = V_{DD}$ to achieve high speed. It is desired to have low leakage and high speed for improving the performance of a MOSFET at very low voltages. A DTMOS is used to overcome these constraints by connecting gate and body terminals of a MOSFET. Note

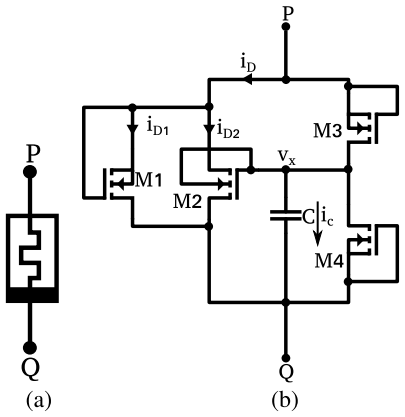


Fig. 1. (a) Memristor symbol and (b) proposed MOS-DTMOS circuit topology for memristor emulator.

that the DTMOS transistor exhibits high threshold when it is off to minimize the leakage, whereas it presents a low threshold under low voltage supplies to drive high current. It also exhibits steeper subthreshold swing and higher carrier mobility than the conventional MOSFET. Due to dynamic body bias voltage, the threshold voltage (V_t) of the MOS transistor becomes a function of the input signal [41]. With an input signal applied at the gate terminal, body bias changes dynamically with the change in the input. Thus, $V_{\mathrm{GS}} = V_{\mathrm{BS}}$ is maintained as gate and body terminals are shorted together [42]. Note that the source–body junction gets slightly forward biased when the gate input of a MOSFET increases, but its V_t decreases because of the body effect. Due to dynamic body bias, gate and body terminals control potential in the channel region, leading to a high transconductance, which drives a faster current into the channel. As we know, the threshold voltage of a DTMOS transistor can be modeled using the following equation [43]:

$$V_t = V_{t_0} + \gamma\left(\sqrt{|2\psi_{\mathrm{S}} + V_{\mathrm{SB}}|} - \sqrt{|2\psi_{\mathrm{S}}|}\right). \tag{1}$$

Here, γ, ψ_{S}, and V_{SB} are the body effect coefficient, surface potential, and the voltage between the source and body, respectively. In the proposed memristor emulator, DTMOS transistor helps in the realization of memristor behavior at different operating frequencies. This further aids in achieving the maximum operating frequency of the proposed memristor emulator. An analytical study of this emulator is given below.

B. Design and Analytical Model of the Proposed Emulator

Fig. 1(a) depicts the symbol of a memristor. An equivalent circuit emulating a memristor (emulator) is shown in Fig. 1(b). This memristor emulator consists of four MOSFETs and an external capacitor. Two MOSFETs, M_1 and M_2, are connected in parallel and are biased in the linear region, which converts the quadratic relationship between current and voltage into linear relationship to form an electronically tunable resistance. The gates of other MOSFETs, M_3 and M_4, are connected to drain, which force them to operate in the saturation region. This forms a feedback system that samples the input voltage difference and controls the gate of M_2. Note that M_2 is configured as DTMOS. The threshold voltage of M_2 varies dynamically with respect to the change in the input voltage change, which helps obtain the stable and desired characteristics of a memristor. A capacitor C is used to convert current into voltage and is connected to the gate terminal of M_2. It helps in exhibiting the nonvolatile property of a memristor because there is no path for the drain current to flow through capacitor to the gate of M_2. A detailed analysis of the proposed memristor emulator is given below.

The variable resistance of M_1 and M_2 can be obtained by adding the currents passing through these MOSFETs operating in the triode region and is expressed by the following equation:

$$i_D = i_{D1} + i_{D2}. \tag{2}$$

After simplifying (2), the following mathematical expression is obtained:

$$i_D = k_{1,2}\left(V_{\mathrm{GS}_{1,2}} - 2V_{t_{1,2}}\right)v_{\mathrm{PQ}}. \tag{3}$$

Here, $k_{1,2}$ is the process parameter of M_1 and M_2. V_{GS} and v_{PQ} are the voltage across the gate and source terminals of a MOSFET, and a time-varying input voltage is applied between terminals P and Q. The resistance of M_1 and M_2 can be derived as follows:

$$r_{\mathrm{ds}_{1,2}} = \frac{1}{k_{1,2}\left(V_{\mathrm{GS}_{1,2}} - 2V_{t_{1,2}}\right)}. \tag{4}$$

By applying Kirchhoff's current law at node v_x, the current flowing through the capacitor is given by the following equation:

$$i_c = i_{M_3} + i_{M_4}. \tag{5}$$

After substituting the current flowing through the capacitor, M_3 and M_4, (5) can be described as mentioned below

$$C\frac{\mathrm{d}v_x}{\mathrm{d}t} = k_3\left(V_{\mathrm{GS}_3} - V_{t_3}\right)^2 + k_4\left(V_{\mathrm{GS}_4} - V_{t_4}\right)^2. \tag{6}$$

As mentioned above, the time-varying input voltage across two floating terminals, P and Q, of the memristor emulator is v_{PQ}. Thus, V_{GS_3} and V_{GS_4} are $(v_{\mathrm{PQ}}/2)$ and $-(v_{\mathrm{PQ}}/2)$, respectively. Considering $(k_3/k_4) = (kM/kN)$ and $V_{t_3} = V_{t_4} = V_t$, then (6) can be depicted as

$$C\frac{\mathrm{d}v_x}{\mathrm{d}t} = Mk\left(\frac{v_{\mathrm{PQ}}}{2} - v_x - V_t\right)^2 + Nk\left(\frac{-v_{\mathrm{PQ}}}{2} - v_x - V_t\right)^2. \tag{7}$$

Here, $k = \mu_n C_{ox}(W/L)$, the common process parameter of M_3 and M_4, whereas M and N are constants. Equation (7) can be further expressed as

$$C\frac{\mathrm{d}v_x}{\mathrm{d}t} = k(M+N)v_x^2\left[4\left[1 - \frac{\left(v_{\mathrm{PQ}} + V_t\right)}{4v_x} + \frac{\left(v_{\mathrm{PQ}} + V_t\right)}{2v_x}\right]^2 + \frac{3V_t^2}{4v_x^2}\right.$$

$$- \frac{(3M-N)}{2(M+N)}\left(\frac{v_{\rm PQ}V_t}{v_x^2}\right) + \frac{\left(\frac{N-M}{M+N}\right)v_{\rm PQ}+2V_t}{v_x} - 3\Bigg]. \tag{8}$$

After simplifying (8), node voltage v_x can be obtained as stated below

$$C\frac{{\rm d}v_x}{{\rm d}t} = 2kv_x^2\left[\frac{v_{\rm PQ}}{2v_x} + \frac{5V_t}{2v_x} - 3\right] \tag{9}$$

or

$$\frac{1}{v_x^2}\frac{{\rm d}v_x}{{\rm d}t} = \frac{k}{C}\left(\frac{v_{\rm PQ}+5v_t}{v_x}\right) - \frac{6k}{C}. \tag{10}$$

Choosing $y = v_x^{-1}$, (10) can be formulated as

$$\frac{{\rm d}y}{{\rm d}t} + \frac{k}{C}\left(v_{\rm PQ}+5v_t\right) = \frac{6k}{C}. \tag{11}$$

Equation (11) implies a perfect first-order linear differential equation as $({\rm d}y/{\rm d}t) + Ey = F$, and its solution is given as

$$ye^{-\int E{\rm d}t} = \int -Fe^{-\int E{\rm d}t}{\rm d}t + Z. \tag{12}$$

Here, Z is an integration constant. By comparing (11) and (12) and substituting the value of E and F, (12) can be formulated as mentioned below

$$ye^{-\int \frac{k}{C}\left(v_{\rm PQ}+5V_t\right){\rm d}t} = \int \frac{6k}{C}e^{-\int \frac{k}{C}\left(v_{\rm PQ}+5V_t\right){\rm d}t}{\rm d}t + Z. \tag{13}$$

After solving (13), y can be approximated as

$$y \approx Ze^{-\int \frac{k}{C}\left(v_{\rm PQ}+5V_t\right){\rm d}t}. \tag{14}$$

As we know, $\varphi(t) = \int\left(v_{\rm PQ}+5V_t\right){\rm d}t$, v_x can be formulated using (14) as mentioned below

$$v_x \approx \frac{1}{Z} + \frac{k}{ZC}\varphi(t). \tag{15}$$

As mentioned above, the proposed memristor comprises the DTMOS transistor. The threshold voltage of DTMOS is depicted in (1) and can be simplified as illustrated in the following equation:

$$V_t \approx V_{t_0} + \alpha_{\rm SB}V_{\rm SB} \tag{16}$$

where $\alpha_{\rm SB}$ is the body effect constant.

Substituting M_2 gate voltage $V_{\rm GS} = v_x$, input voltage $v_{\rm PQ} = v_{\rm in}(t)$, and DTMOS threshold voltage depicted in (16) to (3), the following mathematical expression for the proposed memristor emulator can be derived:

$$\frac{i_D}{v_{\rm in}(t)} = k_{1,2}(1+2\alpha_{\rm SB})v_x. \tag{17}$$

The above-mentioned mathematical expression states the memductance of a memristor, which can be further denoted as

$$M^{-1}(\varphi(t)) = k_{1,2}(1+2\alpha_{\rm SB})\left(\frac{1}{Z} + \frac{k}{ZC}\varphi(t)\right). \tag{18}$$

Note that (18) converts linear resistance $r_{{\rm ds}_{1,2}}$ of the MOSFET into the time-dependent drain-to-source resistance, which is used to emulate the characteristic behavior of a memristor. The proposed memristor emulator also exhibits nonvolatility by storing charge in the capacitor.

For analyzing the frequency behavior of the proposed memristor emulator, input excitation is considered as $v_{\rm in}(t) = A_m\sin(\omega t)$, where A_m and ω are its amplitude and operating frequency, respectively. Therefore, memductance of the proposed memristor emulator can be represented as mentioned below

$$M^{-1}(\varphi(t)) = \underbrace{\frac{k_{1,2}(1+2\alpha_{\rm SB})}{Z}}_{\text{linear time-invariant}} + \underbrace{\frac{k_{1,2}(1+2\alpha_{\rm SB})kA_m\cos(\omega t-\pi)}{ZC\omega}}_{\text{linear time-variant}}. \tag{19}$$

Using (19), it can be observed that as the frequency tends to infinity, the time-variant part of memductance becomes zero and behaves as a linear resistor. The time-dependent behavior of the memristor can be obtained by (19), which is defined below

$$\mathscr{A} \approx \frac{kA_m}{2\pi fC} = \frac{1}{\tau f}. \tag{20}$$

Here

$$\tau = \frac{2\pi C}{kA_m} \tag{21}$$

where τ is the time constant of the proposed emulator.

The time constant τ regulates the PHL of the proposed emulator, and $T = 1/f$ is the period of excitation. τ is based on the parameters of circuit elements used in the memristor emulator. It can be changed according to the desired operating frequency. Only C can be changed effectively, whereas other parameters are considered constant. Therefore, the capacitor acts as a tuning parameter for τ. The following observations are derived using (20) and (21).

1) $\mathscr{A} \to 0$, when $f \to \infty$ or $A_m \to 0$, which drives the emulator to behave as a linear time-invariant resistor.
2) $\mathscr{A} \to 1$, when $f \to 1/\tau$ or A_m is monotonically increased. In this case, the emulator generates maximum PHL to exhibit memristor behavior.
3) $\mathscr{A} \geq 1$, when $f \leq 1/\tau$ or A_m increases substantially, yielding distorted I–V characteristics.

C. Nonideal Analysis

The proposed emulator uses ideal MOSFETs, but in reality, parasitic elements impact the behavior of the memristor. The parasitic capacitances, resistances, and nonidealities are exhibited due to parameter mismatch of MOSFETs, affecting the overall performance and deviating the emulator from its ideal behavior.

As shown in Fig. 2, a MOSFET has parasitic capacitances due to charge in the depletion region and gate-to-source or gate-to-drain overlap. These capacitances exhibit dependence on source/drain voltage (biasing) in a MOSFET [43]. The equivalent capacitance of the proposed memristor emulator is $C_{\rm eq} = C_{\rm DB} + C_{\rm GD} + C_{\rm GS} + C = C_{\rm par} + C$, where $C_{\rm par} = C_{\rm DB} + C_{\rm GD} + C_{\rm GS}$ is the parasitic capacitance and

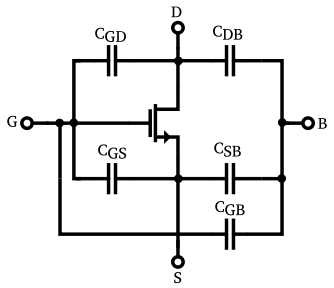


Fig. 2. Parasitic capacitance in a MOSFET.

C is an external capacitor used in the proposed emulator. Let R_{par} denote the parasitic resistance, then memductance can be expressed using the following mathematical expression:

$$M^{-1}(\varphi(t)) = k_{1,2}(1+2\alpha_{\text{SB}})\left(\frac{1}{Z}+\frac{k}{Z(C_{\text{eq}})}\varphi(t)\right)+\frac{1}{R_{\text{par}}}. \tag{22}$$

It can be observed that C_{par} affects memductance and with an increase in the frequency, the linear time-variant part of memductance becomes negligible. Therefore, it can be stated that the memductance of the circuit depends on the nonideal and parasitic components of the MOSFET.

Using the analytical model of the proposed emulator, numerical analysis is performed, and its characteristic is validated in various conditions while varying operating voltage and frequency and at different process corners, etc., which is described in Section III.

III. Performance Analysis of the Proposed Memristor Emulator

The numerical analysis of the proposed emulator is performed using TSMC 180-nm process design kits (PDKs) in Cadence Analog Design Environment, and its vital characteristics are verified extensively. Its detailed performance evaluation is described below.

A. Numerical Analysis

The proposed memristor emulator is designed by choosing aspect ratios $(W/L)_1 = 220$ n/1 μ, $(W/L)_2 = 40$ μ/1 μ, and $(W/L)_3 = (W/L)_4 = 1$ μ/1 μ. The sinusoidal input with a peak voltage of 800 mV and 100 kHz is applied to the terminals P to Q of the emulator. The transient response of the current flowing through the proposed emulator is shown in Fig. 3(a). The nonlinearity of the current waveform in the proposed memristor emulator demonstrates the nonlinear behavior of memristors. This nonlinearity decreases with an increase in the frequency, and the memristive effect disappears [44], [45]. Fig. 3(a) exhibits a very little to no-phase shift between the current and the voltage, illustrating the memristor's resistive nature. Many earlier memristive devices, such as HP memristor models [2], do not show the nonlinear behavior of the memristors. Hence, they illustrate a symmetrical current waveform. Although the HP memristor model enabled researchers to understand and analyze critical aspects of the memristor, it was later acknowledged that the HP model could not provide the actual nonlinear behavior of the memristor [44]. The primary fingerprint of a memristor is the zero-crossing PHL. The hysteresis lobe area of the first and third quadrants may be unsymmetrical due to parasitic elements with the memristor emulator. These parasitic elements depend on the properties of the components used to mimic the memristor behavior [46]. The physical memristor usually exhibits an unsymmetric PHL [47], [48], [49]. Similar unsymmetrical PHLs can also be observed in other emulators reported in [39], [50], and [31]. Therefore, the unsymmetrical current waveform shown in Fig. 3(a) of the proposed memristor emulator exhibits the nonlinear behavior of the memristor and is due to the nonlinear characteristics of the MOSFETs and the parasitic elements [48], [51]. The I–V characteristics exhibiting nonlinear and nonvolatile properties of the memristor by generating a PHL are depicted in Fig. 3(b). Furthermore, PHLs of the proposed memristor emulator generated at different operating voltages are illustrated in Fig. 3(c). The lobe area of the PHL is directly proportional to the amplitude of the input voltage (A_m) and inversely proportional to its frequency (f), which is stated in (19) of the proposed emulator. The lobe area of the PHL increases with an increase in the amplitude of the applied voltage, as shown in Fig. 3(c). It can be observed that a higher amplitude of the input voltage causes a higher lobe area of the PHL, which verifies the correctness of the proposed memristor.

As we know, the external capacitor is used for generating PHL at different operating frequencies. The different external capacitors of 10 nF, 10 pF, and 100 fF are selected for low-, medium-, and high-frequency operations. Fig. 4 exhibits the analytical results of the proposed memristor emulator at different operating frequencies using the capacitors mentioned above. It can be seen that upscaling the input frequency with smaller capacitors reduces the lobe area of the PHL. Therefore, the proposed emulator validates important fingerprints of an actual memristor.

It can be observed in Fig. 5 that the current through memristor increases with respect to time. This change happens only when the pulse is on. It can be seen that the voltage across the capacitor is proportional to memductance, which exhibits the nonvolatile property of the memristor. Since the voltage across the capacitor increases/decreases for the positive/negative pulse, as depicted in Fig. 5(b), in the absence of a voltage pulse, the memristor emulator retains previous information emulating the nonvolatile behavior of an actual memristor.

The two memristors connected in series and parallel are used to analyze the characteristics of the proposed memristor emulator. It can be observed in Fig. 6(a) that PHL becomes a straight line due to an increase in the memristance when two memristors are connected in series. Similarly, PHL increases with a decrease in the memristance due to two memristors connected in parallel.

The correctness of the proposed memristor is evaluated by analyzing its behavior at different process corners illustrated in Fig. 6(b) and (c). Its stability and reliability are validated at different process corners under varied temperature conditions. The PHL of our proposed memristor is generated without

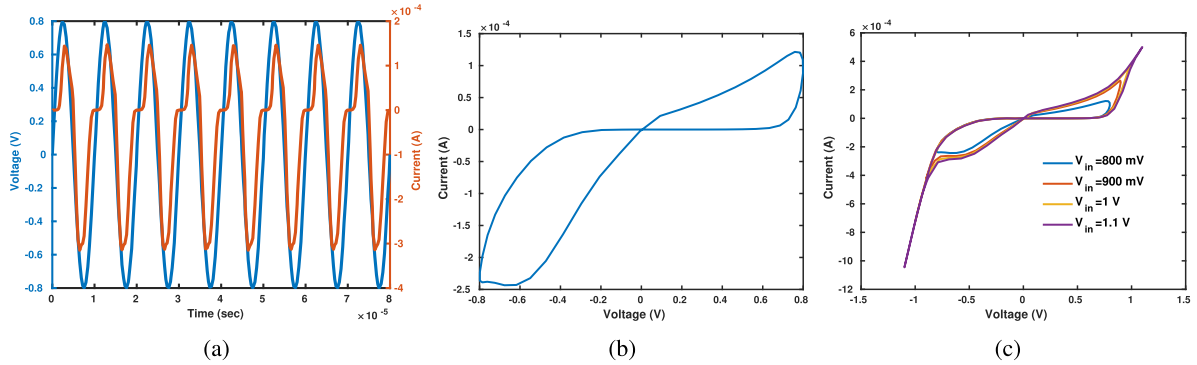


Fig. 3. (a) Transient response, (b) I–V characteristic (PHL), and (c) PHLs of a proposed emulator at different input voltages.

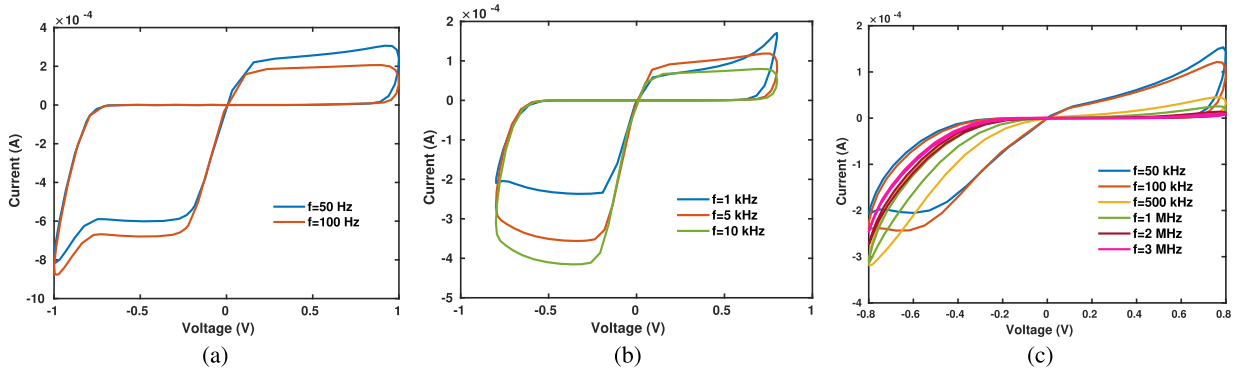


Fig. 4. PHLs of a proposed emulator for (a) 10 nF, (b) 10 pF, and (c) 100 fF at different frequencies.

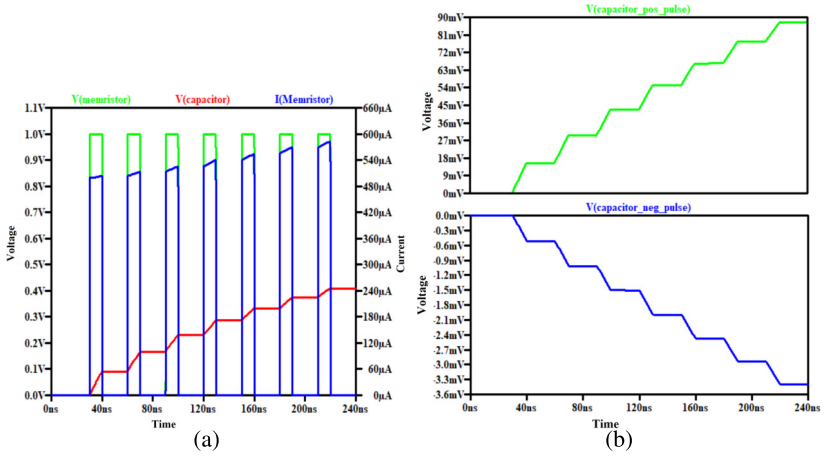


Fig. 5. Transient response of the emulator using 1-pF capacitor using an input pulse having 10-ns ON state and 40-ns time period of (a) 1-V amplitude and (b) 0.4-V and −0.4 V amplitude.

any distortion and is shown in Fig. 6(b) and (c). It can be seen that a rise in temperature reduces the current flowing through the memristor [52], which increases its memristance. It can also be seen in Fig. 6(b) that the lobe area of PHL increases at low temperatures (10 °C) and decreases at high temperatures (80 °C). Furthermore, the proposed memristor emulator is analyzed at different process corners, as shown in Fig. 6(c). The lobe area of the PHL varies with different process corners. Note that the proposed emulator consists of n-channel MOSFETs only, which directs us to choose FF, TT, and SS only to perform corner analysis. It can be seen in Fig. 6(c) that at FF, the current through the proposed emulator is high, whereas at SS, it is comparatively low. Thus, it can be summarized that the proposed emulator showcases stable and reliable behavior at different temperatures for various process corners and illustrates its optimal characteristics at room temperature (27 °C) for a typical (TT) process corner.

The Monte Carlo analysis is used to investigate the effect of process parameter variations and mismatch between transistors and to prove the robustness of the proposed emulator. The

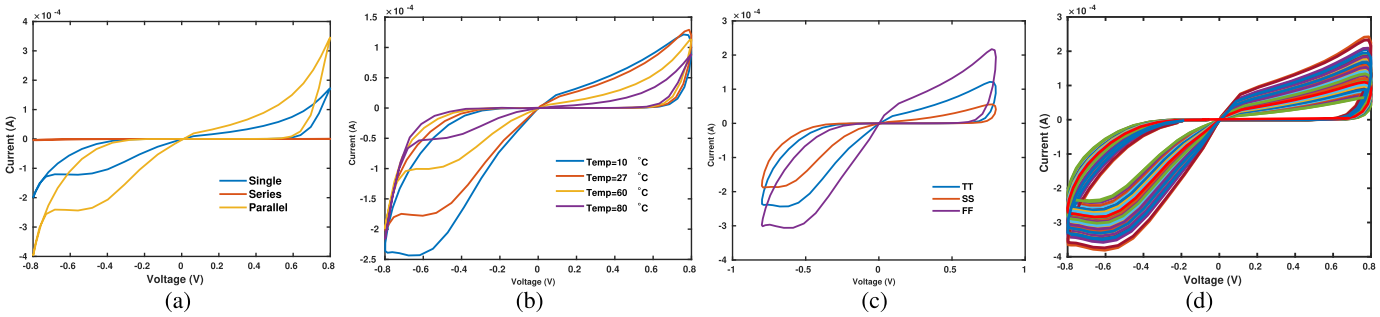


Fig. 6. PHLs of the proposed emulator at (a) series and parallel combination, (b) different temperatures, (c) different process corners, and (d) Monte Carlo analysis.

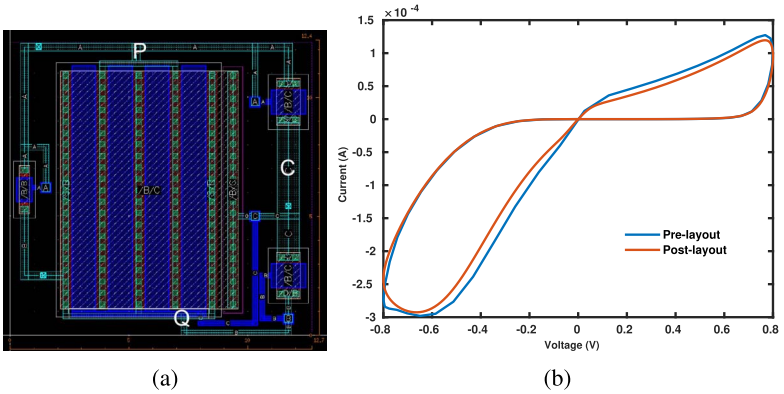


Fig. 7. (a) Layout design and (b) pre- and post-layout analyses of the proposed emulator.

deviations in the parameters, such as aspect ratios, threshold voltages, and capacitances, are chosen as the uniform distribution within the tolerance limits of each parameter. By analyzing Fig. 6(d), it can be seen that the proposed emulator retains memristor behavior by generating PHLs irrespective of the variations in the capacitance and device parameters exhibiting stable performance. It can be observed in Fig. 6(d) that the I–V characteristic remains pinched at the origin, and the memristive nature is conserved. Note that the proposed memristor emulator provides stable PHL without any distortion up to the maximum operating frequency at 3 MHz.

B. Pre- and Post-Layout Analysis

The physical design of the proposed memristor emulator is generated using the Cadence layout design platform using TSMC 180-nm technology, as shown in Fig. 7(a). In this layout, there are three pins named P, Q, and C. P and Q are used to connect memristor emulator to an external input source, and C is connected to an external capacitor, which can be tuned with the frequency of input signal. Furthermore, the post-layout simulation is also performed to ensure reliable characteristic behavior of the proposed emulator, and the desired PHL is obtained, as shown in Fig. 7(b), which shows that there is a slight deviation in the post-layout PHL when compared with the pre layout PHL due to the effect of parasitic elements. The area and power utilization of the proposed emulator are estimated as 157.48 μm^2 and 8.24 μW, respectively. The DTMOS is an essential part of the proposed emulator. It reduces the circuit complexity and the number of MOSFETs required to design a memristor emulator. Due to this, the area utilization and the circuit complexity of the proposed memristor get reduced substantially. Note that the proposed memristor emulator consumes less area than most of the memristor emulators reported in the literature. The performance of the emulator presented in this article is validated experimentally, which is described below.

C. Experimental Validation

The experiment to validate the memristive behavior of the proposed memristor emulator shown in Fig. 1(b) is performed by selecting suitable n-channel MOSFETs and capacitors. In this experiment, four ALD1106 n-channel MOSFETs [53] are used. The capacitors of different values are chosen depending on the operating frequencies. Rigol DG1022 function generator is used to apply the sinusoidal input voltage to the proposed memristor emulator, and MDO3012 Mixed Domain Oscilloscope is used to observe the response of the memristor emulator.

The prototype of the proposed emulator circuit is assembled on a breadboard as depicted in Fig. 8(a), and its experimental setup is shown in Fig. 8(b). Transient response and I–V characteristics of the proposed memristor emulator at an input having 1-V peak voltage and 500-Hz frequency using 0.22-F capacitor is obtained, which is shown in Fig. 9(a) and (b), respectively. It can be observed that scaling the frequency to 1 kHz shrinks the lobe area of the PHL, which is illustrated in Fig. 9(c). In addition, acceptable memristor

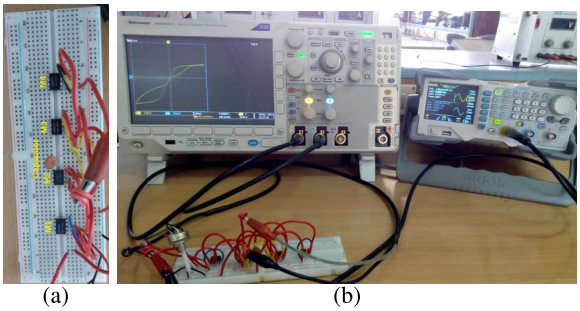


Fig. 8. (a) Prototype circuit on breadboard and (b) experimental setup of the proposed emulator.

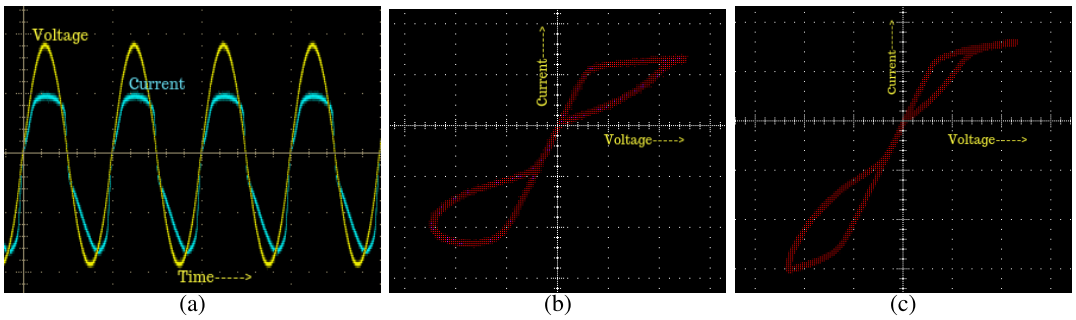
behavior is observed at different operating frequencies by selecting suitable capacitors. The outcome of this experiment states that an increase in frequency leads to reduce the lobe area of the PHL, which is shown in Figs. 10 and 11. Note that the ALD1106 n-channel MOSFETs design parameters differ from those designed to realize the proposed emulator, using TSMC 180-nm PDKs. Due to this, there is a difference in the shape of the PHLs of experimental analysis and the simulated results. It validates that the outcome of numerical and experimental analyses of the proposed memristor emulator is in coherence, which proves its correctness and reliability.

There are numerous memristor emulators [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [34], [35], [36], [37], [54] available, which are designed using operational transconductance amplifiers (CA3080), Opamps, analog multipliers (AD633), CCIIs (AD844), and other analog IC components. The hardware complexity of these emulators is high, and the operating frequency is limited in the kHz range. The other emulators [33], [35], [36], [37] are also configured using analog ICs and able to generate PHL in the range of MHz, but these emulators require discrete analog ICs and passive components, which make them unsuitable for monolithic IC integration. The comparative analysis of the proposed emulator and other memristor emulators reported in the literature is shown in Table II. It can be observed that our emulator consists of the least number of devices and is 592.2× more power-efficient and exhibits 3× better operating frequency range than [34]. Although [35] has a better operating frequency, it uses more than 35 transistors to mimic memristive behavior, and its power consumption is also higher. Similarly, [31] has the lowest power consumption, but its maximum operating frequency is only 10 kHz. Also, [32] has less power consumption than the proposed emulator, but its operating frequency is 30 Hz, which is the least among all the state-of-the-art emulators.

As we know, the operating frequency of an emulator depends on the circuit topology and on the type of emulator, i.e., grounded-type emulator [22], [23], [26], [27], [28], [29], [30], [34], [39] or floating-type emulator [24], [25], [29], [30], [31], [32], [33], [35], [36], [37], [54]. Designing a floating memristor is more complex than designing a grounded memristor circuit. However, grounded memristors have limited applications [40]. The proposed emulator is a floating two-terminal device similar to a resistor, capacitor, and inductor. It can be easily incorporated into any circuit. Any terminal of the proposed emulator can be connected to the ground or any other device or circuit elements while designing an application. The proposed emulator occupies 157.48-μm^2 area when compared with 366 μm^2 used by the grounded emulator [39] and other emulators available in [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [35], [36], [37], and [34].

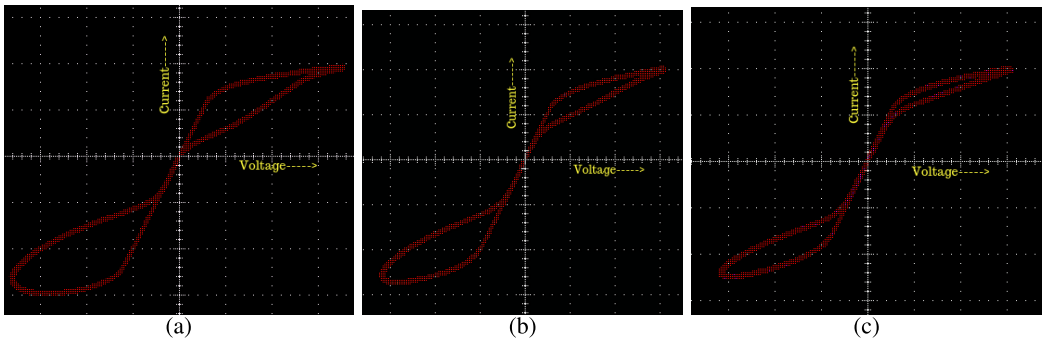
The memristor emulator proposed in [39] consists of a CMOS inverter, which exhibits high dynamic power dissipation, leakage current [52], [55], etc. In contrast, our proposed emulator consists of only four nMOS transistors and an optional external capacitor. The maximum power consumption of the emulator presented in [39] is 128.71 μW, whereas the maximum power consumption of our memristor emulator is 8.24 μW. Thus, it can be stated that our proposed emulator is 36.02× better when compared with [39], considering area utilization and power consumption. Our proposed memristor emulator has an optional external capacitor, which is used to tune the frequency as per the requirement of the applications by changing its value. It works efficiently for a range of frequencies, i.e., a few Hz to MHz, which is thoroughly verified theoretically and experimentally. Although our proposed memristor may work with or without a capacitor up to 2 MHz comfortably, we choose to use an external capacitor in the design to enhance its utilization in practical applications.

It can be observed that the operating frequency of the memristor emulator proposed in [39] is 100 MHz, which is higher compared with our emulator. As stated above, the operating frequency of an emulator depends on the circuit topology and its type. Note that the time constant of the emulator presented in [39] is $B(C_2/C_1)$ times lower than that of the time constant of our proposed emulator. Here, B is a constant, and C_1 and C_2 are the total capacitance of the proposed emulator and the emulator presented in [39], respectively. It is to mention that due to different topologies, each emulator has different parasitic capacitances, which impact the time constants of the emulators. Since the time constant is inversely proportional to the operating frequency, because of the difference in the time constants, the maximum operating frequency of the proposed emulator is lower than the maximum operating frequency of the emulator described in [39]. Although the post-layout I–V characteristics of the memristor presented in [39] range up to 100 MHz, it generates acceptable I–V characteristics only up to 4 Hz, when it is physically validated using discrete transistor arrays (ALD1116 and ALD1117) and a single grounded capacitor of 100 nF. Furthermore, ZnO-based memristor fabricated using direct-current reactive magnetron sputter as described in [39] also exhibits acceptable I–V characteristics only up to 10 Hz. It can also be observed in [39] that with varying frequencies, the PHL of the emulator also shifts its origin, which is not recommended for the reliable behavior of a memristor. Moreover, the physical validation of our proposed memristor emulator depicts acceptable I–V characteristics up to 500 kHz using ALD1106 n-channel MOSFETs and a 4.7-nF external capacitor exhibiting better reliability and performance. In addition, the maximum operating frequency of the memristor emulator presented in [50] is working up to 1 MHz, which is 3× less than the proposed emulator. The



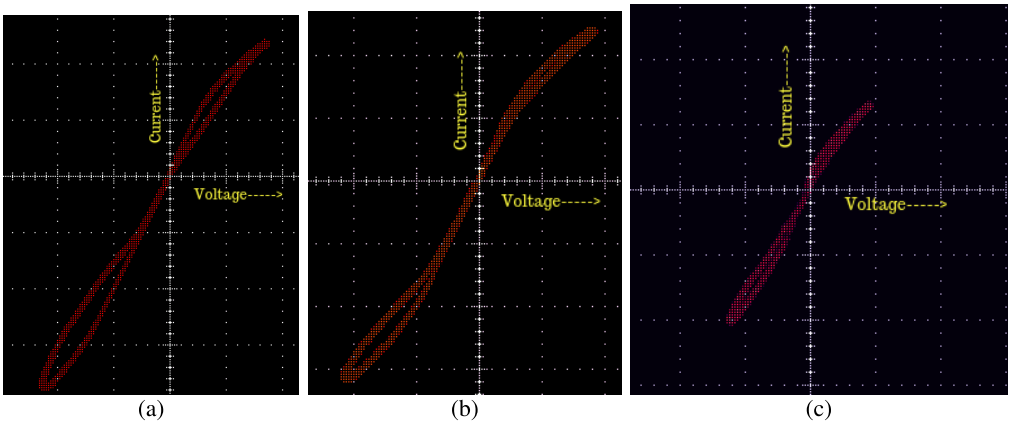
(a) (b) (c)

Fig. 9. Proposed memristor emulator having 0.22-μF capacitor. (a) Transient analysis. (b) PHL at 500 Hz. (c) PHL at 1 kHz.



(a) (b) (c)

Fig. 10. PHL of the proposed memristor emulator having 0.1-μF capacitor at (a) 8 kHz, (b) 16 kHz, and (c) 25 kHz.



(a) (b) (c)

Fig. 11. PHL of the proposed memristor emulator having 4.7-nF capacitor at (a) 40 kHz, (b) 100 kHz, and (c) 500 kHz.

emulator presented in [50] requires an external dc supply and a capacitor additionally. However, the proposed emulator does not require a dc supply, making it a simple circuit element. The maximum area utilization of the emulator presented in [50] is 2803.25 μm^2, which is 17.8$\times$ higher than the proposed emulator. Srivastava et al. [56] presented an MOS-only memristor. The PHLs of this floating emulator are not pinched precisely at the origin, especially at high frequencies, and there is no variation in the positive lobe area of the PHL at 500 kHz and 1 MHz, which violates the frequency-dependent behavior of a memristor. The post-layout analysis is not performed, which is required for the ON-chip performance validation, and also, no application involving the memristor presented in [56] is reported. Due to this, area utilization and power consumption of the memristor proposed in [56] could not be estimated. Furthermore, the experimental result is validated only up to 24 kHz, whereas the proposed emulator is validated for a diverse range of frequencies numerically and experimentally, and the maximum frequency of the experimental result is up to 500 kHz. The emulator reported in [56] relies on the parasitic capacitances of MOSFETs to provide memristive nonlinear behavior and nonvolatile property. As we know, parasitic capacitance gets affected by the applied voltage [67], and thus, it becomes difficult to model the behavior of the emulator reported in [56] accurately. The grounded memristor showcased in [57] requires seven MOSFETs, an external capacitor, and a dual power supply, which exhibits high design complexity and occupies 2.89$\times$ more area than the proposed emulator. The presence of dc bias also introduces static power consumption, which is zero in our circuit because of the

TABLE II
COMPARATIVE ANALYSIS OF THE PROPOSED MEMRISTOR EMULATOR WITH AVAILABLE MEMRISTOR EMULATORS

Ref.	Active comp.	Passive comp.	Transistor counts	Sim./Exp.	Floating/ Grounded	Technology used	Power consumption	Max. operating freq.
[22]	1OTA, 2CFOA	3R, 2C	>56	Both	Grounded	-	260 mW	2 KHz
[23]	2OPAMPs, 1Multiplier, 10Transistors	2R, 1C	>150	Both	Grounded	-	1.81 W	800 Hz
[33]	1DDCC, 1 Multiplier	2R, 1C	50	Sim.	Floating	0.35 μm CMOS	74.5 W	1 MHz
[24]	4CCIIs, 1Multiplier	2R, 1C	>80	Both	Floating	-	596 mW	20.2 KHz
[25]	4CCIIs, 1Multiplier, 1OPAMP	8R, 1C	-	Both	Floating	-	-	120 Hz
[31]	3OTAs, 4CCIIs	6R, 1C	-	Both	Floating	-	1.21 μW	10 KHz
[32]	1OTA, 2Transistors	1C	16	Sim.	Floating	0.18 μm TSMC	8.05 μW	30 Hz
[26]	2CCII, 1Multiplier	2R, 1C	>60	Both	Grounded	-	356 mW	160 KHz
[27]	1CCII, 1Multiplier	1R, 1C	>40	Both	Grounded	-	204 mW	860 KHz
[28]	1MO-OTA, 1Multiplier	1R, 1C	>40	Both	Grounded	-	-	5 KHz
[29]	1CBTA, 1Multiplier	2R, 1C	23	Sim.	Grounded	0.18 μm TSMC CMOS	-	10 KHz
[30]	3CFOAs	4R, 2C, 1D	-	Exp.	Floating	-	-	700 Hz
[34]	1 DVCCTA, 1OTA	3R, 1C	29	Both	Grounded	0.18 μm TSMC CMOS	4.88 mW	1 MHz
[35]	CCTA, CCII	3R, 1C	>35	Both	Floating	-	-	5 MHz
[36]	1VDTA, 1Multiplier	2R, 1C	>32	Both	Floating	0.18 μm CMOS	-	2 MHz
[37]	1OTA, 1CDTA	1C	-	Sim.	Both	-	-	2 MHz
[54]	4Multipliers, 1OPAMP	5R, 3C	-	Both	Floating	-	-	8 KHz
[39]	4MOSFETs	-	4	Both	Grounded	0.18 μm TSMC CMOS	128.71 μW	100 MHz
Proposed	**4MOSFETs**	**1C**	4	**Both**	**Floating**	**0.18 μm TSMC CMOS**	8.24 μW	**3 MHz**

absence of dc bias. Furthermore, the experimental results are not pinched at the origin, which violates the important fingerprint of a memristor, and the applications involving this emulator are not presented. Therefore, based on the experiments, the proposed emulator can be considered an optimal emulator with respect to area, power, and operating frequency.

IV. PROPOSED EMULATOR APPLICATIONS

Memristor has several advantages as it requires less area (sub-nanometer range), less static power dissipation, and nonvolatile memory behavior. To exploit the properties of the memristor, analog and digital applications are designed below using our proposed emulator for validating its adaptiveness as a circuit element.

A. High Pass Filter

A memristor-based high-pass filter is designed using the proposed emulator. The schematic representation of the memristor-based HPF is depicted in Fig. 12(a). By applying an ac magnitude of 1 V with a capacitor C of 10 pF to HPF, as shown in Fig. 12(a), the corresponding frequency response of the filter is depicted in Fig. 12(b). The memristance of a memristor for the sinusoidal signal of $V_m\text{Sin}(2\pi\text{ft})$ can be expressed by the following equation:

$$M_R = R_{\text{avg}} \pm R_{\text{mem}}\text{Sin}(\omega t + \phi) \tag{23}$$

where R_{avg} and $R_{\text{mem}}\text{Sin}(\omega t + \phi)$ are the linear time-invariant and time-variant resistances, respectively; the value of R_{avg} and $R_{\text{mem}}\text{Sin}(\omega t + \phi)$ can be derived from (19). The memristance value depends on the amplitude, frequency, and excitation time of the applied input signal. The cutoff frequency of the high-pass filter can be obtained using the following equation:

$$f = \frac{1}{2\pi C M_R}. \tag{24}$$

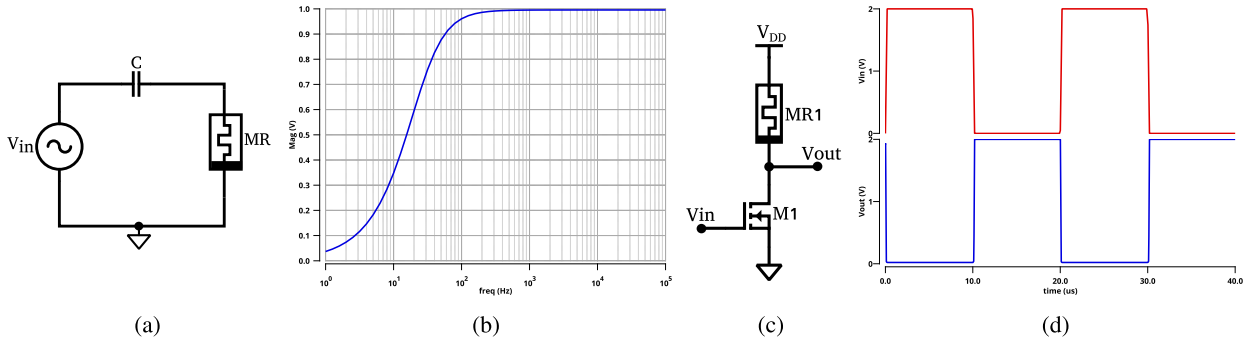


Fig. 12. Memristor-based (a) HPF, (b) frequency response, (c) inverter, and (d) input and output waveforms.

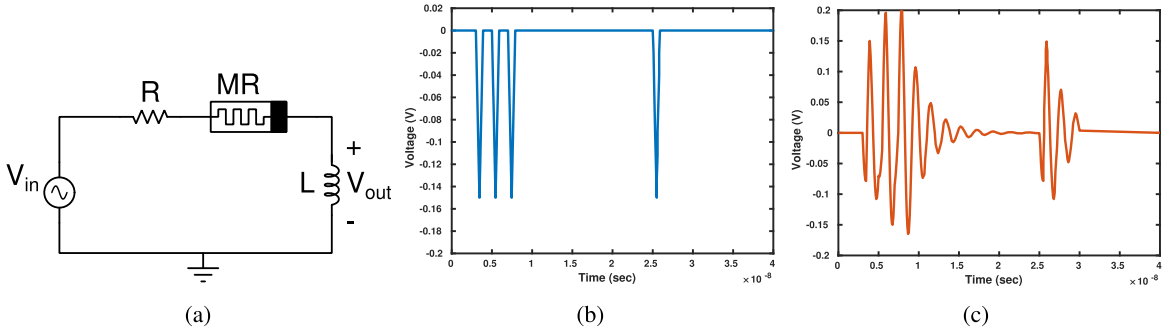


Fig. 13. Adaptive learning (a) schematic, (b) input voltage spikes, and (c) response of the adaptive circuit.

Therefore, the result of HPF exhibits the expected behavior using the proposed emulator, which validates its applicability in analog circuit design.

B. Logic Inverter Design

An inverter designed using a memristor is shown in Fig. 12(c). An nMOS transistor of aspect ratio $W/L = 30\ \mu/0.180\ \mu$ is used in designing this inverter. A square wave of 2 V amplitude and 20 μs period is applied to this circuit. The output of the inverter is illustrated in Fig. 12(d), which is the inverse of the input applied. Note that this aspect ratio, the voltage amplitude, and the time period are arbitrarily chosen to obtain the desired output and can be varied as per the design constraints. For example, the aspect ratios 8 $\mu/0.180\ \mu$ and 2 $\mu/0.180\ \mu$, when square waveforms of 1.2 V and 900 mV having 20- and 80- ns time period are applied, it is verified that the proposed emulator-based inverter produces the desired output.

The proposed emulator offers easier integration with other devices and its flexibility in analog and digital applications is thoroughly verified by designing applications in the domains mentioned above. Therefore, based on the detailed description provided, our proposed four-transistor floating emulator may be considered an optimal floating-type memristor emulator among other memristor emulators.

C. Adaptive Learning Circuit

A memristor can be used in the realization of neuromorphic circuits [58]. Synapses are the key elements for computation and information storage in natural and artificial neural networks. An artificial synapse must remember its past behavior and store a continuous set of states according to the presynaptic and postsynaptic neuronal activity [59]. The nonlinear dynamical behavior of the memristor exhibits the feasibility of imitating the synaptic operation for neural cells, which is demonstrated in [60]. An adaptive neuromorphic architecture (ANA) that self-adjusts its inherent parameters naturally following the stimuli frequency is presented in [61]. This circuit is based on the behavior of the biological organism ameba to its external stimulus. This unicellular organism illustrates puzzle and maze-solving abilities, recalling the past and learning and predicting future occurrences based on its past behavior [62]. An ameba slows down its locomotive speed in response to the changes in temperature and other environmental conditions.

The circuit that realizes the behavior of an ameba is shown in Fig. 13(a), which consists of a resistor ($R = 900\ \Omega$), an inductor ($L = 1\ \mu$H), and the proposed memristor ($C = 0.1$ pF). These three circuit elements are arranged in series to produce a resonance whenever the applied input varies. The applied voltage (V_{in}) signifies a change in the temperature, and the output voltage (V_{out}) across the inductor is analogous to the locomotive speed of an ameba. The correctness of the circuit is verified by applying three negative spikes along with a fourth spike after some delay, as shown in Fig. 13(b). The first three spikes are used to train the circuit, causing oscillations due to the resonant behavior of the circuit, as illustrated in Fig. 13(c). At a fourth input spike, the circuit resonates with the same frequency as earlier, anticipating the next spike, as showcased in Fig. 13(c). The amplitude of the output voltage diminishes in the absence of input spikes, generating

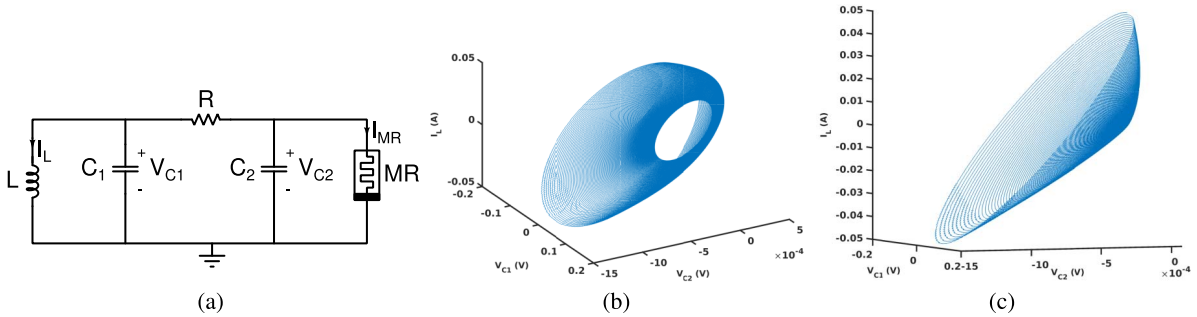


Fig. 14. Chaotic oscillator (a) schematic; (b) $C_1 = 10$ nF, $V_{C1}(0) = 50$ mV, $C_2 = 5$ nF, $R = 1.5$ kΩ, and $L = 0.1$ μH; and (c) $C_1 = 10$ nF, $V_{C1}(0) = 50$ mV, $C_2 = 15$ nF, $R = 500$ Ω, and $L = 0.1$ μH attractors with circuit parameters.

damped oscillations [61]. This validates the behavior of an ameba using a circuit using the proposed emulator.

D. Chaotic Circuit

The proposed memristor-based chaotic oscillator is designed to validate its effectiveness as a nonlinear circuit element. A circuit for generating chaos was introduced by Chua [63] using a well-known Chua circuit. Chua's circuit [64] is realized using one memristor (MR), three energy storage elements, and a linear resistor. The nonlinear property of the proposed MR is used to model a chaotic oscillator along with an inductor (L), two capacitors (C_1 and C_2), and a resistor R, as shown in Fig. 14(a).

The chaotic oscillator is modeled by the following mathematical expressions:

$$\frac{\mathrm{d}\varphi(t)}{\mathrm{d}t} = V_{C1} \tag{25}$$

where $\varphi(t)$ is the flux associated with the inductor, L

$$\frac{\mathrm{d}V_{C1}}{\mathrm{d}t} = \frac{1}{C_1}\left[\frac{V_{C2} - V_{C1}}{R_1} - I_L\right] \tag{26}$$

$$\frac{\mathrm{d}V_{C2}}{\mathrm{d}t} = \frac{1}{C_2}\left[\frac{V_{C1} - V_{C2}}{R_1} - I_{\mathrm{MR}}\right] \tag{27}$$

where I_{MR} is the current flowing through MR. The following mathematical model gives the current passing through the inductor:

$$\frac{\mathrm{d}I_L}{\mathrm{d}t} = \frac{V_{C1}}{L}. \tag{28}$$

The behavior of the chaotic oscillator is obtained using two different combinations of the circuit parameters, as shown in Fig. 14(b) and (c). Due to the proposed memristor, irregular and unpredictable patterns [65] are generated by changing circuit parameters only. Any change in the circuit parameters causes variations in the characteristic of the chaotic oscillator, validating the generation of random and indeterministic attractors. Chaotic oscillators can be leveraged in applications ranging from cryptography, encryption, secure communications, random signal generators, through-wall radar, and robotics. Therefore, the proposed memristor aids in designing a chaotic circuit, reducing the circuit complexity and area compared with other state-of-the-art chaotic oscillators [66]. Thus, the proposed emulator is highly flexible, versatile, and suitable for both general purpose and specific applications.

V. Conclusion

In this article, a new circuit topology for the floating memristor emulator is presented, which consists of four MOSFETs and an external capacitor to realize the expected behavior of a memristor. Its numerical analysis is performed using a Cadence design environment with TSMC 180-nm PDKs. Its characteristics are validated at different operating frequencies, temperatures, and process corners using pre- and post-layout simulations. Our emulator exhibits acceptable characteristics while varying various parameters at different process corners. It is found that the proposed emulator functions reliably from a few Hz to 3 MHz producing acceptable I–V characteristics. Its area utilization and power consumption are 157.48 μm^2 and 8.24 μW, respectively, at the maximum operating frequency of 3 MHz. The functional validation of the proposed emulator is performed experimentally using ALD1106 n-channel MOSFETs in the laboratory, which certifies its coherence with the numerical analysis. The acceptability and applicability of the proposed memristor emulator are showcased using various analog and digital applications. The main advantages of this emulator are its: 1) suitability for monolithic IC fabrication; 2) stable and reliable behavior; 3) high-frequency operation; 4) low power consumption; and 5) less area utilization, which makes it a perfect candidate to be used in the wide range of area and power optimal applications operating at high frequencies.

References

[1] L. O. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.
[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and S. R. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, Jun. 2008.
[3] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, nos. 25–26, pp. 2632–2663, Jul. 2009.
[4] T. D. Dongale et al., "TiO_2 based nanostructured memristor for RRAM and neuromorphic applications: A simulation approach," *Nano Converg.*, vol. 3, no. 1, pp. 1–7, Dec. 2016.
[5] A. Al-Shidaifat, S. Chakrabartty, S. Kumar, S. Acharjee, and H. Song, "A novel characterization and performance measurement of memristor devices for synaptic emulators in advanced neuro-computing," *Micromachines*, vol. 11, no. 1, p. 89, Jan. 2020.
[6] T. A. Wey and W. D. Jemison, "Variable gain amplifier circuit using titanium dioxide memristors," *IET Circuits, Devices Syst.*, vol. 5, no. 1, pp. 59–65, 2011.
[7] M. Itoh and L. O. Chua, "Memristor oscillators," *Int. J. Bifurcation Chaos*, vol. 18, no. 11, pp. 3183–3206, 2008.

[8] X.-B. Tian and H. Xu, "The design and simulation of a titanium oxide memristor-based programmable analog filter in a simulation program with integrated circuit emphasis," *Chin. Phys. B*, vol. 22, no. 8, Aug. 2013, Art. no. 088501.

[9] S. Duan, X. Hu, Z. Dong, L. Wang, and P. Mazumder, "Memristor-based cellular nonlinear/neural network: Design, analysis, and applications," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 26, no. 6, pp. 1202–1213, Jun. 2015.

[10] J. Cong and B. Xiao, "MrFPGA: A novel FPGA architecture with memristor-based reconfiguration," in *Proc. IEEE/ACM Int. Symp. Nanosc. Archit.*, Jun. 2011, pp. 1–8.

[11] A. Ghofrani, A. Rahimi, M. A. Lastras-Montano, L. Benini, R. K. Gupta, and K.-T. Cheng, "Associative memristive memory for approximate computing in GPUs," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 6, no. 2, pp. 222–234, Jun. 2016.

[12] Y. V. Pershin and M. Di Ventra, "Practical approach to programmable analog circuits with memristors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1857–1864, Aug. 2010.

[13] S. Shin, K. Kim, and S. M. Kang, "Memristor applications for programmable analog ICs," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 266–274, Mar. 2011.

[14] M. P. Sah, H. Kim, and L. O. Chua, "Brains are made of memristors," *IEEE Circuits Syst. Mag.*, vol. 14, no. 1, pp. 12–36, 1st Quart., 2014.

[15] M. R. Azghadi, B. Linares-Barranco, D. Abbott, and P. H. W. Leong, "A hybrid CMOS-memristor neuromorphic synapse," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 2, pp. 434–445, Apr. 2017.

[16] G. S. Snider, "Self-organized computation with unreliable, memristive nanodevices," *Nanotechnology*, vol. 18, no. 36, Sep. 2007, Art. no. 365202.

[17] (Mar. 25, 2019). *KNOWM Datasheet Knowm Memristor*. [Online]. Available: https://knowm.org/downloads/Knowm_Memristors.pdf

[18] C. Yakopcic, T. M. Taha, G. Subramanyam, R. E. Pino, and S. Rogers, "A memristor device model," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1436–1438, Oct. 2011.

[19] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold adaptive memristor model," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 211–221, Jan. 2013.

[20] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM: A general model for voltage-controlled memristors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 8, pp. 786–790, Aug. 2015.

[21] S. Kvatinsky, K. Talisveyberg, D. Fliter, A. Kolodny, U. C. Weiser, and E. G. Friedman, "Models of memristors for SPICE simulations," in *Proc. IEEE 27th Conv. Electr. Electron. Eng. Isr.*, Nov. 2012, pp. 1–5.

[22] M. T. Abuelma'atti and Z. J. Khalifa, "A continuous-level memristor emulator and its application in a multivibrator circuit," *AEU-Int. J. Electron. Commun.*, vol. 69, no. 4, pp. 771–775, 2015.

[23] H. Kim, M. P. Sah, C. Yang, S. Cho, and L. O. Chua, "Memristor emulator for memristor circuit applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2422–2431, Oct. 2012.

[24] C. Sánchez-López, J. Mendoza-López, C. Muñiz-Montero, and M. A. Carrasco-Aguilar, "A floating analog memristor emulator circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 309–313, May 2014.

[25] D. Yu, H. H.-C. Iu, A. L. Fitch, and Y. Liang, "A floating memristor emulator based relaxation oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2888–2896, Oct. 2014.

[26] C. Sánchez-López, M. A. Carrasco-Aguilar, and C. Muñiz-Montero, "A 16 Hz–160 kHz memristor emulator circuit," *AEU-Int. J. Electron. Commun.*, vol. 69, no. 9, pp. 1208–1219, 2015.

[27] C. Sánchez-López and L. E. Aguila-Cuapio, "A 860 kHz grounded memristor emulator circuit," *AEU-Int. J. Electron. Commun.*, vol. 73, pp. 23–33, Mar. 2017.

[28] Y. Babacan, A. Yesil, and F. Kacar, "Memristor emulator with tunable characteristic and its experimental results," *AEU-Int. J. Electron. Commun.*, vol. 81, pp. 99–104, Nov. 2017.

[29] U. E. Ayten, S. Minaei, and M. Sağbaş, "Memristor emulator circuits using single CBTA," *AEU-Int. J. Electron. Commun.*, vol. 82, pp. 109–118, Dec. 2017.

[30] M. T. Abuelma'atti and Z. J. Khalifa, "A new memristor emulator and its application in digital modulation," *Analog Integr. Circuits Signal Process.*, vol. 80, no. 3, pp. 577–584, 2014.

[31] H. Sözen and U. Çam, "Electronically tunable memristor emulator circuit," *Analog Integr. Circuits Signal Process.*, vol. 89, no. 3, pp. 655–663, 2016.

[32] Y. Babacan and F. Kaçar, "Floating memristor emulator with subthreshold region," *Analog Integr. Circuits Signal Process.*, vol. 90, no. 2, pp. 471–475, 2017.

[33] A. Yeşil, Y. Babacan, and F. Kaçar, "A new DDCC based memristor emulator circuit and its applications," *Microelectron. J.*, vol. 45, no. 3, pp. 282–287, Mar. 2014.

[34] R. K. Ranjan, N. Raj, N. Bhuwal, and F. Khateb, "Single DVCCTA based high frequency incremental/decremental memristor emulator and its application," *Int. J. Electron. Commun.*, vol. 82, pp. 177–190, Dec. 2017.

[35] R. K. Ranjan, S. Sagar, S. Roushan, B. Kumari, N. Rani, and F. Khateb, "High-frequency floating memristor emulator and its experimental results," *IET Circuits, Devices Syst.*, vol. 13, no. 3, pp. 292–302, 2018.

[36] P. B. Petrović, "Floating incremental/decremental flux-controlled memristor emulator circuit based on single VDTA," *Anal. Integr. Circuits Signal Process.*, vol. 96, no. 3, pp. 417–433, Sep. 2018.

[37] S. Gupta and S. K. Rai, "New grounded and floating decremental/incremental memristor emulators based on CDTA and its application," *Wireless Pers. Commun.*, vol. 113, no. 2, pp. 773–798, Jul. 2020.

[38] S. P. Adhikari, M. P. Sah, H. Kim, and L. O. Chua, "Three fingerprints of memristor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 3008–3021, Nov. 2013.

[39] Y. Babacan, A. Yesil, and F. Gul, "The fabrication and MOSFET-only circuit implementation of semiconductor memristor," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1625–1632, Apr. 2018.

[40] H. Abd and A. König, "A compact four transistor CMOS-design of a floating memristor for adaptive spiking neural networks and corresponding self-X sensor electronics to industry 4.0," *Tm Technisches Messen*, vol. 87, no. s1, pp. s91–s96, Sep. 2020.

[41] M. Maymandi-Nejad and M. Sachdev, "DTMOS technique for low-voltage analog circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 10, pp. 1151–1156, Oct. 2006.

[42] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414–422, Mar. 1997.

[43] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2002.

[44] A. G. Alharbi, M. E. Fouda, Z. J. Khalifa, and M. H. Chowdhury, "Electrical nonlinearity emulation technique for current-controlled memristive devices," *IEEE Access*, vol. 5, pp. 5399–5409, 2017.

[45] K. Eshraghian et al., "Memristive device fundamentals and modeling: Applications to circuits and systems simulation," *Proc. IEEE*, vol. 100, no. 6, pp. 1991–2007, Jun. 2012.

[46] S. Poornima and C. P. Sugumaran, "Investigation of pinched hysteresis of a memristor emulator under ferroresonance," *Appl. Math. Inf. Sci.*, vol. 13, no. 5, pp. 759–767, Sep. 2019.

[47] L. K. Kengne, J. R. Mboupda Pone, and H. B. Fotsin, "Symmetry and asymmetry induced dynamics in a memristive twin-T circuit," *Int. J. Electron.*, vol. 109, no. 2, pp. 337–366, Feb. 2022.

[48] M. P. Sah, C. Yang, H. Kim, B. Muthuswamy, J. Jevtic, and L. Chua, "A generic model of memristors with parasitic components," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 891–898, Mar. 2015.

[49] L. Chua, "If it's pinched it's a memristor," *Semicond. Sci. Technol.*, vol. 29, no. 10, 2014, Art. no. 104001.

[50] J. Vista and A. Ranjan, "A simple floating MOS-memristor for high-frequency applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 5, pp. 1186–1195, May 2019.

[51] Y. Shen, G. Wang, Y. Liang, S. Yu, and H. H.-C. Iu, "Parasitic memcapacitor effects on HP TiO_2 memristor dynamics," *IEEE Access*, vol. 7, pp. 59825–59831, 2019.

[52] G. K. Yeap, *Practical Low Power Digital VLSI Design*. Chicago, IL, USA: Motorola, 2012, doi: 10.1007/978-1-4615-6065-4.

[53] (2021). *Datasheet ALD1106/ALD1116*. [Online]. Available: http://www.aldinc.com/pdf/ALD1116.pdf

[54] D. Yu, X. Zhao, T. Sun, H. H. C. Iu, and T. Fernando, "A simple floating mutator for emulating memristor, memcapacitor, and meminductor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1334–1338, Jul. 2020.

[55] N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. London, U.K.: Pearson Education India, 2015.

[56] P. Srivastava, R. K. Gupta, R. K. Sharma, and R. K. Ranjan, "MOS-only memristor emulator," *Circuits, Syst., Signal Process.*, vol. 39, no. 11, pp. 5848–5861, Nov. 2020.

[57] A. Yesil, "A new grounded memristor emulator based on MOSFET-C," *AEU-Int. J. Electron. Commun.*, vol. 91, pp. 143–149, Jul. 2018.

[58] M. Hu, H. Li, Y. Chen, Q. Wu, G. S. Rose, and R. W. Linderman, "Memristor crossbar-based neuromorphic computing system: A case study," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 25, no. 10, pp. 1864–1878, Oct. 2014.
[59] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Netw.*, vol. 23, no. 7, pp. 881–886, 2010.
[60] H. Kim, M. P. Sah, C. Yang, T. Roska, and L. O. Chua, "Memristor bridge synapses," *Proc. IEEE*, vol. 100, no. 6, pp. 2061–2070, Jun. 2012.
[61] F. Z. Wang et al., "Adaptive neuromorphic architecture (ANA)," *Neural Netw.*, vol. 45, pp. 111–116, Sep. 2013.
[62] T. Nakagaki, R. Kobayashi, Y. Nishiura, and T. Ueda, "Obtaining multiple separate food sources: Behavioural intelligence in the *Physarum plasmodium*," *Proc. Roy. Soc. London. B, Biol. Sci.*, vol. 271, no. 1554, pp. 2305–2310, Nov. 2004.
[63] L. O. Chua, "The genesis Chua's circuit," *Int. J. Electron. Commun.*, vol. 46, no. 4, 1992.
[64] M. P. Kennedy, "Three steps to chaos. II. A Chua's circuit primer," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 40, no. 10, pp. 657–674, Oct. 1993.
[65] L. Pivka, C. W. Wu, and A. Huang, "Chua's oscillator: A compendium of chaotic phenomena," *J. Franklin Inst.*, vol. 331, no. 6, pp. 705–741, Nov. 1994.
[66] B. Muthuswamy and P. P. Kokate, "Memristor-based chaotic circuits," *IETE Tech. Rev.*, vol. 26, no. 6, pp. 417–429, 2009.
[67] K. Gauen, "The effects of MOSFET output capacitance in high frequency applications," in *Proc. Conf. Record IEEE Ind. Appl. Soc. Annu. Meeting*, 1989, pp. 1227–1234.

Ananda Y. R. received the B.E. degree in electronics and communication engineering and the M.Tech. degree in VLSI design and embedded system from Visvesvaraya Technological University, Belgaum, Karnataka, India, in 2011 and 2014, respectively. He is currently working towards a Ph.D. degree at the Department of Electronics and Electrical Engineering, IIT Guwahati, Guwahati, India.

His research interests include memcomputing devices, digital IC design, and analog and mixed-signal integrated circuit design.

Nehal Raj is currently working toward the B.Tech. degree at the Department of Electronics and Communication Engineering, Bhusanayana Mukundadas Sreenivasaiah College of Engineering (BMSCE), Bengaluru, India.

His areas of interest lie in VLSI design for high-speed wireless communication, including 5G, architectures for advanced processing, and networking algorithms.

Gaurav Trivedi (Member, IEEE) received the Ph.D. degree from the Department of Electrical Engineering, IIT Bombay, Mumbai, India, in 2007.

He is currently an Associate Professor with the Department of Electronics and Electrical Engineering, IIT Guwahati, Guwahati, India. His research interests include circuit simulation (analog and digital) and VLSI computer-aided design (CAD), high-performance computing, VLSI cryptographic circuits design, and hardware security.