A High-Swing CMOS Telescopic Operational Amplifier

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***Abstract*— A high-swing, high-performance CMOS telescopic operational amplifier is described. The high swing of the op-amp is achieved by employing the tail and current source transistors in the deep linear region. The resulting degradation in differential gain, common-mode rejection ratio (CMRR), and other amplifier characteristics are compensated by applying regulated-cascode differential gain enhancement and a replica-tail feedback technique. A prototype of the op-amp has been built in a 0.8-μm CMOS process. Operating from a power supply of 3.3 V, it achieves a differential swing of $\pm$2.45 V, a differential gain of 90 dB, unity-gain frequency of 90 MHz, and >50-dB CMRR. It is shown, analytically and through simulations, that the operational amplifier maintains its high CMRR even at high frequencies.**

***Index Terms*—CMOS analog integrated circuits, feedback, gain enhancement, op-amp, operational amplifier, replica tail, telescopic.**

I. Introduction

DESIGNING high-performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifier. At large supply voltages, there is a tradeoff among speed, power, and gain, amongst other performance parameters. Often these parameters present contradictory choices for the op-amp architecture. At reduced supply voltages, output swing becomes yet another performance metric to be considered when designing the op-amp. Of the several architecture alternatives, Fig. 1 shows some of the most popular topologies. Fig. 1(a) shows the design of a simple two-stage amplifier. With all the transistors in the output stage of this amplifier placed in the saturation regime, it has a differential output swing of $2V_{\rm sup} - 4V_{ds,\rm sat}$, where $V_{\rm sup}$ is the supply voltage and $V_{ds,\rm sat}$ is the minimum V_{ds} required to saturate a transistor. For a typical $V_{ds,\rm sat}$ of 200 mV, the differential swing is about $2V_{\rm sup}-$ 0.8 V, which is superior to that of most other topologies. Its nondominant pole, arising from its output node, is located at gm_6/C_L, where gm_6 is the transconductance of transistor M5 or M6 and C_L is the load capacitance. Since this pole is determined by an explicit load capacitance, it typically occurs at a relatively low frequency. As a result, this amplifier has a compromised frequency response. Other drawbacks of this architecture include high power consumption because of two stages in its design and poor negative power-supply rejection (from V_{ss} in the figure) at high frequencies.

The folded-cascode topology is shown in Fig. 1(b). The swing of this design is constrained by its cascoded output stage. Although only $V_{ds,\rm sat}$ is needed to saturate the bottom-most load transistors and the top-most current source transistors, in order to allow for process variations, a small safety margin $V_{\rm margin}$ is often added to V_{ds} to ensure saturation. Accounting for these, and the $V_{ds,\rm sat}$ required across the cascode devices, the differential output swing is $2V_{\rm sup} - 8V_{ds,\rm sat} - 4V_{\rm margin}$. With a voltage margin of 100 mV, this is estimated to be $2V_{\rm sup}-$ 2 V. The second pole of this op-amp is located at $gm_8/\Sigma C_p$, where gm_8 is the transconductance of transistor M7 or M8 and ΣC_p is the sum of the parasitic capacitance contributed from transistors M2, M8, and M10 at the source of transistor M8. Since its second pole frequency is higher than the nondominant pole of a typical two-stage topology, this design has correspondingly superior frequency response. Also, because the compensation for this amplifier terminates to ground in contrast to the two-stage compensation style, it has better high-frequency power-supply rejection ratio (PSRR). The power consumption of this design is approximately the same as that of the two-stage design. Although the current in the output stage can be much smaller than that flowing through the input devices, in practice, the output stage current is picked to be the same or almost the same as the current in the input stage. If the current in the output stage is smaller, a slow common-mode feedback (CMFB) circuit leads to nonsymmetrical output slewing, and the output current becomes the bottleneck for the differential slew rate of the op-amp. On the other hand, if the common-mode feedback is as fast as the differential path of the op-amp, the differential slew rate is independent of the quiescent current in the output, in which case the output current can be reduced without affecting the slew rate. A fast CMFB, however, compromises the differential frequency response. Typically, the differential frequency response is optimized at the cost of slower common-mode feedback. Therefore, it becomes necessary to have the output stage current equal to that of the input stage.

A telescopic cascode op-amp, as shown in Fig. 1(c), typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response stems from the fact that its second pole corresponding to the source nodes of the n-channel cascode devices is determined by the transconductance of n-channel devices as opposed to p-channel devices, as in the case of a folded cascode. Also,

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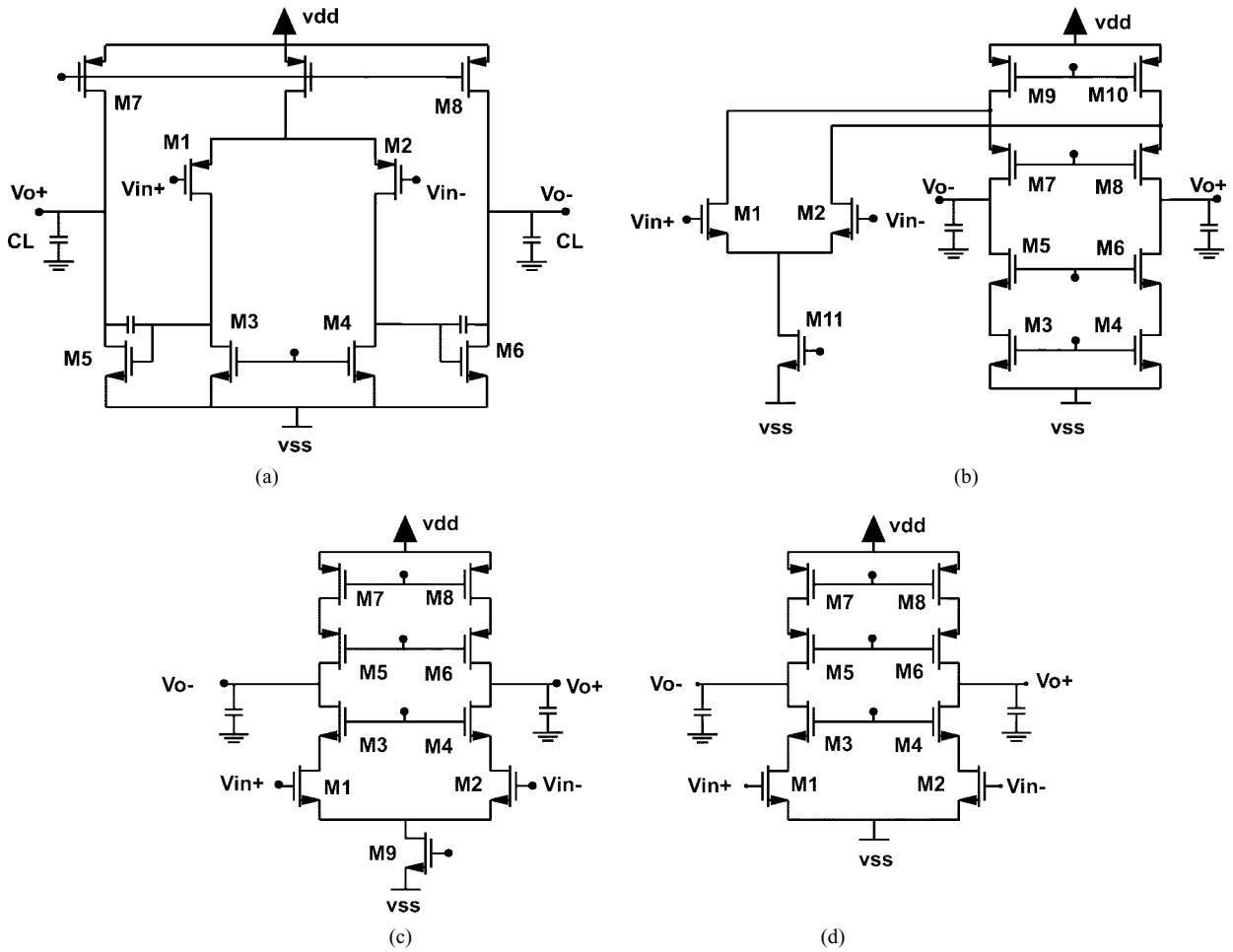


Fig. 1. Conventional op-amp topologies. (a) Two-stage amplifier. (b) Folded-cascode amplifier. (c) Telescopic amplifier. (d) No-tail telescopic amplifier.

the parasitic capacitance at this node arises from only two transistors instead of three, as in the latter. The single stage architecture naturally suggests low power consumption. The disadvantage of a telescopic op-amp is severely limited output swing. It is smaller than that of the folded cascode because the tail transistor directly cuts into the output swing from both sides of the output. In the telescopic op-amp shown in Fig. 1(c), all transistors are biased in the saturation region. Transistors M1–M2, M7–M8, and the tail current source M9 must have at least $V_{ds,\mathrm{sat}}$ to offer good common-mode rejection, frequency response, and gain. The maximum differential output swing of a telescopic op-amp is shown to be $2V_{\mathrm{sup}} - 10V_{ds,\mathrm{sat}} - 6V_{\mathrm{margin}}$. Under identical conditions as before, the output swing of this design can be shown to be limited to $2V_{\mathrm{sup}} - 2.6V$. In a 3-V supply system, this represents a 45% reduction of the available output swing.

At large supply voltages, the telescopic architecture becomes the natural choice for systems requiring moderate gain from the op-amp. Reducing supply voltages, on the other hand, forces reconsideration in favor of the folded cascode, or, in the extreme case, the two-stage design. Although a telescopic op-amp without the tail current source [1] [Fig. 1(d)] improves the differential swing by $2V_{ds,\mathrm{sat}} + 2V_{\mathrm{margin}}$ (600 mV), the common-mode rejection and power-supply rejection of such a circuit is greatly compromised. Moreover, the performance parameters (such as unity-gain frequency and settling time) of an op-amp with no tail or with a tail transistor in the linear region is sensitive to input common-mode and supply-voltage variation, which is undesirable in most analog systems.

Other op-amps that have traditionally been employed in high-performance applications include the class AB op-amp [2]. This amplifier, however, requires a minimum supply voltage of $2V_t + 4V_{ds,\mathrm{sat}} + 2V_{\mathrm{margin}}$, where V_t is the threshold. For V_t of 0.8 V, V_{sup} must be greater than 2.6 V. This requirement renders this architecture unsuitable in future low-voltage applications. Other drawbacks include degraded frequency response because of the presence of current mirrors (which lead to pole-zero doublets in the differential path) and large op-amp noise. Other rail-to-rail amplifiers with class-AB-type output stage [3] deliver very high swing. These too, however, typically require current mirrors in the differential path with a high minimum supply-voltage requirement.

This paper presents a design that combines the low-power, high-speed advantage of the telescopic architecture with the high-swing capability of the folded cascode and the two-stage design. It achieves its high performance while maintaining high common-mode and supply rejection and ensuring constant performance parameters. The techniques described are general and can potentially be applied to improve the performance of some other topologies as well.

II. High-Swing Operational Amplifier

A. Importance of High Swing in Operational Amplifiers

In analog circuits where kT/C noise is the dominant noise, the relationship between op-amp performance metrics such as speed, signal-to-noise ratio (SNR), and power consumption can be shown to be

$$\frac{\text{SNR} \cdot \text{Speed}}{\text{Power}} = \frac{(\text{Swing})^2}{\gamma\left(\frac{kT}{C}\right)} \cdot \frac{\beta\left(\frac{gm}{C}\right)}{V_{\text{sup}} \cdot (\lambda I)} \tag{1}$$

where the constants β, γ, and λ are the feedback factor of the closed-loop op-amp, the number of kT/C noise contributions at the output of the amplifier, and the ratio of the total current consumption of the op-amp to the current I flowing through one of the input devices, respectively. Here, speed corresponds to the dominant pole location of the op-amp.

The above expression simplifies to

$$\frac{\text{SNR} \cdot \text{Speed}}{\text{Power}} \propto \frac{(\text{Swing})^2}{V_{\text{sup}}} \tag{2}$$

when $gm \propto I$, as in the case when the input devices are in weak inversion or in the saturation region of strong inversion. The proportionality constant in the last term is a function of the architecture of the op-amp and the switched-capacitor circuitry around the op-amp. It is clear from this expression that increase in the swing of the op-amp leads to overall performance improvement that can be exploited to achieve lower power or higher SNR or speed.

B. Methodology for Improved Swing

In the topology shown in Fig. 2, transistors M7–M9 are deliberately driven deep into the linear region. Since these transistors normally operate in the linear region, V_{margin} is not needed across these devices. Under these conditions, the output swing is shown to be $2V_{\text{sup}} - 6V_{ds,\text{sat}} - 2V_{\text{margin}} - 2V_{ds,\text{lin-tail}} - 2V_{ds,\text{lin-load}}$, where $V_{ds,\text{lin-tail}}$ and $V_{ds,\text{lin-load}}$ are the drain-to-source voltages for the tail and load transistors, respectively. With $V_{ds,\text{sat}}$ of 200 mV, V_{margin} of 100 mV, $V_{ds,\text{lin-tail}}$ of 80 mV, and $V_{ds,\text{lin-load}}$ of 160 mV, the differential output swing is $2V_{\text{sup}} -$ 1.88 V, which is superior not only to a telescopic amplifier by about 0.7 V but also to a regular folded-cascode amplifier by roughly 100 mV. The swing enhancement stems not only from the difference between $V_{ds,\text{sat}}$ and the voltage across the devices in the linear region but also because of the fact that we no longer need V_{margin} across devices placed in the linear region. It is important to note that any reduction in voltage across the tail transistor improves differential swing twofold as the tail transistor cuts into the output swing from both sides of the amplifier. Also, the elimination of V_{margin} across the tail and the load devices itself contributes to a swing enhancement of $4V_{\text{margin}}$. This benefit of increased swing by pushing the load and tail transistors in the linear region, however, is accompanied by degraded common-mode rejection ratio (CMRR), PSRR, and differential gain of the amplifier. Additionally, as in the case of the no-tail telescopic amplifier, performance parameters of the amplifier are sensitive to the input common-mode voltage level. The reduction in dc gain has been compensated for by a regulated cascode gain enhancement scheme, and a replica-tail feedback technique is used to recover the CMRR and PSRR and to ensure constant performance parameters for the op-amp.

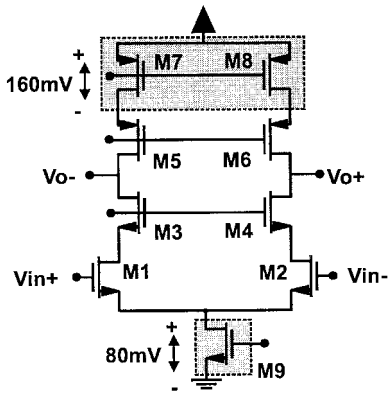


Fig. 2. Methodology for enhancing swing.

C. Regulated Cascode for Recovering Gain

The gain enhancement used in the amplifier employs the well-known differential regulated cascode [4] structure, as shown in Fig. 3(a), with the difference being the presence of a third input in the gain-enhancement amplifiers [5] to bias the load transistors and the input devices in the linear and saturation region, respectively. In addition, the bottom gain-enhancement amplifier incorporates part of the replica-tail feedback scheme, as will be described in Section III-A. Fig. 3(b) illustrates the tradeoff between differential gain and swing of the op-amp. Pushing the load devices deeper into the linear region increases swing at the cost of reduced gain. This tradeoff can be invoked as long as the gain of the op-amp is greater than the application requirements. The dot on the curve represents the operating point for the op-amp presented in this paper, as will be described.

D. Concept of Replica-Tail Feedback Technique

The concept of the replica tail feedback is illustrated in Fig. 4(a). The basic goal of the replica tail feedback is to keep the tail current constant despite variations in the input common-mode voltage level. It accomplishes this by sensing the drain-to-source voltage across the transistor and modulating its gate voltage. The circuit realization of the "feedback circuit" is shown in Fig. 4(b). Transistors M1, M2, and M9 represent the input devices and tail current source of a differential amplifier, while M1R, M2R, and M9R form their corresponding replicas. A constant current Ic is forced through the replica transistors. Amplifier Ao is placed in negative feedback across the replica circuitry, which forces the voltage at node y to be equal to the voltage V_{pc} at the third input of the gain-amp. Also, the common-mode gain of the gain enhancement amplifier A2 forces the common-mode component of the drain voltages of M1 and M2 to be equal to the voltage V_{pc}. Under these conditions, it can be

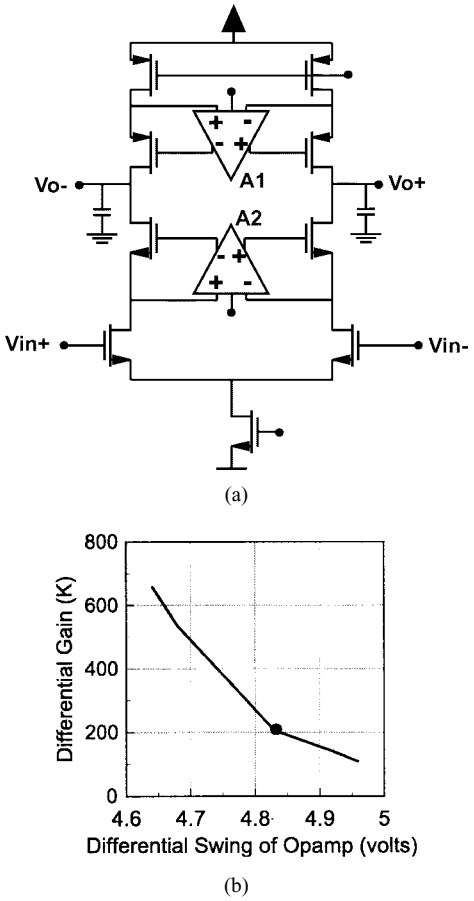


Fig. 3. (a) Regulated cascode scheme to recover differential gain. (b) Variation of differential gain with differential swing of op-amp.

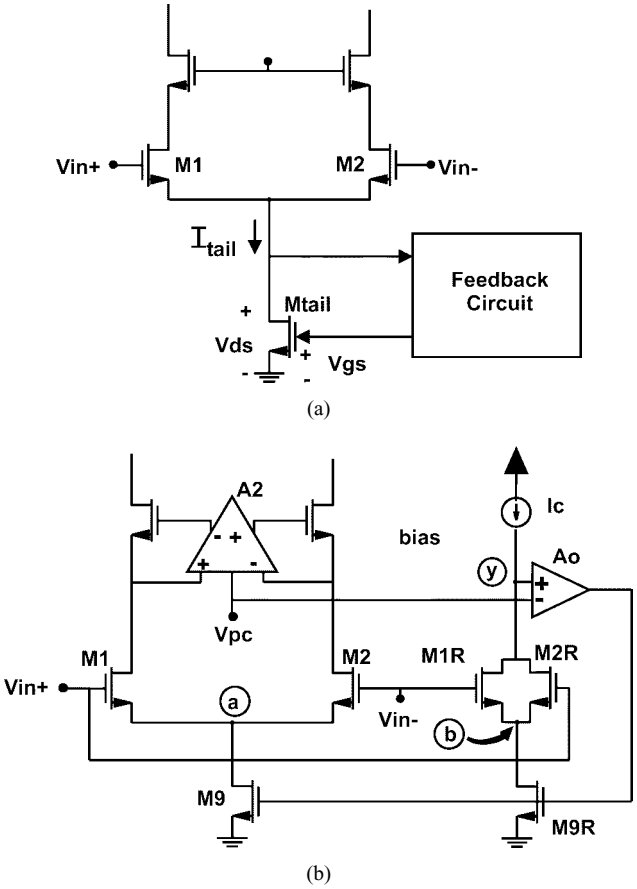


Fig. 4. (a) Basic concept of replica-tail feedback. (b) Circuit realization of replica-tail feedback.

shown that the voltage at the drain of the tail transistor (node a) always equals the voltage at the drain of the replica tail transistor (node b). Since current through M9R is fixed by Ic, current through M9 must also remain fixed, thus suggesting a larger "effective" resistance looking into the tail transistor. This "excess tail resistance" can be traded off for output swing by pushing M9 into the deep linear region while retaining the CMRR and PSRR of the conventional telescopic amplifier. A similar technique was proposed for the tail current of a two-stage amplifier, but without silicon results [6]. It can be shown that our method, however, provides superior CMRR and PSRR by ensuring better replica-main circuit match by making use of a gain-enhancement amplifier.

Under the conditions that the main and replica circuits are perfectly matched, small-signal analysis shows that the effective resistance looking into the tail-current transistor can be approximated as

$$R_{\text{tail}} = ro_9(1 + Ao \cdot (gm_{9R} \cdot ro_{9R}) \cdot (gm_{1R} \cdot ro_{1R})). \quad (3)$$

Since $M9R$ is in the linear region, its product $gm \cdot ro$ is less than unity. Thus, the enhancement is mainly provided by the product of Ao and $gm_{1R} \cdot ro_{1R}$. It is intuitively consistent to note that the enhancement in the effective resistance equals the loop gain of the replica loop.

III. Implementation of Op-Amp

A. Circuit Description

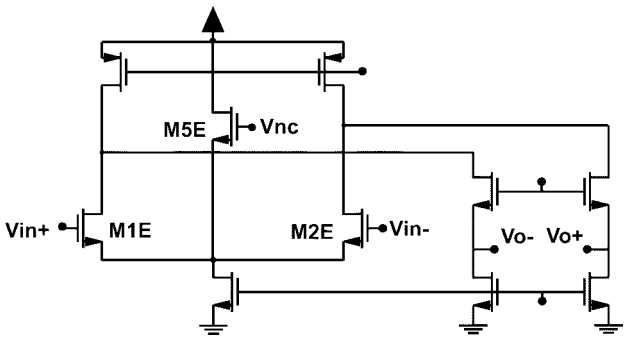
The internal structure of the gain enhancement amplifier A1, as shown in Fig. 3(a), is depicted in Fig. 5(a). This amplifier uses a standard folded-cascode architecture; the choice of architecture was determined by requirements of speed and desired input/output voltage levels. The third input (applied at the gate of transistor M5E) sets the drain voltages of M7 and M8 in the main amplifier. Fig. 5(b) shows a complementary version of the amplifier A1. Normally, an amplifier of this type would serve as the lower gain enhancement amplifier A2. We have modified this architecture [Fig. 5(c)] to incorporate the amplifier Ao used in the negative feedback loop across the replica circuit. The basic idea is to split the third input transistor M3W, in the circuit on the left, to create a new differential pair consisting of transistors M3X and M4X, and transistors M7X and M8X acting as an active load, as shown in the shaded region. The differential amplifier, thus realized, serves as the replica amplifier Ao with output V_t. Viewed in the common-mode sense, this differential pair still acts like the third input that enables us to set the dc level of the common-mode voltage at the drains of the input devices of the main amplifier as before. This implementation has several advantages. First, the current through the single third input transistor is being reused in the new differential pair. Hence, no additional power consumption is required to

construct amplifier Ao. Second, since the differential gain enhancement amplifier (with input transistors M1X and M2X) is in common-mode unity-gain feedback across the cascode devices in the telescopic amplifier, the common-mode voltage at the inputs of this enhancement amplifier equals the common-mode voltage of the inputs of amplifier Ao. Also, since amplifier Ao is in negative feedback, its inputs are virtually shorted. Hence, the voltage at the drain of transistors M1R and M2R (node y), as seen in Fig. 4(b), tracks the common-mode voltage at the drains of transistors M1 and M2, thus ensuring good replica-main matching, which improves the performance of the replica-tail feedback technique. Additionally, this implementation allows simultaneous setting of the dc levels of the common-mode voltage at the drains of the input devices and the replica input devices and ensures their equality.

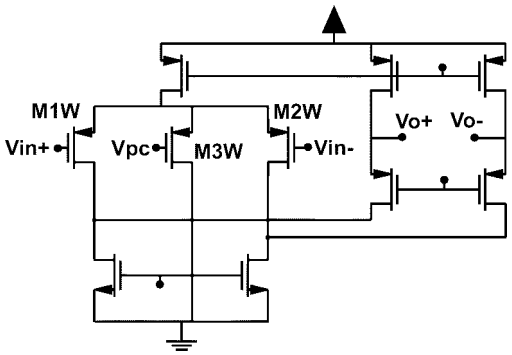
The overall implementation of the operational amplifier is shown in Fig. 5(d). The common-mode loop, as highlighted by the dashed path, can be regarded as a two-stage amplifier, with the replica amplifier Ao as the first stage and the replica circuit as the second stage. Capacitance Cc is used to push the pole corresponding to node y (or the second stage pole) to a higher frequency. Note that the unity-gain frequency of the replica-loop is determined by the ratio of the transconductance of the replica amplifier to the capacitance Cc. The gain amps, on the other hand, are stabilized by the combination of an explicit capacitance and parasitic capacitance at the gates of the cascode devices. A cascode current mirror is used to supply the current to the replica circuit. For the common-mode feedback, the standard switched-capacitor circuit is employed.

B. Optimization of Power Consumption and Area

Since the replica circuit and the gain enhancement amplifiers drive much smaller capacitive loads than the main amplifier, it is possible to scale down these circuits with respect to the main amplifier. Here, scaling entails reducing the device widths and current through the transistors. Such scaling will not change the voltage levels at various nodes in the circuit. This process allows us to minimize power consumption and area associated with the gain enhancement and replica tail feedback. The process of scaling reduces the nondominant pole location of the two-stage amplifier in the replica loop and would ultimately force the reduction of the unity-gain frequency (given the need for adequate phase margin) of the loop, which in turn would degrade the high-frequency PSRR and CMRR of the overall amplifier. Thus, the limit to such scaling is determined by the requirements of high-frequency CMRR and PSRR on the amplifier. In this implementation, the transistor widths and current in the replica circuitry were scaled by a factor of four, while 2.6 is the scaling factor employed for the gain enhancement amplifiers. These circuits can be scaled further; such aggressive scaling, however, was not executed here because the main idea in this paper was to forward the concept. After scaling, the power consumed by both gain-enhancement amplifiers combined is about a third of the total power consumption of the op-amp.



(a)



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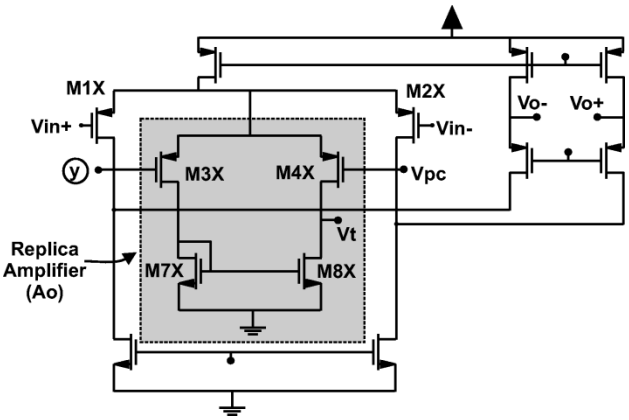

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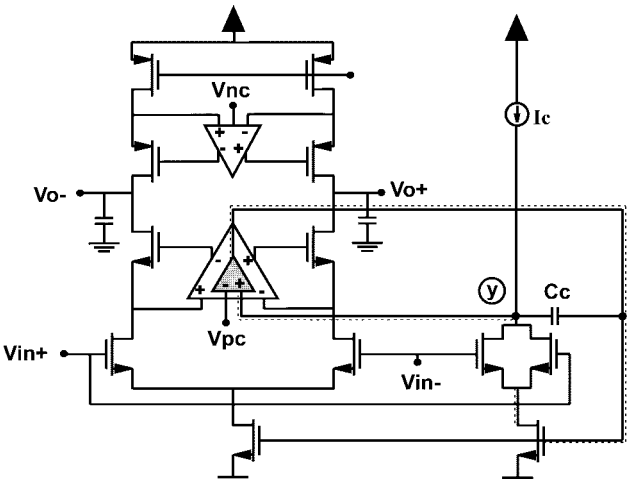


(d)

Fig. 5. Gain amp across p-channel cascodes. (b) and (c) Gain amp across n-channel cascodes. (d) Overall implementation.

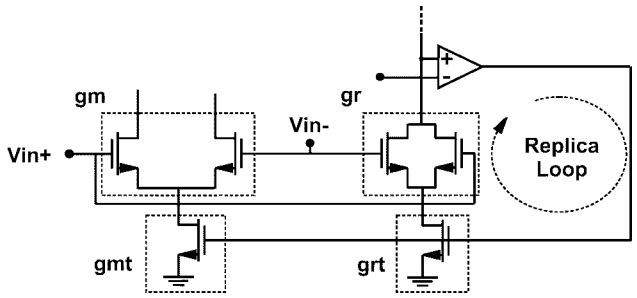


Fig. 6. Effect of mismatch.

C. Effect of Mismatch

Previous analysis in this paper assumes that the main and replica circuits are perfectly matched. In practice, mismatch limits the effectiveness of the replica-tail feedback, thereby limiting the enhancement of common-mode rejection that arises from the use of this scheme. It can be shown that the effective output resistance and CMRR enhancement due to the replica circuit can be described by

Condition	Enhancement
$\Delta_{\rm rep} \ll \dfrac{1}{A_{\rm loop}}$	$1 + A_{\rm loop}$
$\Delta_{\rm rep} \gg \dfrac{1}{A_{\rm loop}}$	$\dfrac{1}{\Delta_{\rm rep}}$

where $\Delta_{\rm rep}$ is a factor that encapsulates the mismatch between the main and the replica circuits and can be expressed as $\Delta_{\rm rep} = 1 - (g_r/g_{rt})/(g_m/g_{mt})$ when the tail transistors are in the deep linear region. Here, g_r, g_{rt}, g_m, and g_{mt} are the transconductances of the replica and the main transistors, as shown in Fig. 6. Please refer to the appendix for details.

If the main-replica mismatch as embodied by the mismatch factor is very small, the enhancement factor equals the loop gain of the replica circuit. Mismatch, on the other hand, leads to reduced enhancement.

D. High-Frequency Behavior of CMRR

The first pole for the common-mode rejection of the amplifier can be shown to be located at $\omega_{pr} + \Delta_{\rm rep} \cdot (\omega_{pr} \cdot A_{\rm loop})$, where $\Delta_{\rm rep}$ is the mismatch factor as defined above, ω_{pr} is the pole location for the open-loop replica circuit, and $A_{\rm loop}$ is the replica circuit loop gain (see appendix). For the second condition as defined in the previous subsection, i.e., for $\Delta_{\rm rep} \gg (1/A_{\rm loop})$, the first pole location of the CMRR is equal to $\Delta_{\rm rep} \cdot (\omega_{pr} \cdot A_{\rm loop})$, where $\omega_{pr} \cdot A_{\rm loop}$ is essentially the unity-gain frequency of the replica circuit over its loop. Mismatch between the main and replica circuits, as mentioned in the previous section, reduces the CMRR enhancement achievable by replica-tail feedback scheme. However, increasing mismatch leads to increased CMRR bandwidth (as represented by its first pole location). In fact, it can be shown that the product of the CMRR at dc and the bandwidth of the CMRR is independent of the main-replica mismatch.

Fig. 7 depicts the simulated high-frequency behavior of the common-mode rejection of the replica-tail feedback telescopic operational amplifier, with and without mismatch between the main and replica circuitry, and compares them to a telescopic topology without the replica feedback. Curve (a) in the figure illustrates the CMRR-frequency dependency for the op-amp using the replica feedback scheme with no main-replica mismatch. The CMRR for the amplifier employing replica-tail feedback with certain mismatch applied between the replica circuit (transistors M1R, M2R, and M9R) and the main circuit (transistors M1, M2, and M9) is shown by curve (b). The mismatch applied between the main and the replica transistors that are supposed to match is $\Delta V_t = 1$ mV for the V_t mismatch and $\Delta L = 0.02$ μm for the length mismatch. Curve (c) is the case when the V_t mismatch between the main and the replica transistors is increased to 10 mV with the same length mismatch as in (b). The increase in CMRR bandwidth with an increase in mismatch is clearly evident from these curves. Curve (d) shows the behavior of the common-mode rejection for the amplifier that does not use the replica-tail scheme while still employing the tail transistor in the linear region. This simulation assumes a differential mismatch (between the input transistors and that between the load devices of the main amplifier) of $\Delta V_t = 1$ mV and $\Delta L = 0.02$ μm that is constant for all four cases.

IV. Experimental Results

The op-amp shown in Fig. 5(d) has been implemented in a standard 0.8-μm n-well, single-poly, double-metal CMOS process. The microphotograph of the chip is shown in Fig. 8. It occupies a die area of 600 $\times$ 630 μm and consumes a total power of 4.8 mW at a 3.3-V supply. As indicated earlier, both the area and power consumption can be further minimized by additional scaling of the replica and the gain enhancement amplifiers. To minimize the mismatch between the main and the replica circuits, a cross-quad layout was employed for the critical transistors.

Fig. 9 shows the transfer characteristic of the amplifier. The "hysteresis-type" behavior observed in the curves occurs due to the phase difference between the input and the output of the amplifier at the 500-Hz frequency at which this measurement was taken. The maximum output range and the slope of this characteristic near its midpoint were used to estimate the swing and the differential gain of the amplifier, respectively.

Fig. 10(a) shows the test circuit employed for measuring the settling time of the amplifier. For this measurement, the op-amp was placed in negative feedback using periodically refreshed capacitors in the feedback path. Fig. 10(b) and (c) shows the measured small-signal and large-signal step response, respectively, of the amplifier. With a 3.65-pF capacitive load and a noise gain of greater than two, the 1% settling time of the amplifier is measured to be 26 ns. The slew rate of the amplifier, as estimated from the large signal step response, is 125 mV/ns.

The chip specifications and performance summary are given in Tables I and II, respectively. The discrepancy between the measured and simulated settling time is attributed to the finite settling time of approximately 10 ns (at a 1% precision)

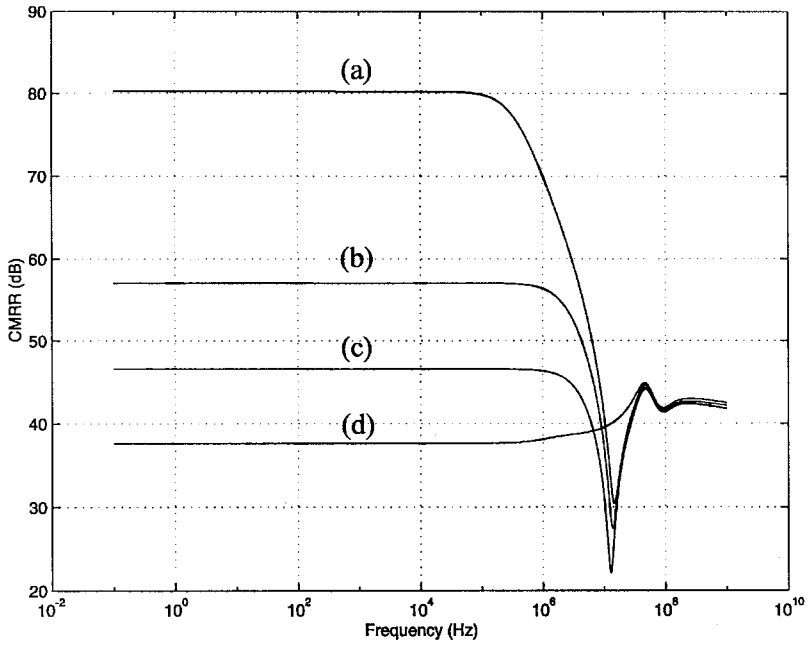


Fig. 7. Behavior of CMRR with frequency.

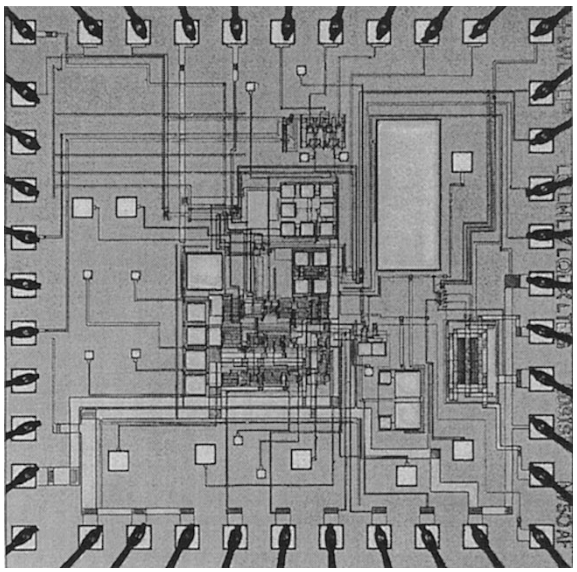


Fig. 8. Op-amp microphotograph.

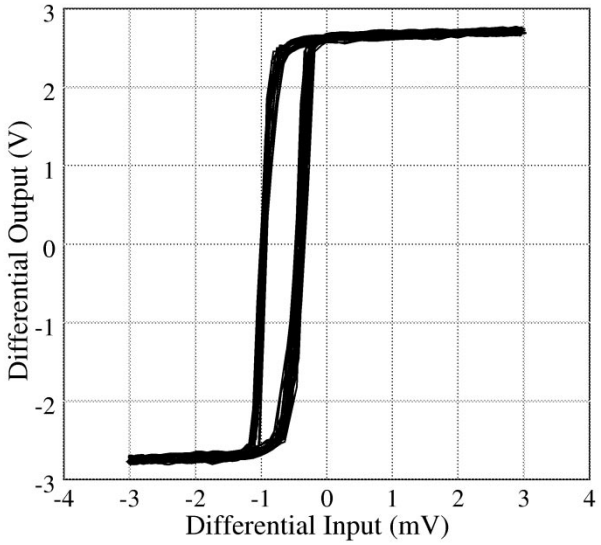
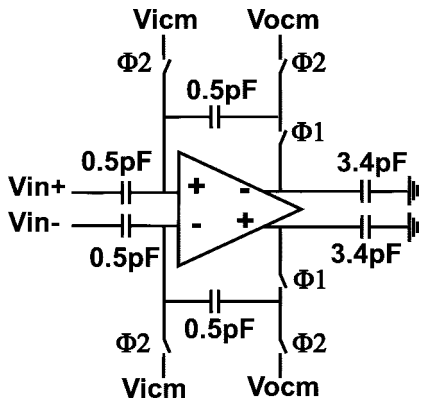


Fig. 9. Transfer characteristic of op-amp.

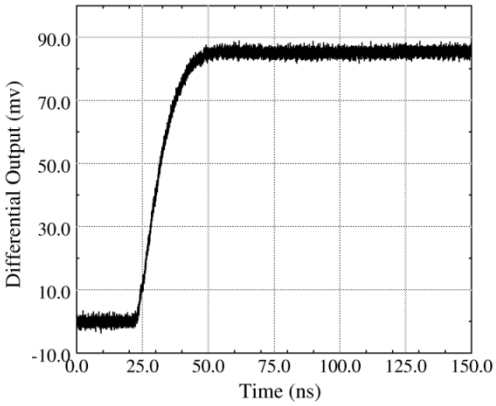
of the input waveform itself. The amplifier has a measured differential output swing of ±2.45 V at a voltage supply of 3.3 V. The swing of the amplifier has been estimated from the maximum output range at which the amplifier maintains a differential small-signal gain of at least 66 dB. At a capacitive loading of 3.52 pF, its measured unity-gain frequency is 90 MHz. The CMRR of the op-amp is greater than 50 dB, and its differential gain is 90 dB, both measured at a frequency of 500 Hz. Telescopic-style op-amps typically have a limited input common-mode voltage range. This op-amp has a simulated input common-mode voltage range of 220 mV about the nominal input common-mode voltage level measured at the points where the small-signal differential gain drops to 90% of its nominal value; note, however, that the application of this op-amp is in a switched-capacitor environment where the common-mode voltage remains fairly fixed.

V. Conclusions

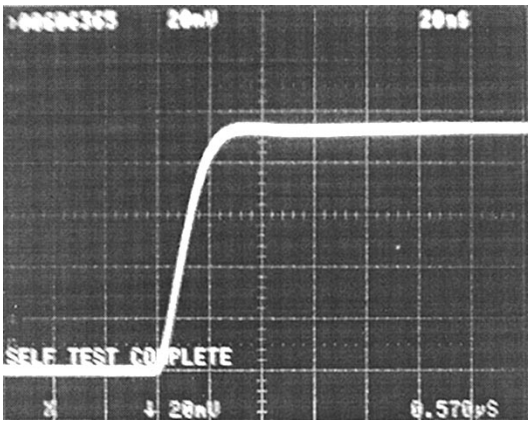
With supply voltages becoming more limited, op-amp output swing becomes an extremely critical parameter. While the telescopic architecture achieves superior speed and power consumption, it has a very limited output swing. The proposed design combines the high-speed, low-power advantage of the telescopic architecture with the high-swing capability of the folded cascode and the two-stage design while maintaining high common-mode and supply rejection and ensuring con-



(a)



(b)



(c)

Fig. 10. Step response of op-amp. (a) Test setup. (b) Small-signal step response. (c) Large-signal step response (horizontal: 20 ns/div; vertical: 200 mV/div considering picoprobe attenuation).

stant performance parameters. The techniques we describe are general and can potentially be applied to improve the performance of some other topologies as well. We have experimentally demonstrated an amplifier with an output swing of ± 2.45 V at a supply of 3.3 V, unity-gain frequency of 90 MHz, and power consumption of 4.8 mW at a capacitive load of 3.6 pF, and >50 dB of CMRR. We have shown, qualitatively and through simulations, that the amplifier maintains its high CMRR even at high frequencies. In light of ever decreasing supply voltages, this op-amp serves as an attractive alternative to conventional topologies.

TABLE I
CHIP SPECIFICATIONS

Technology	0.8μm CMOS
Power Supply	3.3 V
Die Size	600μm x 630μm
Power Consumption	4.8mW

TABLE II
OP-AMP MEASURED AND SIMULATED PERFORMANCE

Opamp Specification	Simulation	Measurement
Differential Open Loop Gain (500Hz)	105db	90dB
Differential Output Swing	±2.4V	±2.45V
Unity Gain Frequency (Output Load=3.52pf)	93MHz	90MHz
Phase Margin	78°	—
Settling Time (1%; noise gain > 2, Output Load ~ 3.65pF)	17.3ns	26ns
Slew Rate	133mV/ns	125mV/ns
Offset (typical)	9.5mv	1-2mv
CMRR (500Hz)	57dB	>50dB

APPENDIX

To understand the interaction of the replica circuitry with the main amplifier, it is useful to look at the entire transistor-level circuitry in the common-mode sense assuming that the input to the amplifier is a pure common-mode signal. Fig. 11 shows the transformation of the full circuit [Fig. 11(a)] to its common-mode counterpart [Fig. 11(b)]. A simplified model for the common-mode circuit is shown in Fig. 12(a). The top half shows the model for the main circuit, while the bottom part represents the replica circuitry. For simplicity, the common-mode feedback is not shown here, and a first-order model is assumed for the replica circuit. The analysis will first be carried out at dc; the results will then be generalized for all frequencies. The transconductance of the tail and the replica-tail transistors is g_t and g_{rt}, respectively, as shown in Fig. 11. R_{om} is the total common-mode small-signal resistance at the output of the main amplifier, while R_{or} is the corresponding small-signal resistance at the output of the replica amplifier. The transconductances G_m and G_r are the source-degenerated transconductance of the main and replica input devices. The degeneration of the transconductance stems from the nonzero intrinsic small-signal resistance of the main and replica-tail transistors. Although degeneration of the input devices is nominal when the tails are in the deep linear region, this effect has been taken into account for generality. The degenerated transconductances can be approximately expressed as

$$G_m = \frac{g_m}{1 + gm \cdot r_t} \tag{4}$$

and

$$G_r = \frac{g_r}{1 + g_r \cdot r_{rt}}. \tag{5}$$

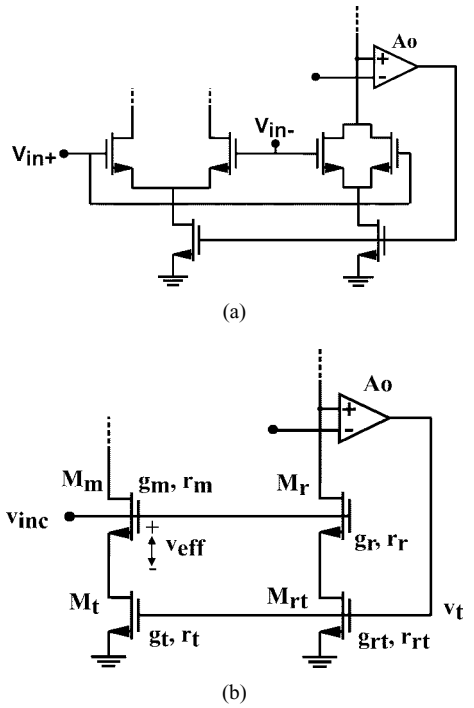


Fig. 11. Differential to common-mode transformation for replica-tail feedback circuit.

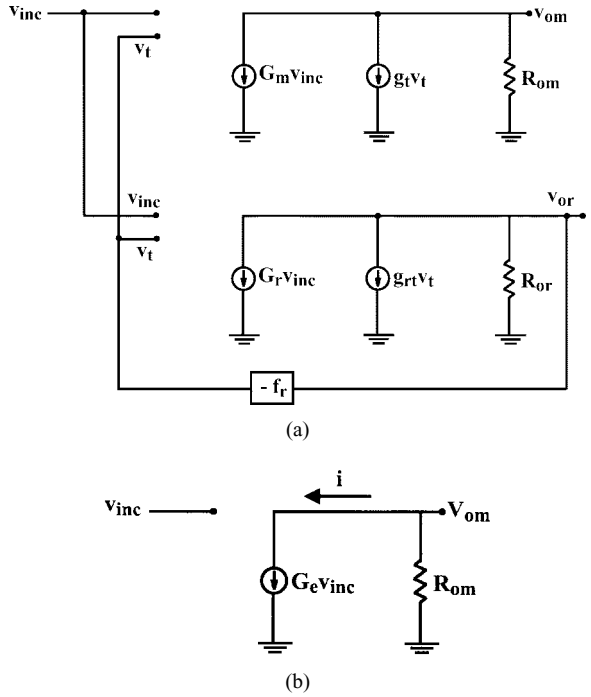


Fig. 12. (a) Small-signal model for the common-mode op-amp circuit. (b) Simplified common-mode op-amp model.

f_r is the feedback factor in the replica loop that, in this case, represents the gain of the replica amplifier. From this model, the open-loop transfer function of the replica-loop can be written as

$$\frac{v_{or}}{v_{\text{inc}}} = \frac{G_r \cdot R_{or}}{1 + f_r \cdot g_{rt} \cdot R_{or}} \tag{6}$$

which can simply be obtained using Black's formula. Representing v_t in terms of v_{inc}, the model in Fig. 12(a) can be simplified as shown in Fig. 12(b). The effective transconductance G_e of the overall model is

$$G_e = G_m \cdot \left(\frac{1 + A_{\text{loop}} \cdot \Delta_{\text{rep}}}{1 + A_{\text{loop}}} \right) \tag{7}$$

where

$$A_{\text{loop}} = f_r \cdot g_{rt} \cdot R_{or} \tag{8}$$

which represents the gain through the replica loop and

$$\Delta_{\text{rep}} = 1 - \frac{g_t}{g_{rt}} \cdot \frac{G_r}{G_m}. \tag{9}$$

Here, Δ_{rep} encapsulates the mismatch between the main and the replica circuits.

Until now, we have shown a model for the common-mode path of the amplifier. To extract the CMRR of the amplifier, note that the common-mode small-signal voltage that eventually appears across the gate-to-source nodes of the main input devices, shown as v_{eff} in Fig. 11(b), for a certain common-mode input voltage v_{inc}, can be obtained by referring the common-mode current i to the voltage across the gate-to-source nodes of the input transistors. Mathematically, this can be expressed as $v_{\text{eff}} = i/g_m$, where g_m is the intrinsic transconductance of the input devices. The transfer function from the input to v_{eff} can be written as

$$T = \frac{v_{\text{eff}}}{v_{\text{inc}}} = \left(\frac{1}{1 + g_m \cdot r_t} \right) \cdot \left(\frac{1 + A_{\text{loop}} \cdot \Delta_{\text{rep}}}{1 + A_{\text{loop}}} \right). \tag{10}$$

Noting that v_{eff} is amplified by the asymmetry in the main input devices to eventually create a differential signal at the output of the op-amp, the CMRR of the amplifier is inversely proportional to T. Rewriting

$$\text{CMRR} \propto (1 + g_m \cdot r_t) \cdot \left(\frac{1 + A_{\text{loop}}}{1 + A_{\text{loop}} \cdot \Delta_{\text{rep}}} \right) \tag{11}$$

which takes into account both the source degeneration due to the intrinsic resistance of the tail transistor (shown by the first term) as well as the CMRR enhancement due to the replica-tail feedback (shown by the second term). The enhancement in CMRR due to the replica circuit can be emulated in an amplifier merely by employing a tail transistor with a larger small-signal resistance R_{efftail}. The value of R_{efftail} gives us an idea of the effectiveness of the replica-tail circuitry. Using the above expression, the effective tail resistance can be found to be $R_{\text{efftail}} = R_{\text{tail}} \cdot (1 + A_{\text{loop}})$ for small main-replica mismatch. Thus, the resistance of the tail is enhanced by the loop gain of the replica-loop.

The frequency behavior of the CMRR can be obtained by employing the following transformations:

$$A_{\text{loop}} \rightarrow A_{\text{loop}}(s) = \frac{A_{\text{loop}}}{1 + \left(\frac{s}{\omega_{pr}} \right)}$$

$$r_t \rightarrow \frac{r_t}{1 + s \cdot (r_t \cdot C_t)}$$

and

$$r_{tr} \rightarrow \frac{r_{tr}}{1 + s \cdot (r_{tr} \cdot C_{tr})} \tag{12}$$

where ω_{pr} is the open-loop dominant pole location of the replica circuit and C_t and C_{tr} are the capacitances across the main and replica-tail transistors, respectively.

Rewriting

$$\text{CMRR}(s) \propto \left(1 + \frac{g_m \cdot r_t}{1 + s \cdot (r_t \cdot C_t)}\right) \cdot \left(\frac{1 + A_{\text{loop}}(s)}{1 + A_{\text{loop}}(s) \cdot \Delta_{\text{rep}}(s)}\right). \tag{13}$$

Case A: Mismatch factor $\Delta = 0$*:* In this case, the replica-tail feedback enhances the CMRR(s) by $1 + A_{\text{loop}}(s)$. In other words, the CMRR of the amplifier is enhanced by the loop gain of the replica circuitry. The overall frequency-dependent part of the CMRR can be represented as

$$\text{CMRR}(s) \propto \left(\frac{s + \omega_{zt}}{s + \omega_{pt}}\right) \cdot \left(\frac{s + \omega_{zr}}{s + \omega_{pr}}\right) \tag{14}$$

where $\omega_{zt} = (1 + g_m \cdot r_t)/(r_t \cdot c_t)$ and $\omega_{pt} = 1/(r_t \cdot c_t)$ are the zero and pole associated with the source degeneration and $\omega_{pr} = (1/R_{or} \cdot C_{or})$ and $\omega_{zr} = \omega_{pr} + \omega_{pr} \cdot A_{\text{loop}}$ are the pole and zero associated with the replica circuitry, respectively. Since the tail transistors are in the linear region, $g_m \cdot r_t$ is comparable to unity; therefore, ω_{pt} and ω_{zt} are very closely spaced and hence represent a pole-zero doublet.

Case B: Mismatch factor $\Delta \gg 1/(A_{\text{loop}})$*:* In this case, it is easy to show that the CMRR enhancement due to the replica circuitry is $1/\Delta_{\text{rep}}$. The frequency response will contain other poles and zeros as well due to the frequency-dependent mismatch between the main and the replica circuitry.

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