CEVGMM: Computationally Efficient Versatile Generic Memristor Model

Mubeen Zafar, Muhammad Naeem Awais, Muhammad Naeem Shehzad, and Abbas Javed

***Abstract*— A memristor is a passive circuit element that has numerous applications ranging from storage to processing. The attributes of memristor, such as low power, fast switching speed, and non-volatility, make it a promising candidate for computing applications. To deploy the memristors at the circuit level, a versatile, computationally efficient, and generic model is required to analyze the circuit performance. This article presents a computationally inexpensive, generic, and accurate phenomenological model of the memristor. The proposed model predicts an accurate current–voltage (I–V) relationship based on the current conduction mechanism. The presented modeling technique can be incorporated into any practical memristor behavior by optimizing the fitting parameters. The model has the capability to optimize its accuracy and computational efficiency by calibrating the model parameters. The results are compared with the characterization data of numerous memristors and noteworthy models of memristors to validate the proposed approach. The results depict that the proposed model is more flexible, computationally efficient, versatile, and generic. It improves the simulation run time up to 24.47% with the relative root mean squared error of 0.4142%. The model exhibits remarkable results when compared with titanium dioxide-based devices. The proposed model can be deployed to various applications, such as logic design, memory design, and neuromorphic computing.**

***Index Terms*— Mathematical modeling, memristor, resistive switching, window function.**

I. Introduction

TWENTIETH CENTURY witnessed extraordinary technological progress, especially in transistors and integrated circuits. Nanoscience, physics, and material sciences have played an essential role in holding Moore's law scaling trend alive [1]. Transistors in CMOS circuits have already approached their minimal possible channel length size, which eventually degrades the performance and reliability. The present analog and digital applications based on CMOS devices are at stake for the concerns mentioned earlier. Therefore, there exists a need for an alternate to CMOS technology to meet the requirements of the electronics industry. The novel memristive device has the potential to use as the fundamental building block for memory and logic gates. Although memristor, as a discrete component, has no leakage current, however, its crossbar architectures and some other modern circuit designs have an ultralow leakage current [2], [3]. Its structure is quite simple as compared with the complex structure of the CMOS transistor.

In 1971, Prof. Leon Chua coined the theoretical concept of two-terminal memristor [4]. The mystery behind the missing memristor is discussed in an S.I, Supplementary Material. The physical realization of the memristor remained unresolved for almost more than 40 years. Hewlett–Packard (HP) serendipitously observed the frequency-dependent pinched hysteresis loop (PHL) in the crossbar nanoscale sandwiched device. The HP researchers gave credit to the seminal work published by Chua in 1971. HP fabricated the first physical memristive device in 2008, in Palo Alto, Santa Clara, CA, USA [5]. It got a lot of unprecedented uproar in industry and research after the ground-breaking discovery of the physical realization of the memristor. After the successful development of the memristor by HP, researchers worldwide used different materials and structures to fabricate a variety of memristors. This surge of progress led to the inevitable development of mathematical models of the memristive devices [6], [7]. Various compact models have been published in the literature. Due to its distinctive current–voltage (I–V) characteristics and infinitesimal dimensions, it has been proclaimed in different applications, i.e., switching element and non-volatile memory [8]–[12]. These applications require an accurate, efficient, close, generic, compact, comprehensive, and less complex mathematical model of the memristor [13]–[19]. Most of the mathematical models of memristors have their inherent strengths and weaknesses. Some of the foreseen limitations in reported models are given in the following.

1) Computational complexity is very high.
2) Sufficient accuracy is not achieved.
3) The models are not generic (i.e., the models fit only to specific practical devices with reasonable accuracy and sufficient complexity).
4) Accurate phenomenological modeling is a big challenge due to the high complexity of the switching mechanism.

This research work proposes a novel memristor model that addresses the limitations reported in the literature. The novel aspects of this research work are as follows.

1) Reduce the computational complexity of the model.
2) Improve the accuracy of the model.
3) Enhance the generality of the model, keeping the accuracy, and complexity in the reasonable range.
4) The model is simple, intuitive, and in closed form.

Manuscript received 17 November 2021; revised 23 April 2022 and 28 June 2022; accepted 24 July 2022. Date of publication 3 August 2022; date of current version 24 October 2022. *(Corresponding author: Muhammad Naeem Awais.)*

The authors are with the Department of Electrical and Computer Engineering, COMSATS University Islamabad, Lahore Campus 54000, Pakistan (e-mail: naeem.awais@cuilahore.edu.pk).

This article has supplementary material provided by the authors and color versions of one or more figures available at https://doi.org/10.1109/TVLSI.2022.3194251.

Digital Object Identifier 10.1109/TVLSI.2022.3194251

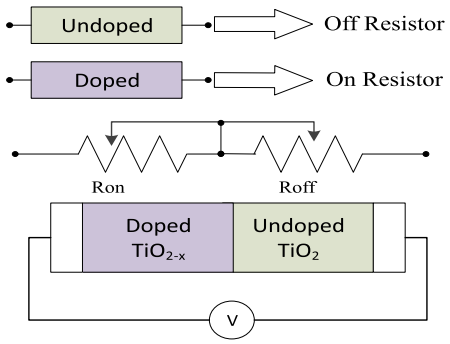

Fig. 1. LDM of memristor based on the variable resistance connected in series. The simplified equivalent circuit of memristor with V, volt source, is given. The doped and the undoped regions indicate the low-resistance $R_{\rm ON}$ and high-resistance $R_{\rm OFF}$ states, respectively [5].

The proposed model has the ability to overcome the demerits of computational inefficiency and inaccuracy in the existing memristor models. The novel model is compared with four versatile practical memristive devices.

The rest of the manuscript is structured as follows. Section II explains the previously reported model of the memristor. In Section III, the novel proposed model of the memristor is inscribed. Section IV comprises the simulation results. Finally, the concluding remarks in Section V sum up this article.

II. Literature Review

An accurate and computationally efficient memristor model is required to analyze, simulate, and design memristor-based circuits and applications. It is desirable and preferable that the memristor model must be intuitive and simple. Following are the different models of memristors reported in the literature.

A. Linear Drift Model

HP elucidated the direct connection between the model and the physical structure of the memristor, which is called a linear drift model (LDM) [5]. The three-layered metal/oxide/metal crossbar array device was fabricated. In these devices, titanium dioxide (TiO_2) acts as the resistive switching (sandwich) layer between the two electrodes. The resistive switching layer further consists of two layers: an oxygen-deficient TiO_{2-x} known as a doped layer and a perfect TiO_2 layer, which is called an undoped layer. TiO_{2-x} considers as the ON-state resistance $R_{\rm ON}$, whereas the perfect TiO_2 considers as the OFF-state resistance $R_{\rm OFF}$. HP demonstrated the working of this device based on the series combination of two resistors: $R_{\rm ON}$ and $R_{\rm OFF}$, as shown in Fig. 1. The current control memristor for circuit analysis is defined in

$$V = R(x)I \tag{1}$$

where V is the applied voltage, I is the current, and R is the general resistance that depends on internal state variable x. The total resistance R_T is given in

$$R_T = R_{\rm ON}(x) + R_{\rm OFF}(1-x). \tag{2}$$

Equation (3) is derived by putting the value of resistance from (2) into (1)

$$V(t) = (R_{\rm ON}(x) + R_{\rm OFF}(1-x))i(t). \tag{3}$$

The boundary drifts between the doped and the undoped regions with an average velocity when the external force is applied as defined in

$$\frac{dx}{dt} = \frac{\mu_v V(t)}{D^2} = \frac{\mu_v R_{\rm ON} i(t)}{D^2} \tag{4}$$

where μ_v is the average dopants mobility, and D is the total thickness of the memristor. The integration of (4) yields the formula for x. x is proportional to the charge q that is passing through the device

$$x = \mu_v \frac{R_{\rm ON}}{D^2} q(t). \tag{5}$$

By applying the positive voltage, oxygen vacancies drift from TiO_{2-x} to TiO_2. Therefore, the width of TiO_{2-x} is increased, and the memristance decreases, due to which current is increased. It switches the device from the OFF state to the ON state. The memristance increases due to which the device switches to the OFF state from the ON state, whenever the negative voltage is applied. Equation (6) is obtained by inserting the value of x from (5) into (3). The value of $R_{\rm ON}$ is much lower than $R_{\rm OFF}$; therefore, $R_{\rm ON}$ could be neglected

$$M(q) = R_{\rm OFF}\left(1 - \mu_v \frac{R_{\rm ON}}{D^2} q(t)\right) \tag{6}$$

where M denotes the memristance of the memristor. Equation (6) determines the memristance of the memristor. The factor $1/D^2$ from (6) indicates that the memristance is critically dependent upon the dimensions of the device. Terminal state and boundary effect problems are the two significant problems associated with LDM.

B. Window Function

Different window functions are proposed in the literature to overcome the boundary limits and nonlinearity problems. The drift velocity of nonlinear dopant can be controlled by introducing a window function $f(x)$ in (4), and that is given in

$$\frac{dx}{dt} = \frac{\mu_v V(t)}{D^2} f(x). \tag{7}$$

1) Strukov's Window Function: The novel window function is presented by Strukov *et al.* [5] for LDM. It resolves the boundary effect problem and shows the partial nonlinear drift close to the boundaries. Strukov's window function is given

$$f(x) = x - x^2. \tag{8}$$

The terminal state problem is not resolved by Strukov's window function. It also lacks the necessary scalability and flexibility.

2) Joglekar's Window Function: A new window function is introduced by Joglekar and Wolf [20]. The control parameter (p) is used to partially control the nonlinearity of the drift velocity. Joglekar's window function is given by

$$f(x) = 1 - (2x - 1)^{2p} \tag{9}$$

where p is a positive exponent parameter. The rate of change in x is also low when the value of p is smaller. As the value of p approaches to infinity, it modifies to LDM.

3) Biolek's Window Function: Biolek *et al.* [21] presented an alternative window function, as defined in (10). The terminal state problem is addressed by Biolek's window function

$$f(x) = 1 - (x - \text{sgn}(-I))^{2p} \Rightarrow \text{stp}(i) = \begin{cases} 1, & i \geq 0 \\ 0, & i < 0. \end{cases} \tag{10}$$

The new function sgn(I) is introduced that resolves the terminal state problem, as given in (10). The positive I increases the doped width, and the negative I decreases the region of doped width due to the sgn(I) function. This window function lacks the necessary scalability and shows the partial nonlinear drift near the boundaries.

4) Prodromakis's Window Function: Prodromakis *et al.* [22] introduced a versatile model with two additional parameters, as given in (11). For scalability and controllability, j and p parameters are used, respectively

$$f(x) = j\left[1 - \left\{(x - 0.5)^2 + 0.75\right\}\right]^{2p}. \tag{11}$$

This window function provides the linkage between linear and nonlinear models. All the window functions depict the nonlinear behavior, but they are not fully capable of imposing nonlinear drift over the entire active core of the device.

C. Nonlinear Ion Drift Model

In the nonlinear ion drift model [23], the switching relationship between current (I) and voltage (V) is based on the experimental results described by

$$I = \omega^n(\beta \sinh(\alpha.V)) + \left(\chi\left[\exp(\gamma.V) - 1\right]\right) \tag{12}$$

where α, β, γ, and χ are the experimental fitting constants. ω is the state variable of the model. The exponent n shows the effect of ω on I. The first expression in (12) dominates, when the memristor is in an ON state, which describes a tunneling mechanism. The second expression in (12) prepotents, when the memristor switches to OFF state. The second part of expression (12) indicates the junction barrier formation. In this model, it is assumed that there is a nonlinear dependency between V and ω. Equation (13) determines the time derivative of ω

$$d\omega/dt = \alpha.f(\omega).g(V) \tag{13}$$

where $f(\omega)$ is a window function, and α is the constant. g is an odd, nonlinear, and monotonically increasing function. This model is not sufficiently accurate.

D. Simmons Tunnel Barrier Memristor Model

All the previous models are based on two variable resistors connected in series. But, the Simmons tunnel barrier model [24] presented a more accurate physical model of the memristor. In this model, the resistance is in series with the electron tunnel barrier, as shown in Fig. S2, Supplementary Material. It assumes asymmetric switching with nonlinear behavior. Equation (14), shown at the bottom of the next page, determines the analytical expression of the state variable x. The switching velocity is dependent on the polarity and current magnitude. Here, c_{OFF}, c_{ON}, i_{ON}, i_{OFF}, and b are the fitting parameters. The magnitude value of x is controlled by the parameters c_{OFF} and c_{ON}. The magnitude of c_{ON} is greater than c_{OFF}, because an ON switching is faster than an OFF switching in the practical devices. Once a current threshold is achieved, the change in x is ignored. a_{ON} and a_{OFF} are the upper and lower limits of x. Thus, the window function is not required. The I–V switching characteristic by the Simmons model is given in

$$v_g = V - i(t)R_s \tag{15}$$

where v_g is the voltage across the tunneling barrier, V is the external voltage applied to the device, and R_s represents the electroformed channel resistance. Although the model is close to the physical memristor, but the computational complexity is very high. This model is not generic in nature.

E. TEAM Model

A threshold adaptive memristor (TEAM) model [25] used the same physical model presented by the Simmons tunnel barrier model [24] but with the simple mathematical expressions. The derivative of x is dependent on the current and x itself, as defined in

$$\frac{dx(t)}{dt} = \begin{cases} k_{\text{OFF}}\left(\dfrac{i(t)}{i_{\text{OFF}}} - 1\right)^{\alpha_{\text{OFF}}} f_{\text{OFF}}(x), & 0 < i_{\text{OFF}} < i \quad \text{(16a)} \\ 0, & i_{\text{ON}} < i < i_{\text{OFF}} \quad \text{(16b)} \\ k_{\text{ON}}\left(\dfrac{i(t)}{i_{\text{ON}}} - 1\right)^{\alpha_{\text{ON}}} f_{\text{ON}}(x), & i < i_{\text{ON}} < 0 \quad \text{(16c)} \end{cases}$$

where k_{OFF}, k_{ON}, α_{ON}, and α_{OFF} are the constants. i_{OFF} and i_{ON} are the current threshold values. The functions $f_{\text{OFF}}(x)$ and $f_{\text{ON}}(x)$ behave as a window function. x is a state variable that represents the effective electric tunnel width. The device can be modeled using the threshold currents, due to the high nonlinear dependency of charge. In this model, the I–V relationship of the memristive device is defined in

$$v_t = \left[R_{\text{ON}} + \frac{R_{\text{OFF}} - R_{\text{ON}}}{x_{\text{OFF}} - x_{\text{ON}}}(x - x_{\text{ON}})\right].i(t) \tag{17}$$

where R_{OFF} and R_{ON} represent the equivalent effective resistance of the device. x_{OFF} and x_{ON} bound the value of x. The TEAM model has a high computational complexity load.

F. System Level Modeling

Some researchers developed the memristor models based on circuit-level applications. There are different models reported

TABLE I
SUMMARY OF PROS AND CONS OF VARIOUS MODELS COME IN DIFFERENT FLAVORS

Model	LDM [5]	Non Linear [23]	Simmon [24]	TEAM [25]
Generic	No	No	No	No
Accuracy	Very low	Low	Moderate	Moderate
Complexity	Moderate	Low	High	Very High

in the literature, which are specific to the applications. An accurate application-based analytical model is developed both for the energy and performance of a one-transistor one-memristor (1T1R) TiO_2-based resistive random access memory (RRAM) cell [26]. The model is based on the write and read operation of the 1T1R RRAM cell. According to this model, the write access time is inversely proportional to the memristance and directly proportional to the square of the device thickness. The memory read access time depends upon the maximum value of memristance, and it is not affected by the device thickness. This model is energy efficient but not versatile in its generic nature.

The partially generic accurate analytical model was developed for TiO_2- and hafnium oxide (HfO_x)-based memristors [27]. This model considers two steps for the read and write operations and nonlinear behavior of TiO_2 and HfO_x devices. In this performance-driven design approach, the optimized results are obtained for the read and write operations of multibit 1T1R resistive RAM [27].

A physical numerical model was proposed based on a universal set/reset characteristic for a bipolar resistive switching memory device [28]. HfO_2-based low power resistive switching RRAM is considered for modeling [28]. The filament growth is considered as a key feature for the modeling of the memristive devices. The universal set/reset characteristics depend on the formation and rupturing of the filament of the bipolar resistive switching memory. The formation and rupturing of filament depend on the compliance current. The pros and cons of reported models are summarized in Table I.

III. PROPOSED MATHEMATICAL MODEL

There are many resistive switching devices having different switching mechanism [29]. Filament and non-filament-based switching mechanisms are most popular among the resistive switching devices. The possibility of formation and rupturing of conductive filament is further classified into two different categories [30], i.e., valence change mechanism (VCM) and electrochemical metallization (ECM). In the VCM [28], the filament is formed by defects, such as oxygen vacancies or electrode metal ions transportation due to joule heating with the external applied potential or reaction between the oxide and the metal, as shown in Fig. 2(a). In the ECM, whenever the device electrodes are forced with a potential source, the electrode particles diffuse into the switching layer and form the metallic bridge, as shown in Fig. 2(b). Consequently, the top electrode makes ohmic contact with the bottom electrode. Both of these phenomena change the state of memristor from an OFF state to an ON state. This transition is known as the setting of the device. As the voltage polarity is reversed, the back-to-back Schottky barriers are formed between the conductive filament, formed either due to (VCM or ECM), and the switching layer, as shown in Fig. 2(c), which changes the device behavior from the ON state to the OFF state. This transition is known as resetting the device. The switching principle of the device is shown in Fig. 2. This is a generic model, which is suitable for any type of memristive devices.

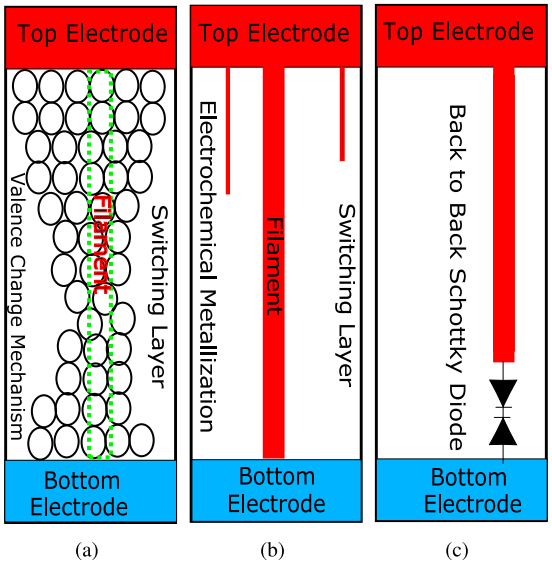

Fig. 2. Proposed physical model of the memristive device. (a) In VCM, the filament formation is due to the vacancies. (b) In ECM, the filament formation is due to the metallization of the electrode. (c) Back-to-back Schottky diodes are formed between the conductive filament and the switching layer due to VCM or ECM.

A. State Variable in the Proposed Model

Memristor is mostly fabricated by sandwiching an oxide layer between two conductive electrodes. Hyperbolic sinusoidal (sinh) function is used in the state variable relationship due to metal–insulator–metal (MIM) junctions in memristive devices. The reported memristor characterization indicates that it is more conductive in a positive region. sinh also increases

$$\frac{dx(t)}{dt} = \begin{cases} c_{\mathrm{OFF}} \sinh\left(\dfrac{i}{i_{\mathrm{OFF}}}\right) \exp\left[-\exp\left(\dfrac{x - a_{\mathrm{OFF}}}{w_{\mathrm{OFF}}}\right) - \dfrac{x}{w_c}\right], & i > 0 \quad (14a) \\ c_{\mathrm{ON}} \sinh\left(\dfrac{i}{i_{\mathrm{ON}}}\right) \exp\left[-\exp\left(\dfrac{x - a_{\mathrm{ON}}}{w_{\mathrm{ON}}}\right) - \dfrac{x}{w_c}\right], & i < 0 \quad (14b) \end{cases}$$

the conductivity of the model. The state variable dynamics are modeled by an exponential function due to the formation of the diode at the oxide and metal interface, since the exponential function is a monotonically increasing function. The motion of the state variable does not remain the same in both directions. Therefore, the combination of the hyperbolic sinusoid and exponential function-based state variable relationship is one of the best options for the memristor modeling. Since the experimental devices have shown a highly nonlinear nature that depend upon the charge, therefore, they can be modeled with threshold voltages. The expression sinh(v(t)) in (18a) describes the tunneling mechanism during the positive cycle of the applied potential. The expression $\exp(v(t))$ of (18b) resembles the ideal diode behavior when the device is forced with the negative potential. The internal state derivative strongly depends upon the voltage and conductivity of the material. Moreover, it also depends on the state variable x itself. The integral segment of the proposed model is based on the derivative of the x. The derivative of x for the proposed model is defined as

$$\frac{dx(t)}{dt} = \begin{cases} (N\sinh(v(t)) + A) f_{\text{ON}}(x), & 0 < V_t < V_{\text{ON}} \quad (18a) \\ (M\exp(v(t)) - B) f_{\text{OFF}}(x), & 0 > V_t > -V_{\text{OFF}} \quad (18b) \end{cases}$$

where N determines the minimum conductivity value of the switching layer, and M determines the maximum conductivity of the switching material. A and B are the experimental fitting parameters. V_{ON} and V_{OFF} are the threshold voltages. $f_{\text{ON}}(x)$ and $f_{\text{OFF}}(x)$ behave as window functions. They depend on the state variable x, and they constrain the value of x within the bounds [0, D], where D is the total length of the device. Different window functions can be used; however, the ideal rectangular window function is used in this article.

B. I–V Relationship in the Proposed Model

Unlike other models, the I–V relationship is based on the physical phenomenon of the passive two-port memristive device. The I–V relationship is not inherently defined in the proposed model. The proposed model correlates the physical structure and I–V relationship of memristor by considering the formation of conductive filament and junction barrier, as shown in Fig. 2. The Schottky diode is considered at the metal–insulator interface. The conductive filament is formed due to the stress of the electric field, whenever the voltage V is applied. The formation and rupturing of conductive filament due to joule heating and ionic diffusion are treated as the ON and OFF states of the device, respectively. The applied voltage across the memristor is calculated by Kirchhoff's voltage law (KVL). The total voltage across the memristor terminals, V_m, is defined in

$$V_m = V_r + V_d \quad (19)$$

where V_r is the voltage across the conductive filament, and V_d is a voltage drop due to potential barrier. As per Ohm's law, the voltage across the filament is given by (20), in which R is the general resistance, and the memristive current is denoted by I

$$V_r = IR. \quad (20)$$

According to diode voltage law, the voltage across the diode is given in

$$V_d = IR_d + V_t \ln\left(1 + \frac{I}{Is}\right) \quad (21)$$

where V_t is Boltzmann's constant, and its value is 25 mV; R_d is the resistance due to potential barrier, and I_s is the reverse saturation current. The voltage drop across R_d is very small, so $I * R_d$ is neglected. Therefore, (21) reduces to

$$V_d = V_t \ln\left(1 + \frac{I}{Is}\right). \quad (22)$$

By applying the logarithm on (22), the resultant equation (23) is obtained

$$V_d = V_t \ln(I) - V_t \ln(Is). \quad (23)$$

There is no reverse saturation current in memristor; therefore, (23) yields

$$V_d = V_t \ln(I). \quad (24)$$

By putting the value of V_t in (24)

$$V_d = 25\ \text{mV} \ln(I). \quad (25)$$

By putting the value of V_r and V_d into (19), the resultant expression (26) is obtained as follows:

$$V_m = IR + 0.25 \ln(I). \quad (26)$$

Equation (26) determines the I–V relationship of the proposed model. V_m is the voltage across the memristor

$$V_m = IR(x) + 0.25 \ln(I)(1 - x). \quad (27)$$

The memristor is in an ON state when the state variable x approaches 1, and OFF when x approaches zero. Equation (27) determines the ON and the OFF states of the memristor.

C. Experimental Setup

This section aims to describe the simulation-based experimental environment. The proposed model is simulated in the MATLAB R2018b software. For the evaluation of the proposed model, the system with the following specification is used.

1) Operating System: Windows 10 (64 bit).
2) Processor: Intel(R) Core(TM) i3-4010u CPU @ 1.70 GHz.
3) RAM: 4 GB.

TABLE II
PERFORMANCE CHARACTERISTICS OF THE PROPOSED MODEL TO EXPERIMENTAL DEVICES

Physical Device			**Types of Memristor**			
	Proposed Model Optimized Parameters	Units	Titanium Dioxide [5]	Polymeric [31]	Hafnium Dioxide [32]	Ferromagnetic [33]
	General Parameters					
1	Von	V	1	5	0.61	3.5
2	Voff	V	-1	-5	0.6	-2
3	Amp		1	3.4	1	3.5
	Device Parameters					
1	R	Ω	190	950	190	900
2	M	1/Ωm	1E-19	1E-14	1E-19	1E-19
3	N	1/Ωm	1E-24	1E-18	1E-24	1E-24
4	D	m	1E-08	1E-08	1E-08	1E-08
	Experimental Fitting Parameters					
1	A		0.1	0.48	0.1	0.095
2	B		0.1	0.24	0.13	0.29
3	Q		0.1	1	0.25	2.5
	Performance Parameters					
1	Root Mean Square Error		0.004142	0.00633	0.005167	0.007906
2	Accuracy		High	Sufficient	Average	Low

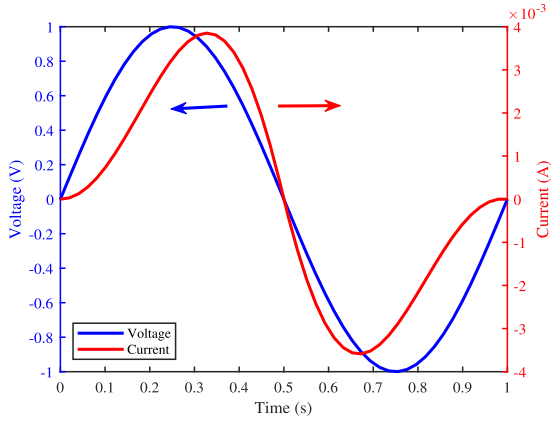

Fig. 3. 1-V sinusoidal waveform with 1 Hz is applied for the I–V characterization of the proposed model for the TiO_2-based memristor.

IV. RESULTS AND DISCUSSION

For the evaluation of the presented model, the model's performance is measured in three different ways. To validate the model I–V behavior, ±1-V sinusoidal is applied at 1 Hz. The result illustrates the symmetric nonlinear bipolar memristive behavior. The value of current varies from −3.6 to 3.6 mA. Fig. 3 shows that v leads i during positive cycle, whereas i leads v in negative cycle. But, both the curves complete the cycle at the same time period. This shows that memristor does not store any charge itself; hence, it is a dissipative electric circuit element.

A. Comparison With Experimental Data

To make a comparison, the plots of I–V behavior are depicted in Fig. 4(a)–(d). The simulated result in Fig. 4(a) presents a better similarity with the experimental data curve, whereas in Fig. 4(b), the proposed model simulation depicts the remarkable similarity with the practical device in the negative region rather than the positive region. When it is analyzed with the HfO_2 device, its behavior presents the symmetric PHL, as shown in Fig. 4(c). The model shows a better similarity with the ferroelectric memristor experimental data curve in the negative region as compared with the positive region, as depicted in Fig. 4(d). The ferroelectric and polymer-based resistive switching devices show asymmetric behavior, whereas HfO_2 and TiO_2 show the symmetric PHL. The results depict that the proposed model has the capability to fit with any bipolar voltage control memristor. Furthermore, the generic model is not supposed to work optimally accurate with all devices, and it may suffer with considerably suboptimal results with fewer devices. The experimental noise also plays its part in reducing the overall accuracy. Therefore, the error at the resistive states and switching points of the experimental device and the presented model is due to the material impurities and experimental setup noise. During the process of memristor modeling, there exists a trade-off between the accuracy of the resistive states and the switching points of the memristor. Moreover, the accuracy of the resistive states is more important as compared with the switching behavior of the device. The digital applications of the memristor utilize one of the resistive states and do not utilize the switching point where abrupt behavior appears.

Different parameter-set values are selected to fit the proposed model to the reference I–V characteristics of a specific memristor. The model parameters are categorized into three distinct categories, as illustrated in Table II. The general

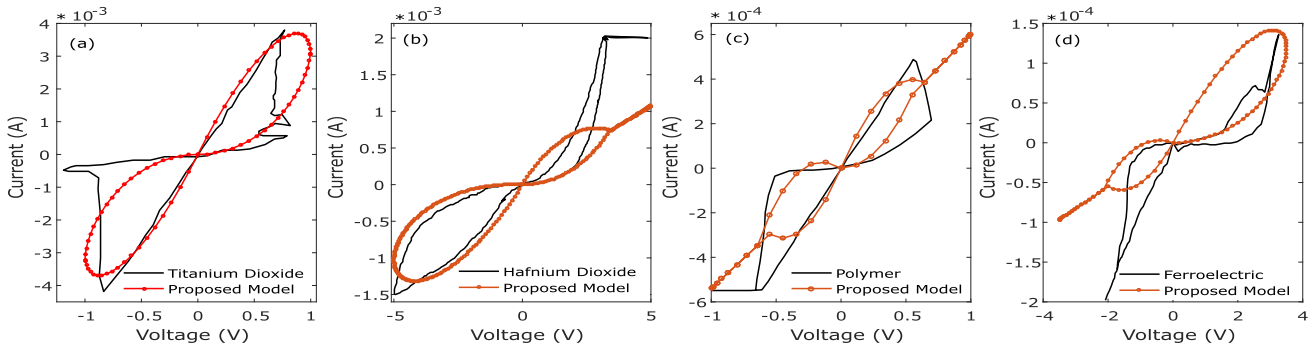

Fig. 4. (a) Comparison of the presented model with the experimental data points of Pt–TiO_2–Pt [7]. (b) Comparison of the presented model with the experimental data points of Ag–F8BT–ITO [31]. (c) Comparison of the presented model with the experimental data points of Ti–HfO_2–TiN [32]. (d) Comparison of the presented model with the experimental data points of ferroelectric memristor [33].

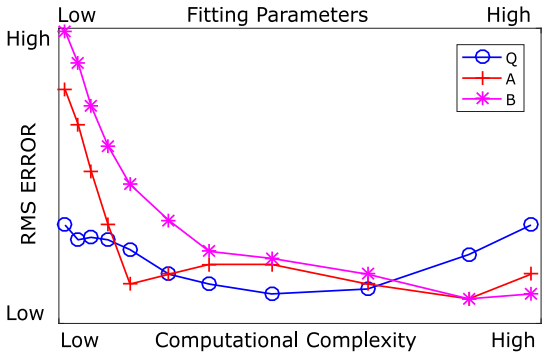

Fig. 5. Model response accuracy versus model complexity.

parameters and device parameters are exactly the same as used by the experimental devices. The experimental fitting parameters values are tunable that are set to match the I–V behavior of the proposed model with the experimental data. The experimental fitting parameters, i.e., A, B, and Q, are manually chosen to reveal I–V characteristics for specific device. These three fitting parameters are associated with accuracy and computational complexity. There is a trade-off between complexity and accuracy, as shown in Fig. 5. It is noteworthy that in the presented model, the relative root mean square (rms) error is decreased at the minimal expense of computational complexity. The relative rms error is high, and the complexity of the proposed model is low whenever the values of A and B are low. The little increase in the values of A and B parameters reduces the error significantly at a minor cost of complexity. After the certain values of A and B, the accuracy of the model does not increase significantly; however, its complexity increases rapidly, whereas the increase in the value of Q increases the accuracy as well as complexity. After a certain threshold of Q, the accuracy decreases, and the complexity increases.

B. Comparison With Other Models

The graphical comparison of the proposed model with different models is given in Fig. 6(a) and (b). As illustrated in Fig. 6(a), the simulated behavior of the LDM [5] does not match the experimental curve. It is also observed that the LDM has a much higher value of current as compared with the experimental curve. Jogelkar's model [5] hysteresis curve shows poor match with the experimental data. Furthermore, in the case of a high resistance state (HRS), the Jogelkar model significantly deviates in both polarities of the applied voltage. Biolek *et al.*'s [21] and Prodromakis *et al.*'s [22] models show partial similarity with the experimental curve. The models in [21] and [22] deviate significantly from a low resistance state (LRS) of the experimental device in both polarities of the applied voltage. Biolek and Prodromakis models partially match in the positive region of the HRS. However, the proposed model significantly matches the LRS in both polarities of the applied potential. The proposed model partially matches the positive region of the HRS. In addition, none of the existing models matches the negative side of the HRS of the experimental device. Our anticipated model adequately matches the negative region of the HRS. As evidenced by the fact, this dominance makes the proposed model superior to the rest of the window function models. The nonlinear model [23] depicts a reasonable matching in the third quadrant; however, as portrayed in Fig. 6(b), the model demonstrates an exponential deviation in the first quadrant. In the Simmon tunnel model [24], hysteresis collapses with the reduction of the phase difference between the voltage and the current. It impacts the accuracy of the model. The hysteresis can be scaled in the Simmon model at the high cost of computational complexity. The TEAM model [25] matches in the LRS and significantly deviates in the HRS during both polarities of the applied voltages. The accuracy of the TEAM model can be increased at the expense of added computational complexity. The presented model deviates from the negative region of the HRS. The suggested model offers the advantages of strong nonlinearity and sufficient accuracy with little computational cost.

Results shown in Tables III and IV are dependent on the setting of the parameters used in the proposed model. Literature reports that the contemporary models diversely increase the simulation run time when accuracy is enhanced, almost doubling the execution overhead each time. The presented model is simple, flexible, more generic, and sufficiently accurate with no compromise on computational run time. The accuracy has been achieved while minimizing the execution time, making

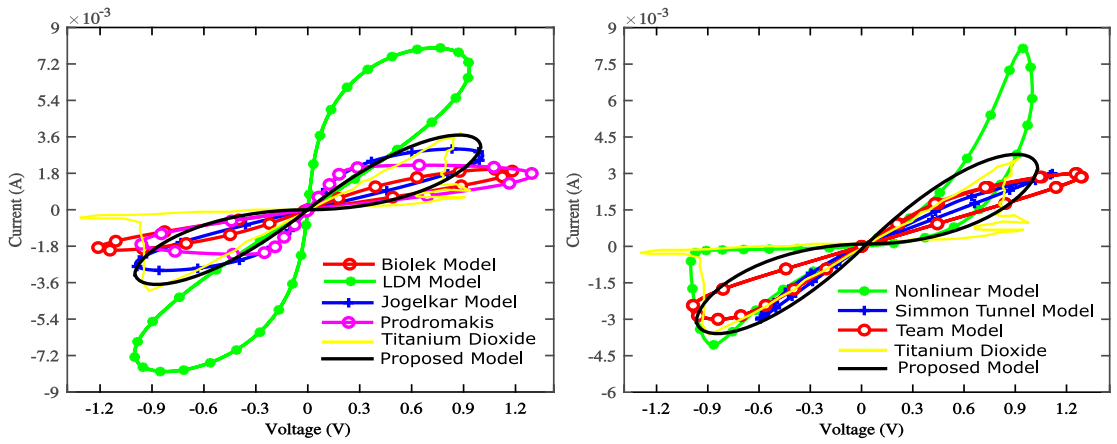

Fig. 6. (a) Comparison of the proposed model with four different window functions of memristor model. (b) Comparison of the proposed model with nonlinear, Simmons tunnel, and TEAM mathematical models of memristor.

TABLE III
COMPARISON WITH DIFFERENT WINDOW FUNCTION MODELS OF MEMRISTOR

Window Function	Biolek [21]	Joglekar [20]	Prodromakis [22]	Strukov [5]	Proposed
Linkage to LDM	Yes	Yes	Yes	No	Yes
Non-linear	Partially	Limited	Partially	No	Yes
Boundary Effect	No	Yes	Yes	Yes	Yes
Scalability	No	No	Yes	No	Yes
Flexibility	Yes	Yes	Yes	No	Yes
Terminal State	Yes	No	No	No	Yes
Error	0.0236	0.0245	0.0221	0.0253	0.004142
V_{on}/V_{off}	1.1/-1.2	1/-1	1.3/-1	1/-1	1/-1
LRS Accuracy	Partially	Limited	Partially	No	Yes
HRS Accuracy	Limited	No	Limited	No	Partially
Switching Point	Limited	Limited	Limited	No	No

TABLE IV
COMPARISON WITH DIFFERENT MATHEMATICAL MODELS OF MEMRISTOR

Models	LDM [5]	Nonlinear [23]	Simmon [24]	TEAM [25]	Proposed
Mechanism	Current	Voltage	Current	Current	Voltage
Threshold	No	No	No	Yes	Yes
Generic	No	No	No	No	Yes
Simulation Time (s)	1.4092	1.1256	1.3504	1.5186	1.147
CPU Time (s)	1.6375	1.31564	1.9094	2.36876	1.2594
Error	0.0253	0.0236	0.0095	0.0128	0.004142
V_{on}/V_{off}	1/-1	1/-0.9	1.1/-0.7	1.3/-1	1/-1
LRS Accuracy	No	No	Limited	Partially	Yes
HRS Accuracy	No	No	Partially	Partially	Partially
Switching Point	No	Limited	Limited	Limited	No

the model distinctive and outperforming the other models. The code is executed five times for each setting, and an average is calculated to obtain the unbiased running time of the developed model. The comparison of the accuracy and the computational run time among the different models is tabularized in Table IV. The proposed model improved the simulation run time up to 24.47%, and it is sufficiently accurate, with a relative rms of 0.4142%.

C. Universal Logic Gates

The proposed model is suitable for digital design applications. The universal logic gates are developed by using a memristor ratio logic (MRL) family [28] to validate the proposed memristor model. The schematics of the NOR and the NAND logic gates are shown in Fig. 7(a) and (b), respectively. Two memristors are connected in series with opposite polarity to build the OR and AND logic gates. The common node of the memristor terminals is used for output, whereas the input signals are provided to the other terminals. The memristance of the memristor is decreased when the current flows from the positive terminal to the negative terminal. Its memristance increases when the flow of current is in the opposite direction. For the cases where both inputs have the same logical value, then no current will flow. Hence, the same input logic will appear at the output. For the cases when one input is logical zero, the other is a logical one. Then, current will flow from higher potential to lower potential. The NAND or NOR gates are built by connecting a CMOS inverter at the end of AND or OR gates, respectively. The simulation results of the universal gates are given in Fig. 7. Two inputs are provided to the circuit,

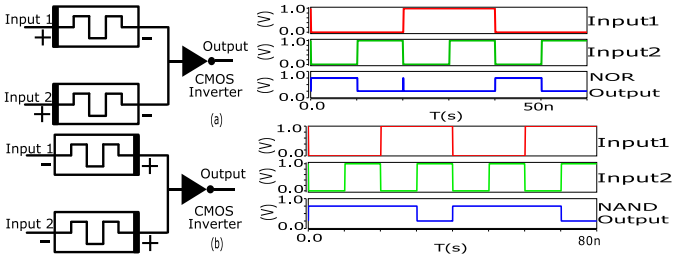

Fig. 7. (a) Simulation result of NOR logic gate using the proposed model of memristor. (b) Simulation result of NAND logic gate using the proposed model of memristor.

where 1 V is considered as logical 1, and 0 V is considered as logical 0, as shown in Fig. 7. The output of the NOR logic gate is logical 0 if any of the inputs are at logical 1, as shown in Fig. 7(a). The output of the NAND logic gate is logical 1 when any of the inputs are at logical 0, as shown in Fig. 7(b). The detailed code is given in S.II, Supplementary Material.

V. Conclusion

The presented model is a generic that can be tailored to different I–V characteristics of the fabricated devices. It can match any practical device more accurately than the published models in the literature. The results describe that the memristor model can reproduce many physical memristor's I–V curves with high accuracy at the minimum simulation run time. The proposed mathematical model of the memristor suggests that the memristive devices exhibit electron tunneling, nonlinearity, and voltage threshold characteristics. The I–V relationship is sorted out based on the formation and rupturing of the conductive filament phenomenon. In addition, the model proposed the threshold voltages to characterize the setting and resetting of the device. Finally, the presented model is validated with the hitherto published key devices and models. The proposed model improved the simulation run time up to 24.47%, and it is sufficiently accurate, with a relative rms of 0.4142%. The model exhibits the finest results when compared with TiO_2-based devices. This model is suitable for digital circuit applications based on memristive devices.

References

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 1965.
[2] X. Ji, S. Hao, K. Y. Pang, K. G. Lim, and R. Zhao, "A vacuum gap selector with ultra-low leakage for large-scale neuromorphic network," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 505–508, Mar. 2020.
[3] Y. Li and K.-W. Ang, "Hardware implementation of neuromorphic computing using large-scale memristor crossbar arrays," *Adv. Intell. Syst.*, vol. 3, no. 1, 2021, Art. no. 2000137.
[4] L. O. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.
[5] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
[6] J. Singh and B. Raj, "Comparative analysis of memristor models and memories design," *J. Semicond.*, vol. 39, no. 7, Jul. 2018, Art. no. 074006.
[7] V. Keshmiri, "A study of the memristor models and applications," Ph.D. dissertation, Dept. Elect. Eng., Linköping Univ., Linköping, Sweden, 2014.
[8] M. J. Rozenberg, I. H. Inoue, and M. J. Sánchez, "Nonvolatile memory with multilevel switching: A basic model," *Phys. Rev. Lett.*, vol. 92, no. 17, Apr. 2004, Art. no. 178302.
[9] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, no. 7290, pp. 873–876, 2010.
[10] L. Eeckhout, "Memristors and more," *IEEE Micro*, vol. 38, no. 5, p. 4, Sep. 2018.
[11] A. Ascoli, R. Tetzlaff, L. O. Chua, J. P. Strachan, and R. S. Williams, "History erase effect in a non-volatile memristor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 3, pp. 389–400, Mar. 2016.
[12] J. Yu, X. Mu, X. Xi, and S. Wang, "A memristor model with piecewise window function," *Radioengineering*, vol. 22, no. 4, pp. 969–974, 2013.
[13] F. García-Redondo, M. López-Vallejo, and P. Ituero, "Building memristor applications: From device model to circuit design," *IEEE Trans. Nanotechnol.*, vol. 13, no. 6, pp. 1154–1162, Nov. 2014.
[14] G. Ligang, F. Alibart, and D. B. Strukov, "Programmable CMOS/memristor threshold logic," *IEEE Trans. Nanotechnol.*, vol. 12, no. 2, pp. 115–119, Mar. 2013.
[15] M. Khalid and J. Singh, "Memristor based unbalanced ternary logic gates," *Anal. Integr. Circuits Signal Process.*, vol. 87, no. 3, pp. 399–406, Jun. 2016.
[16] K.-H. Kim *et al.*, "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications," *Nano Lett.*, vol. 12, no. 1, pp. 389–395, 2011.
[17] Y. Zhou, Y. Li, L. Xu, S. Zhong, R. Xu, and X. Miao, "A hybrid memristor-CMOS XOR gate for nonvolatile logic computation," *Phys. Status Solidi (A)*, vol. 213, no. 4, pp. 1050–1054, Apr. 2016.
[18] F. García-Redondo, R. P. Gowers, A. Crespo-Yepes, M. López-Vallejo, and L. Jiang, "SPICE compact modeling of bipolar/unipolar memristor switching governed by electrical thresholds," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 8, pp. 1255–1264, Aug. 2016.
[19] T. D. Dongale *et al.*, "Effect of write voltage and frequency on the reliability aspects of memristor-based RRAM," *Int. Nano Lett.*, vol. 7, no. 3, pp. 209–216, 2017.
[20] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: Properties of basic electrical circuits," *Eur. J. Phys.*, vol. 30, no. 4, p. 661, 2009.
[21] Z. Biolek, D. Biolek, and V. Biolkova, "SPICE model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, Jun. 2009.
[22] T. Prodromakis, B. P. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with nonlinear dopant kinetics," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3099–3105, Sep. 2011.
[23] E. Lehtonen and M. Laiho, "CNN using memristors for neighborhood connections," in *Proc. 12th Int. Workshop Cellular Nanosc. Netw. Appl. (CNNA)*, Feb. 2010, pp. 1–4.
[24] M. D. Pickett *et al.*, "Switching dynamics in titanium dioxide memristive devices," *J. Appl. Phys.*, vol. 106, no. 7, Oct. 2009, Art. no. 074508.
[25] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold adaptive memristor model," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 211–221, Nov. 2012.
[26] M. Zangeneh and A. Joshi, "Performance and energy models for memristor-based 1T1R RRAM cell," in *Proc. Great Lakes Symp. VLSI*, 2012, pp. 9–14.
[27] M. Zangeneh and A. Joshi, "Design and optimization of nonvolatile multibit 1T1R resistive RAM," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 8, pp. 1815–1828, Aug. 2014.
[28] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field-and temperature-driven filament growth," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4309–4317, Dec. 2011.
[29] B. Hajri, H. Aziza, M. M. Mansour, and A. Chehab, "RRAM device models: A comparative analysis with experimental validation," *IEEE Access*, vol. 7, pp. 168963–168980, 2019.
[30] C. Wang, H. Wu, B. Gao, T. Zhang, Y. Yang, and H. Qian, "Conduction mechanisms, dynamics and stability in ReRAMs," *Microelectron. Eng.*, vols. 187–188, pp. 121–133, Feb. 2018.
[31] M. N. Awais, M. Mustafa, M. N. Shehzad, U. Farooq, M. T. Hamayun, and K. H. Choi, "Resistive-switching and current-conduction mechanisms in F8BT polymer resistive switch," *Micro Nano Lett.*, vol. 11, no. 11, pp. 712–714, 2016.
[32] Y.-E. Syu *et al.*, "Atomic-level quantized reaction of HfO_x memristor," *Appl. Phys. Lett.*, vol. 102, no. 17, Apr. 2013, Art. no. 172903.
[33] A. Chanthbouala *et al.*, "A ferroelectric memristor," *Nature Mater.*, vol. 11, no. 10, pp. 860–864, Sep. 2012.