SB3 - Datalogger
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Abstract

A compact, high speed logic analyser is designed with onboard buffering for the simultaneous analysis and logging of up to eight digital channels, plus an optional clock line for analysis of synchronous transfers. The supporting desktop application is also developed to configure and control the analyser, as well as to retrieve and post-process the recorded data and display it in a convenient format.

1 Hardware Overview

A PIC18F4550 microcontroller on a breakout board provides the core of the datalogging hardware, clocked at 48MHz. The USB peripheral external hardware already exists on the board, along with hardware to bring the device out of reset into either the bootloader or user code.

Additional hardware will be put in place to provide the following functionality:

- Monitor and log up to eight digital channels plus a clock.
- Store up to 1Mbit of data (that is to say, 128k samples if using all eight channels).
- Retrieve the samples from memory and transmit them to the desktop computer via USB interface for post processing, analysis and charting.

1.1 Filtering

Frontend antialiasing filters will be put in place to avoid frequency domain aliasing caused by signals at the input above the Nyquist frequency, which will be defined by the sampling frequency of the device. Simple first order low pass RC filters will suffice for this, with a $-3dB$ frequency placed just above the Nyquist frequency.

1.2 Buffering

The datalogger will dump data to an SRAM buffer during the logging process, since the PIC does not have enough internal RAM to store a suitable number of samples to satisfy the specification. SRAM, whilst relatively expensive, also demonstrates extremely fast write speeds which is essential to keeping the sampling rate high.

The hardware of choice is the AS6C1008 1Mbit SRAM IC from Alliance Memory, which is divided into eight blocks. A 17-bit wide parallel interface is used for byte-addressing, and a byte-wide parallel interface is provided for data.

The address lines will be directly attached to the PIC using the two byte-wide ports PORTB and PORTD, plus one additional line from another port. After the hardware anti-aliasing filters, the eight input channels are connected directly to the SRAM data interface via a 8-gate tri-state buffer, controlled by the PIC. This buffer is enabled during the data acquisition phase, and subsequently disabled to detach the input channels from the memory.

1.3 Data Retrieval

Retrieving data from the SRAM is achieved via the use of a parallel-in/serial-out shift register such as the 74HC165 series. The byte-wide parallel input to this device is attached to the SRAM data interface, and data is clocked out to the PIC before being packetised and transmitted to the desktop computer via the USB interface.

A diagram of how to set up the apparatus is shown in figure 1.

Appendices

A Appendix 1

Figure 1: Apparatus setup