ASAP 7 DRC Violation Waiver Checklist for PDN Voltage Droop Experiments using Cadence Voltus

Violation Category	Specific DRC Violations	Rules	Operating Margin	Description	Design Functionality and Structural Integrity		Impact on Vdroop Evaluation	
					Assessment	Justification	Assessment	Justification
Minimum Enclosure of Vias by metal lines	V1.M1.EN.1	(5,2) nm	(3,2) nm	Minimum Enclosure of Vias by metal lines on two opposite sides	No Impact	This DRC error is related to via placement and the allowed margins for its meta line enclosure. Slight slight offset in vias along the metal line during P&R does not alter design functionality or alter the structural integrity of the netlist after P&R.	No Impact	The requirement for minimum enclosure on both the sides of the via by a metal line does not impact the via's or the metal line's resistance. In our case, the via placement is offset on side by 2 nm but is completely enclosed by the metal line. This will not alter the resistance of the connection, thereby having no impact of IR drop analysis.
	V1.M2.EN.2	(5,5) or (5,0) nm	(3,0)	Minimum Enclosure of Vias by metal lines on two opposite sides	No Impact		No Impact	
	V2.M3.AUX.2	Same width of metal line	16% Not overlapping	Via must exactly be the same width as metal line along the direction perpendicular to the M2 length.	No Impact		No Impact	
	V0.M1.AUX.3	Same width of metal line	18% Not overlapping	Via must exactly be the same width as metal line along the direction perpendicular to the M2 length.	No Impact		No Impact	
Spacing between metal lines	M1.S.2	25nm	21nm	Minimum spacing between two metal lines. 1st Metal line is <=36nm and the second metal line is >36nm	No Impact	Metal spacing requirements are enforced by the tool to ensure proper metal separation is maintained to prevent metal shorts during fabrication. Waiving these violations has no impact on structural integrity of netlist after P&R.	No Impact	Metal spacing requirements do not have any significant impact on voltage droop calculation or IR drop analysis run by Cadence Voltus.
	M1.S.6	20nm	18nm	Minimum corner to corner spacing between two metal line polygons.	No Impact		No Impact	
Via Spacing Requirements	V1.S1	18nm or 27nm	21nm	Minimum spacing between two vias if they are perfectly aligned or partially aligned	No Impact	Via spacing requiremnts are also guidelines for minimizing defects during fabrication. They have no impact on netlist integrity	No Impact	Voltage droop impact due to via spacing is insignificant. IR drop calculations done by Cadence Voltus remain unaffected.
	V1.S2	23nm	21nm	Minimum corner to corner spacing between two vias	No Impact		No Impact	
Gate Poly Proximity	GATE.S.3	54nm	NA	Every GATE (not cut by GCUT and not interacting with the layer SRAMDRC) must have at least one other GATE within 54 nm of its surrounding along the horizontal axis. The spacing being the distance between centers of the two GATE layer polygons.	No Impact	This violation is related to gates not being uniformly spaced for poly deposition. This does not alter the netlist or interconnection integrity	No Impact	Voltage droop and IR drop analysis remain unimpacted due to this violation because every gate's poly is connected to the metal lines for IR analysis.