

JONTI TALUKDAR

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• Research: <https://jontitalukdar.github.io/research>

EDUCATION

Pratt School of Engineering, Duke University Master of Science, Electrical & Computer Engineering, (<i>Track: Computer Engineering</i>)	2018 -2020
Institute of Technology, Nirma University Bachelor of Technology, (<i>Electronics and Communication Engineering</i>) GPA: 8.7	2014 -2018

RESEARCH INTERESTS

- Computer Architecture and Machine Learning, with focus on using AI/ML techniques to facilitate Processor Performance optimization, circuit testing, and architecture design etc.
- Designing emerging energy-efficient microarchitectures which focus on accelerating compute performance for applications in datacenters, deep learning, big-data analytics, computer vision, cloud computing etc.

TECHNICAL SKILLS

Programming Languages: Verilog HDL, C, C++, Python, TCL, Bash.

Operating Systems: UNIX, Linux, Embedded Linux.

Tools and Frameworks: OpenCV, Caffe, TensorFlow, Make, RISC-V GNU toolchain.

Software: Synopsys Spyglass, Mentor Graphics Questa, Xilinx ISE, Keil μ Vision, NI Multisim, Simulink.

EXPERIENCE

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| SoC Front End & Architecture Intern, NXP Semiconductors | Jan 2018 – Jul 2018 |
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- Hands on experience in automated flow based techniques for rapid **RTL integration** and glue logic insertion including clocking, reset and power connectivity for 16FFC based automotive SoCs.
 - Owned and incorporated **IO Virtualization** feature in the latest cut of automotive platform SoCs. Implemented and Integrated the IPs (RTL level) responsible for SoC pad protection through virtualized core access (ARM R52 cores) as per ISO26262 & ASIL D safety requirements.
 - Handled CDC/RDC/Lint Sign-offs at top level hierarchy for automotive radar based SoC.
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| Research Intern, HPC Lab, IIT Gandhinagar | Apr 2017 - Jul 2017 |
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- Joined the High Performance Computing Facility at IIT Gandhinagar under Dr. Ravi Hegde, in the capacity of a research intern, working on Deep Learning solutions for Computer Vision problems.
 - Gained hands on experience working with state of the art deep learning architectures like SSD, Faster-RCNN etc. (through Caffe & TensorFlow implementations) for training on GPUs like the Nvidia TitanX and Nvidia GTX 1070.

ACADEMIC PROJECTS

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| Design and Development of a Two-lane Serializer | Jan 2018-Feb 2018 |
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- Designed a two lane serializer sub-system with input data lanes operating at 400MHz and serialized output at 1 GHz.
 - Round robin strategy utilized for arbitration between lanes.
 - Sub blocks coded and integrated in Verilog HDL followed by linting using Spyglass.
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| Transfer Learning for Object Detection using Deep CNNs | Apr 2017 – Jul 2017 |
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- Trained Deep Convolutional Neural Networks on synthetic images for the task of object detection.
 - Developed strategies for artificially rendering synthetic datasets using 3D object models from ShapeNet.

- Trained state of the art deep CNN architectures like faster RCNN, SSD, R-FCN, GoogLeNet, DetectNet, etc. using Caffe and TensorFlow frameworks and increased overall mAP by more than 35% through hyperparameter optimization.

Real-time Human Action Recognition System

Apr 2016 - Feb 2017

- Developed a novel approach for recognizing human actions like ‘clapping’, ‘boxing’, ‘running’, etc. using good features.
- Training and testing was done on the KTH action recognition dataset using MLP based neural network.
- Implemented and tested the system on embedded Linux platforms including Odroid XU4, Raspberry Pi 3.

RISC V ISA Simulator

Jan 2017-Apr 2017

- Compiled the RISC V software toolchain for simulation of on Linux kernel.
- Implemented the RISC V instruction set simulator ‘Spike’ for functional simulation of memory and register operations.
- Used RISC V cross compiler for compilation of basic C programs in assembly language.

Design of 8-bit dual port SRAM

Jun 2017-Sep 2017

- Designed and implemented 8-bit dual port SRAM in Verilog HDL.
- Deployed the code on Altera Cyclone II FPGA.

Smart Spectrum Sensing for Cognitive Radio

Nov 2016 – Feb 2017

- Developed a Signal to Noise Ratio (SNR) based adaptive threshold algorithm for energy detection and spectrum sensing in GNU Radio.
- Used it to monitor primary user activity in radio environment using USRP B200 and reallocated bandwidth to secondary users, enhancing channel utilization.

EXTRA CURRICULARS

Center Head, Fellowship Program, Make a Difference

Apr 2015 - May 2016

- Joined the Ahmedabad city Core Team as part of fellowship program under Make a Difference.
- Played an active role in the Leadership X Design (**LxD**) **Programme**, increasing student attendance, pass ratio and reducing child stress in shelter homes.

Ed Support Volunteer, Make a Difference

Aug 2014 - Apr 2015

- Took up ownership to teach Science and Math to secondary school students at a shelter home in Gandhinagar.
- Provided after-school support through teaching assistance and mentorship of the kids at the shelter.

ACHIEVEMENTS

- Summer Research Fellow, 2017, High Performance Computing Lab, IIT Gandhinagar
- Received funding grant from IdeaLab R&D Incubator for the year 2016-17.
- Fellow, Leadership X Design Programme 2015-16, Make a Difference.
- University Finalist, TI Analog Design Challenge 2015.
- Finalist, Space Habitat Design Challenge, 2011.

PUBLICATIONS

- **J. Talukdar**, B. Mehta, S. Gajjar, “Computational Intelligence in Embedded Systems Design: A Review”, *3rd International Conference on Information and Communication Technology for Intelligent Systems (Springer SIST)*, Mar. 2018
- P. Rajpura, A. Aggarwal, M. Goyal, S. Gupta, **J. Talukdar**, R. Hegde, H. Bojinov, ‘Transfer Learning by Finetuning Pretrained CNNs Entirely with Synthetic Images’, *6th National Conference on Computer Vision, Pattern Recognition, Image Processing and Graphics (Springer CCIS)*, Dec. 2017
- **J. Talukdar**, B. Mehta, ‘Human Action Recognition using Good Features and Multilayer Perceptron Network’, *6th IEEE International Conference on Communication and Signal Processing (ICCSP)*, April. 2017. (presented) (**arxiv-preprint**, arxiv:1708.06794)
- B. Mehta, **J. Talukdar**, S. Gajjar, ‘High Speed SRT Divider for Intelligent Embedded System’, *2nd Int. Conf. on Soft Computing (IcSoftComp)*, Dec. 2017.