JONTI TALUKDAR

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EDUCATION

Duke University, Durham, NC — **Expected- Dec 2019**
Master of Science, Electrical & Computer Engineering, *(Track: Computer Engineering)*

Institute of Technology, Nirma University, Ahmedabad, India — **2014 -2018**
Bachelor of Technology, *(Electronics and Communication Engineering)*

TECHNICAL SKILLS

Programming Languages: Verilog, System Verilog, UVM, C, C++, Python, Perl, TCL, Bash, MATLAB.

EDA Skills: Cadence Virtuoso, Mentor Tessent, Mentor Questa Sim, Mentor Questa CDC, Mentor Fastscan, Synopsys TetraMax, Synopsys Spyglass, Synopsys HSPICE

Software Frameworks: Make, Git, IBM Doors, Enovia DesignSync, OpenCV, Caffe, TensorFlow.

Courses: Digital Integrated Circuits, VLSI Testing, Hardware Verification, Adv. Computer Arch. , Algorithms

EXPERIENCE

Logic Technology Development (Q&R) Intern, Intel Corporation, Hillsboro, OR — **May 2019 – Current**
- Developed analytical models for propagation of single event transients (SETs) in combinational logic paths through SPICE based pre-characterization of Intel's 3D Standard Cell Library (10nm technology).
- Developed an automated framework to estimate chip level soft error rates (SER) based on circuit topology by performing path sensitization and applying the analytical models to large scale systems through chip level netlists.
- Validating analytical simulation framework to establish runtime improvements compared to SPICE based methods.

SoC Front End & Architecture Intern, NXP Semiconductors, India — **Jan 2018 – Jul 2018**
- Worked on SoC RTL integration including clocking, reset, power connectivity of 16FFC based automotive SoCs.
- Implemented SoC pad protection through virtualized core access (ARM R52 cores) as per ISO26262 standards.
- Performed CDC, Reset De-assertion and Lint Sign-offs at top level hierarchy for automotive radar based SoC.
- Responsible for detailed documentation of integrated IPs, tool analysis and methodology reports.

Research Intern, HPC Lab, Indian Institute of Technology, Gandhinagar — **Apr 2017 - Jul 2017**
- Worked on Deep Learning solutions for Computer Vision problems specific to object detection and classification.
- Used data augmentation techniques to improve robustness and quality of synthetic datasets.
- Trained deep learning architectures like SSD, Faster-RCNN etc. on GPUs like the Nvidia TitanX and GTX 1070.

ACADEMIC PROJECTS

Functional Verification of 32-bit ALU Sub-System — **Feb 2019 – Apr 2019**
- Architected a coverage driven verification environment for a 32-bit ALU of an out of order processor core in UVM.
- Designed all sub-blocks, including drivers, scoreboards, monitors, sequences, tests, coverage monitors etc. from scratch.
- Implemented an assertion based verification environment with binds to check DUT internals (Gray Box Approach).

Design of SRAM Cell Read/Write Circuitry in 180nm Technology — **Mar 2019 - Apr 2019**
- Designed the read/write circuit for a 256*256 SRAM Array and validated design characteristics using HSPICE.
- Designed the Differential Voltage Sensing Amplifier, Write Driver Circuitry, Saturated Enhancement Load based Pull-up Circuitry for the SRAM array.

Hierarchical Scan Insertion and Pattern Retargeting — **Feb 2019 – Apr 2019**
- Partitioned different RTL benchmarks into hierarchical sub-blocks for scan insertion and pattern retargeting.
- Designed test wrappers for partitioned cores as per IEEE 1500 test standard.
- Developing a methodology (tool flow) to invoke tools, perform hierarchical ATPG and evaluate fault coverage.

Performance evaluation of Z-Cache in SimpleScalar — **Oct 2018 - Dec 2018**
- Implemented a Z-Cache with 2-level and 3-level lookup configurations in SimpleScalar.
- Analyzed performance metrics of Z-Cache with baseline 2-way and 4-way set associative cache configurations.

Design and Development of a Two-lane Serializer — **Jan 2018-Feb 2018**
- Designed a two lane serializer sub-system with input data lanes operating at 512MHz and serialized output at 1 GHz.
- Round robin based arbiter designed for both lanes, designed and integrated in Verilog HDL followed by linting and CDC analysis through Synopsys Spyglass toolset.