PolarFire SoC FPGA DSP FIR Filter Demo Application Note

AN5165

Introduction (Ask a Question)

PolarFire® SoC FPGA devices integrate a fifth-generation flash-based FPGA fabric architecture that includes embedded Math blocks optimized specifically for Digital Signal Processing (DSP) applications such as Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters, and Fast Fourier Transform (FFT) functions.

This document describes the DSP FIR filter demo design and how to run the demo on a PolarFire SoC Discovery Kit. The DSP FIR filter demo is implemented using Libero® SoC. The demo design consists of:

- A 127 tap FIR filter with re-loadable coefficients.
- A 256 point FFT on filter output to view spectrum.
- An UART interface to the host PC to load the filter coefficients and input signals (low-pass, high-pass, band-pass, and band-stop frequencies).
- A Host PC GUI application to generate and interface with the demo design running on the PolarFire SoC FPGA device. The GUI also plots the input/output waveforms and the required spectrum.

Table of Contents

1. Demo Requirements (Ask a Question)

The following table lists the hardware and software requirements for the demo.

Table 1-1. Design Requirements

Requirements	Version
Operating System	Windows® 10
Hardware	
PolarFire® SoC Discovery Kit (MPFS-DISCO-KIT with FPGA: MPFS095T-1FCSG325E)	REV 2
Software	
FlashPro® Express	Available with Libero® SoC installation package.
Libero SoC	**Note:** Refer to the `readme.txt` file provided in the design files for the software versions used with this design.
GUI	The GUI is only supported on Windows 10.

Before you start:

1. Download the demo design files from www.microchip.com/en-us/application-notes/an5165. The design files folder contains the following sub-folders:
   - Programming_Job: Contains the programming `.job` file. The demo design is programmed using the `.job` file, see Programming the Device Using FlashPro Express.
   - GUI_Installer: Contains the GUI installation package required to run the demo design.
   - TCL_Scripts: Contains the Tcl scripts for creating the demo design. For more information on creating the demo design using Tcl, see Appendix 1: Running the Tcl Script.
2. Download and install Libero SoC on the host PC. To evaluate the designs using the PolarFire SoC Discovery Kit, use the free Libero SoC Silver license.

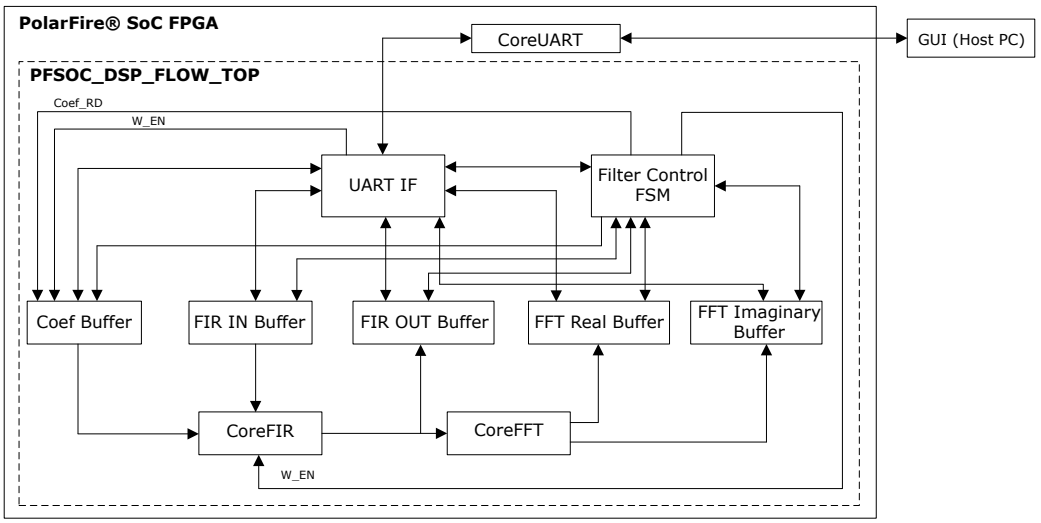
2. Demo Design Description (Ask a Question)

The DSP FIR Filter design is developed to showcase the Math block capabilities of PolarFire SoC for implementing filtering applications.

In the design, the host interface and the FIR filter are implemented in the fabric for low-pass, high-pass, band-pass, and band-stop filtering operations. The testbench provided for this demo uses pre-generated filter coefficients and input signals (low-pass, high-pass, band-pass, and band-stop frequencies) and passes the values to the demo design. The CoreFIR_PF IP suppresses unwanted frequency components, and the CoreFFT IP generates the output spectrum to verify the filtering operation.

The following figure shows the top-level block diagram of the DSP FIR filter design.

Figure 2-1. Block Diagram



The following steps describe the data flow in the design:

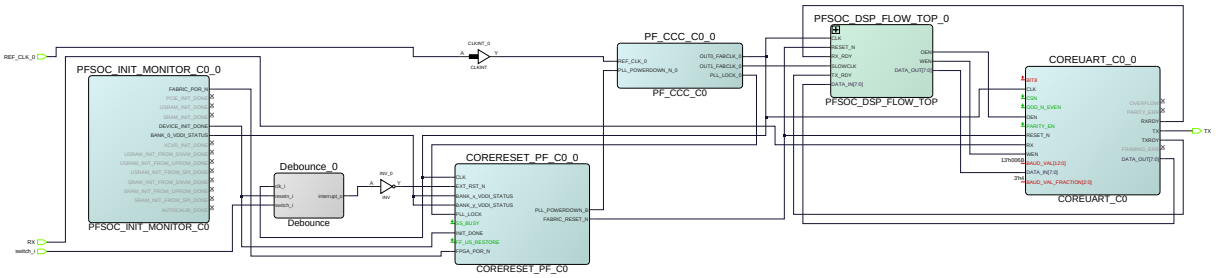
1. Upon UART handshaking (sending and receiving the known patterns over the UART bus to pre-verify the serial channel before actual usage), the GUI application running on the host PC sends the filter coefficients followed by filter input data.
2. UART IF block creates 16-bit packets and stores the data in the corresponding input data buffers (FFT Imaginary Buffer, FFT Real Buffer, FIR IN buffer, and FIR OUT Buffer) and coefficient buffers (Coef Buffer).
3. Filter Control FSM controls the following operations:
   - Reading the data from buffers
   - Writing the data into CoreFIR IP
4. Once the CoreFIR generates the output response, the data is stored in the FIR OUT buffer.
5. The CoreFIR output is sent to CoreFFT. After receiving, the CoreFFT generates the frequency spectrum of the filtered data and generates the real and imaginary output data. The CoreFFT-generated real and imaginary outputs are stored in FFT Real and FFT Imaginary buffers.
6. UART IF block reads the data from FIR and FFT output buffers and sends the data to GUI through UART. The GUI plots the received data.

2.1 Design Implementation (Ask a Question)

This section shows the DSP Filter design implemented using the CoreFIR and CoreFFT IP cores in Libero SoC.

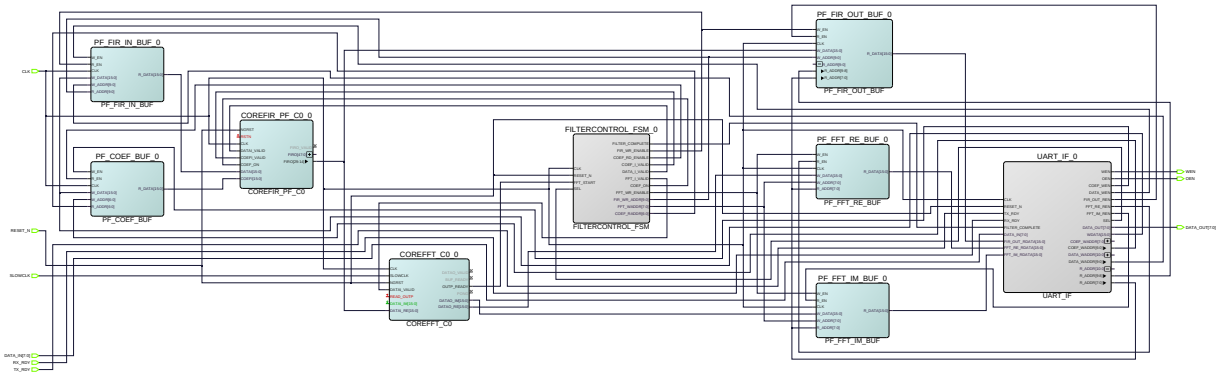
The following figure shows the top-level SmartDesign, which includes the clocking (PF_CCC_C0_0), Reset (CORERESET_PF_C0_0), the SmartDesign of DSP Flow (PFSOC_DSP_FLOW_TOP), and COREUART_C0_0.

Figure 2-2. Top-level SmartDesign



The following figure shows the PFSOC_DSP_FLOW_TOP SmartDesign, which includes FIR filter (COREFIR_PF_C0_0), FFT filter (COREFFT_PF_C0_0), buffers, control FSM and UART_IF blocks.

Figure 2-3. DSP FIR Filter SmartDesign



For more information on creating the demo design using Tcl, see Appendix 1: Running the Tcl Script.

Important: There is a known issue with the CoreFIR IP due to which the FIR output valid signal (FIRO_VALID) is not used; instead, an initial latency of 128 cycles is used as a workaround. This will be fixed in the next release.
This reference design and the associated GUI are created to support only the given CoreFIR and CoreFFT IP configurations.

2.2 IP Blocks Used in the Design (Ask a Question)

The following table lists the IP blocks used in the FIR filter design.

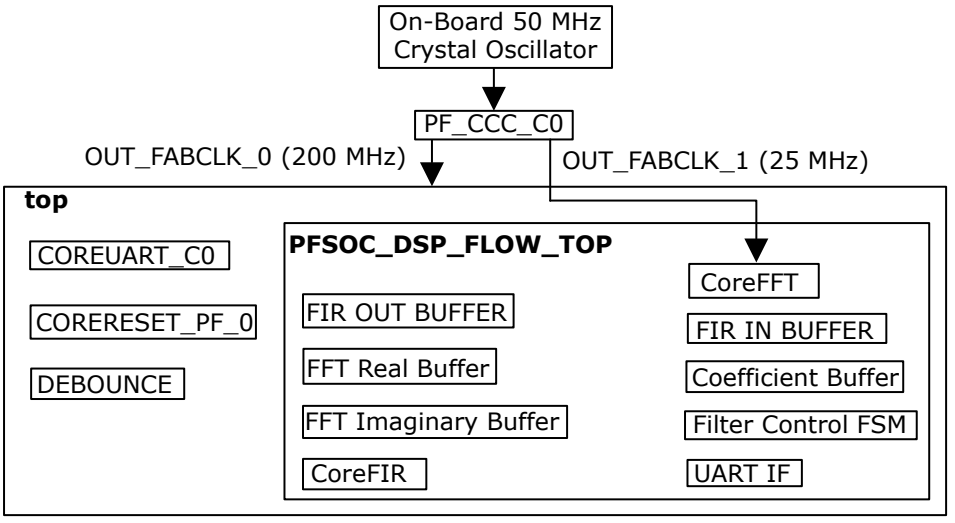
Table 2-1. IP Blocks

IP Block	Description
COREFIR_PF_C0	The COREFIR_PF_C0 IP is used in re-loadable coefficient mode to support low-pass, high-pass, band-pass, and band-stop filters.
COREFFT_C0	The COREFFT_C0 IP generates the frequency spectrum of the filtered data.
FILTERCONTROL_FSM_0	The filter control FSM block handles the data flow and controls signals of the FIR filter and FFT. It loads the filtered data with respect to the corresponding output buffer and moves the FFT output data to the corresponding FFT real and imaginary buffers.
UART_IF	The UART_IF block consists of a finite state machine for handling control operations between UART and the fabric logic. Control operations include the following: • Loading of filter coefficients. • Filtering input data with respect to the corresponding input data buffers and coefficient buffers. • Sending and receiving data from UART.
PF_TPSRAM	Five instances of PF_TPSRAM blocks are used in the design to store coefficients, FIR input data, FIR output data, FFT real, and FFT imaginary output data.
PF_CCC_C0	The PF_CCC_C0 IP is configured to take a 50 MHz reference clock as an input and generates 25 MHz and 200 MHz output clocks.

2.3 Clocking Structure (Ask a Question)

The following figure shows the clocking structure of the demo design.

Figure 2-4. Clocking Structur



As shown in the preceding figure, the on-board 50 MHz crystal oscillator provides a reference clock to the PF_CCC_C0 block. PF_CCC_C0 generates the following clocks:

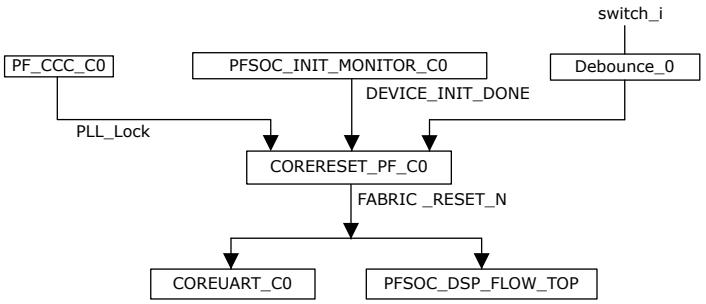
- 200 MHz clock that drives all the blocks of top_0 and PFSOC_DSP_FLOW_TOP
- 25 MHz slow clock is a secondary clock needed by the CoreFFT block which is within the PFSOC_DSP_FLOW_TOP

2.4 Reset Structure (Ask a Question)

The DEVICE_INIT_DONE, PLL Lock, and switch_i signals initiate the reset signal (FABRIC_RESET_N) from the CORERESET_PF_C0 block, which is synchronized with the OUT_FABCLK_0. The switch_i signal is connected to SW1 on the kit and this acts as external reset input to the design.

The following figure shows the reset structure of the demo design.

Figure 2-5. Reset Structure

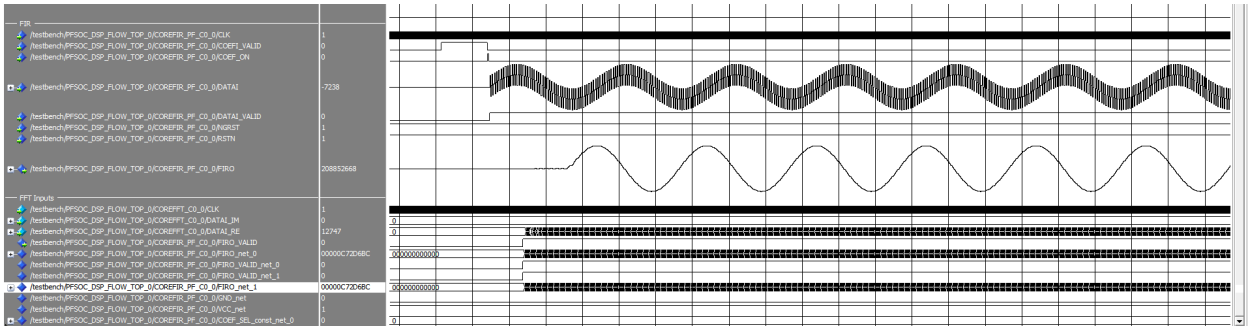


2.5 Simulating the Design (Ask a Question)

A testbench (`top.v`) is provided to simulate the design. The testbench simulates the filter pattern and waveform selection. It contains the test selection for the coefficient inputs (low-pass, high-pass, band-pass, and band-stop) and data input. It also monitors the UART_IF module status signals, output signals (DATAOUT), and FFT output status signals (DATA Valid and output ready) for the verification of filter output.

The following figure shows the simulation waveform.

Figure 2-6. CoreFIR Input and Output Signals



Important: To get this waveform, perform the following steps:

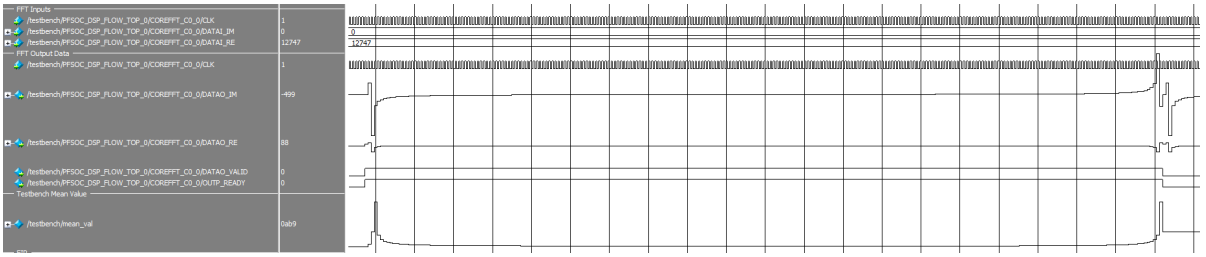
1. Change the radix of the input to decimal, right-click **DATAI**, go to the **radix** option, and select **decimal**.
2. Right-click **DATAI**, select the format option and select **Analog (automatic)**.

In the preceding figure:

- **COEFFI** represents Input coefficients
- **DATAI** represents FIR input data
- **FIRO** represents FIR output data

The following figure contains the Low-Pass Filter Output waveform, which is highlighted in the following figure.

Figure 2-7. Low-Pass Filter Output



In the preceding figure:

- DATAO_IM represents the imaginary part of the FFT output
- DATAO_RE represents the real part of the FFT output

3. Board Setup (Ask a Question)

The board setup involves the following steps:

3.1 Powering Up the Board (Ask a Question)

Before powering up the board, ensure that the jumper settings are the same as listed in the following table.

Table 3-1. Jumper Settings

Jumper	Setting	Description
J45	1 and 2 closed	To set Bank 1 and Bank 5 voltages (VDDI1_5) to 3.3V for Rpi GPIO and mikroBus operation
J46	1 and 2 closed	To set the VDDAUX1 voltage to 3.3V
J47	1 and 2 closed	To receive power from the USB Type-C port (J4) for the board
J49	2 and 3 closed	To set the 7 Segment display voltage to 5V

To power up the board, connect the Cable C Male to C Male cable from the USB Type-C port (J4) on the Discovery Kit to the Type C compatible (5V, 3A) port on the Host PC. The power status LEDs 5P0V, VDD, and 1P8V glow indicating that the board is powered-up.

3.2 Programming the Device Using FlashPro Express (Ask a Question)

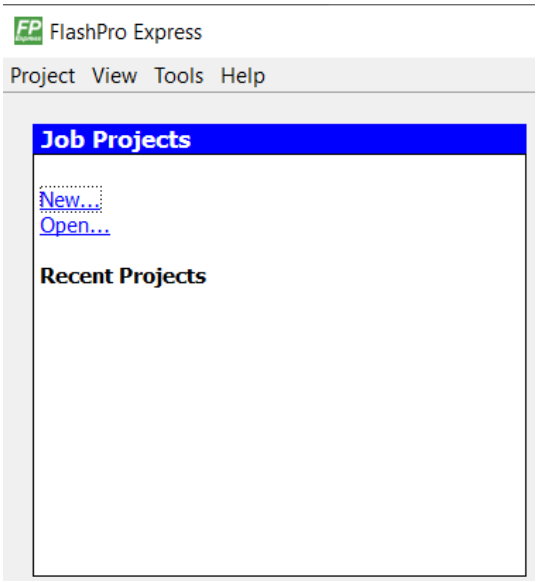
This section describes the steps to program the PolarFire SoC device with the programming job file. The `.job` file is available at the following location in the provided design files:

`mpfs_an5165_v2024p1_df/Programming_Job`

To program a PolarFire SoC device using FlashPro Express, perform the following steps:

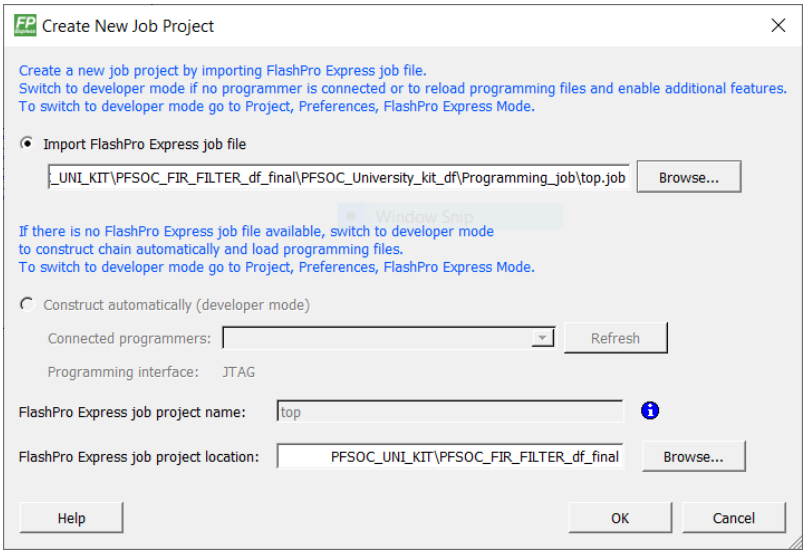
1. Ensure that all the steps described in Board Setup are completed.
2. On the host PC, launch the FlashPro Express software from the **Windows Start** menu.
3. Create a new job project by clicking **New**, as shown in the following figure.

Figure 3-1. FlashPro Express Job Project



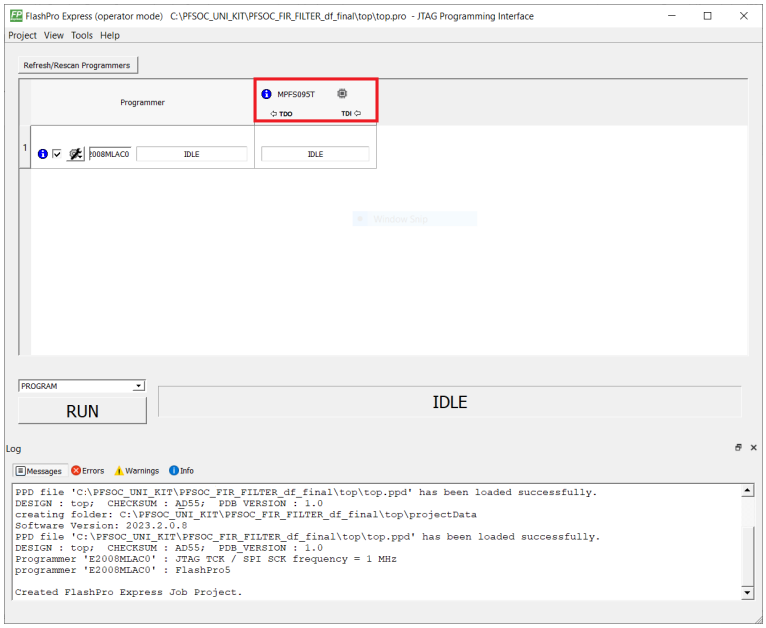
4. Enter the following in the **Create New Job Project** dialog box:
   - In the **Import FlashPro Express job file**: Click **Browse**, navigate to the location where the `.job` file is located, and select the file.
   - In the **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.

Figure 3-2. Creating New Job Project



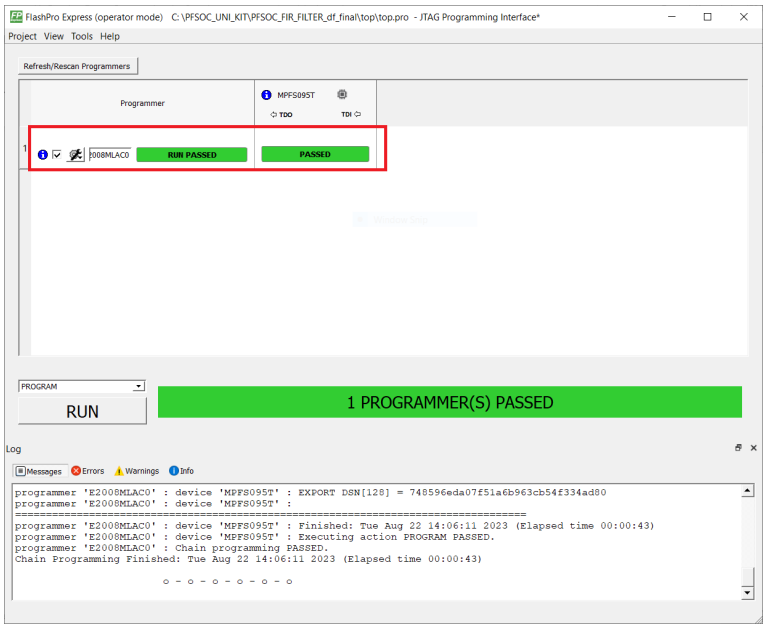
5. Click **OK**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears.
6. Verify that a programmer number appears in the **Programmer** box. If it does not show, verify the board connections, and click **Refresh/Rescan Programmers**.

Figure 3-3. Refresh/Rescan Programmers



7. Click **RUN** to program the device. When the device is programmed successfully, a `RUN PASSED` status is displayed as shown in the following figure.

Figure 3-4. FlashPro Express-RUN PASSED



4. Running the Demo (Ask a Question)

Before you start, ensure that all the steps described in Board Setup are completed. Once the device is programmed, perform the following steps to run the demo:

1. Installing and Starting the GUI
2. Generating the Filter Coefficients and Input Signal
3. Generating the Filter Output

4.1 Installing and Starting the GUI (Ask a Question)

To install and start the GUI, perform the following steps:

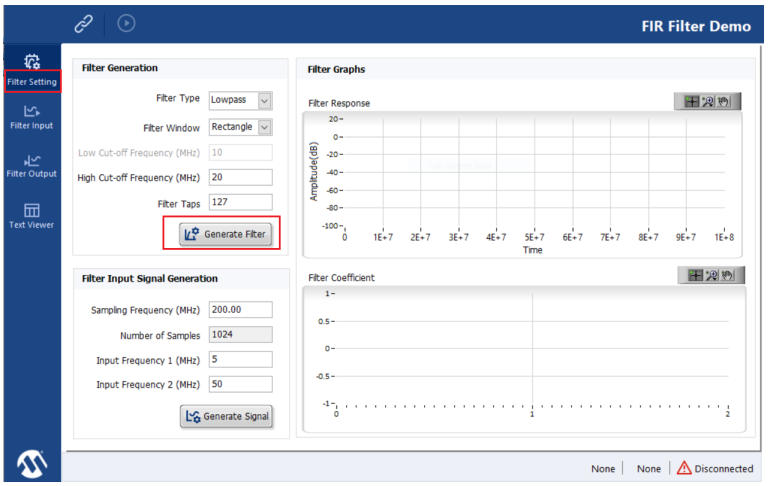
1. Double-click the **DSP FIR Demo GUI** application (`setup.exe`) from the following location in the provided design files:
   `mpfs_an5165_v2024p1_df/GUI_Installer/Volume`
2. Follow the installation wizard to install the GUI application.

4.2 Generating the Filter Coefficients and Input Signal (Ask a Question)

Follow these steps:

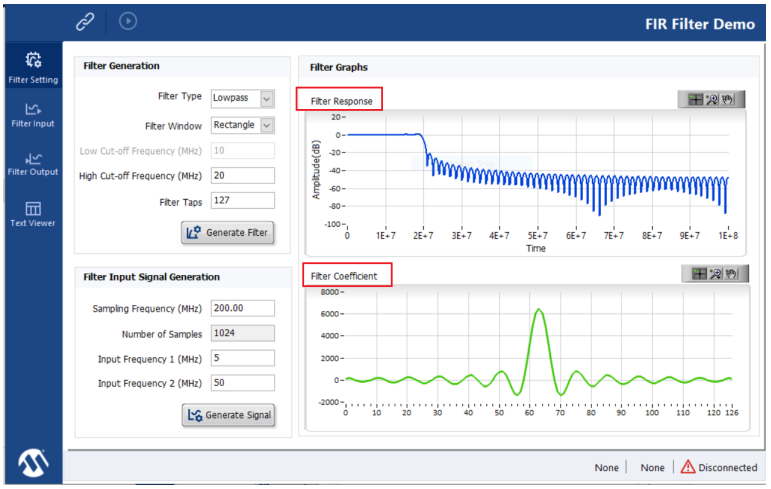
1. Launch the GUI and go to **Filter Settings** to generate the filter coefficients.
2. Retain the default **Filter Generation** parameters and select **Generate Filter** as shown in the following figure.

Figure 4-1. Filter Generation Parameters



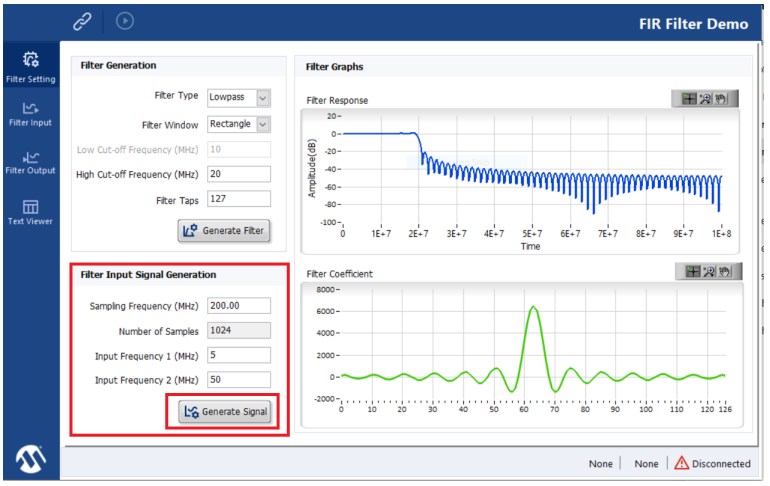
3. After generating the filter coefficients, the **Filter Response** and the **Filter Coefficient** plots are displayed as shown in the following figure.

Figure 4-2. Filter Response and Filter Coefficient



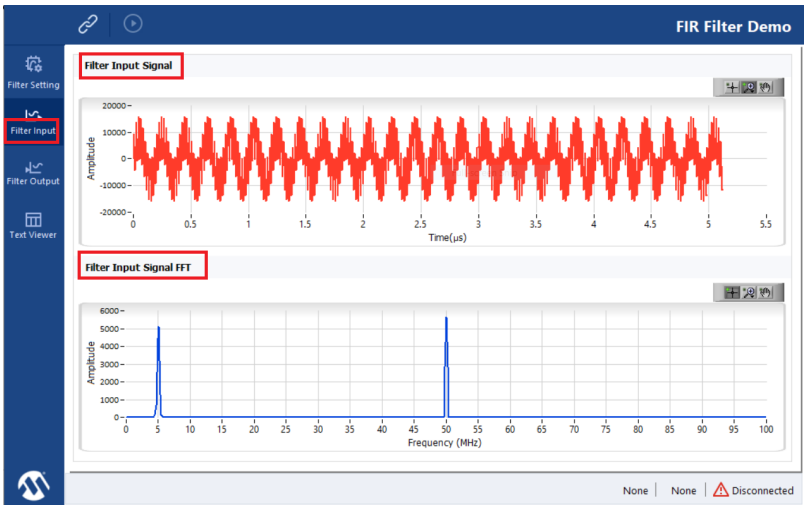
4. To generate the input signals, retain the default parameters in the GUI and click **Generate Signal** as shown in the following figure.

Figure 4-3. Generate Signal



5. The input signals and the frequency spectrum of the specified signals are displayed in the **Filter Input** tab, as shown in the following figure.

Figure 4-4. Filter Input Tab

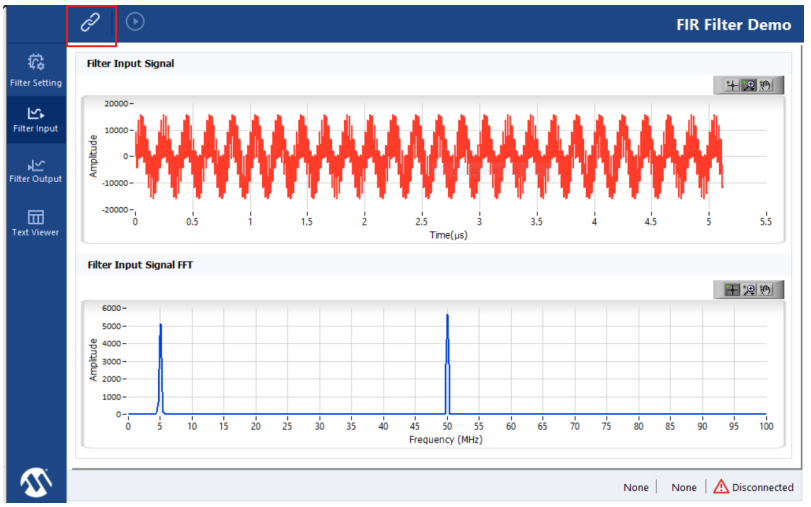


4.3 Generating the Filter Output (Ask a Question)

To generate the filter output, complete the following steps:

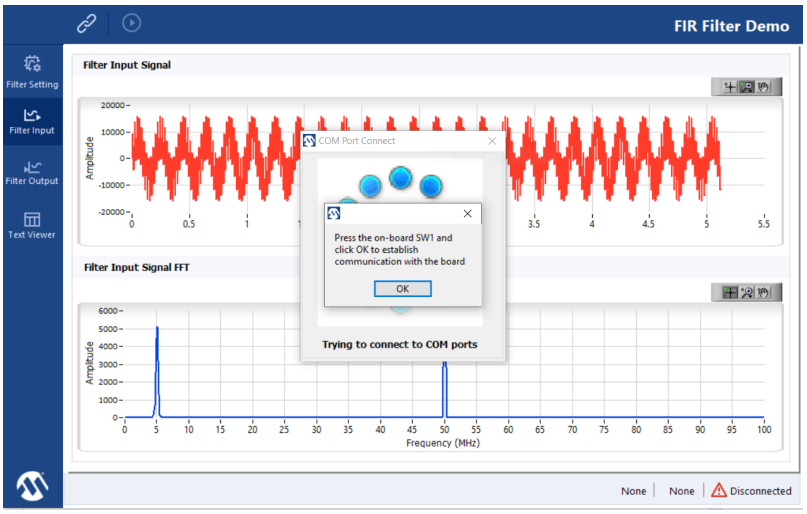
1. To configure the input frequencies and coefficients, click the icon to connect as shown in the following figure.

Figure 4-5. Connect



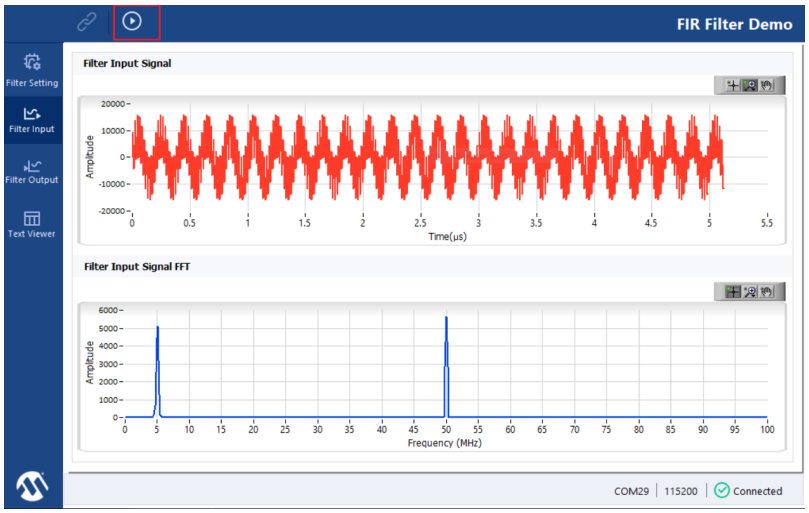
2. After clicking the icon , the GUI prompts you to press the **SW1** on the board and to click **OK** as shown in the following figure.

Figure 4-6. Establish Communication



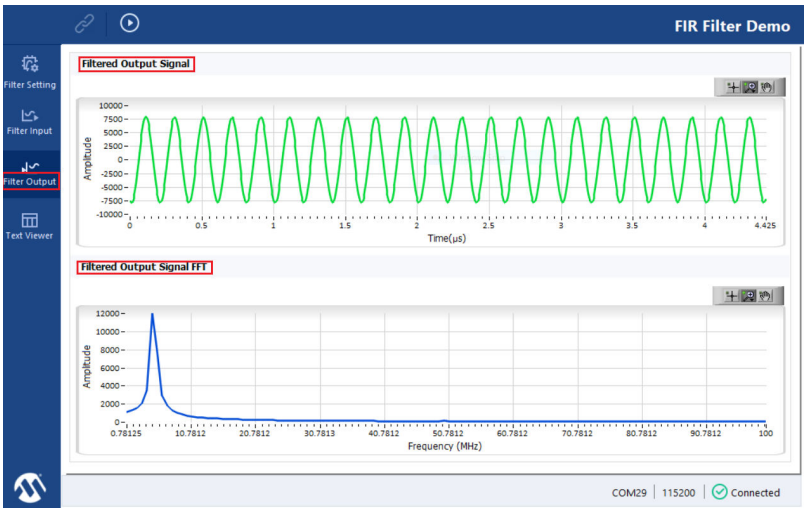
3. After clicking **OK**, click the icon to start as shown in the following figure.

Figure 4-7. Start



4. After clicking the icon, the filter operation completes. The GUI displays the `Operation Completed` message and plots the filtered data and the FFT data on the **Filter Output** tab as shown in the following figure. As the low-pass filter option was selected, the high-frequency component is suppressed while the low-frequency signal is preserved. This is observable in the frequency spectrum of the output signal.

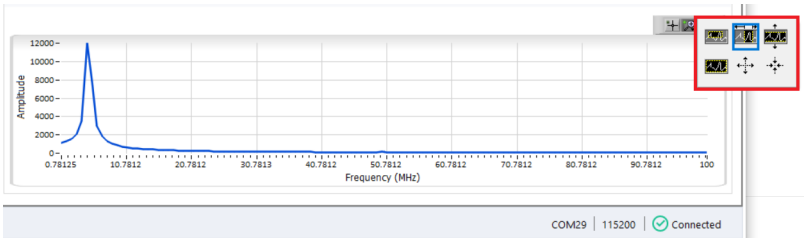
Figure 4-8. Filter Output Tab



Important: The accuracy of frequencies represented in the frequency plot depends on the frequency resolution used (sampling rate and FFT length).

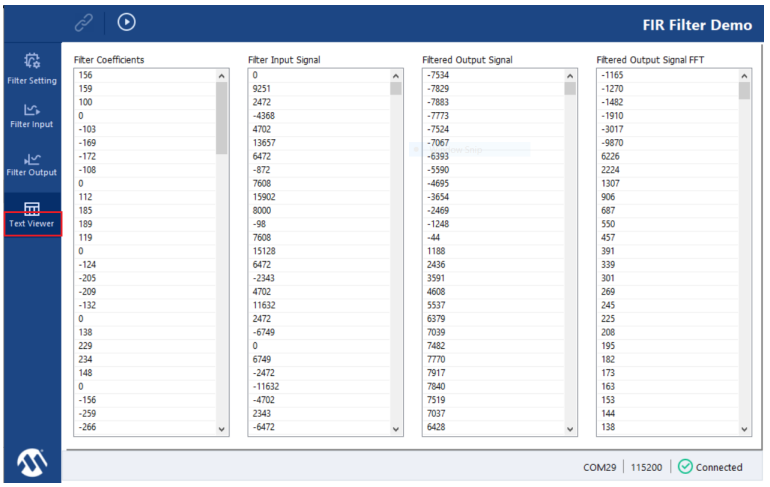
5. Zoom-in or zoom-out the waveform using the options shown in the following figure.

Figure 4-9. Zooming the Filter Output



6. The **Text Viewer** displays the filter coefficients, input signal, output signal, and FFT output data values, as shown in the following figure.

Figure 4-10. Text Viewer



7. Close the GUI.

This concludes DSP FIR Filter demo.

5. Appendix 1: Running the Tcl Script (Ask a Question)

Tcl scripts are provided in the folders of design files under the directory `TCL_Scripts`. If necessary, the design flow can be reproduced from Design Implementation (which includes Synthesis, Place and Route, and Verify Timing) till the generation of the job file.

To run the Tcl, follow these steps:

1. Launch Libero SoC.
2. Select **Project** > **Execute Script**
3. Click **Browse** and select `script.tcl` from the downloaded `TCL_Scripts` directory.
4. Click **Run**.

After successful execution of the Tcl script, a Libero project is created within the `TCL_Scripts` directory.

Important: This is a known issue. When designs are executed on longer paths, they may fail. To prevent this, run the `.tcl` script (`script.tcl`) from shorter paths. It is recommended to download and save the TCL files closer to the root directory (for example, near the C drive) to ensure a shorter path.

For more information about Tcl scripts, see the `readme.txt` at `mpfs_an5165_v2024p1_df/TCL_Scripts`.

For more details on Tcl commands, see the Tcl Commands Reference Guide. Contact the Technical Support team for any queries encountered while running the Tcl script.

6. Appendix 2: References (Ask a Question)

This section lists documents that provide more information about the DSP filters and IP cores used in the design.

- For more information about PF_TPSRAM, see the PolarFire Family Fabric User Guide.
- For more information about PF_CCC, see the PolarFire Family Clocking Resources User Guide.
- For more information about CoreFIR, see the CoreFIR page.
- For more information about CoreFFT, see the CoreFFT page.
- For more information about CoreUART, see the CoreUART page.
- For more information about Libero, ModelSim, and Synplify Pro, see the Libero SoC Documentation.

7. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
C	10/2024	The following is the list of changes made in Revision C of the document: • Added a Note regarding the TCL script in the Appendix 1: Running the Tcl Script section
B	04/2024	The following is the list of changes made in Revision B of the document: • Updated the document for Libero v2024.1. • Updated the PolarFire SoC Discovery Kit (MPFS-DISCO-KIT) version from Rev 1 to Rev 2 in Table 1-1. • Added a new GUI section in Table 1-1. • Added a note about a known issue in section Design Implementation. • Added the `top.v` testbench file name in section Simulating the Design. • Removed the note “Output data is valid when FIRO_VALID is high.” in section Simulating the Design. • Updated the folder name from v2023p2 to **v2024p1** in section Programming the Device Using FlashPro Express. • Updated the folder name from v2023p2 to **v2024p1** in section Installing and Starting the GUI. • Updated the folder name from v2023p2 to **v2024p1** in Appendix 1: Running the Tcl Script.
A	12/2023	Initial release.

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