RT PolarFire 1G Ethernet Loopback Application Note

AN4509

Introduction (Ask a Question)

Microchip's RT PolarFire® FPGAs support 1G (1000BASE-T) Ethernet solutions for various networking applications. In RT PolarFire devices, 10/100/1000 Mbps (1G) Ethernet is implemented using the CoreTSE Media Access Control (MAC) soft IP core. The CoreTSE IP provides 10/100/1000 Mbps Ethernet MAC with a Gigabit Media Independent Interface (GMII), that is used to interface with an Ethernet PHY through the RGMII_TO_GMII bridge IP. 1G Ethernet solutions can be implemented using the CoreTSE or CoreTSE_AHB MAC IP. The IP must be initialized and configured using a soft processor.

For GMII/RGMII-based designs, GPIOs or HSIOs connect an Ethernet MAC to an external Ethernet PHY. For RGMII-based designs, the PF_RGMII_TO_GMII IP converts GMII signals (MAC side) to RGMII signals (PHY side). CoreTSE is configured in GMII mode and connected to PF_RGMII_TO_GMII. The PF_RGMII_TO_GMII IP is connected to an external PHY.

This document describes how to run the 1G Ethernet loopback demo design. The reference design is created to demonstrate 1G Ethernet loopback using GPIO on a RT PolarFire Evaluation Board. The demo design is built using the PF_RGMII_TO_GMII, CoreTSE, and Mi-V soft processor IP cores. The reference design is for a single RGMII lane (single RJ45 cable).

The demo design can be programmed using either of the following options:

- Using a pre-generated `.job` file: To program the device using the `.job` file provided along with design files, see 7. Appendix 1: Programming the Device Using FlashPro Express.
- Using Libero® SoC: To program the device using Libero SoC, see 5. Libero Design Flow.

Note: A license is required to use the CoreTSE IP core. To request a license, contact Microchip Support.

Table of Contents

1. Design Requirements (Ask a Question)

The following table lists the hardware and software requirements for running the demo.

Table 1-1. Design Requirements

Hardware	Description
RT PolarFire® Evaluation Kit (RTPF500TS -1CG1509M) • RT PolarFire Evaluation Board • 12V/5A AC power adapter and cord • External FlashPro4 Programmer • RJ45 cable to connect the board with the host PC	Rev 1.0
Host PC	Windows® 10
Software	
Cat Karat (Ethernet packet generator) To install the appropriate version, see the packetbuilder.net/.	v1.51.200
FlashPro Express	See the `readme.txt` file provided in the design files for the software versions used for building this reference design.
Libero® SoC Design Suite	

Note: Libero SmartDesign and configuration screen shots provided in this document are for illustration purposes only. Open the Libero design to see the latest updates.

2. Prerequisites (Ask a Question)

Before you begin:

1. Download the design files using the following link:
   www.microchip.com/en-us/application-notes/AN4509
2. Download and install Libero SoC on the host PC from the following web page:
   www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions#Download%20Software
3. Download and install Cat Karat.

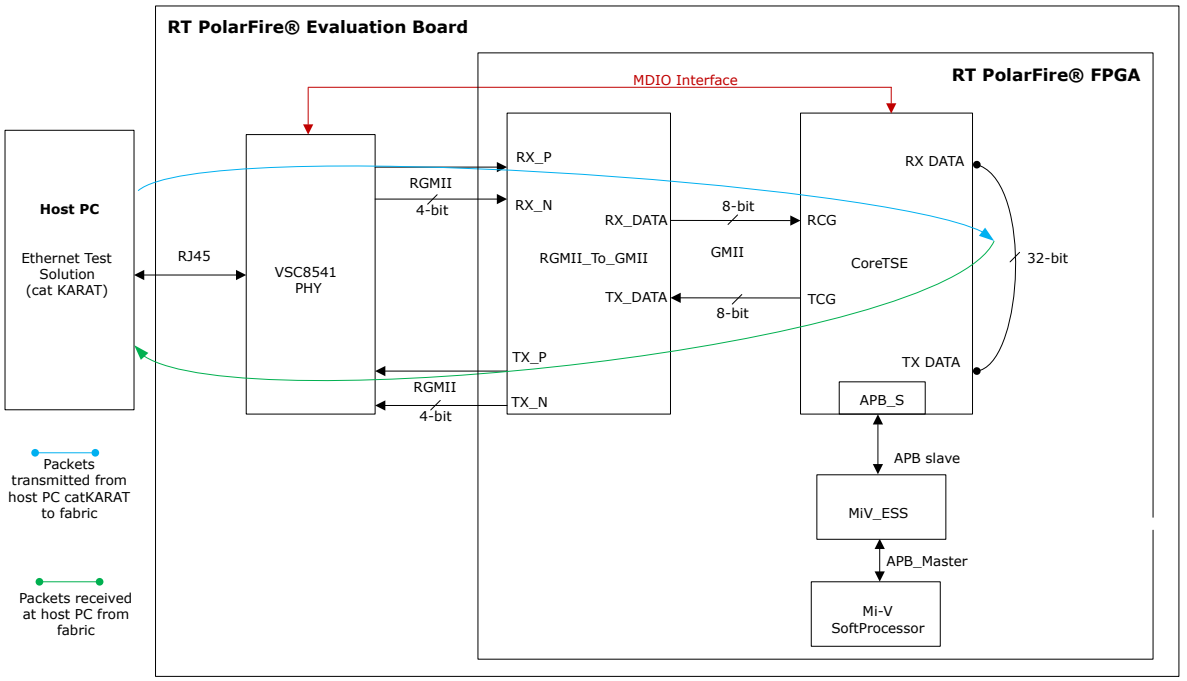
3. Design Description (Ask a Question)

To summarize the data flow of the 1G Ethernet loopback design,

1. The PF_CCC_0 IP provides the clock to the Mi-V processor and other APB peripherals.
2. The Mi-V soft processor performs the following functions:
   - Executes the application from TCM.
   - Configures the management registers of CoreTSE and VSC8541 PHY.
3. The CoreTSE IP implements 1G Ethernet MAC. The CoreTSE IP is configured in GMII mode to interface with the PF_RGMII_TO_GMII IP. The CoreTSE IP has an inbuilt MDIO interface to exchange control and status information with the VSC8541 PHY.
4. PF_RGMII_TO_GMII IP performs the following functions:
   - Interfaces with the on-board VSC8541 PHY and establishes an RGMII link.
   - Converts RGMII signals from VSC8541 PHY into GMII signals for the CoreTSE IP, and vice versa.

The following figure shows the functional blocks of the design.

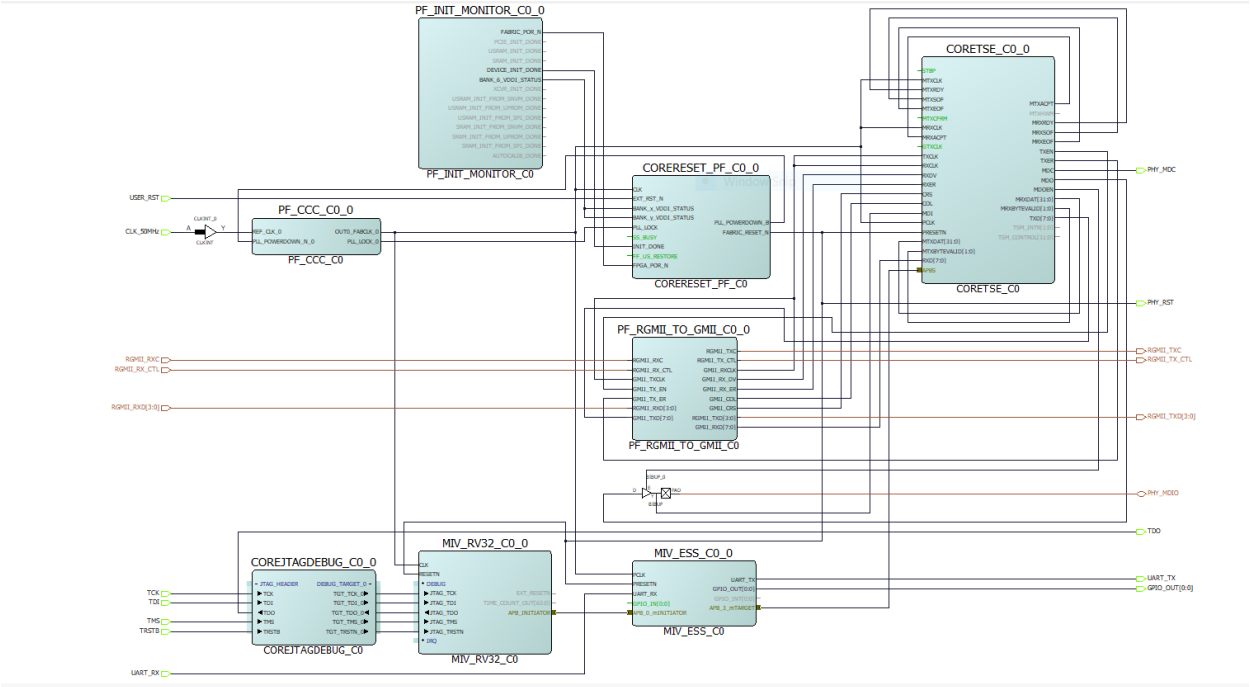
Figure 3-1. Block Diagram



4. Design Implementation (Ask a Question)

The following figure shows the Libero SoC implementation of the demo design.

Figure 4-1. Hardware Implementation



The following table lists the important I/O ports of the design.

Table 4-1. Important I/O Ports

Ports	Direction	Description
RGMII_RXC	Input	RGMII RX clock received from the on-board VSC8541 PHY.
RGMII_TXC	Output	RGMII TX clock sent to the on-board VSC8541 PHY.
RGMII_RX_CTL	Input	RX control signal received from the on-board VSC8541 PHY.
RGMII_TX_CTL	Output	TX control signal sent to the on-board VSC8541 PHY.
CLK_50MHz	Input	50 MHz input clock received from the on-board 50 MHz oscillator and fed to PF_CCC_C0.
TCK, TDI, TMS, and TRSTB	Input	JTAG signals interfaced with the soft processor for debugging.
RGMII_RXD[3:0]	Input	RX data signals connected to the on-board VSC8541 PHY transmit data signals.
RGMII_TXD[3:0]	Output	TX data signals connected to the on-board VSC8541 PHY receive data signals.
PHY_MDC	Output	Management Data I/O clock fed to the on-board VSC8541 PHY.
PHY_MDIO	Inout	Management Data I/O Interface for accessing the on-board VSC8541 PHY registers.
PHY_RST	Output	Active-high reset signal to the on-board VSC8541 PHY.
TDO	Output	JTAG test serial data output from tap.
TX and RX	Input and Output	UART controller signals for serial communication.
USER_RST	Input	Active-low design reset. Asserted by pressing the on-board E31 push button.
PHY_RST	Output	Active-high reset signal to the on-board VSC8541 PHY.
GPIO_OUT	Output	GPIO controller signal to interface with the on-board user LED.

4.1 IP Configuration (Ask a Question)

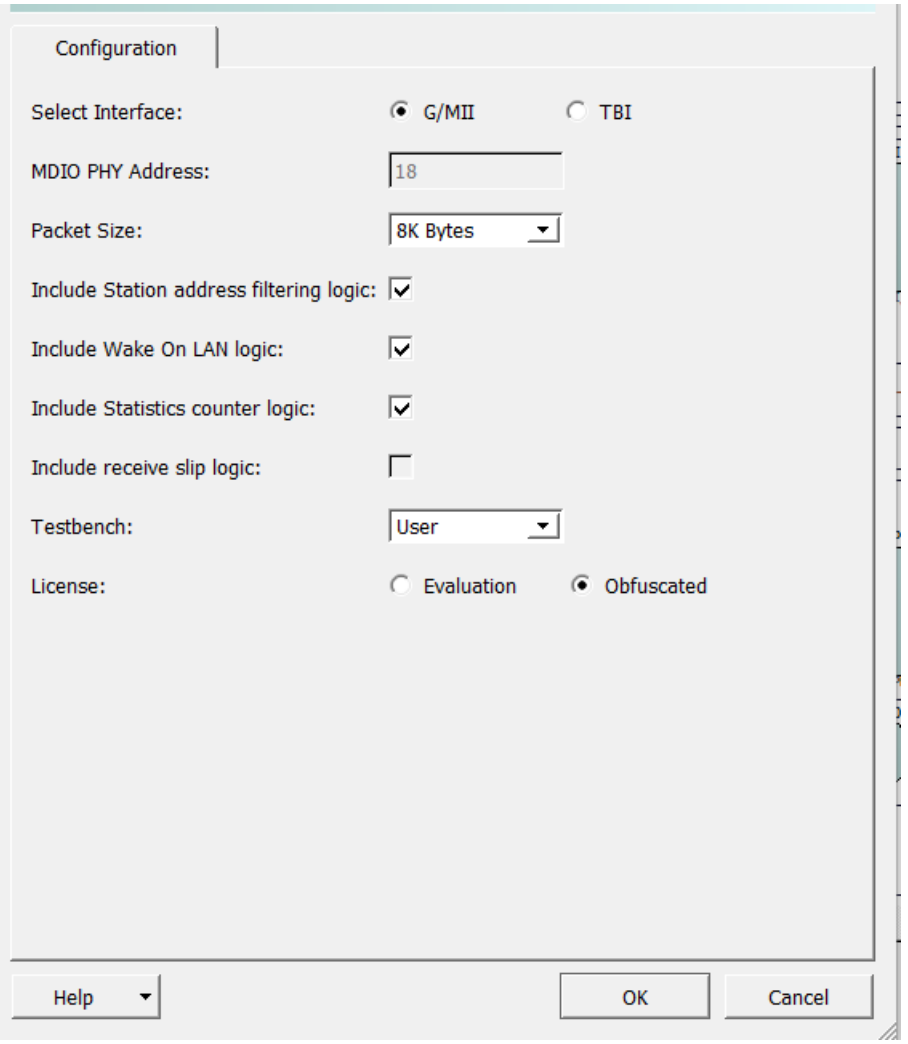
This section describes the IP blocks and user-defined blocks instantiated in the demo design.

4.1.1 CORETSE_C0 (Ask a Question)

The CORETSE_C0 (CoreTSE) IP implements the Ethernet MAC. This block is configured in GMII mode to interface with the PF_RGMII_TO_GMII IP, which interfaces with the VSC8541 PHY using the RGMII interface. The Mi-V soft processor uses the **MDIO PHY Address** value to read and write to the management registers of the CoreTSE IP. The **Include receive slip logic** option is not selected because the CoreTSE IP has a built-in word alignment logic in GMII mode. Use the **CoreTSE MAC IP** option to handle the transmission and reception of Ethernet packets.

The following figure shows the CoreTSE IP configuration.

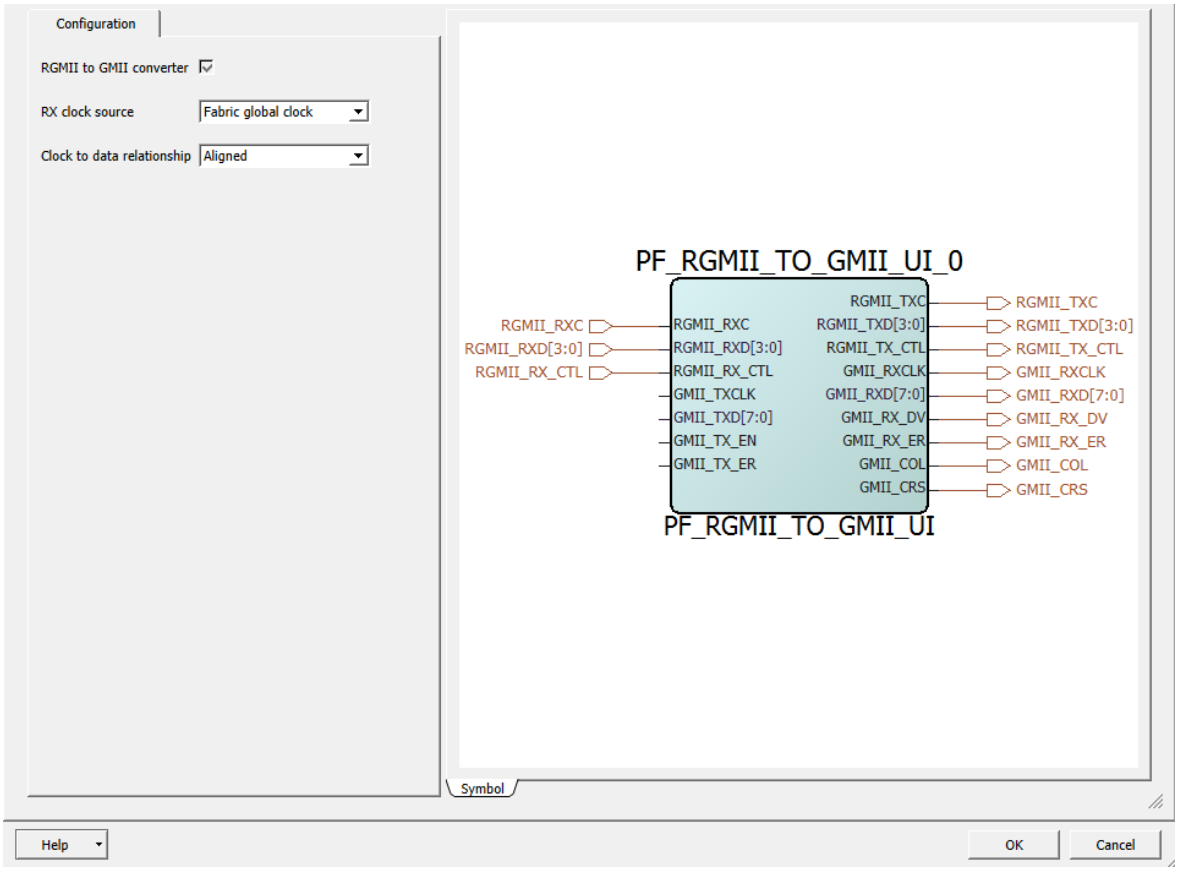
Figure 4-2. CoreTSE Configurator



4.1.2 PF_RGMII_TO_GMII (Ask a Question)

The PF_RGMII_TO_GMII IP converts RGMII data into GMII and vice versa. The following figure shows the PF_RGMII_TO_GMII IP configuration.

Figure 4-3. PF_RGMII_TO_GMII IP Configurator



4.1.3 PF_INIT_MONITOR_C0 (Ask a Question)

The PF_INIT_MONITOR_C0 IP is used to issue a reset signal to the user logic (FABRIC_RESET_N). To ensure a glitch-free reset, the DEVICE_INIT_DONE signal is connected to the CORERESET_PF_C0 IP with a lock signal from the PF_CCC_C0 macro. This IP retains the default configuration.

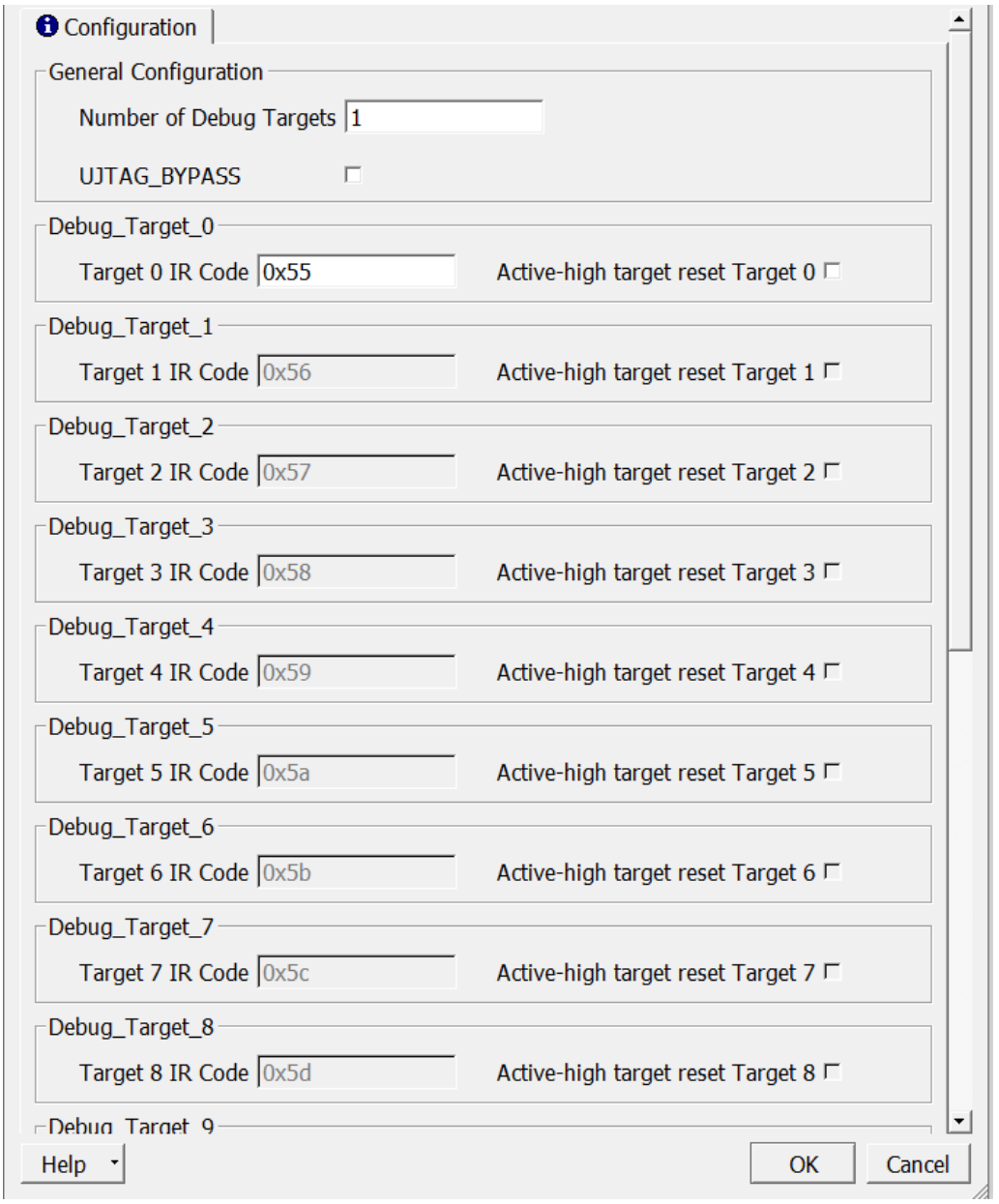
4.1.4 CORERESET_PF_C0 (Ask a Question)

The CORERESET_PF_C0 IP handles the sequencing of reset signals in the RT PolarFire device. The CORERESET_PF_C0 IP synchronizes the reset of all the connected blocks when the RT PolarFire device is powered up.

4.1.5 COREJTAGDEBUG_C0 (Ask a Question)

The CoreJTAGDebug IP is used to debug the Mi-V soft processor. The following figure shows the CoreJTAGDebug IP configuration.

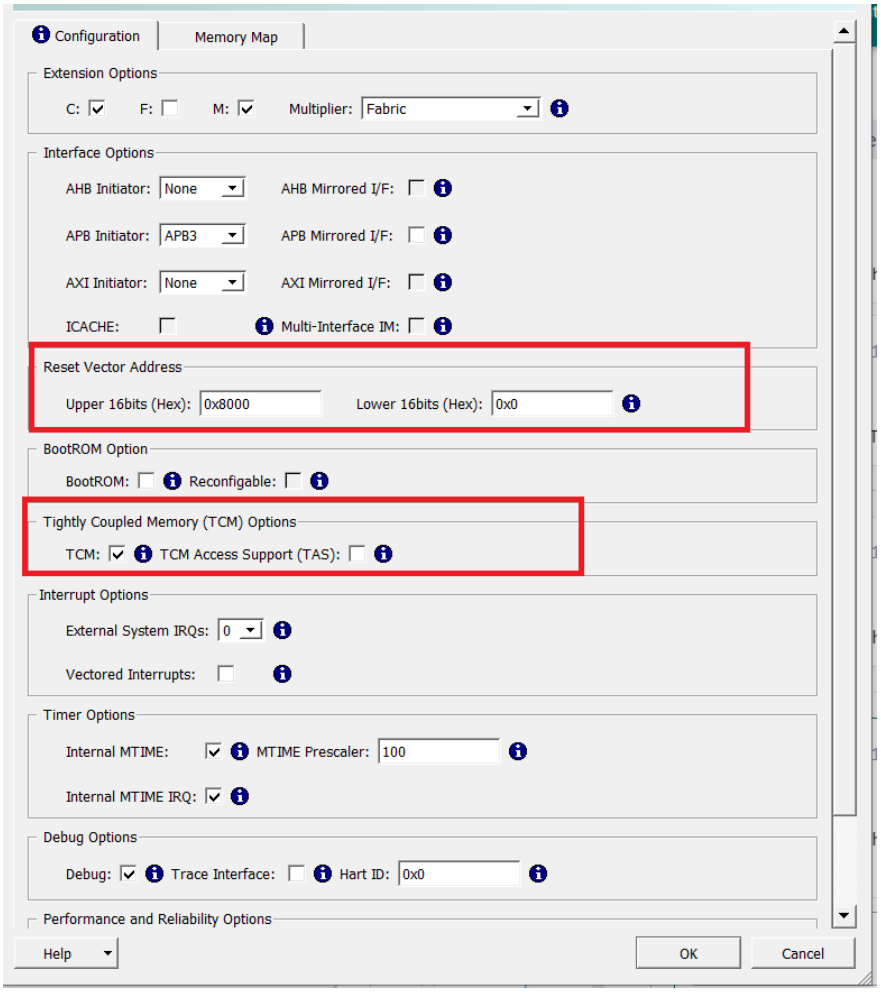
Figure 4-4. CoreJTAGDebug IP Configuration



4.1.6 MIV_RV32_C0 (Ask a Question)

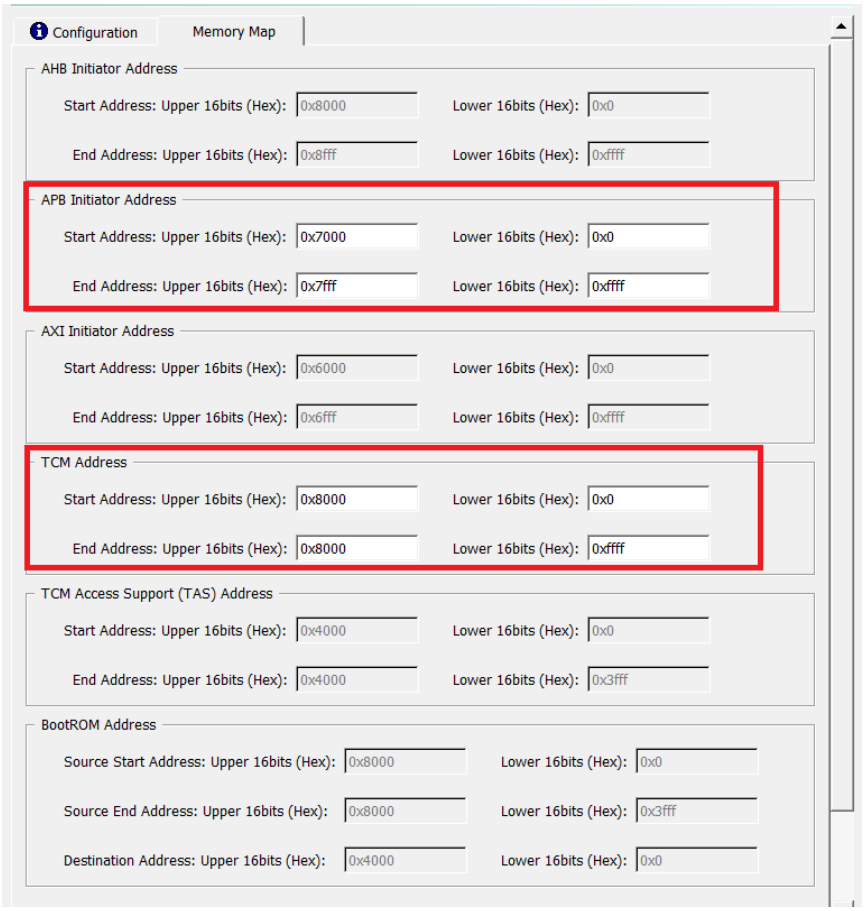
The MIV_RV32_C0 IP (Mi-V soft processor) supports RISC-V processor-based designs. It configures the VSC8541 PHY through the CoreTSE MDIO interface. It also configures the CoreTSE registers using the APB interface. The **Reset Vector Address** is set to 0x8000_0000 and **Tightly Coupled Memory (TCM)** option is set to TCM, see the following figure.

Figure 4-5. Mi-V Soft Processor Configuration-Rest Vector Address and TCM



The following figure shows the memory range used for the APB interface and the memory range used for TCM.

Figure 4-6. Mi-V Soft Processor Configuration-APB Interface and TCM Address Range

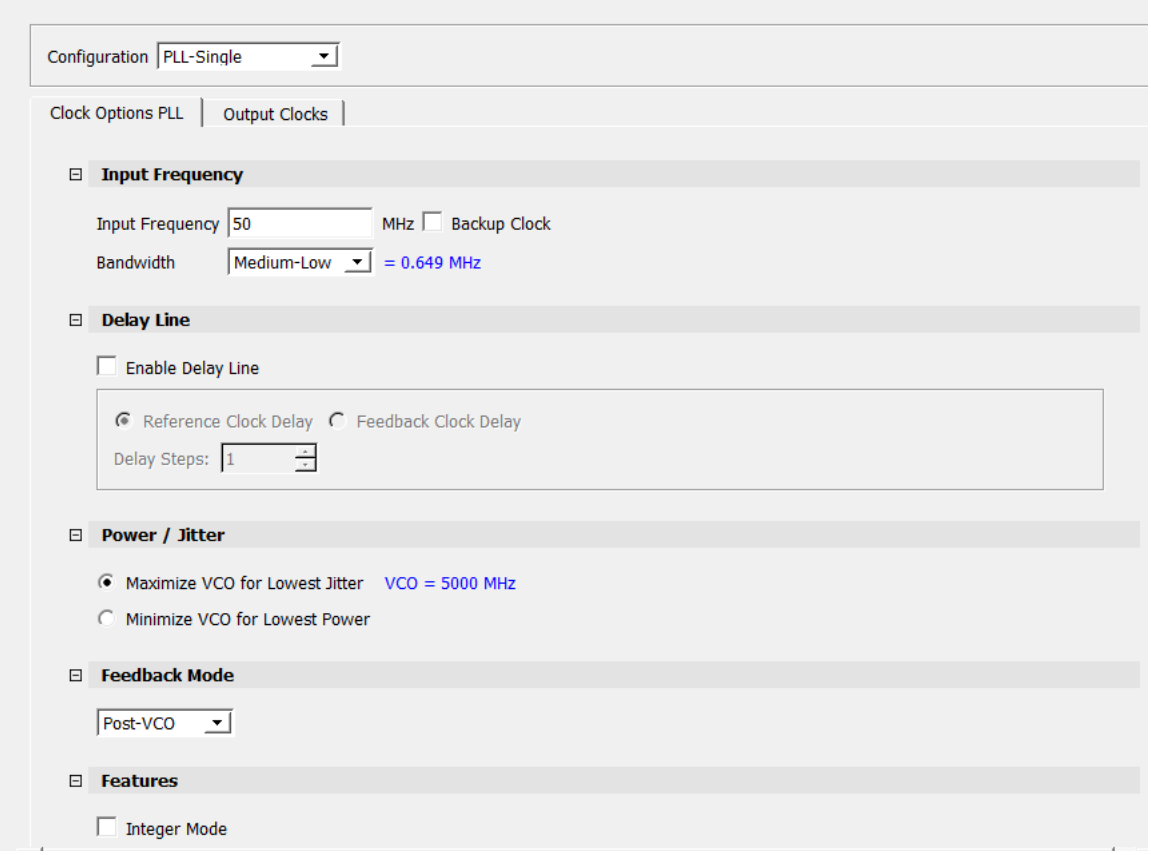


4.1.7 PF_CCC_C0 (Ask a Question)

The PF_CCC_C0 (Clock Conditioning Circuitry) generates the fabric reference clock that drives the soft processor and the APB peripherals (CoreTSE, CoreUARTapb, and CoreGPIO). The PF_CCC_C0 IP is configured to generate one output fabric clock from an on-board 50 MHz crystal oscillator.

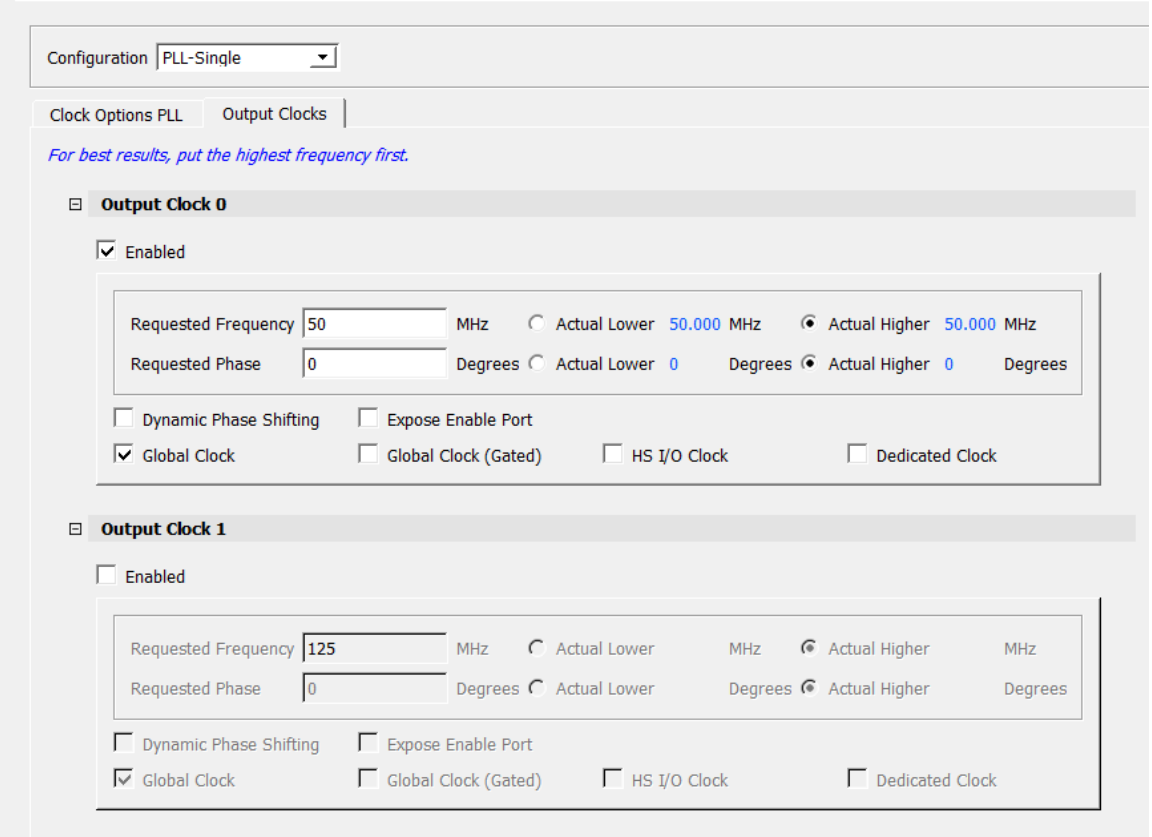
The following figure shows the PF_CCC_C0 input clock configuration.

Figure 4-7. PF_CCC PLL Configuration



The following figure shows the PF_CCC_C0 output clock configuration. The design uses a 50 MHz system clock.

Figure 4-8. PF_CCC Output Clocks Configuration



4.1.8 MiV_ESS_C0 (Ask a Question)

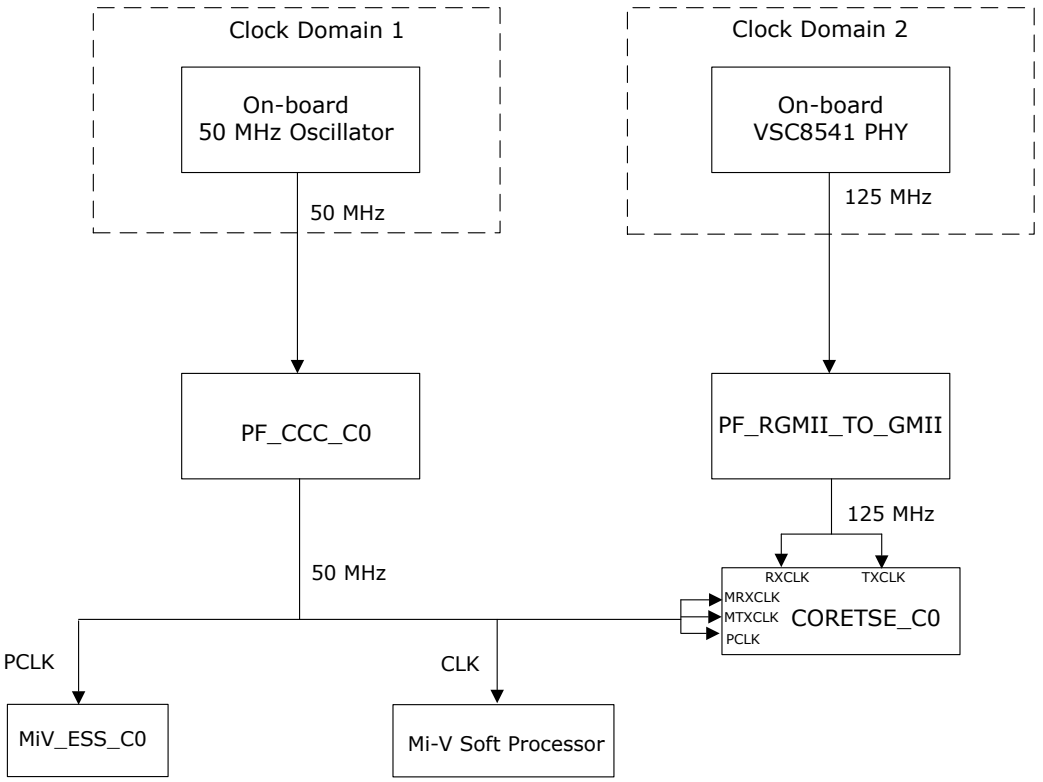
The MiV_ESS_C0 IP is used to connect the Mi-V soft processor with CoreTSE, CoreGPIO, and CoreUARTapb peripherals as slaves through MiV_ESS.

4.2 Clocking Structure (Ask a Question)

The on-board 50 MHz oscillator drives the PLL that generates a 50 MHz clock for the Mi-V soft processor and peripherals. In this design, the Mi-V soft processor runs at 50 MHz. Additionally, the following clocks are also used in the design:

- TX_CLK 125 MHz regional transmit clock (for 1000 Mbps), sourced from the MAC to the PHY.
- RX_CLK 125 MHz regional receive clock (for 1000 Mbps), sourced from the PHY to the MAC.

Figure 4-9. Clocking Structure

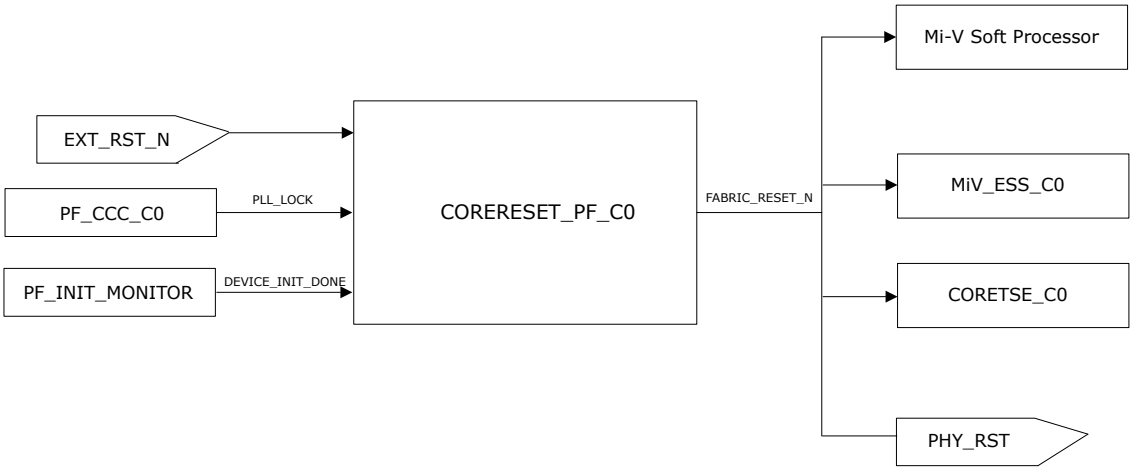


4.3 Reset Structure (Ask a Question)

The CoreUARTapb, CoreGPIO, Mi-V soft processor, CoreTSE, and PHY are reset using the CORERESET_PF_C0:FABRIC_RESET_N active-low signal. The CORERESET_PF IP asserts the FABRIC_RESET_N signal when the PF_CCC_C0: PLL_LOCK and PF_INIT_MONITOR_C0:INIT_DONE are asserted.

The following figure shows the reset structure of the design.

Figure 4-10. Reset Structure



5. Libero Design Flow (Ask a Question)

This section describes the steps to run the demo design using the Libero design flow. Before you start, open the Libero project by following these steps:

1. Download the design files and execute the TCL scripts to generate the Libero Project. www.microchip.com/en-us/application-notes/AN4509.

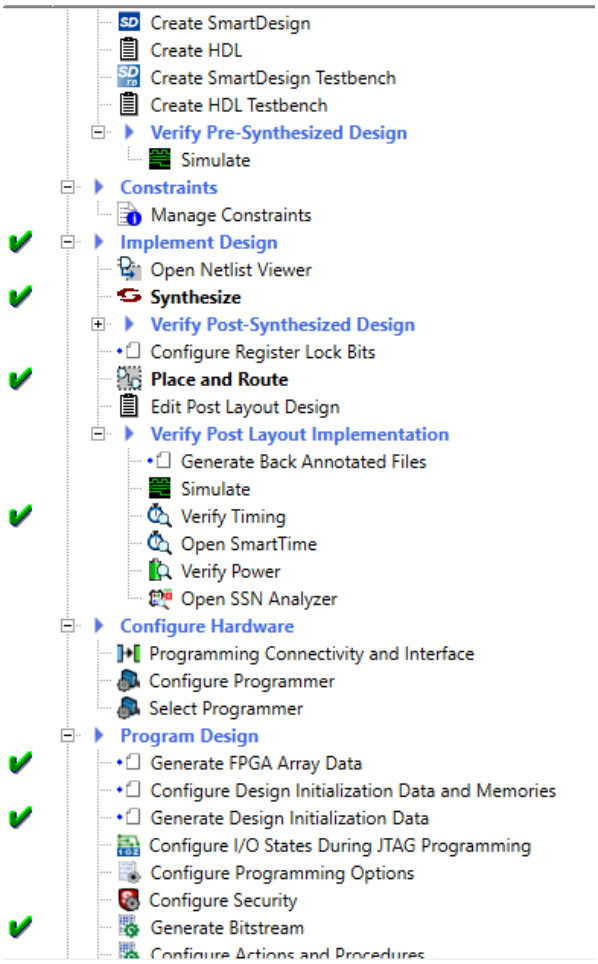
To complete the Libero design flow, run the following steps:

- 5.1. Synthesize
- 5.2. Place-and-Route
- 5.3. Verify Timing
- 5.4. Generate FPGA Array Data
- 5.5. Configure Design Initialization Data and Memories
- 5.6. Generate Bitstream
- 5.7. Run PROGRAM Action

Note: To initialize the TCM in RT PolarFire using the system controller, a local parameter `l_cfg_hard_tcm0_en`, in the `miv_rv32_subsys_pkg.v` file must be changed to `1'b1` prior to synthesis. See the 2.7 TCM section in MIV_RV32 Handbook.

The following figure shows these options in the Design Flow tab.

Figure 5-1. Libero Design Flow



5.1 Synthesize (Ask a Question)

To synthesize the design, on the **Design Flow** window, double click **Synthesize**.

When the synthesis is successful, a green tick mark appears next to **Synthesize**, see Figure 5-1.

5.2 Place-and-Route (Ask a Question)

To Place-and-Route the design, on the **Design Flow** window, double click **Place-and-Route**.

When Place-and-Route is successful, a green tick mark appears next to **Place-and-Route**, see Figure 5-1.

Important: When using the VSC8541 interface, set the PHY IOs to 3.3V. For more information, see RT PolarFire Schematics.

5.3 Verify Timing (Ask a Question)

To verify timing, on the **Design Flow** window, double click **Verify Timing**.

When the design successfully meets the timing requirements, a green tick mark appears next to **Verify Timing**, see Figure 5-1.

5.4 Generate FPGA Array Data (Ask a Question)

On the **Design Flow** window, double click **Generate FPGA Array Data**.

When the FPGA array data are successfully generated, a green tick mark appears next to **Generate FPGA Array Data**, see Figure 5-1.

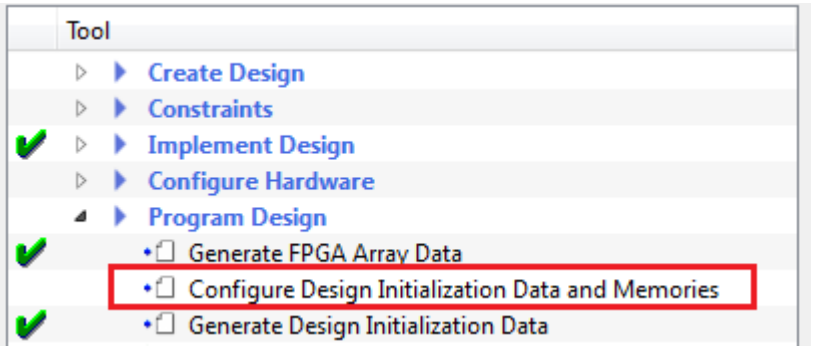
5.5 Configure Design Initialization Data and Memories (Ask a Question)

The TCM block must be initialized with the user application to configure the PHY and management registers of CoreTSE. The user application (`.HEX` file) is generated using SoftConsole. This step is used to select the TCM client (`.HEX` file), its storage location (sNVM, µPROM, or SPI Flash), and generate the TCM client. The nonvolatile memory is programmed with this client and at device power-up, the TCM block is initialized with the content from the selected NVM. The Configure Design Initialization Data and Memories option creates the TCM initialization client. When the RT PolarFire device powers up, the TCM memory is initialized with the sNVM contents.

To create the TCM initialization client, perform the following steps:

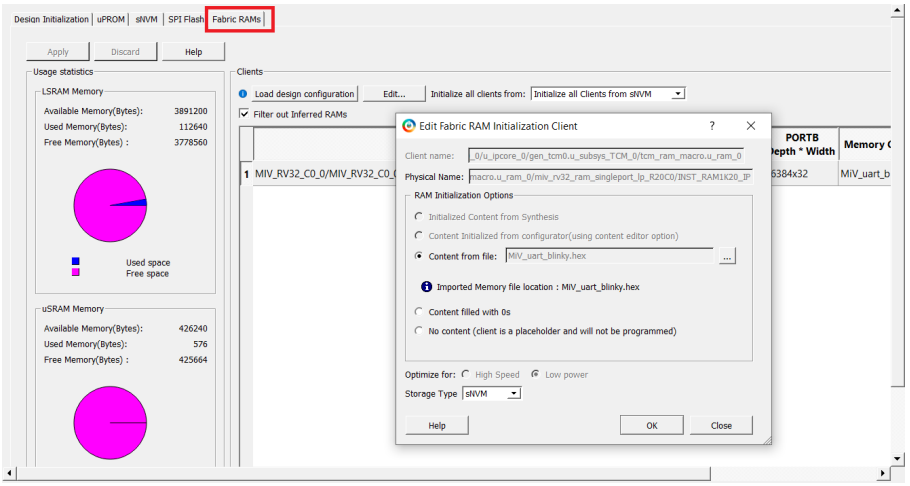
1. On the **Design Flow** window, double click **Configure Design Initialization Data and Memories**, see the following figure.

Figure 5-2. Configure Design Initialization and Memories Option



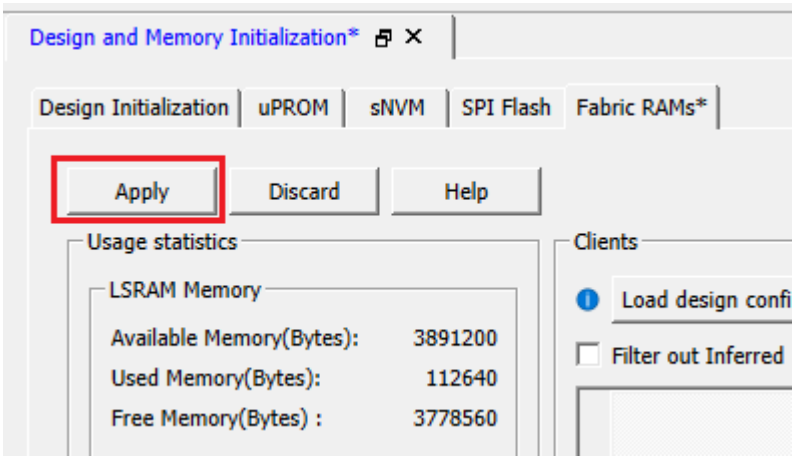
2. In the **Fabric RAMs** tab, configure the `MIV_RV32_C0_0/MIV_RV32_C0_0/u_ipcore_0/gen_tcm0.u_subsys_TCM_0/tcm_ram_macro.u_ram_0` instance and ensure contents are stored in sNVM, set the **Storage Type** as **sNVM**, see the following figure.

Figure 5-3. Fabric RAMs Tab



3. Click **Apply**, see the following figure.

Figure 5-4. Applying the Fabric RAM Content



4. On the **Design Flow** window, double click **Generate Design Initialization Data**. When the initialization client is successfully generated in sNVM, a green tick mark appears next to **Generate Design Initialization Data**, see Figure 5-1.

5.6 Generate Bitstream (Ask a Question)

To generate the bit stream, on the **Design Flow** window, double click **Generate Bitstream**.

When the bit stream is successfully generated, a green tick mark appears next to **Generate Bitstream**, see Figure 5-1.

5.7 Run PROGRAM Action (Ask a Question)

After generating the bit stream, the RT PolarFire device must be programmed. The programming procedure involves setting up board and invoking the programming command.

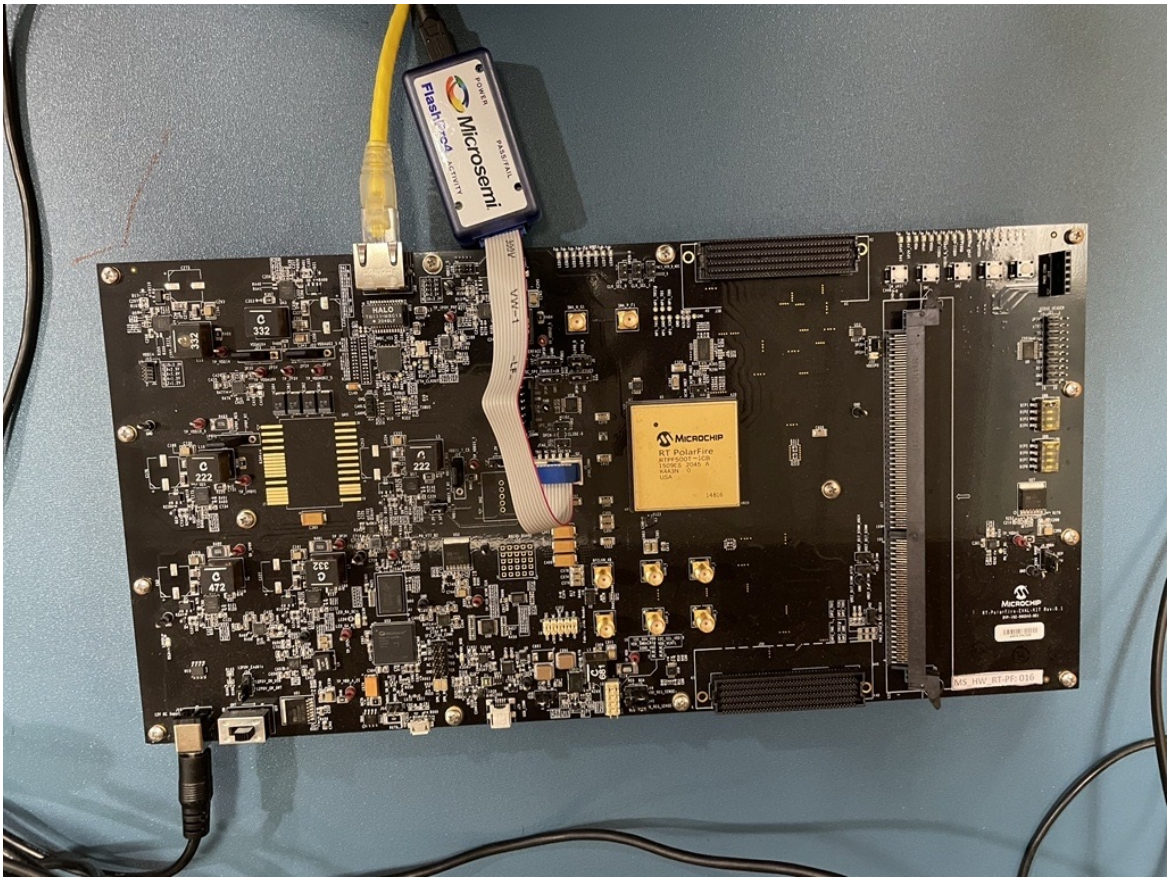
Note: If you want to program the board using the `.job` file instead, see 7. Appendix 1: Programming the Device Using FlashPro Express.

Follow these steps:

1. Ensure that the **RJ45** cable is connected from the host PC to the **J68** connector on the board.
2. Ensure the jumper settings on the board are set to the default except the following:
   - **J15**—Short pin 9 and 10
   - **J22**—Short pin 2 and 3
   - **J31**—Open (when programming through External FlashPro programmer)
3. Connect the host PC to the **J3** connector using External FlashPro Programmer.
4. Connect the power supply to the **J19** connector.
5. Power up the board using the **SW7** slide switch.
6. Confirm that **VSC8541_LED0 (LD1)** and **VSC8541_LED1 (LD2)** glow, indicating the Ethernet PHY link is up and running.

The following figure shows the board setup.

Figure 5-5. Board Setup



1. On the **Design Flow** window, double click **Run PROGRAM Action**.
2. When the device is successfully programmed, and a green tick mark appears next to **Run PROGRAM Action**, see Figure 5-1.

The demo design is ready to run. For more information about how to run the demo, see 6. Running the Demo.

6. Running the Demo (Ask a Question)

This section describes the steps to run the 1G loopback demo. The procedure involves transmitting packets from the network card of the host PC to the board and verifying the packets transmitted to and received from the board using Cat Karat.

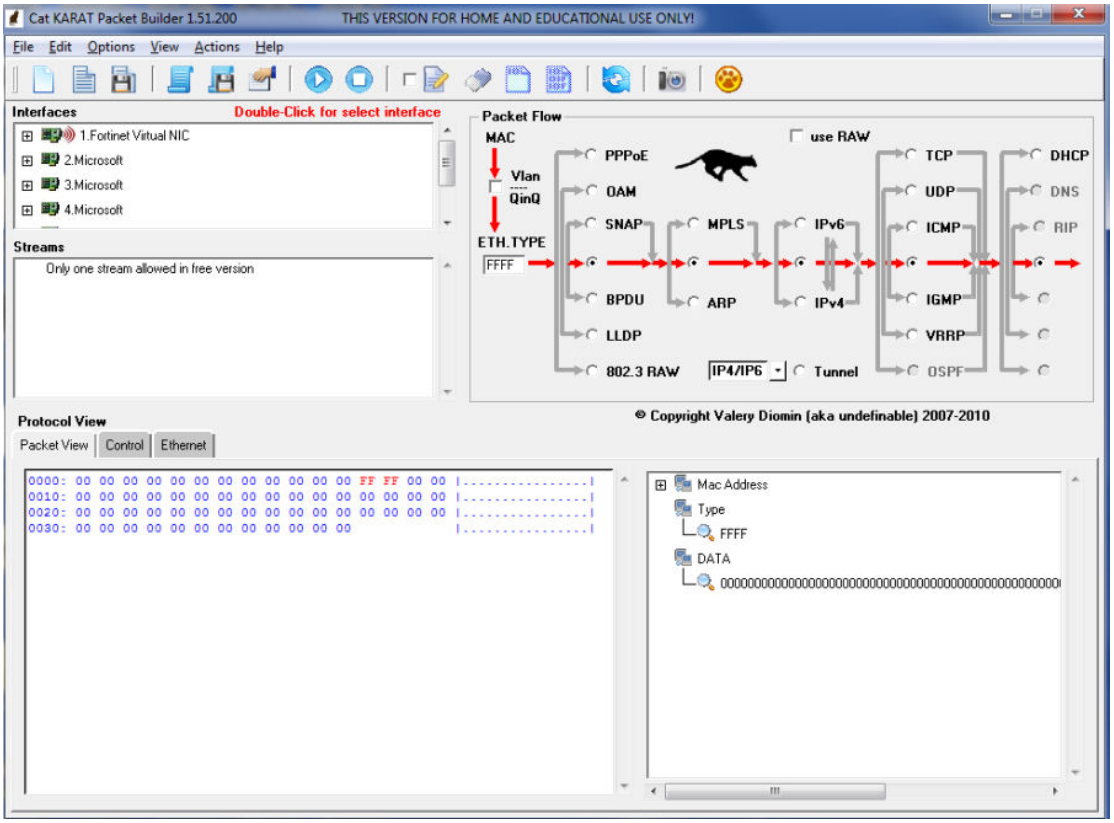
Before you start, ensure that the following steps are completed:

- Setting up the hardware, see the steps described in 5.7. Run PROGRAM Action.
- Programming the device, see 7. Appendix 1: Programming the Device Using FlashPro Express.

To run the demo, follow the steps:

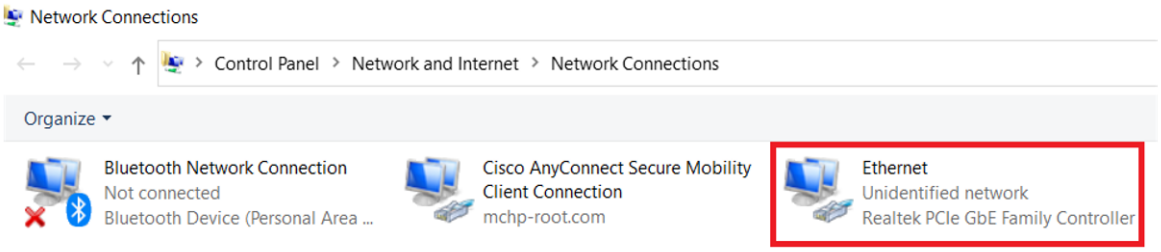
1. Open the Cat Karat software from the Start menu of the host PC.
   The Cat Karat Packet Builder window opens, see the following figure.

Figure 6-1. Cat Karat Packet Builder Window



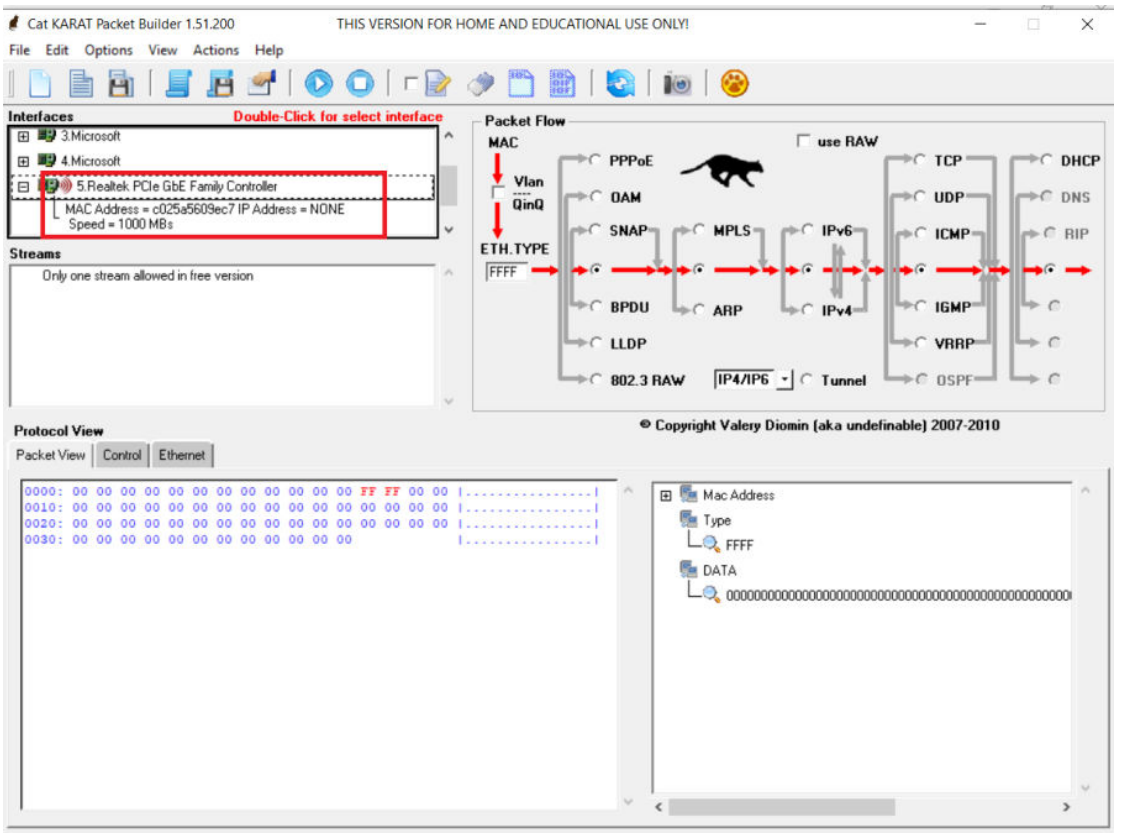
2. From the control panel of the host PC, note the name of the Ethernet network connection, see the following figure. On a Windows 10 machine, this connection is **Ethernet**.

Figure 6-2. Ethernet Network Connection



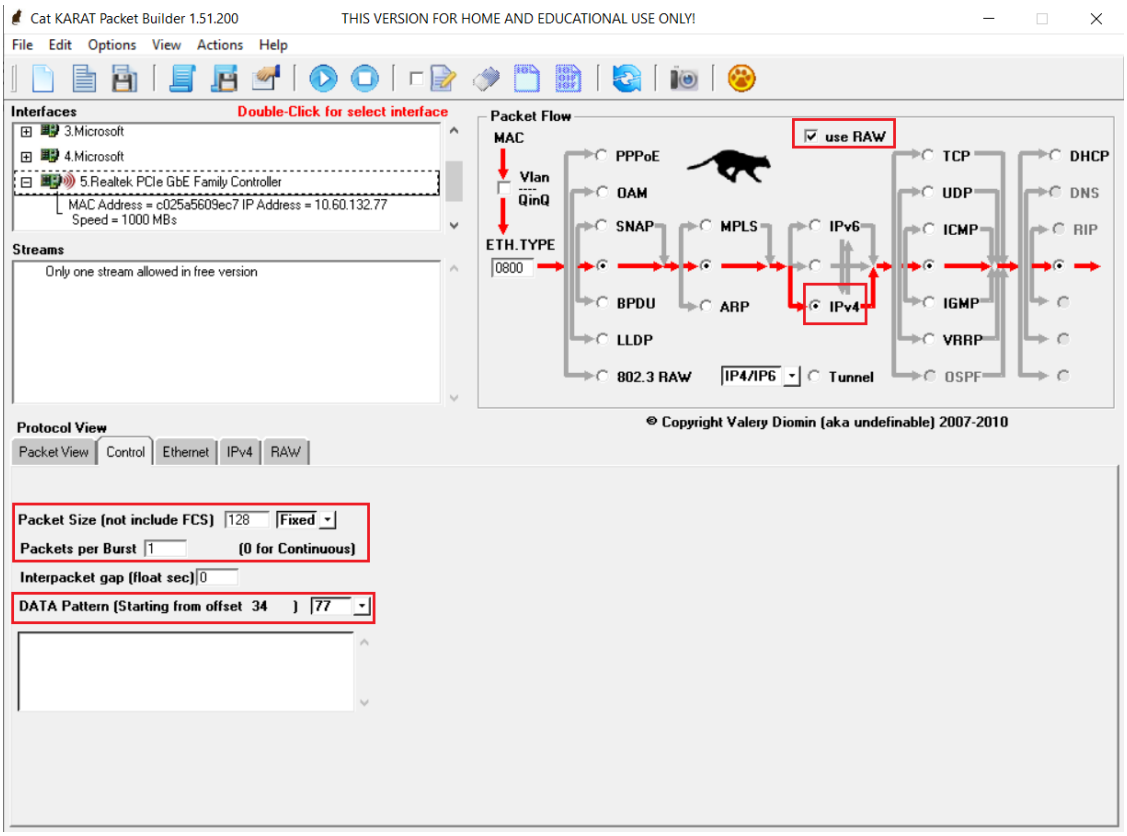
3. In the **Cat Karat Packet Builder** > **Interfaces** pane, double click **Ethernet network connection**, see the following figure.

Figure 6-3. Interface Selection



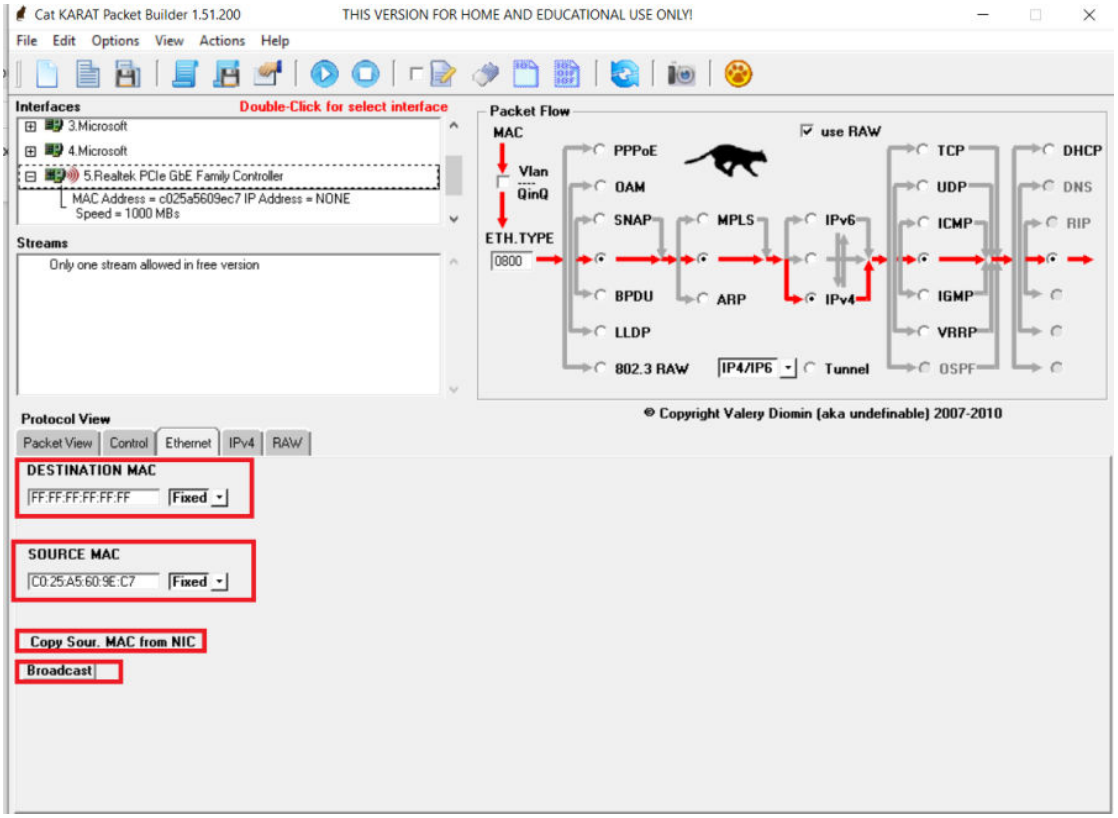
4. In the **Control** tab, select **use RAW** check box and **IPv4** from the list, and set **Packets per Burst** to **1**, **Packet Size** to **128** and the **Data Pattern** to **77**, see the following figure.

Figure 6-4. Cat Karat Control Tab

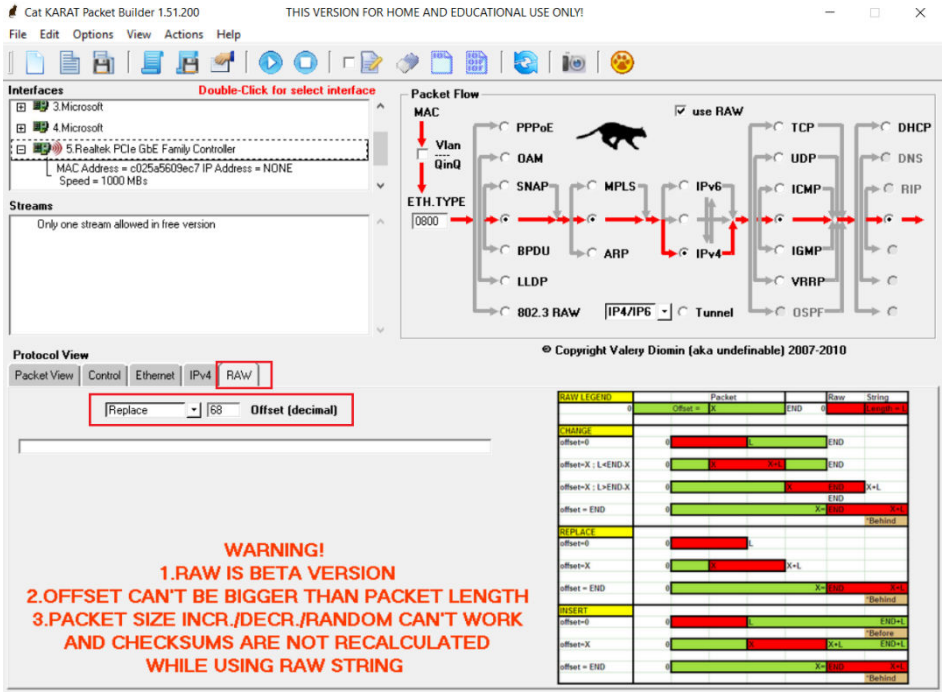


5. In the **Ethernet** tab, select **Copy Source MAC from NIC** for **Source MAC** and select **Broadcast** for **Destination MAC**, see the following figure.

Figure 6-5. Cat Karat Ethernet Tab

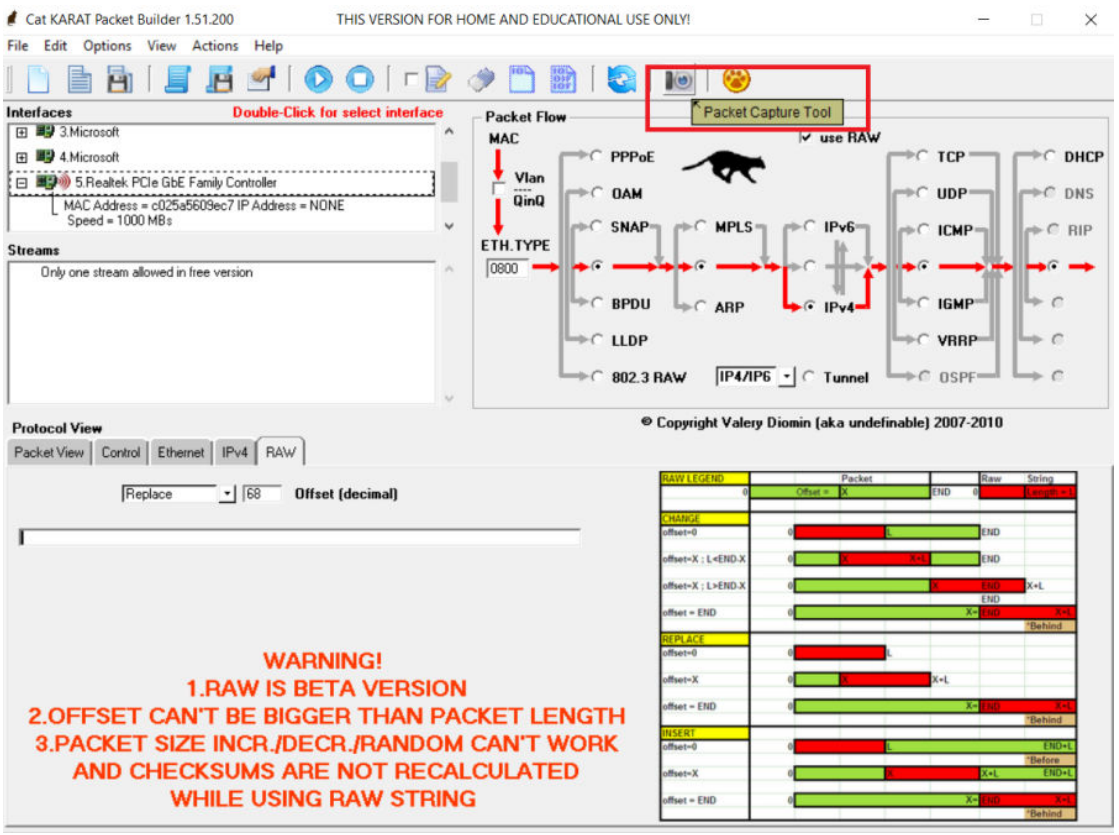


6. In **IPv4** tab, retain the default settings.
7. In **RAW** tab, configure **Offset**, see the following figure.



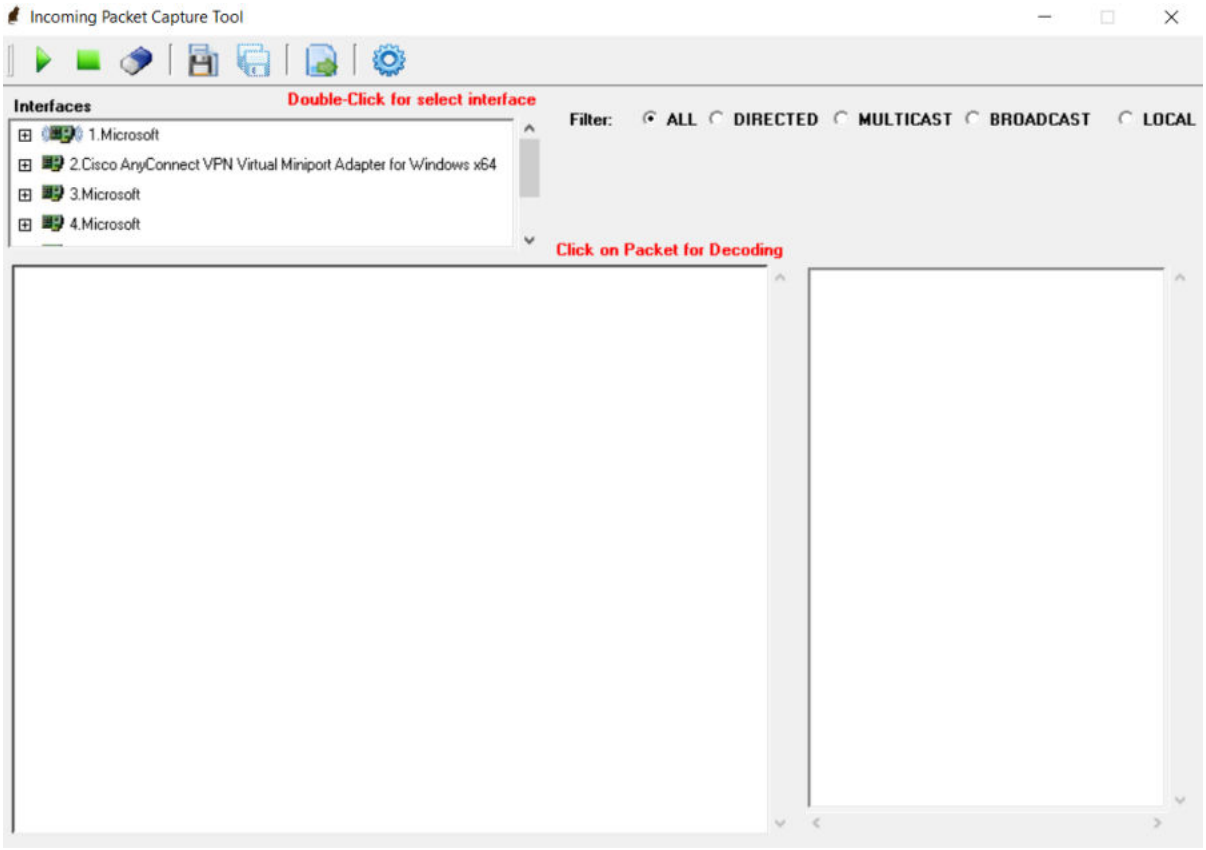
8. Launch **Packet Capture Tool**, see the following figure.

Figure 6-6. Packet Capture Tool



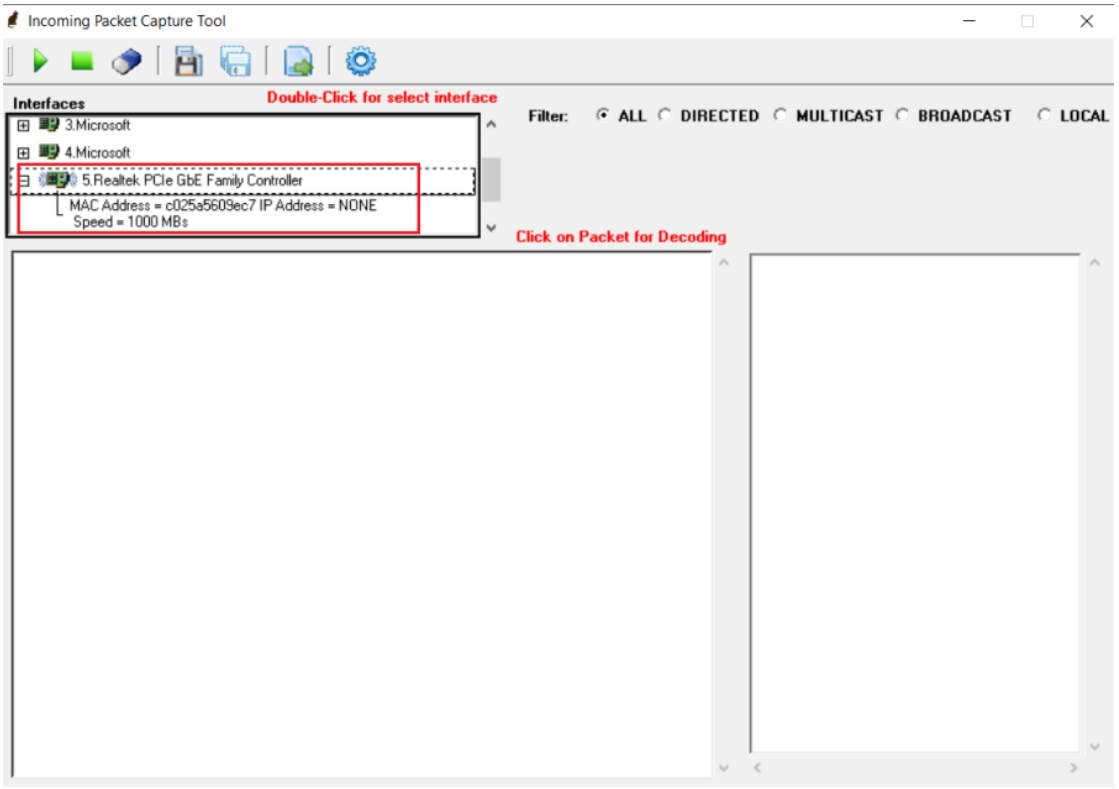
9. Monitor the transmitted and received packets on the **Incoming Packet Capture Tool** window, see the following figure.

Figure 6-7. Incoming Packet Capture Tool



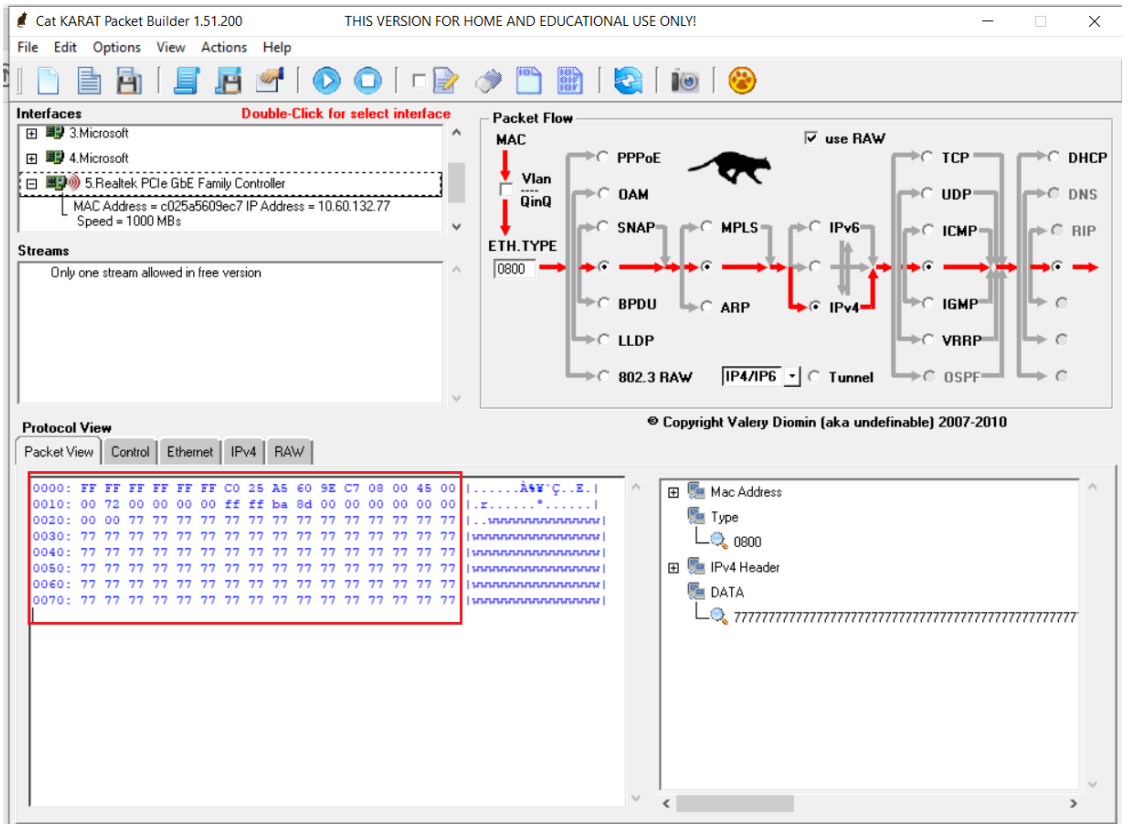
10. In **Incoming Packet Capture Tool**, select the Interface in **Interfaces** pane, see the following figure.

Figure 6-8. Incoming Packet Capture Tool: Interfaces Pane



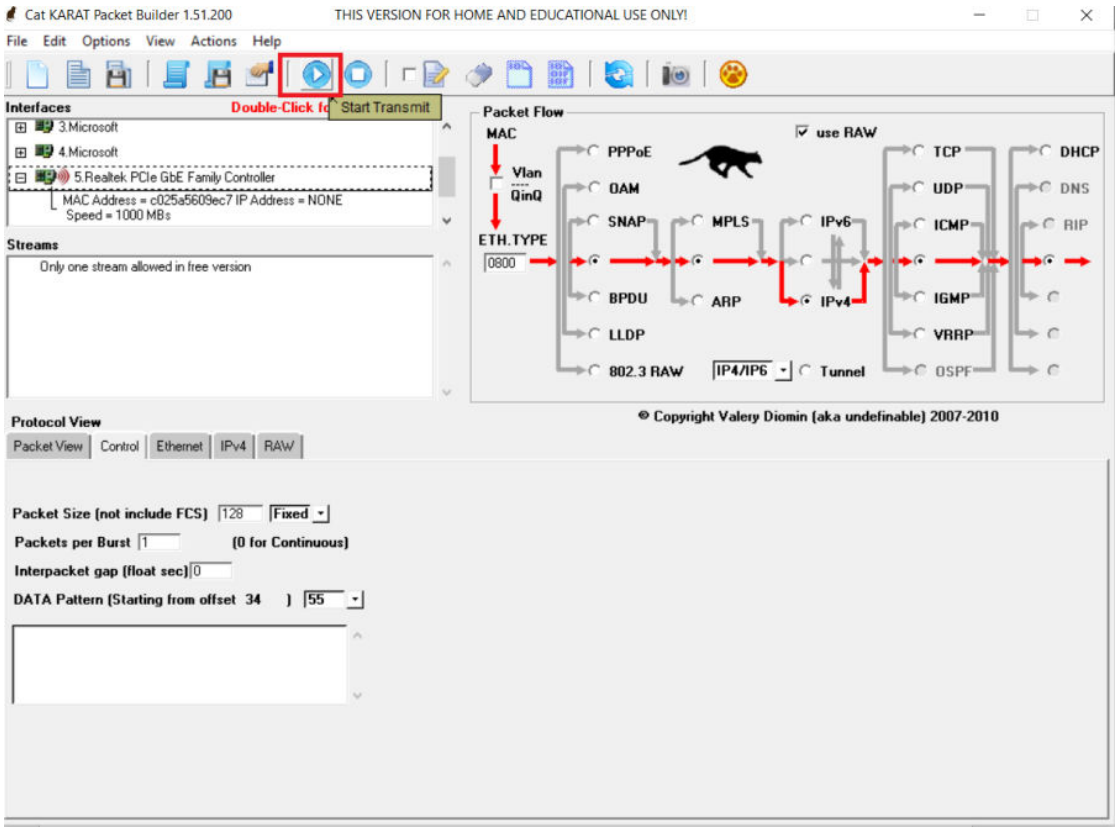
11. Before transmitting, in the **Packet View** tab, check the packet being transmitted, see the following figure.

Figure 6-9. Packet View Tab



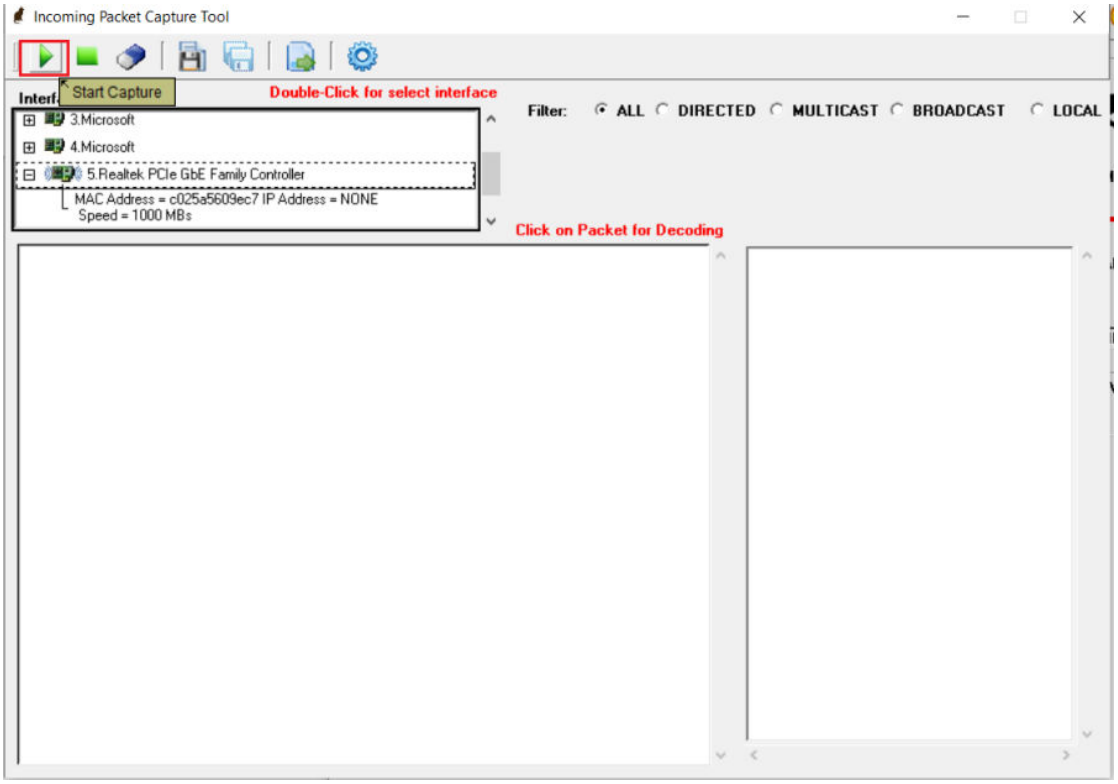
12. In the **Cat Karat** window, click **Start Transmit** to transmit 1 packet from the host PC to the board, see the following figure.

Figure 6-10. Start Transmit



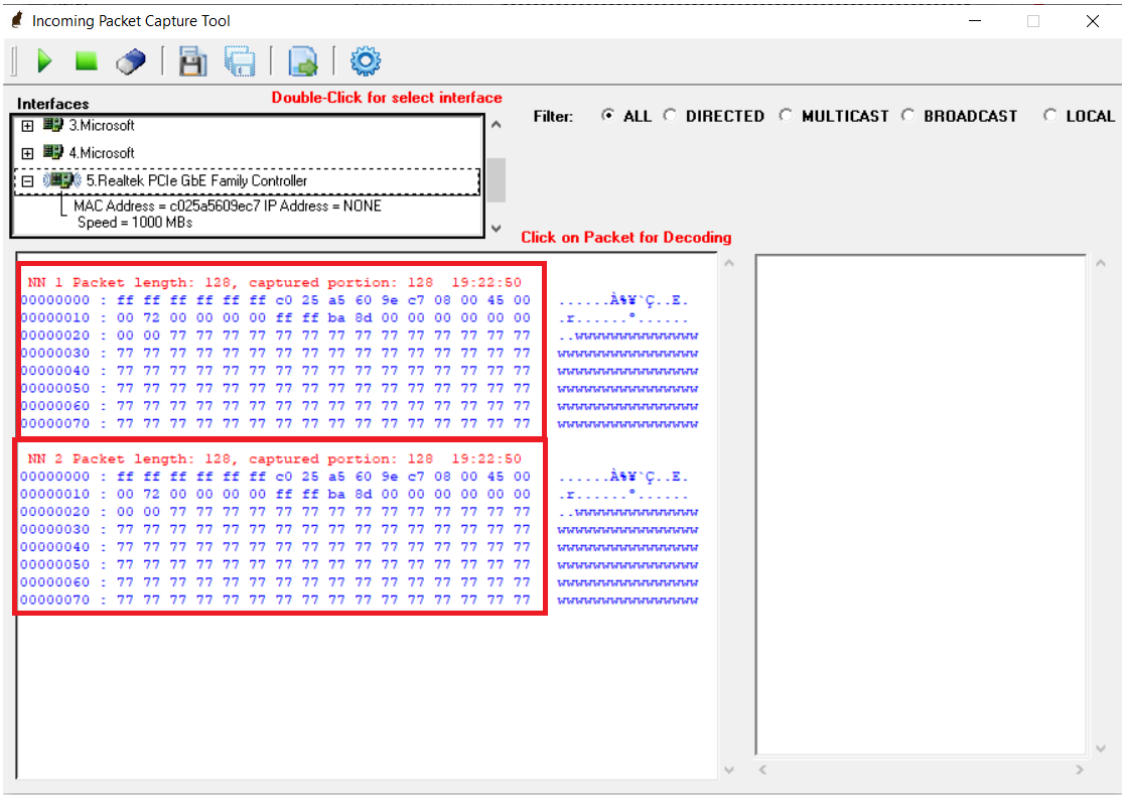
13. Click the **Start Capture** option in **Incoming Packet Capture Tool** window, see the following figure.

Figure 6-11. Start Capture



14. After clicking **Start Capture**, you see the transmitted and received packets, see the following figure.

Figure 6-12. Transmitted and Received Packets



The preceding figure shows that one packet was transmitted from the host PC to the board. The same packet was looped back at the CoreTSE IP and was sent back to the host PC. All packets transmitted from the host PC network are looped back in the same way.

15. Select different burst rates, data patterns, and transmit packets to the board.
16. Power-down the board and close the Cat Karat software.

You have successfully run the demo.

7. Appendix 1: Programming the Device Using FlashPro Express (Ask a Question)

This section describes the steps to program the RT PolarFire device with the `.job` file using FlashPro Express. The `.job` file is available at `<$Download_Directory>\rtpf_an4509_v2023p2_df\Programming_Job`.

To program the device using FlashPro Express, follow the steps:

1. Start the FlashPro Express software from its installation directory.
2. On the **Project** menu, click **New** or **New Job Project from FlashPro Express Job** to create a new job project.
3. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:
   - **Programming job file**: Click **Browse** and select the `.job` file from `<$Download_Directory>\rtpf_an4509_v2023p2_df\Programming_Job`
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.
6. Click **RUN** to program the device. When the device is programmed successfully, a “RUN PASSED” message is displayed.
7. Close FlashPro Express (**Project** > **Exit**).

8. Appendix 2: Running the TCL Script (Ask a Question)

TCL scripts are provided in the design files folder under the TCL_Scripts directory. If required, the design flow can be reproduced from Design Implementation till the generation of `.job` file.

To run the TCL script, follow the steps:

1. Launch the Libero SoC.
2. Click **Project** > **Execute Script**.
3. Click **Browse** and select `script.tcl` from `<$Download_Directory>\rtpf_an4509_v2023p2_df\TCL_Scripts`.
4. Click **Run**. After successful execution of TCL script, Libero project is created within TCL_Scripts directory. For more information about TCL scripts, see `<$Download_Directory>\rtpf_an4509_v2023p2_df\TCL_Scripts\readme.txt`. For more information about TCL commands, see Libero® SoC TCL Command Reference Guide. Contact Microchip Support for any queries encountered when running the TCL script.

9. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Revision	Date	Description
B	09/2023	The following is the list of changes in the revision B of the document: • Updated the Design revision from 0.1 to 1.0 in Table 1-1 • Updated Figure 3-1 • Updated Figure 4-1 • Removed a note from Table 4-1 • Updated Figure 4-2 • Updated Figure 4-6 • Removed CoreUARTapb_C0 section • Removed CoreGPIO_C0 section • Replaced CoreAPB3_C0 with MIV_ESS_C0 • Removed instances of CoreGPIO and CoreUARTapb • Updated Figure 4-10 • Updated Figure 4-5 • Removed step 2 from 5. Libero Design Flow section • Updated file name from miv_rv32_opsrv_cfg_pkg.v to miv_rv32_subsys_pkg.v in 5. Libero Design Flow note. • Added a note in 5.2. Place-and-Route section • Updated Figure 5-3 • Updated design file from rtpf_an4509_df to rtpf_an4509_v2023p2_df in 7. Appendix 1: Programming the Device Using FlashPro Express and 8. Appendix 2: Running the TCL Script sections • Updated programming file from Programming_File to Programming_Job in 7. Appendix 1: Programming the Device Using FlashPro Express section
A	04/2022	Initial Revision

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