UG0747
User Guide
PolarFire FPGA Evaluation Kit

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

Updated the PolarFire Power Monitor link under Prerequisites, page 36.

1.2 Revision 10.0

Updated the note under Table 6, page 11.

1.3 Revision 9.0

Following is a list of changes that are made in this revision.

- Updated Table 1, page 2 with the License information. The License information is removed from the table.
- Updated Software Settings, page 8 with License information.

1.4 Revision 8.0

Added a note about DQ swapping in Memory Interface, page 14 section.

1.5 Revision 7.0

Throughout the document replaced DDR3 with DDR3L as per *PCN21009*.

1.6 Revision 6.0

Updated Table 6, page 11 voltages information for Bank0 and Bank1.

1.7 Revision 5.0

Added Table 7, page 12 that lists the suggested power regulators.

1.8 Revision 4.0

Added performance measurement data for different protocols, see Appendix 4: Performance Data, page 39.

1.9 Revision 3.0

Updated Figure 18, page 33 and Figure 19, page 33.

1.10 Revision 2.0

Updated Appendix 3: Power Monitoring, page 36.

1.11 Revision 1.0

The first publication of this document.

2 Getting Started

The Microchip PolarFire® FPGA Evaluation Kit (MPF300-EVAL-KIT), which is RoHS-compliant, enables you to evaluate the PolarFire family of FPGAs with support for the following interfaces:

- PCI Express Gen1 and Gen2
- 1 GbE
- DDR3L and DDR4 memory
- FMC HPC with 8 Transceiver lanes
- 1 Full-Duplex Transceiver SMAs
- SFP+ Cage
- UART Interface to FTDI device
- SPI Interface to SPI Flash device

2.1 Kit Contents

The following table lists the contents of the PolarFire FPGA Evaluation Kit.

Table 1 • **Kit Contents**

Item	Quantity
PolarFire Evaluation Board (printed circuit board) featuring MPF300TS-1FCG1152I device with 300K logic elements	1
12 V/5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for UART/power interface (up to 1 A) to PC	1
Quickstart card	1

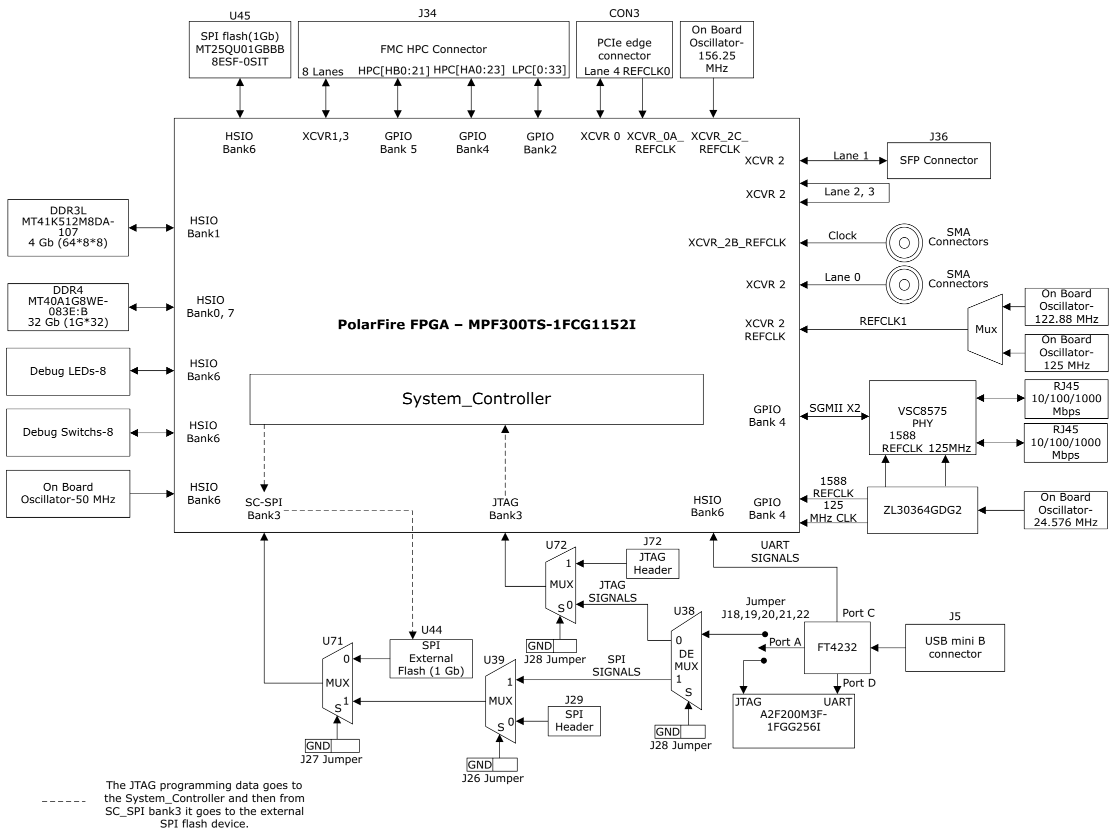
Note: The PolarFire device is programmed using the on-board FlashPro5 programmer. The on-board FlashPro5 programmer is used to develop and debug embedded applications using SoftConsole, Identify, or SmartDebug.

For more information, see *UG0726: PolarFire FPGA Board Design User Guide*.

2.2 Block Diagram

The following block diagram shows all of the components of the PolarFire Evaluation Board.

Figure 1 • **PolarFire Evaluation Kit Block Diagram**



2.3 Web Resources

For more information about the PolarFire Evaluation Board, see https://www.microchip.com/en-us/development-tool/MPF300-EVAL-KIT.

2.4 Board Overview

The PolarFire Evaluation Board features the PolarFire MPF300TS-1FCG1152I FPGA. The device has the following capabilities:

- 20 Kb dual-port or two-port large static random access memory (LSRAM) block with a built-in single error correct double error detect (SECDED)
- 64 × 12 two-port µSRAM block implemented as an array of latches
- 18 × 18 Multiply Accumulate (MACC) block with a pre-adder, a 48-bit accumulator, and an optional 16 deep × 18 coefficient RO
- Built-in µPROM, modifiable at program time, readable at run time for user data storage
- Digest integrity check for FPGA, µPROM, and sNVM
- Low-power features:
    - Low device static power
    - Low inrush current
    - Low power transceivers
    - Unique Flash*Freeze (F*F) mode
    - High-performance communication interfaces

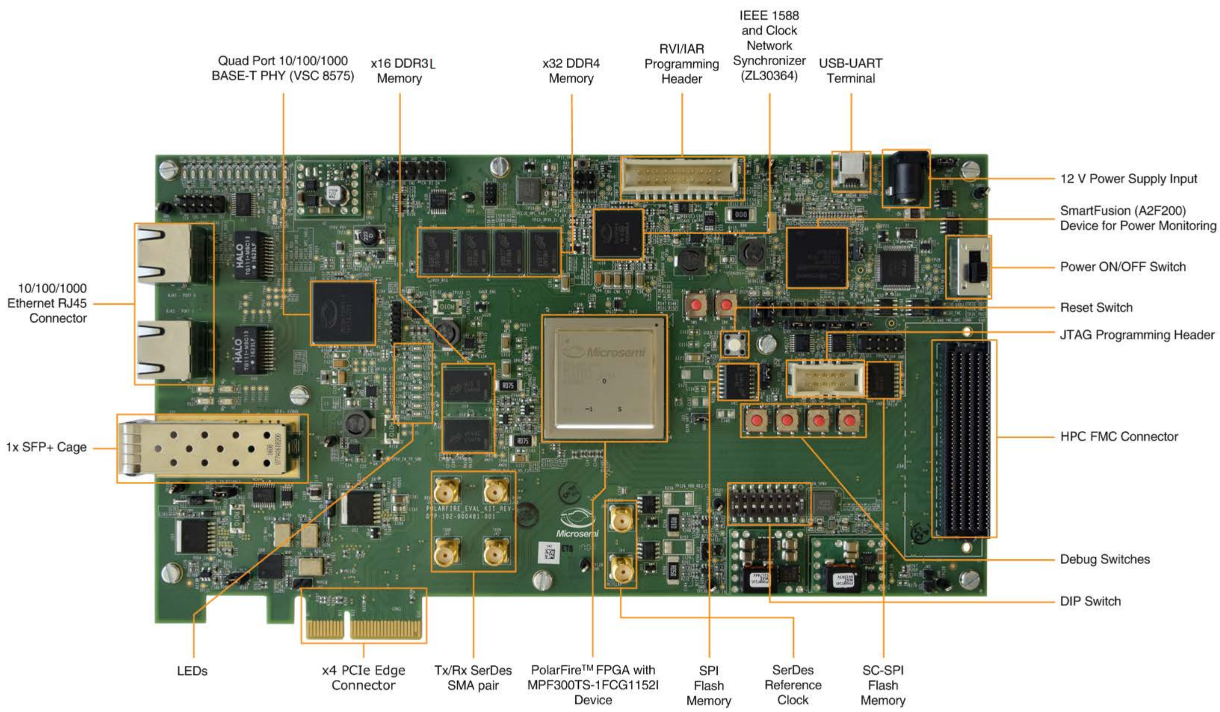
The PolarFire Evaluation Board has several standard interfaces, including:

- VSC8575 with two RJ45 connector for 10\100\1000 Mbps Ethernet
- 8 Full-Duplex Transceiver lanes connected through FMC connector
- FMC HPC connector
- DDR3L memory
- DDR4 memory
- Power Sequence and monitor chip
- x4 Lane PCIe Edge connector
- SFP+ connector
- Two SPI Flash devices

The PolarFire Evaluation Board has 14 layers and it is manufactured using NElco-SI material for top and bottom layers, and FR4 dielectric material for inner layers.

The following labeled image highlights various components of the PolarFire Evaluation Board.

Figure 2 • **PolarFire Evaluation Board**



The following table lists the important components of the PolarFire Evaluation Board:

Table 2 • **PolarFire Evaluation Board Components**

Component	Label on Board	Description
Featured Device		
PolarFire FPGA	—	MPF300TS-1FCG1152I FPGA with data security feature
Power Supply and Monitoring		
12 V power supply input	J9	The board is powered by a 12 V power source using an external +12 V/5 A DC jack
ON/OFF switch	SW3	Power ON/OFF switch from +12 V external DC jack
Power Monitoring FPGA	U27	Microchip SmartFusion FPGA (A2F200M3F-1FGG256I) used for power sequence and monitoring the voltage rails on the PolarFire Evaluation Board
Clocks		
On-board 50 MHz clock oscillator	Y9	50 MHz clock oscillator with single-ended output
XCVR reference clock connectors	J40 and J44	SMA connectors (used by external clock source)
OSC	Y6	122.88 MHz oscillator (differential LVDS output) is the input to the DS08MB200TSQ clock MUX buffer
OSC	Y4	125 MHz oscillator (differential LVDS output) is the input to the DS08MB200TSQ clock MUX buffer
OSC	Y5	156.25 MHz oscillator (differential LVDS output) provides the REFCLK to XCVRs connected to the PolarFire device pins AC27 and AC28
Clock Network synchronous chip	U16	ZL30364GDG2 IEEE 1588 & Synchronous Ethernet Packet Clock Network Synchronizer that provides the clock to VSC8575 and the PolarFire device
Clock MUX\Buffer	U58	DS08MB200TSQ_NOPB (differential LVDS output) provides the REFCLK to XCVRs connected to PolarFire device pins AE27 and AE28
FPGA Programming and Debugging		
USB - UART terminal	J5	FTDI programmer interface to program the external SPI flash and the PolarFire device The J5 cable powers up the SmartFusion and the FTDI device that are required for power monitoring. The J5 and J9 cables must be connected to power up the board.
SPI flash	U44 and U45	Two 1 Gb SPI flash Micron MT25QL01GBBB8ESF-0SIT connected to SPI pins on bank 3 and bank 6 of the PolarFire device
FT4232H	U29	USB-to-quad serial ports in various configurations
JTAG programming header	J32	This header is used to program and debug the PolarFire device using FlashPro4 or FlashPro5. In the FlashPro software, the appropriate programmer (FlashPro4 or FlashPro5) must be selected.
Communication Interfaces		

Table 2 • **PolarFire Evaluation Board Components *(continued)***

Component	Label on Board	Description
x4 PCIe edge connector	—	PCIe edge connector with four lanes
Tx/Rx XCVR2 SMA pairs	J41 J42 J37 J38	XCVR0 TXD0P XCVR0 TXD0N XCVR0 RXD0P XCVR0 RXD0N
Two 10/100/1000 Ethernet RJ45 connectors	J15 and J30	Ethernet (RJ45) jacks with external magnetics interfacing with Microchip quad 10/100/1000 BASE-T PHY chip and 1588 timing feature in SGMII mode. VSC8575 interfaces with the Ethernet ports of the PolarFire device
FMC HPC connector	J34	FMC connector with eight XCVR lanes and 80 Differential pairs (HPC[HB0:21], HPC[HA0:23] and LPC[0:33])
SFP+ connector	J36	SFP connector of one XCVR lane to support the optical interface with an external interface
Memory Chips		
DDR3L Memory	U18 and U19	Two 4 Gb (MT41K512M8DA-107:P- 64 Meg x 8 x 8) chips are connected in Fly-by topology with a 16-bit data bus for storing data bits For more information, download the datasheet from https://in.micron.com/products/dram/ddr3-sdram/part-catalog/mt41k512m8da-107
DDR4 Memory	U36, U42, U47, and U48	Four 8 Gb (MT40A1G8WE-083E:B- 1G Meg × 8) chips are connected in Fly-by topology with a 32-bit data bus for storing data bits For more information, download the datasheet from https://www.micron.com/parts/dram/ddr4-sdram/mt40a1g8we-083e?pc={0759757A-85DB-4AD3-9B4D-B7E7DDE8A22D}
General Purpose I/O		
Switches	SW7, SW8, SW9, and SW10	Push-button switches for user-interface debugging applications
DIP Switches	SW11	Eight DIP switches for testing
Light-emitting diodes (LEDs)	—	Eight active-high LEDs connected to some of the user I/Os for debugging, and twelve active high LEDs used for indicating power supply
Reset switch	SW6	Push-button system reset for the PolarFire device Users must program this GPIO for PolarFire device reset function

2.5 Compatibility With Daughter Boards

Daughter boards with FMC connectors can be plugged into the PolarFire Evaluation board.

2.6 Handling the Board

Pay attention to the following points while handling or operating the board to avoid possible damage or malfunction:

- Handle the board with electrostatic discharge (ESD) precautions to avoid damage. For information about using the board with ESD precautions, see https://www.microsemi.com/document-portal/doc_view/126483-esd-appnote.
- Power down the board to switch between Programming headers J32, J29, PCIe CONN (CON3), SFP+ cage (J36), and GPIO headers (J7, J8).

2.7 Powering Up the Board

The PolarFire Evaluation Board is powered up using either the 12 V DC jack or the PCIe connector.

To power up the board, connect the 12 V DC jack to the board, and connect the J5 USB port to the host PC.

Note: If the J5 USB port is not connected to the Host, the board will not power up even if the 12 V supply is on.

The PolarFire Evaluation Board ships with a pre-programmed bring-up design (LED toggling). Install the software required for developing designs and set the jumpers for the pre-programmed design. For more information, see Installation and Settings, page 8.

3 Installation and Settings

This section provides information about the software and hardware settings required to run the pre-programmed demo design on the PolarFire Evaluation Board.

3.1 Software Settings

Download and install the latest release of Microchip Libero® SoC PolarFire from the Microchip website, and register for a Silver license. The Libero SoC PolarFire installer includes FlashPro5 drivers.

For instructions about installing Libero SoC PolarFire and SoftConsole, see the *Libero Software Installation and Licensing Guide*.

For instructions about how to download and install Microchip DirectCores and driver firmware cores on the PC where Libero SoC is installed, see the *Installing IP Cores and Drivers User's Guide*.

3.2 Hardware Settings

This section provides information about jumper settings, switches, LEDs, and DIP switches on the PolarFire Evaluation Board.

3.2.1 Jumper Settings

Connect the jumpers according to the settings specified in the following table.

Table 3 • **Jumper Settings**

Jumper	Description	Pin	Default Setting
J18, J19, J20, J21, J22	Jumpers to select the PolarFire JTAG or A2F JTAG	Close pin 1 and 2 for programming the power sequence and monitoring chip through the FTDI	Open
		Close pin 2 and 3 for programming the PolarFire FPGA through FTDI User must always retain the default jumper setting	Closed
J46	Jumper to select switch-side MUX inputs of A or B to the line side	Close pin 1 and 2 (Input A to the line side) for routing the on-board 122.88 MHz differential clock oscillator output to the line side	Open
		Close pin 1 and 2 (Input B to the line side) for routing the on-board 125 MHz differential clock oscillator output to the line side	Closed
J28	Jumper to select the external JTAG or the on-board FlashPro5 for programming the PolarFire device	Close pin 1 and 2 for programming through the on-board FlashPro5	Closed
J26	Jumper to select the FTDI SPI or SC_SPI header	Close pin 1 and 2 for programming through the SC_SPI Header	Open

Table 3 • Jumper Settings (continued)

Jumper	Description	Pin	Default Setting
J27	Jumper to select between FTDI SPI or External SPI Flash to program the device	Close pin 1 and 2 for programming through the External SPI flash	Open
J23	Jumper to define the SPI interface mode	Close pin 1 and 2 to define the SPI Slave mode	Open
J4	Jumper to select the SW3 input or the ENABLE_FT4232 signal from the FT4232H chip	Close pin 1 and 2 for manual power switching using SW3 Close pin 2 and 3 for remote power switching using the GPIO capability of the FT4232 chip	Closed Open
J12	Jumper to select the PolarFire VCCIO voltage (VCCIO_HPC_VADJ) to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V	Close pin 1 and 2 for 3.3 V Close pin 3 and 4 for 2.5 V Close pin 5 and 6 for 1.8 V Close pin 7 and 8 for 1.5 V Close pin 9 and 10 for 1.2 V	Open Closed Open Open Open
J43	Jumper to select the VDD voltage	close Pin 1 and 2 for 1.05V	Open

For locations of various jumpers and test points on the PolarFire Evaluation Board, see Figure 18, page 33.

3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs.

Table 4 • LEDs

LED	Description
DS3 - Green	1 V Voltage rail
DS4 - Green	1.5 V Voltage rail
DS5 - Green	0.75 V Voltage rail
DS6 - Green	1.2 V Voltage rail
DS7 - Green	0.6 V Voltage rail
DS8 - Green	1.8 V Voltage rail
DS9 - Green	1.0 V Voltage rail for VSC8575
DS10 - Green	1.0 V Voltage rail for VDDA
DS11 - Green	VDDAUX_GPIO Voltage rail
DS12 - Green	2.5 V Voltage rail

Table 4 • **LEDs *(continued)***

LED	Description
DS13- Green	VCCIO_HPC_VADJ voltage
DS14 - Green	VDDAUX Voltage rail
DS18 - Green	12 V voltage rail
DS16 - Green	5 V voltage rail
DS17 - Green	3.3 V voltage rail

3.2.3 Test Points

The following table lists USB, ground, and other test points.

Table 5 • **Test Points**

Test Point	Description
TP12	Test point to probe the voltage of 1P8V_ZL
TP18	Test point to probe 5 V voltage
TP12	Test point to probe 3.3 V voltage
TP126	Test point to probe 1 V voltage
TP22	Test point to probe 1.5 V voltage for DDR3L
TP8	Test point to probe 0.75 V
TP12	1.5V current-sensing test point
TP115	Test point to probe 1.2 V voltage for DDR4
TP109	Test point to probe 0.6 V voltage
TP124	Test point to probe 1.8 V voltage
TP23	Test point to probe 1 V voltage of VSC8575 PHY
TP123	Test point to probe 1.0 V (VDDA)
TP30	Test point to probe VDDAUX voltage
TP16	Test point to probe IO voltage
TP33	Test point to probe AUX voltage
TP118, 130,15,119,129,29,121,128,19,3	Ground

3.3 Power Sources

The PolarFire Evaluation Board uses Microchip power supply devices. For more information about power supply devices, see https://www.microchip.com/en-us/products/power-management.

The following table lists the key power supplies required for normal operation of the PolarFire Evaluation Board.

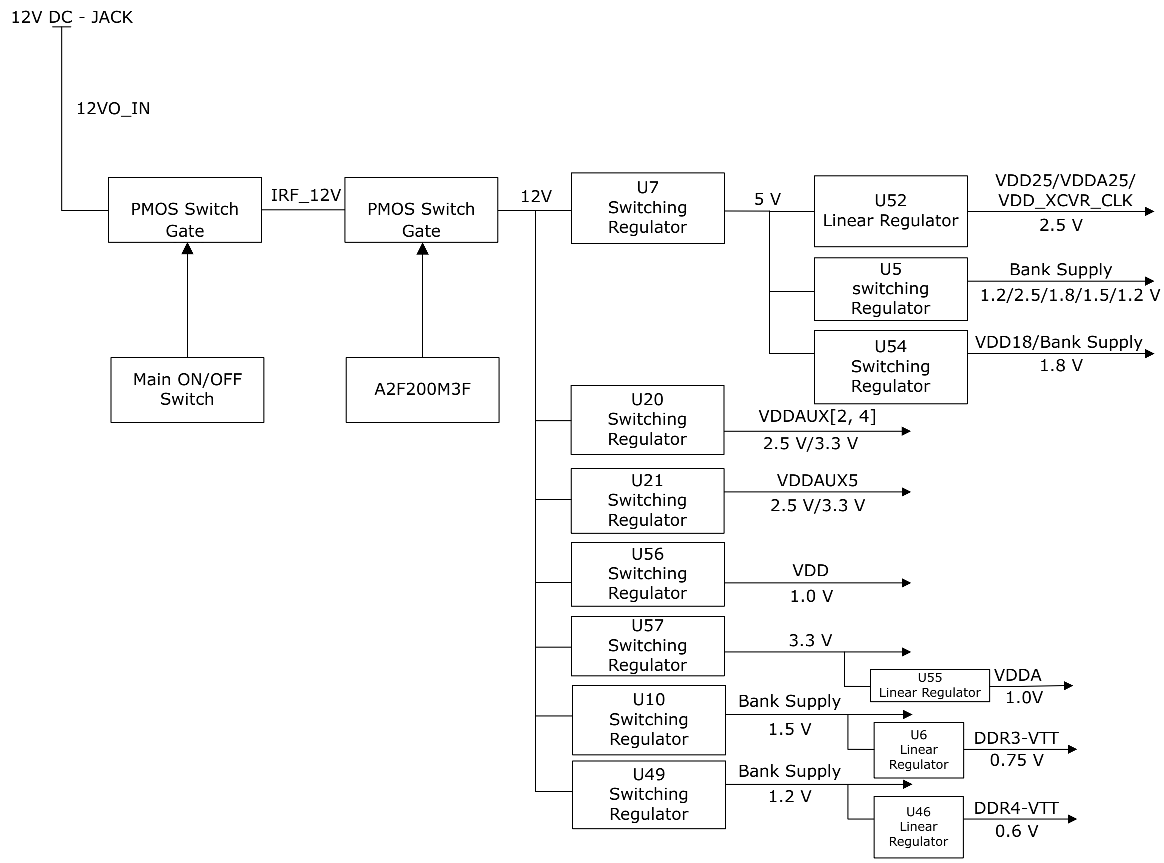
Table 6 • **I/O Voltage Rails**

PolarFire Bank	I/O Rail	Voltage
Bank 0	1P5V_REG	1.2 V
Bank 1	1P2V_REG	1.5 V
Bank 2	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank 3	3P3V	3.3 V
Bank 4	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank 5	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank 6	1P8V	1.8V
Bank 7	1P2V_REG	1.2V VDD_XCVR_CLK VDD25_DUT 2P5V

Note: The Bank 3 voltage is set to 3.3 V for Rev B boards, this voltage has been updated in Rev C boards to 2.5 V. Designers may use any voltage for VDDI3 as per the datasheet for building their own boards.

The following figure shows voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.0 V) available on the PolarFire Evaluation Board.

Figure 3 • **Voltage Rails in PolarFire Evaluation Board**



The following table lists the suggested Microchip power regulators for PolarFire FPGA voltage rails.

Table 7 • **Power Regulators**[1]

Voltage rail	Part Number	Description	Current
5V	MIC24055YJL-TR	IC REG BUCK ADJ 12A SYNC 28QFN	12A
VDD (1.0V)	MIC45212-2YMP-T1	DC DC CONVERTER 0.8-5.5V 77W	14 A
VDDIO (3.3V)	MIC24055YJL-TR	IC REG BUCK ADJ 12A SYNC 28QFN	12 A
VCCIO_HPC_VADJ	MIC24046YFL-TR	IC REG BUCK PROG 5A SYNC 20VQFN	5 A
DDR4 (1.2V)	MIC23303YML-T5	IC REG BUCK ADJ 3A SYNC 12DFN	3 A
DDR3L (1.5V)	MIC23303YML-T5	IC REG BUCK ADJ 3A SYNC 12DFN	3 A
VDDAUX[2,4]	MIC23303YML-T5	IC REG BUCK ADJ 3A SYNC 12DFN	3 A
VDDAUX5	MIC23303YML-T5	IC REG BUCK ADJ 3A SYNC 12DFN	3 A
VTT_DDR4 (0.6V)	MIC5166YML-TR	IC PWR SUP 3A HS DDR TERM 10MLF	3 A
VTT_DDR3L (0.75V)	MIC5166YML-TR	IC PWR SUP 3A HS DDR TERM 10MLF	3 A
VDDIO (1.8V)	MIC24046YFL-TR	IC REG BUCK PROG 5A SYNC 20VQFN	5 A
3V3_F2	MCP1726T-ADJE/MF	IC REG LINEAR POS ADJ 1A 8DFN	1 A
1V5_F2	MCP1726T-ADJE/MF	IC REG LINEAR POS ADJ 1A 8DFN	1 A
VDDA (1.0V)	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5 A

Table 7 • **Power Regulators[1] *(continued)***

Voltage rail	Part Number	Description	Current
VDD25, VDDA25, VDD_XCVR_CLK	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5 A
VDD18	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5 A

1. These regulators are not pin compatible with the existing evaluation kit schematics. Use these regulators for new board designs.

4 Board Components and Operations

This section describes the key components of the PolarFire Evaluation board and important board operations. For device datasheets, visit https://www.microchip.com/en-us/development-tool/MPF300-EVAL-KIT.

4.1 Memory Interface

GPIO and HSIO bank I/Os for DDR3L and DDR4 are available in the PolarFire device. In addition to dedicated I/Os, regular I/Os can also be used to connect to other memory devices.

Note: DQ swapping within the byte lane is executed on this PCB between the logical pin of the DDR controller, as defined in the device/package PPAT tables, and the physical pin of the memory device.

4.1.1 DDR3L

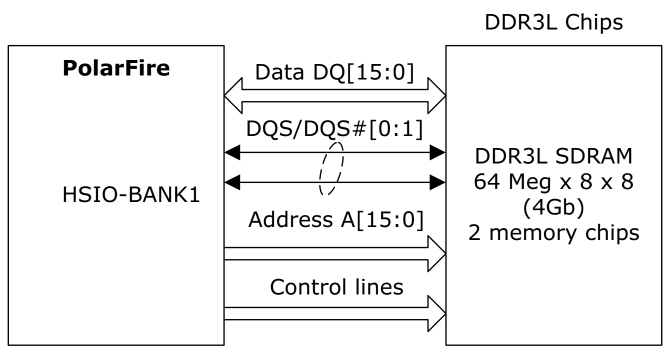
Two 4 Gb DDR3L SDRAM chips are provided to serve as flexible volatile memory for user applications. The DDR3L interface is implemented in HSIO bank 1.

The DDR3L SDRAM specifications for the PolarFire device are:

- MT41K512M8DA-107:P- 64 Meg x 8 x 8
  - Two chips are connected in Fly-by topology
- Density: 16 Gb
- Data rate: DDR3L 16-bit at 166 MHz clock rate

The PolarFire Evaluation Board design uses the DDR3L and SSTL15 standards for the DDR3L interface. The default board assembly available for the DDR3L standard has RC terminations.

Figure 4 • **DDR3L Memory Interface**



For more information, see the Board-Level Schematics document (provided separately).

4.1.2 DDR4

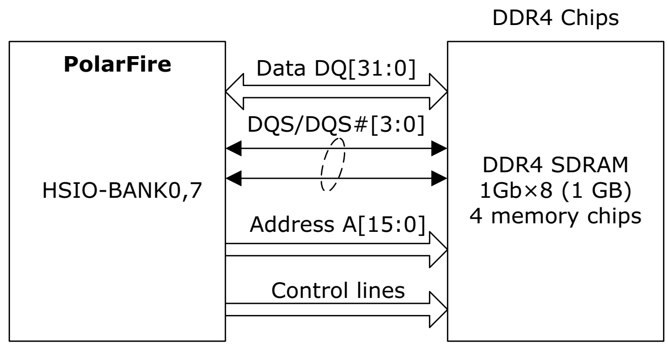
Four 8 Gb DDR4 SDRAM chips are provided to serve as flexible volatile memory for user applications. The DDR4 interface is implemented in HSIO bank 0 and Bank 7.

The DDR4 SDRAM specifications for the PolarFire device are:

- MT40A1G8WE-083E:B
  - Quantity: Four chips are connected in Fly-by topology
- Density: 32 Gb
- Data rate: DDR4 32-bit at 166 MHz clock rate

The PolarFire Evaluation Board design uses the DDR4 and POD12 standards for the DDR4 interface. The default board assembly available for the DDR4 standard has RC terminations.

Figure 5 • **DDR4 Memory Interface**



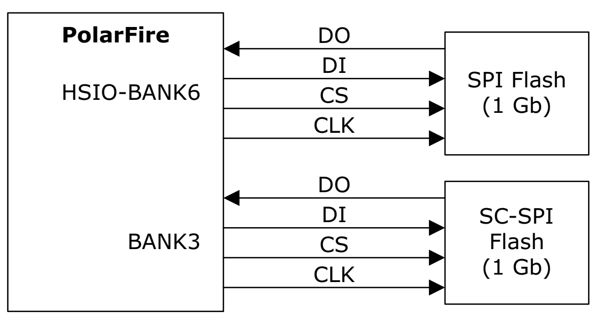
For more information, see the Board Level Schematics document (provided separately).

4.2 SPI Serial Flash

The SPI flash specifications for the PolarFire device are:

- Density: 1 Gb
- Voltage: 2.7 V to 3.6 V (MT25QL01GBBB8ESF-0SIT)
- Voltage: 1.7 V to 2 V (MT25QU01GBBB8ESF-0SIT)
- Frequency: 90 MHz
- Quantity = 2
- SPI mode support: Modes 0 and 3
- HSIO bank 6 and Dedicated Bank 3

Figure 6 • **SPI Flash Interface**



For more information, see the Board Level Schematics document (provided separately).

4.3 Transceivers

The PolarFire MPF300TS-1FCG1152I device has 16 transceiver lanes. These transceiver lanes can be accessed through the PCIe edge, SFP+, SMA, and FMC connectors on the board. For information about transceiver protocols, see *PolarFire Family Transceiver User Guide*.

4.3.1 XCVR0 Interface

The XCVR0 interface has four lanes connected as follows:

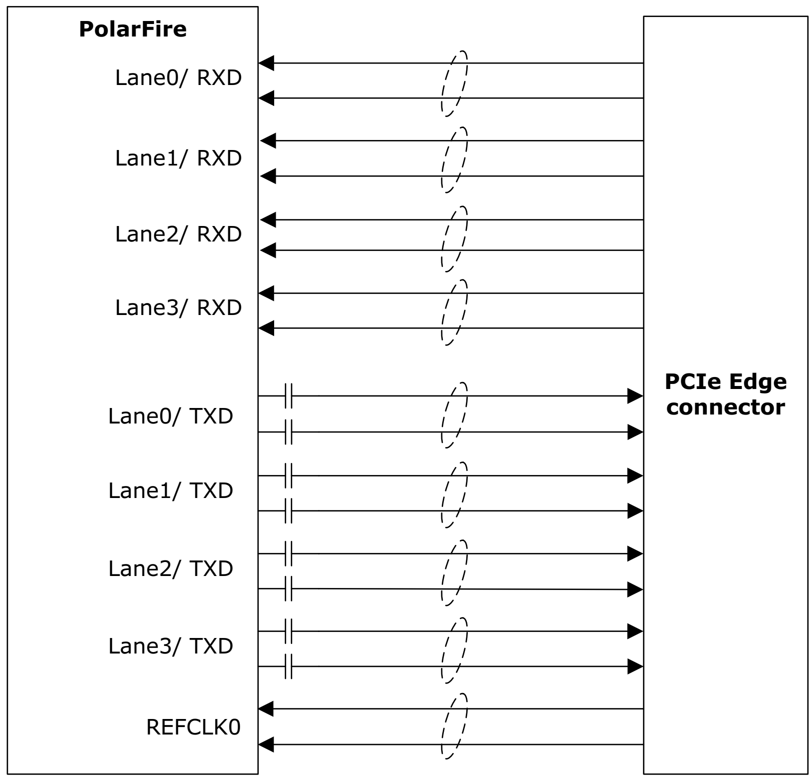
- Lanes 0, 1, 2, and 3 are directly routed to the PCIe connector
  - TX pad > trace > AC coupling > trace > via (to bottom layer) > trace > PCIe connector pad
  - RX pad > trace > via (to Top layer) > trace > PolarFire device pad

The XCVR0 reference clock is routed directly from the PCIe connector to the PolarFire device.

The XCVR0 TXD pairs are capacitively coupled to the PolarFire device. Serial AC-coupling capacitors are used to provide common-mode voltage independence.

The following figure shows the XCVR0 interface of the PolarFire Evaluation Board.

Figure 7 • **XCVR0 Interface**



For information about PCI Express support in PolarFire, see *PolarFire Family PCI Express User Guide*.

4.3.2 XCVR1 and XCVR3 Interface

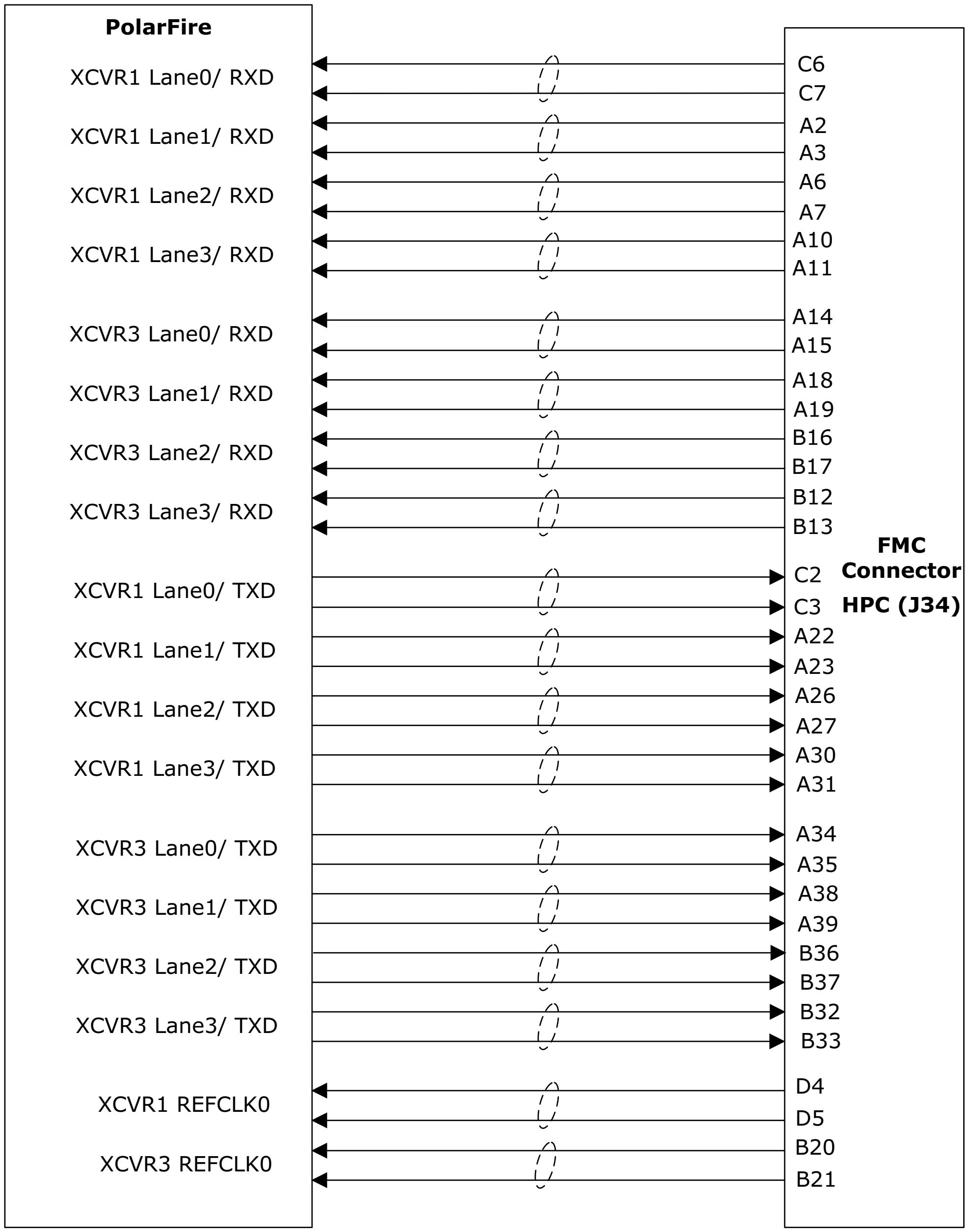
The XCVR1 and XCVR3 interfaces have four lanes each, that are connected to FMC HPC connector and the signals are routed in the PCB as follows:

- Lanes 0 to 7 are directly routed to the FMC HPC connector.
  - TX pad > trace > via (to bottom layer) > trace > FMC HPC connector pad
  - RX pad > trace > via (to Top layer) > trace > PolarFire device pad

The XCVR1 and XCVR3 reference clock is routed directly from the HPC connector to the PolarFire device.

The following figure shows the XCVR1 and 3 interface of the PolarFire Evaluation Board.

Figure 8 • **XCVR1 and XCVR3 Interface**



4.3.3 XCVR2 Interface

The XCVR2 interface has four lanes connected as follows:

- Lane 0 is connected to SMA connectors.
  - TX pad > trace > AC coupling > trace > SMA connectors (J41 (P) and J42 (N))
  - RX pad > trace > via (to Top layer) > trace > SMA connectors (J37 (P) and J38 (N))
- Lane 1 is connected to the SFP+ connector.
  - TX pad > bottom trace > via (to Top layer) > SFP+ connector
  - RX pad > bottom trace > via (to Top layer) > SFP+ connector
- Lanes 2 and 3 are used for loopback testing. This path is routed between the TX and RX pads with trace and two vias.
  - TX pad > via (to bottom layer) > trace > AC coupling > trace > via (to top layer and Inner layer) > RX pad.

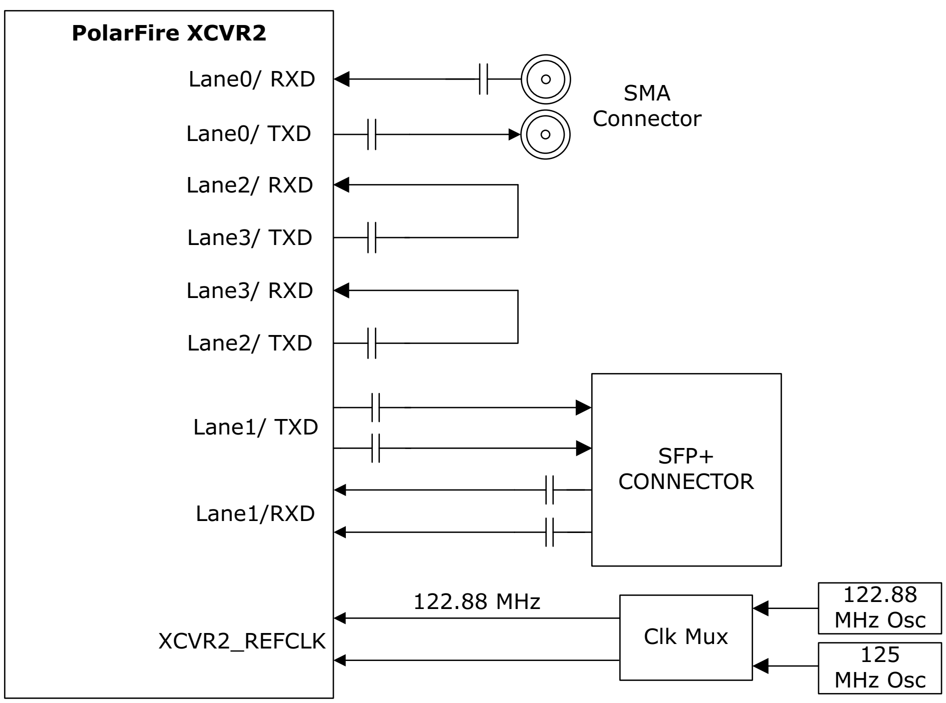
The XCVR2 reference clock is routed from the on-board LVDS MUX chip and the default setting is 122.8 MHz and 125 MHz clock is routed to MUX chip.

The expected Clock Mux outputs are as follows:

- Voltage level: 3.3 (± 0.3) V
- Differential LVDS
- Symmetry: 50% (± 10%)
- Differential output voltage: 250 mV minimum, 350 mV Typical, 500 mV maximum

The following figure shows the XCVR2 interface of the PolarFire Evaluation Board.

Figure 9 • **XCVR2 Interface**



For information about the J46 jumper, see Table 3, page 8.

For more information, see the Board-Level Schematics document (provided separately).

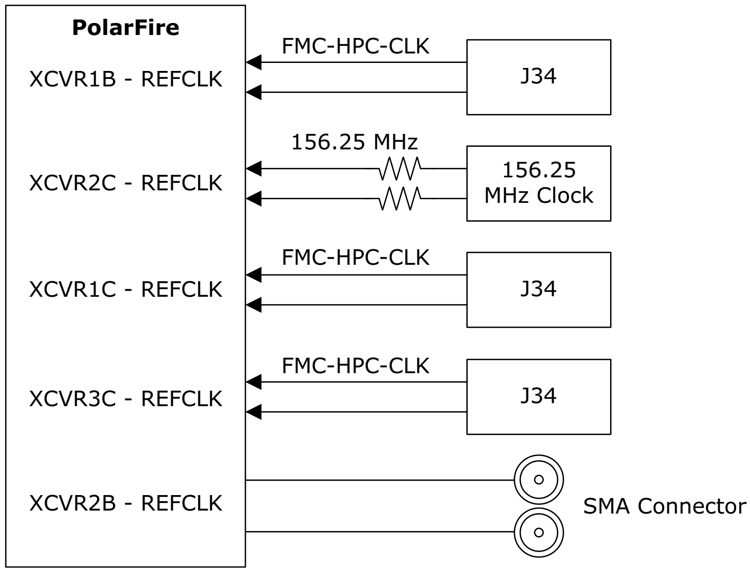
4.3.4 XCVR Reference Clocks

The XCVR supports the reference clocks connected as follows:

- XCVR 1B,1C, and 3C Reference clocks are connected to FMC HPC connector
- XCVR 2B Reference clock is connected to external SMA connector(J40 and J44)
- XCVR 2C Reference clock is connected on board 156.25 MHz oscillator

The following figure shows the XCVR reference clocks are interface of the PolarFire Evaluation Board.

Figure 10 • **XCVR Reference Clocks**



For more information, see the Board Level Schematics document (provided separately).

4.4 Microchip PHY (VSC8575)

The PolarFire Evaluation Board uses Microchip physical layer (PHY) device VSC8575 for Ethernet communications at 10/100/1000 Mbps. Device VSC8575 has four independent gigabit Ethernet transceivers; however, the board uses only two of the transceivers. Each transceiver performs all the PHY functions for 10BASE-T, 100BASE-TX, and 1000BASE-T full-duplex or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with external magnetics. The VSC8575 device supports Quad SGMII for direct connection to a PolarFire chip. The registers are configured through SPI interface, MDC\MDIO and JTAG. Device VSC8575 supports the IEEE 1588v2 timing implementation. The ZL30364GDG2 chip provides the 125 MHz clock and reserved clocks to VSC8575 PHY. Device ZL30364GDG2 is configurable through the SPI interface and connected to PolarFire device.

The key features of Microchip PHY VSC8575 are:

- Low Power
- IEEE 1588v2
- Wide range of support (SGMII,QSGMII)

4.4.1 Microchip 1588v2 (ZL30364GDG2)

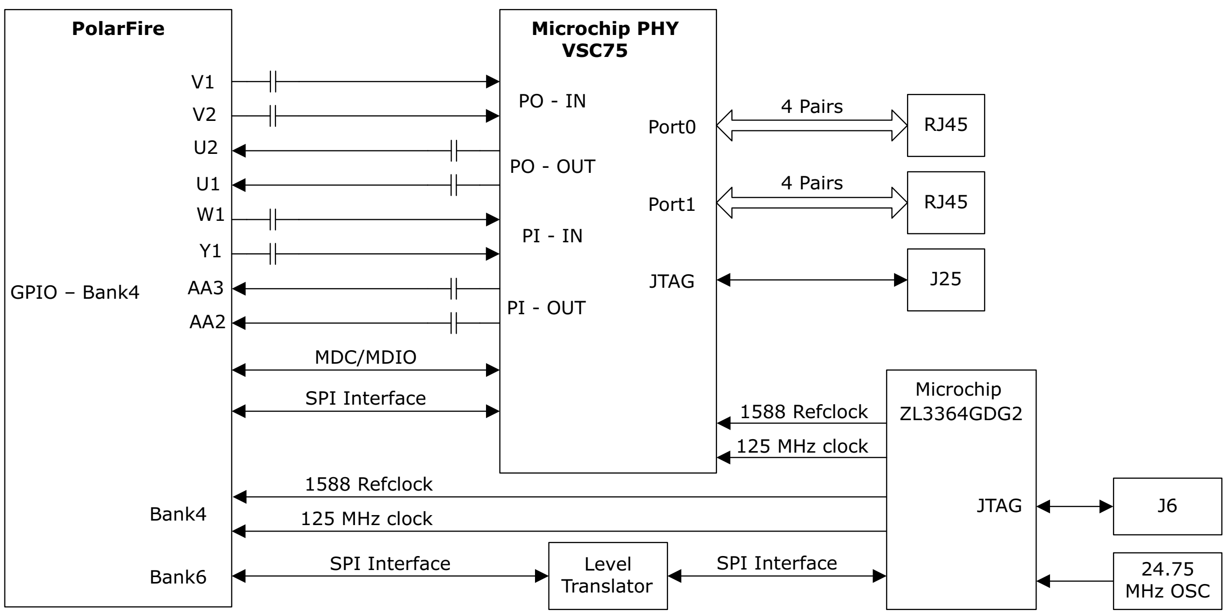
The PolarFire Evaluation Board uses Microchip ZL30364GDG2 to provide the 125 MHz clock and reserved clocks to VSC8575 PHY. Device ZL30364GDG2 is configurable through the SPI interface and connected to the PolarFire device. The ZL30364GDG2 clock outputs are LVPECL and LVCMOS.

Key features of Microchip PHY ZL30364GDG2 are as follows:

- XOin: XO master clock output (24.576 MHz)
- HPDIFF: High Performance differential output clocks (LVPECL) specifications:
  - Voltage level: 3.3 V
- Differential output voltages, minimum 380 mV and maximum is 940 mV
- Rise or fall time: Maximum 1 ns at the rate of 20% to 80% of the supply (3.3 V)
- Output voltage levels:
  - High (minimum = 2.14 V and maximum = 2.42 V)
  - Low (minimum = 1.49 V and maximum = 1.75 V)
- Input voltages:
- Differential input common mode voltage minimum is 1.1 V and maximum is 2 V
- Differential input voltage difference minimum is 250 mV and maximum is 1 V

The following figure shows the PolarFire-Microchip PHY interface.

Figure 11 • **PHY Interface**



4.5 Power Monitoring

The PolarFire Evaluation Board uses the Microchip A2F200M3F-1FGG256I device to monitor the voltage rails. The A2F200M3F-1FGG256I device is programmed through the FTDI interface and it supports the UART interface. The A2F200M3F-1FGG256I device needs an external 20 MHz crystal frequency.

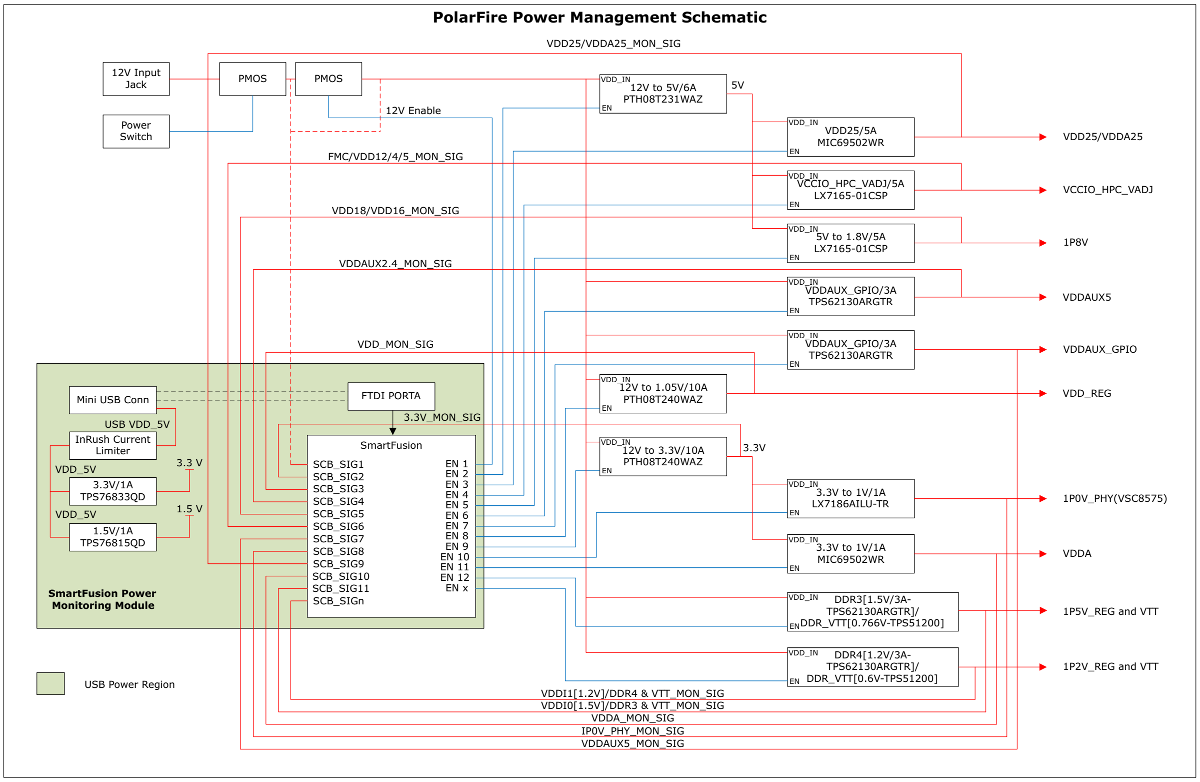
Key features of Microchip A2F200M3F-1FGG256I are:

- Microcontroller Subsystem (MSS)
- Analog Compute Engine (ACE)
- Programmable Analog Front-End (AFE)

For more information on how to monitor power on the board, see Appendix 3: Power Monitoring, page 36.

The following figure shows the Microchip PolarFire Power measurement system on the PolarFire Evaluation Board.

Figure 12 • **Power Management**



4.6 Programming

The PolarFire device is programmed using the on-board FlashPro5 programmer. For more information about programming the PolarFire device, see Appendix 2: Programming PolarFire FPGA Using the On-Board FlashPro5, page 35 and *PolarFire and PolarFire SoC FPGA Programming User Guide*.

For more information, see PolarFire Evaluation Kit Schematics.

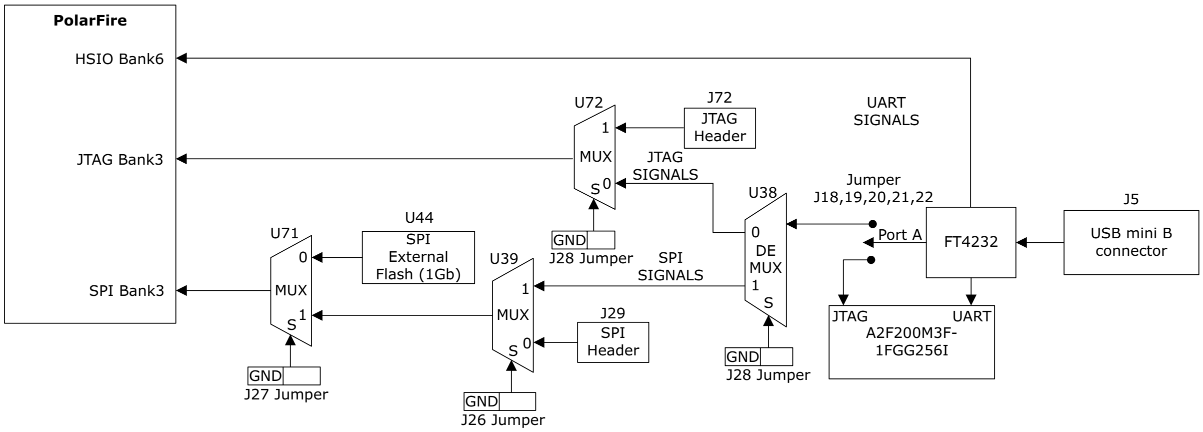
4.6.1 FTDI

The key features of the FT4232H chip are:

- USB 2.0 high-speed (480 Mbps) to UART/MPSSE IC
- Single-chip USB-to-quad serial ports in various configurations
- Entire USB protocol handled on the chip without requiring USB-specific firmware programming
- USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) compatibility
- Two multi-protocol synchronous serial engines (MPSSE) on channel A and channel B to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design
- FTDI chip requires 1.8 V chip core voltage and +3.3 V I/O voltage

The following figure shows the FTDI interface of the PolarFire Evaluation Board.

Figure 13 • **FTDI Interface**



4.7 System Reset

DEVRST_N is an input-only reset pad that allows assertion of a full reset of the chip at any time. The DEVRST_N signal (active-low) is asserted in the following cases:

Information to be added.

4.8 50 MHz Oscillator

A 50 MHz clock oscillator with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip PolarFire PLL can be configured to generate a wide range of high-precision clock frequencies.

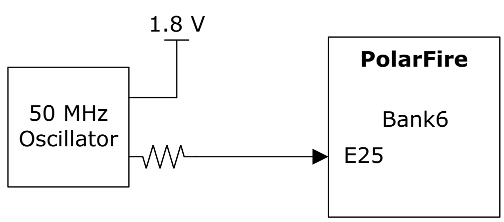
The package and pin details of the 50 MHz oscillator are:

Pin Number: E25

Pin Name: HSIO63PB6/CLKIN_S_12/CCC_SE_CLKIN_S_12/CCC_SE_PLL0_OUT0

The following figure shows the 50 MHz clock oscillator interface.

Figure 14 • **50 MHz Clock Oscillator**



For more information, see the Board-Level Schematics document (provided separately).

4.9 User Interface

The PolarFire Evaluation Board has user LEDs as well as push-button switches.

4.9.1 User LEDs

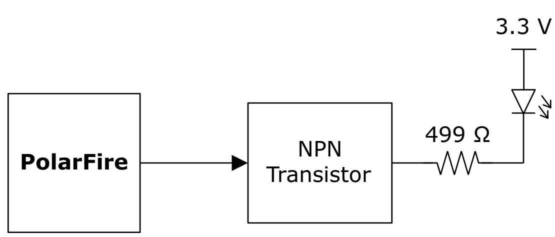
The board has eight active-High LEDs that are connected to the PolarFire device. The following table lists the on-board user LEDs.

Table 8 • **User LEDs**

PolarFire Evaluation Board Pin	PolarFire FPGA Pin Number	PolarFire FPGA Pin Name	Bank
LED7	D25	HSIO70PB6/CCC_SE_PLL1_OUT1	Bank - 6
LED6	C26	HSIO70NB6	Bank - 6
LED5	B26	HSIO71NB6	Bank - 6
LED4	F22	HSIO64NB6	Bank - 6
LED11	H21	HSIO36NB6	Bank - 6
LED10	H22	HSIO60NB6	Bank - 6
LED9	F23	HSIO62PB6/DQS/CCC_SE_PLL0_OUT0	Bank - 6
LED8	C27	HSIO71PB6/CCC_SE_CLKIN_S_15	Bank - 6

The following figure shows the LED interface of the PolarFire Evaluation Board.

Figure 15 • **LED Interface**



For more information, see the Board-Level Schematics document (provided separately).

4.9.2 Push-Button Switches

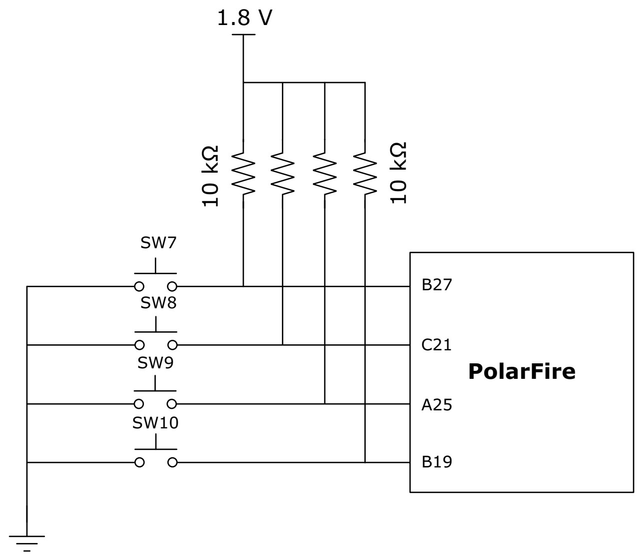
The PolarFire Evaluation Board comes with four push-button tactile switches that are connected to the PolarFire device. The following table lists the on-board push-button switches.

Table 9 • **Push-Button Switches**

PolarFire Evaluation Board Pin	PolarFire FPGA Pin Number	PolarFire FPGA Pin Name	Bank
SW10	B19	HSIO46PB6	Bank - 6
SW8	C21	HSIO49PB6	Bank - 6
SW9	A25	HSIO68PB6/DQS/CCC_SE_PLL1_OUT0	Bank - 6
SW7	B27	HSIO69NB6	Bank - 6

The following figure shows the switches interface of the PolarFire Evaluation Board.

Figure 16 • **Switches Interface**



4.9.3 Slide Switches (DPDT)

The SW3 slide switch powers the device ON or OFF from +12 V external DC jack.

4.9.4 DIP Switches (SPST)

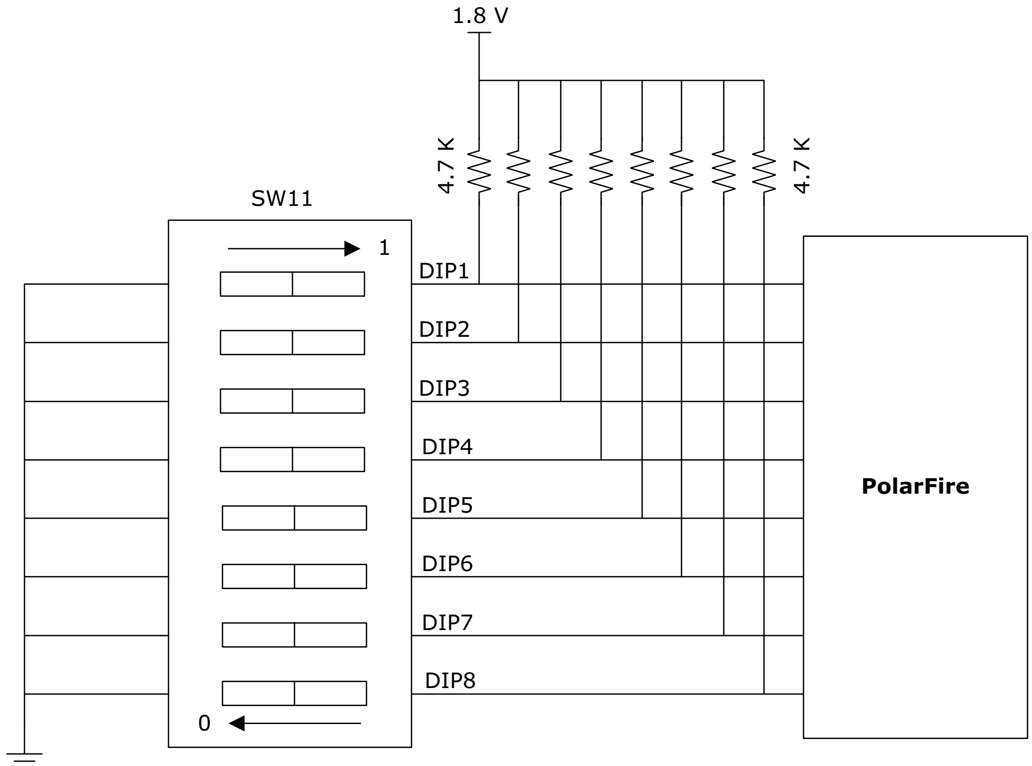
The SW11 DIP switch has eight connections to the PolarFire device. The following table lists the on-board DIP switches.

Table 10 • **DIP Switches**

PolarFire Evaluation Board Pin	PolarFire FPGA Pin Number	PolarFire FPGA Pin Name	Bank
DIP1	H23	HSIO60PB6	Bank - 6
DIP2	D21	HSIO48NB6	Bank - 6
DIP3	H24	HSIO61NB6	Bank - 6
DIP4	C22	HSIO50PB6/DQS	Bank - 6
DIP5	B21	HSIO49NB6	Bank - 6
DIP6	G20	HSIO41PB6	Bank - 6
DIP7	F24	HSIO62NB6/DQS	Bank - 6
DIP8	F25	HSIO63NB6	Bank - 6

The following figure shows the SPST interface on the PolarFire Evaluation Board.

Figure 17 • **SPST Interface**



For more information, see the Board-Level Schematics document (provided separately).

4.9.5 FMC HPC Connector

The PolarFire Evaluation Board has one HPC (J34) FMC connector for the daughter cards for future expansion of interfaces. This FMC connector is compliant with VITA 57.1 specification.

4.9.6 FMC Connector - HPC (J34)

The PolarFire GPIO, XCVR1, and XCVR3 signals are routed to the FMC connector (J34) for application development.

The following table provides the J34 FMC pinout details.

Table 11 • **J34 FMC Connector Pinout**

FMC Pin Number-J34	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
A2	HPC_SERDES_1_RX1_P	P29	XCVR_1_RX1_P
A3	HPC_SERDES_1_RX1_N	P30	XCVR_1_RX1_N
A6	HPC_SERDES_1_RX2_P	R31	XCVR_1_RX2_P
A7	HPC_SERDES_1_RX2_N	R32	XCVR_1_RX2_N
A10	HPC_SERDES_1_RX3_P	T29	XCVR_1_RX3_P
A11	HPC_SERDES_1_RX3_N	T30	XCVR_1_RX3_N
A14	HPC_SERDES_3_RX0_P	G31	XCVR_3_RX0_P
A15	HPC_SERDES_3_RX0_N	G32	XCVR_3_RX0_N

Table 11 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
A18	HPC_SERDES_3_RX1_P	J31	XCVR_3_RX1_P
A19	HPC_SERDES_3_RX1_N	J32	XCVR_3_RX1_N
A22	HPC_SERDES_1_TX1_P	P33	XCVR_1_TX1_P
A23	HPC_SERDES_1_TX1_N	P34	XCVR_1_TX1_N
A26	HPC_SERDES_1_TX2_P	T33	XCVR_1_TX2_P
A27	HPC_SERDES_1_TX2_N	T34	XCVR_1_TX2_N
A30	HPC_SERDES_1_TX3_P	U31	XCVR_1_TX3_P
A31	HPC_SERDES_1_TX3_N	U32	XCVR_1_TX3_N
A34	HPC_SERDES_3_TX0_P	F33	XCVR_3_TX0_P
A35	HPC_SERDES_3_TX0_N	F34	XCVR_3_TX0_N
A38	HPC_SERDES_3_TX1_P	H33	XCVR_3_TX1_P
A39	HPC_SERDES_3_TX1_N	H34	XCVR_3_TX1_N
B1	HPC_CLK_DIR_B6	D19	HSIO42PB6
B4	HPC_DP9_M2C_P	L27	XCVR_1C_REFCLK_P
B5	HPC_DP9_M2C_N	L28	XCVR_1C_REFCLK_N
B8	HPC_DP8_M2C_P	R27	XCVR_1B_REFCLK_P
B9	HPC_DP8_M2C_N	R28	XCVR_1B_REFCLK_N
B12	HPC_SERDES_3_RX3_P	L31	XCVR_3_RX3_P
B13	HPC_SERDES_3_RX3_N	L32	XCVR_3_RX3_N
B16	HPC_SERDES_3_RX2_P	K29	XCVR_3_RX2_P
B17	HPC_SERDES_3_RX2_N	K30	XCVR_3_RX2_N
B20	HPC_SERDES_3_INT_REFCLK_P	J27	XCVR_3A_REFCLK_P
B21	HPC_SERDES_3_INT_REFCLK_N	J28	XCVR_3A_REFCLK_N
B28	HPC_DP8_C2M_P	H29	XCVR_3C_REFCLK_P
B29	HPC_DP8_C2M_N	H30	XCVR_3C_REFCLK_N
B32	HPC_SERDES_3_TX3_P	M33	XCVR_3_TX3_P
B33	HPC_SERDES_3_TX3_N	M34	XCVR_3_TX3_N
B36	HPC_SERDES_3_TX2_P	K33	XCVR_3_TX2_P
B37	HPC_SERDES_3_TX2_N	K34	XCVR_3_TX2_N
C2	HPC_SERDES_1_TX0_P	N31	XCVR_1_TX0_P
C3	HPC_SERDES_1_TX0_N	N32	XCVR_1_TX0_N
C6	HPC_SERDES_1_RX0_P	M29	XCVR_1_RX0_P
C7	HPC_SERDES_1_RX0_N	M30	XCVR_1_RX0_N
C10	HPC_LA06_P_B2	G15	GPIO5PB2
C11	HPC_LA06_N_B2	G16	GPIO5NB2
C14	HPC_LA10_P_B2	J16	GPIO31PB2
C15	HPC_LA10_N_B2	K16	GPIO31NB2

Table 11 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
C18	HPC_LA14_P_B2	F13	GPIO22PB2
C19	HPC_LA14_N_B2	E13	GPIO22NB2
C22	HPC_LA18_CC_P_B2	G5	GPIO11PB2/CLKIN_S_7
C23	HPC_LA18_CC_N_B2	F5	GPIO11NB2
C26	HPC_LA27_P_B2	E6	GPIO13PB2
C27	HPC_LA27_N_B2	D6	GPIO13NB2
C30	HPC_SCL_B4	V12	GPIO205PB4/DQS
C31	HPC_SDA_B4	V11	GPIO205NB4/DQS
D4	HPC_SERDES_1_INT_REFCLK_P	N27	XCVR_1A_REFCLK_P
D5	HPC_SERDES_1_INT_REFCLK_N	N28	XCVR_1A_REFCLK_N
D8	HPC_LA01_CC_P_B2	G9	GPIO6PB2/CLKIN_S_4
D9	HPC_LA01_CC_N_B2	F9	GPIO6NB2
D11	HPC_LA05_P_B2	F14	GPIO19PB2
D12	HPC_LA05_N_B2	F15	GPIO19NB2
D14	HPC_LA09_P_B2	L17	GPIO30PB2
D15	HPC_LA09_N_B2	M17	GPIO30NB2
D17	HPC_LA13_P_B2	H14	GPIO3PB2
D18	HPC_LA13_N_B2	G14	GPIO3NB2
D20	HPC_LA17_CC_P_B2	F8	GPIO9PB2/CLKIN_S_6
D21	HPC_LA17_CC_N_B2	F7	GPIO9NB2
D23	HPC_LA23_P_B2	C7	GPIO12PB2
D24	HPC_LA23_N_B2	B7	GPIO12NB2
D26	HPC_LA26_P_B2	G12	GPIO18PB2
D27	HPC_LA26_N_B2	G11	GPIO18NB2
D29	HPC_TCK		
D30	HPC_TDI		
D31	HPC_TDO		
D33	HPC_TMS		
D34	HPC_TRST_L		
E2	HPC_HA01_CC_P_B4	V3	GPIO208PB4
E3	HPC_HA01_CC_N_B4	V4	GPIO208NB4
E6	HPC_HA05_P_B4	AB12	GPIO187PB4/DQS
E7	HPC_HA05_N_B4	AA12	GPIO187NB4/DQS
E9	HPC_HA09_P_B4	T5	GPIO217PB4/DQS
E10	HPC_HA09_N_B4	T4	GPIO217NB4/DQS
E12	HPC_HA13_P_B4	AB5	GPIO182PB4
E13	HPC_HA13_N_B4	AC4	GPIO182NB4

Table 11 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
E15	HPC_HA16_P_B4	W8	GPIO199PB4/DQS
E16	HPC_HA16_N_B4	Y8	GPIO199NB4/DQS
E18	HPC_HA20_P_B4	W6	GPIO197PB4
E19	HPC_HA20_N_B4	Y6	GPIO197NB4
E21	HPC_HB03_P_B5	J6	GPIO235PB5/DQS
E22	HPC_HB03_N_B5	J5	GPIO235NB5/DQS
E24	HPC_HB05_P_B5	L8	GPIO236PB5
E25	HPC_HB05_N_B5	L7	GPIO236NB5
E27	HPC_HB09_P_B5	J8	GPIO237PB5
E28	HPC_HB09_N_B5	K8	GPIO237NB5
E30	HPC_HB13_P_B5	M2	GPIO221PB5
E31	HPC_HB13_N_B5	M1	GPIO221NB5
E33	HPC_HB19_P_B5	N8	GPIO231PB5
E34	HPC_HB19_N_B5	M7	GPIO231NB5
E36	HPC_HB21_P_B5	M6	GPIO234PB5
E37	HPC_HB21_N_B5	M5	GPIO234NB5
F1	HPC_PG_M2C_B6	C19	HSIO45NB6
F4	HPC_HA00_CC_P_B4	W5	GPIO195PB4
F5	HPC_HA00_CC_N_B4	Y5	GPIO195NB4
F7	HPC_HA04_P_B4	AB9	GPIO183PB4
F8	HPC_HA04_N_B4	AA8	GPIO183NB4
F10	HPC_HA08_P_B4	AB7	GPIO179PB4
F11	HPC_HA08_N_B4	AB6	GPIO179NB4
F13	HPC_HA12_P_B4	T7	GPIO218PB4
F14	HPC_HA12_N_B4	U7	GPIO218NB4
F16	HPC_HA15_P_B4	V8	GPIO198PB4
F17	HPC_HA15_N_B4	V7	GPIO198NB4
F19	HPC_HA19_P_B4	AB4	GPIO177PB4
F20	HPC_HA19_N_B4	AC3	GPIO177NB4
F22	HPC_HB02_P_B5	L4	GPIO225PB5
F23	HPC_HB02_N_B5	M4	GPIO225NB5
F25	HPC_HB04_P_B5	P9	GPIO230PB5
F26	HPC_HB04_N_B5	P8	GPIO230NB5
F28	HPC_HB08_P_B5	L3	GPIO223PB5/DQS
F29	HPC_HB08_N_B5	L2	GPIO223NB5/DQS
F31	HPC_HB12_P_B5	N4	GPIO224PB5
F32	HPC_HB12_N_B5	N3	GPIO224NB5

Table 11 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
F34	HPC_HB16_P_B5	K5	GPIO232PB5
F35	HPC_HB16_N_B5	L5	GPIO232NB5
F37	HPC_HB20_P_B5	N7	GPIO228PB5
F38	HPC_HB20_N_B5	N6	GPIO228NB5
G2	HPC_CLK1_M2C_P_B2	C11	GPIO29PB2/CLKIN_S_9/CCC_SE_CLKIN_S_9
G3	HPC_CLK1_M2C_N_B2	B11	GPIO29NB2
G6	HPC_LA00_CC_P_B2	H9	GPIO7PB2/CLKIN_S_5
G7	HPC_LA00_CC_N_B2	H8	GPIO7NB2
G9	HPC_LA03_P_B2	H16	GPIO32PB2/DQS
G10	HPC_LA03_N_B2	H17	GPIO32NB2/DQS
G12	HPC_LA08_P_B2	J14	GPIO2PB2/DQS
G13	HPC_LA08_N_B2	J13	GPIO2NB2/DQS
G15	HPC_LA12_P_B2	F12	GPIO23PB2
G16	HPC_LA12_N_B2	E12	GPIO23NB2
G18	HPC_LA16_P_B2	D10	GPIO26PB2/DQS
G19	HPC_LA16_N_B2	D11	GPIO26NB2/DQS
G21	HPC_LA20_P_B2	B9	GPIO25PB2
G22	HPC_LA20_N_B2	A9	GPIO25NB2
G24	HPC_LA22_P_B2	D8	GPIO14PB2/DQS
G25	HPC_LA22_N_B2	C8	GPIO14NB2/DQS
G27	HPC_LA25_P_B2	J11	GPIO4PB2
G28	HPC_LA25_N_B2	H11	GPIO4NB2
G30	HPC_LA29_P_B2	B10	GPIO28PB2
G31	HPC_LA29_N_B2	A10	GPIO28NB2
G33	HPC_LA31_P_B2	E7	GPIO15PB2
G34	HPC_LA31_N_B2	E8	GPIO15NB2
G36	HPC_LA33_P_B2	H7	GPIO8PB2/DQS
G37	HPC_LA33_N_B2	G7	GPIO8NB2/DQS
H2	HPC_PRSNT_M2CL_B6	D20	HSIO42NB6
H4	HPC_CLK0_M2C_P_B2	D13	GPIO27PB2/CLKIN_S_8/CCC_SE_CLKIN_S_8
H5	HPC_CLK0_M2C_N_B2	C12	GPIO27NB2
H7	HPC_LA02_P_B2	L19	GPIO34PB2
H8	HPC_LA02_N_B2	L18	GPIO34NB2
H10	HPC_LA04_P_B2	J18	GPIO33PB2/CCC_SE_CLKIN_S_10
H11	HPC_LA04_N_B2	J19	GPIO33NB2

Table 11 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
H13	HPC_LA07_P_B2	K15	GPIO0PB2
H14	HPC_LA07_N_B2	J15	GPIO0NB2
H16	HPC_LA11_P_B2	K18	GPIO35PB2/CCC_SE_CLKIN_S_11
H17	HPC_LA11_N_B2	K17	GPIO35NB2
H19	HPC_LA15_P_B2	A7	GPIO16PB2
H20	HPC_LA15_N_B2	A8	GPIO16NB2
H22	HPC_LA19_P_B2	C6	GPIO17PB2
H23	HPC_LA19_N_B2	B6	GPIO17NB2
H25	HPC_LA21_P_B2	H13	GPIO1PB2
H26	HPC_LA21_N_B2	H12	GPIO1NB2
H28	HPC_LA24_P_B2	E10	GPIO20PB2/DQS
H29	HPC_LA24_N_B2	E11	GPIO20NB2/DQS
H31	HPC_LA28_P_B2	D9	GPIO24PB2
H32	HPC_LA28_N_B2	C9	GPIO24NB2
H34	HPC_LA30_P_B2	G10	GPIO21PB2
H35	HPC_LA30_N_B2	F10	GPIO21NB2
H37	HPC_LA32_P_B2	E1	GPIO245PB2/CCC_SW_CLKIN_S_1
H38	HPC_LA32_N_B2	D1	GPIO245NB2
J2	HPC_CLK3_BIDIR_P_B4	AD4	GPIO180PB4/CLKIN_W_6/CCC_NW_CLKIN_W_6/CCC_NW_PLL0_OUT1
J3	HPC_CLK3_BIDIR_N_B4	AD5	GPIO180NB4
J6	HPC_HA03_P_B4	AB11	GPIO186PB4
J7	HPC_HA03_N_B4	AB10	GPIO186NB4
J9	HPC_HA07_P_B4	AB14	GPIO185PB4
J10	HPC_HA07_N_B4	AC13	GPIO185NB4
J12	HPC_HA11_P_B4	V13	GPIO203PB4
J13	HPC_HA11_N_B4	W13	GPIO203NB4
J15	HPC_HA14_P_B4	W11	GPIO202PB4
J16	HPC_HA14_N_B4	Y11	GPIO202NB4
J18	HPC_HA18_P_B4	V9	GPIO201PB4
J19	HPC_HA18_N_B4	W9	GPIO201NB4
J21	HPC_HA22_P_B4	AC1	GPIO175PB4/DQS
J22	HPC_HA22_N_B4	AD1	GPIO175NB4/DQS
J24	HPC_HB01_P_B5	K2	GPIO238PB5/CCC_SW_PLL0_OUT1
J25	HPC_HB01_N_B5	K3	GPIO238NB5

Table 11 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	PolarFire Pin Number	PolarFire Pin Name
J27	HPC_HB07_P_B5	K7	GPIO233PB5
J28	HPC_HB07_P_B5	K6	GPIO233NB5
J30	HPC_HB11_P_B5	N2	GPIO220PB5
J31	HPC_HB11_N_B5	N1	GPIO220NB5
J33	HPC_HB15_P_B5	P4	GPIO222PB5
J34	HPC_HB15_N_B5	P3	GPIO222NB5
J36	HPC_HB18_P_B5	R7	GPIO226PB5
J37	HPC_HB18_N_B5	R8	GPIO226NB5
K4	HPC_CLK2_BIDIR_P_B4	AC2	GPIO174PB4/CLKIN_W_7/CCC_NW_CLKIN_W_7/CCC_NW_PLL0_OUT0
K5	HPC_CLK2_BIDIR_N_B4	AD3	GPIO174NB4
K7	HPC_HA02_P_B4	AC7	GPIO178PB4
K8	HPC_HA02_N_B4	AC6	GPIO178NB4
K10	HPC_HA06_P_B4	AC9	GPIO181PB4/DQS/CCC_NW_PLL0_OUT0
K11	HPC_HA06_N_B4	AC8	GPIO181NB4/DQS
K13	HPC_HA10_P_B4	AC11	GPIO184PB4
K14	HPC_HA10_N_B4	AC12	GPIO184NB4
K16	HPC_HA17_CC_P_B4	T9	GPIO219PB4/CLKIN_W_3/CCC_SW_CLKIN_W_3
K17	HPC_HA17_CC_N_B4	T8	GPIO219NB4
K19	HPC_HA21_P_B4	W10	GPIO200PB4
K20	HPC_HA21_N_B4	Y10	GPIO200NB4
K22	HPC_HA23_P_B4	AB2	GPIO176PB4
K23	HPC_HA23_N_B4	AB1	GPIO176NB4
K25	HPC_HB00_CC_P_B5	G2	GPIO243PB5/CLKIN_W_0/CCC_SW_CLKIN_W_0
K26	HPC_HB00_CC_N_B5	G1	GPIO243NB5
K28	HPC_HB06_CC_P_B5	H2	GPIO240PB5/CLKIN_W_1/CCC_SW_CLKIN_W_1
K29	HPC_HB06_CC_P_B5	H1	GPIO240NB5
K31	HPC_HB10_P_B5	P6	GPIO229PB5/DQS
K32	HPC_HB10_N_B5	P5	GPIO229NB5/DQS
K34	HPC_HB14_P_B5	R5	GPIO227PB5
K35	HPC_HB14_N_B5	R6	GPIO227NB5
K37	HPC_HB17_CC_P_B5	J1	GPIO239PB5/CLKIN_W_2/CCC_SW_CLKIN_W_2/CCC_SW_PLL0_OUT0
K38	HPC_HB17_CC_N_B5	K1	GPIO239NB5

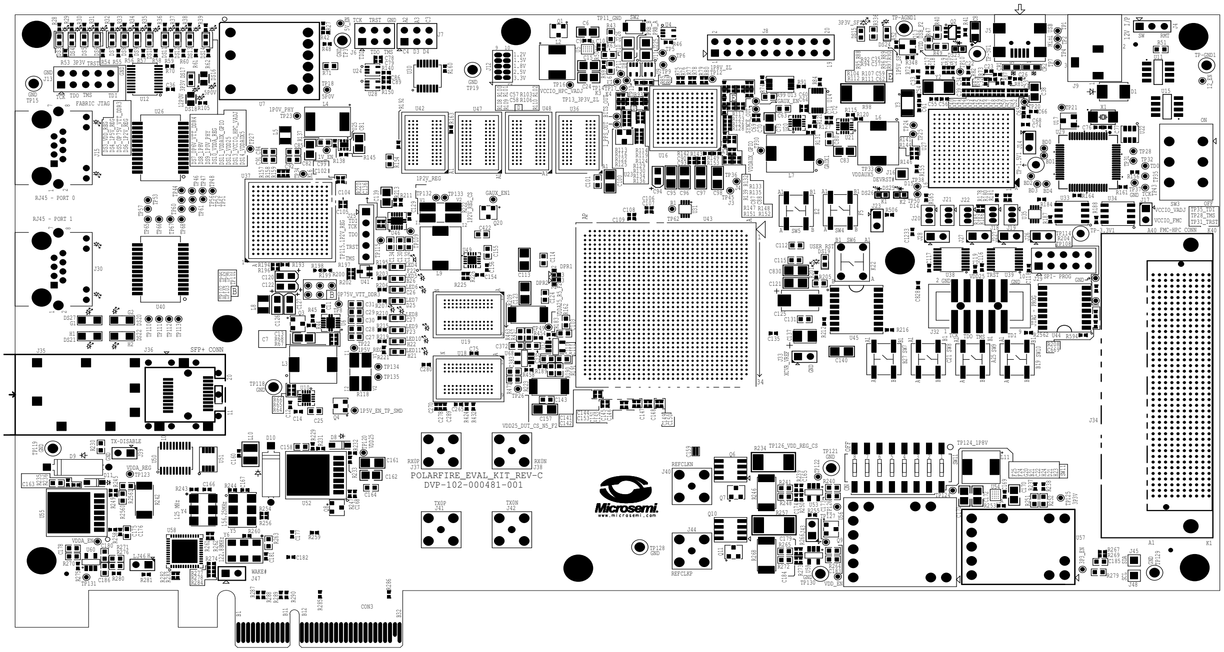
5 Pin List

For information on all of the package pins on the PolarFire device, see *Package Pin Assignment Table*.

6 Board Component Placement

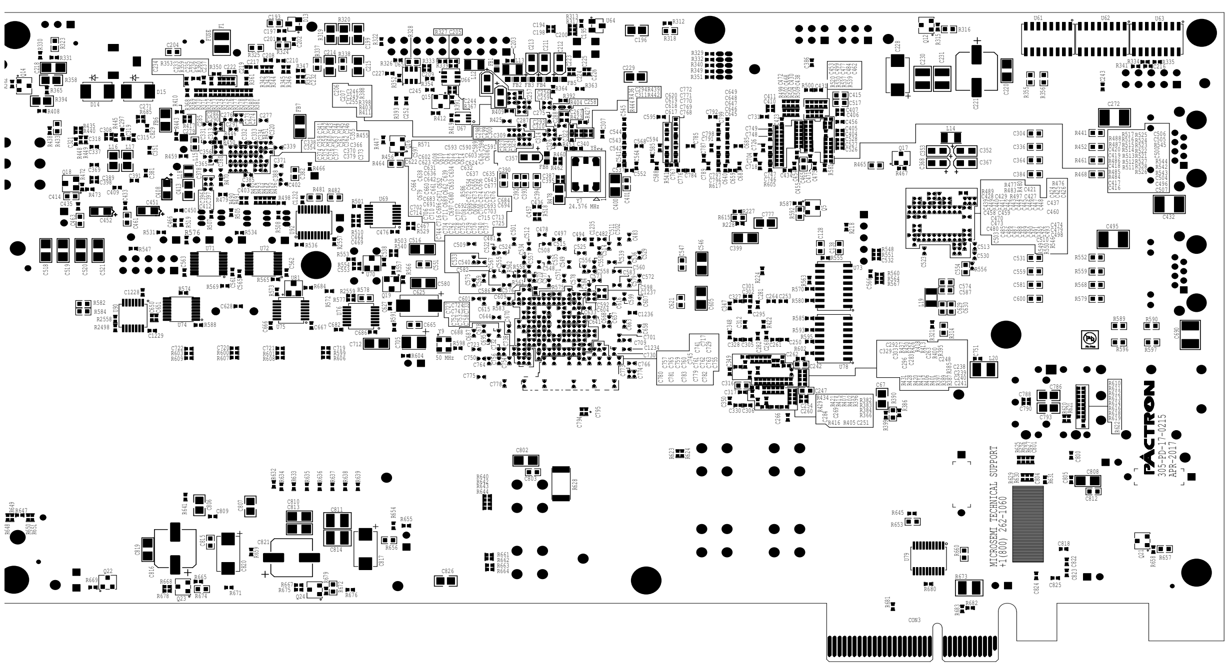
The following figure shows the placement of various components on the PolarFire Evaluation Board silkscreen.

Figure 18 • Silkscreen Top View



The following figure shows the bottom view of the PolarFire Evaluation Board silkscreen.

Figure 19 • Silkscreen Bottom View



7 Appendix 1: Running the Demo Design

The onboard PolarFire FPGA comes with a programmed design. For more information on running the demo, see *DG0755: PolarFire FPGA JESD204B Standalone Interface*.

8 Appendix 2: Programming PolarFire FPGA Using the On-Board FlashPro5

The PolarFire Evaluation Board includes onboard FlashPro5 programmer hardware. An external programmer hardware is therefore not required to program the PolarFire device. The device can be programmed using the FlashPro software installed on the host PC.

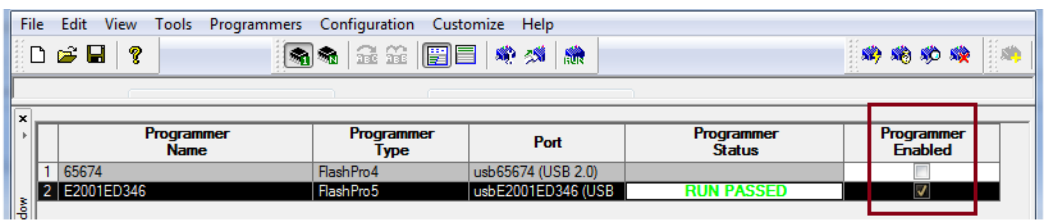
Follow these steps to program the on-board PolarFire device:

1. Connect the power supply cable to the **J9** connector on the board.
2. Connect the USB cable from the Host PC to the **J5** (FTDI port) on the board.
3. Power on the board using the **SW3** slide switch.
   When the board is successfully set up, the LEDs start glowing.
4. On the host PC, start the FlashPro software.
5. Click **New Project** to create a new project.
6. In the **New Project** window, do the following, and click OK:
   - Enter a project name.
   - Select **Single device** as the programming mode.
7. Click **Configure Device**.
8. Click **Browse**, and select the “xxxxxxxxxxxxxx.stp file from the **Load Programming File** window.

Note: The programming file will be available in a future release.

9. From the **View Programmer** pane, select the on-board FlashPro5 programmer as shown in the following figure.

Figure 20 • **Selecting the On-Board FlashPro5**



10. Click **Program** to program the device.
    The **Programmer List Window** in the FlashPro, shows the Programmer Name, Programmer Type, Port, Programmer Status, and the Programmer Enabled information.
11. When the device is programmed successfully, a Run Program PASSED status is displayed.

9 Appendix 3: Power Monitoring

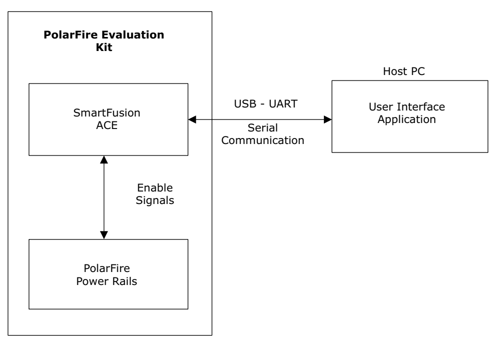
The SmartFusion A2F 200 device on the PolarFire Evaluation Board, monitors the voltage and current on different PolarFire power rails. It measures the current for different components and displays the power on the Microchip PowerMonitor application. PowerMonitor is a Graphical User Interface (GUI) application that runs on the host PC. The power monitoring program on the SmartFusion device measures the total device power without any manual measurements.

The power monitoring program does the following:

- Monitors voltage on all PolarFire power rails.
- Measures current and power on the following rails:
  - VDD_REG: Power supply for fabric core.
  - VDDA_REG: Power supply for transceiver and common circuits.
  - VDDA25: Power supply for transceiver PLLs. This supply is isolated from other power supplies to keep the noise low and avoid leakage for PCIe, EXT_PLL, and GPSS.
  - VDD25_DUT: Power supply for corner phase-locked loop (8 PLLs) and secure non-volatile memory (sNVM). These are tied together at the package level to keep the noise on the stand alone PLLs low.
- Monitors Flash*Freeze power when the PolarFire device is in Flash*Freeze mode.
- Powers-up and powers-down the board when pins 2 and 3 of the J4 jumper are closed.
- Powers-down the board if voltage threshold violations are observed on a power rail.

The analog computing engine block in the SmartFusion device is configured to measure the voltage and current on the PolarFire power rails. The following figure shows the power monitoring block diagram.

Figure 21 • **Power Monitoring Block Diagram**



9.1 Prerequisites

Before installing PowerMonitor, perform the following steps:

1. Download the PowerMonitor application from the following location:
   PolarFire Power Monitor
2. Ensure that Pin 1 and 2 of the J4 Jumper are closed.
3. Connect the Mini USB cable from **J5** to the host PC.
   The LEDs D2 and D3 start blinking when the power monitor program is running on the SmartFusion device. The board will not power ON unless it is connected via USB to the host PC.
4. Connect the power supply to **J9** and turn ON the **SW3** switch.
5. Ensure that the screen resolution of the Host PC is at least 1280×720. The screen resolution can be set from `Control Panel\Appearance and Personalization\Display\Screen Resolution`.
6. Ensure that the text size in the display setting of the Host PC is set to either small (100%) or medium (150%). The display size can be set from `Control Panel\Appearance and Personalization\Display`.

9.2 Installing PowerMonitor

To install PowerMonitor:

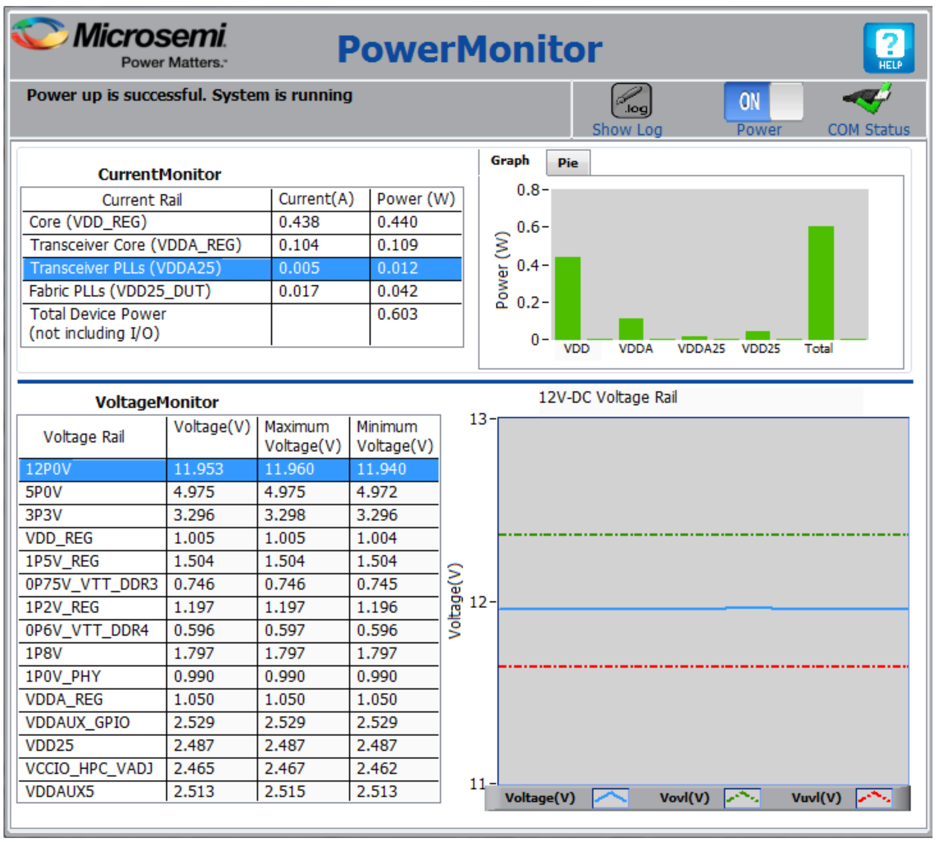
1. Extract the contents of the polarfire_power_monitor.rar file.
2. From POWER_MONITOR_GUI\Installer folder, double-click the `setup.exe` file.
3. Follow the instructions displayed on the installation wizard.
   After successful installation, PowerMonitor appears on the Start menu of the host PC desktop.
4. From the Start menu, click **PowerMonitor**.
   The **COMPort SetUp** window opens.
5. Select the highest numbered COM port, and click **Connect**.

The PowerMonitor GUI appears on the host PC.

9.3 About Microchip PowerMonitor

The following figure shows the PowerMonitor GUI.

Figure 22 • **PowerMonitor GUI**



The PowerMonitor GUI has the following panes:

- **CurrentMonitor**—This pane displays the current and power measured on VDD_REG, VDDA_REG, VDDA25, VDD25_DUT rails. This pane also displays the total device power. The I/Os are excluded.
- **VoltageMonitor**—This pane displays the present voltage measured on each voltage rail. This pane also displays the maximum and minimum voltage measured on each voltage rail over the time period of the PowerMonitor application.
  - **Voltage Rail Plot**—This pane displays the voltage plot of the selected rail as a blue line. The green and red lines represent the over-voltage (+3%) and under-voltage (-3%) tolerance levels of that rail. After staring the PowerMonitor GUI, the voltage plot takes minimum 5 seconds to plot the samples.

Note: For more information about the recommended minimum and maximum operating voltage of each rail, see the “Recommended Operating Conditions” section of *DS0141: PolarFire FPGA Datasheet*.

The PowerMonitor GUI has the following buttons:

- **Graph**—Click this button to view the power consumed by VDD_REG, VDDA_REG, VDDA25, and VDD25_DUT rails, and the total device power.
- **Pie**—Click this button to view the percentage power consumed by VDD_REG, VDDA_REG, VDDA25, and VDD25_DUT rails out of the total device power.
- **Show Log**—Click this button to view all of the power monitor program actions in a file.
- **Power**—Click this button to power-up or power-down the board when pins 2 and 3 of J4 jumper are closed.

Note: When pins 1 and 2 of J4 jumper are closed, use **SW3** switch to power-up or power-down the board.

10 Appendix 4: Performance Data

This section describes the performance results of MPF300T Evaluation Kit with different SERDES protocols. All of the steps required to set up the test environment are described. The section also provides information about eye diagram and jitter, and how they vary with protocol.

All the measurements are taken on MPF300T Evaluation Kit with 23 GHz Tektronix scope.

The following protocols are considered for evaluating the performance of the MPF300T Evaluation Kit.

1. JESD204B
   Data Rate: 12.5 Gbps - Reference Clock 156.25 MHz
2. 10BASE-G KR
   Data Rate: 10.3125 Gbps - Reference Clock 156.25 MHz
3. INTERLAKEN
   Data Rate: 10.312 Gbps - Reference Clock 156.25 MHz
4. CPRI
   Data Rate: 10.137 Gbps - Reference Clock 122.88 MHz

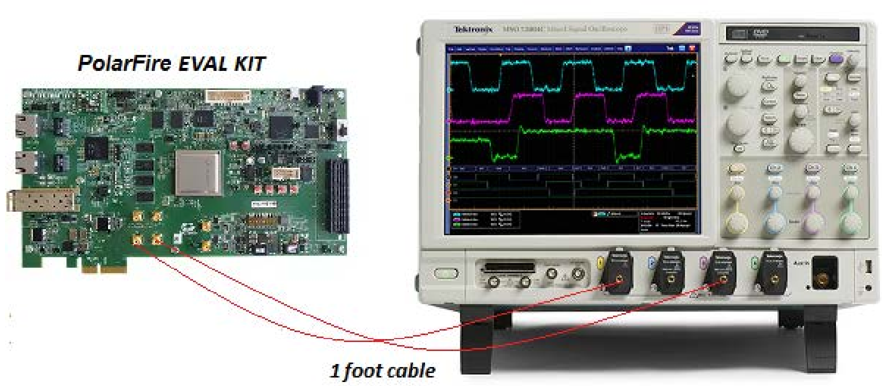
10.1 Setup Details

The following hardware and settings are used:

- MPF300T-1FCG1152
- Transceiver block 0, Lane 2
- Dedicated internal reference clock for the transceiver block (156.25 MHz or 122.88 MHz)
- LVDS25 I/O standard for reference clock input
- 23 GHz Tektronix (DPO72304) scope set to 100G samples/sec for measuring jitter and plotting eye
- Clock recovery configurations for scope:
  - Method: PLL-Custom BW
  - PLL Model: Type II
  - Damping: 700 m
- 1 foot long cable (part# Sucoflex 100 126E) for connecting the TX ports to the scope
- On PolarFire Evaluation board, a 2.3 inch long PCB trace exists between the device and TX SMA connectors.

The following figure provides a pictorial representation of the hardware setup used for the measurement.

Figure 23 • **Hardware Setup for Measurement**



Note: All measurements are taken with de-embedding the PCB trace.

10.2 JESD204B Results

The following driver settings are used for JESD measurements:

- Signal amplitude: 500 mV
- De-emphasis: 0 dB
- Pattern used: JSPAT (500 bits)
- Driver Impedance: 100 Ω
- Data Rate: 12.5 Gbps

The following table summarizes the measurements captured by the scope at 12.5 Gbps transmitter data rate and at a BER of 10E-12.

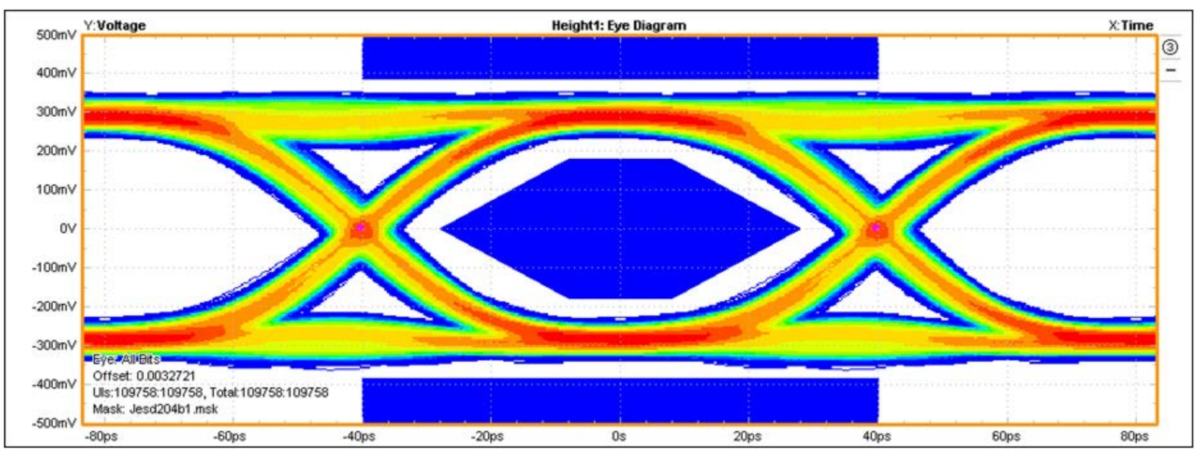
Table 12 • **JESD204B Jitter Measurements**[1]

Parameter	Value
Height	462.03 mV
TJ@BER	18.704 ps
Width@BER	61.296 ps
RJ	673.62 fs
DJ	9.27 ps

1. The measurement data is only indicative. The data is measured in typical conditions using 109757 bits. Results vary with different PVT conditions and scope. See the datasheet for the worst case jitter numbers.

The following figure shows the data eye plotted for the above settings.

Figure 24 • **JESD204B Eye Diagram With De-embedding**



10.3 10BASE-G KR

The following driver settings are used for 10BASE-G KR measurements:

- Signal amplitude: 1000 mV
- De-emphasis: -1 dB
- Pattern used: PRBS31
- Driver impedance: 180 Ω
- Data rate: 10.3125 Gbps

The following table summarizes the measurements captured by the scope at 10.3125 Gbps transmitter data rate and at a BER of 10E-12.

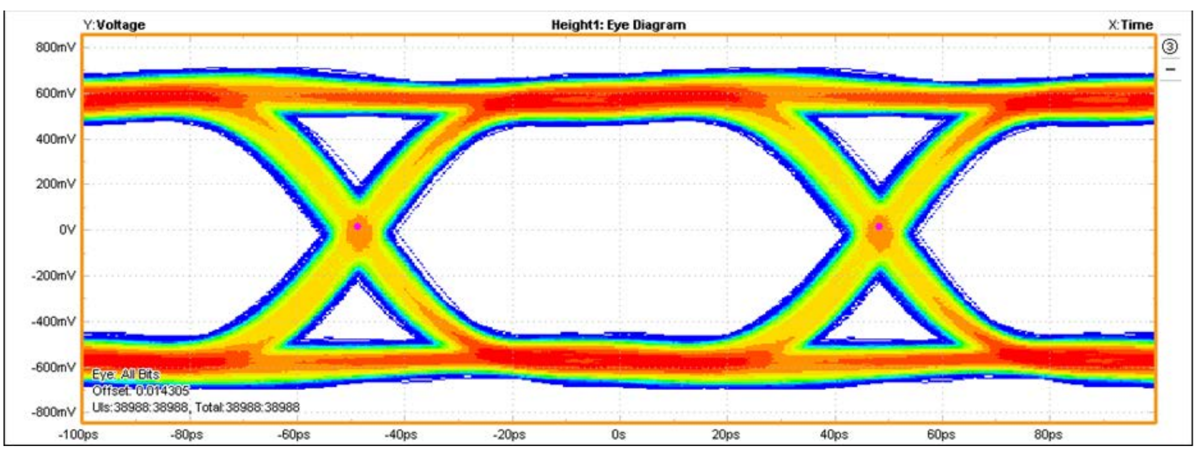
Table 13 • **10BASE-G KR Jitter Measurements[1]**

Parameter	Values
Height	911.44 mV
TJ@BER	21.31 ps
Width@BER	75.662 ps
RJ	760.57 fs
DJ	10.66 ps

1. The measurement data is only indicative. The data is measured in typical conditions using 38988 bits. Results vary with different PVT conditions and scope. See the datasheet for the worst case jitter numbers.

The following figure shows the data Eye plotted for the above settings.

Figure 25 • **10BASE-G KR Data Eye Diagram**



10.4 Interlaken

The following driver settings are used for Interlaken measurements:

- Signal amplitude: 500 mV
- De-emphasis: 0 dB
- Pattern used: PRBS31
- Driver impedance: 100 Ω
- Data rate: 10.3125 Gbps

The following table summarizes the measurements captured by the scope at of 10.3125 Gbps transmitter data rate and at a BER of 10E-12.

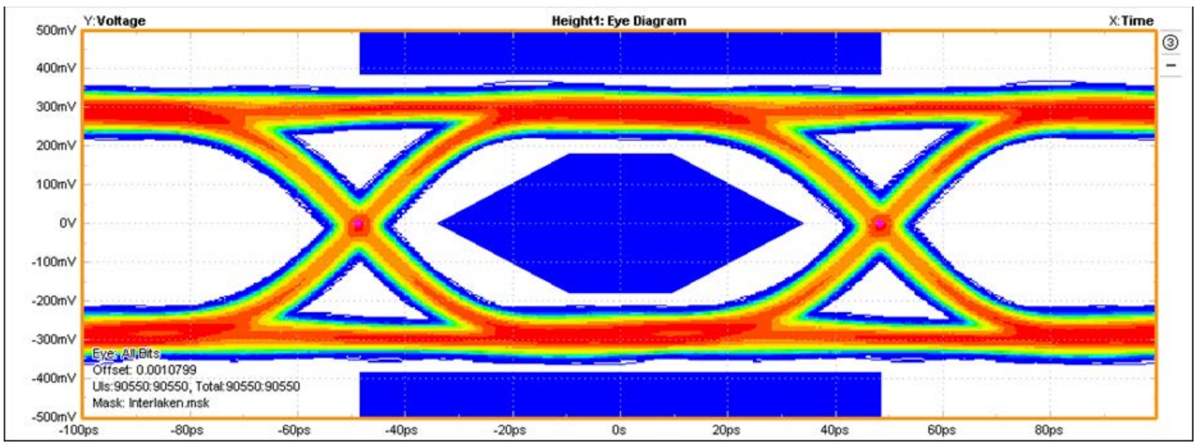
Table 14 • **Interlaken Jitter Measurements[1]**

Parameter	Values
Height	430.13 mV
TJ@BER	20.572 ps
Width@BER	76.396 ps
RJ	930.07 fs
DJ	7.55 ps

1. The measurement data is only indicative. The data is measured in typical conditions using 90550 bits. Results vary with different PVT conditions and scope. See the datasheet for the worst case jitter numbers.

The following figure shows the data Eye plotted for the above settings.

Figure 26 • **Interlaken Data Eye Diagram**



10.5 CPRI

The following driver settings are used for CPRI measurements:

- Signal amplitude: 1000 mV
- De-emphasis: -1 dB
- Pattern used: PRBS31
- Driver Impedance: 180Ω
- Data Rate: 10.137 Gbps

The following table summarizes the measurements captured by the scope at 10.137 Gbps transmitter data rate and at a BER of 10E-12.

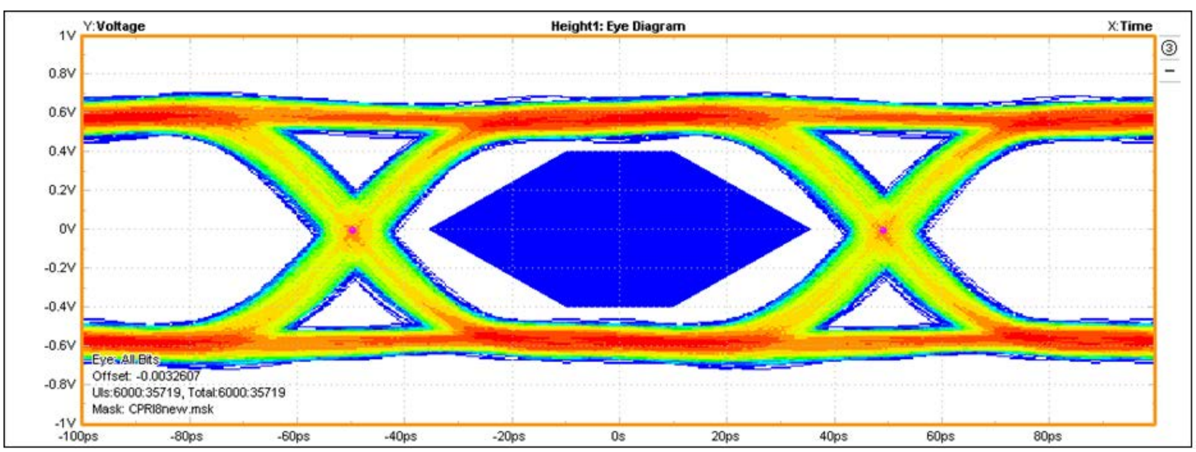
Table 15 • **CPRI Jitter Measurements[1]**

Parameter	Value
Height	903.58 mV
TJ@BER	26.664 ps
Width@BER	71.98 ps
RJ	1.08 ps
DJ	11.57 ps

1. The measurement data is only indicative. The data is measured in typical conditions using 35719 bits. Results vary with different PVT conditions and scope. See the datasheet for the worst case jitter numbers.

The following figure shows the data Eye plotted for the above settings.

Figure 27 • **CPRI Data Eye Diagram**



11 Appendix 5: Errata

This section contains information about known issues specific to the PolarFire Evaluation Board.

11.1 Errata Descriptions

11.1.1 Hot swapping is not supported on Programming headers J32, J29, PCIe CONN (CON3), SFP+ cage (J36), GPIO headers (J7, J8)

This restriction applies to Rev B and C of the board.

11.1.2 The VDDI3 (Bank 3) supply voltage is higher than the Datasheet specification

Bank 3 (VDDI3) and all circuits connected to Bank 3 have supply voltage of 3.3 V. User should not use the supply voltage of 3.3 V for Rev B board of Bank 3. This is addressed in the Rev C board.