

Efficient Virtual Memory for Big Memory Servers

Summary:

The objective of this paper is to introduce an idea for removing TLB miss penalties in the context of dealing with massive-memory workloads. The idea is to use a direct segment to map a portion of a linear virtual address space within a process, while page-mapping the other portions of the virtual address space. Direct segments use minimal per-core hardware to directly assign contiguous virtual memory sections to contiguous physical memory sections. From these schemes, the possibility of TLB misses for key data structures (e.g., in-memory key-value stores and database buffer pools) are reduced. Whenever necessary, it is possible to convert a memory mapped by a direct segment back to paging.

Strengths:

The idea of using a direct segment seems interesting. It is shown in the experiments that virtually all TLB performance penalties in massive-memory workloads are removed. Before using this feature, massive-memory servers are proven to be entangled with issues on high TLB misses. Plus, memory accesses in workloads are targeted to a huge anonymous region allocated considering available physical memory. Such issues are removed efficiently using a direct segment, as clearly shown in the experiments.