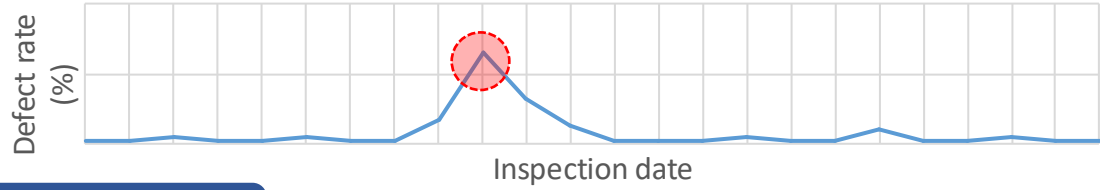
Identified and Resolved an ESD Defect Spike via Dielectric Thickness Control

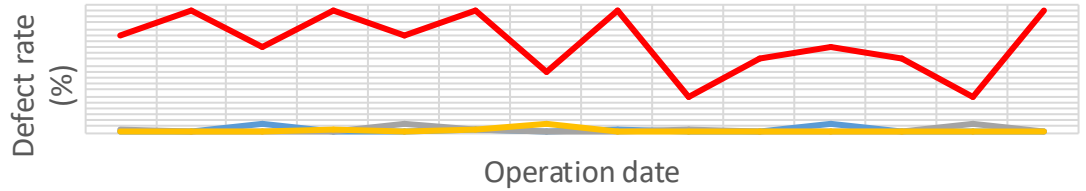
Problem

- ESD defect rate spike
  - A sudden spike in the electrostatic discharge (ESD) defect rate occurred
  - This defect caused reliability failures, scrap, and significant yield loss

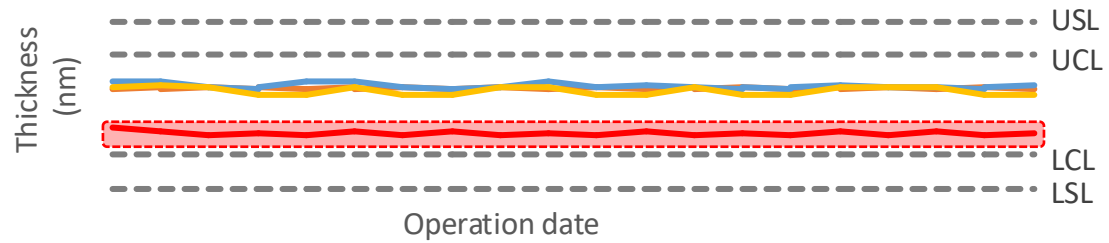


Investigation

- Tool-to-tool defect rate variation
  - **One photolithography coater** showed a higher defect rate than others
  - Confirmed through tool-level analysis at a specific process step

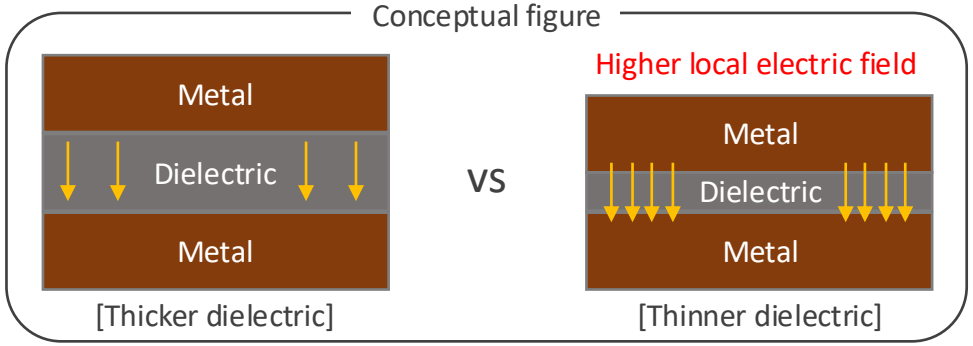


- Lower thickness
  - The same photolithography coater produced **a thinner layer**
  - Confirmed by inline thickness monitoring data and SEM analysis



Hypothesis

- Capacitive coupling effect
  - **Thinner dielectrics** in the capacitive stack led to **higher local electric fields**, increasing ESD susceptibility



Verification

- Higher thickness target
  - Resulted in **a lower defect rate** in tool-level pre/post comparisons
- SEM analysis
  - Showed that most ESD-defective samples had **thinner dielectric layers**

Action

- Thickness spec & control limit
  - **Adjusted the thickness target** and **redefined spec** with related teams
- Thickness monitoring
  - Implemented automated thickness monitoring with email alerts
  - Increased thickness measurement frequency

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