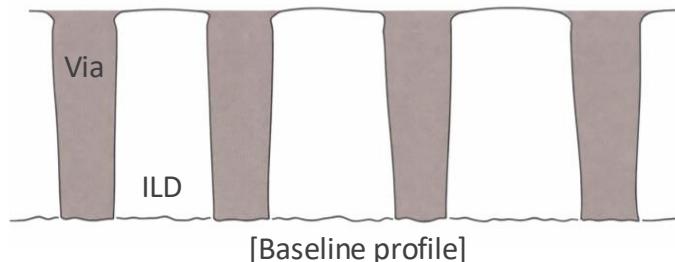


Increased Via Metal Volume While Maintaining Leakage Margin without Arcing

Objectives

- Via etch process development

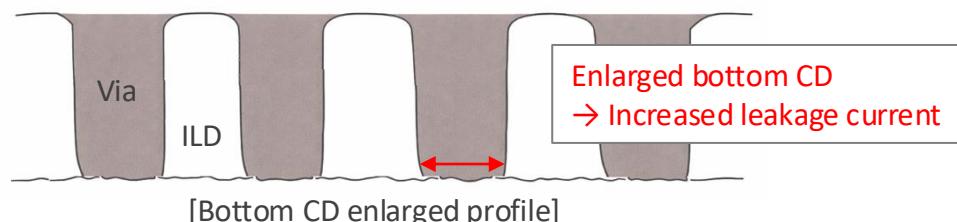
- Increase via metal volume while maintaining leakage margin



Challenges

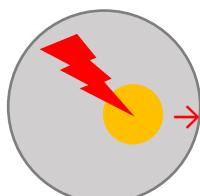
- Bottom CD enlargement

- Ion and radical bombardment at the via bottom causes **bottom CD enlargement**, resulting in **increased leakage current**



- Arcing during processing

- Significant **plasma-induced arcing** causes **localized surface damage**



→ Charge accumulation leading to localized electric field and arcing

[Arcing on wafer]

Approach

- Gas chemistry design

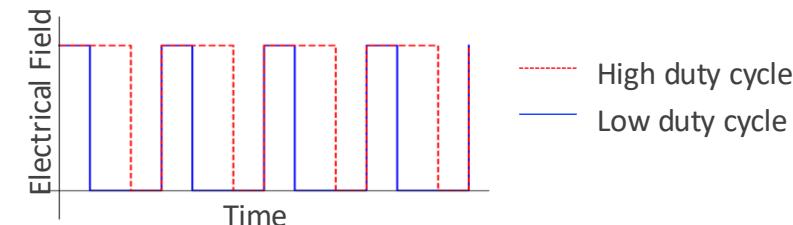
- Optimize multi-step etch gas chemistries to improve via profile while **preserving bottom CD**

- Ion beam angle control

- Control ion beam angle to **suppress bottom CD enlargement**

- Duty cycle adjustment

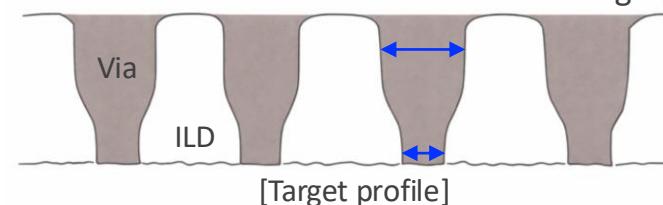
- Adjust duty cycle to enable plasma relaxation during off periods, **mitigating charge buildup** with a controlled etch-rate trade-off



Outcome

- Target via profile achievement

- Maintained bottom CD while increasing upper CD



- Plasma process stability

- Eliminated plasma arcing during processing