741 Operational Amplifier

Ghassan Arnouk

ELEC 3509B
Summer 2020
Lab 3 Report

Instructor: Qi-Jun Zhang

Lab Period: B1
Day 1 Preformed: 2020/07/29
Day 2 Preformed: 2020/07/30

Date Submitted: 2020/08/06

Contents

List of Tables

List of Figures

1 Introduction

The first amplifying device looked at when studying electronics is the operational amplifier (op-amp). The main purpose of the op-amp is to amplify weak signals when amplified signals are needed. One of the most common op-amps in currently in the market is the 741 op-amp. Along with its ability to amplify signals well, the 741 op-amp is low in cost, thus making it at one point in time, one of the most commonly used devices in electronics.
This lab looks at the 741 op-amp in further detail. The op-amp is analyzed to find its parameters in each transistor within the op-amp and is then simulated on the simulating software PSPICE to compare the measured parameters with the calculated ones. A schematic of the 741 op-amp used in this lab is shown in Figure 1 below.

2 Prelab

Fig. 1 below shows the 741 Operational Amplifier circuit that will analyzed for this prelab.

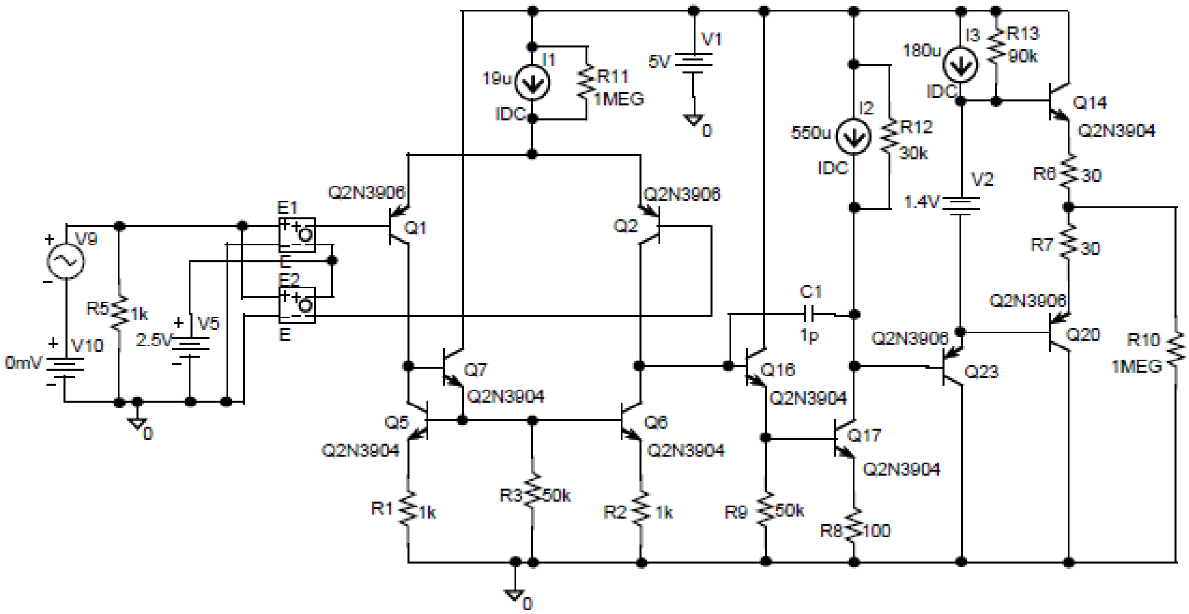


Figure 1: 741 Operational Amplifier

Table 1 below lists some assumptions for NPN and PNP parameters that is an asset in completing the prelab calculations.

Table 1: Assumptions of parameters

Parameter	**NPN**	**PNP**
Early Voltage V_A	80 V	20 V
Beta (assume constant but note that it normally depends on current)	100	100
I_s (recall that $I_c = I_s e^{\frac{V_{BE}}{V_T}}$)	6.73 fA	1.41 fA
V_{BE}	0.6 V	0.6 V
V_{CC}	5 V	5 V

2.1 DC Analysis

Q_{14} and Q_{20} Transistors

Applying KVL:

$$-1.4\ V = V_{BE_{14}} + R_6(I_{R_{10}} + I_{R_{10}}) + R_7(I_{E_{20}}) + V_{BE_{20}}$$

By substitution, we get the following:

$$1.4 = ln(\frac{I_C}{I_{S_{20}}})V_T + R_6(I_{E_{20}} + I_{R_{10}}) + R_7(I_{E_{20}}) + ln(\frac{I_C}{I_{S_{14}}})V_T$$

Solving the above equation and ignoring $I_{R_{10}}$, we get the following:

$$1.4\ V = ln\left[\frac{\left(\frac{100}{101}\right) I_{E_{20}}}{I_{S_{20}}}\right](25\ mV) + (30\ \Omega)(I_{E_{20}}) + ln\left[\frac{\left(\frac{100}{101}\right) I_{E_{20}}}{I_{S_{14}}}\right](25\ mV)$$

$$\therefore I_{E_{20}} = I_{E_{14}} \approx 1.14\ mA$$

Finding the collector current:

$$\begin{aligned} I_{C_{20}} = I_{C_{14}} &= \frac{\beta}{\beta+1}(I_E) \\ &= \frac{100}{100+1}(1.14\ mA) \\ &\approx 1.13\ mA \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_{20}} = g_{m_{14}} &= \frac{I_C}{V_T} \\ &= \frac{1.13\ mA}{25\ mV} \\ &= 45.2\ mA/V \end{aligned}$$

Finding r_o:

$$\begin{aligned} r_{o_{20}} &= \frac{V_A}{I_{C_{20}}} \\ &= \frac{20\ V}{1.13\ mA} \\ &= 17.7\ k\Omega \end{aligned}$$

$$\begin{aligned} r_{o_{14}} &= \frac{V_A}{I_{C_{14}}} \\ &= \frac{80\ V}{1.13\ mA} \\ &= 70.8\ k\Omega \end{aligned}$$

Q_{23} Transistor

$$I_{E_{23}} = \frac{I_{C_{20}}}{\beta} + \left[180\ \mu A + \left(\frac{5\ V - 3.22\ V}{R_{13}} - \frac{I_{C_{14}}}{\beta}\right)\right]$$
$$I_{E_{23}} = \frac{1.13\ mA}{100} + \left[180\ \mu A + \left(\frac{5\ V - 3.22\ V}{R_{13}} - \frac{1.13\ mA}{100}\right)\right]$$

$$\therefore I_{E_{23}} = 200\ \mu A$$

Finding the collector current:

$$\begin{aligned} I_{C_{23}} &= \frac{\beta}{\beta+1}(I_{E_{23}}) \\ &= \frac{100}{100+1}(200\ \mu A) \\ &\approx 198\ \mu A \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_{23}} &= \frac{I_{C_{23}}}{V_T} \\ &= \frac{198\ \mu A}{25\ mV} \\ &= 7.92\ mA/V \end{aligned}$$

Finding r_o:

$$\begin{aligned} r_{o_{23}} &= \frac{V_A}{I_{C_{23}}} \\ &= \frac{20\ V}{198\ \mu A} \\ &= 101\ k\Omega \end{aligned}$$

Q_{17} Transistor

Finding the collector current:

$$\begin{aligned} I_{C_{17}} &= \frac{I_{C_{23}}}{\beta} + 550\ \mu A + \frac{5\ V - 1.22\ V}{30\ k\Omega} \\ &= \frac{198\ \mu A}{100} + 550\ \mu A + \frac{5\ V - 1.22\ V}{30\ k\Omega} \\ &= 678\ \mu A \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_{17}} &= \frac{I_{C_{17}}}{V_T} \\ &= \frac{678\ \mu A}{25\ mV} \\ &= 27.1\ mA/V \end{aligned}$$

Finding r_o:

$$\begin{aligned} r_{o_{17}} &= \frac{V_A}{I_{C_{17}}} \\ &= \frac{80\ V}{678\ \mu A} \\ &= 118\ k\Omega \end{aligned}$$

$\mathbf{Q_{16}}$ Transistor

Finding the emitter current:

$$\begin{aligned} I_{C_{16}} &= \frac{I_{C_{17}}}{\beta} + \frac{669\ mV}{R_9} \\ &= \frac{678\ \mu A}{100} + \frac{669\ mV}{50\ k\Omega} \\ &= 20.2\ \mu A \end{aligned}$$

Finding the collector current:

$$\begin{aligned} I_{C_{16}} &= \frac{\beta}{\beta+1}(I_{E_{16}}) \\ &= \frac{100}{100+1}(20.2\ \mu A) \\ &\approx 19.96\ \mu A \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_{16}} &= \frac{I_{C_{16}}}{V_T} \\ &= \frac{19.96\ \mu A}{25\ mV} \\ &= 798\ \mu A/V \end{aligned}$$

Finding r_o:

$$\begin{aligned} r_{o_{16}} &= \frac{V_A}{I_{C_{16}}} \\ &= \frac{80\ V}{19.96\ \mu A} \\ &= 4\ M\Omega \end{aligned}$$

$\mathbf{Q_1}$ Transistor

$$\begin{aligned} V_{in} = 2.5\ V &\rightarrow V_{B_1} = 2.5\ V \\ V_{E_1} = V_{E_2} = 2.5\ V + 0.6\ V &= 3.1\ V \\ \therefore I_{E_1} = I_{E_2} &= 10.45\ \mu A \end{aligned}$$

Finding the collector current:

$$\begin{aligned} I_{C_1} &= \frac{\beta}{\beta+1}(I_{E_1}) \\ &= \frac{100}{100+1}(10.45\ \mu A) \\ &= 10.35\ \mu A \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_1} &= \frac{I_{C_1}}{V_T} \\ &= \frac{10.35\ \mu A}{25\ mV} \\ &= 414\ \mu A/V \end{aligned}$$

Finding r_o:

$$\begin{aligned} r_{o_1} &= \frac{V_A}{I_{C_1}} \\ &= \frac{80\ V}{10.35\ \mu A} \\ &= 1.93\ M\Omega \end{aligned}$$

Q_2 Transistor

Finding the collector current:

$$I_{C_2} = I_{C_1} = 10.35\ \mu A$$

Finding the transconductance:

$$g_{m_2} = g_{m_1} = 414\ \mu A/V$$

Finding r_o:

$$r_{o_2} = r_{o_1} = 1.93\ M\Omega$$

Q_6 Transistor

Finding the collector current:

$$\begin{aligned} I_{C_6} &= I_{C_2} - \frac{I_{C_{16}}}{\beta} \\ &= 10.35\ \mu A - \frac{19.96\ \mu A}{100} \\ &\approx 10.15\ \mu A \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_6} &= \frac{I_{C_6}}{V_T} \\ &= \frac{10.15\ \mu A}{25\ mV} \\ &= 406\ \mu A/V \end{aligned}$$

Finding the r_o:

$$\begin{aligned} r_{o_6} &= \frac{V_A}{I_{C_{16}}} \\ &= \frac{80\ V}{10.15\ \mu A} \\ &= 7.9\ M\Omega \end{aligned}$$

Q_5 Transistor

Finding the emitter current:

$$\begin{aligned} I_{E_5} &= \frac{10.25\ mV}{R_1} \\ &= \frac{10.25\ mV}{1\ k\Omega} \\ &= 10.25\ \mu A \end{aligned}$$

Finding the collector current:

$$\begin{aligned} I_{C_5} &= \frac{\beta}{\beta+1}(I_{E_5}) \\ &= \frac{100}{100+1}(10.25\ \mu A) \\ &\approx 10.15\ \mu A \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_5} &= \frac{I_{C_5}}{V_T} \\ &= \frac{80\ V}{25\ mV} \\ &= 406\ \mu A/V \end{aligned}$$

Finding r_o:

$$\begin{aligned} r_{o_6} &= \frac{V_A}{I_{C_5}} \\ &= \frac{80\ V}{10.15\ \mu A} \\ &= 7.9\ M\Omega \end{aligned}$$

Q_7 Transistor

Finding the emitter current"

$$\begin{aligned} I_{E_7} &= \frac{I_{C_5}}{\beta} + \frac{0.61\ V}{R_3} + \frac{I_{C_6}}{\beta} \\ &= \frac{10.15\ \mu A}{100} + \frac{0.61\ V}{50\ k\Omega} + \frac{10.15\ \mu A}{100} \\ &= 12.4\ \mu A \end{aligned}$$

Finding the collector current:

$$\begin{aligned} I_{C_7} &= \frac{\beta}{\beta+1}(I_{E_7}) \\ &= \frac{100}{100+1}(12.4\ \mu A) \\ &\approx 12.28\ \mu A \end{aligned}$$

Finding the transconductance:

$$\begin{aligned} g_{m_7} &= \frac{I_{C_7}}{V_T} \\ &= \frac{12.28\ \mu A}{25\ mV} \\ &= 491.2\ \mu A/V \end{aligned}$$

Finding r_o:

$$\begin{aligned} r_{o_7} &= \frac{V_A}{I_{C_7}} \\ &= \frac{80\ V}{12.28\ \mu A/V} \\ &= 6.5\ M\Omega \end{aligned}$$

Table 2: DC Analysis Summary

Transistor	I_C	g_m	r_o
Q_1	10.35 μA	414 μA/V	1.93 MΩ
Q_2	10.35 μA	414 μA/V	1.93 MΩ
Q_5	10.15 μA	406 μA/V	7.90 MΩ
Q_6	10.15 μA	406 μA/V	7.90 MΩ
Q_7	12.28 mA	491.2 μA/V	6.50 MΩ
Q_{14}	1.13 mA	45.2 mA/V	70.8 kΩ
Q_{16}	19.96 μA	798 μA/V	4 MΩ
Q_{17}	678 μA	27.1 mA/V	118 kΩ
Q_{20}	1.13 mA	45.2 mA/V	17.7 kΩ
Q_{23}	198 μA	7.92 mA/V	101 kΩ

2.2 AC Analysis

Stage 1 Gain (A_{v_1}):

The gain in the first stage, which is defined as the input to the base of Q_{16}, including the impedance seen looking into the base of Q_{16} as a load to the first stage, is found using the following equations.

Figure 2 below shows the small-signal circuit of the first stage of the gain.

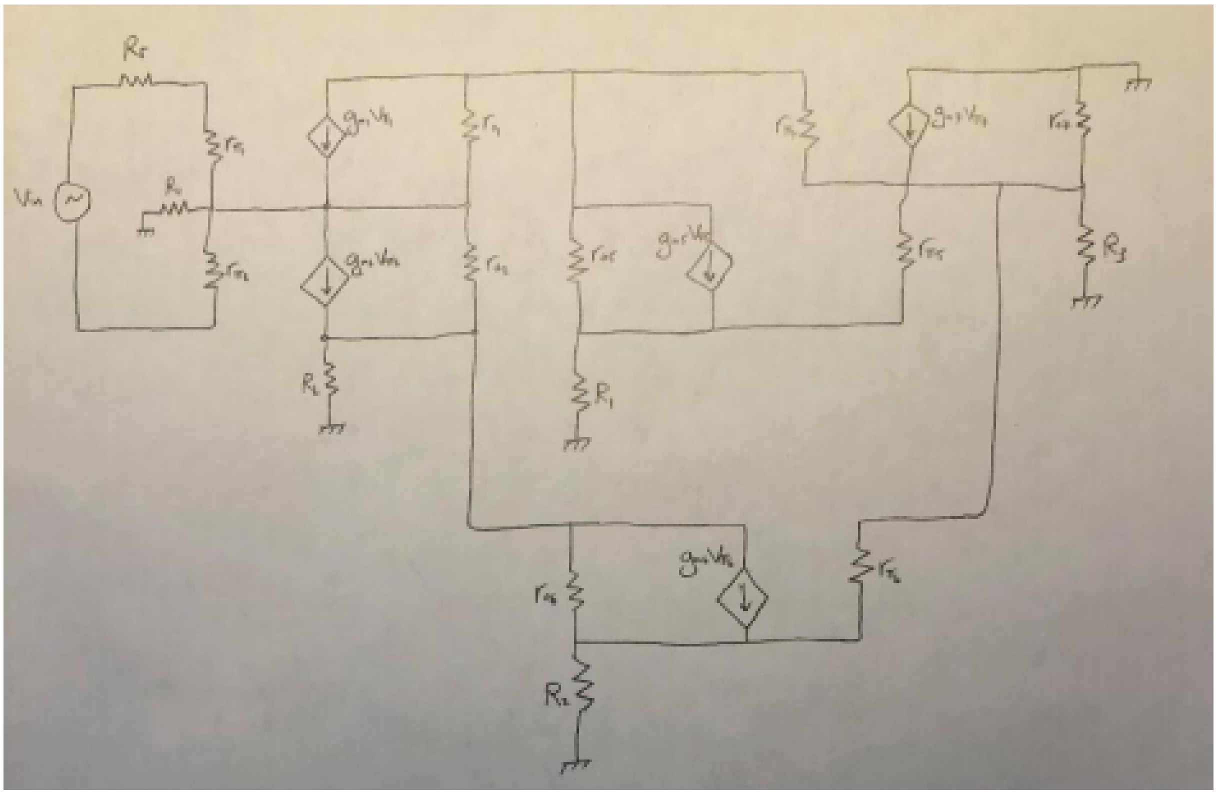


Figure 2: Small Signal Model of The First Stage of The Gain

Note that Q_7 is treated as a short due to the fact that there is no degeneration resistors and a single-ended load

$$
\begin{aligned}
I_5 &= \frac{v_{\pi_5}}{r_{o_5}} + \frac{v_{\pi_5}}{r_{\pi_5}} + g_{m_5} v_{\pi_5} \\
&= \frac{v_{\pi_5}}{r_{o_5} // r_{\pi_5} // \frac{1}{g_{m_5}}} \rightarrow parallel\ with\ r_{\pi_6}
\end{aligned}
$$

A simplified small signal model of the first stage of the gain is shown below in Figure 3.

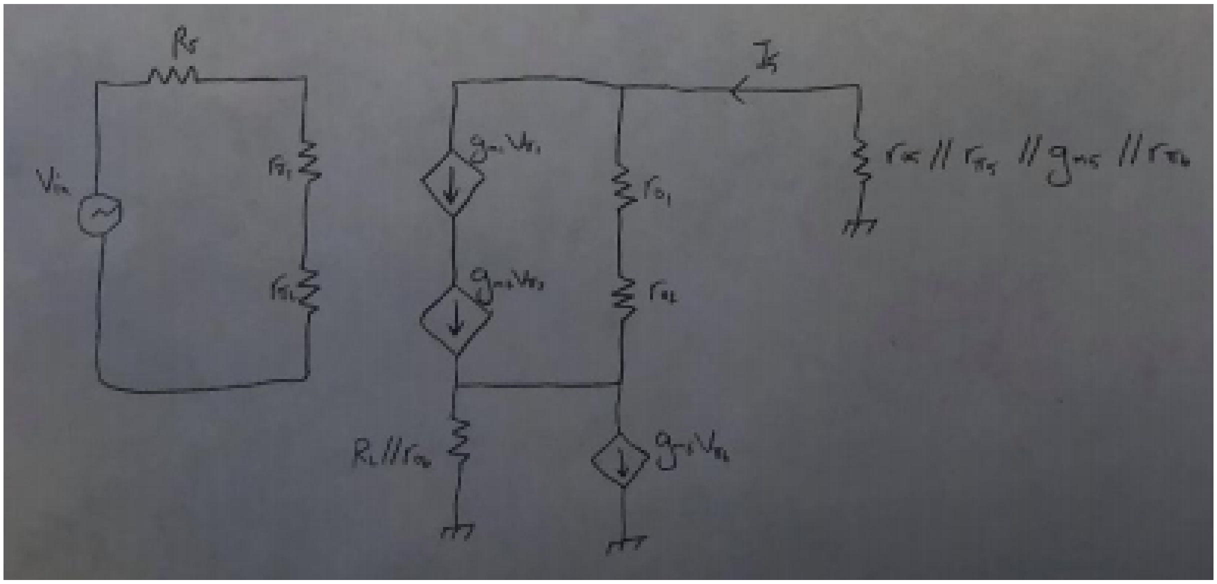


Figure 3: Simplified Small Signal Model of The First Stage of The Gain

In order to analyze the circuit easily, assumptions have been made:

- $r_{o_1} + r_{o_2}$ is a very large so they act as an open circuit
- $g_{m_1}v_{\pi_1}$ and $g_{m_2}v_{\pi_2}$ can be combined since they are biased the same
- $g_{m_5} = g_{m_6}$ since both transistors are biased the same
- R_S is negligible when compared to r_{π_1} and r_{π_2}
- High input impedance for Stage 1

$$
\begin{aligned}
V_L &= 2g_{m_2}v_{\pi_2}(R_{L_1}//r_{o_6}//r_{o_2}) \\
A_{v_1} &= \frac{V_L}{V_{in}} \\
&= g_{m_2}(R_{L_1}//r_{o_6}//r_{o_2})
\end{aligned}
$$

To determine the output resistance, a resistor equivalent is added to R_2:

$$
\begin{aligned}
R_{out_1} &= r_{o_6}[1 + g_{m_6}(R_2//r_{\pi_6})] + (R_2//r_{\pi_6}) \\
&= (7.90\ M\Omega)[1 + 406\ \mu A/V(1\ k\Omega//249\ k\Omega)] + (1\ k\Omega//249\ k\Omega) \\
&= 11.095 M\Omega
\end{aligned}
$$

Determining R_{in} for the second stage of the gian:

$$
\begin{aligned}
R_{in_2} &= (\beta_{16} + 1)[r_{e_{16}} + r_{o_{16}}//R_9//(r_{\pi_{17}} + R_8 + (r_{\pi_{17}})(R_8)(g_{m_{17}}))] \\
&= (100 + 1)[1253.13\ \Omega + 4\ M\Omega//50\ k\Omega//(3.7\ k\Omega + 100\ \Omega + (3.7\ k\Omega)(100\ \Omega)(27.1\ \mu A/V))] \\
&= 1.218\ M\Omega
\end{aligned}
$$

Determining R_{L_1}:

$$
\begin{aligned}
R_{L_1} &= R_{in_2}//R_{out_1} \\
&= 1.218\ M\Omega//11.095 M\Omega \\
&= 1.098\ M\Omega
\end{aligned}
$$

The first stage of the gain can be calculated as follows:

$$\begin{aligned} A_{v_1} &= g_{m_2}(R_{L_1}//r_{o_6}//r_{o_2}) \\ &= 414\ \mu A/V(1.098\ M\Omega//7.90\ M\Omega//1.93\ M\Omega) \end{aligned}$$

$$\therefore A_{v_1} = 266.16\ v/v$$

Stage 2 Gain (A_{v_2}):

The second stage of the gain is calculated, which is defined as the gain from the base of Q_{16} to the base of Q_{23}. The small-signal model of stage 2 is shown in Figure 4 below.

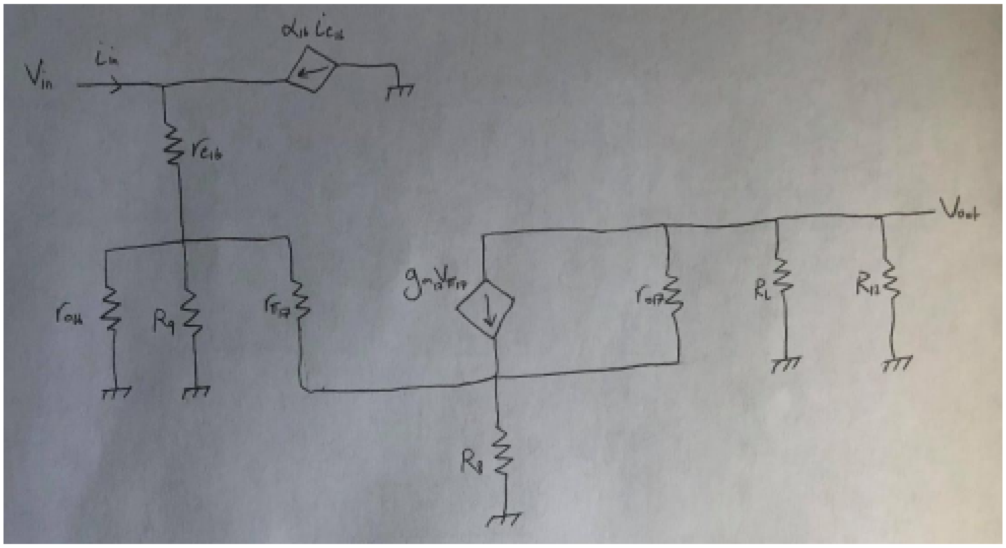


Figure 4: Small Signal Model of The Second Stage of The Gain

The second stage of the gain can be calculated as follows:

$$\begin{aligned} A_{v_2} &= \frac{v_{out}}{v_{in}} \\ &= \frac{v_{out}}{v_{\pi_{17}}} * \frac{v_{\pi_{17}}}{v_{b_{17}}} * \frac{v_{b_{17}}}{v_{in}} \end{aligned}$$

$$\begin{aligned} \frac{v_{out}}{v_{\pi_{17}}} &= (-g_{m_{17}})(R_{L_2}//R_{12}) \\ &= (-27.1\ mA/V)(R_{L_2}//R_{12}) \end{aligned}$$

$$\begin{aligned} \frac{v_{\pi_{17}}}{v_{b_{17}}} &= \frac{r_{\pi_{17}}}{r_{\pi_{17}} + R_8(1+\beta)} \\ &= \frac{3.7\ k\Omega}{3.7\ k\Omega + (100\ \Omega)(1+100)} \\ &= 0.2681\ v/v \end{aligned}$$

Define $r'_{\pi_{17}}$ as follows:

$$\begin{aligned} r'_{\pi_{17}} &= r_{\pi_{17}} + R_8(1+\beta) \\ &= 3.7\ k\Omega + (1+100)(100\ \Omega) \\ &= 13.8\ k\Omega \end{aligned}$$

$$\begin{aligned}\frac{v_{b_{17}}}{v_{in}} &= \frac{(1+\beta)[r_{o_{16}}//R_9//r'_{\pi_{17}}]}{(1+\beta)[r_{o_{16}}//R_9//r'_{\pi_{17}}] + r_{e_{16}}(1+\beta)} \\ &= \frac{(1+100)[4\ M\Omega//50\ k\Omega//13.8\ k\Omega]}{(1+100)[4\ M\Omega//50\ k\Omega//13.8\ k\Omega] + (1253.13\ \Omega)(1+100)} \\ &= 0.8959\ v/v\end{aligned}$$

The input impedance of the third stage is calculated as follows:

$$\begin{aligned}R_{in_3} &= r_{e_{23}}(1+\beta) + (1+\beta)[(1+\beta)[R_{10} + (r_{e_{14}} + R_6)//(r_{e_{20}} + R_7)]//R_{13}] \\ &= (126.6\ \Omega)(1+100) + (1+100)[(1+100)[1\ M\Omega + (22.1\ \Omega + 30\ \Omega)//(22.1\ \Omega + 30\ \Omega)]//90\ k\Omega] \\ &\approx 9.095\ M\Omega\end{aligned}$$

In this stage, R_{L_2} is equivalent to R_{in_3}

$$\therefore R_{L_2} = 9.095\ M\Omega$$

Therefore, the gain for the second stage is:

$$A_{v_2} = [(-27.1\ mA/V)(9.095\ M\Omega//30\ k\Omega)]\,[0.2681 * 0.8959]$$

$$\therefore A_{v_2} = -194.65\ v/v$$

Stage 3 Gain (A_{v_3}):

The third stage of the gain is calculated. The small-signal model of stage 2 is shown in Figure 5 below. The

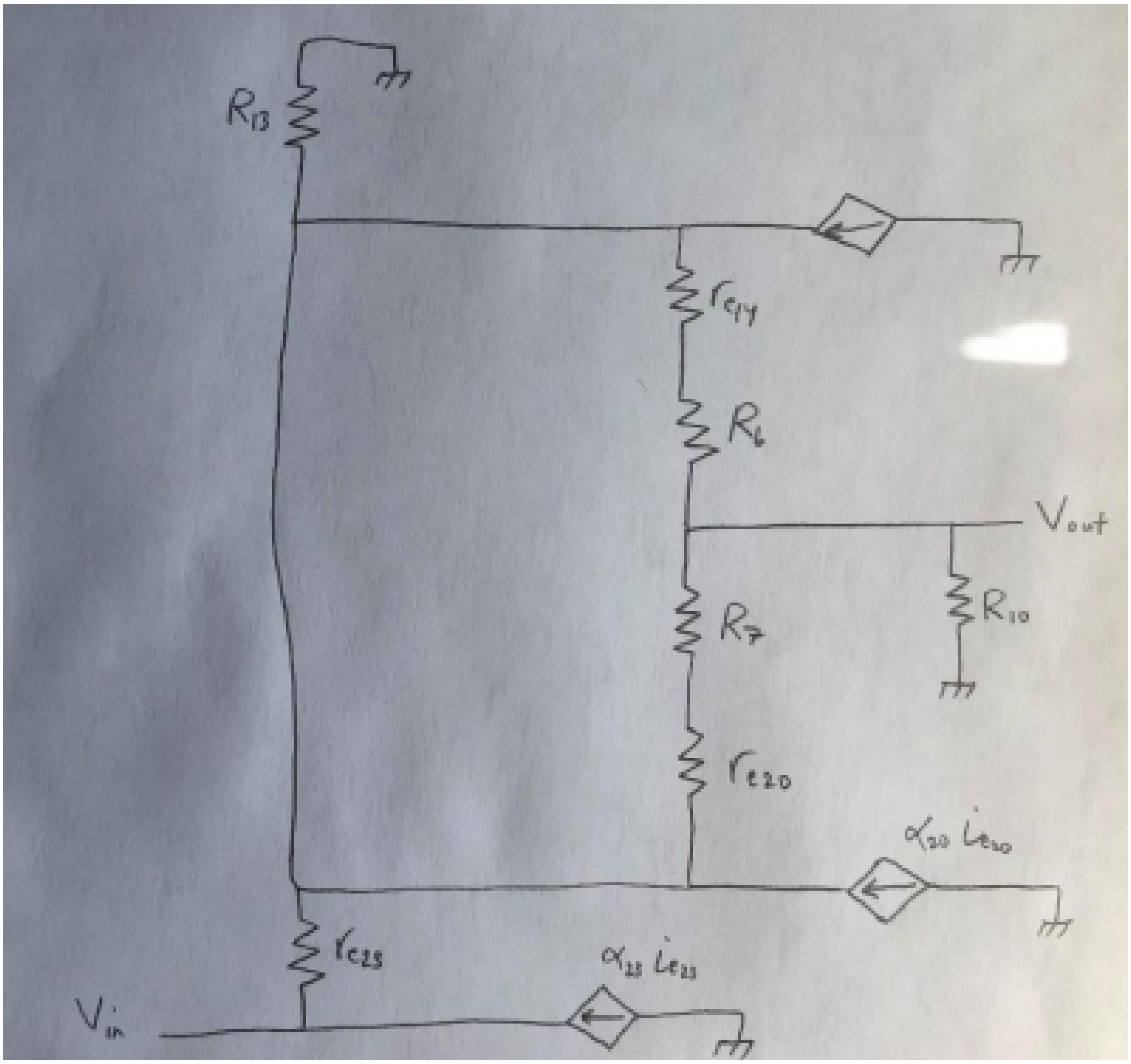


Figure 5: Small Signal Model of The Third Stage of The Gain

third stage of the gain can be calculated as follows:

$$
\begin{aligned}
A_{v_3} &= \left[\frac{R_{10}}{R_{10} + (r_{e_{14}} + R_6)//(r_{e_{20}} + R_7)}\right]\left[\frac{(1+\beta)[R_{10} + [(r_{e_{16}} + R_6)//(r_{e_{20}} + R_7)//R_{13}]]}{r_{e_{23}} + (1+\beta)[R_{10} + [(r_{e_{16}} + R_6)//(r_{e_{20}} + R_7)//R_{13}]]}\right] \\
&= \left[\frac{1\ M\Omega}{1\ M\Omega + (22.1\ \Omega + 30\ \Omega)//(22.1\ \Omega + 30\ \Omega)}\right] * \\
&\quad \left[\frac{(1+100)[1\ M\Omega + [(22.1\ \Omega + 30\ \Omega)//(22.1\ \Omega + 30\ \Omega)//30\ k\Omega]]}{126.26\ \Omega + (1+100)[1\ M\Omega + [(22.1\ \Omega + 30\ \Omega)//(22.1\ \Omega + 30\ \Omega)//30\ k\Omega]]}\right]
\end{aligned}
$$

$$\therefore A_{v_3} = 0.99 \approx 1\ v/v$$

Total Gain (G_v):

Therefore, the total gain of the 741 operational amplifier can be calculated as follows:

$$\begin{aligned} G_v &= A_{v_1} * A_{v_2} * A_{v_3} \\ &= (266.16)(-1944.65)(0.9999) \\ &= -51.8k\ v/v \end{aligned}$$

Input Common Mode Range:

The maximum value of the common mode range is 4.4 V because we want to keep Q_1 and Q_2 operating in the active region.

$$V_{max} = 4.4V$$

$$\begin{aligned} V_{min} &= V_{BE_1} + V_{BE_2} \\ &= 0.6\ V + 0.6\ V \\ &= 1.2\ V \end{aligned}$$

Output Voltage Swing:

$$\begin{aligned} V_{max} - V_{min} &= 4.4\ V - 1.2\ V \\ &= 3.2\ V \end{aligned}$$

Capacitor Value:

In order to get the unity gain frequency f_u to be 1 MHz, the value of C_1 is determined using the following equations:

$$\begin{aligned} C_A &= C_1(1 + A_{v_2}) \\ W_p &= \frac{1}{C_A(R_{out}//R_{in})} \\ W_T &= A_o W_p \end{aligned}$$

$$\begin{aligned} C_1 &= \frac{A_o}{2\pi f_u(1 + A_{v_2})(R_{out}//R_{in}//r_{o_2})} \\ &\approx 60.23\ pf \end{aligned}$$

Slew Rate:

$$\begin{aligned} Slew\ rate &= \frac{I_{C_1}}{C_1} \\ &= \frac{19\ \mu A}{60.23\ pf} \\ &= 0.316\ V/\mu S \end{aligned}$$

3 Additional Manual Questions

1. V_{10} is the input DC voltage to the op-amp. It is used to set the differential voltage mode of the circuit. It is also used to conduct input DC voltage sweeps and input offset voltage. V_5 is used to find the common-mode input voltage which is supplied to the two input transistors Q_1 and Q_2.

2. The purpose of Q_7 and R_3 is to act as an active load for the input of the op-amp, as well as to keep the signal stable such that the gain doesn't change. Shorting the base and collector of Q_5 would cause Q_{16} to have a large base current and could possibly cause the circuit to be unstable.

3. The role of C_1 is to provide stability in the circuit and to maintain the unity-gain frequency at 1 MHz, such that a steady consistent roll-off for the circuit can occur.

4. An ideal current source would have infinite internal resistance so that 100% of the current from the current source can go to the load resistance. In a real circuit, current sources would be replaced by current mirrors. Thus, R_{in}, R_{out}, and the gain would differ from when using an ideal current source.

5. The purpose of V_2 is to provide a stable biasing voltage to Q_{14} and Q_{20}. V_2 would be implemented using 2 BJTs and a resistor.

6. The purpose of the first two stages in the circuit is to achieve a high gain. The purpose of the third stage is to have a small load resistance value such that the high gain value is maintained. Splitting the circuit into three stages makes the circuit fairly easier to analyze.

7. Assuming no input signal, the power consumption is calculated using the following euqation:

$$P = V_{CC} * I_{CC} \approx 6\ mW$$

4 Simulation

4.1 DC Sweep

After setting C_1 to the value found in the prelab, 60.23 pF, a DC sweep of the input differential voltage V_d between -10 mV to 10 mV was done.
Figure 6 below is the transfer curve for V_o versus V_d.

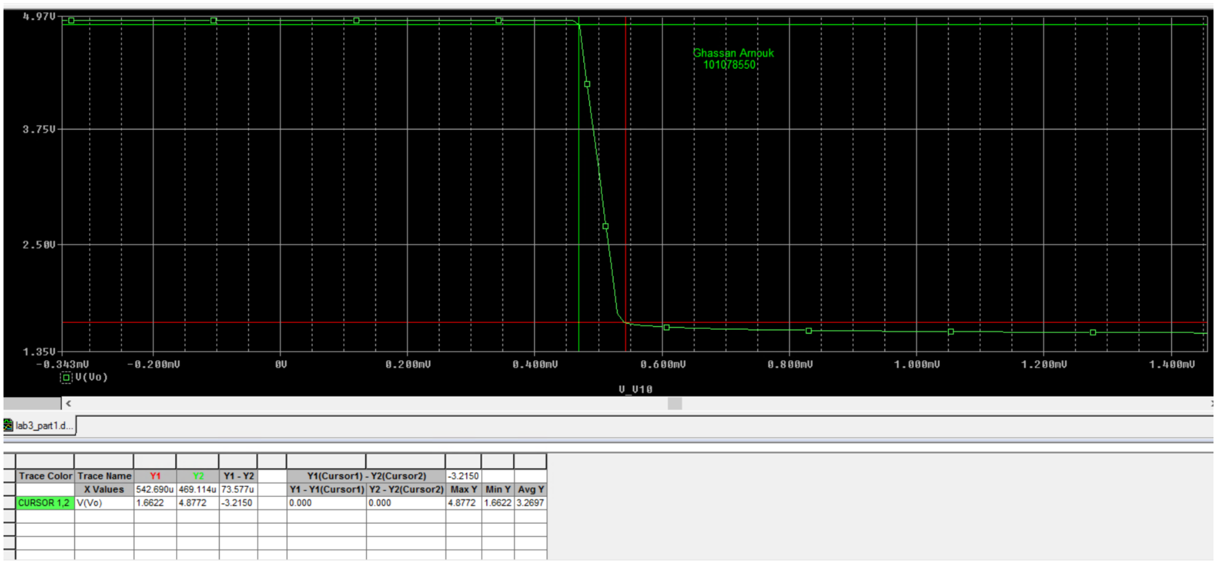


Figure 6: Transfer Curve for V_o vs. V_D

As shown in Figure 6, cursors used to find the range of the linear region. The range of the linear region is from 1.66 V to 4.87 V. The output voltage swing can be calculated as follows:

$$Output\ voltage\ swing = 4.87\ V - 1.66\ V = 3.21\ V$$

In comparison to the output voltage swing found in the prelab calculations, 3.20 V, the simulated value is very close.
The differential gain is the slope of the linear region of the transfer curve. Using the values at which the cursors were placed to determine the linear region range, the differential gain can be calculated as follows:

$$Differential\ gain = \frac{y_2 - y_1}{x_2 - x_1} = \frac{4.87\ V - 1.66\ V}{469\ \mu V - 543\ \mu V} = -43,378\ v/v$$

The total gain calculated in the prelab was found to be -51.8 kv/v. In comparison to the simulation value, the prelab value seems close to the simulated value. The difference can be attributed to the assumptions made during the calculations, such as the beta value. The difference can also be attributed to where the cursors on the simulation plot were place. Moving the cursors wihtin the linear region would yield a different differential gain value.

The input offset voltage, which is value of V_d at which V_o is 2.5 V, was found to be approximately 515 μV.

4.2 Transistor Parameters

For this part of the experiment, the transistor parameters for each transistor in the op-amp circuit were found. The simulation diagram of these parameter values are shown in Figure 12 and can be found in the Appendix.

Table 3 below illustrates a comparison between the calculated and simulated transistor parameters. As

Table 3: Calculated vs. Simulated Transistor Parameters

Transistor	I_C		g_m		r_o		β	
	Calculated	Measured (A)	Calculated	Measured (A/V)	Calculated	Measured (Ω)	Calculated	Measured
Q_1	10.35 μA	-1.03E-5	414 μA/V	3.99E-4	1.93 MΩ	1.94E+6	100	194
Q_2	10.35 μA	-1.05E-5	414 μA/V	4.04E-4	1.93 MΩ	1.90E+6	100	192
Q_5	10.15 μA	1.02E-5	406 μA/V	3.94E-4	7.9 MΩ	7.32E+6	100	79.4
Q_6	10.15 μA	1.02E-5	406 μA/V	3.94E-4	7.9 MΩ	7.33E+6	100	79.5
Q_7	12.28 mA	1.13E-5	491.2 μA/V	4.36E-4	6.5 MΩ	6.91E+6	100	83.7
Q_{14}	1.13 mA	7.57E-4	45.2 mA/V	2.89E-2	70.8 kΩ	1.00E+5	100	151
Q_{16}	19.96 μA	1.96E-5	798 μA/V	7.57E-4	4 MΩ	3.97E+6	100	91.5
Q_{17}	678 μA	6.80E-4	27.1 mA/V	2.60E-2	118 kΩ	1.09E+5	100	147
Q_{20}	1.13 mA	-7.57E-4	45.2 mA/V	2.90E-2	17.7 kΩ	2.71E+4	100	194
Q_{23}	198 μA	-1.97E-4	7.92 mA/V	7.60E-3	101 kΩ	1.00E+5	100	190

shown in Table 3 above, the majority of the calculated values are very close to the simulated values. Any discrepancies or differences in values, such as in I_C for Q_{20} can be attributed to the beta value assumed for each transistor. Each transistor's beta value is not a constant, and instead relies on the current.

The gain calculations using the measured parameter values can be shown below.

Stage 1 Gain (A_{v_1}):

$$\begin{aligned}R_{in_2} &= (\beta_{16}+1)[r_{e_{16}} + r_{o_{16}}//R_9//(r_{\pi_{17}} + R_8 + (r_{\pi_{17}})(R_8)(g_{m_{17}}))]\\ &= (91.5+1)[1321\ \Omega + 3.97\ M\Omega//50\ k\Omega//(5.65\ k\Omega + 100\ \Omega + (5.65\ k\Omega)(100\ \Omega)(0.26\ mA/V))]\\ &= 1.459\ M\Omega\end{aligned}$$

$$\begin{aligned}R_{out_1} &= r_{o_6}[1 + g_{m_6}(R_2//r_{\pi_6})] + (R_2//r_{\pi_6})\\ &= (7.33\ M\Omega)[1 + 394\ \mu A/V(1\ k\Omega//202\ k\Omega)] + (1\ k\Omega//202\ k\Omega)\\ &= 10.071\ M\Omega\end{aligned}$$

$$\begin{aligned}R_{L_1} &= R_{in_2}//R_{out_1}\\ &= 1.459\ M\Omega//10.071\ M\Omega\\ &\approx 1.247\ M\Omega\end{aligned}$$

$$\begin{aligned}A_{v_1} &= \frac{v_L}{v_{in}}\\ &= g_{m_2}(R_{L_1}//r_{o_6}//r_{o_2})\\ &= 404\ \mu A/V(1.247\ M\Omega//7.33\ M\Omega//1.90\ M\Omega)\end{aligned}$$

$$\therefore A_{v_1} = 279.07\ v/v$$

Stage 2 Gain (A_{v_2}):

$$\begin{aligned}A_{v_2} &= \frac{v_{out}}{v_{in}} \\ &= \frac{v_{out}}{v_{\pi_{17}}} * \frac{v_{\pi_{17}}}{v_{b_{17}}} * \frac{v_{b_{17}}}{v_{in}}\end{aligned}$$

$$\begin{aligned}\frac{v_{out}}{v_{\pi_{17}}} &= (-g_{m_{17}})(R_{L_2}//R_{12}) \\ &= (-26\ mA/V)(R_{L_2}//30\ k\Omega)\end{aligned}$$

$$\begin{aligned}\frac{v_{\pi_{17}}}{v_{b_{17}}} &= \frac{r_{\pi_{17}}}{r_{\pi_{17}} + R_8(1+\beta)} \\ &= \frac{5.63\ k\Omega}{5.63\ k\Omega + (100\ \Omega)(1+147)} \\ &= 0.2756\ v/v\end{aligned}$$

Define $r'_{\pi_{17}}$ as follows:

$$\begin{aligned}r'_{\pi_{17}} &= r_{\pi_{17}} + R_8(1+\beta) \\ &= 5.63\ k\Omega + (1+147)(100\ \Omega) \\ &= 20.43\ k\Omega\end{aligned}$$

$$\begin{aligned}\frac{v_{b_{17}}}{v_{in}} &= \frac{(1+\beta)[r_{o_{16}}//R_9//r'_{\pi_{17}}]}{(1+\beta)[r_{o_{16}}//R_9//r'_{\pi_{17}}] + r_{e_{16}}(1+\beta)} \\ &= \frac{(1+91.5)[3.97\ M\Omega//50\ k\Omega//20.43\ k\Omega]}{(1+91.5)[3.97\ M\Omega//50\ k\Omega//20.43\ k\Omega] + (1321\ \Omega)(1+91.5)} \\ &= 0.9162\ v/v\end{aligned}$$

The input impedance of the third stage is calculated as follows:

$$\begin{aligned}R_{in_3} &= r_{e_{23}}(1+\beta_{23}) + (1+\beta_{23})[(1+\beta_{14})[R_{10} + (r_{e_{14}} + R_6)//(r_{e_{20}} + R_7)]//R_{13}] \\ &= (131.58\ \Omega)(1+190) + (1+190)[(1+151)[1\ M\Omega + (60.6\ \Omega//64.48\ \Omega)]//90\ k\Omega] \\ &\approx 17.205\ M\Omega\end{aligned}$$

In this stage, R_{L_2} is equivalent to R_{in_3}

$$\therefore R_{L_2} = 17.205\ M\Omega$$

$$\begin{aligned}\frac{v_{out}}{v_{\pi_{17}}} &= (-g_{m_{17}})(R_{L_2}//R_{12}) \\ &= (-26\ mA/V)(17.205\ M\Omega//30\ k\Omega) \\ &= -778.64\ v/v\end{aligned}$$

Therefore, the gain for the second stage is:

$$A_{v_2} = (-778.64)(0.2756)(0.9162)$$

$$\therefore A_{v_2} = -196.60\ v/v$$

Stage 3 Gain (A_{v_3})

$$
\begin{aligned}
A_{v_3} &= \left[\frac{R_{10}}{R_{10} + (r_{e_{14}} + R_6)//(r_{e_{20}} + R_7)}\right]\left[\frac{(1+\beta_{14})[R_{10} + [(r_{e_{16}} + R_6)//(r_{e_{20}} + R_7)//R_{13}]]}{r_{e_{23}} + (1+\beta_{14})[R_{10} + [(r_{e_{16}} + R_6)//(r_{e_{20}} + R_7)//R_{13}]]}\right] \\
&= \left[\frac{1\ M\Omega}{1\ M\Omega + (64.6\ \Omega)//(64.48\ \Omega)}\right] * \\
&\quad \left[\frac{(1+151)[1\ M\Omega + [(64.6\ \Omega)//(64.48\ \Omega)//90\ k\Omega]]}{131.58\ \Omega + (1+151)[1\ M\Omega + [(64.6\ \Omega)//(64.48\ \Omega)//90\ k\Omega]]}\right]
\end{aligned}
$$

$$\therefore A_{v_3} = 0.9999 \approx 1\ v/v$$

Total Gain (G_v):

Therefore, the total gain of the 741 operational amplifier can be calculated as follows:

$$
\begin{aligned}
G_v &= A_{v_1} * A_{v_2} * A_{v_3} \\
&= (279.07)(-196.60)(0.9999) \\
&= -54,864\ v/v
\end{aligned}
$$

As shown in Table 4, the gain values from the prelab come very close to the gain values using the simulation

Table 4: Prelab vs. Simulated Voltage Gains

Stage Gain	Prelab Gain	Simulated Gain
A_{v_1}	266.16 v/v	279.07 v/v
A_{v_2}	-194.65 v/v	-196.60 v/v
A_{v_3}	0.9999 v/v	0.99997 v/v
G_v	-51,800 v/v	-54,863 v/v

determined parameters. The difference between the gains can again be attributed mainly to the different beta values determined by the simulation. They make significant differences when used in the calculations. Also, in the simulation, I_B is not assumed to be zero. In the prelab, I_B was assumed to be zero in order to ease the calculations. The accuracy of the calculations in the prelab are less when compared to the simulated results. This is due to the fact that assumptions were made when doing the prelab calculations, whereas the simulation is very accurate in its data.

4.3 DC Sweep from 0V to 5V

Another DC sweep was done, set from 0 V to 5 V, and the differential voltage V_d was set to the input offset voltage, which in this case was approximately 515 μV.
The transfer curve of V_o vs. V_{cm} is shown in Figure 7 below.

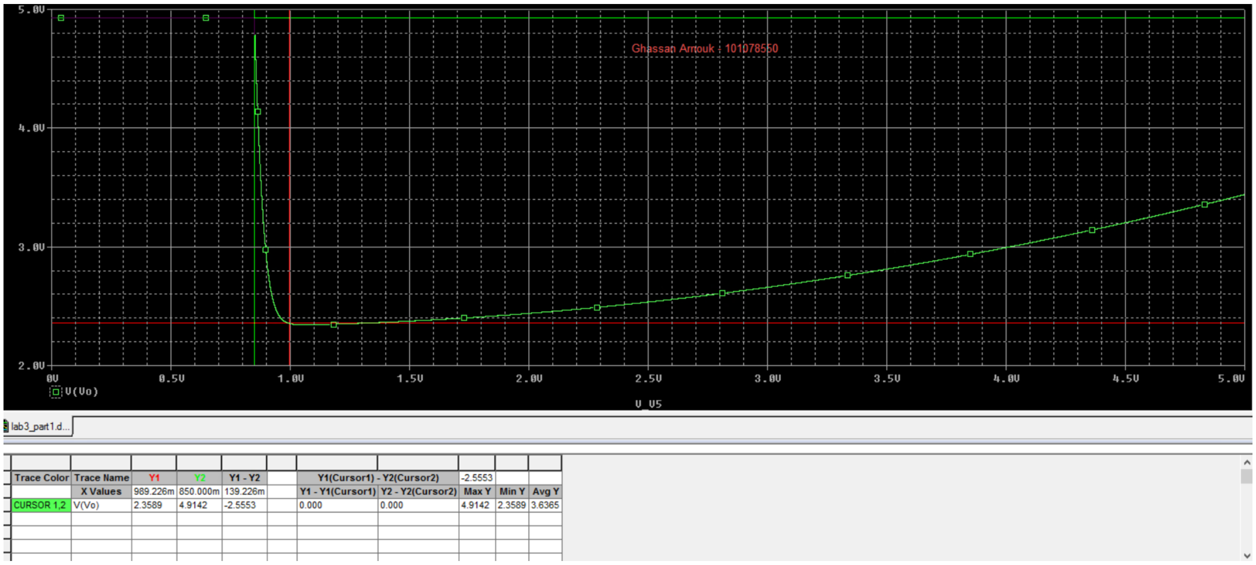
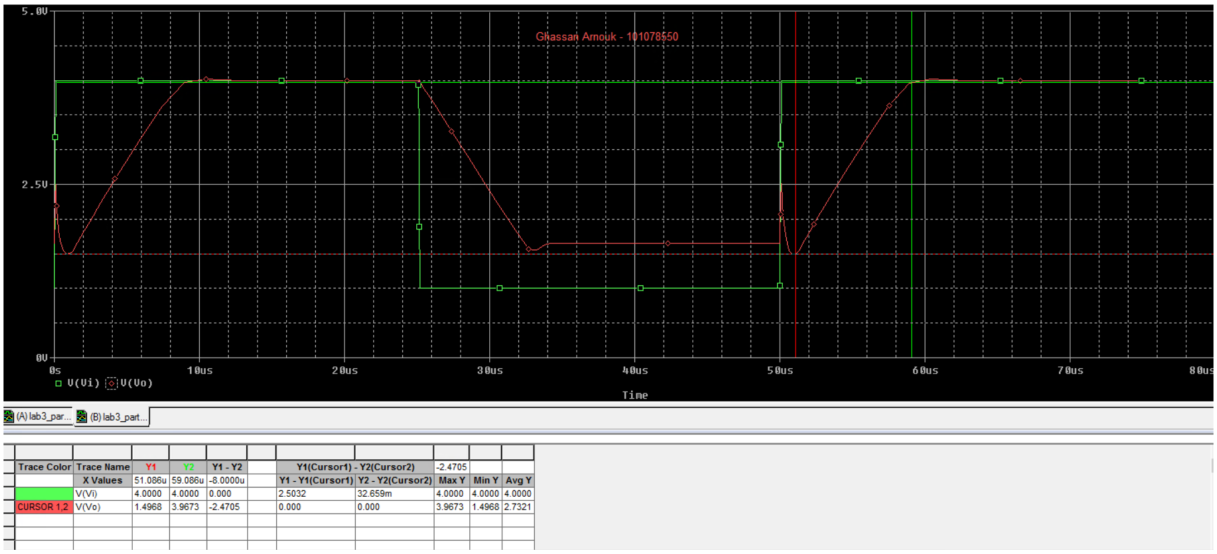


Figure 7: Transfer Curve of V_o vs. V_{cm}

As shown in Figure 7, the common-mode range starts from 1 V and progresses onwards to 5 V. Due to the fact that 5 V is the maximum value for the sweep, the plot cannot go any further. This range is expected and is very close to the common-mode range determined in the prelab.

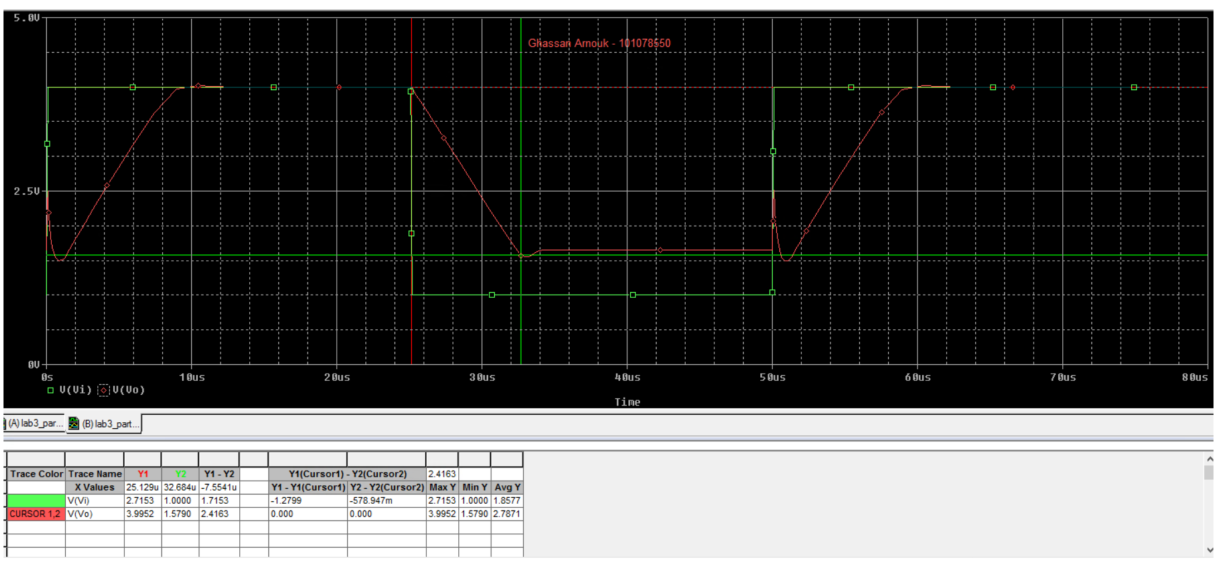
4.4 Slew Rate

The maximum rate-of-change of the output voltage is known as the slew rate. In order to measure it, the op-amp is set to the unity-gain voltage-follower configuration. The positive and negative slew rates are shown in the input and output transient voltage waveforms in Figure 8 and Figure 9 below.
Figure 8 illustrates the use of cursors to measure the positive slew rate while Figure 9 illustrates the use of cursors to measure the negative slew rate.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-2.4705		
	X Values	51.086u	59.086u	-8.0000u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(Vi)	4.0000	4.0000	0.000		2.5032	32.659m	4.0000	4.0000	4.0000
CURSOR 1,2	V(Vo)	1.4968	3.9673	-2.4705		0.000	0.000	3.9673	1.4968	2.7321

Figure 8: Positive Slew Rate Transient Waveform



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		2.4163		
	X Values	25.129u	32.684u	-7.5541u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(Vi)	2.7153	1.0000	1.7153		-1.2799	-578.947m	2.7153	1.0000	1.8577
CURSOR 1,2	V(Vo)	3.9952	1.5790	2.4163		0.000	0.000	3.9952	1.5790	2.7871

Figure 9: Negative Slew Rate Transient Waveform

As shown in Figure 8 and Figure 9, the cursors are used to determine the range over which the positive and negative slew rates can be found respectively.
The positive and negative slew rate calculations can be done as follows:

$$\begin{aligned} Positive\ slew\ rate &= \frac{\Delta y}{\Delta x} \\ &= \frac{-2.4705\ V}{-8.0\ \mu\,\text{sec}} \\ &\approx 0.309\ V/\mu\,\text{sec} \end{aligned}$$

$$\begin{aligned} Negative\ slew\ rate &= \frac{\Delta y}{\Delta x} \\ &= \frac{2.4163\ V}{-7.5541\ \mu\,\text{sec}} \\ &\approx -0.319\ V/\mu\,\text{sec} \end{aligned}$$

In comparison between the value of the slew rate determined in the prelab, 0.316 $V/\mu\,\text{sec}$, and calculated one, it is shown that the values are very close. Thus, the prelab calculations were done correctly and the correct capacitor value was chosen.

4.5 Frequency Response

In this part of the experiment, an AC sweep was done from 1 Hz to 10 MHz and Figure 10 below shows the plot of the magnitude and phase, top and bottom respectively.

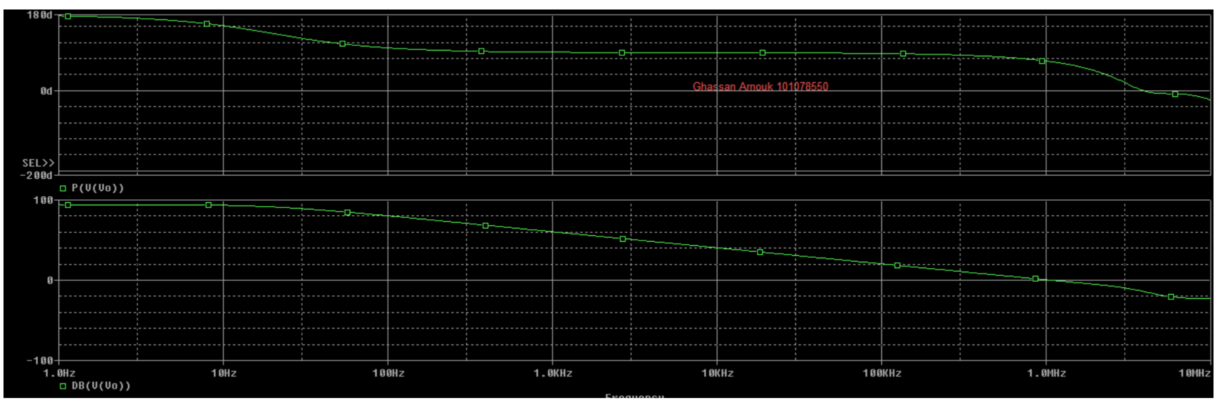


Figure 10: Magnitude and Phase Response Plots of the 741 Op-Amp Circuit

In order to determine the unit gain frequency f_u, the magnitude response was zoomed into to determine at what frequency the plot crosses zero on the y-axis as shown in Figure 11.

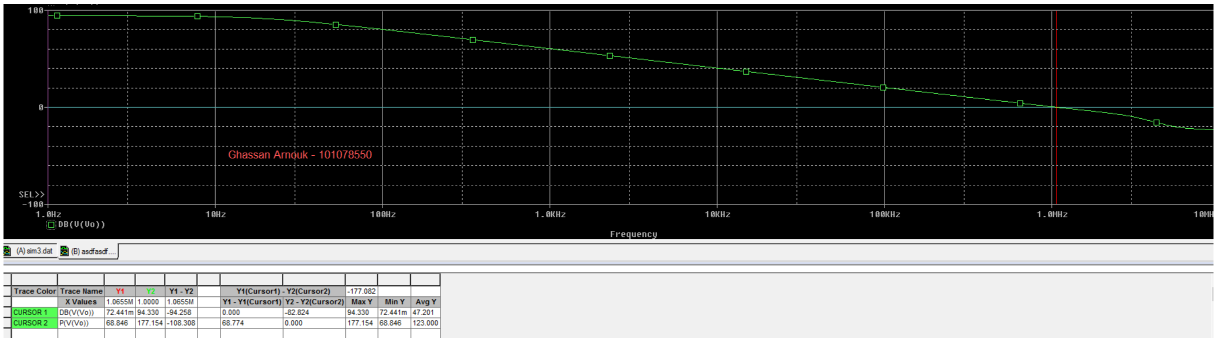


Figure 11: Zoomed in Magnitude Response Plot

Using the cursors in Figure 11, it is seen that the unity gain frequency is 1.0655 MHz. In comparison to the 1 MHz value found in the prelab, the simulated value is very close. This plot confirms that the capacitor value chosen from the prelab is correct.

5 Conclusion

This lab allowed us to analyze the 741 op-amp in detail. We were able to calculate and determine the calculated and simulated op-amp's transistor parameters. As well, We were able to determine various factors of the op-amp, such as the common-mode range and the slew rate. We were also able to observe the magnitude at which this op-amp can amplify signals. Finally, this lab allowed us to get hands on experience with the simulation software, which will be very useful in further academic and professional endeavours.

6 References

[1] "Lab 3: 741 Op-Amp," Carleton Univeristy, Ottawa, 2017.

7 Appendix

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q14	Q_Q20	Q_Q23	Q_Q17	Q_Q16
MODEL	Q2N3904	Q2N3906	Q2N3906	Q2N3904	Q2N3904
IB	5.79E-06	-3.86E-06	-1.03E-06	5.36E-06	2.58E-07
IC	7.57E-04	-7.57E-04	-1.97E-04	6.80E-04	1.96E-05
VBE	6.58E-01	-6.96E-01	-6.62E-01	6.56E-01	5.62E-01
VBC	-1.82E+00	1.78E+00	1.12E+00	-3.96E-01	-3.71E+00
VCE	2.48E+00	-2.48E+00	-1.78E+00	1.05E+00	4.28E+00
BETADC	1.31E+02	1.96E+02	1.91E+02	1.27E+02	7.60E+01
GM	2.89E-02	2.90E-02	7.60E-03	2.60E-02	7.57E-04
RPI	5.21E+03	6.71E+03	2.51E+04	5.63E+03	1.21E+05
RX	1.00E+01	1.00E+01	1.00E+01	1.00E+01	1.00E+01
RO	1.00E+05	2.71E+04	1.00E+05	1.09E+05	3.97E+06
CBE	1.52E-11	1.89E-11	1.47E-11	1.43E-11	6.30E-12
CBC	2.49E-12	4.82E-12	5.74E-12	3.19E-12	2.10E-12
CJS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
BETAAC	1.51E+02	1.94E+02	1.90E+02	1.47E+02	9.15E+01
CBX/CBX2	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
FT/FT2	2.61E+08	1.95E+08	5.92E+07	2.37E+08	1.43E+07

NAME	Q_Q1	Q_Q2	Q_Q7	Q_Q5	Q_Q6
MODEL	Q2N3906	Q2N3906	Q2N3904	Q2N3904	Q2N3904
IB	-5.33E-08	-5.44E-08	1.63E-07	1.55E-07	1.55E-07
IC	-1.03E-05	-1.05E-05	1.13E-05	1.02E-05	1.02E-05
VBE	-5.86E-01	-5.86E-01	5.48E-01	5.47E-01	5.46E-01
VBC	1.40E+00	1.21E+00	-3.90E+00	-5.48E-01	-7.30E-01
VCE	-1.98E+00	-1.80E+00	4.44E+00	1.09E+00	1.28E+00
BETADC	1.94E+02	1.92E+02	6.93E+01	6.56E+01	6.58E+01
GM	3.99E-04	4.04E-04	4.36E-04	3.94E-04	3.94E-04
RPI	4.85E+05	4.76E+05	1.92E+05	2.02E+05	2.02E+05
RX	1.00E+01	1.00E+01	1.00E+01	1.00E+01	1.00E+01
RO	1.94E+06	1.90E+06	6.91E+06	7.32E+06	7.33E+06
CBE	1.26E-11	1.26E-11	6.15E-12	6.13E-12	6.13E-12
CBC	5.30E-12	5.58E-12	2.07E-12	3.07E-12	2.95E-12
CJS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
BETAAC	1.94E+02	1.92E+02	8.37E+01	7.94E+01	7.95E+01
CBX/CBX2	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
FT/FT2	3.55E+06	3.53E+06	8.44E+06	6.80E+06	6.91E+06

Figure 12: Simulated Transistor Parameters