ROM-Based Finite State Machine

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Lab 1 Report
Group 1

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1 Discussion Questions

1.1 What is the minimum ROM Address Bit Width needed to implement Table 1, and why?

If the number of address bits is m, then the ideal number of words in the bank would be 2^m. Therefore, the minimum number of bits needed to store eight states is **three** ($2^3 = 8$) bits.

1.2 What is the minimum ROM Data Bit Width needed to implement Table 1, and why?

The minimum ROM Data Bit Width is **six** since three bits are necessary to store the three bits of the output (O2,O1,O0), and three more bits are necessary to store the Next State. The tables have eight bits to store the data but the two most significant bits are zeros and can be ignored.

1.3 Fill in the following table; it is the content of your FSM ROM that you are going to implement.

Table 1: Content of the FSM ROM

Address	DATA content (binary)	DATA content (Hex)
0	0010 0011	23
1	0001 1100	1c
2	0000 0000	00
3	0011 0101	35
4	0000 1010	0a
5	0011 1111	3f
6	0000 0110	06
7	0011 1001	39

1.4 Show here a screenshot of your final Logisim circuit for your implementation.

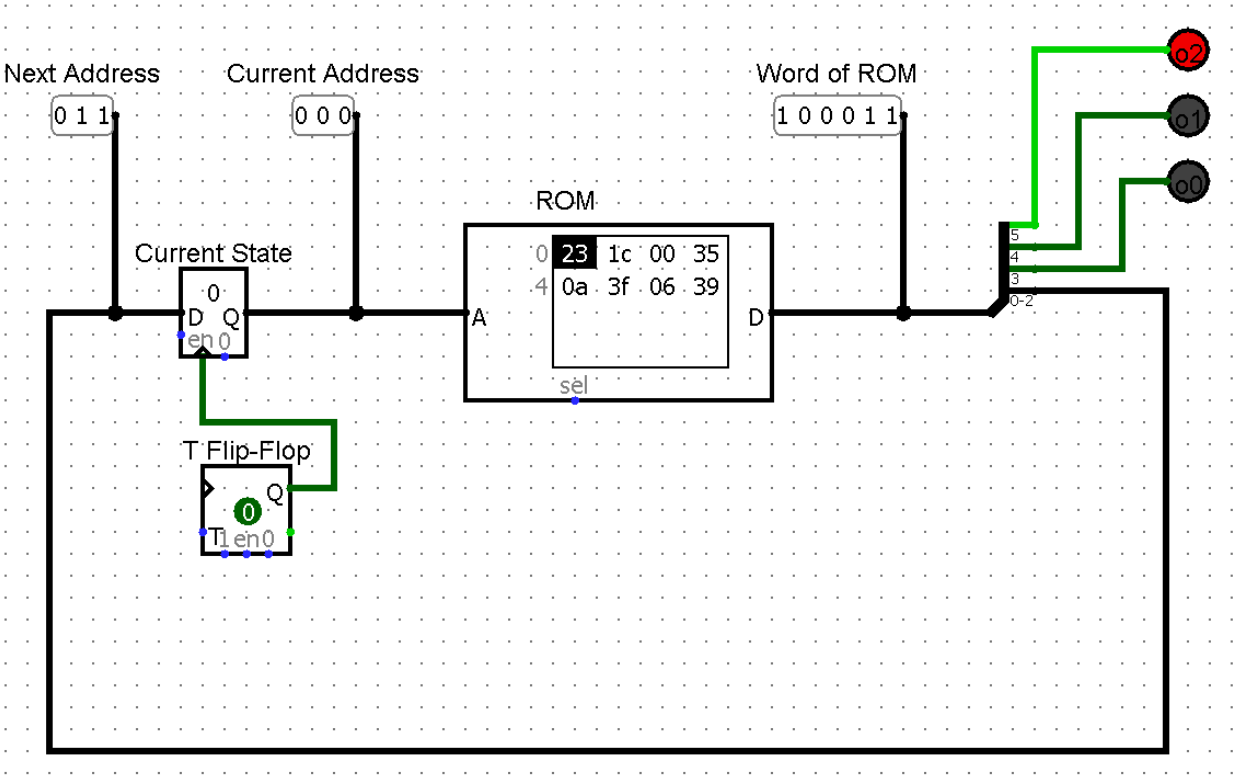

Figure 1: ROM Circuit Implementation

1.4.1 A short description of how the component attributes have been configured to meet the lab requirements.

- Toggle Switch: used as a clock input to the Current State Register and is manually toggled to go to the Next State
- Register: added as an input to the ROM to hold the Current State and is triggered on the fallingedge of the clock
- ROM: contains the content of eight words. The current state is the address of a word in ROM. For example, state 2 corresponds to the word with address 2 in ROM. It is worth mentioning that state 6 forks a child state of its own
- Splitter: at the output of the ROM, a splitter is used to split the data into one bundle and three wires:
  - a bundle with bits (b2,b1,b0) for the Next state
  - three separate wires for three outputs (o2,o1,o0)
- LEDs: three LEDs are added at the three outputs and the lamps light up when the corresponding output is 1.

1.4.2 Insert below a screenshot of your Log table (0.5-mark for the Log table and 1.5-mark for a circuit working properly and respecting the design specifications described in this statement).

Table 2: Simulation Log Table of the ROM-Based FSM Circuit

Current State	o2	o1	o0
000	1	0	0
011	1	1	0
101	1	1	1
111	1	1	1
001	0	1	1
100	0	0	1
010	0	0	0
000	1	0	0
011	1	1	0
101	1	1	1