Lab 2: Amplifier Project

Schedule for This Lab:

Day 1: Single-transistor and 2-transistor amplifiers
Day 2: Present your Cascode Amplifier design to the TA and build/test your circuit
Day 3: Continuation of week 2. Your amplifier should be working by the start of this period so that you can demonstrate it to the TAs.

The report should discuss all of the results including Day 1. You must discuss your design and show the complete process and results.

Purpose:

The purpose of this laboratory is to investigate the use of BJTs as amplifier circuit elements. First, the three basic configurations (CE, CC and CB) are observed. Then, by proper combinations and permutations, 2-transistor amplifier configurations can be studied for improved gain-bandwidth performance. Finally, a specific configuration is required to be designed to meet or exceed a prescribed set of specifications.

Introduction:

Before starting this project, read the relevant class notes, and the sections of this laboratory outline dealing with design approaches.

Day 1: Single Transistor amplifiers and Two-Transistor Amplifiers

You will be constructing and measuring 3 different single amplifier configurations and 3 different two-transistor configurations. Your results should help you identify the strengths and weaknesses of each one. Note that while it is mandatory to do the prelab for day 1 prior to coming in to the lab, you are strongly suggested to do the prelab for the day 2 as well, as it is long and intensive.

Part 1: Circuit Construction and D.C. Measurements

Construct the circuit shown in Figure 2.1. This circuit contains 3 separate amplifiers (you need to build all 3 at the same time on the same board). As you will be making high frequency measurements, you should keep your circuits neat and clean with as short wires as possible.

Tip: Assembling this circuit BEFORE your lab will save you a lot of time.

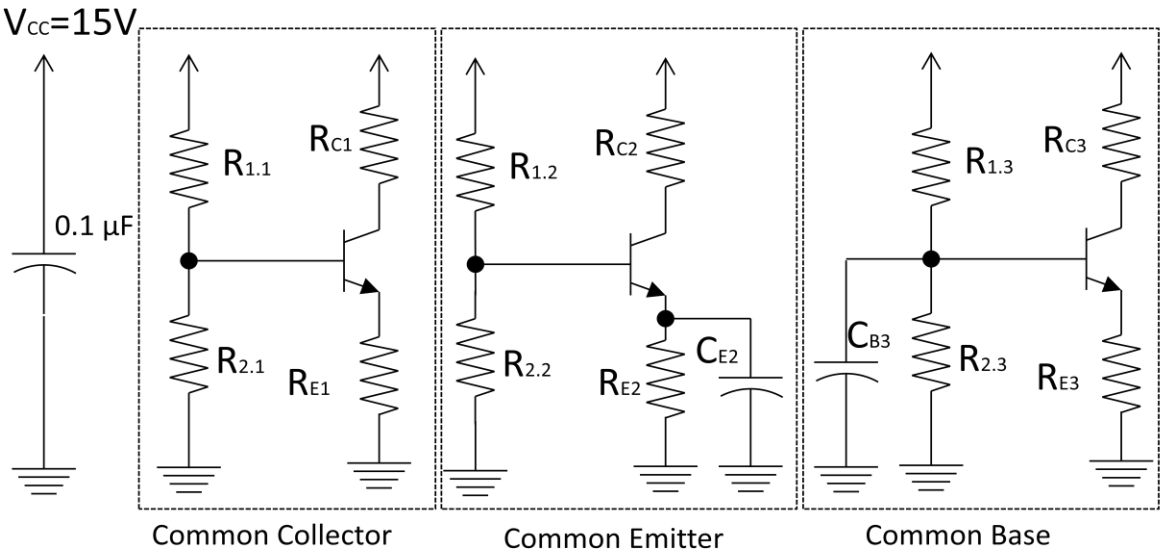

Figure 2.1 Schematic showing the 3 single transistor amplifiers

The component values are as follows (i.e. R1.1=R1.2=R1.3=100kΩ):

Component (CC)	Component (CE)	Component (CB)	Component value
$R_{1.1}$	$R_{1.2}$	$R_{1.3}$	100 kΩ
$R_{2.1}$	$R_{2.2}$	$R_{2.3}$	39 kΩ
R_{C1}	R_{C2}	R_{C3}	5.6 kΩ
R_{E1}	R_{E2}	R_{E3}	3.3 kΩ
	C_{E2}		100 µF
		C_{B3}	1 µF

Note: R_{C1} is to be present when verifying the DC operating point. However, when performing your AC measurements, it is to be shorted out.

Experiment:

- Build the D.C. bias network (Fig. 2.1) on your circuit board. Your layout should be neat and compact such that access to the three terminals (E, B and C) of each transistor can be made easily. Measure all resistors before connecting the circuit to the bench supply.
- For every transistor, take D.C. measurements of all relevant voltages (V_B, V_E, V_C and V_{CC}). Determine the terminal currents from the following relationships:

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$I_E = \frac{V_E}{R_E}$$

$$I_B = I_{R1} - I_{R2} = \frac{V_{CC} - V_B}{R_1} - \frac{V_B}{R_2}$$

Note that I_B is calculated by subtracting two large values that are very similar, and so the error will be large if you are not accurate. Check if $I_E \approx I_B + I_C$ and determine the DC value of β by calculating $\frac{I_C}{I_B}$

- Define the "AC ground" node of the three transistors as follows:
  - The first transistor is to be connected as a common-collector amplifier. Thus, the collector

should be by-passed to ground either by a capacitor, or, by replacing R_{C1} with a short-circuit to V_{CC}.

- The second transistor is to be connected as a common-emitter amplifier by connecting a large value (100μF) capacitor C_{E2} from E2 to ground.
- The third transistor is to be connected as a common-base amplifier by connecting a capacitor C_{B3} ($C_{B3} \geq 1$ μF) from B3 to ground.

Report:
Briefly summarize the results you have obtained here. Answer the following questions:

- Why can R_{C1} be made 0 when testing the amplifier? Why do you need to have it when checking the DC operating point?
- Could we instead use a capacitor like we do for the CE and CB amplifiers?
- Why do we need R_{E2}? Why can't we just short this node to ground?

Part 2: AC Measurements for Single-Transistor Amplifiers

Pre-lab:
Using the formulas in the notes, **identify the expected gain, input and output impedance, and high/low frequency cut-off points of each amplifier** (this is a lot of work so plan accordingly). For component parameters, use the values you measured in lab 1, or make reasonable assumptions.

For each amplifier, a 3.3 kΩ resistor is placed at the series of the input, and the source impedance of the generator is 50 Ω. The load impedances and the coupling capacitors can be seen in Figure 2.2 and Figure 2.3.

Experiment:

- Connect the following network (seen in Figure 2.2) to the far left of the circuit board to provide a low impedance AC signal source with low signal amplitude. This circuit is needed since the minimum output amplitude of the signal generator is not low enough for the purposes of this lab.

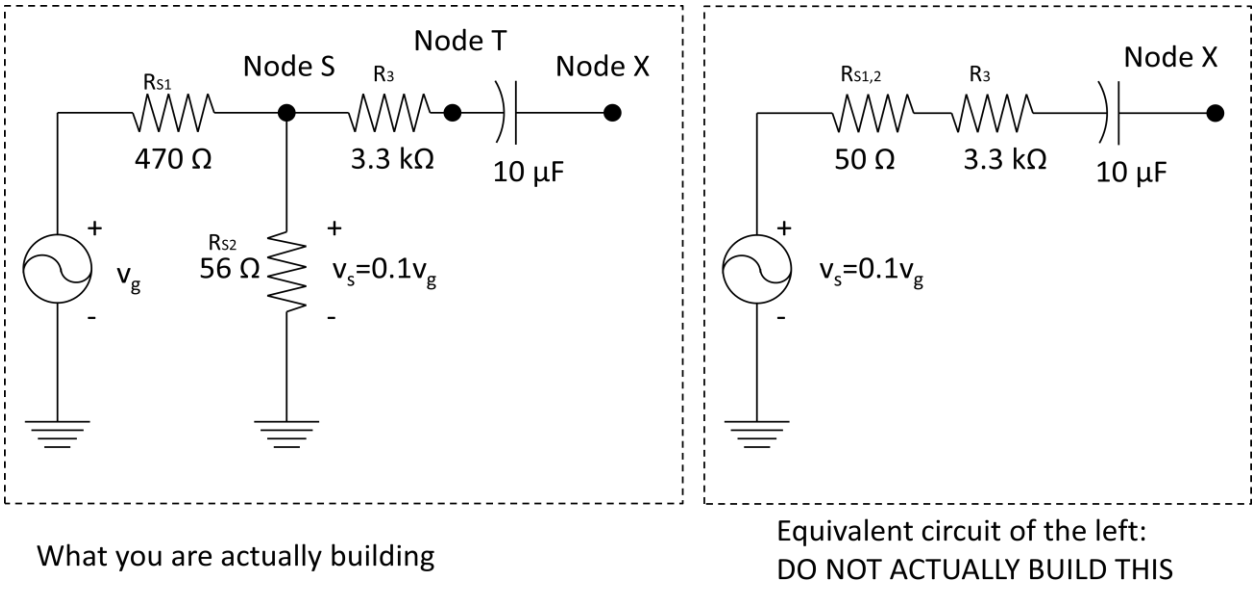

Figure 2.2 Schematic and equivalent circuit of amplifier test circuit.

- Connect the following network seen in Figure 2.3 to the far right of the circuit board to provide an

AC load. The jumper is a small piece of wire that can be easily removed. When it is removed, the load removed is removed from the circuit.

- Remove any DC offsets from the measurements by setting the scope to AC coupling (Vertical > Menu > Coupling > AC).

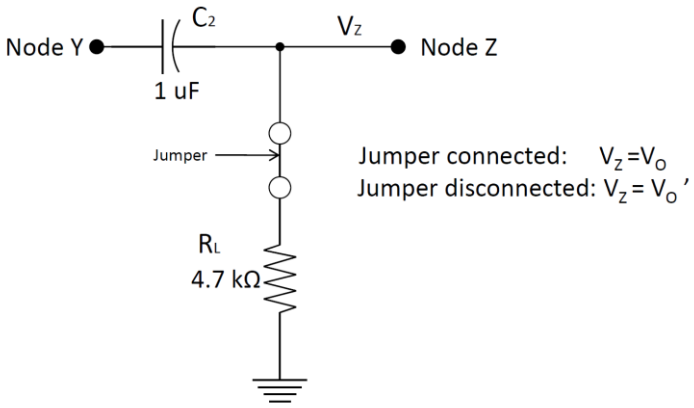

Figure 2.3 Schematic of load test module

Oscilloscope Measurements: Be wary of using the scope's built-in "measure" function to display any values (i.e. peak-to-peak voltage). If your signal is noisy or untriggered, the values will be inaccurate. Make sure that you have a clean signal with multiple wavelengths displayed before trusting these numbers. To be safe **use your cursors (cursor -> horizontal bars)** and manually measure the peak to peak voltages.

- **CE Amplifier**:
  - Connect the low-amplitude source to the input of the CE amplifier (i.e. node X to the base of the CE). Then connect the output to the load (collector of the CE to node Y).
  - Attach oscilloscope probes to monitor v_Z (at node Z). Since the jumper is connected, v_Z is v_O. Set the signal frequency to 1kHz and adjust the output level (amplitude) of the signal generator until v_o shows an output peak-to-peak swing of 2 volts.
  - Measure the peak-to-peak values of v_s-v_X (using the 2 channel method described in Lab 1) and v_s.
  - Measure v_o' by disconnecting the jumper.
  - Determine R_{in}, R_{out} and A_{mid} using the following relationships.

$$R_{in} = R_3 + R_{inA} = R_3 + \frac{v_x}{i_{R3}}$$

$$R_{out} = \frac{v_O' - v_O}{i_{RL}}$$

$$A_{mid} = \frac{v_O}{v_S}$$

  - Next, we wish to find the **high frequency cutoff** point of this circuit by finding where the gain drops by 3 dB. Reconnect R_L and observe v_o and v_s. Increase the frequency of the signal generator until v_o drops to 1.4 volts peak-to-peak. Ensure that the value of v_s remains constant. If it decreases or increases with frequency, adjust the signal generator to maintain the same value. This frequency is the upper cutoff (or 3dB) frequency, f_H, of the amplifier. Next, decrease the frequency of the signal source until, again, v_o drops to 1.4 volts peak-to-peak (again keeping v_s constant) to obtain the **lower cutoff frequency**, f_L, of the amplifier.

- **CC Amplifier**
  - Connect the input circuit (node X) to the input of the CC amplifier (the base of the CC). Then connect the output (emitter of the CC) to the load circuit (node Y). Move the signal generator output **directly to node S** instead of through the 470Ω resistor. Set a 2 V p-p signal at the output. You may have to use the "HI" output of the signal generator.
  - Repeat the previous steps to get R_{in}, R_{out}, A_{mid}, f_H and f_L of the CC amplifier.

- **CB Amplifier**
  - Connect the input circuit (node X) to the input of the CB amplifier (emitter of the CB). Then connect the output (collector of the CB) to the load circuit (node Y). Keep the Wavetek output connection to node S. Set a 2 V p-p signal at the output. You may have to use the "HI" output of the Wavetek generator.
  - Repeat the previous steps to get R_{in}, R_{out}, A_{mid}, f_H and f_L of the CB amplifier.

Report:
Show a complete table summarizing the values of calculated and measured of R_{in}, R_{out}, A_{mid}, f_H and f_L for all 3 amplifiers. Comment on any differences you see between measured and calculated values. Explain any differences you see. Try to be as specific as possible.

Recall that some of the AC measurements you made were probably not very accurate. Identify those as a starting point. Comment on the differences between all 3 amplifiers. Mathematically explain any differences you see: for instance if one amplifier has a higher gain, explain why that is so. Which ones are better for which tasks and why?

Part 3: 2-transistor Amplifiers

In addition to the input signal coupling network and the output loading network, you will need an AC coupling capacitor to connect from the first transistor to the second one. Since the large value capacitor is usually of the polarized type (electrolytic), make sure that you observe the polarity of the capacitor when connecting it to the circuit.

Pre-lab:
- For each of 2-transistor amplifiers you will test in the section below, qualitatively estimate what you expect their properties to be (eg. R_{in}, R_{out}, A_{mid}, f_H and f_L). Feel free to do a full analysis here if you like, as you will need to do that for the report anyway.

Experiment:
- **CE-CB Amplifier**
  Connect the input circuit (node X) to the input of the common emitter (base). Connect the CE output (collector) to the **positive side** of the coupling capacitor (≥22μF) and negative side to the input of the common base (emitter). Finally connect the output (collector of CB) to node Y. Now repeat all AC measurements to get the amplifier's parameters to get to get R_{in}, R_{out}, A_{mid}, f_H and f_L.

- **CC-CB Amplifier**
  Connect the input circuit (node X) to the input of the common collector (base). Connect the CC output (emitter) through the coupling capacitor to the input of the CB (emitter). The output of the CB should still be connected to the load from before. Repeat all measurements to get to get R_{in}, R_{out}, A_{mid}, f_H and f_L.

- **CC-CE Amplifier**

Keep the input connected to the CC. Connect the output of the common collector (emitter) to the minus side of the coupling capacitor, the plus side of the coupling capacitor to the input of the CE (base). Connect Collector 2 to node Y. Repeat all measurements to get to get R_{in}, R_{out}, A_{mid}, f_H and f_L.

Report:
Include a table summarizing the measured values of R_{in}, A_{mid}, f_H and f_L. **Calculate expected values** for these and compare them. Like with the 1 transistor amplifiers, explain any differences between the two set of values.

Comment on the differences between all three 2-transistor amplifiers. Like you did for the previous section, explain any differences in performance. Which ones are better for which tasks and why?

In weeks 2 & 3 you will be designing a cascode amplifier, a variation on the CE-CB amplifier. Identify what advantages this has over any of the single transistor amplifiers you tested. What are the advantages and disadvantages of using the cascode topology over any of the 2-transistor topologies you just tested?

Design Project for Days 2 and 3

During the remaining two weeks of the lab period you are expected to design the Cascode amplifier similar to Figure 2.4. You will assemble and test your circuit to verify that it meets the expected requirements.

The onus for correctness in the design is on the student. The TAs are there to help you, but not to do your design for you. You want to have your design ready for Day 2. Your amplifier should be working by the start of Day 3 so that the TAs may check out all students before the end of the period.

Cascode Amplifier Requirements:

You will need to design a cascode amplifier, which should be built and tested to meet the following requirements:

1. Magnitude of the voltage gain = 12*SQRT(Z+35):± 10%, where Z is the sum of the last 3 digits of your student number.
2. The load resistance $R_L = 6*(Z+40)^2$, rounded up to the nearest standard value stocked in the lab, i.e., decade multiples of 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, and 8.2 kΩ.
3. The high frequency cutoff f_H is to be maximized. **It must exceed 1 MHz.**
4. The output voltage should be able to get to 2 V peak-peak without appreciable distortion*. To ensure this, the AC base-emitter voltage must be kept under 10 mV peak-peak for such an output.
5. No DC current may flow in R_L and no DC current may flow into or out of the signal generator.
6. The low frequency f_L must be less than 200 Hz.
7. The input and output impedances are left to the discretion of the designer, but their magnitudes at 1 kHz are to be determined by calculation and then measured.
8. Total circuit power is not to exceed 50 mW.
9. The transistors are all to be 2N3904.
10. Collector currents in the transistors are to be 1.0 mA ±10%.
11. Power-supply voltages are to be limited to +5 volts and/or +15 volts and/or -15 volts.
12. No adjustable components, e.g. trim-pots, will be allowed.
13. The choice of all other components is left up to the designer.

* Many students have a hard time deciphering if their signal is distorted or not. Your input is a sine wave and your output should also be a sine wave. Distortion can be obvious (jagged edges, clipping) or more subtle (rounder peaks compared to valleys).

Design Approach- to be done by days 2-3:

There is no unique solution to the amplifier design problem that has been laid out. There are more variables in the circuit than there are design parameters that have to be met. Consequently, a design solution requires the fixing of some of the unspecified degrees of freedom in the circuit in order to begin to solve the problem. In almost all cases the solution requires iteration because the choices made to optimize one design parameter will often impact negatively on the other parameters.

In the Appendix an example design approach is presented for a single-stage common-emitter amplifier, along with many of the assumptions and approximations that are usually made in making the problem tractable. Much of what will be presented will provide insight into the design of the project amplifier, and indeed, much of it can be directly applied, or modified to suit. The course notes should also provide significant insight as to how to start your design.

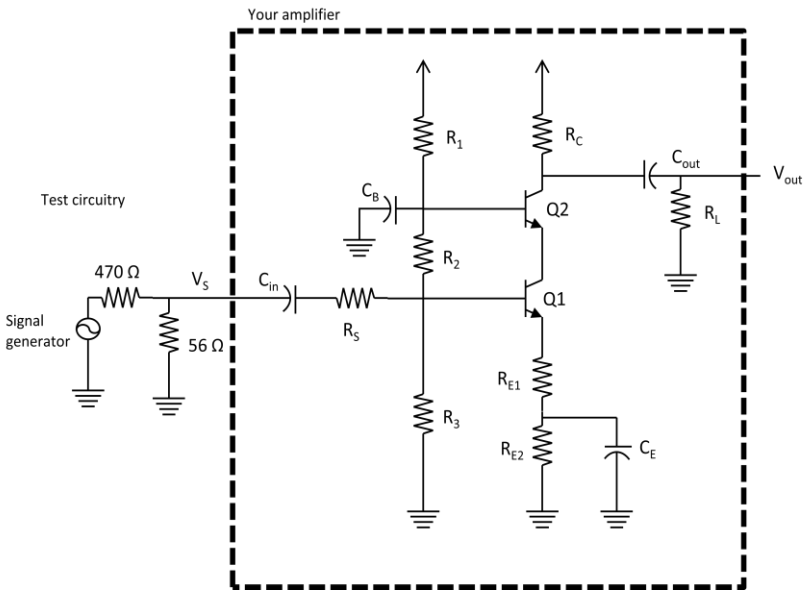

Figure 2.4 Schematic of cascode amplifier

Figure 2.4 shows an example schematic. The signal generator will likely need a voltage divider in order to get a small enough input signal, but is not actually part of your circuit. R_S and R_{E1} are used to reduce the gain which is needed, due to the large value of R_C need to maintain a small AC V_{BE}. You don't need both of them, but you will need one or the other.

ADDITIONAL DESIGN PRACTICES FOR TWO-TRANSISTOR AMPLIFIERS:

The following short list of practices is intended to give a starting point for setting some of the additional parameters found in two-transistor amplifiers.

1. Set the collector currents of the transistors to the same value unless there is good reason not to.
2. A single base-bias network is used to provide the base currents for two transistors. Set the bias network current to be about 10 times the sum of the two transistor's base currents.
3. For the cascode configuration, it is reasonable to initially allot 0.1 to 0.3 of the V_{CC} supply voltage to R_E, 2 to 3 volts to the V_{CEQ} of the lower transistor (to make sure that it is in the active mode yet still leave ample signal swing for the output), and to allot the remaining supply voltage to the upper transistor and R_C.
4. In all high-bandwidth circuits it is mandatory to shunt the power supply with a bypass capacitor, typically 0.l µF or more, as close to the circuit as possible, and to keep all lead lengths within the circuit as short as possible.

Pre-lab:

- Design your Cascode amplifier and show it to a TA. You will be choosing **resistors** and **capacitors** that will allow you to meet the specific requirements stated below. **This design needs to be ready at the start of the lab.**

Experiment:

- Measure R_{in}, R_{out}, A_{mid}, f_H and f_L using the same techniques that you did in Day 1. It is not uncommon for your initial circuit to miss some of these requirements, so be prepared to iterate. When tweaking your design you want to understand the circuit and identify which component can be adjusted to change a certain performance metric. This is especially true with f_H.
- In order to demonstrate the amount of **distortion** your amplifier has as the signal amplitude

increases, you will need to make a series of measurements:
    - Measure the input and output peak-peak voltage swings at a low input signal amplitude (6 mV peak-peak).
    - Gradually increase the input signal and again measure the peak-peak voltage swing of both the input and the output. Keep this up until at least 80 mV peak-peak at the input. Use at least 15 points.
- Create a **frequency response** plot of gain vs frequency. Take 15 – 20 measurements starting lower than f_L and going significantly beyond than f_H.

Results:

As with all labs, you must show your pre-lab work and calculations for both parts of the lab. You need to show several plots and tables in order to clearly demonstrate that your circuit meets specifications. For R_{in} and R_{out}, show a table comparing measured and calculated results. Explain any significant differences.

Show a plot showing measured gain vs. frequency. Show the theoretical result you expected using your pre-lab calculations (the gain should be constant across your frequency range and that the f_H and f_L represent parts where the gain drops by 3 dB. Also note that past f_H or f_L, the gain drops by 20 dB/decade. Show solid lines indicating the minimum and maximum gain that is required, as per the specifications. See Figure 2.8 for a similar example (this is for a filter, not an amplifier).

Show a plot measuring gain as a function of input peak-peak voltage swing. The x-axis (input voltage) should be plotted on a log scale, and the gain should be plotted in dB. Calculate the gain as the ratio between output and input peak-peak voltage swings. The gain should be constant for low voltage swings, and drop as the input increases (sometimes a rise is possible). Identify the location where the gain differs from the low signal gain by 1 dB (you may need to interpolate). In later courses, you will learn about something called the 1-dB compression point- just so we are clear, this is NOT how you measure it, but we will ignore this for now.

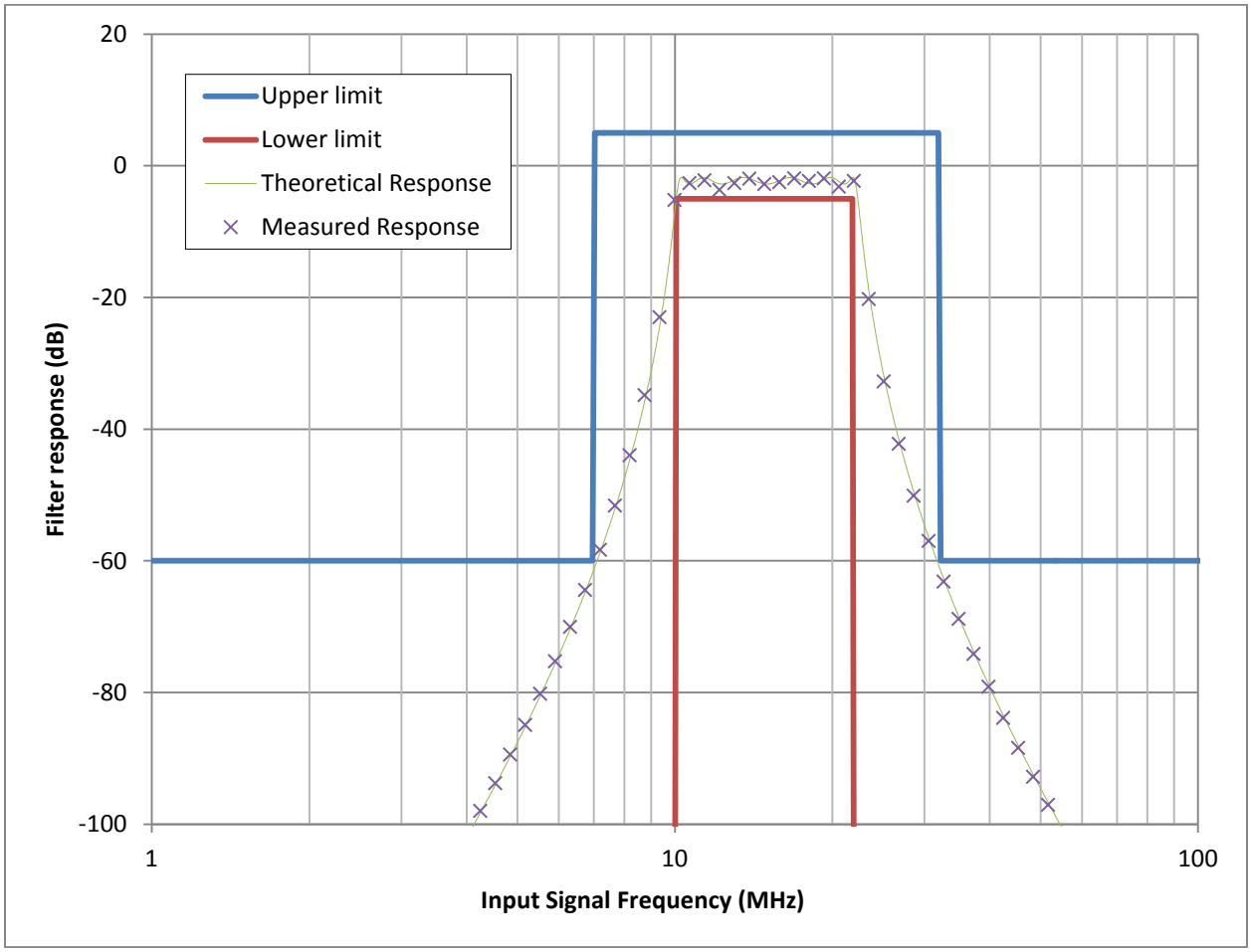

Figure 2.8 Example of a graph showing measured, calculated and required response of a band-pass filter.

APPENDIX

Example Design Approach for a Classical Common-Emitter Amplifier:

As an example design approach we will consider the classical common-emitter voltage amplifier with a four-resistor bias network, as shown in Figure 2.5.

In designing such a circuit, it is generally first necessary to establish the DC bias conditions in the circuit. This action fixes many of the free variables thus making the subsequent design choices simpler. Unfortunately, at this point, the establishment of the DC bias conditions must be done with only a qualitative understanding of their implications on the other design parameters, likely making the solution sub-optimal. However, it does provide the most efficient starting point for the design.

Following the establishment of the DC bias conditions, the AC characteristics can be set. If this first design proves to be inadequate, the process can be repeated, under different assumptions, and the circuit improved. This iterative approach may have to be repeated several times before a satisfactory solution is generated.

The approach proceeds as follows:

1. **Choose I_{CQ}:** Setting I_{CQ} (or I_{EQ}) is often the most reasonable starting point as it is fairly simply related to many design parameters that are often specified. The collector current itself, or the output current of the circuit, or the power dissipated in the circuit, may be specified. In addition, if a wide-bandwidth or high-frequency amplifier is called for, it may be necessary to optimize I_{CQ} in order to maximize f_T of the transistor. Trade-offs exist between these considerations in determining I_{CQ}.

2. **Choose Power-Supply Voltage(s):** In making this choice, consideration must be given to any restrictions that may exist on the choice, such as power dissipation in the circuit elements, what voltages are available, and the magnitude of the output voltage swing that is required.

3. **Choose V_{EQ}:** This choice involves a direct trade-off between bias stability, with respect to variations between individual transistors, variations in temperature etc., and the magnitude of the required output voltage swing. Figure 2.5 shows this trade-off in a graphical form. Typically, V_{EQ} is chosen to be between 0.1 V_{CC} and 0.3 V_{CC}.

4. **R_E is now defined by:**

$$R_E = \frac{\alpha V_{EQ}}{I_{CQ}}, \alpha \approx 1$$

$$\therefore R_E = \frac{V_{EQ}}{I_{CQ}}$$

Choose the nearest standard resistor value, and recalculate V_{EQ} based on this real value.

5. **I_{BQ} is now defined by:**

$$I_{BQ} = \frac{I_{CQ}}{\beta_{DC}}$$

As β_{dc} can take on a range of values, consult the manufacturer's specification of β_{dc}. This choice will guarantee that the subsequent design will provide enough base current for the transistor, regardless of what actual transistor is put into the circuit, which is a valuable advantage in production.

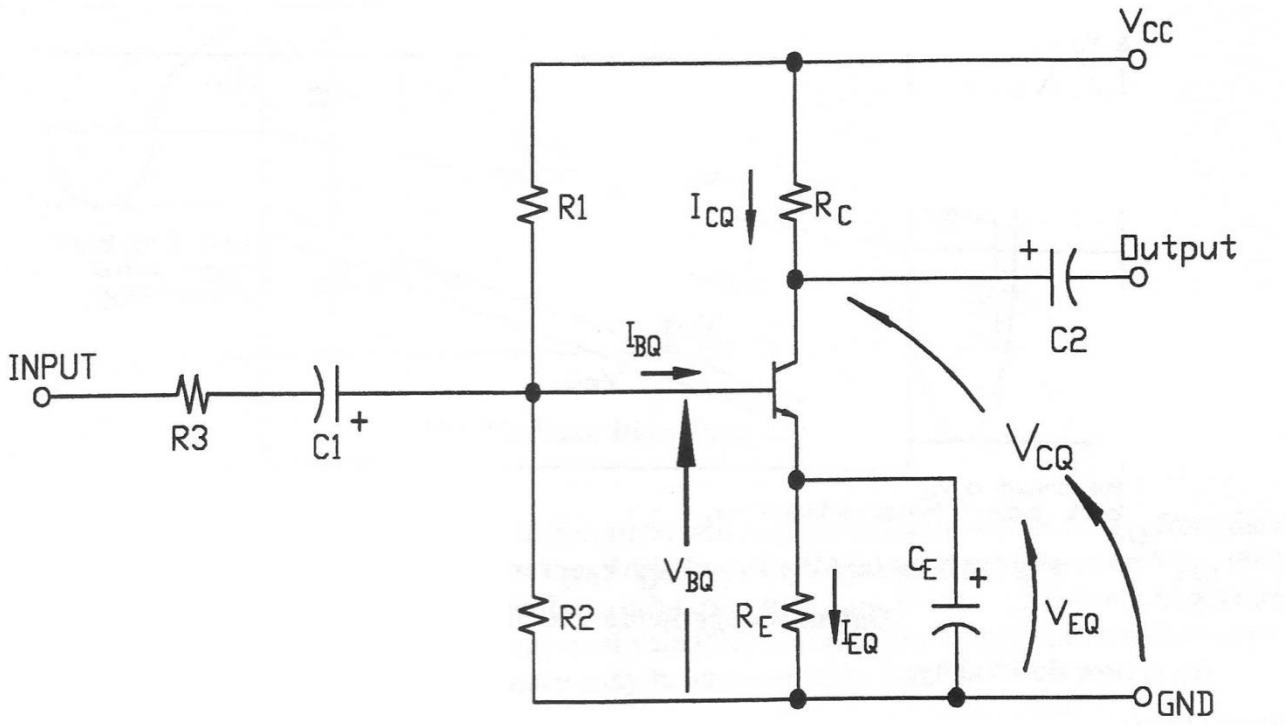

Figure 2.5 *The Classical Common-Emitter Amplifier*

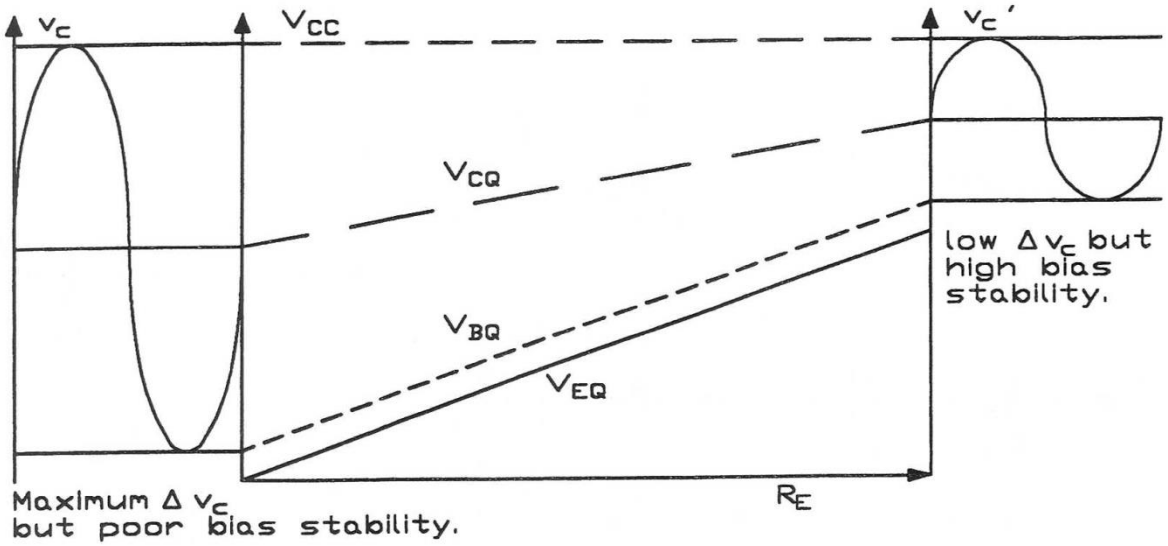

Figure 2.6 Graph of V_C, V_{CQ}, V_{BQ}, V_{EQ} versus R_E Showing the Available Output Voltage Swing and Stability Trade-Off

6. **Choose the Base Bias Resistors, R_1 and R_2:** In the circuit, the base bias resistors fix the base voltage and provide the base bias current to the transistor. The process of choosing the resistors is best broken down, as follows:

(i) The base bias circuit is analyzed. Figure 2.7 shows the base bias circuit removed from the rest of the amplifier.

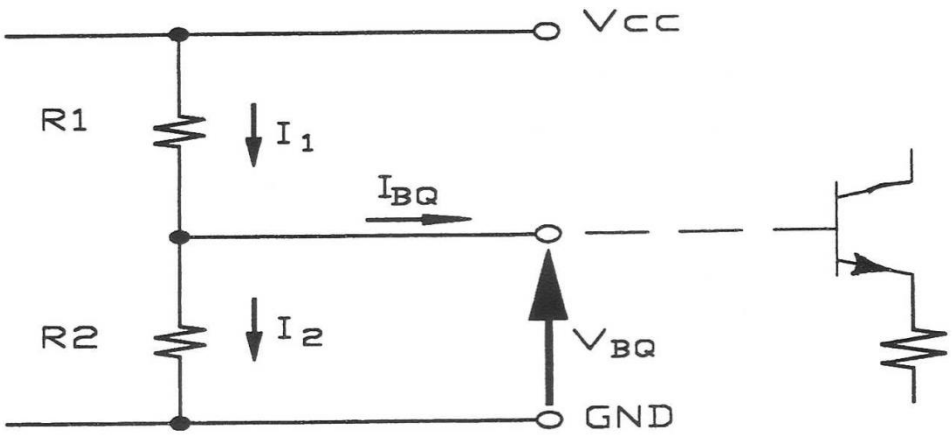

Figure 2.7 Base Bias Circuit.

Different transistors with different values of β will require different values of I_{BQ} from the bias circuit. To minimize the effect that these different current demands will have on V_{BQ}, the bias network currents, I_1 and I_2, should be much larger than I_{BQ}. On the other hand, to get large values of bias network currents may cost valuable power, and/or imply such small resistor values that the circuit's input impedance may be unacceptably low.

As a very practical and easy-to-work-with compromise, I_2 is usually made to be about 10 I_{BQ}. Thus set: $I_2 = 10\ I_{BQ}$; $I_1 = 10\ I_{BQ} + I_{BQ} = 11\ I_{BQ}$

(ii) V_{BQ} is defined by choices already made to be: $V_{BQ} = V_{EQ} + 0.7$ volts

(iii) R_1 and R_2 are now defined by the circuit conditions:

$$R_1 = \frac{V_{CC} - V_{BQ}}{I_1} = \frac{V_{CC} - V_{BQ}}{11 I_{BQ}}$$

$$R_2 = \frac{V_{BQ}}{I_2} = \frac{V_{BQ}}{10 I_{BQ}}$$

Choose the nearest standard resistor values that keep V_{BQ} nearest the level determined at step 6(ii) and use the new value of V_{BQ} in subsequent steps.

(iv) The new I_{BQ} value is determined by

$$I_{BQ} = \frac{\frac{V_{CC} R_2}{R_1 + R_2} - 0.7}{\frac{R_1 R_2}{R_1 + R_2} + R_E(1 + \beta_{DC})}$$

Thus

$$V_{BQ} = \frac{V_{CC} R_2}{R_1 + R_2} - I_{BQ} \frac{R_1 R_2}{R_1 + R_2}$$

Consequently, V_{EQ} should be recalculated using: $V_{EQ} = V_{BQ} - 0.7$ volts and so should I_{EQ}, using:

$$I_{EQ} = \frac{V_{EQ}}{R_E}$$

and finally I_{CQ}, using: $I_{CQ} \sim I_{EQ}$

7. Choose R_C: R_C primarily determines V_{CQ}, the maximum v_c signal swing, and the maximum gain. Usually, the signal swing is maximized, and the small compromise that this places on the gain is accepted. To maximize the signal swing, V_{CQ} is placed at the midpoint between V_{BQ} and V_{CC}. Consequently,

$$R_C = \frac{V_{CC} - V_{BQ}}{2I_{CQ}}$$

Choose the nearest standard resistor value, and recalculate V_{CQ} and the v_c signal swing.

$$V_{CQ} = V_{CC} - I_{CQ}R_C$$

This then concludes the D.C. biasing for the transistor. Next, the ac circuit parameters will be set

8. **Choose R3:** This resistor is determined by the gain that is required of the circuit. Generally, the value used for the gain in the calculation is set high by about 10% in an attempt to compensate for unaccounted circuit losses. Any resulting extra gain usually can be tolerated, as opposed to a deficit which cannot. If necessary, the extra gain can be removed by increasing the resistance value of R3.

Analysis of the circuit will determine the required value for R3. Choose the nearest lower standard resistance value in order to maintain the gain. (N.B. For maximum bandwidth R3 should really be zero.)

9. -12. Determine (9) the Bandwidth, (10) the Magnitude of the Input Impedance, (11) the Magnitude of the Output Impedance, and (12) the Loaded Output Signal Swing: These parameters can all be determined by analyses of the circuit under the assumption that all external capacitor values are infinite.

13. -15.Choose C_1, C_2, and C_E: These capacitors determine the lower band-limit of the amplifier by introducing poles into its response. Analyses of the circuit will yield equations for each pole frequency. Using equations SS4 (7.43) - (7.46) (SS5 5.178, 5.180, 5.182) and the argument presented on p. 610 of SS4 (pp. 502-503 of SS5), the values for the capacitors in the circuit can be determined.

16. **Iterate Solution:** With the completion of this last step, the amplifier design procedure will have finished its first iteration. If nowhere along the way were one or more of the specifications not met, then the design could be considered to be complete. If, however, one or more of the specifications were not met, then it will be necessary to iterate the solution, with the knowledge that certain parameters of the design must be improved, and with the insight into how best to improve them that consideration of the first solution can give.

Following the example design approach just given, a common-emitter amplifier was designed to meet the following specifications:

Gain:	35 ± 20%
R_L:	4.7 kOhm
Bandwidth:	unimportant
V_{out}:	2 volts peak-to-peak
Distortion:	"low"
I_C:	1.0 mA ± 20%
f_L:	<200 Hz

The highlights of the design procedure, along with results, without the details of analysis, are presented below.

CE DESIGN CALCULATIONS:

1. I_{CQ} = 1.0 mA (spec.)
2. Let V_{CC} = 15 volts (available, and should easily allow 2 volt p-p output swing)

3. Let V_{EQ} = 0.2 V_{CC} = 3 volts (moderate stability)
4. $\therefore R_E$ = 3 kOhm, use R_E = 3.3 kOhm

   $\therefore$*New* V_{EQ} = 3.3 volts
5. I_{BQ} = 2.5 to 10μA (since β = 100 to 400) Use I_{BQ} = 10μA
6. (i) $I_1 = I_2 = 10I_{BQ}$ = 100μA (very approx.)

   (ii) $\therefore V_{BQ}$ = 4.0 volts

   (iii) ∴R1 = 100kOhm and R2 = 40 kOhm. Use 39 kOhm. New I_{BQ} = 9.7μA

   $\therefore$*New* V_{BQ} = 3.94 volts New V_{EQ} = 3.24 volts

   New I_{EQ} = 0.98 mA

   New I_{CQ} = 0.98 mA

7. Let $V_{CQ} = \frac{V_{CC}+V_{BQ}}{2} = \frac{15V+3.94V}{2} = 9.47V$

   $\therefore R_C$ = 5.53kOhm .

   Use R_C = 5.6 kOhm (to give max. signal swing, but V_{be} will exceed 20mV pp causing distortion before either cut-off or saturation occur; see (step 12)

8. R3: Following Sedra and Smith *p. 609,* Fig. 7.14

$$|A_M| = \left|\frac{V_o}{V_S}\right| = g_m (r_o \| R_C \| R_L) \bullet \frac{R_B || (r_X + r_\pi)}{R_S + R_B || (r_X + r_\pi)} \bullet \frac{r_\pi}{r_X + r_\pi}$$

   where we take $R_S = R_3$ and include it in the amplifier to limit the gain with

   g_m = 0.04 A/V (measured)

   r_o = 100 kOhm (measured) (actual value is large)

   R_B = 100 kOhm || 39 kOhm =28.1 kOhm

   r_x = 20 Ohm (measured) (actual value is small)

   r_{π} = 2.5 kOhm (measured) (actual value has large range)

   and A_M + 10% = 38.5

   R3 = 3.65 kOhm. Use R3 = 3.3 kOhm

   New A_M = 40.9 v/v
9. f_H Not required.
10. Analysis of Fig. 7.14 yields $|Z_{in}|$ = 5.6 KOhm
11. Analysis of Fig. 7.14 yields $|Z_{out}|$ = 5.3 KOhm
12. Setting V_π = 20 mV peak to peak, V_{out} (low distortion) = 2.0 volts
13. From Sedra and Smith SS4 equations (7.43) - (7.46) (SS5 5.178, 5.180, 5.182) we have $\omega_L = 2\pi \times 200 = 400\pi$ rad/sec.

$$C_1 = \frac{1}{0.1\omega_L R_{C1}} = \frac{1}{0.1 \times 400\pi \times 5600} = 1.42\mu F \rightarrow 2.2\mu F$$

14.

$$C_2 = \frac{1}{0.1\omega_L R_{C2}} = \frac{1}{0.1 \times 400\pi \times 10000} = 0.796\mu F \rightarrow 1\mu F$$

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$$C_E = \frac{1}{0.8\omega_L R_E} = \frac{1}{0.8 \times 400\pi \times 13} = 76.5\mu F \rightarrow 100\mu F$$

(β_{max} = 400 for W.C. value)

$\therefore f_L$ <200Hz

16. Some increase in R_3 to remove excessive gain may have to be undertaken, say R_3 = 3.9 kOhms.