CMOS Combinational Logic

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ELEC 3500B
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Lab 2 Report

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1. Design of the CMOS Inverter

Q1. Classify the inverter circuits of Figure 2.2 as "won't work," "will work with poor output swing," and "will work well". Explain which one does not have the inverting structure.

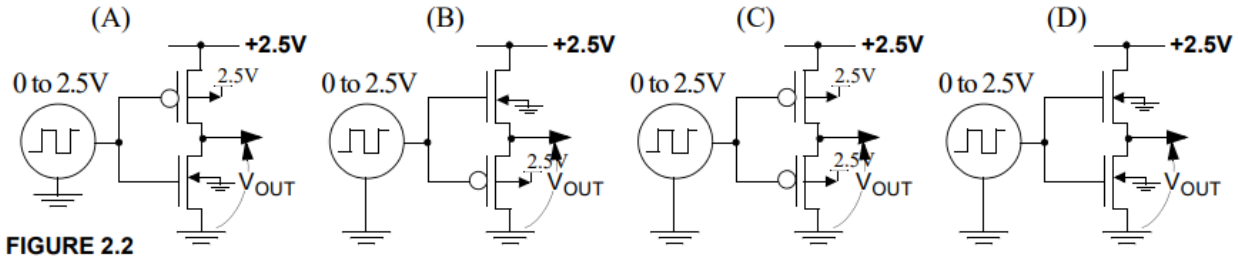

Figure 1 - The Provided Schematic for Q1 [1]

(A) Will work well. This is an inverter with PMOS pulling up and NMOS pulling down.
(B) Will work with poor output swing, and does not have the inverting structure. This is a buffer structure with PMOS pulling down and NMOS pulling up. Using the knowledge learned in lab 1, the PMOS could not pull the output voltage down close to ground (0V) and the NMOS could not pull the output voltage up because of the threshold voltages. Therefore, this circuit will work with poor output swing and does not have the inverting structure.
(C) Won't work. When the input was low, both transistors would be on, and it would act as a short circuit from V_{DD} to ground. When the input was high, both transistors will be off, and the output could be considered as floating. This circuit do not have the inverting structure.
(D) Won't work. When the input was low, both transistors would be off, and the output could be considered as floating. When the input was high, both transistors would be on, and it acts as a short circuit from V_{DD} to ground. This circuit do not have the inverting structure.

Q2. Using simulations, sketch the output waveform from circuits (A) and (B). Use the knowledge you gained from last week to explain

Figure 2 below shows the simulation of the output waveforms for circuits (A) and (B). The circuit (A) is working properly as an inverter. When the input is high, the NMOS pulls the output voltage close to ground. When the input is low, the PMOS pull the output voltage close to V_{DD}. On the other hand, the circuit (B) is working with poor output swing as a buffer. This is due to the fact that PMOS could not pull the output voltage down close to ground and the NMOS could not pull the output voltage up because of the threshold voltages.

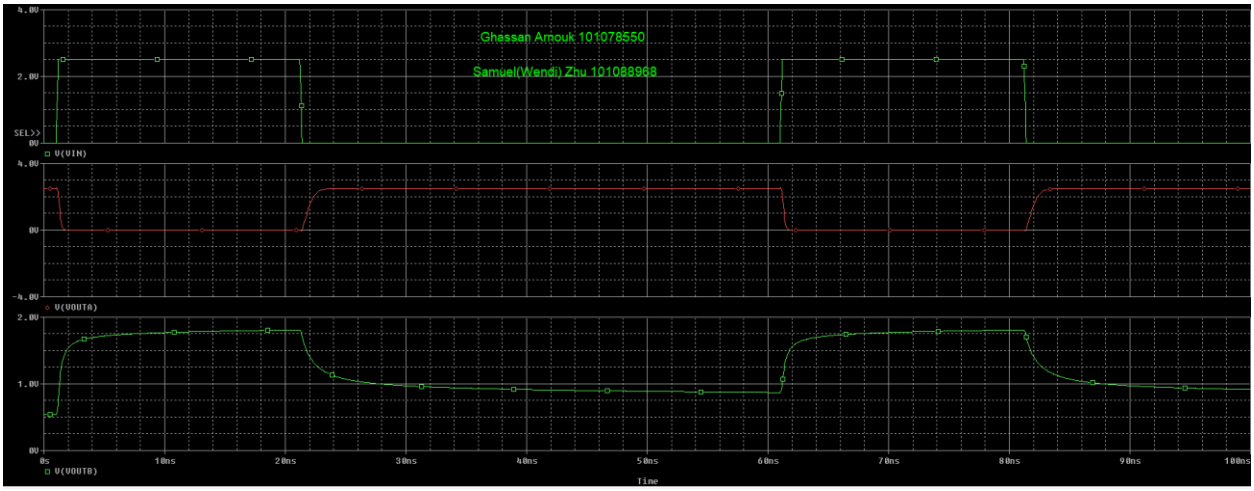

Figure 2 - Simulation for V_{in}, V_{outA}, and V_{outB}

Q3. For the CMOS inverter in (A) measure the falling and rising times (10% - 90% swing), and measure the falling and rising delays (50% input swing to 50% output swing).

Figure 3 below shows the simulation waveforms for V_{IN} and V_{OUT} for the inverter in (A).

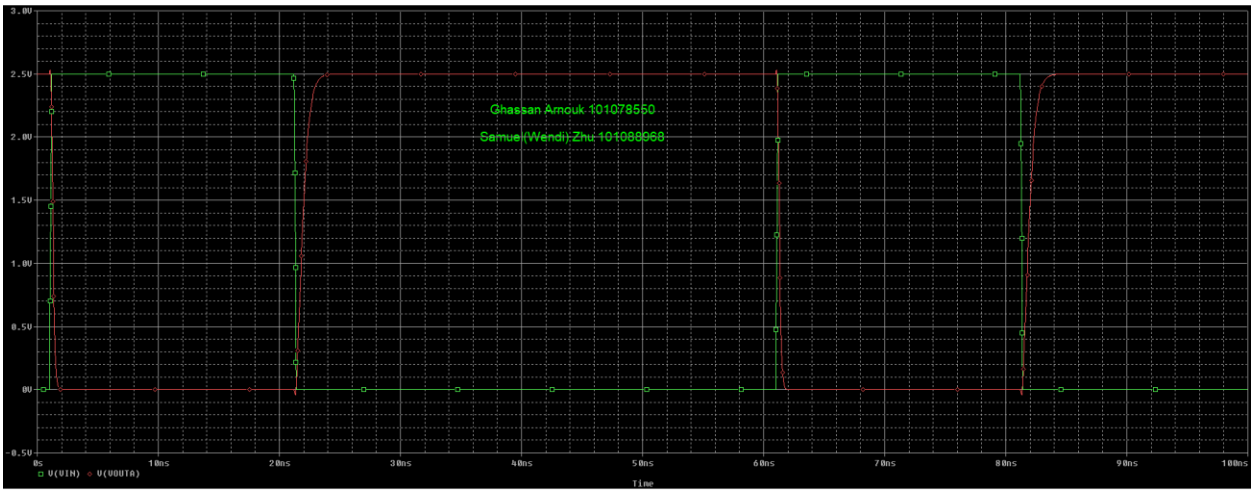

Figure 3 - Simulation waveforms for V_{IN} and V_{OUT} for the CMOS inverter in (A)

Figures 4 & 5 below show the simulations for the measurement for falling and rising times (10% - 90% swing). Figures 6 & 7 below show the simulations for the measurement for falling and rising delays (50% input swing to 50% output swing).

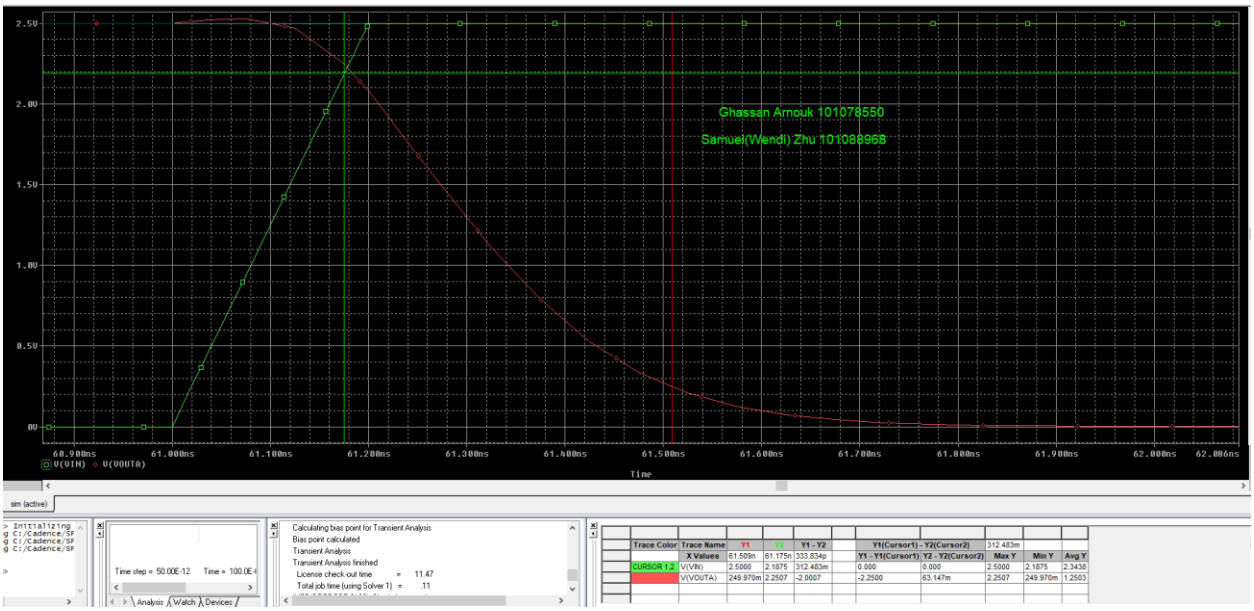

Figure 4 - Simulation for Falling Time Measurement (10% - 90% swing)

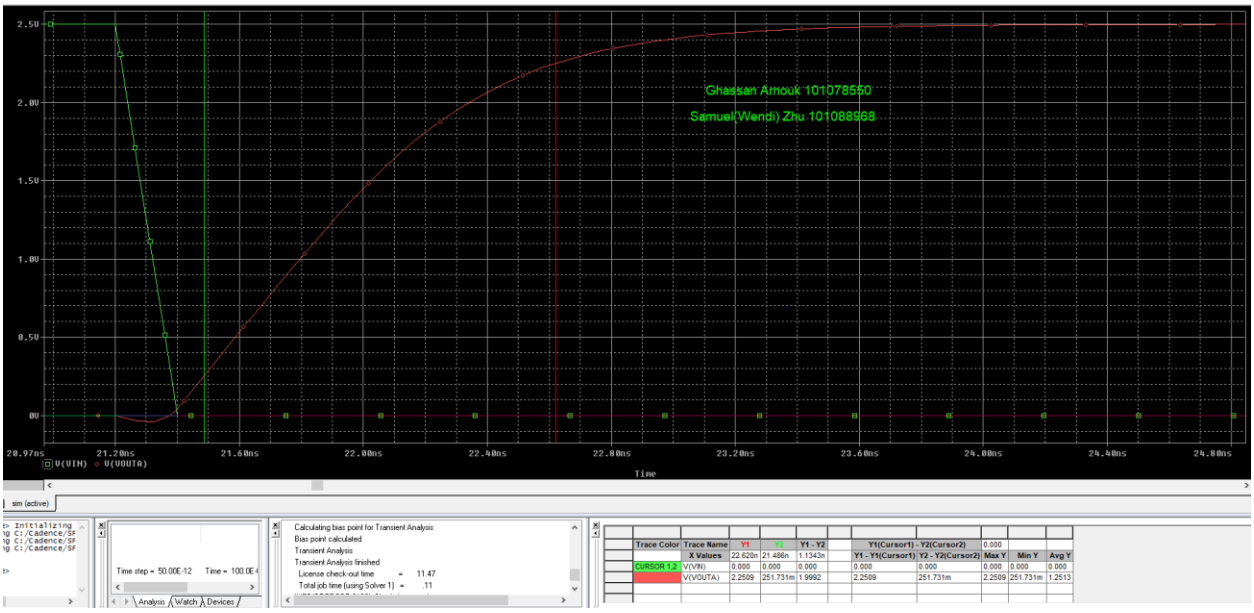

Figure 5 - Simulation for Rising Time Measurement (10% - 90% swing)

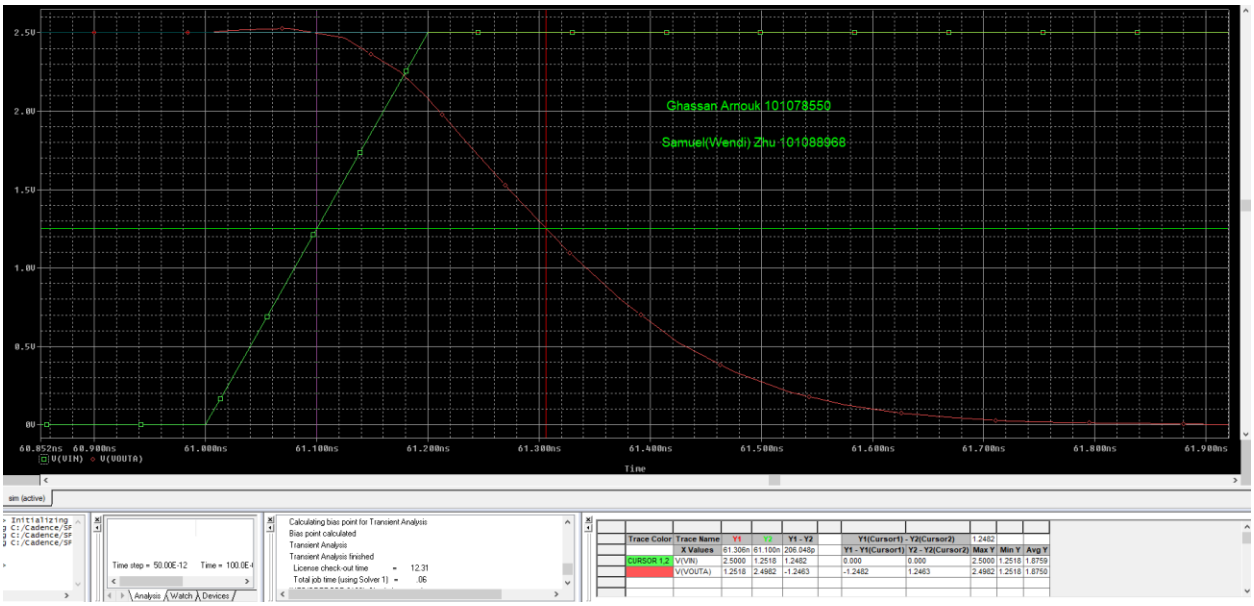

Figure 6 - Simulation for Falling Delay (50% input swing to 50% output swing)

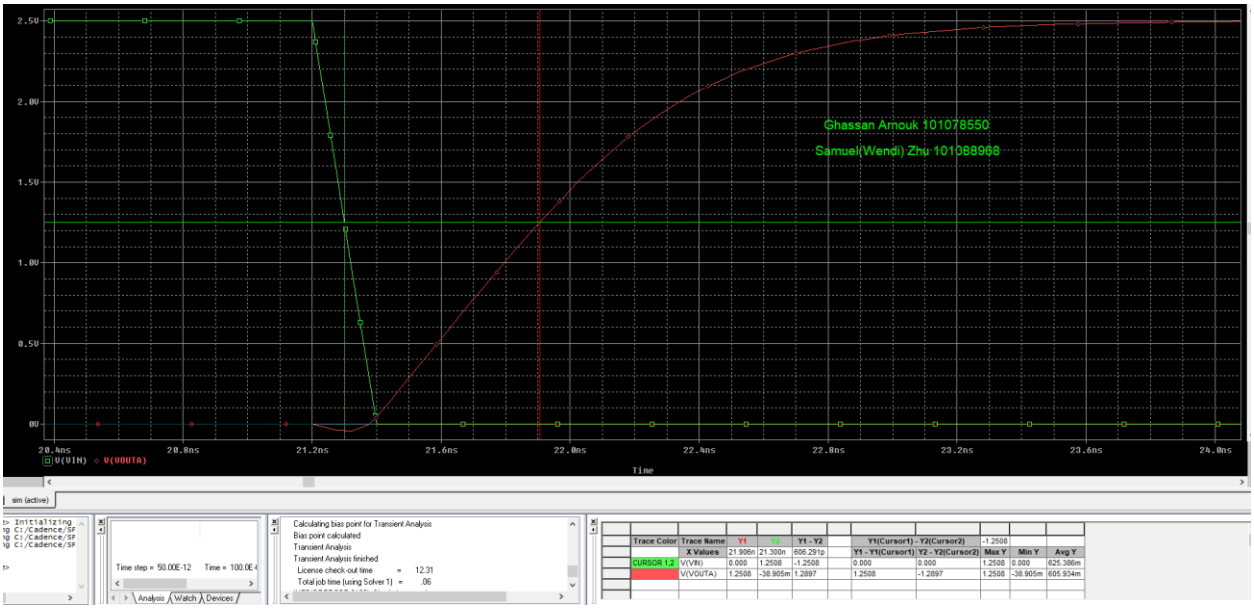

Figure 7 - Simulation for Rising Delay (50% input swing to 50% output swing)

From Figure 4 above, the falling time was found using cursors values:

$$Falling\ time = 61.509ns - 61.175ns = 333.834\,ps$$

From Figure 5 above, the rising time was found using cursors values:

$$Rising\ time = 22.620ns - 21.486ns = 1.1343\,ns$$

From Figure 6 above, the falling delay was found using cursors values:

$$Falling\ delay = 61.306ns - 61.100ns = 206.048\,ps$$

From Figure 7 above, the rising delay was found using cursors values:

$$Rising\ delay = 21.906ns - 21.300ns = 606.291\,ps$$

Q4. Which delay is larger? Why? (Hint: look into PMOS and NMOS transistors relative sizes.)

The rising delay was larger. This is because PMOS was used in pull up, and it caused the rising delay. The NMOS was used in pull down, and it caused the falling delay. Because the electrons mobility was higher than the holes mobility, the delay for PMOS is larger than NMOS since the charge carriers in PMOS were mainly holes and the charge carriers for NMOS were mainly electrons.

Q5. For what size ratio (W/L) you expect a symmetric output (i.e. almost equal rising and falling times, and almost equal rising and falling delays.) Prove your suggestion by simulation results. You may want to try a number of cases such that the rising and falling delays differ by less than 5%.

(Check this later)

In order to have the same rising and falling delays, we could set the current for the PMOS and NMOS the same to find the ratio. For same length L for PMOS and NMOS:

$$\frac{(W/L)_p}{(W/L)_n} = \frac{(W)_p}{(W)_n} = \frac{\mu_n}{\mu_p} = \frac{1440}{450} = 3.2$$

We could expect the ratio of 3.2 to give us a symmetric output. The width for PMOS could increase from 1um to 3.2um for a symmetric output.

Figures 8 & 10 below show the simulation for falling and rising time. Figures 9 & 11 below show the simulation for falling delay and rising delay. Using Fig. 8, the falling time was 338.834 ps. Using Fig. 10, the rising time was 333.534 ps. From Fig. 9, the falling delay was 230.528 ps. From Fig. 11, the rising delay was 233.654 ps.

$$\%Error = \frac{233.654 - 230.528}{230.528} \times 100\% = 1.356\%$$

Therefore, the rising and falling delays was differ by less than 5%.

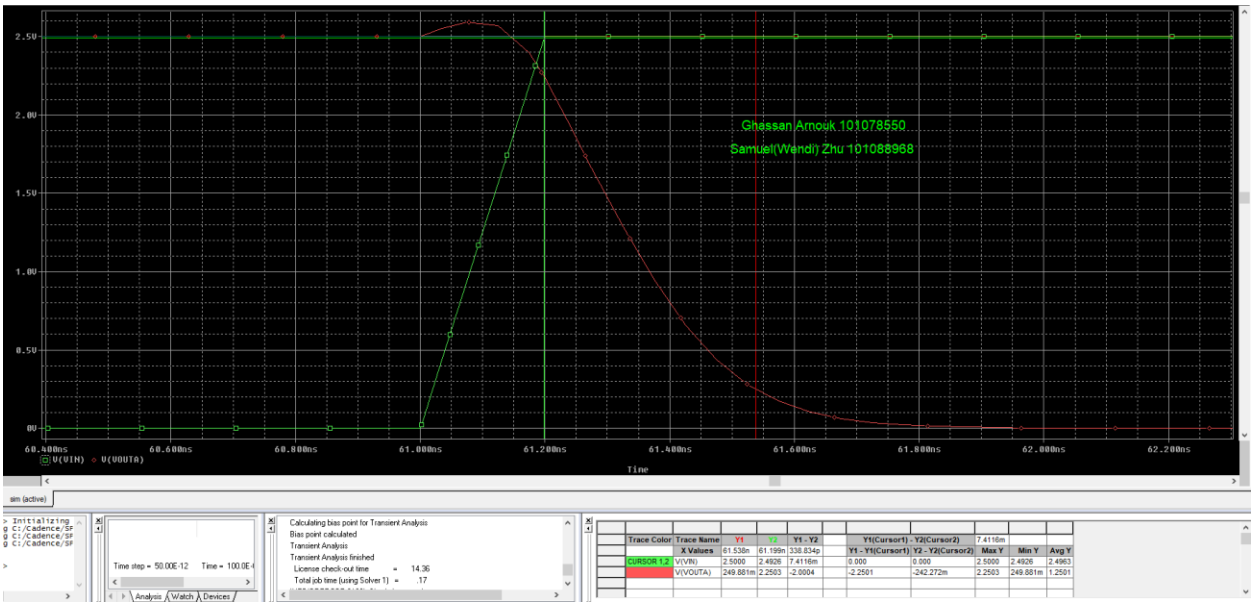

Figure 8 – Simulation for Falling Time

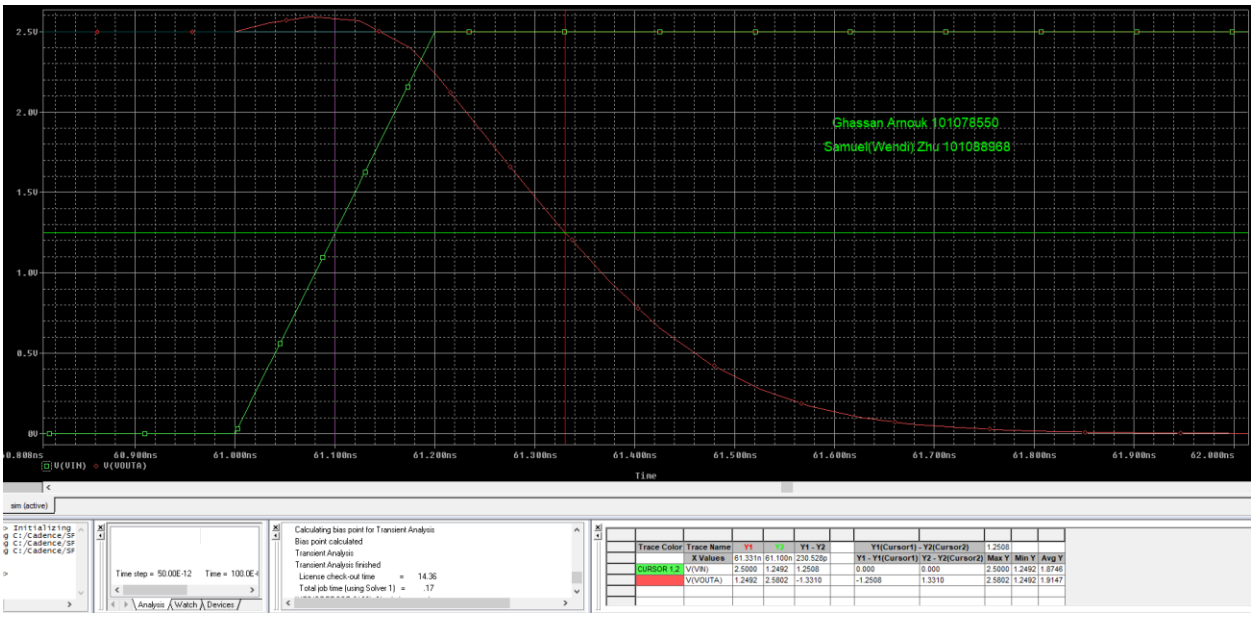

Figure 9 - Simulation for falling delay

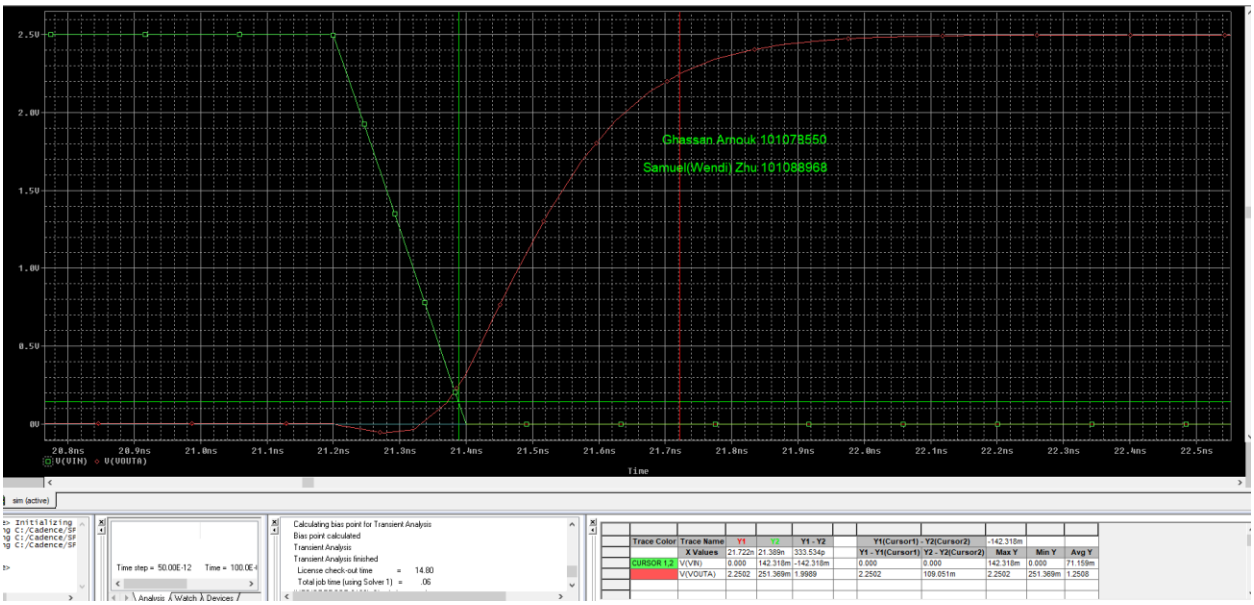

Figure 10 – Simulation for Rising Time

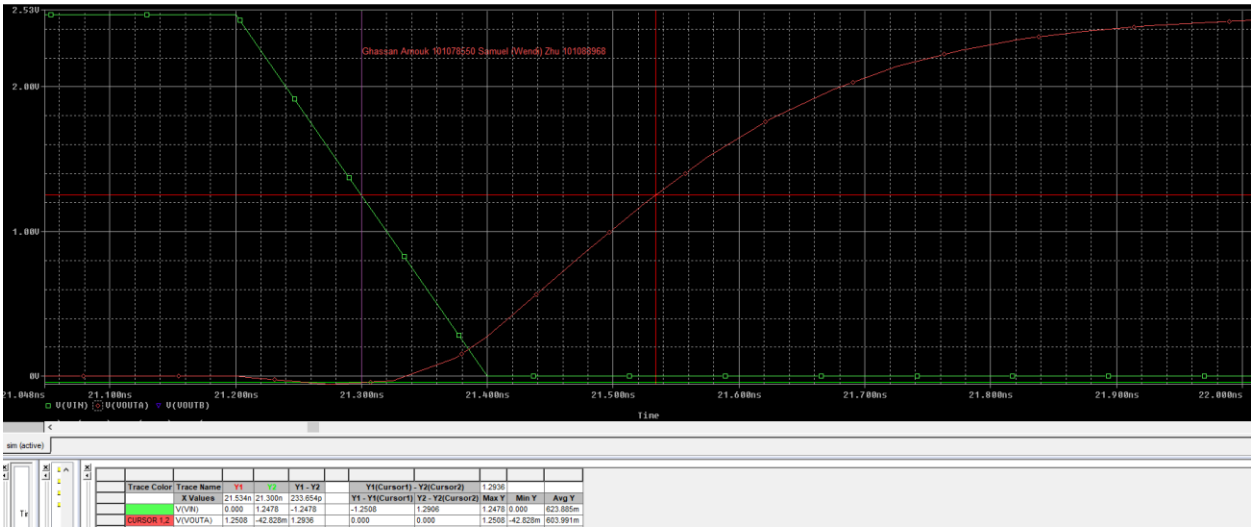

Figure 11 - Simulation for rising delay

Q6. Plot VTC of the inverter by sweeping the input from 0V to 2.5V at 0.05V intervals and measuring the output. On the graph show and measure the Switching Threshold. (Use original values for W, L).

Figure 12 below shows the simulation for the measurement of the Switching Threshold.

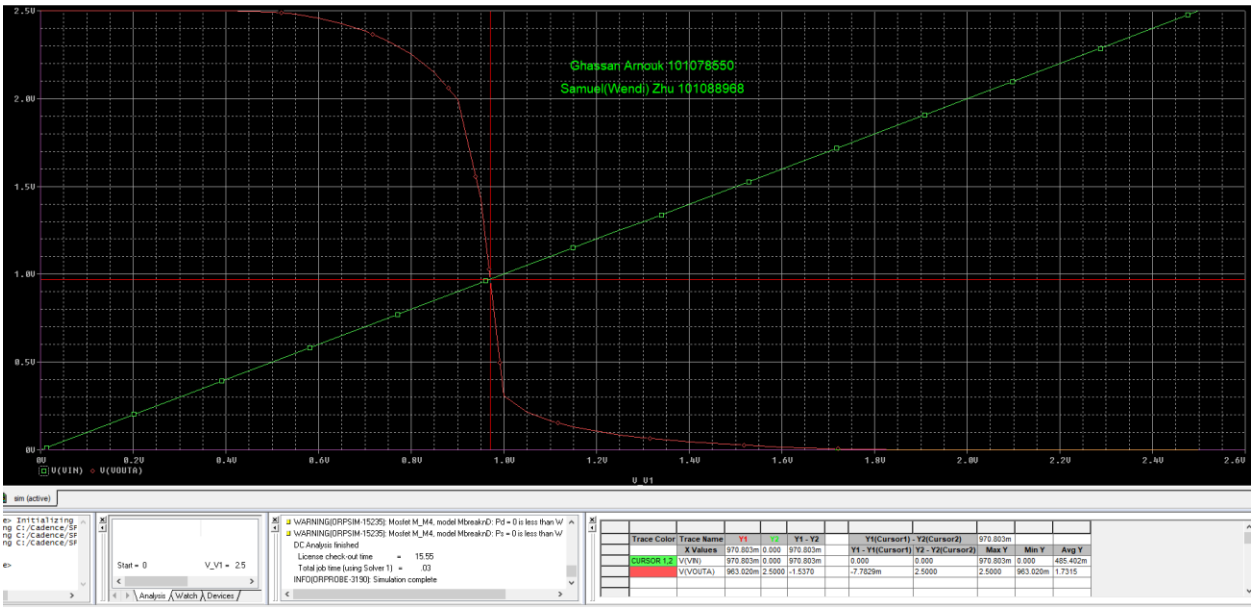

Figure 12 - Simulation for the measurement of the Switching Threshold

Using the cursor measurement, the Switching Threshold was (970.803 mV, 970.803 mV)

Q7. Try Q6 with the width of the PMOS at 8um instead of 1um. What difference do you realize? Explain.

Figure 13 below shows the Switching Threshold with the width of the PMOS at 8um instead of 1um.

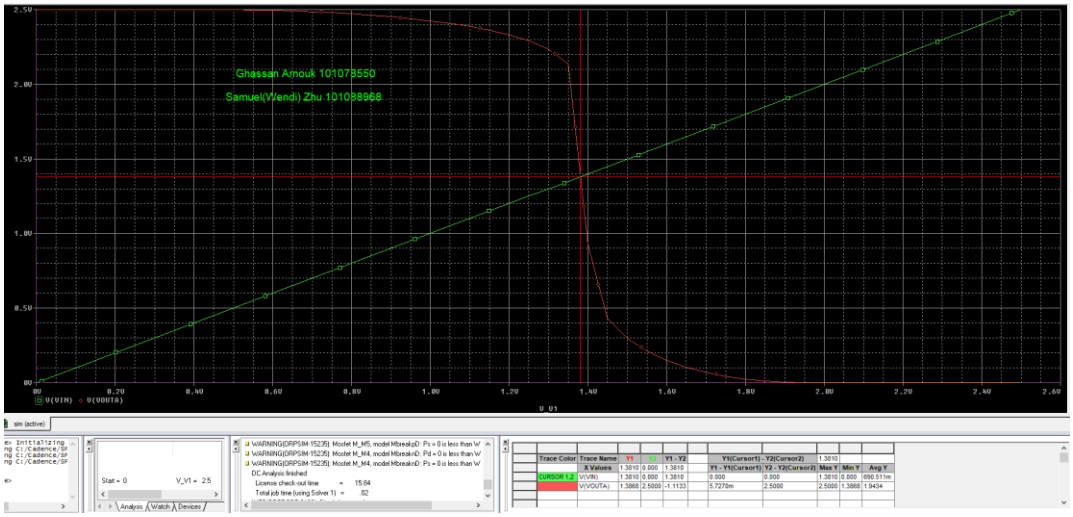

Figure 13 - Switching Threshold with the width of the PMOS at 8um

The Switching Threshold with the width of the PMOS at 8um was (1.3810 mV, 1.3810 mV). This switching threshold was larger than the previous one (970.803 mV, 970.803 mV). This is because as the width of the PMOS increases, the ratio of W/L increases. This increased the current of the PMOS hence increased the voltage.

NAND GATE

Q8. Plot the input and output waveforms and make sure the gate functions properly for all input cases. Measure the delay in each of the four cases. Present the data in the table.

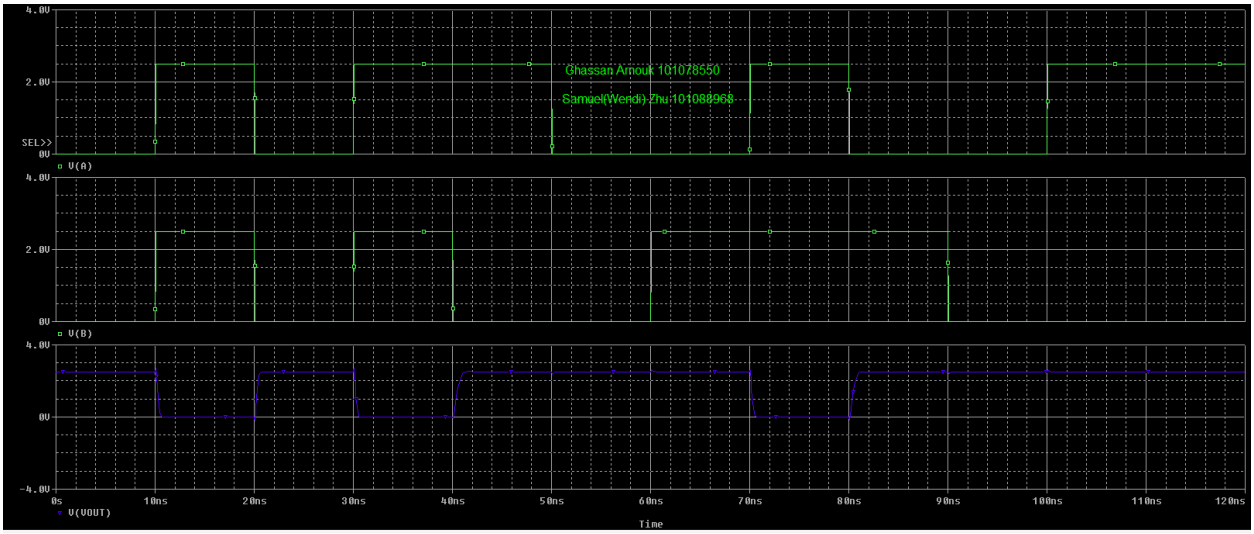

Figure 14 – V_A, V_B, and V_{out} Waveforms of a NAND Gate

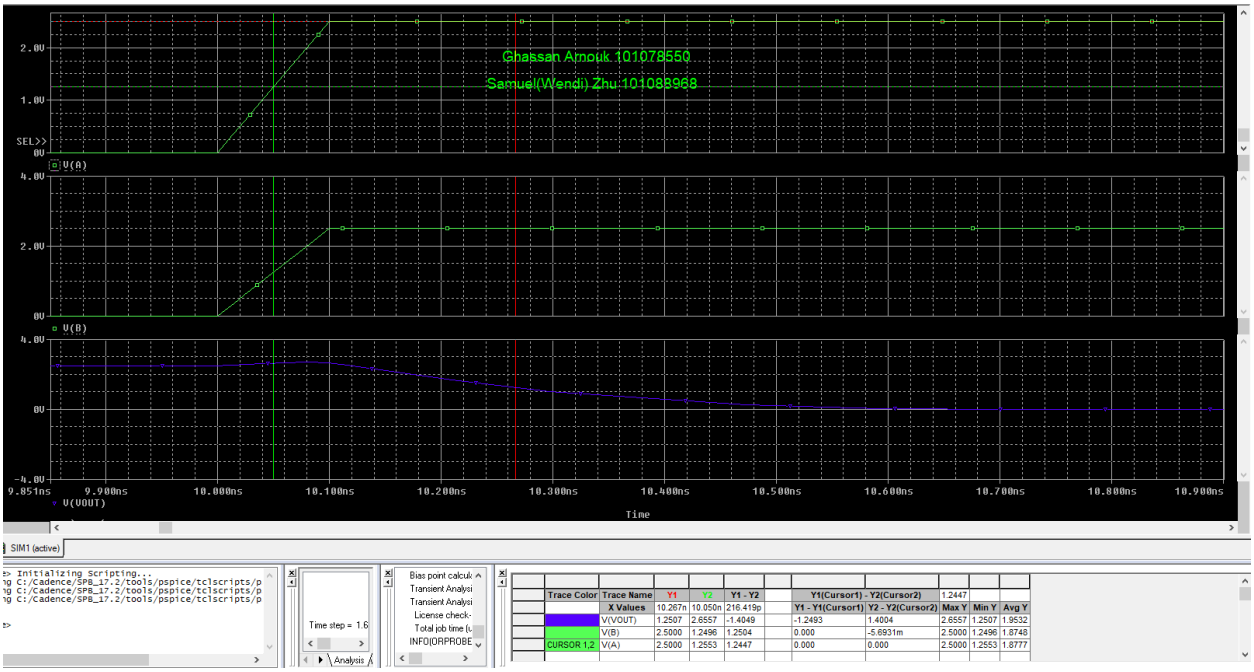

Figure 15 – Case 1: 00 > 11

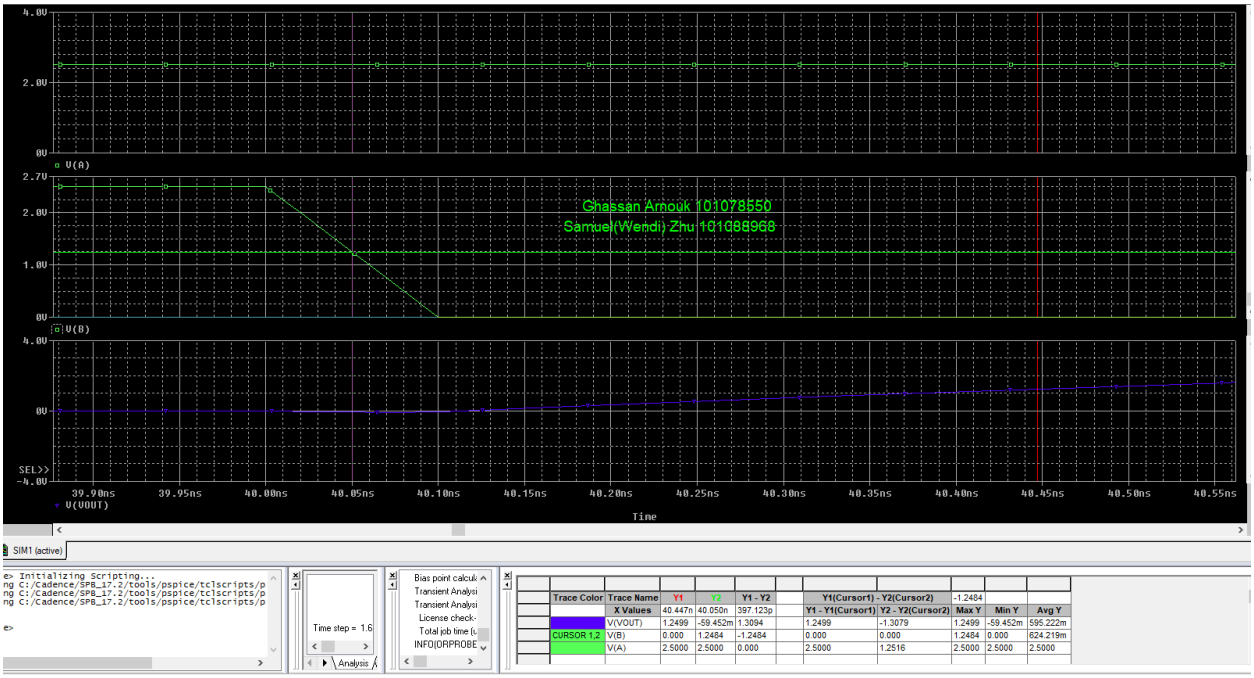

Figure 16 – Case 2: 11 > 10

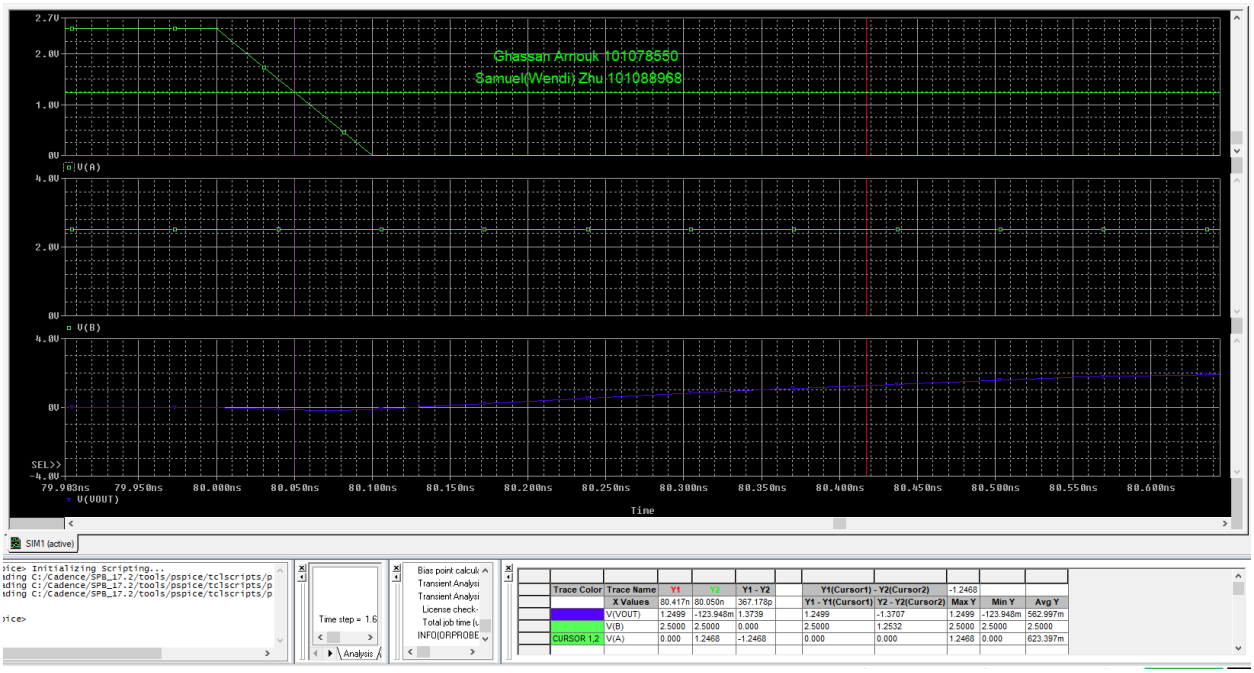

Figure 17 – Case 3: 11 > 01

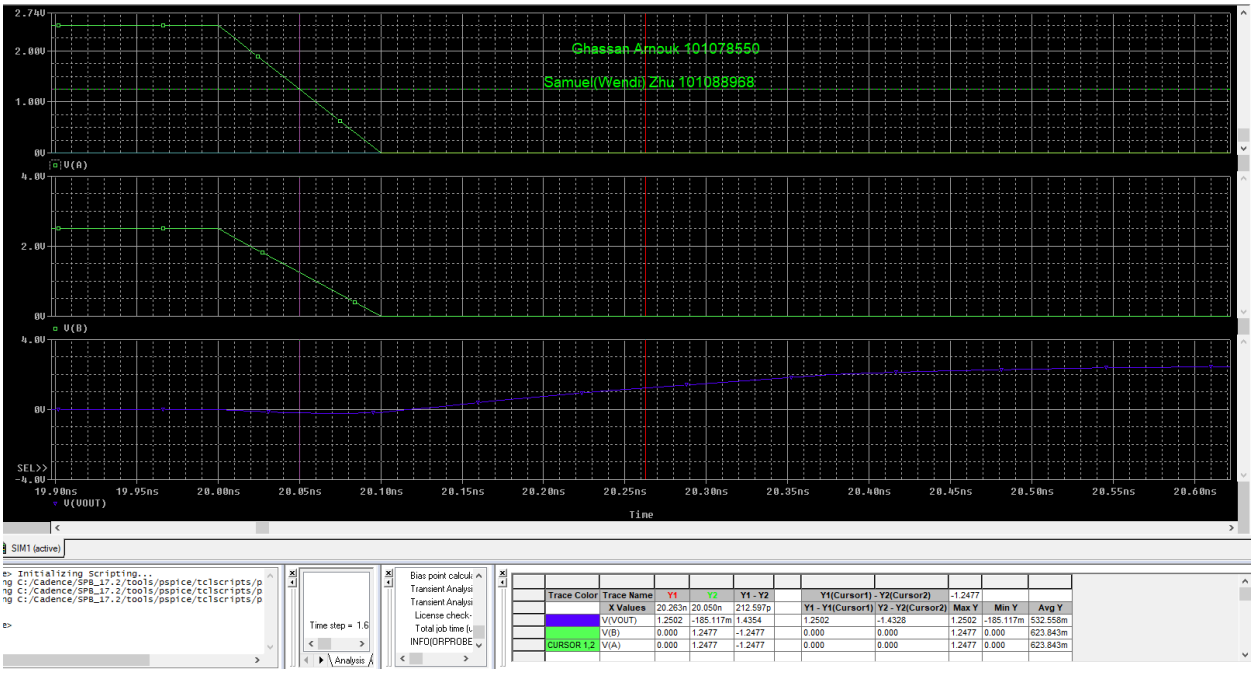

Figure 18 - Case 4: 11 > 00

Table 1 - Data Associated with Q8

Case Number	From AB	To AB	Delay (ps)	Rising/Falling
1	0 0	1 1	216.419	Falling
2	1 1	1 0	397.123	Rising
3	1 1	0 1	367.178	Rising
4	1 1	0 0	212.597	Rising

Q9. Which input combination defines the worst-case rising delay? What is this delay?

The input combination that defines the **worst-case** rising delay is from [11] to [10]. It has a long falling delay of 397.123ps.

Q10. Which input combination defines the best-case rising delay? What is this delay?

The input combination that defines the **best-case** rising delay is from [11] to [00]. It has a long falling delay of 212.597ps.

Q11. What is the relation between the numerical rising delay values of the two cases in Q9 and Q10? Can you explain why?

The relation between the numerical is that the worst-case falling delay value is almost doubled the best-case falling delay value (397.123/212.597 = 1.87). The best-case rising delay has two operating PMOS transistors connected in parallel which is faster than the worst-case rising delay that has only one operating PMOS.

Q12. Which input combination defines the falling delay?

The input combination that defines the falling delay is from [00] to [11]. It has a falling delay of 216.419ps.

NOR Gate

Q13. Consider a NOR gate: Z = NOT (A or B). Sketch a logic network of 4 transistors (2 NMOS + 2 PMOS) to create this gate. Get a TA to verify this and mark it on the spot before continuing.

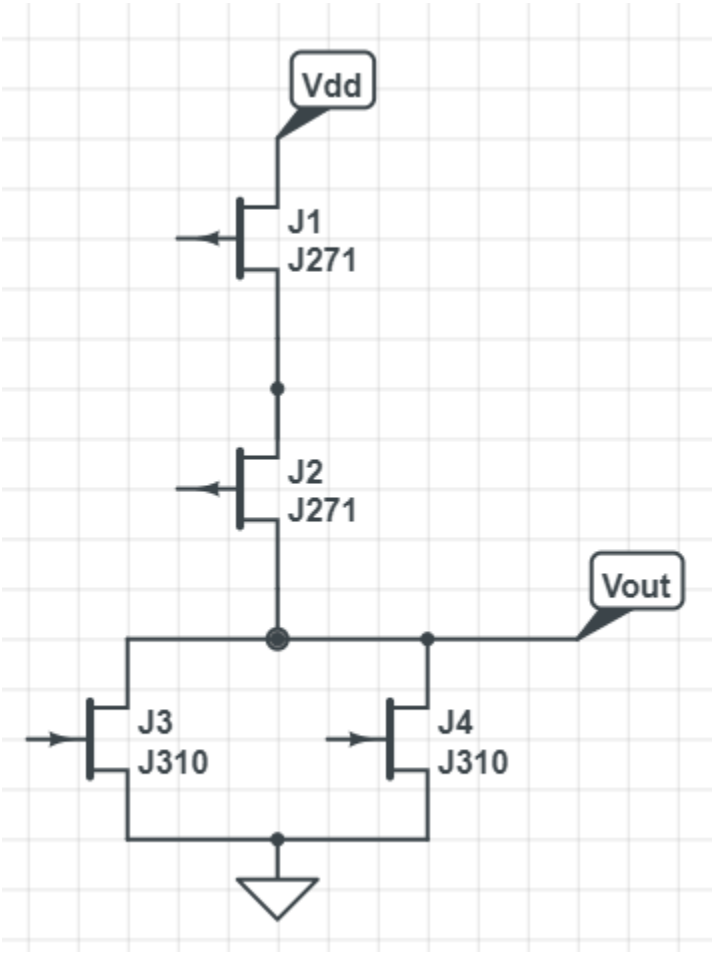

Figure 19 - NOR Gate Made of 2 NMOS + 2 PMOS Transistors

Q14. Plot the input and output waveforms and make sure the gate functions properly for all input cases. Measure the delay in each of the four cases. Present the data in the table.

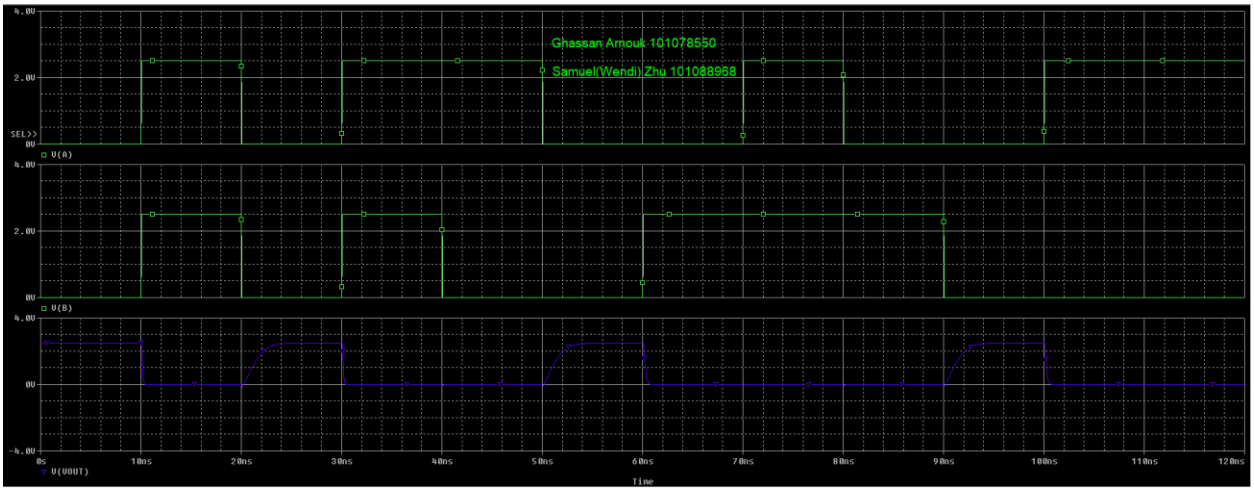

Figure 20 - VA, VB, and V_{out} Waveforms of a NOR Gate

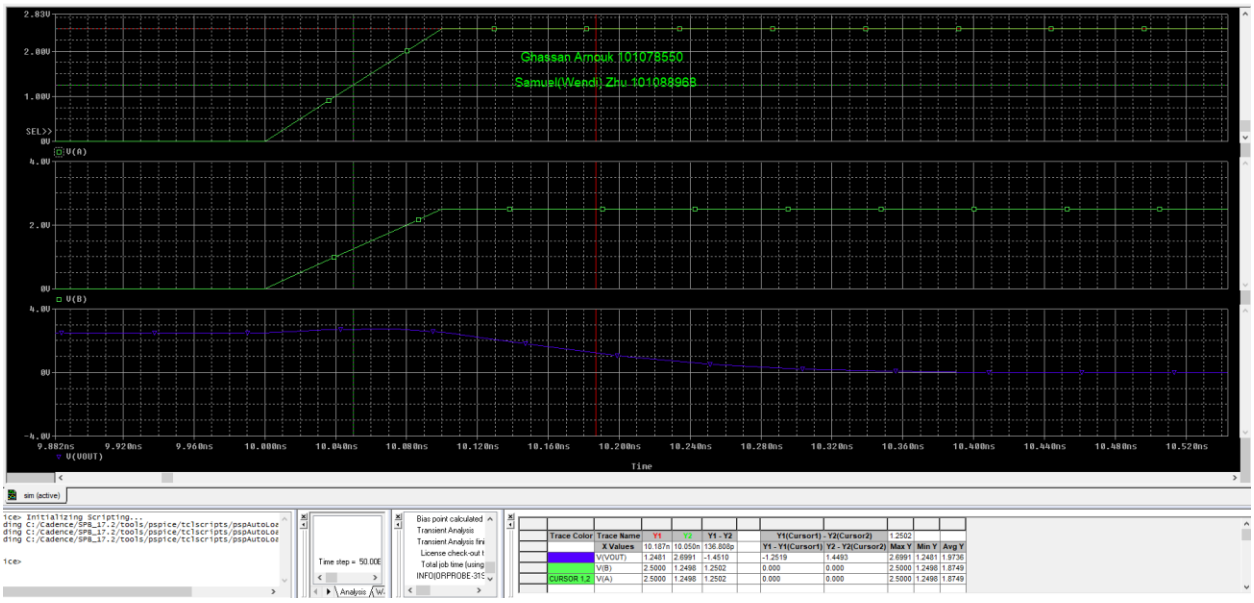

Figure 21 – Case 1: 00 > 11

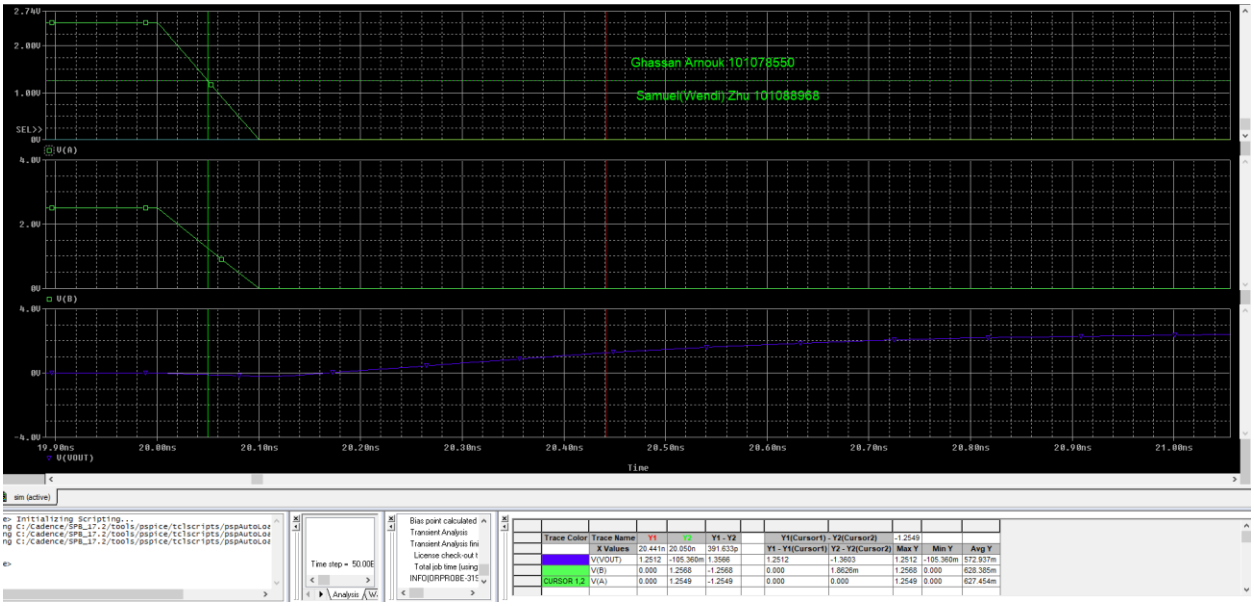

Figure 22 – Case 2: 11 > 00

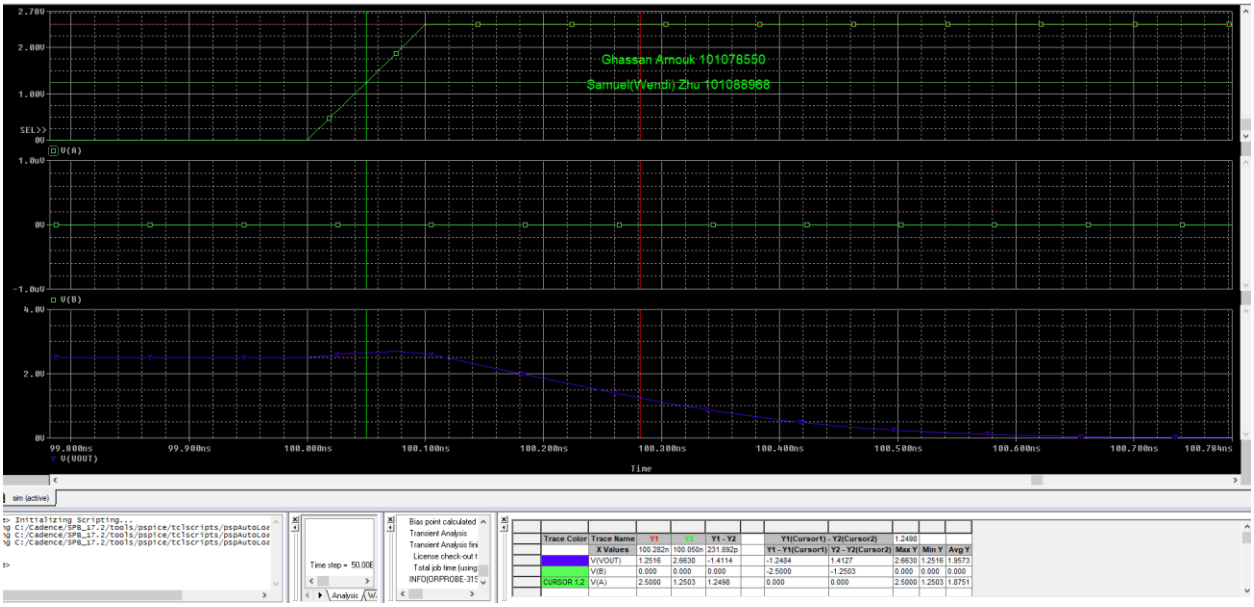

Figure 23 - Case 3: 00 > 10

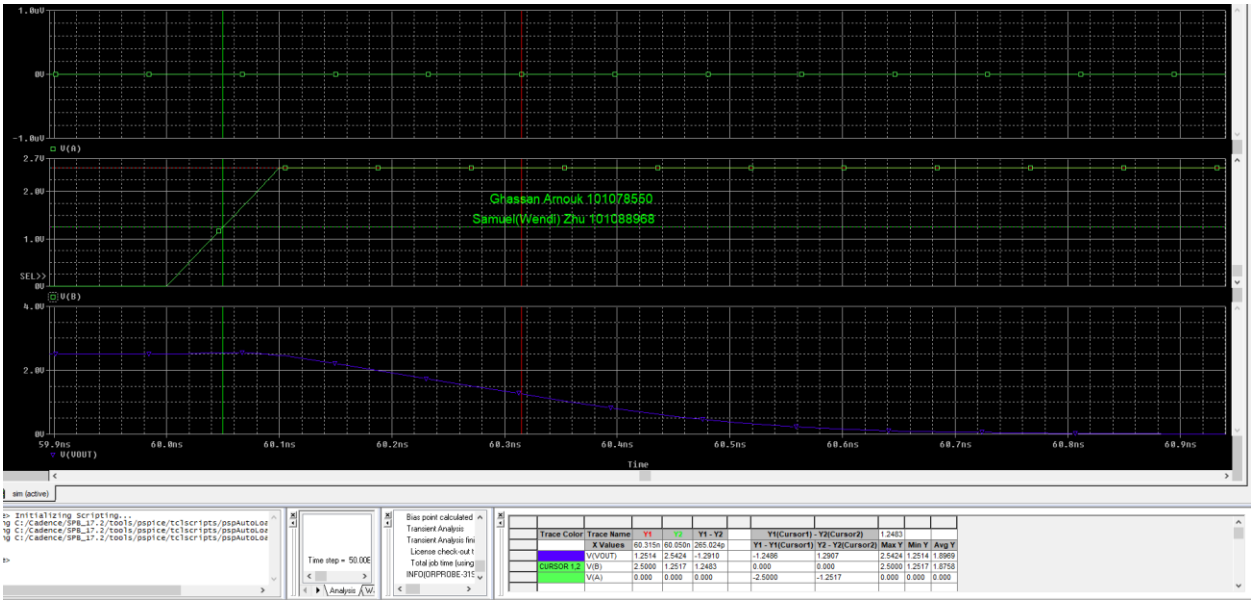

Figure 24 – Case 4: 00 > 01

Table 2 - Data Associated with Q14

Case Number	From AB	To AB	Delay (ps)	Rising/Falling
1	0 0	1 1	136.808	Falling
2	1 1	0 0	391.633	Rising
3	0 0	1 0	231.892	Falling
4	0 0	0 1	265.024	Falling

Q15. Which input combination defines the worst-case falling delay? What is this delay?

The input combination that defines the **worst-case** falling delay is from [00] to [01]. It has a long falling delay of 265.024ps.

Q16. Which input combination defines the best-case falling delay? What is this delay?

The input combination that defines the **best-case** falling delay is from [00] to [11]. It has a short falling delay of 136.808ps.

Q17. What is the relation between the numerical falling delay values of the two cases in Q15 and Q16? Can you explain why?

The relation between the numerical is that the worst-case falling delay value is almost doubled the best-case falling delay value (265.024/136.808 = 1.94). The best-case rising delay has two operating NMOS transistors connected in parallel which is faster than the worst-case rising delay that has only one operating NMOS.

Q18. Which input combination defines the rising delay?

The input combination that defines the rising delay is from [11] to [00]. It has a rising delay of 391.633ps.

References

(2006). *Lab 2: CMOS Combinational Logic*. Ottawa: Carleton Univeristy.