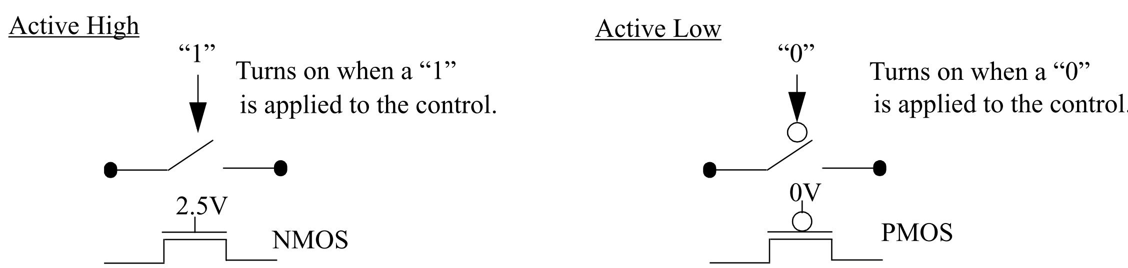
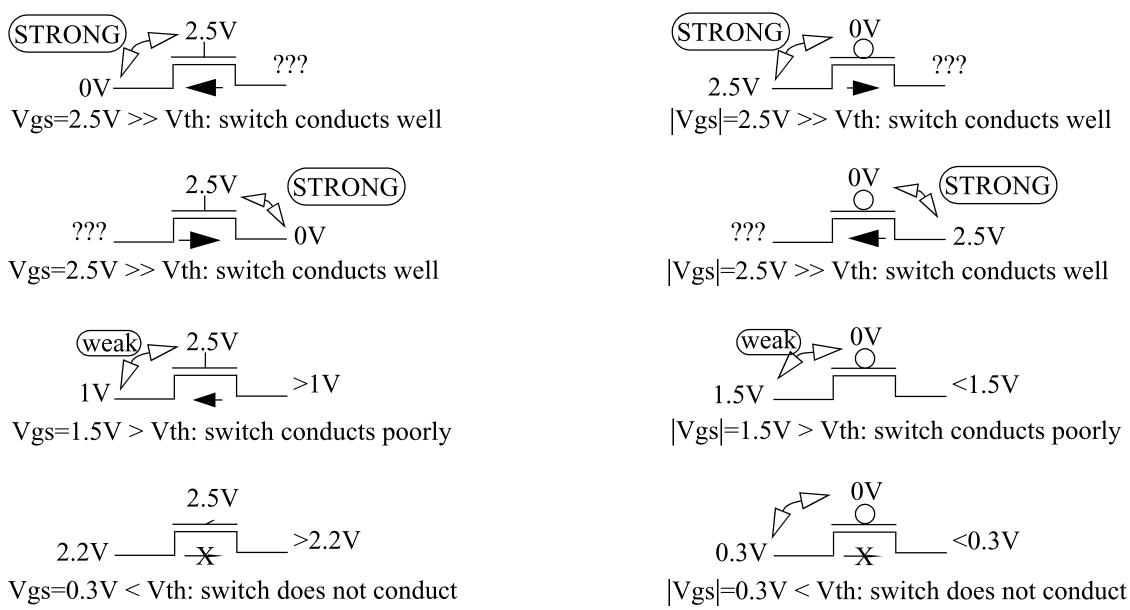
Lab 1 : MOSFET Switches

1. Design and Specification of MOSFET Devices

Digital circuits are implemented by arranging switches (typically Billions of them) together into logical networks. Today, metal-oxide field effect transistors (MOSFETs) are the most common way to implement these switches due to their ease of manufacture and high density. To implement logic networks, we typically use 2 types of switches. One that conducts with a “1” input, and one that conducts with a “0” input. These can be made with NMOS and PMOS transistors respectively.



But... for the switch to work, there must be a strong voltage difference from the gate to one of the terminals.



In this lab, you will modify some MOSFET based circuits, and simulate their use as switches.

1.1 Transistors as Switches

Digital gates are made from switches. FIGURE 2.1 shows four types of switch connections. We will look at how to use MOS transistors in each type of connection.

a) PMOS and NMOS as pull down switches.
b) PMOS and NMOS as pull up switches.

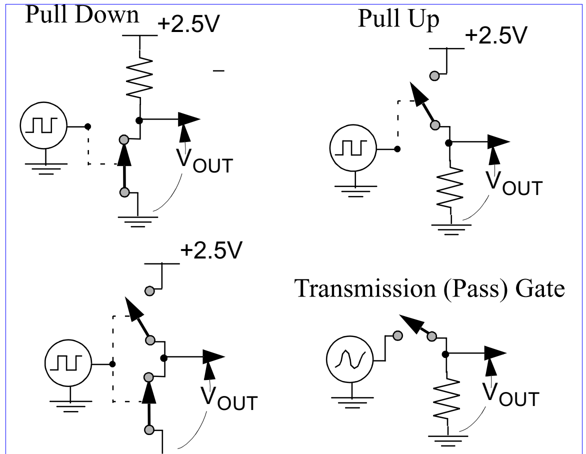


FIGURE 2.1

1.2 NMOS transistors.

1.2.1 Transistor Pulling Down

To use transistors in digital circuits one must know how to connect them to get the full 0V to 2.5V output swing

Here, with the NMOS gate at 2.5V, and the source at 0V, Vgs is large and so the transistor is strongly conducting.

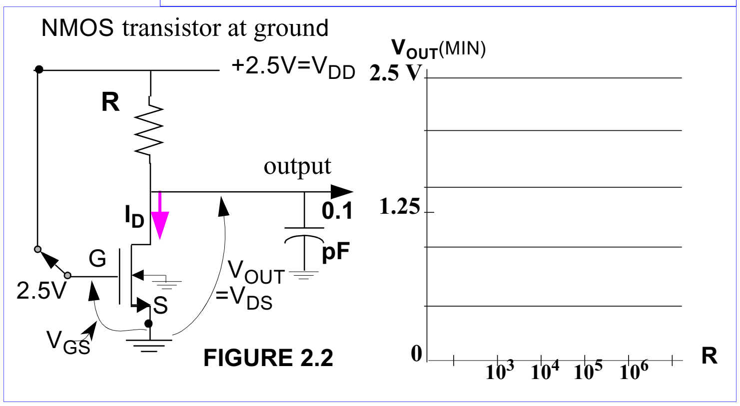


FIGURE 2.2

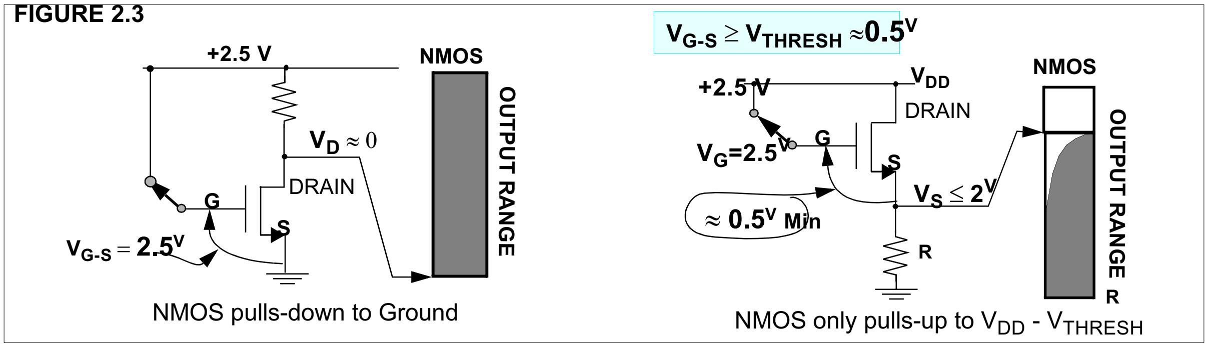
Q1. Simulate the circuit in Figure 2.2 to find the lowest output voltage Vout (min) with different values of R. (Try R=10 kOhm, R=25 kOhm, 50kOhm, 200kOhm, 1000 kOhm)
a) Plot the observations of Vout min versus R.
*b) What is the delay from Vin **rising to** 1.25V to Vout **falling to** 1.25V with R = 200 kOhm*
c) Considering how fast the output would take to charge and discharge (which is normally very important in digital circuits), what is the disadvantage of making R very high (eg. 1000 kOhm)?

The 0.1pF capacitor is stray circuit capacitance. Many MOS circuits have only stray capacitance (no resistors) in them, particularly if they feed only other MOS circuits.

Q2. a) With R= 1 kOhm, using simulations plot I_d versus V_{GS}.
b) Is there a sharply-defined threshold voltage, above which the transistor starts conducting?
c) From your plot, make an estimate for this value. Find corresponding current and compare it to the maximum current.

Q3. With R =200 kOhm, L = 1 um, sweep W (the width of the transistor) from 1um to 10um (at least 4 points), and for each value measure the delay from Vin rising to 1.25V --> Vout falling to 1.25. Plot the simulation sweep, and plot the measurement results for your report.

FIGURE 2.3



Q4. *Keep R = 200 kOhm, W = 1 um, sweep L (the length of the transistor) from 1um to 10um (at least 4 points), and for each value measure the delay from Vin rising to 1.25V --> Vout falling to 1.25. Plot the simulation sweep, and plot the measurement results for your report.*

1.2.2 Transistor at Top End (V_{DD}End) Of Circuit.

Now consider the NMOS transistor connected at the top of instead of the bottom (FIGURE 2.4). With the gate at 2.5V, the transistor is turned on, so one would expect V_{OUT} to be close to 2.5V. But is it really that close?

The Threshold Voltage

The MOS transistors used in gates have a minimum V_{GS} to turn on called V_{TH} (threshold voltage). Typically V_{TH} is 0.4 to 0.8V. Even at $V_{GS} = V_{TH}$ conduction is poor. One needs a voltage many times higher to give a low channel resistance. FIGURE 2.3 shows how even with V_G=2.5V, V_{GS} can be much smaller. Further the pull-up connection can never have an output above V_{DD}-V_{TH}.

The MORAL:

To STRONGLY turn on an NMOS transistor, we want a full strength control voltage (i.e. 2.5V) from the gate to one of its other terminals (source or drain). In a ‘normal’ digital circuit (Figure 2.2), the NMOS source is always grounded (at 0V) and so when it is turned ON, the full 2.5V is always across the transistor and it has a lot of ‘ummph!’. If the transistor is connected as in Figure 2.3b, then Vgd = 0 (absolutely no ‘ummph’ on that side) and as the output charges, Vgs will vary between 2.5V (lots of ‘ummph!’) to Vth (no ummph).

Q5. *Run simulations of the circuit in Figure 2.4 for different values of R, and*
a) find the maxiumum value of the output voltage(s), plotting them on a curve of Vout(MAX) vs R.
b) From this plot, what do you estimate the threshold voltage of the NMOS to be? Compare with Q2c

You should find the output (Source) can never rise closer than $V_{THRESHOLD}$.

Q6. *Comment: Would you think digital circuits would perform better when NMOS transistors were connected to pull the output up or down?*

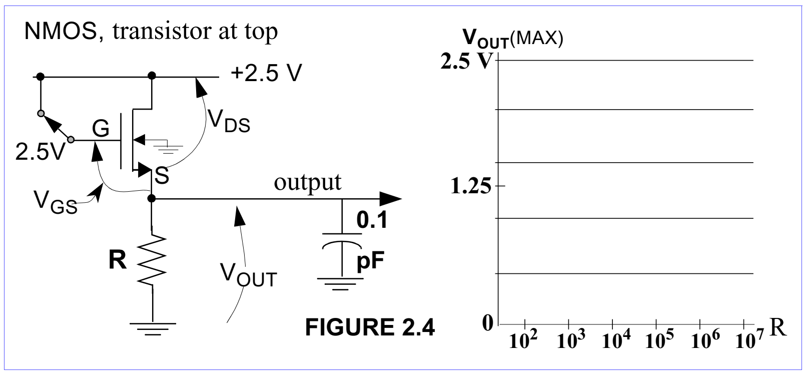


FIGURE 2.4

1.3 PMOS transistors

Just like NMOS transistors that wanted a full control swing to turn ON with a lot of ‘ummph!’, PMOS transistors are the same way. They turn on when the gate is at a LOWER voltage compared to either of the source or drain terminals. The stronger this (-ve) voltage swing is, the lower the ‘ON’ resistance and the better the switch.

Another thing to keep in mind is that due to the chemistry of things, PMOS transistors are 2-3x slower than NMOS ones.

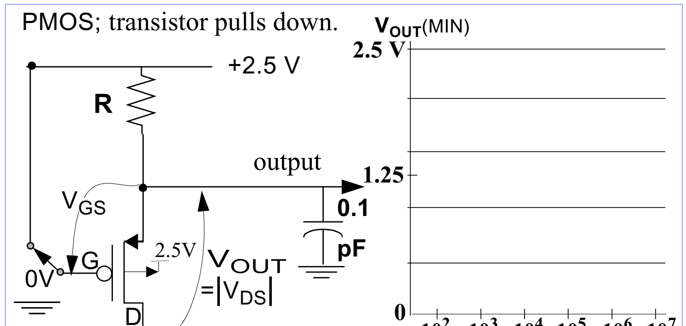


FIGURE 2.5

1.3.1 Pulling Down with a PMOS

Q7. Simulate the circuit of Figure 2.5 to find V_{OUT} for a range of R.
a) Plot the graph Vout min versus R.
b) How close can V_{OUT} get to 0V?
c) Estimate the threshold voltage of the PMOS transistor from this.

1.3.2 PMOS Transistor Pulling Up

Q8. Simulate the circuit of Figure 2.6 to plot V_{OUT} max vs R, particularly find the maximum V_{OUT}.

Q9. Comment: Would you think digital circuits would perform better when PMOS transistors were connected to pull the output up or down?

Q10. a) For R=200 kOhm, calculate the delay from Vin falling to 1.25V --> vout rising to 1.25V. Include this plot in your report.
b) How does this compare to the delay of the NMOS? (Refer to Q1)

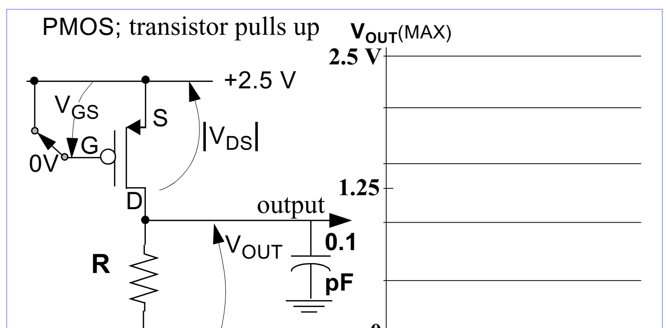


FIGURE 2.6

Deliverables:

- Print and Fill out a cover sheet.
- Show your completed work to a TA at the end of your section and Get signed.
- Answer all the questions and submit it with supporting printouts (Only answer the questions. This report does not need introduction, conclusion etc)
- Attach your signed coversheet as the first page of your report.