1) Using what you learned from Lab 1, answer the first question from Lab 2 (found in the 'Lab 2 Combinational CMOS Logic' link):
"Classify the inverter circuits of Figure 2.2 as "won't work," "will work with poor output swing," and "will work well". Explain which one does not have the inverting structure."

2) Assuming the transistors are all the same size, would you expect the rise delay and fall delay in an inverter to be the same? Why? If not, which is larger and why?

3) Using the data you collected in the previous lab, what transistor size (W/L) ratio between the N and P type would you expect gives equal delays (do not estimate)?

4) Sketch a CMOS NOR gate using 4 transistors.