MOSFET Switches

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Lab 1 Report

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1.2.1 Transistor Pulling Down

Q1: Simulate the circuit in Figure 2.2 to find the lowest output voltage V_{out} (min) with different values of R. (Try R=10 kΩ, R=25 kΩ, 50kΩ, 200 kΩ, 1000 kΩ)

a) Figure 1 below shows the plot of V_{out} Vs. R for different values of R.

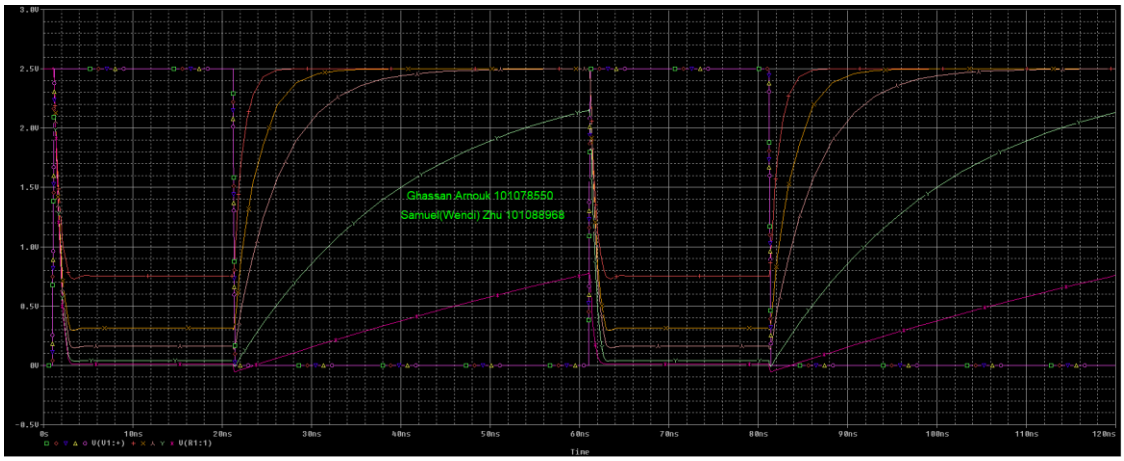

Figure 1 - Plot of V_{out} Vs. R = 10 kΩ, 25 kΩ, 50 kΩ, 200 kΩ, 1000 kΩ.

Table 1 - Minimum V_{out} VS. R

R (kΩ)	10	25	50	200	1000
V_{out} min (mV)	754	317	160.5	40.4	8.1

Table 1 above shows the minimum V_{out} data collected using the cursor for R = 10 kΩ, 25 kΩ, 50 kΩ, 200 kΩ, 1000 kΩ.

Figure 2 below shows the plot of min V_{out} Vs. R. The min V_{out} decreases as R increases, and V_{out} min was close to 0 for a large value of R. This indicates that the NMOS transistor was good at pulling down the output voltage.

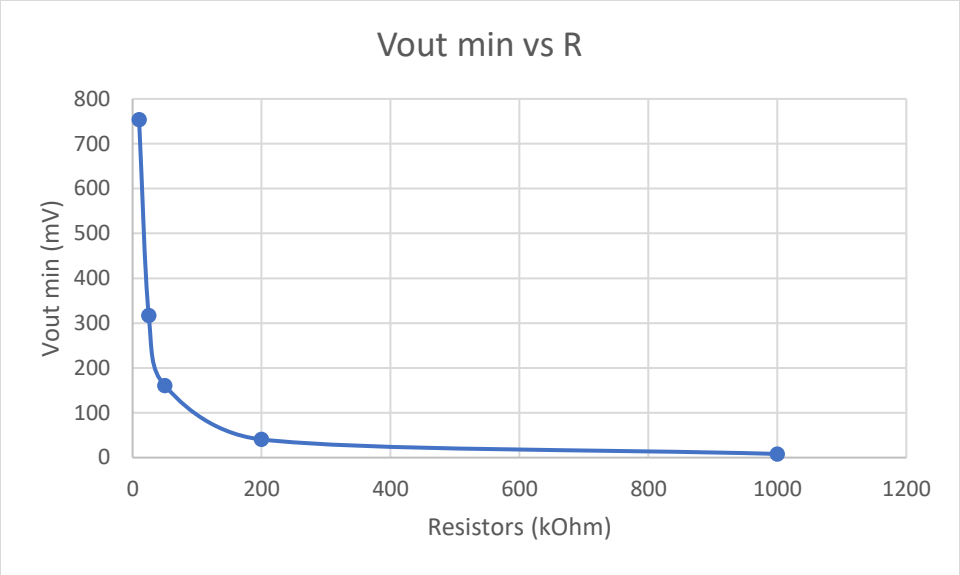

Figure 2 - Plot of min V_{out} Vs. R for NMOS Transistor Pulling Down

b) What is the delay from V_{in} rising to 1.25V to V_{out} falling to 1.25V with R = 200 kΩ

Figure 3 below shows the simulation results to find the delay time from V_{in} rising to 1.25V to V_{out} falling to 1.25V with R = 200 kOhm. Note that the delay time was obtained using the cursor values shown at the bottom right of the screen. Delay time = 434.069 ps.

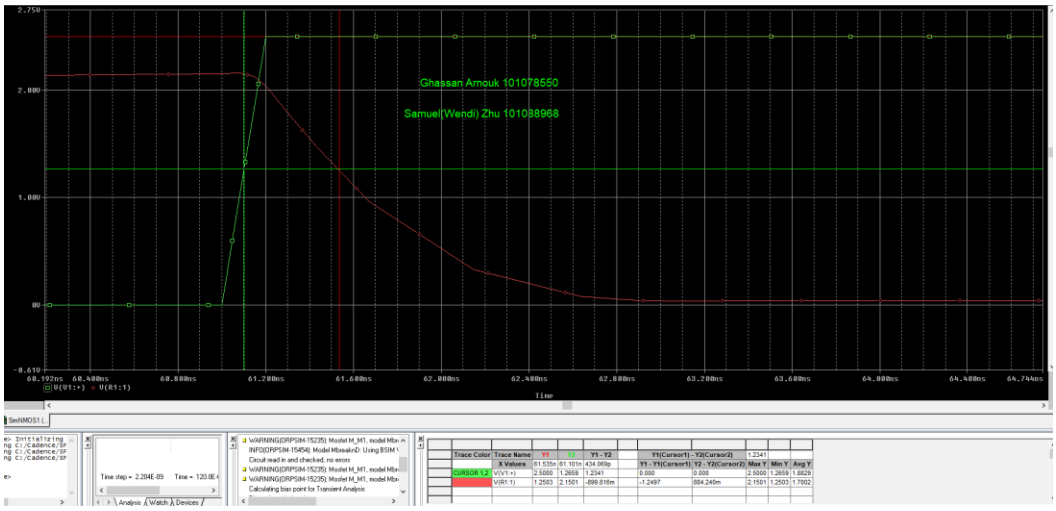

Figure 3 - Plot for Delay Time from V_{in} rising to 1.25V to V_{out} falling to 1.25V with R = 200 kΩ

c) Considering how fast the output would take to charge and discharge (which is normally very important in digital circuits), what is the disadvantage of making R very high (eg. 1000 kΩ)?

Figure 4 below shows the simulation results for R = 1000 kΩ.

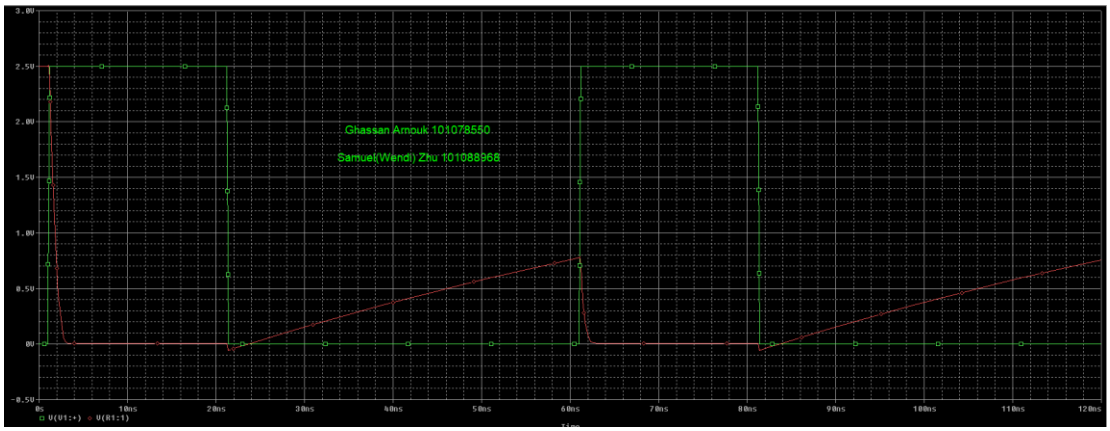

Figure 4 - Plot for V_{in} and V_{out} for R = 1000 kΩ

The time for output to charge and discharge will be increased as R increases because the RC time constant, τ, increased. This would limit the time needed for the output voltage to fully charge for high frequency input. The disadvantage of making R very high is the circuit would not respond quick enough for high frequency input.

Q2

a) With R = 1 kΩ, using simulations *plot* I_d versus V_{GS}

Figure 5 below shows the simulation plot of I_d Vs. V_{GS} with R = 1 kΩ.

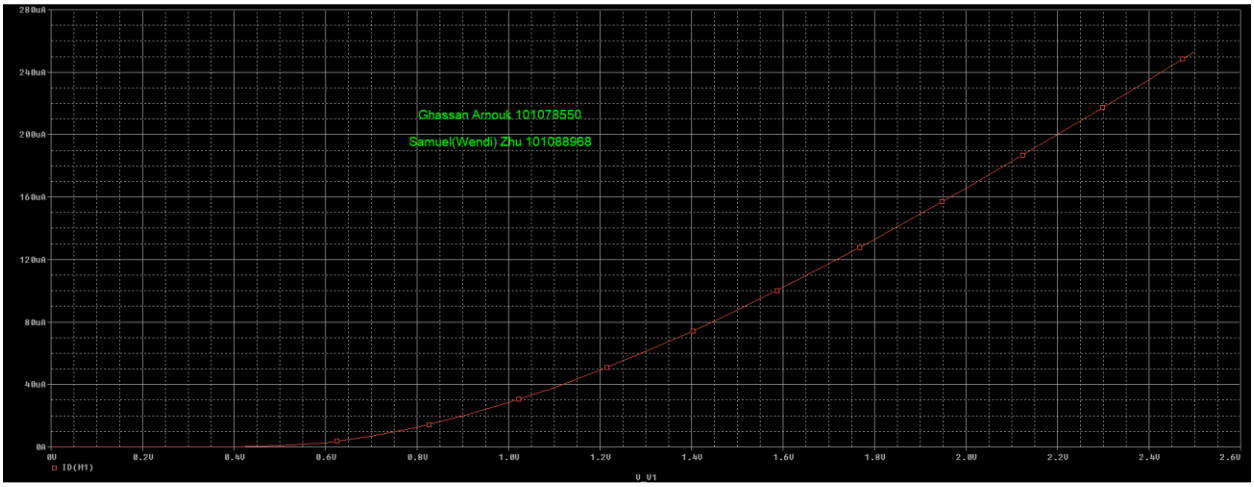

Figure 5 - Simulation Plot of Id Vs. V_{GS}

b) Is there a sharply defined threshold voltage, above which the transistor starts conducting?

The transistor starts conducting at roughly 0.43V which is the threshold voltage.

c) From your plot, make an estimate for this value. Find corresponding current and compare it to the maximum current.

The threshold voltage is approximately 0.43 V since the transistor starts conducting with current I_d = 2.75nA. The maximum current, taken from the plot, is 253uA, which occurred at 2.5V. The corresponding current of when the transistor starts conducting was very small in comparison to the maximum current.

Q3: With R = 200 kΩ, L = 1um, sweep W (the width of the transistor) from 1 um to 10um (at least 4 points), and for each value measure the delay from V_{in} rising to 1.25 → V_{out} falling to 1.25. *Plot the simulation sweep*, and plot the measurement results for you report.

Figure 6 below shows the simulation sweep plot of W from 1um to 10um with R = 200 kΩ and L = 1um.

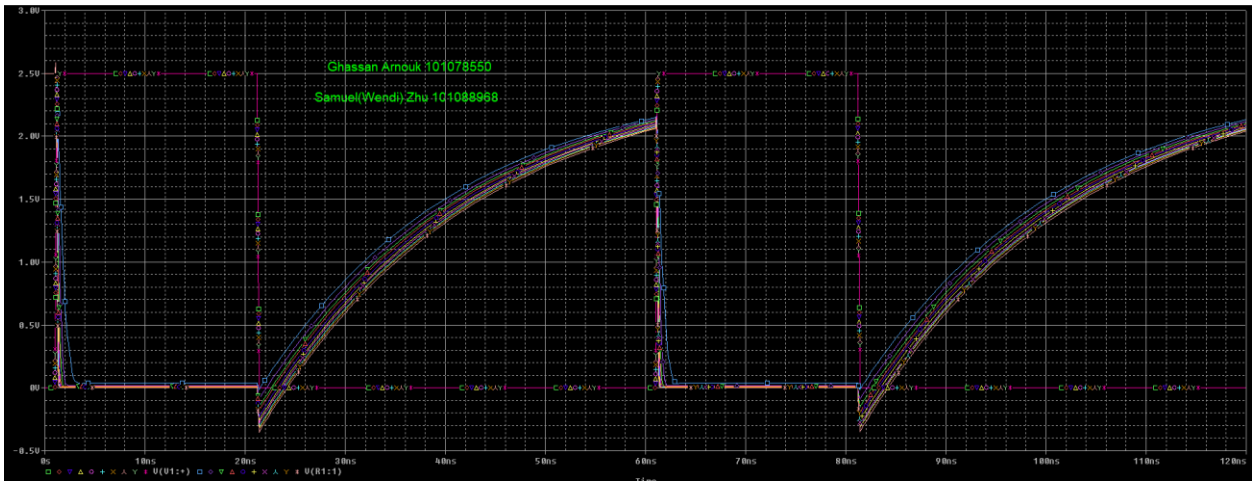

Figure 6 – Simulation Sweep of W from 1um to 10um with R = 200 kΩ and L = 1um

Table 2 below summarizes the collected data using cursors for delay time versus W.

Table 2 - Collected Data Using Cursors for Delay Time Vs. W

W (um)	1	2	4	6	8	10
Delay time (ps)	434	237	142	112.66	98.32	87.12

Figure 7 below shows the plot for delay time Vs. W. The delay time decreases as the width of the transistor increases.

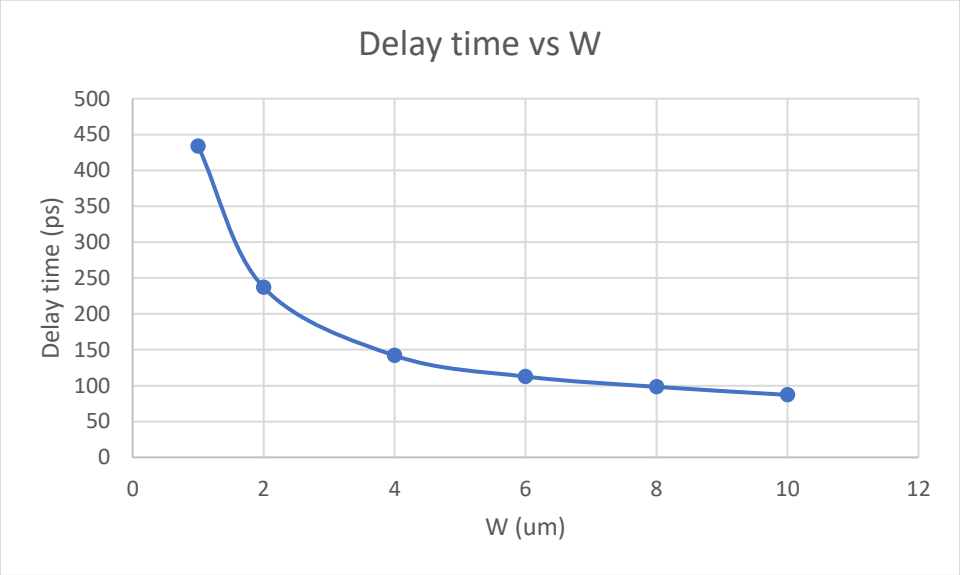

Figure 7 - Plot of Delayed Time Vs. W

Q4: Keep R = 200 kΩ, W = 1um, sweep L (the length of the transistor) from 1um to 10um (at least 4 points), and for each value measure the delay from V_{in} rising to 1.25V → V_{out} falling to 1.25. *Plot the simulation sweep*, and plot the measurement results for your report.

Figure 8 below shows the simulation sweep plot for L from 1um to 10um with R = 200kΩ and W = 1um.

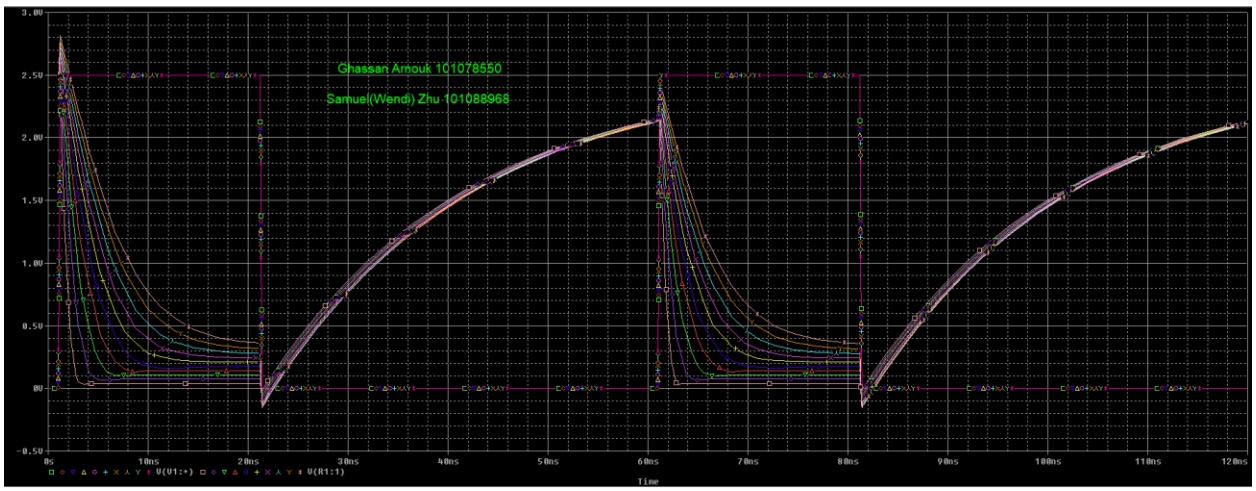

Figure 8 – Simulation Sweep for L from 1um to 10um with R = 200kΩ and W = 1um

Table 3 summarizes the collected data using the cursors for delay time Vs. L.

Table 3 - Collected Data Using Cursors for Delay Time Vs. L.

L (um)	1	2	4	6	8	10
Delay time (ps)	437	771	1544	2400	3484	4400

Figure 9 below shows the plot of delay time Vs. L. They delay time increases as the length of the transistor increases.

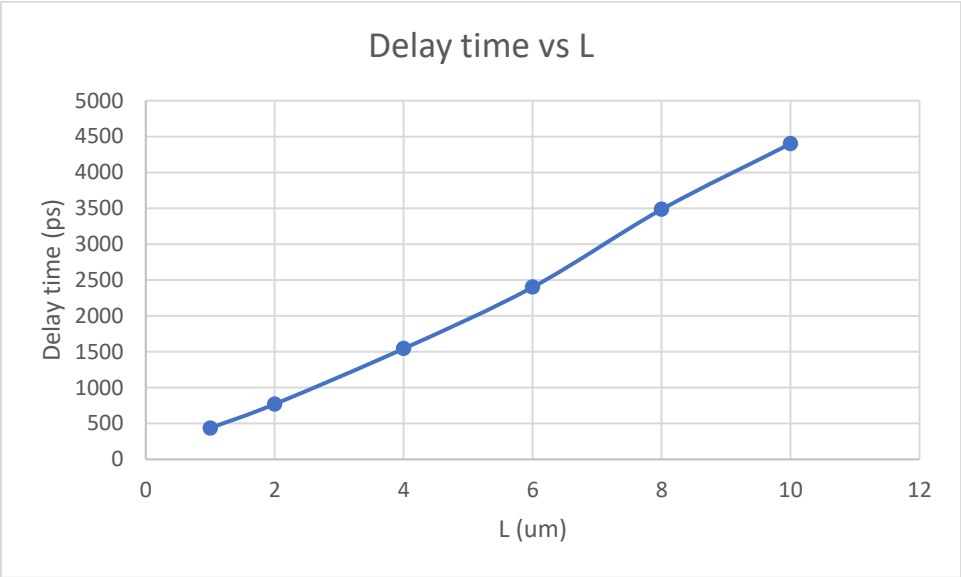

Figure 9 – Plot of delay Time Vs. L

1.2.2 Transistor at Top end (V_{DD}End) of Circuit.

Q5: Run simulations of the circuit in Figure 2.4 for different values of R, and

a) Find the maximum value of the output voltage(s), plotting them on a curve of V_{out}(MAX) Vs. R

Figure 10 below shows the simulation results for R = 10kΩ, 25kΩ, 50kΩ, 200kΩ, and 1000kΩ.

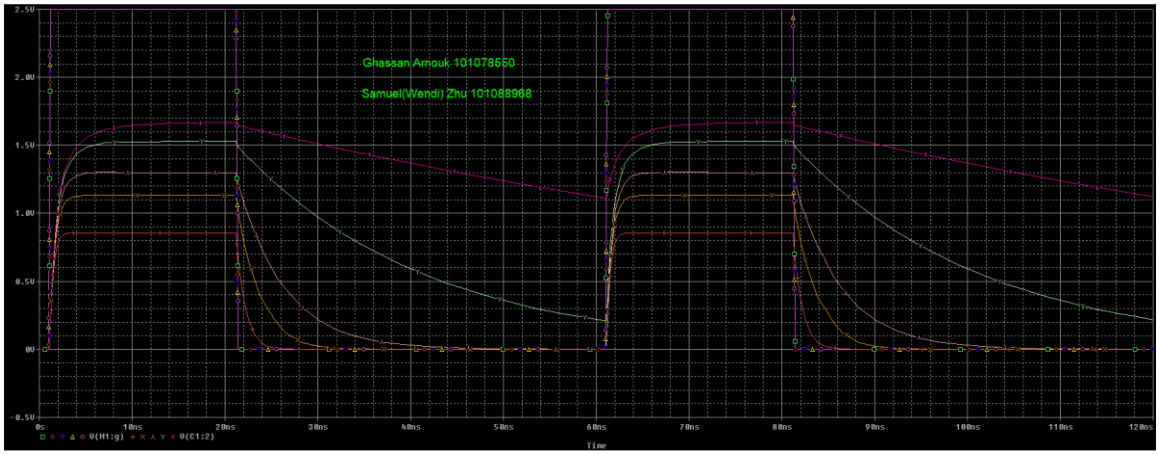

Figure 10 - Simulation of the Circuit in Fig. 2.4 for R =10kΩ, 25kΩ, 50kΩ, 200kΩ, and 1000kΩ

Table 4 below shows the collected data using cursors for V_{out} max Vs. R.

Table 4 - V_{out} Max Vs. R

R (kΩ)	10	25	50	200	1000
V_{out} max (mV)	856	1132.5	1300	1527	1665

Figure 11 shows the plot of V_{out} max Vs. R

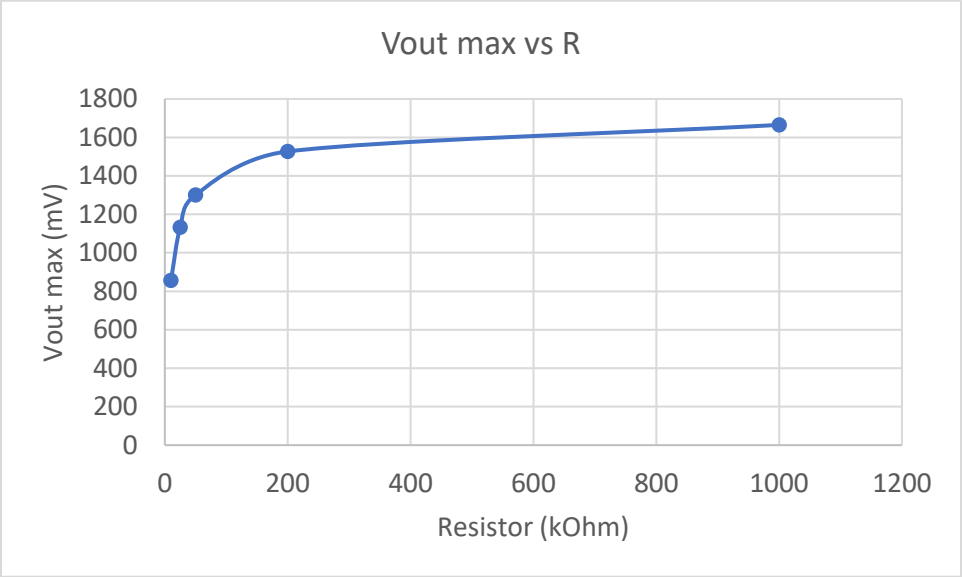

Figure 11 - Plot of V_{out} Max Vs. R

b) From this plot, what do you estimate the threshold voltage of the NMOS to be? Compare with Q2c.

The threshold voltage was estimated as followed:

$$V_{TH} \approx 2.5 - 1.7 = 0.8\,V$$

From Q2c, the threshold voltage was estimated as 0.43V. The V_{TH} estimated here is larger than the threshold voltage estimated from Q2c.

Q6: Comment: Would you think digital circuits would perform better when NMOS transistors were connected to pull the output up or down?

The digital circuits would perform better when NMOS transistors were connected to pull the output down.

Using Figure 11 above, the highest V_{out} that the NMOS transistor could pull up was roughly 1.7V, which was not very close to the supply voltage 2.5V. Using Figure 2 above, the minimum V_{out} that the NMOS transistor could pull down was very close to 0V. Therefore, digital circuits would perform better when NMOS transistors were connected to pull the output down.

1.3 PMOS Transistor

1.3.1 Transistor Pulling Down

Q7: Simulate the circuit in Figure 2.5 to find V_{out} for a range of R

Figure 12 below shows the simulation plot of V_{out} for R = 10kΩ, 25kΩ, 50kΩ, 200kΩ, 1000kΩ.

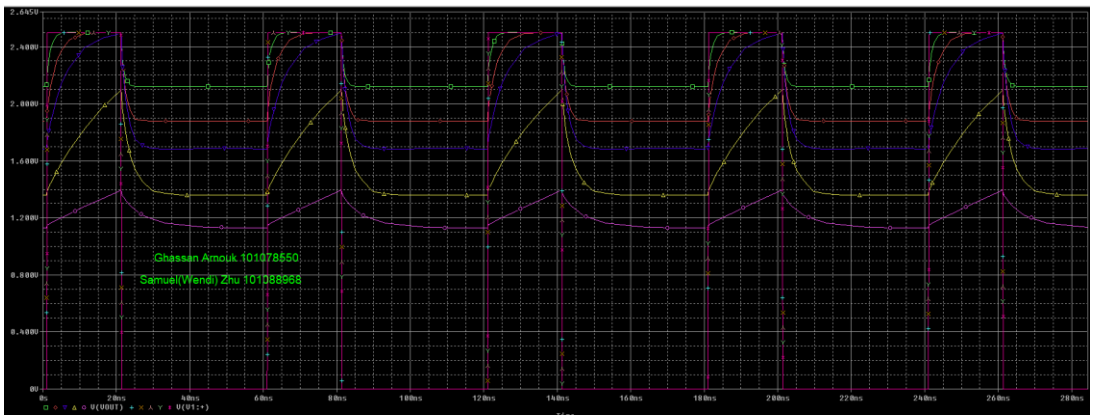

Figure 12 - The Simulation Plot of V_{out} for R =10kΩ, 25kΩ, 50kΩ, 200kΩ, 1000kΩ.

a) Plot the graph V_{out} min versus R.

Table 5 shows the data obtained using the cursors for V_{out} min Vs. R.

Table 5 - V_{out} min Vs. R

R (kΩ)	10	25	50	200	1000
V_{out} min (V)	2.1232	1.879	1.6847	1.3587	1.1309

Figure 13 below shows the graph of V_{out} min Vs. R.

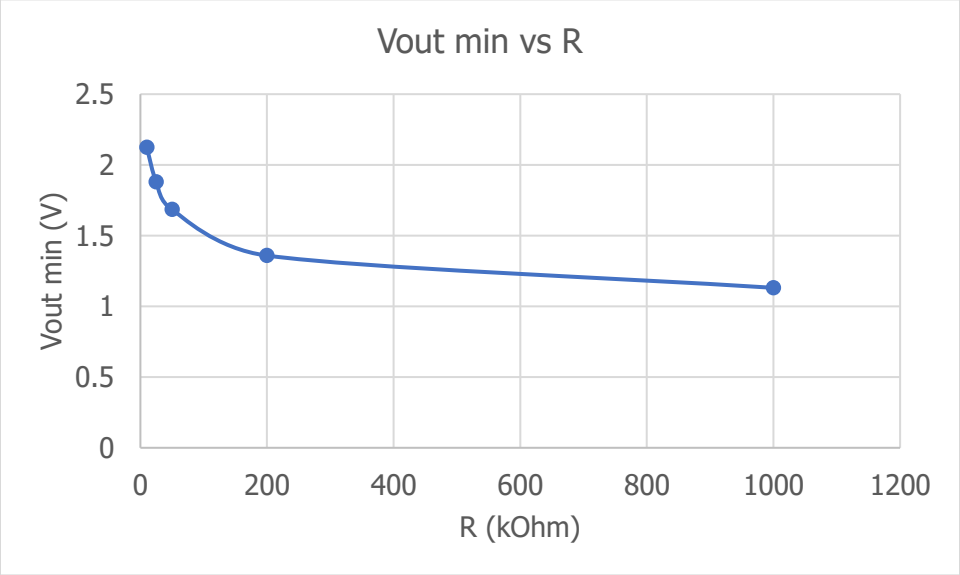

Figure 13 - V_{out} min Vs. R for Pulling Down with a PMOS

b) How close can V_{out} get to 0V?

The minimum of V_{out} could go down to roughly 1V. This value was not close to 0.

c) Estimate the threshold voltage of the PMOS transistor from this.

The threshold voltage was estimated from Figure 13.0 as followed:

$$|V_{TH}| \approx 1V$$

1.3.2 PMOS Transistor Pulling Down

Q8: Simulate the circuit in Figure 2.6 to plot V_{out} max Vs. R, particularly find the maximum V_{out}

Figure 14 below shows the simulation results of the circuit of Fig. 2.6 for V_{out} versus R = 10kΩ, 25kΩ, 50kΩ, 200kΩ, 1000kΩ.

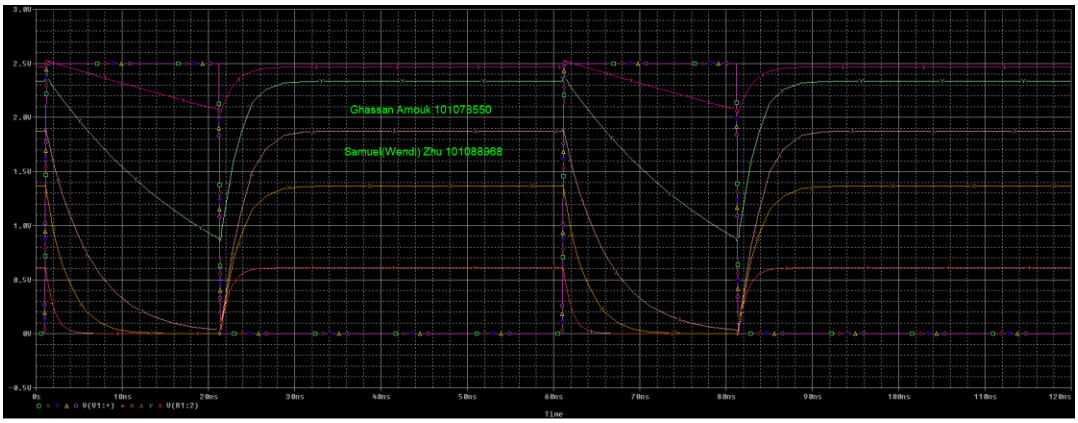

Figure 14 - Simulation Plot for V_{out} Vs. R for R =10kΩ, 25kΩ, 50kΩ, 200kΩ, 1000kΩ.

Table 6 below summarizes measured data using cursors for V_{out} max Vs. R.

Table 6 - V_{out} min Vs. R

R (kΩ)	10	25	50	200	1000
V_{out} max (V)	0.609	1.3653	1.8739	2.3343	2.4664

The maximum V_{out} from the measured data was 2.4664V, which is very close to the supply voltage 2.5V.

Figure 15 below shows the plot of V_{out} max Vs. R.

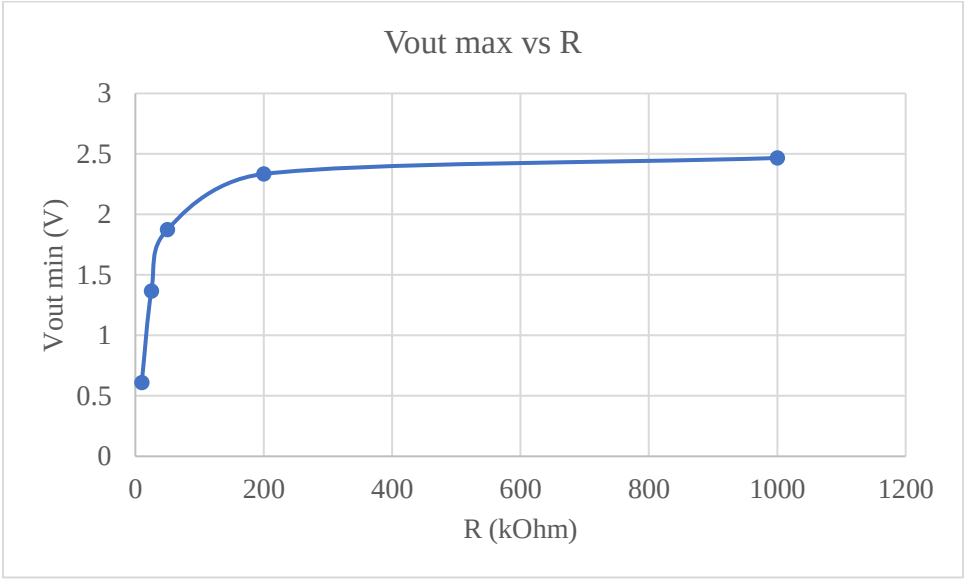

Figure 15 - V_{out} Max Vs. R for PMOS Transistor Pulling Up

Q9: Comment: Would you think digital circuits would perform better when PMOS transistors were connected to pull the output up or down?

Digital circuits would perform better when PMOS transistors were connected to pull the output up.

When pulling down with a PMOS transistor (as shown in section 1.3.1), the lowest V_{out} is roughly 1V due to the threshold voltage, and V_{out} is not close to 0. When pulling up with a PMOS transistor, the highest V_{out} is roughly 2.5V, which is close to the supply voltage. Therefore, PMOS transistors were better to connected to pull the output up.

Q10

a) For R = 200 kΩ, calculate the delay from V_{in} falling to 1.25V → V_{out} rising to 1.25V. Include this plot in your report.

Figure 16 below shows the simulation plot of V_{in} and V_{out} with R = 200 kΩ.

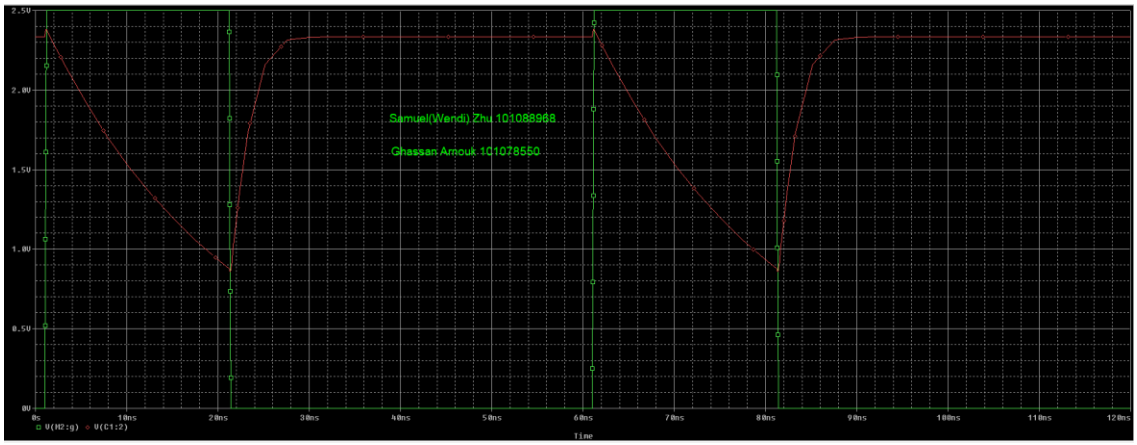

Figure 16 - The Simulation Plot for V_{in} and V_{out} with R = 200 kΩ

Figure 17 below shows the zoomed-in plot to calculate the delay time from V_{in} falling to 1.25V to V_{out} rising to 1.25V. Note that the cursors values are shown in the bottom right corner of the plot.

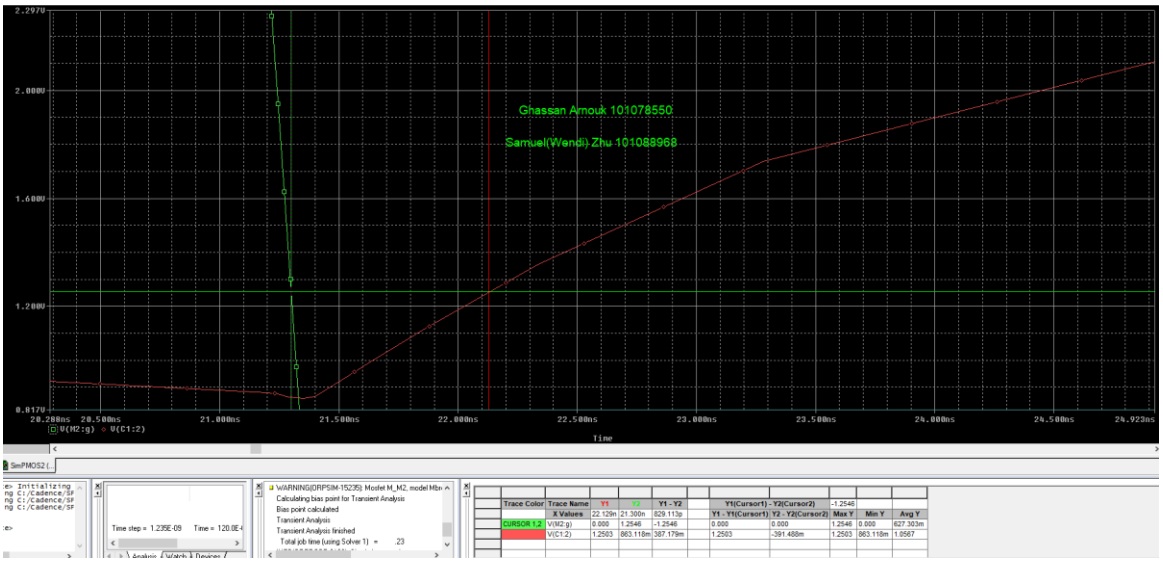

Figure 17 - Zoomed-in Plot to Calculated the Delay Time

The time for the first cursor was $t_1 = 22.129\, ns$.

The time for the second cursor was $t_2 = 21.3\, ns$.

Time delay was calculated as: $Time\ delay = t1 - t2 = 829.113\, ps$.

b) How does this compare to the delay of the NMOS? (Refer to Q1)

The delay time for PMOS was around 829 ps, and the delay time for NMOS was around 434 ps. Therefor, the delay time for PMOS is larger than the delay time for NMOS.