CMOS Sequential Logic Gates

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ELEC 3500B
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Lab 3 Report

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List of Figures

1. The Mux

Q1. Plot the output waveforms showing the ctrl and y signals. Explain what is happening when the CLK is high and when the CLK is low.

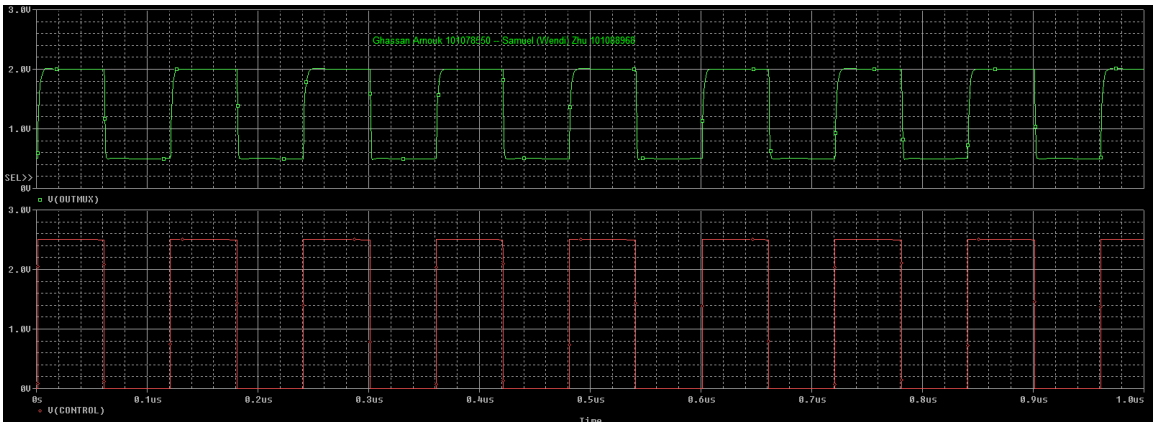
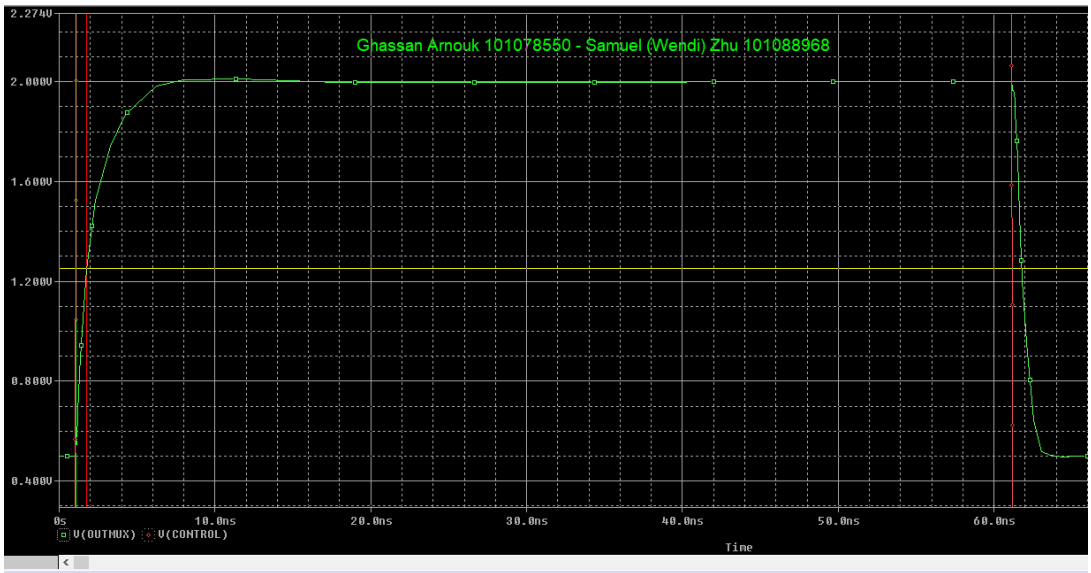


Figure 1 - Output Waveforms Showing ctrl and y Signals

When the clock is high, the V_{out} equals to V_d, which is 2V. When the clock is low, the V_{out} equals to V_q, which is 0.5V. The circuit acts as a mux.

Q2. Record t_{CHYV} and the similar signal t_{CLYV} (Control Low Y Valid).

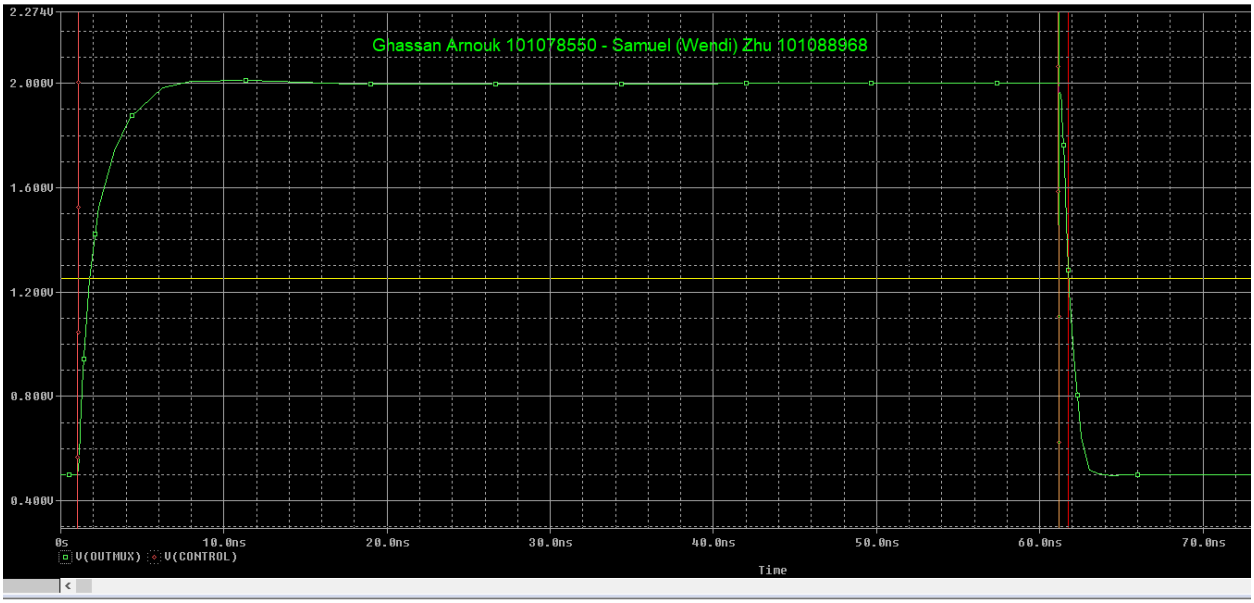
Figure 2 below shows the time from Control High to Y Valid, **t_{CHYV} = 705.728 ps**.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		0.000		
	X Values	1.7558n	1.0501n	705.728p		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1	V(OUTMUX)	1.2520	521.075m	730.968m		0.000	-730.968m	1.2520	521.075m	886.559m
CURSOR 2	V(CONTROL)	2.5000	1.2520	1.2480		1.2480	0.000	2.5000	1.2520	1.6760

Figure 2 - Measured t_{CHYV}

Figure 3 below shows the time from Control High to Y Valid, $\mathbf{t_{CLYV}}$ **= 657.557 ps**.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		0.000		
	X Values	61.798n	61.150n	647.557p		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1	V(OUTMUX)	1.2520	1.9762	-724.178m		0.000	724.178m	1.9762	1.2520	1.6141
CURSOR 2	V(CONTROL)	0.000	1.2520	-1.2520		-1.2520	0.000	1.2520	0.000	626.022m

Figure 3 - Measured t_{CLYV}

2. The D-latch

Q3. What components are added to your D latch (Ref: Figure 2.15b) to make it work with transmission gates.1 Why are they necessary?

A 20kΩ resistor and a capacitor (perhaps parasitic capacitance) are added to the D latch at the Q output.

Figure 4 shown the schematic for the D latch.

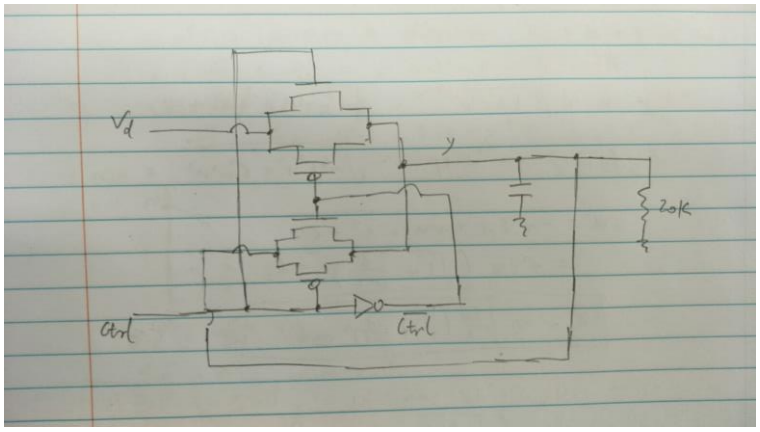


Figure 4 - Schematic for the D latch

One possible reason that the capacitor is necessary is to hold the charge for the output. The resistor is necessary for the output voltage since V = IR. For example, if the output of the latch is high, the capacitor will be charged, and there will be a small current flowing through R to provide an output voltage as high. If the output of the latch is low, the capacitor will not be charged. There will be no current flowing though R, and the output voltage is low. However, the D latch may fail to hold the bit after some time because the capacitor will discharge over time. In this lab, we did **not** add the capacitor and resistor, and the simulation worked properly.

Q4. Sketch part of your test waveform that proves the latch functions as a transparent latch.

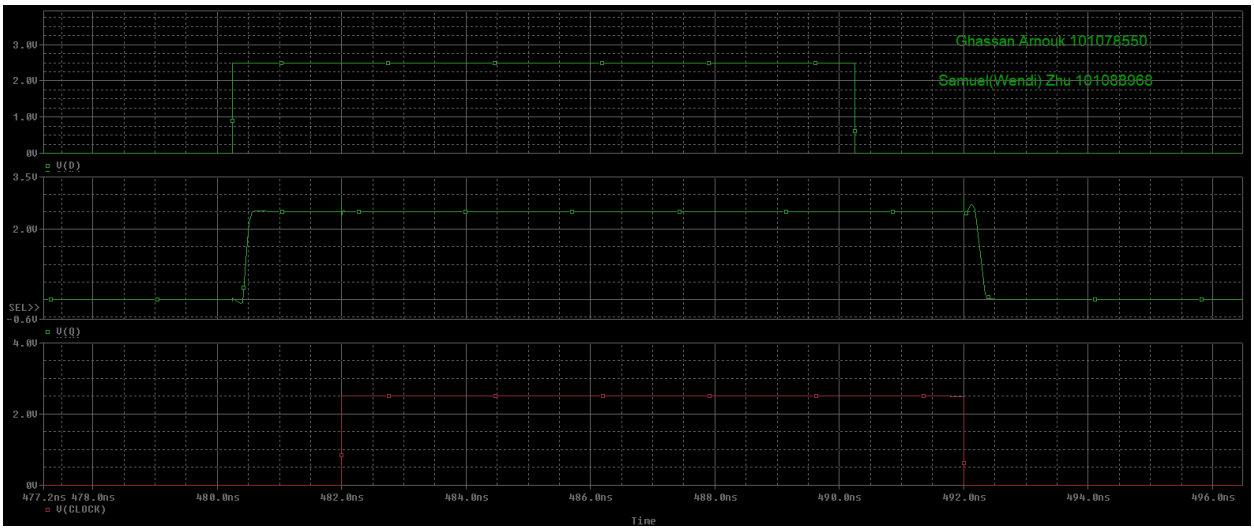
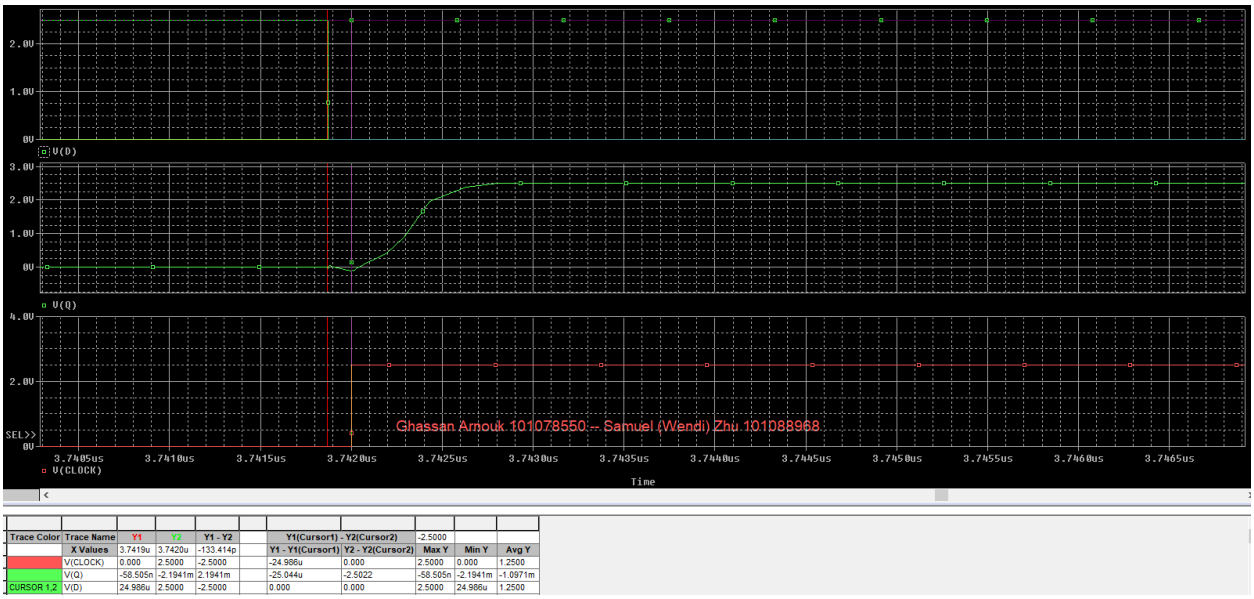


Figure 5 - Output Waveform when Latch Functioning as a Transparent Latch

The circuit acts as a transparent low latch. For example, when the clock (Enable signal) is low, V(Q) is following V(D). When the clock is high, the V(Q) will latch the signal and ignore the changes in V(D).

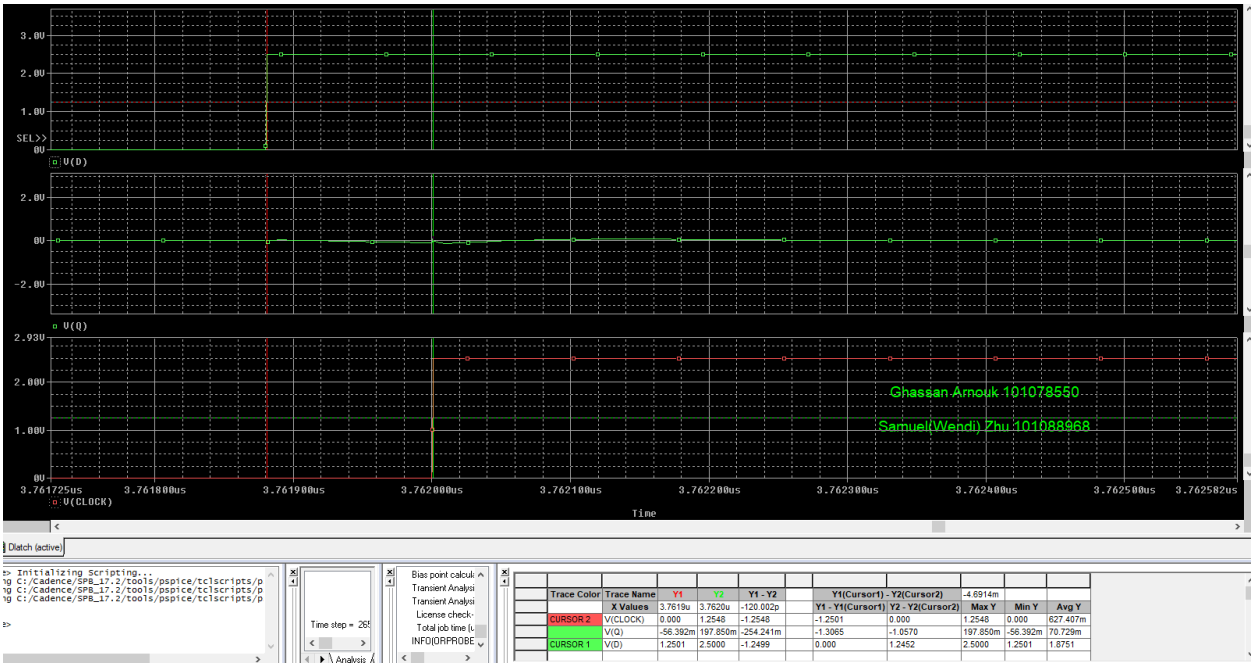
Q5. Measure the setup time using your sliding waveforms. You may want to extend the time of the simulation. Show a plot of where you measured the setup time.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		-2.5000		
	X Values	3.7419u	3.7420u	-133.414p	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(CLOCK)	0.000	2.5000	-2.5000	-24.986u	0.000	2.5000	0.000	1.2500
	V(Q)	-58.505n	-2.1941m	2.1941m	-25.044u	-2.5022	-58.505n	-2.1941m	-1.0971m
CURSOR 1,2	V(D)	24.986u	2.5000	-2.5000	0.000	0.000	2.5000	24.986u	1.2500

Figure 6 - Last valid Setup Time Using Sliding Waveforms

The last valid setup time (i.e. V(Q) goes flat and does not follow V(D) when clock is low) is **133.414 ps**.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)		-4.6914m		
	X Values	3.7619u	3.7620u	-120.002p	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 2	V(CLOCK)	0.000	1.2548	-1.2548	-1.2501	0.000	1.2548	0.000	627.407m
	V(Q)	-56.392m	197.850m	-254.241m	-1.3065	-1.0570	197.850m	-56.392m	70.729m
CURSOR 1	V(D)	1.2501	2.5000	-1.2499	0.000	1.2452	2.5000	1.2501	1.8751

Figure 7 - First invalid Setup Time Using Sliding Waveforms

The first invalid setup time is **120 ps**.

Q6. Measure the new setup time. Comment on it.

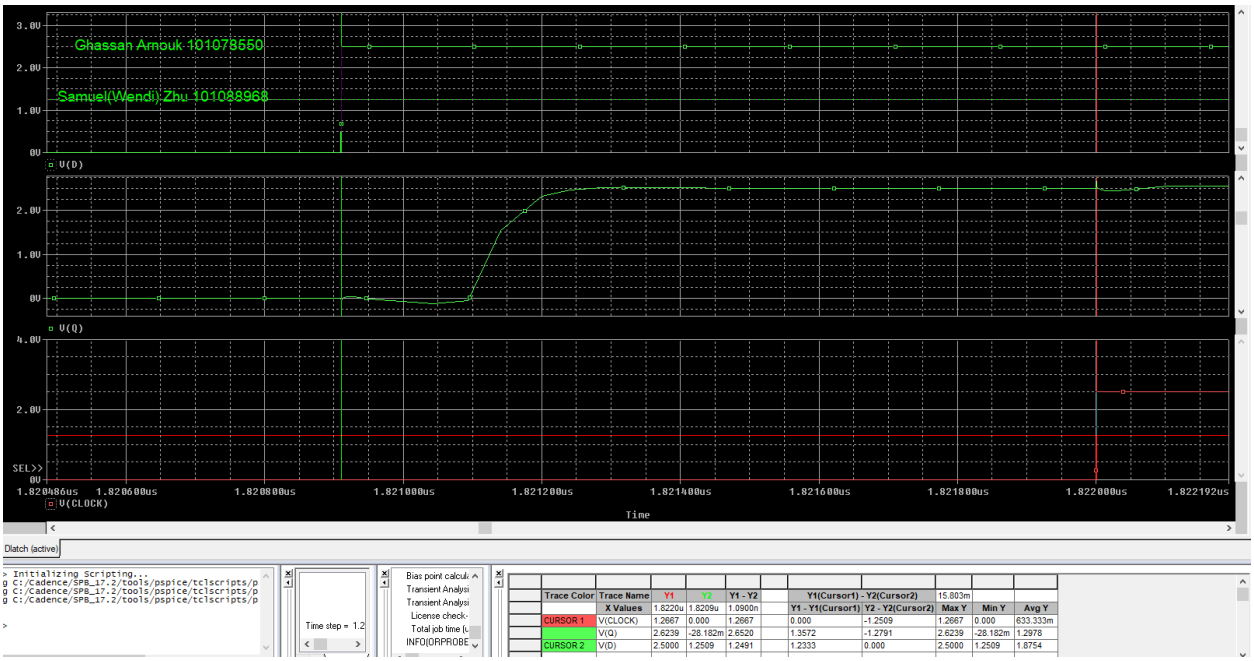


Figure 8 - Setup time for last valid after adding 0.5pf capacitor

The new last valid setup time after adding 0.5pf capacitor is **1.09ns.**

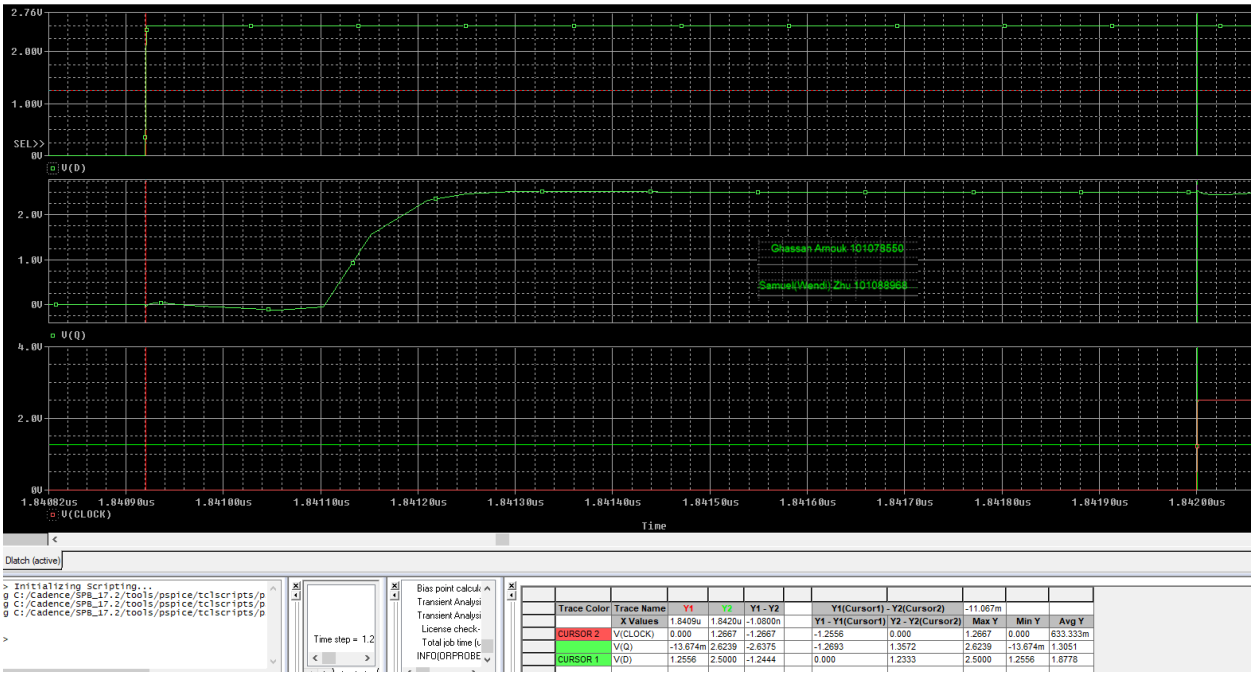


Figure 9 - Setup time for first invalid after adding 0.5pf capacitor

The new first invalid setup time after adding 0.5pf capacitor is **1.08ns**. The difference between the last valid setup time and the first invalid setup time was 0.01ns.

3. The D Flip-Flop

Q7. Measure the setup time of the D flip-flop using the sliding waveform.

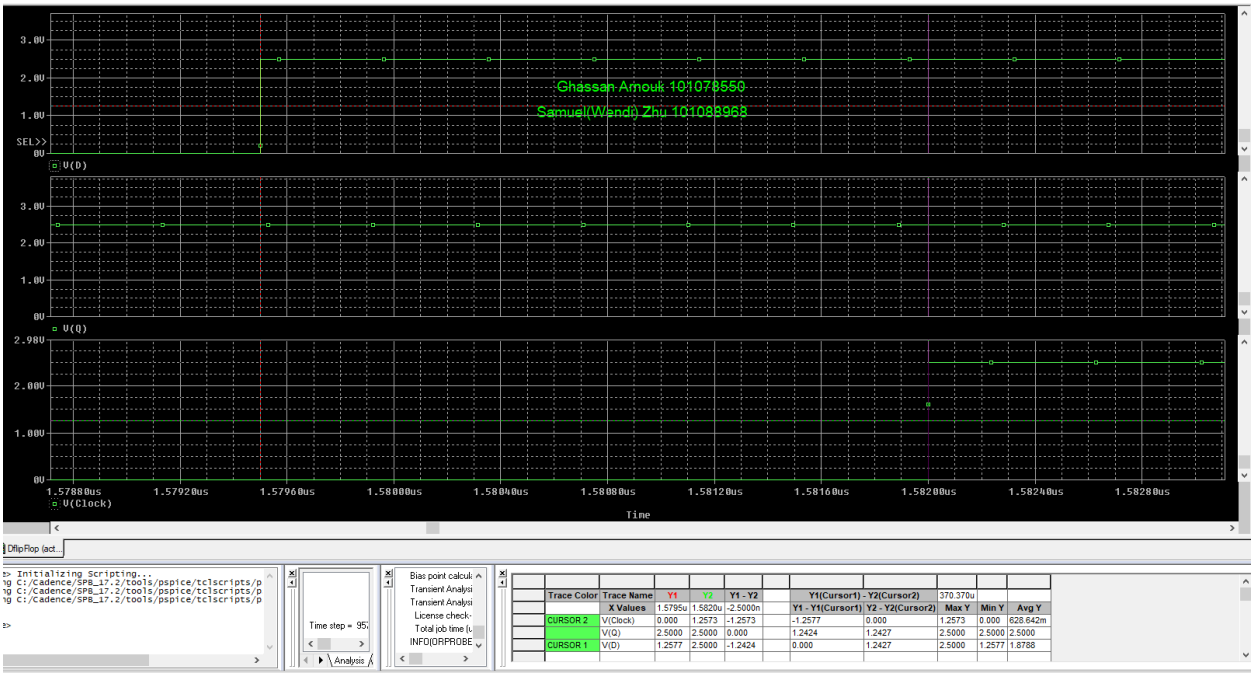


Figure 10 - Last valid Setup time for D flip-flop

The last valid setup time for D flip-flop is **2.5ns**.

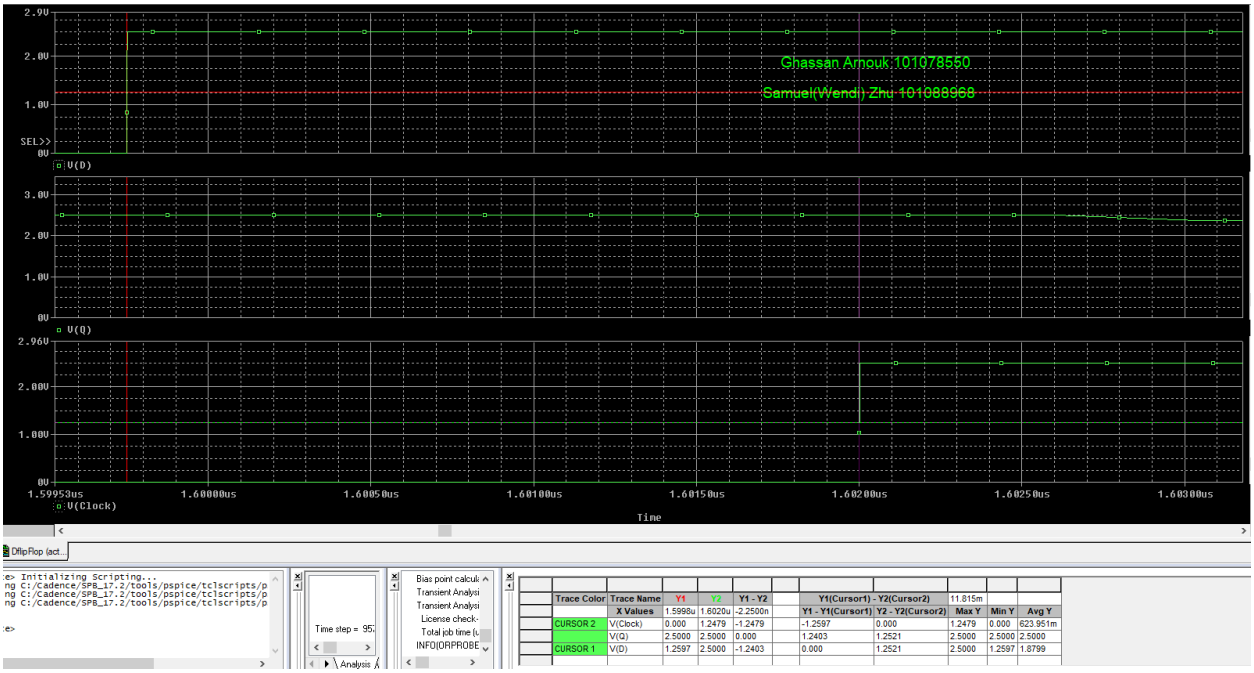


Figure 11 - First invalid Setup time for D flip-flop

The first invalid setup time for D flip-flop is **2.25ns**. The difference between the last valid setup time and the first invalid setup time is 0.25ns.