

Multi-Output Circuits: Encoders, Decoders, and Memories

Introduction

Boolean expressions are used to output a Boolean function of a number of variables. Dataflow construct like `assign` can be used to model such functions. There are circuits which have multiple outputs and multiple inputs. In this lab you will design encoders, decoders, and read only memories. Please refer to the Vivado tutorial on how to use the Vivado tool for creating projects and verifying digital circuits.

Objectives

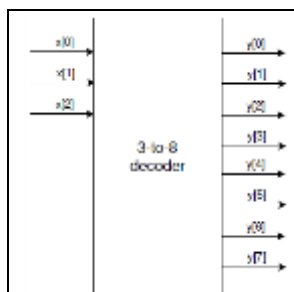
After completing this lab, you will be able to:

- Design multi-output decoder circuits using behavioral modeling
- Design encoders using behavioral modeling
- Use read only memories using `reg` data type and `$readmemb` system task available in Verilog

Multi-output Decoder Circuits

Part 1

Decoders are combinational circuits which have multiple outputs. They are widely used in memory chips to select one of the words addressed by the address input. For example, an 8-words memory will have three bit address input. The decoder will decode the 3-bit address and generate a select line for one of the eight words corresponding to the input address. The 3-to-8 decoder symbol and the truth table are shown below.

	X ₀ X ₁ X ₂	Y ₇ Y ₆ Y ₅ Y ₄ Y ₃ Y ₂ Y ₁ Y ₀
	0 0 0	0 0 0 0 0 0 0 1
	0 0 1	0 0 0 0 0 0 1 0
	0 1 0	0 0 0 0 0 1 0 0
	0 1 1	0 0 0 0 1 0 0 0
	1 0 0	0 0 0 1 0 0 0 0
	1 0 1	0 0 1 0 0 0 0 0
	1 1 0	0 1 0 0 0 0 0 0
	1 1 1	1 0 0 0 0 0 0 0

Such circuits, also known as binary decoders, and can be modeled using dataflow statements as only each output is true for a unique input combination.

1-1. Design a 3-to-8 line decoder. Let the input be through SW2-SW0 and output be on LED7-LED0. Use dataflow modeling constructs.

1-1-1. Open Vivado and create a blank project called lab3_1_1.

1-1-2. Create and add the Verilog module, naming it `decoder_3to8_dataflow.v`, that defines the 3-to-8 line decoder with three-bit input `x` and 8-bit output `y`. Use dataflow modeling constructs.

1-1-3. Add the provided testbench (`decoder_3to8_dataflow_tb.v`) to the project.

1-1-4. Simulate the design for 50 ns and verify that the design works.

- 1-1-5. Add the appropriate board related master XDC file to the project and edit it to include the related pins, assigning x to **SW2-SW0** and y to **LED7-LED0**. Note that one and only one LED will be turned ON for a given input combination.
- 1-1-6. Synthesize and implement the design.
- 1-1-7. Generate the bitstream, download it into the Basys3 or the Nexys4 DDR board, and verify the functionality.
- 1-1-8. **Demonstrate simulation results, working circuit and Verilog code to the TA.**

Multi-output Encoder Circuits

Part 2

Encoder circuit converts information from one format (code) to another for the purposes of standardization, speed, secrecy, security, or saving space by shrinking size. In digital circuits, encoding information may reduce size and/or prioritize functions. Widely used encoder circuits examples include priority encoders, Huffman encoders, etc.

2-1. Design an 8-to-3 priority encoder, whose truth table is given below. Use dataflow or behavioral modeling.

Inputs									Outputs				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	X	X	X	X	X	X	X	0	0	0	0	0	1
0	X	X	X	X	X	X	0	1	0	0	1	0	1
0	X	X	X	X	X	0	1	1	0	1	0	0	1
0	X	X	X	X	0	1	1	1	0	1	1	0	1
0	X	X	X	0	1	1	1	1	1	0	0	0	1
0	X	X	0	1	1	1	1	1	1	0	1	0	1
0	X	0	1	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1

X = don't care

2-1-1. Open Vivado and create a blank project called lab3_2_1.

2-1-2. Create and add the Verilog module with v and en_in_n input; y, en_out, and gs output. The v input will be 8-bit data inputs (labeled 0 to 7 in the table), en_in_n input will be one bit (E1), y output will be 3-bit (A2, A1, A0), en_out will be one bit output (GS), and **en_out** will be one bit output (E0).

2-1-3. Add the appropriate board related master XDC file to the project and edit it to include the related pins. Assign x input to **SW7-SW0**, en_in_n to **SW15**, y to **LED2-LED0**, en_out to **LED7**, and gs to **LED6**.

2-1-4. Synthesize and implement the design.

2-1-5. Generate the bitstream, download it into the Basys3 or the Nexys4 DDR board, and verify the functionality.

2-1-6. **Demonstrate the working circuit and Verilog code to the TA.**

Read-Only Memories

Part 3

Read-only memories (ROM) consist of interconnected arrays to store an array of binary information. Once the binary information is stored it can be read any time but cannot be altered. Large ROMs are typically used to store programs and/or data which will not change by the other circuitry in the system. Small ROMs can be used to implement combinatorial circuits or Look Up Tables (LUTs). A ROM can be used as a decoder similar to the one designed in lab 1-1 earlier.

A ROM will have m address input pins and n information output pins to store 2^m words information, each word being n bit in length. The content is accessed by placing an address and the content of the corresponding word is read at the output pins.

In Verilog HDL, memories can be defined as a two dimensional array using `reg` data type, as illustrated below:

```
reg [3:0] MY_ROM [15:0];
```

where `reg` is data type, MY_ROM is a 16x4 memory with 16 locations each location being 4-bit wide. If the memory is to be modeled as read only then two things must happen: (i) memory should only be read and not written into, and (ii) memory should somehow be initialized with the desired content. Verilog HDL provides a system task, called `$readmemb`, to initialize memory with a content. Following is an example of definition and usage of 4x2 ROM.

```
module ROM_4x2 (ROM_data, ROM_addr);
    output [1:0] ROM_data;
    input [1:0] ROM_addr;

    reg [1:0] ROM [3:0]; // defining 4x2 ROM

    assign ROM_data = ROM[ROM_addr]; // reading ROM content at the address
    ROM_addr

    initial $readmemb ("ROM_data.txt", ROM, 0, 3); // load ROM content from
    ROM_data.txt file
endmodule
```

The ROM_data.txt file, for this example, should be present in the same directory where the model is defined (since no directory path is given), and may have 8 or less lines such as:

```
10
0x
11
00
```

Note that if the number of lines is less than the size of the ROM, the unspecified locations will be initialized with 0s. Also, note that there is another system task available, called `$readmembh`, which allows the data file to be written using hexadecimal symbols.

3-1. Design a 2-bit comparator that compares two 2-bit numbers and asserts outputs indicating whether the decimal equivalent of word A is less than, greater than, or equal to that of word B. You will use a ROM as a Look Up Table (LUT) and use the `$readmemb` task.

3-1-1. Open Vivado and create a blank project called lab3_3_1.

3-1-2. Create and add the Verilog module with two inputs (a, b) and three outputs (lt, gt, and eq) using ROM and `$readmemb` system task.

- 3-1-3.** Add the appropriate board related master XDC file to the project and edit it to include the related pins. Assign a to **SW3 to SW2**, b to **SW1 to SW0**, lt to **LED2**, gt to **LED1** and eq to **LED0**.
- 3-1-4.** Create and add a text file that describes design output.

b	a	Lt	Gt	Eq
00	00	0	0	1
00	01	1	0	0

The table shows the first two comparisons for b is **greater than, less than, or equal to** a. Continue the logic comparison until **b is 11** and **a is 11**.

Create the logic in a document and save as **.txt** file. Then click on **Add Sources** under the Flow Navigator. Select the **Add or create design sources** and click **next**. Click the **green plus** button and **add file**. Add the **.txt** file and click **finish**.

- 3-1-5.** Synthesize and implement the design.
- 3-1-6.** Generate the bitstream, download it into the Basys3 or the Nexys4 DDR board, and verify the functionality.
- 3-1-7.** **Demonstrate the working circuit and Verilog code to the TA.**

Conclusion

In this lab, you learned how to model multiple output circuits such as decoders, encoders, and ROM. You also learned how to use a system task \$readmemb to initialize ROM memory. There are more system tasks which the language supports and you will learn some of them in future labs.