Lab 1: The Bipolar Junction Transistor (BJT): DC and AC Characterization

Schedule for this lab:
Day 1: BJT DC Characteristics
Day 2: BJT AC Characteristics

Introduction

When designing a circuit, it is important to know the properties of the devices that you will be using. This lab will look at obtaining important device parameters from a BJT. Although many of these can be obtained from the datasheet, datasheets may not always include the information we want. Even if they do, it is also useful to perform our own tests and compare the results. This process is called device characterization. In addition, the tests you will be performing will help you get some experience working with your tools so you don't waste time fumbling around with them in future labs.

In day 1, you will be looking at the **DC characteristics** of your transistor. This will give you an idea of what the I-V curves look like, and how you would measure them. You will also have to build and test a current mirror, which should give you an idea of how they work and where their limitations are.

In day 2, you will look at the **AC characteristics**. You will learn how to measure medium and higher frequency measurements, and how to calculate useful transistor characteristics from them.

Day 1: BJT DC Characterization

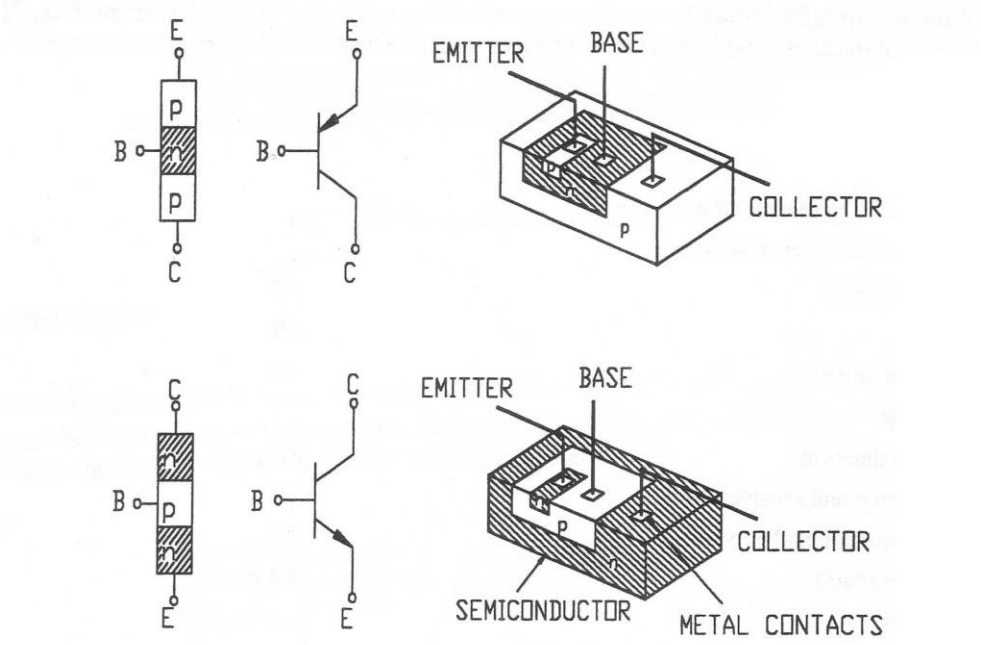
Background:

The BJT is a three-terminal semiconductor device containing two PN junctions. If checked with an ohm-meter it appears to be two diodes of opposite polarity connected in series. However, unlike two series diodes, the BJT can be used to amplify. This is because the base is small enough to allow the two sets of PN-junctions to interact with each other. There are two basic types of BJT, as illustrated in Figure 1.1.

BJT Operating Regions:

Figure 1.2 shows an example of an I-V curve of a NPN BJT transistor. As its name would imply, an I-V curve plots the device current of the device against a sweep of terminal voltage. Figure 1.2 shows an example of collector current as the collector-emitter voltage is changed, with a separate curve for different base currents. This family of curves is organized by base current since the diode-like characteristics of the current vs. base-emitter voltage would make the voltages of each curve very similar (and highly susceptible to process variations). Figure 1.3 shows the opposite type of curve, with a plot of collector current as the base-emitter voltage is swept. The collector-emitter voltage is not changed as this does not affect the family of curves significantly. This curve doesn't give as much insight as the first curve, but is shown as a comparison (more information could be obtained if I_{CE} was plotted on a log scale instead of a linear scale, but is still not as useful).

BJTs, like all transistors, are non-linear. The non-linear properties are what make it useful as an amplifier or switch, but as you will find in higher level courses, non-linear devices are a pain to analyze. Fortunately, we can treat a BJT as a linear device as long as its current/voltage characteristics remain in one of a few confined regions. Figure 1.2 shows the 3 main regions of operation of the BJT. A fourth one exists (reverse active) but is not used in practice due to its poor properties. The very same semiconductor conditions that give high gain in the normal active region are the same ones that cause low gain in the reverse active region.



(a) Basic structure. (b) Symbol (c) Practical structure.

Figure 1.1 BJT (PNP top figure and NPN bottom figure).

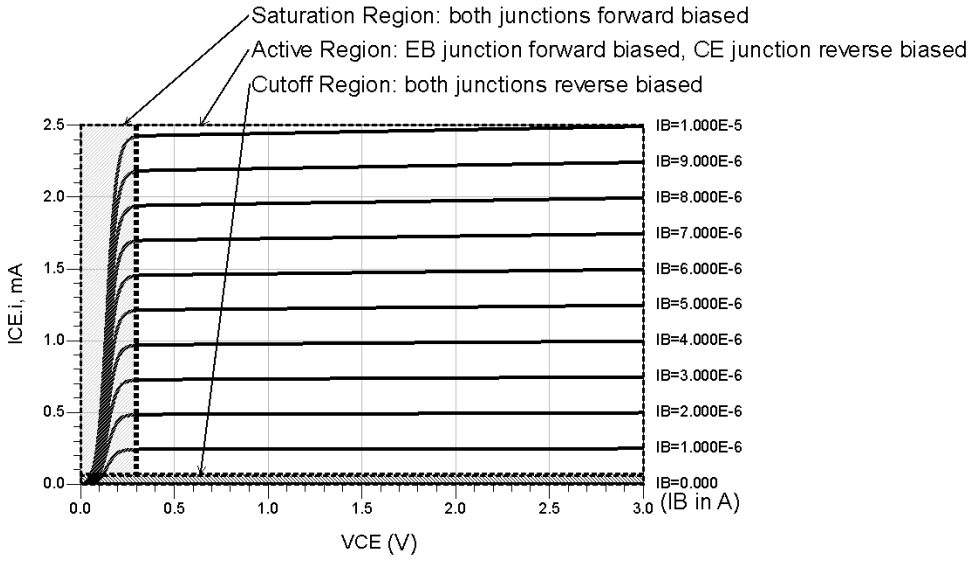


Figure 1.2: Plot of the I-V curves of an example transistors sweeping V_{CE} for different I_B showing 3 regions of operation of the BJT

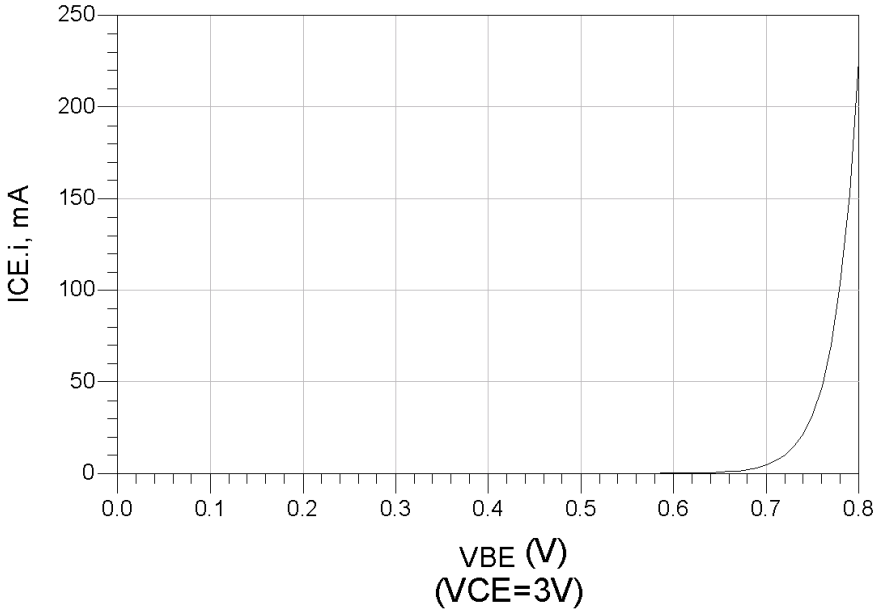
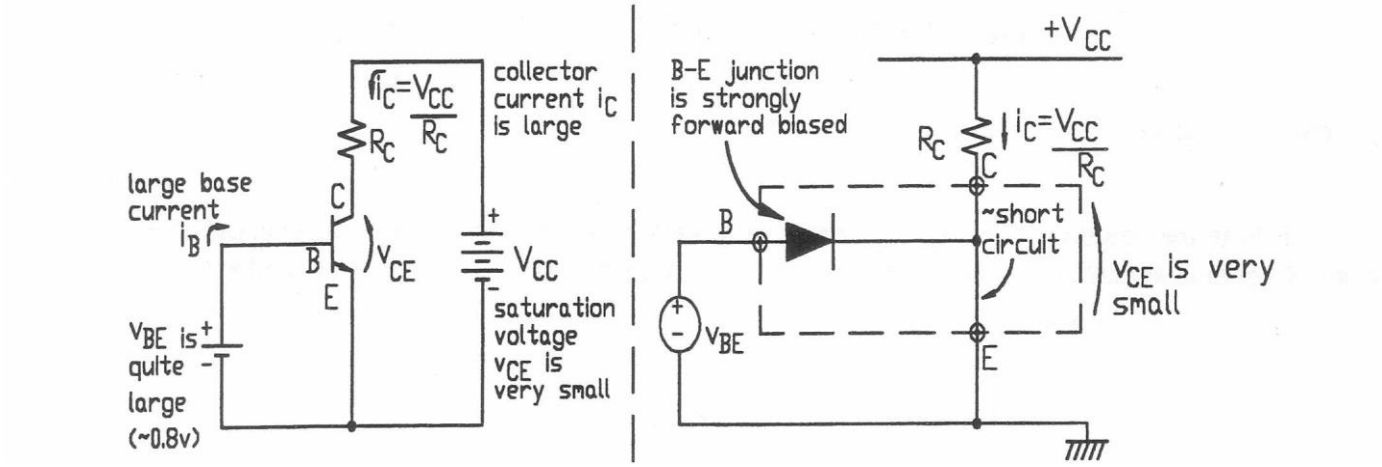


Figure 1.3 Plot of an I-V curve of an example transistor sweeping V_{BE} with a fixed V_{CE}

(i) Saturation Region

In this region, both BJT junctions are forward biased. V_{CE} is small, e.g. 50-100 mV, but quite large collector and base currents (I_c & I_B) can flow. This region is not used for amplification. There is a low resistance between the C and E terminals: the BJT acts like a closed switch. Figure 1.4 shows an actual circuit of a BJT in saturation and the small-signal equivalent (that is, the linear model) of the circuit.



An actual circuit with an NPN BJT Approximate equivalent circuit.

Figure 1.4 Saturation region

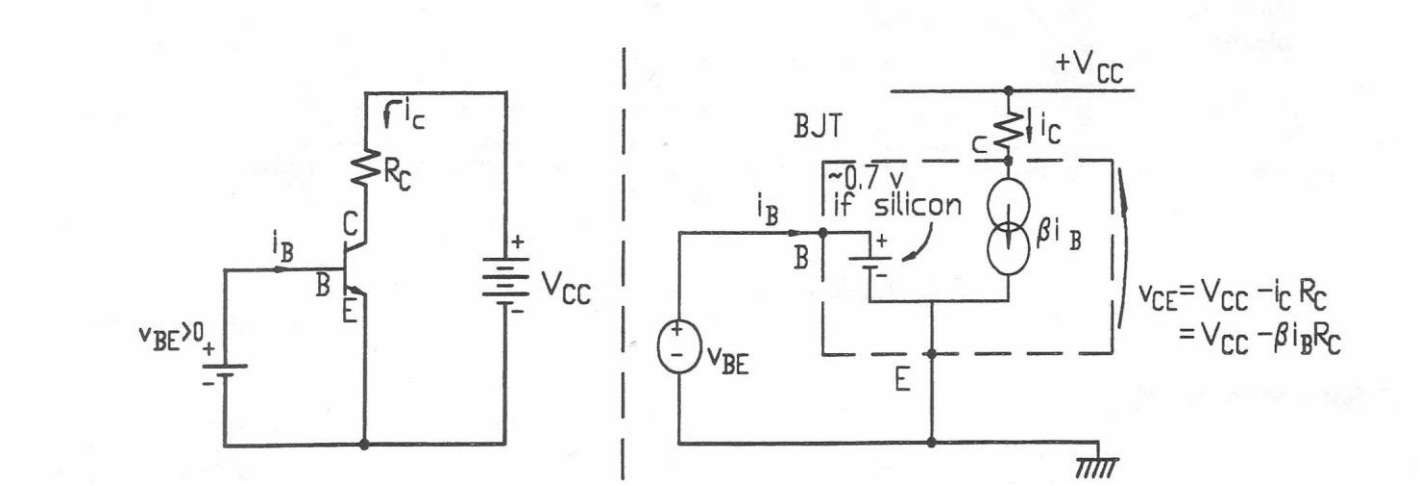
(ii) Active Region

Here the B-E junction is forward biased but the B-C junction is reverse biased. Because the two junctions are very close together, the emitter "emits" carriers which shoot across the central base region and are "collected" by the collector region. This flow of carriers manifests itself externally as a relatively large collector current I_C. This process is strongly influenced by the external injection of a much smaller current I_B into the base region.

This lets the collector current be controlled almost completely by the base-emitter junction voltage, and is nearly independent on the collector node voltage (a very useful result). As the collector/emitter current ratio is dependent on fixed semi-conductor parameters, we can define the BJT current gain:

$$\beta = \frac{I_C}{I_B}$$

Figure 1.5 shows an actual BJT operating in the active region and the small signal equivalent model. Do not confuse this with a MOSFET in saturation, which behaves similarly to the BJT in the active region.



An actual circuit with an NPN BJT Approximate equivalent circuit for silicon BJT.

Figure 1.5 Active region, B-E diode is forward biased

(iii) Cutoff Region

If both the junctions are reverse-biased, only very small reverse leakage currents can flow across them. No gain is available in this mode, and there is a high resistance between the C and E terminals.

The small-signal circuit model is not shown: it is just an open circuit between all 3 nodes.

Part 1: Diode-Like behavior of BJT Junctions, and BJT Type

Experiment: Using the Digital Volt Meter (DVM) on the *"diode"* setting, measure the forward and reverse voltages of the B-E, B-C and C-E junctions of a 2N3904 transistor, shown in Fig. 1.6. The *"diode"* range actually forces an output current of 1mA from its "V" terminal, and then measures the voltage developed between the "V" and common terminals. Thus, the DVM can directly measure the forward voltage drop of PN junction under 1mA of bias. Note the orientation of the device as seen in Figure 1.6: it is a very common mistake to switch the emitter and collector terminals. Another common mistake is to confuse a PNP transistor for an NPN transistor or vice-versa.

Figure 1.6 Lead Configuration of a 2N3904 Transistor. The lead configuration for the 2N3906 is exactly the same.

There should be diode-like behavior between the B-E and B-C terminals, but not between the C-E terminals in either direction. Any other behavior usually indicates a damaged BJT. Of course, it is possible for a BJT to be damaged but still pass this test. Remember to record which meter lead is connected to which transistor terminal. By measuring the polarity of the voltage appearing across the ohmmeter leads, *determine whether the 2N3904 is a pnp or npn type*. Do the same for the 2N3906 transistor.

Report: Show your results in a table and explain your conclusions.

Part 2: BJT I_C vs. V_{CE} Characteristic Curves - Point-by-Point Plotting

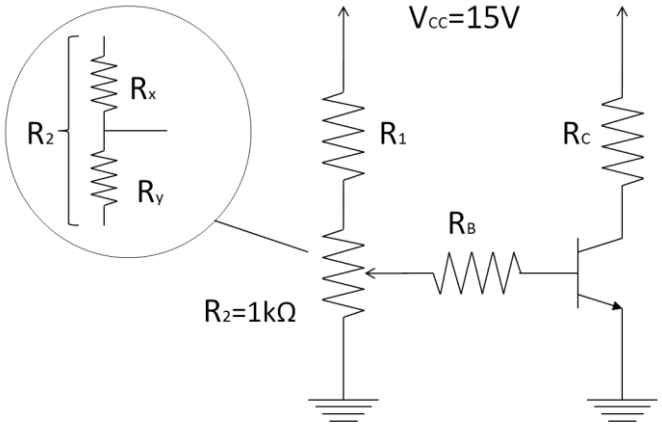


Figure 1.7 Test circuit for Part 2

For this section, you will generate a plot similar to Figure 1.2 by plotting I_C vs V_{CE}. The figure shows several curves for different I_B values. You will produce <u>one curve at a single constant I_B value</u> that gives I_C in the active region around **2 mA.**

R_2 is a potentiometer (the symbol is a resistor with an arrow pointing to it). It is a 3-terminal variable voltage divider with a total resistance of 1kΩ. This allows the base voltage to be tuned by fine increments.

Prelab: For this part, determine appropriate values of R_1, R_B and R_C. You will need to justify these choices in your report with good reasons. Obviously there will be many possible values of R_C, with each representing a different V_{CE}. Choose at least 5 values in the active region and another 5 or more values in the saturation

region. Show the expected V_{CE} for each resistance.

As a hint, for these calculations, keep in mind that V_{BE} is around 0.7 V in the active region, $V_{CE,sat}$ is 0.5V, beta is around 150 and that the voltage drop across any resistor should be at least 0.25 V to be able to measure it accurately. In addition, the current flowing in the left branch should be much greater than the base current and the potentiometer should be in its middle range (i.e. $R_x=R_y=500\Omega$).

Experiment: Assemble the circuit using your calculated resistance values. Verify that the voltages at various nodes are what you expect them to be. With the device in the active region, adjust the potentiometer so that it produces I_C of 2mA. Measure I_B and keep this value fixed while you change the values of R_C. **Measure I_C, V_{BE} and V_{CE} for each R_C.** Every time you change R_C be sure to verify that I_B has not changed. If it has, you can adjust it with the potentiometer.

Report:

- Plot the I_C-V_{CE} line for the base current that was used. Determine the I_C/I_B current ratio for the transistor at each point.
- Plot V_{BE} vs. V_{CE}. Does V_{BE} change very much as V_{CE} is changed? Why? What happens to this current ratio when the transistor goes into saturation?
- From your plot, determine the value of beta and a value for the Early voltage V_A.

Part 3: The Current Mirror

In network analysis, you have encountered two types of sources: fixed voltage and fixed current courses. With a voltage source, the voltage across the terminals is always a fixed value, while with a current source, the current flowing through the source is always a fixed value. While it is fairly easy to implement a fixed voltage source (e.g. a voltaic cell), implementing a current source is more difficult.

Your notes show examples of a circuit called a current mirror which is the easiest implementation of a current source. A current mirror typically has two or more branches. In one branch (known as the reference branch) a fixed, known current flows, which can be controlled by adjusting a potentiometer, some controllable switches or by a self-correcting circuit such as a band-gap generator. The other branch has a current flowing through them which is a direct multiple of the reference branch: ratios of 1:1 to 1:4 are common, and higher ratios are possible if less accuracy is needed.

A NPN current mirror with emitter degeneration resistors is shown in Figure 1.8. The emitter resistors, R_{E1} and R_{E2}, reduce the effect that mismatches in V_{BE} between the two discrete transistors have on the matching of the output current to the reference current. These resistors can also be conveniently used to alter the ratio between the two currents. Different permutations of this circuit exist which allow the mirror to operate at a wider output voltage range, or increase output impedance.

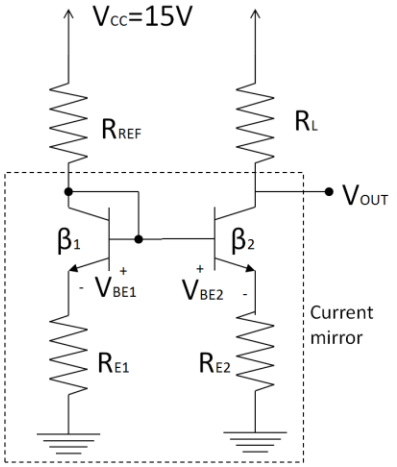


Figure 1.8 The Current Mirror and Test Circuit.

Prelab:

- Given the circuit in Fig. 1.8, derive an equation for the output current (I_{out}) in terms of I_{REF}, V_{BE1}, V_{BE2}, β_1, β_2, R_{E1}, R_{E2} and V_{CC}.
- You may assume $V_{BE1}=V_{BE2}$ and that βs are both very large.
- With R_{E1} set to 2kΩ, pick a value of R_{E2} so that the current is mirrored (1:1 ratio). Choose an appropriate value of R_{Ref} (remember that the base is shorted to the collector) so that the reference current is approximately 0.5 mA.
- Determine the maximum value of R_L for which the current mirror will still be able to deliver the necessary amount of current. Keep in mind that the behavior of the transistor changes if it enters a different region of operation. Choose 10 values for R_L, 5 that show the range of load resistances over which the current mirror operates and 5 that show where the current mirror fails. Show the expected current and output voltage for each load resistance.
- Design a **1:2 current multiplier** where the output current is two times the reference current.
- Design a PNP current mirror such that it can be connected to the NPN current mirror as can be seen below. Note that the PNP current mirror may have other connections not seen in the figure (such as a connection to power). The PNP current mirror should mirror its reference current in a 1:1 ratio.

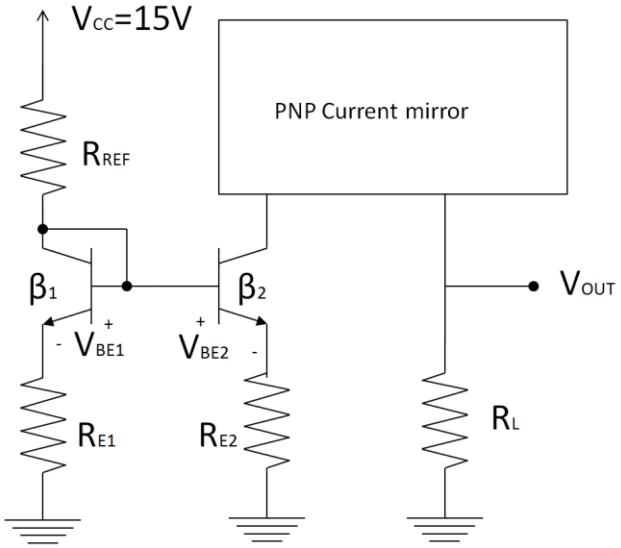


Figure 1.9 Schematic of the NPN current mirror connected to the PNP current mirror with test circuit

Experiment:

- Construct the NPN current mirror as shown in Figure 1.8 and test the circuit with the set of loads you picked out in the prelab. For each load, measure the output voltage (V_{out}), and calculate the current flowing through the load resistor.
- Modify the circuit create the 1:2 current multiplier and measure the current flowing through a few different loads (at least 4) to show that the current mirror is in fact still acting as a current source with the correct output current.
- Change your original NPN mirror back to a 1:1 ratio and connect the PNP current mirror that you designed as shown in Figure 1.9. *Note that the load resistance of the NPN current mirror is replaced by the reference branch of the PNP current mirror*. Measure the current flowing through a few loads (at least 4) to show that the current mirror is in fact still acting as a current source with the correct output current.

Report:

- Show your derivations for your equation for the current mirror's output current and the 1:2 current multiplier.
- With your measurements from your 1:1 mirror, plot output current vs. load resistance and output voltage vs output current. From the second plot, **determine the output impedance**. Keep in mind that a current mirror can be modeled as an ideal current source in parallel with a large resistance (which is its output resistance).
- Make another plot showing the output current vs. load resistance for your multiplier.
- Comment on the first transistor (the one with the base and collector shorted), what two-terminal device does it resemble the closest? With the transistor configured in this way, can it enter the saturation region of operation? If so, under what conditions? If not, why not?
- Consider the range of loads over which the 1:2 mirror can deliver its rated current. How would you expect this range to change with the multiplier and why?

Day 2: BJT AC Characteristics

Purpose:

Previously, we measured some of the DC characteristics of a BJT transistor. In this part of the lab, we will look at the AC operation of the transistor. In this course and in other courses, you may have encountered names such as R_{pi} or g_m when performing calculations. These parameters are specific to the device (and the device model) that you are using. In order to compare devices of different types, we use a different set of network parameters. In this lab, you will become familiar with the h-parameters and the hybrid-pi model of the bipolar junction transistor.

Introduction:

Part 4: The Transistor's h-Parameters and Bandwidth:

The four h-parameters describe all of a transistor's small-signal ac characteristics for a given set of dc bias conditions, at one frequency. At low to medium frequencies, they are independent of frequency. The four parameters are:

h_{ie}: the ac input impedance with the output short-circuited
h_{oe}: the output admittance with the input open-circuited
h_{fe}: the ac forward current gain with the output short-circuited, and
h_{re}: the reverse, or feedback, voltage ratio with the input open-circuited

The second subscript, **e**, indicates that these parameters are measured with respect to the emitter, the emitter being the terminal common to both the input circuit and the output circuit. All but the last h-parameter will be measured in this exercise, the last one being so close to zero as to be practically unobservable using the equipment of the ELEC 3509 laboratory.

The one other transistor parameter of major interest is its unity-gain bandwidth, f_T, the frequency at which its ac current gain is reduced to one. In most cases, equipment bandwidth limitations prevent the direct measurement of f_T for any active device, so it is usually determined by extrapolating results at lower frequencies. In this case, this can be done by observing the low-frequency current gain h_{fe}, and by measurements of the beta cut-off frequency, f_β, the frequency at which h_{fe} drops by 3dB; f_T is the product of f_β and h_{fe} (see Figure 1.10).

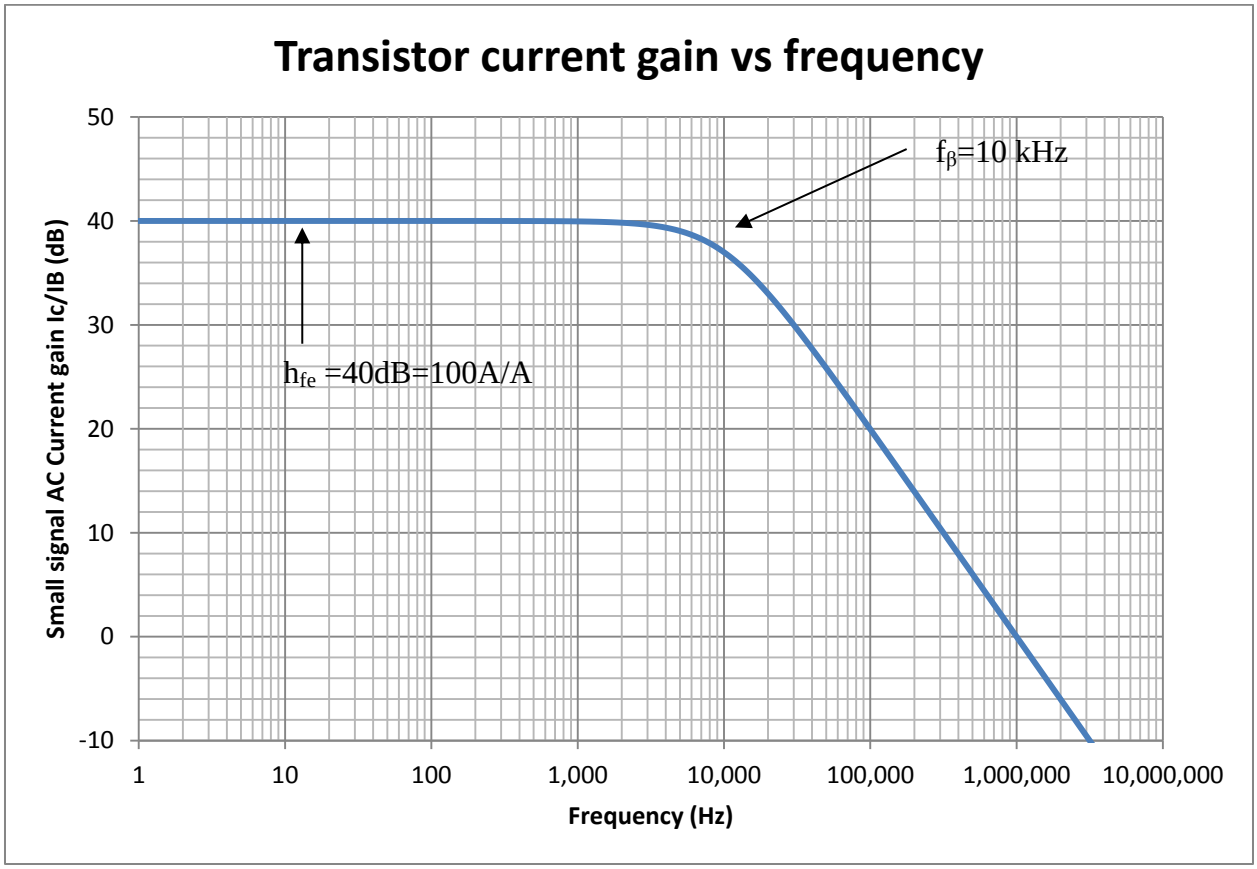


Figure 1.10 A example plot showing current gain vs frequency. Here, the f_T can be seen directly to be 1 MHz, but can be calculated by multiplying h_{fe}=100 by f_β=10kHz (note: your transistor's values will not be the same as in this sample).

Part 4 (a): Dc-Biasing Circuit

Set up the circuit shown in Figure 1.11. Be sure to use the same transistor that was partially characterized in part 2. **Use a value of R_C to maintain a V_{CE} around 6 V** and whatever values of R_1 and R_B you used in week 1. Be sure to actually measure the real value of the resistors used.

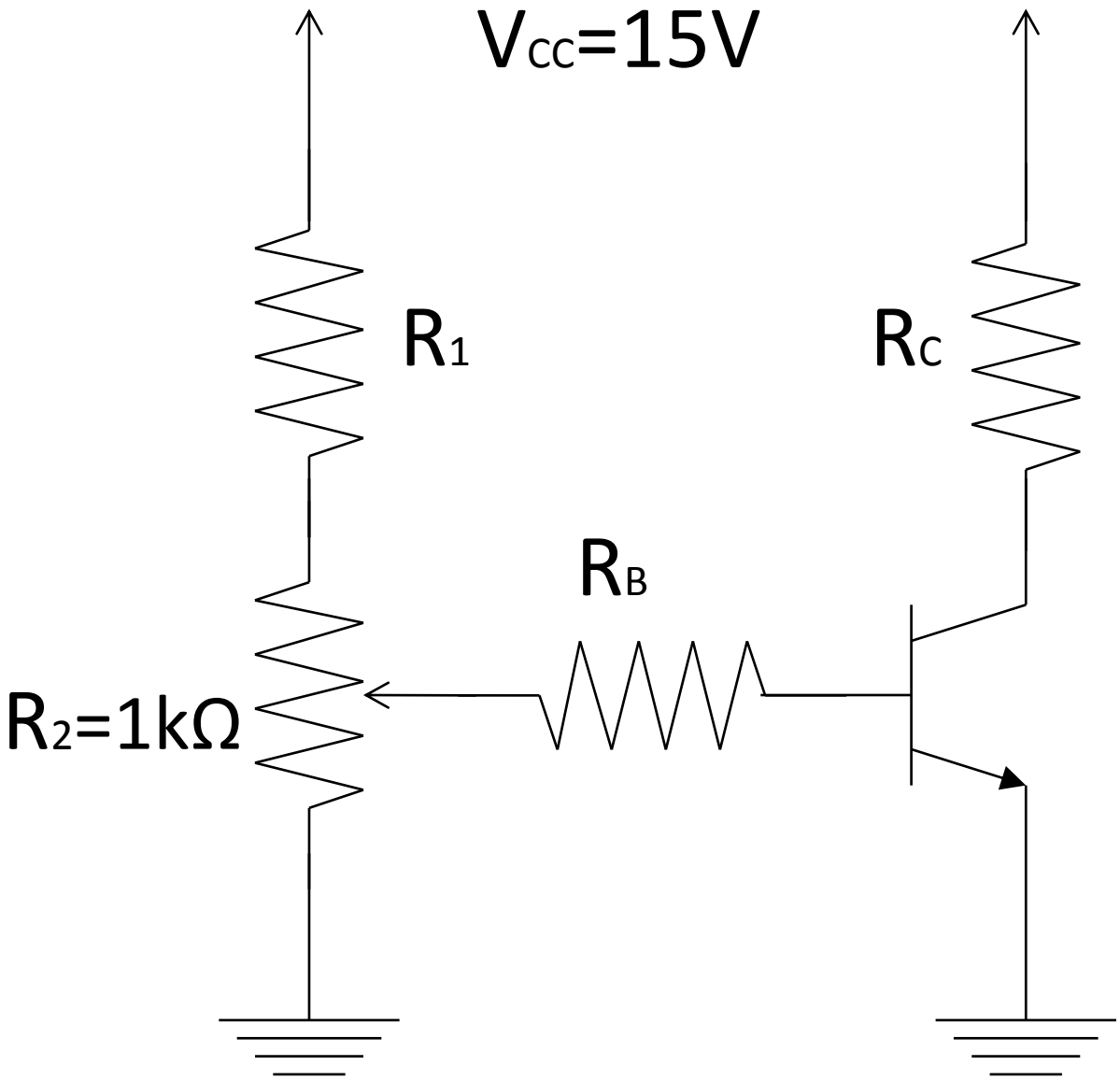


Figure 1.11 DC Bias circuit for the AC characterization tests

Adjust the potentiometer to set **I_C to 2 mA** and measure the actual V_{CE} so that during the subsequent tests the dc collector conditions in the circuit will be known.

Part 4 (b): Ac-Coupling of Input and Output Signals

Add the additional circuitry shown in Figure 1.12. This additional circuitry couples AC test signals into and out of the DC-biased transistor circuit, which is the device under test (D.U.T). Fig, 1.13 represents a "black-box" view of the D.U.T. in the test circuit.

In your report, explain the purpose of the capacitors C_1 and C_2, making sure to identify what would happen if they were absent.

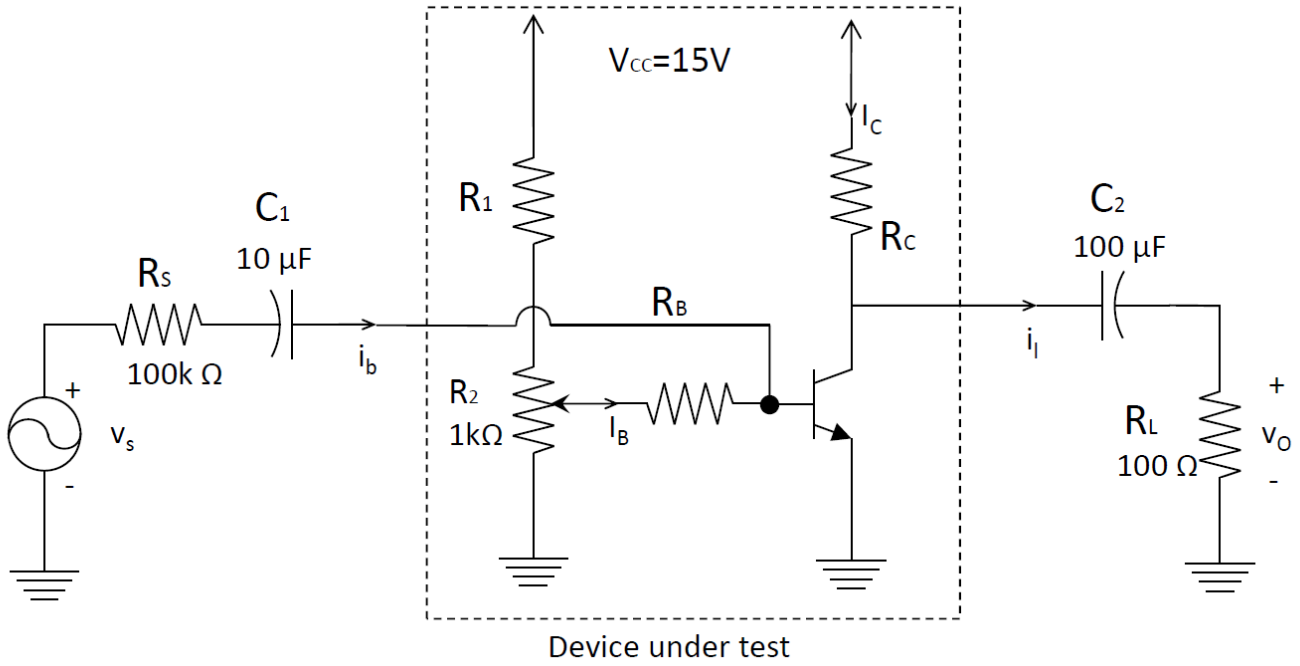


Figure 1.12 Ac Test Circuit for the Biased BJT

Be certain to observe the **POLARITY** of the electrolytic capacitors when connecting them; if reversed, they will conduct dc current, and will permanently ruin them. **RECALL: The arrow points to the negative terminal.**

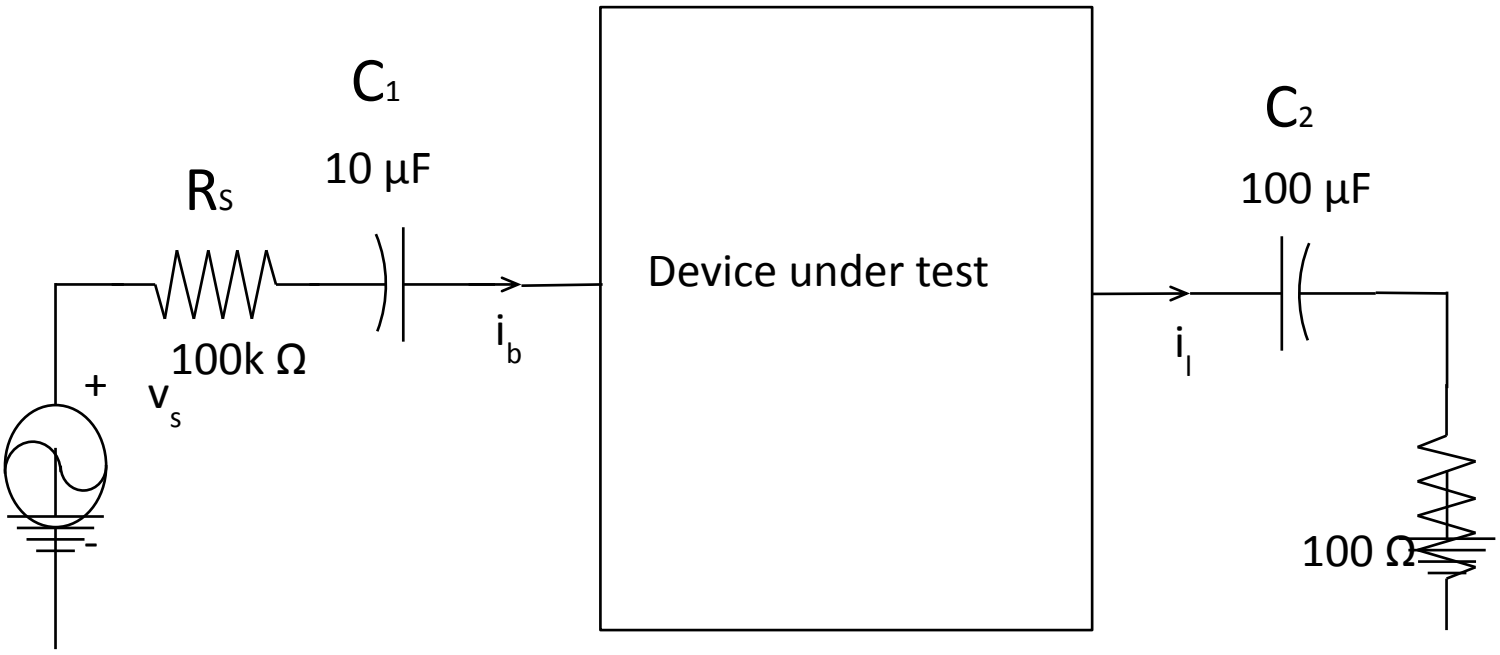


Figure 1.13 "Black-Box" View of the DUT in the AC Test Circuit.

Part 4 (c): The AC Input Impedance, h_{ie}, and the ac Forward Current Gain, h_{fe}
Experiment: Connect the signal generator to the circuit and set the signal source to provide a 1 kHz sinusoid. Use the source's **"low-amplitude"** output connector. Set the AC base current, i_b, to **1.0 µA RMS** by adjusting

the output level (amplitude) of the single generator while using the multimeter to monitor v_{ib} across R_S (make sure to measure it using the AC Voltage mode). Note that the multimeter's output is RMS, not peak-peak or peak. The input impedance of the multimeter is high enough that its effect on measurements in this circuit can be ignored at low frequencies.

Using the oscilloscope, qualitatively ensure that the circuit is not distorting the signal. Using the multimeter measure and calculate the following:

AC input impedance:

$$h_{ie} = \frac{v_{be}}{i_b} = \frac{v_{be}}{v_{ib}} R_S$$

AC forward current gain:

$$h_{fe} = \frac{i_c}{i_b}$$

where

$$i_c = \frac{v_O}{R_L}$$

The expected range of results for h_{ie} and h_{fe} can be found in the attached specifications for the 2N3904 transistor. Note that the output short-circuit condition properly required for measuring h_{ie} and h_{fe} is only approximately met by the 100Ω load resistance that was used in the test circuit. However, the error that it produces here is small. In later calculations of the hybrid-pi parameters, the fact that there exists an AC output voltage will have to be taken into account.

Report: In your report, show your results and calculations. Describe why the value of the load resistor cannot be made to be zero.

Part 4(d): The AC Output Admittance, h_{oe}, and the AC Reverse, or Feedback, Voltage Ratio, h_{re}

Since we are dealing with very low frequencies, the ac output admittance, h_{oe}, can be found from the DC characterization you performed in day 1. In this case, it is the slope of the I_C vs. V_{CE} characteristic curve at the point of dc operation. Use the I_C vs. V_{CE} graph from part 2 to find h_{oe}, ignoring the fact that I_C may not be exactly the same in the graph as it is in this part of the experiment, but it will be close. The units of h_{oe} are amps/volt, or mhos. Express the admittance in μmhos, as this is usual since its value will be quite small. The expected range of h_{oe} can be found in the attached specifications.

Note that in general, AC parameters cannot be found from looking at the DC I-V curves, although this is usually ok if we are not working at very high frequencies.

The ac feedback voltage ratio, as previously mentioned, is too small to measure in the ELEC 3509 laboratory. Therefore, take $h_{re} = 0$.

Part 4 (e): The Unity-Gain Bandwidth, f_T, and the Beta Cut-Off Frequency, f_β

Note: See appendix A at the end of this lab for more information about making AC measurements.

Experiment: Make sure AC i_b is still set to approximately 1.0 μA RMS at 1 kHz. Use the oscilloscope to measure the voltage across R_L and use the method described in the appendix to measure the voltage across R_S. From this, calculate the current gain, h_{fe}.

Continue to make these measurements as you increase the frequency. You will need enough data points to make a plot like Figure 1.10. Increasing the frequency by factors of 2-3 per measurement should be ok. You won't be able to directly measure unity-gain frequency (0 dB) however. Instead you must be able to reach and exceed the point where the current gain drops to 71% of its low frequency value (a 3 dB drop). This frequency is **f_β**. Note that you cannot assume that the signal generator voltage will remain constant over frequency. You must re-measure the voltage across R_S each time.

From these values, calculate f_T:

$$f_T = h_{fe} \text{ (low frequencies)} \times f_\beta$$

Change the DC bias conditions so that the DC I_C is 0.5 mA and find f_T again. Change RC to keep V_{CE} around 7.5V. Repeat with I_C=1 mA. Make a plot of current gain/frequency for these two new currents and find h_{fe}, f_β and as a result, f_T.

Report: For all three bias conditions, plot current gain (in dB) as a function of frequency (in a log scale). On the plot, show your values of h_{fe} and f_β.

Part 5: The BJT High-Frequency Hybrid-Pi Model

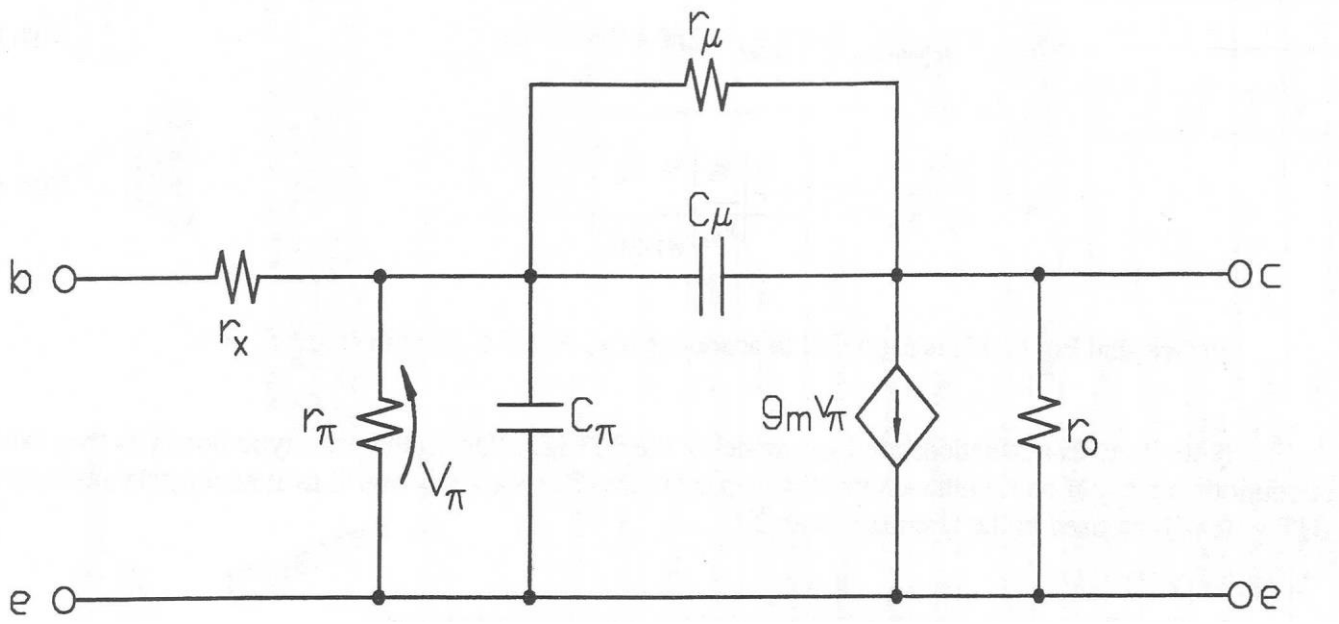


Fig. 1.14 *The High-Frequency Hybrid-Pi Model of a BJT.*

Report: Figure 1.14 shows the high-frequency hybrid-pi model of a BJT. The equations given below define its elemental values in terms of the previously measured circuit parameters. For your report, calculate all of these values, and make a copy of them as they will be needed for designing the amplifiers of the first project.

$$g_m = \frac{I_c}{V_T}, V_T = \frac{KT}{q} = \frac{1.381\times10^{-23} J^\circ/K}{1.602\times10^{-19} C} \cdot T \approx 25mV \quad \text{at } 20^\circ C \qquad \text{Eqs. (1.5)}$$

$$r_\pi = \frac{h_{fe}}{g_m} \qquad \text{Eqs. (1.6)}$$

$r_x = h_{ie} - r_\pi$ (If through experimental error r_x becomes negative, then set $r_x = 0.$) Eqs. (1.7)

$$r_\mu = \frac{r_\pi}{h_{re}} \approx \infty \qquad \text{Eqs. (1.8)}$$

$$r_o = \left(h_{oe} - \frac{h_{fe}}{r_\mu}\right)^{-1} \approx h_{oe}^{-1} \qquad \text{Eqs. (1.9)}$$

$$w_\beta = 2\pi f_\beta \qquad \text{Eqs. (1.10)}$$

$C_\mu = C_{BCjunction} + C_{board} \approx 2pf + 2pf = 4pf$ Eqs. (1.11)

$$C_\pi = \frac{1}{r_\pi \cdot \omega_\beta} - C_\mu \left[1 + \left| \frac{v_o}{v_{be}} \right|_{@1KHz} \right] \qquad \text{Eqs. (1.12)}$$

Notice that Eq. (1.12) is modified to account for $v_o \neq 0$. If C_π negative set $C_\pi = 0$.

Note that these equations are for a model of the BJT installed on the prototype board as they take into account the effect of board inter-connection capacitances. This model is useful as it accurately represents the BJT as it will be used in the circuits of Lab 2

The 2N3904 transistor specifications are provided in the following page.

2N3903 (SILICON)
2N3904

$V_{CB} = 60$ V
$I_C = 200$ mA
$C_{ob} = 4.0$ pf (max)

CASE 29
(TO-92)

NPN silicon annular transistors, designed for general purpose switching and amplifier applications, features one-piece, injection-molded plastic package for high reliability. The 2N3903 and 2N3904 are complementary with types 2N3905 and 2N3906, respectively.

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CB}	60	Vdc
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Emitter-Base Voltage	V_{EB}	6	Vdc
Collector Current	I_C	200	mAdc
Total Device Dissipation @ $T_A = 60°C$	P_D	210	mW
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	310 2.81	mW mW/°C
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW
Junction Operating Temperature	T_J	135	°C
Storage Temperature Range	T_{stg}	-55 to +135	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		BV_{CBO}	60	—	Vdc
Collector-Emitter Breakdown Voltage* (I_C = 1 mAdc)		BV_{CEO}*	40	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	6	—	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{OB} = 3 Vdc)		I_{CEX}	—	50	nAdc
Base Cutoff Current (V_{CE} = 40 Vdc, V_{OB} = 3 Vdc)		I_{BL}	—	50	nAdc

*Pulse Test: Pulse Width = 300 μsec, Duty Cycle = 2% V_{OB} = Base Emitter Reverse Bias

ELECTRICAL CHARACTERISTICS (continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain* (I_C = 0.1 mAdc, V_{CE} = 1 Vdc)	2N3903	h_{FE}*	20	—	—
	2N3904		40	—	
(I_C = 1.0 mAdc, V_{CE} = 1 Vdc)	2N3903		35	—	
	2N3904		70	—	
(I_C = 10 mAdc, V_{CE} = 1 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1 Vdc)	2N3903		30	—	
	2N3904		60	—	
(I_C = 100 mAdc, V_{CE} = 1 Vdc)	2N3903		15	—	
	2N3904		30	—	
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1 mAdc)		$V_{CE(sat)}$*	—	0.2	Vdc
(I_C = 50 mAdc, I_B = 5 mAdc)			—	0.3	
Base-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1 mAdc)		$V_{BE(sat)}$*	0.65	0.85	Vdc
(I_C = 50 mAdc, I_B = 5 mAdc)			—	0.95	
SMALL SIGNAL CHARACTERISTICS					
High Frequency Current Gain (I_C = 10 mA, V_{CE} = 20 V, f = 100 mc)	2N3903	$\lvert h_{fe} \rvert$	2.5	—	—
	2N3904		3.0	—	
Current-Gain–Bandwidth Product (I_C = 10 mA, V_{CE} = 20 V, f = 100 mc)	2N3903	f_T	250	—	MHz
	2N3904		300	—	
Output Capacitance (V_{CB} = 5 Vdc, I_E = 0, f = 100 kc)		C_{ob}	—	4	pf
Input Capacitance (V_{OB} = 0.5 Vdc, I_C = 0, f = 100 kc)		C_{ib}	—	8	pf
Small Signal Current Gain (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc)	2N3903	h_{fe}	50	200	—
	2N3904		100	400	
Voltage Feedback Ratio (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc)	2N3903	h_{re}	0.1	5.0	$X10^{-4}$
	2N3904		0.5	8.0	
Input Impedance (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc)	2N3903	h_{ie}	0.5	8	Kohms
	2N3904		1.0	10	
Output Admittance (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kc)	Both Types	h_{oe}	1.0	40	μmhos
Noise Figure (I_C = 100 μA, V_{CE} = 5 V, R_S = 1 Kohms, Noise Bandwidth = 10 cps to 15.7 kc)	2N3903	NF	—	6	db
	2N3904		—	5	
SWITCHING CHARACTERISTICS					
Delay Time	V_{CC} = 3 Vdc, V_{OB} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1 mA	t_d	—	35	nsec
Rise Time		t_r	—	35	nsec
Storage Time	V_{CC} = 3 Vdc, I_C = 10 mAdc, $I_{B1} = I_{B2}$ = 1 mAdc	t_s	—	175	nsec
			—	200	
Fall Time		t_f	—	50	nsec

*Pulse Test: Pulse Width = 300 μsec, Duty Cycle = 2% V_{OB} = Base Emitter Reverse Bias

Lab 1 Appendix A: Making AC voltage measurements

There are two ways of measuring AC voltage (which can be used to find AC currents). One method is to use the multimeter in AC voltage mode and measure across the device in mind. This reports the RMS voltage, and is accurate for low frequencies (up to ~10 kHz).

Using the oscilloscope is a time intensive but more accurate method that is needed for higher frequency measurements. If we are measuring a voltage with respect to ground, we can simply place a scope probe on the net in question and observe the waveform in the scope. However, if we are measuring the voltage across a device where neither terminal is AC grounded, then it is more difficult. Some of the more obvious methods will not work:

- Using the multi-meter may not be accurate, as the multi-meter is not designed for high frequency measurements and the highly capacitive input impedance of the meter will short out the terminals you are measuring at high frequencies.
- Connecting a scope and its corresponding ground terminal across the device also will not work since the ground terminal of the probe is connected to the ground of the other probe and every other ground. This will short out the circuit.
- You also cannot measure one terminal to ground and then measure the other terminal to ground and subtract the results (as you would for DC). This is because there may be a phase shift between the nodes, even if the device you are measuring across is a resistor.

The **correct way to make the measurements** is to create a new waveform which shows the voltage difference between both terminals. To do this, perform the following steps:

1. Connect both probes, one at each end of the terminal. Make sure coupling mode is set to AC (Vertical > Menu > Coupling). Ensure that the waveforms are triggered properly (Trigger > Menu). If they are, then the waveforms will remain stationary on the display. Make sure both waveforms are displayed with a decent magnitude: not too small and not clipping. At least 1 period of each (preferably 2) should be visible.
2. Then we must tell the oscilloscope to display another waveform which shows the difference between both probes. Do this by pushing the MATH button and set the scope to do 2 channel operations and not FFT (this is located on the bottom left of the screen). Then use the buttons to select channel 1 and channel 2 as the sources (the operands), and set the operation to subtract. A red waveform appears which is either Ch1-Ch2 or Ch2-Ch1.
3. Use the measurement operations or the cursors as you normally would.
4. You can disable the red math channel by selecting the MATH button and turning the channel off.

For measurements of small magnitude (less than 50 mV peak-peak), we can improve accuracy significantly by averaging in the time domain. This reduces thermal the noise that the scope itself adds in due to its high resistance and large bandwidth.

Normally, the scope records a single sample, and immediately displays that value. Any noise that is sampled is also displayed. When in averaging mode, the scope records the last N samples for a given part of the display, and averages those and displays that. The signal magnitudes add up together in phase, while the noise on all of the measurements tends to cancel each other out. Note that if the signal is changing (some part of your circuit is modified, or improper triggering for instance) the averaged signal will take some time to change as the previous values and new values are averaged together.

To set the scope in averaging mode:

1. First make sure that the waveform you want to average is visible on the screen, is not too small or clipping, is **triggered properly**, and has several periods visible.
2. Press the "Menu" key in the acquire section of the scope (the rightmost column).
3. Select the "average" option on the bottom. To restore the scope into normal operation, use the "sample" option on the top.
4. When "Average" is selected, you can turn the dial on the top of the scope (the one next to the "select" and "coarse" buttons) to change the number of samples. Increasing the number of samples improves accuracy but takes longer- this is the tradeoff with all measurements. Realistically, only a few averages are necessary- accuracy goes up with the square root of the number of samples.

Note that when you make a change to the circuit, you will need to reset the scope's built-in memory, so you don't average the changed values with the previous values. You can do this by turning averaging off and then back on again. If your average is small enough, you don't need to worry about this (the previous samples will be forgotten before you change the scope settings).