Carleton University

Department of Systems and Computer Engineering

SYSC 3006 (Computer Organization) summer 2020

Lab / Assignment 1 – Answering file

Question 1 [0.5-mark]

What is the minimum ROM Address Bit Width needed to implement Table 1, and why?
Answer in this space:

2^m >= number of states = 8, and m is the minimum Address with. $2^3 = 8$, so 3-bit width is the minimum to have a unique address for each state.

Question 2 [0.5-mark]

What is the minimum ROM Data Bit Width needed to implement Table 1, and why?
Answer in this space:

6-Bit, we need 3-bit provide the address of next state, and 3-bit for the outputs (one bit to actuate each of the 3 led at the output)

Question 3 [1-mark]

Fill in the following table; it is the content of your FSM ROM that you are going to implement.

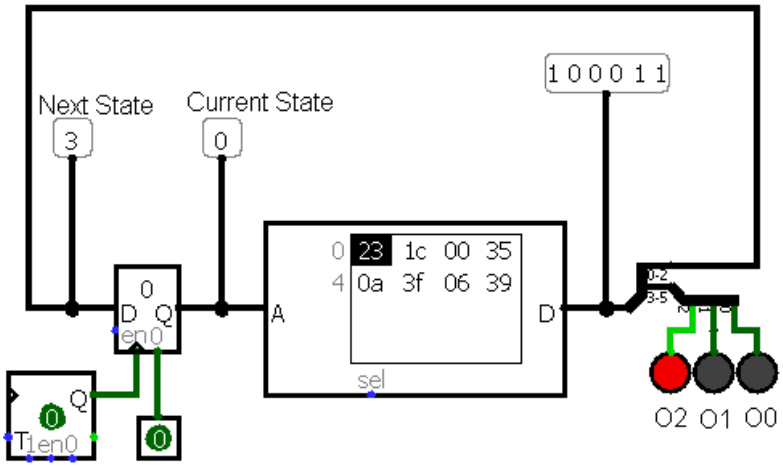
Address	DATA content (binary)	DATA content (Hex)
0b000 (0)	100011	23
0b001 (1)	011100	1C
0b010 (2)	000000	00
0b011 (3)	110101	35
0b100 (4)	001010	0A
0b101 (5)	111111	3F
0b 110 (6)	000110	06
0b111 (7)	111001	39

Table 2 - Lab1 ROM content

Question 4 [3-mark]

4.1 [0.5-mark] Show here a screenshot of your final Logisim circuit for your implementation.

Insert your image in this space:



[0.5-mark]A short description of how the component attributes have been configured to meet the lab requirements.

Answer here:

The ROM address width is chosen to 3 in order to cover a minimum of 8 states required.

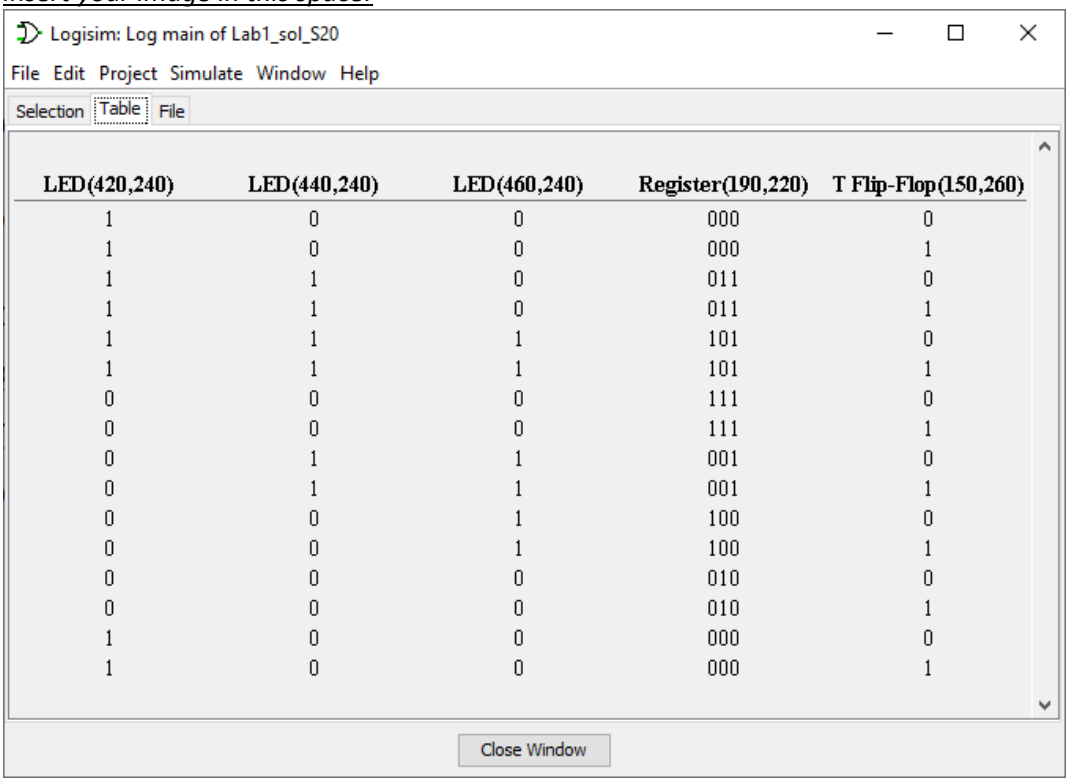
The ROM data Bit width isselected to have 6-bit, 3 to feed back next state address and 3 to each output.

The Curent state DFF databit is chosen to 3 in order to match the width of the ROM address.

The splitter Bit width in must match the data bit width of the ROM, so it is selected to 6. Then the Fan out is selected to two branches. The LSBs (0 to2) branch feed to next state DFF, then the other branch to fedd the input of another 3-Bit width in spliter with a fan out equal to 3 to feed each of the 3 output LEDs (note that there is different acceptable ways configuring the splitters).

4.2 [2-mark] Including this document, submit your Logisim lab1 file circuit (.circ) in a zip folder. Also insert below a screenshot of your Log table (0.5-mark for the Log table and 1.5-mark for a circuit working properly and respecting the design specifications described in this statement).

Insert your image in this space:



LED(420,240)	LED(440,240)	LED(460,240)	Register(190,220)	T Flip-Flop(150,260)
1	0	0	000	0
1	0	0	000	1
1	1	0	011	0
1	1	0	011	1
1	1	1	101	0
1	1	1	101	1
0	0	0	111	0
0	0	0	111	1
0	1	1	001	0
0	1	1	001	1
0	0	1	100	0
0	0	1	100	1
0	0	0	010	0
0	0	0	010	1
1	0	0	000	0
1	0	0	000	1

Now save this document as PDF and do not forget to include your .circ file with your submission!

Submission deadline

Must be submitter on cuLearn, locate (Assignment 1 submission) and follow instructions, submission exact deadline (date and time) is displayed clearly with the Assignment 1 submission on cuLearn.

Note: If you have any question please contact your respective group TA (see TA / group information posted on cuLearn).

Good Luck