Lab 2 : CMOS Combinational Logic

1. Design of the CMOS Inverter

There were two problems with making logic gates with a transistor and a resistor:
i) Getting a full 0-2.5V output swing. This was solved by choosing correctly between NMOS and PMOS.
ii) When the transistor was off there was a long slow RC time constant while the capacitor discharged through the resistor.

In CMOS logic gates two transistors are used and no resistors. One transistor pulls the output up and another to pulls it down. There is no large time constant.

NB: As an anti-counterfitting measure, every plot you print out must include your group member's names added to the curves 'digitally' by the tool.

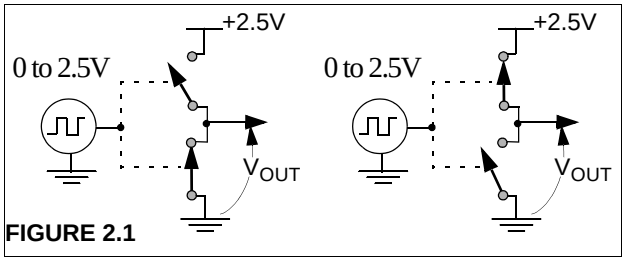


FIGURE 2.1

*Q1. Classify the inverter circuits of **Figure 2.2** as "won't work," "will work with poor output swing," and "will work well". Explain which one does not have the inverting structure.*

Q2. Using simulations, sketch the output waveform from circuits (A) and (B). Use the knowledge you gained from last week to explain.

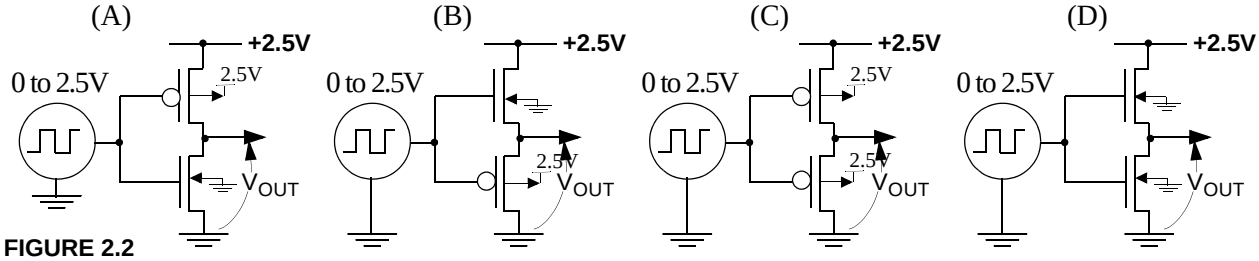


FIGURE 2.2

Q3. For the CMOS inverter in (A) measure the falling and rising times (10% - 90% swing), and measure the falling and rising delays (50% input swing to 50% output swing).

Q4. Which delay is larger? Why? (Hint: look into PMOS and NMOS transistors relative sizes.)

Q5. For what size ratio (W/L) you expect a symmetric output (i.e. almost equal rising and falling times, and almost equal rising and falling delays.) Prove your suggestion by simulation results. You may want to try a number of cases such that the rising and falling delays differ by less than 5%.

Q6. Plot VTC of the inverter by sweeping the input from 0V to 2.5V at 0.05V intervals and measuring the output. On the graph show and measure the Switching Threshold. (Use original values for W,L).

Q7. Try Q6 with the width of the PMOS at 8um instead of 1um. What difference do you realize? Explain.

Width/Length

An important factor when building MOS transistors is W/L. Just as a long thin wire has more resistance than a short thick one, a transistor with a small W/L has more resistance than one with a large W/L. A large W is used for transistors that need to deliver power like bus drivers.

Substrate Bias

In MOS transistors, the substrate is always made a reversed biased diode with the channel. In PMOS this means connecting the substrate to VDD. In NMOS it is connected to ground. .

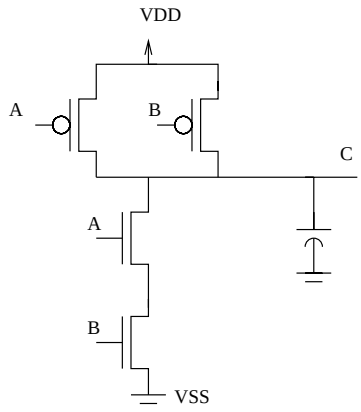
2. Design of the CMOS Combinational Logic Gates

CMOS inverters and combinational logic gates are made of PMOS and NMOS. By sizing the transistors in the combinational logic gates, you can manipulate the performances of the logic gates.

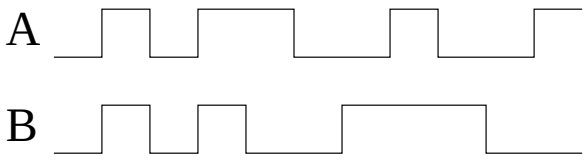
In this section, we implment NOR and NAND gates. Sizing the transistors in these combinational CMOS logic gates, we get the same delay charateristics as the CMOS inverter. Assume a capacitive load of C_L = 0.05 pF at the output of all gates for simulations.

2.1 NAND Gate

Manipulate the provided schematic to create a two-input NAND gate, as shown below:



Given the size of the transistors to be NMOS W/L =2/0.5 and PMOS W/L=2/0.5. Resize the given transistors in the schematics. Simulate the circuit using the given waveforms below.



Q8. Plot the input and output waveforms and make sure the gate functions properly for all input cases. Measure the delay in each of the four cases. Present the data in the table.

Q9. Which input combination defines the worst-case rising delay? What is this delay?

Q10. Which input combination defines the best-case rising delay? What is this delay?

Q11. What is the relation between the numerical rising delay values of the two cases in Q9 and Q10? Can you explain why?

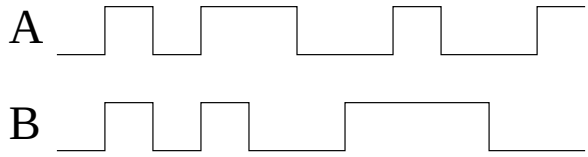
Q12. Which input combination defines the falling delay?

3. NOR Gate

Q13. Consider a NOR gate: Z = NOT (A or B). Sketch a logic network of 4 transistors (2 NMOS + 2 PMOS) to create this gate. Get a TA to verify this and mark it on the spot before continuing.

Open the provided schematic, and edit it to implement the NOR gate.

Given the size of the transistor to be NMOS W/L =1/0.5 and PMOS=4/0.5. Resize the given transistors in the schematics. Simulate the circuit using the given waveforms below.



Q14. Plot the input and output waveforms and make sure the gate functions properly for all input cases. Measure the delay in each of the four cases. Present the data in the table.

Q15. Which input combination defines the worst-case falling delay? What is this delay?

Q16. Which input combination defines the best-case falling delay? What is this delay?

Q17. What is the relation between the numerical falling delay values of the two cases in Q15 and Q16? Can you explain why?

Q18. Which input combination defines the rising delay?

4. Deliverables:

- Fill out a cover sheet.
- Demo your work to a TA.
- Answer all questions. Include all plots with names printed out on them by adding labels to the curves.