Joonwon Choi

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Research Interests

- Formal synthesis for protocols in message-passing systems.
- Formal verification (proof) for correct hardware design and synthesis. Take a look at the Kami project page for details.
- Formal verification of realistic processors.

Current Position

PhD Candidate, MIT CSAIL — Sep 2014 – Present
Advisors: Adam Chlipala and Arvind

Education

MIT CSAIL — Sep 2014 – Jun 2016
Master of Science in Electrical Engineering and Computer Science

Seoul National University — Mar 2006 – Feb 2013
Bachelor of Science in Computer Science and Engineering
Double major in Mathematical Sciences
graduated with honors (summa cum laude)

Publications

[1] Kami: A Platform for High-Level Parametric Hardware Specification and its Modular Verification.
Joonwon Choi, Muralidaran Vijayaraghavan, Benjamin Sherman, Adam Chlipala, and Arvind.
Proceedings of the 22nd ACM SIGPLAN International Conference on Functional Programming (ICFP'17).
September 2017. [pdf]

[2] An Inlining Approach to Formal Hardware Semantics.
M.S. Thesis in Electrical Engineering and Computer Science. Massachusetts Institute of Technology. [pdf]
Thesis Supervisor: Arvind

Posters

[1] Extensible Verified Validation for LLVM Optimizations.
Sungkeun Cho, Joonwon Choi, Jeehoon Kang, Chung-Kil Hur, and Kwangkeun Yi.
12th Asian Symposium on Programming Languages and Systems (APLAS'14). [pdf]

[2] Towards Scalable Verified Validation of Static Analyzers.
Jeehoon Kang, Sungkeun Cho, Joonwon Choi, and Chung-Kil Hur.
12th Asian Symposium on Programming Languages and Systems (APLAS'14). [pdf]

Current Research Projects

Kami: A Coq framework to support implementing and verifying hardware components

- Kami is a Coq framework to support implementing, specifying, verifying, and compiling Bluespec-style hardware components. The core of the approach is modular proofs of hardware components. We aim for specifications and proofs that mirror the modular decomposition of a large hardware system into simpler parts. We also intend to support techniques for machine-checked correctness proofs of key synthesis algorithms that translate high-level hardware designs into low-level circuit descriptions.

Honors & Awards

Kwanjeong Educational Fellowship — Sep 2014 – Current
MIT Emerson Scholarship for Private Music Study — Sep 2014 – Current

Top Honor (summa cum laude) Certification — Feb 2013
Seoul National University

Teaching Experience

MIT 6.887: Formal Reasoning About Programs — Spring 2017
Teaching Assistant

SNU 4190.310: Programming Languages — Fall 2013
Teaching Assistent

Working Experience

Microsoft Research Cambridge, United Kingdom — Mar 2013 – Apr 2013
Visiting Researcher

Google, Korea — Jan 2009 – Apr 2009
Software Engineering Intern(SWE Intern)

Last updated: September 19, 2017
http://joonwon.net/c/docs/cv.pdf