

Joonwon Choi

PhD Candidate in MIT CSAIL

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Research Interests

- ▶ Mechanized proof for the correctness of hardware implementation. Take a look at the [Kami](#) project page for details.
- ▶ Formal specification of [RISC-V](#) and verification of realistic processors.
- ▶ High-level language for coherent systems, for easy design and automated proof.

Current Position

PhD Candidate, MIT CSAIL

Sep 2014 – Present

Advisors: Adam Chlipala and Arvind

Education

MIT CSAIL

Sep 2014 – Jun 2016

Master of Science in Electrical Engineering and Computer Science

Seoul National University

Mar 2006 – Feb 2013

Bachelor of Science in Computer Science and Engineering

Double major in Mathematical Sciences

graduated with honors (summa cum laude)

Publications

- [1] An Inlining Approach to Formal Hardware Semantics. M.S. Thesis in Electrical Engineering and Computer Science. Massachusetts Institute of Technology. [\[pdf\]](#)

Thesis Supervisor: Arvind

Current Research Projects

Kami: A Coq framework to support implementing and verifying hardware components

- ▶ Kami is a Coq framework to support implementing, specifying, verifying, and compiling Bluespec-style hardware components. The core of the approach is modular proofs of hardware components. We aim for specifications and proofs that mirror the modular decomposition of a large hardware system into simpler parts. We also intend to support techniques for machine-checked correctness proofs of key synthesis algorithms that translate high-level hardware designs into low-level circuit descriptions.

Honors & Awards

Kwanjeong Educational Fellowship

Sep 2014 – Current

MIT Emerson Scholarship for Private Music Study

Sep 2014 – Current

Top Honor (summa cum laude) Certification
Seoul National University

Feb 2013

Working Experience

Microsoft Research Cambridge, United Kingdom
Visiting Researcher

Mar 2013 – Apr 2013

Google, Korea
Software Engineering Intern(SWE Intern)

Jan 2009 – Apr 2009

Last updated: December 10, 2016
<http://joonwon.net/c/docs/cv.pdf>