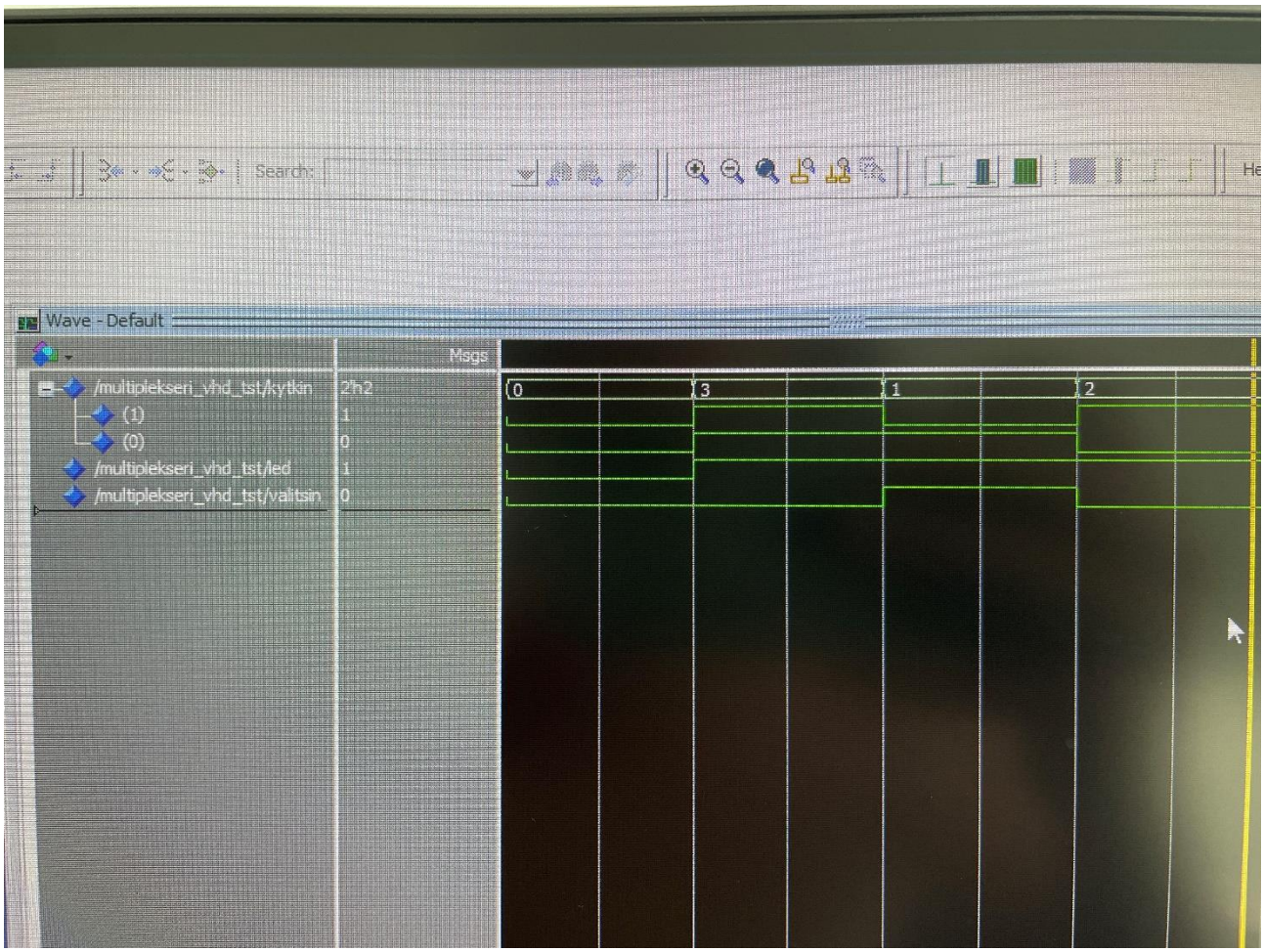
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity multiplekseri is
	port (
		valitsin : in STD_LOGIC;
		kytkin   : in STD_LOGIC_VECTOR(1 downto 0);
		led      : out STD_LOGIC
	);
end multiplekseri;

architecture behavioral of multiplekseri is
begin
	process(kytkin, valitsin)
	begin
		case kytkin is
			when "00" =>
				led <= '0';
			when "11" =>
				led <= '1';
			when "01" =>
				led <= valitsin;
			when "10" =>
				led <= not valitsin;
			when others =>
				led <= '0';
		end case;
	end process;

end behavioral;
```

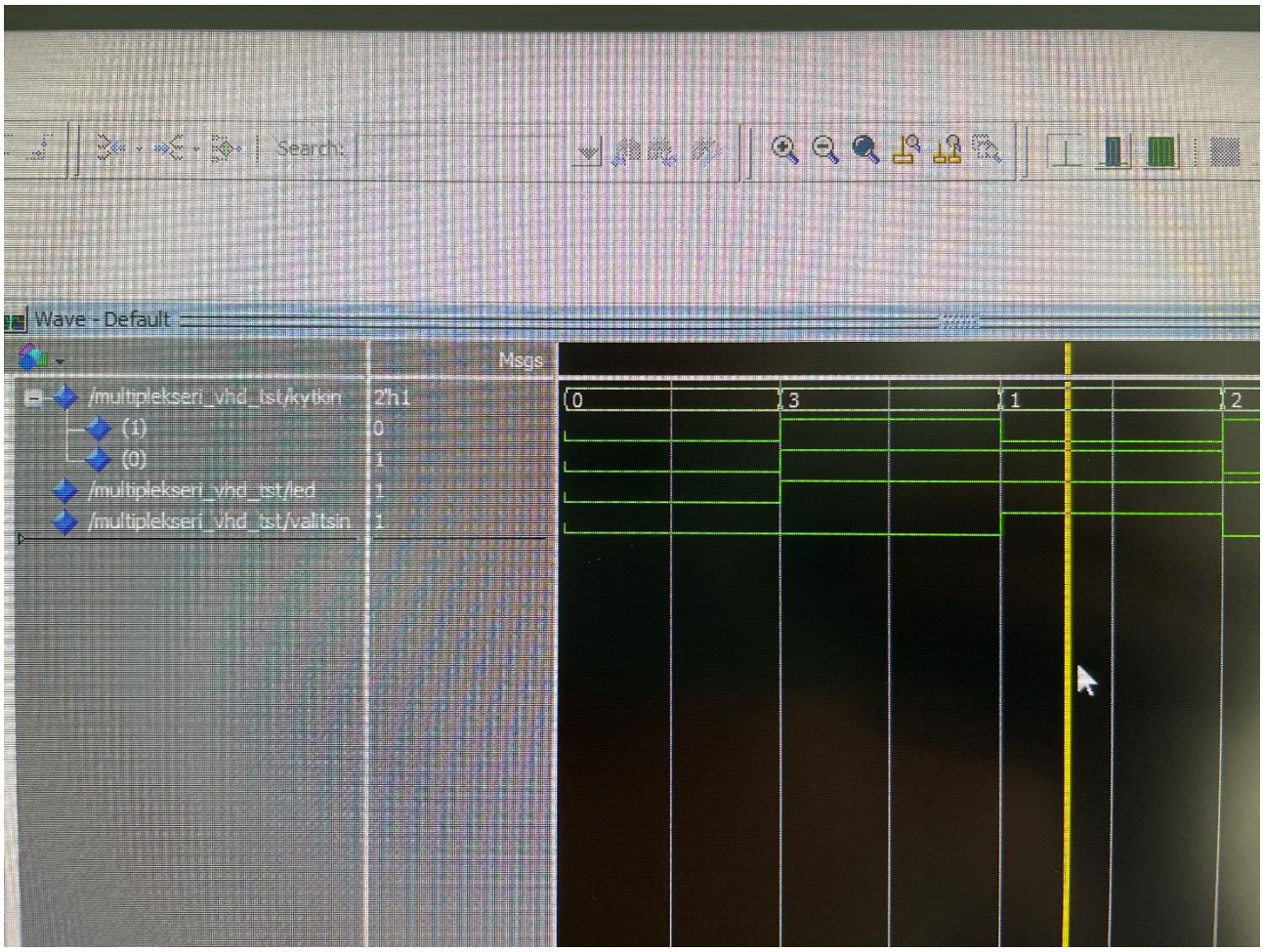
Testbench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY multiplekseri_vhd_tst IS
END multiplekseri_vhd_tst;
ARCHITECTURE multiplekseri_arch OF multiplekseri_vhd_tst IS
-- constants
-- signals
SIGNAL kytkin : STD_LOGIC_VECTOR(1 DOWNTO 0);
SIGNAL led : STD_LOGIC;
SIGNAL valitsin : STD_LOGIC;
COMPONENT multiplekseri
          PORT (
          kytkin : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
          led : OUT STD_LOGIC;
          valitsin : IN STD_LOGIC
          );
END COMPONENT;
BEGIN
          i1 : multiplekseri
          PORT MAP (
-- list connections between master ports and signals
          kytkin => kytkin,
          led => led,
          valitsin => valitsin
          );

init : PROCESS
-- variable declarations
BEGIN
          kytkin <= "00";
          valitsin <= '0';
          wait for 10 ns;

          kytkin <= "11";
          valitsin <= '0';
          wait for 10 ns;

          kytkin <= "01";
          valitsin <= '1';
          wait for 10 ns;

          kytkin <= "10";
          valitsin <= '0';
          wait for 10 ns;

WAIT;
END PROCESS init;

END multiplekseri_arch;
```

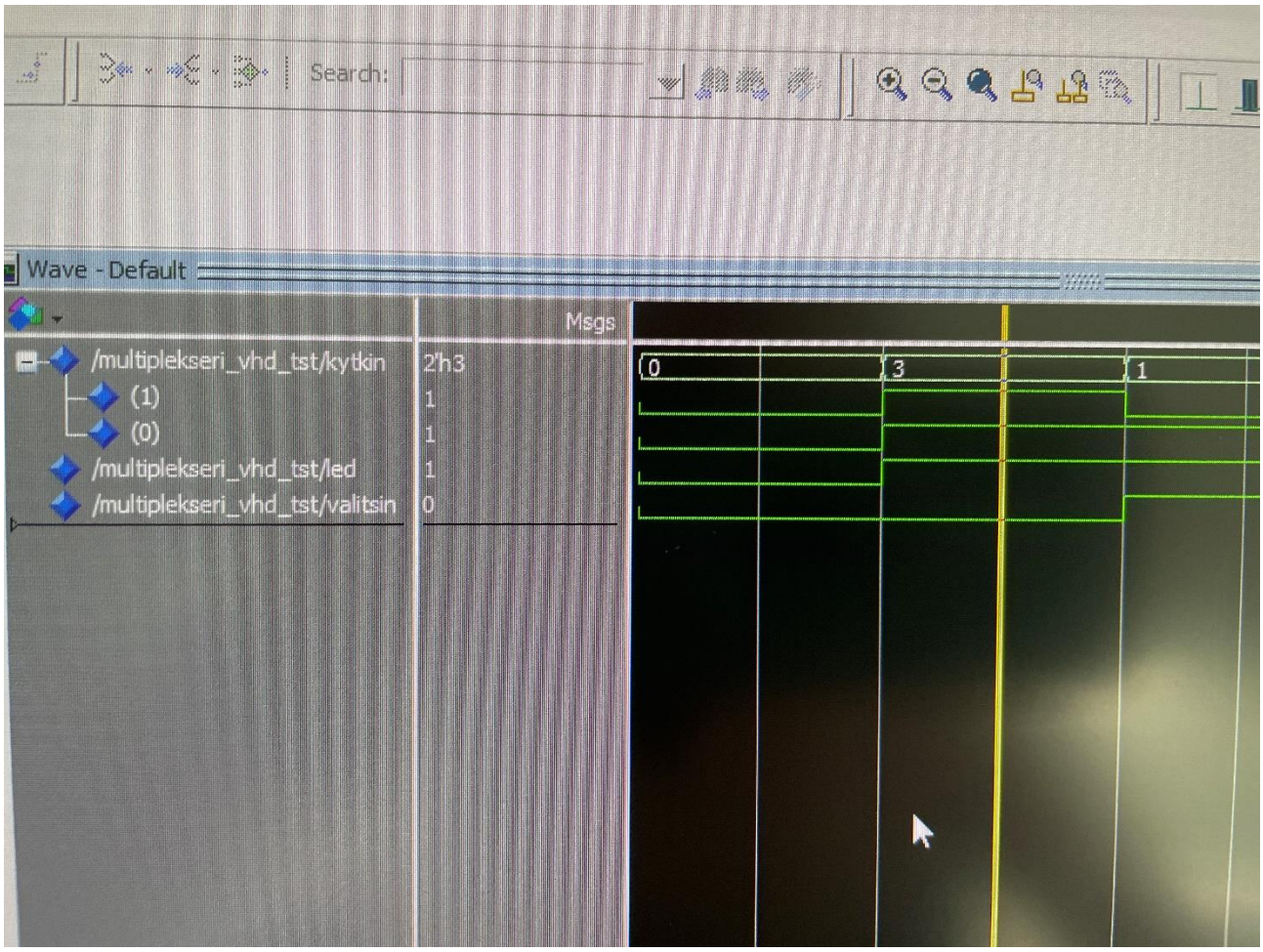
Kuvia simulaatiosta:



Kuva 1 tila(10) = näytetään käänteinen painonapin(valitsin) tila



Kuva 2 tila (01) = näytetään painonapin(valitsin) tila



Kuva 3 tila(11) = ledi palaa