-------------------------------------------------------VENDOR REPORT-------------------------------------------------------------

elease 14.7 - xst P.20131013 (lin64)

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-->

Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.08 secs

-->

Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.08 secs

-->

Reading design: ALEY\_GroupBryant\_FPADD\_VENDOR.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Compilation

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "ALEY\_GroupBryant\_FPADD\_VENDOR.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "ALEY\_GroupBryant\_FPADD\_VENDOR"

Output Format : NGC

Target Device : xc4vlx100-12-ff1148

---- Source Options

Top Module Name : ALEY\_GroupBryant\_FPADD\_VENDOR

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 32

Number of Regional Clock Buffers : 48

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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Compiling vhdl file "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd" in Library work.

Architecture rtl of Entity compareexp is up to date.

Architecture rtl of Entity computeshift is up to date.

Architecture rtl of Entity shiftman is up to date.

Architecture compare of Entity compareman is up to date.

Architecture rtl of Entity addsubman is up to date.

Architecture rtl of Entity addsubpipeman is up to date.

Architecture rtl of Entity norm1 is up to date.

Architecture rtl of Entity norm2 is up to date.

Architecture reg16bit\_arch of Entity ALEY\_groupbryant\_finalreg is up to date.

Architecture beh\_first\_bs of Entity ALEY\_groupbryant\_first\_bslice is up to date.

Architecture beh\_bs of Entity ALEY\_groupbryant\_gen\_bslice is up to date.

Architecture reg16bit\_arch of Entity ALEY\_groupbryant\_lastreg is up to date.

Architecture reg16bit\_arch of Entity ALEY\_groupbryant\_firstreg is up to date.

Architecture reg16bit\_arch of Entity ALEY\_groupbryant\_genreg is up to date.

Architecture beh of Entity ALEY\_groupbryant\_rca\_6b is up to date.

Architecture beh\_gen\_2b of Entity ALEY\_groupbryant\_rca\_gen\_2b is up to date.

Architecture beh\_first\_6b of Entity ALEY\_groupbryant\_rca\_first\_6b is up to date.

Architecture beh\_gen\_6b of Entity ALEY\_groupbryant\_rca\_gen\_6b is up to date.

Compiling vhdl file "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_VENDOR.vhd" in Library work.

Entity <ALEY\_GroupBryant\_FPADD\_VENDOR> compiled.

Entity <ALEY\_GroupBryant\_FPADD\_VENDOR> (Architecture <RTL>) compiled.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for entity <ALEY\_GroupBryant\_FPADD\_VENDOR> in library <work> (architecture <RTL>).

Analyzing hierarchy for entity <CompareExp> in library <work> (architecture <rtl>).

Analyzing hierarchy for entity <ComputeShift> in library <work> (architecture <rtl>).

Analyzing hierarchy for entity <ShiftMan> in library <work> (architecture <rtl>).

Analyzing hierarchy for entity <CompareMan> in library <work> (architecture <compare>).

Analyzing hierarchy for entity <AddSubMan> in library <work> (architecture <rtl>).

Analyzing hierarchy for entity <Norm1> in library <work> (architecture <rtl>).

Analyzing hierarchy for entity <Norm2> in library <work> (architecture <rtl>).

Analyzing hierarchy for entity <ALEY\_GroupBryant\_FinalReg> in library <work> (architecture <reg16bit\_arch>).

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\* HDL Analysis \*

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Analyzing Entity <ALEY\_GroupBryant\_FPADD\_VENDOR> in library <work> (Architecture <RTL>).

Entity <ALEY\_GroupBryant\_FPADD\_VENDOR> analyzed. Unit <ALEY\_GroupBryant\_FPADD\_VENDOR> generated.

Analyzing Entity <CompareExp> in library <work> (Architecture <rtl>).

Entity <CompareExp> analyzed. Unit <CompareExp> generated.

Analyzing Entity <ComputeShift> in library <work> (Architecture <rtl>).

Entity <ComputeShift> analyzed. Unit <ComputeShift> generated.

Analyzing Entity <ShiftMan> in library <work> (Architecture <rtl>).

Entity <ShiftMan> analyzed. Unit <ShiftMan> generated.

Analyzing Entity <CompareMan> in library <work> (Architecture <compare>).

Entity <CompareMan> analyzed. Unit <CompareMan> generated.

Analyzing Entity <AddSubMan> in library <work> (Architecture <rtl>).

Entity <AddSubMan> analyzed. Unit <AddSubMan> generated.

Analyzing Entity <Norm1> in library <work> (Architecture <rtl>).

Entity <Norm1> analyzed. Unit <Norm1> generated.

Analyzing Entity <Norm2> in library <work> (Architecture <rtl>).

Entity <Norm2> analyzed. Unit <Norm2> generated.

Analyzing Entity <ALEY\_GroupBryant\_FinalReg> in library <work> (Architecture <reg16bit\_arch>).

Entity <ALEY\_GroupBryant\_FinalReg> analyzed. Unit <ALEY\_GroupBryant\_FinalReg> generated.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

Synthesizing Unit <CompareExp>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <SSign>.

Found 23-bit register for signal <LMan>.

Found 8-bit register for signal <SExp>.

Found 1-bit register for signal <RunO>.

Found 1-bit register for signal <LSign>.

Found 23-bit register for signal <Sman>.

Found 8-bit register for signal <LExp>.

Found 9-bit comparator greater for signal <LMan$cmp\_gt0000> created at line 43.

Summary:

inferred 65 D-type flip-flop(s).

inferred 1 Comparator(s).

Unit <CompareExp> synthesized.

Synthesizing Unit <ComputeShift>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <LSignP>.

Found 8-bit register for signal <SExpP>.

Found 5-bit register for signal <shiftdistance>.

Found 23-bit register for signal <SManP>.

Found 1-bit register for signal <RunO>.

Found 1-bit register for signal <SSignP>.

Found 8-bit register for signal <LExpP>.

Found 23-bit register for signal <LManP>.

Found 8-bit subtractor for signal <sdistance$sub0000> created at line 115.

Summary:

inferred 70 D-type flip-flop(s).

inferred 1 Adder/Subtractor(s).

Unit <ComputeShift> synthesized.

Synthesizing Unit <ShiftMan>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 8-bit register for signal <t\_LExpP>.

Found 25-bit register for signal <t\_LManP>.

Found 1-bit register for signal <t\_LSignP>.

Found 1-bit register for signal <t\_RunO>.

Found 25-bit register for signal <t\_SManP>.

Found 25-bit shifter logical right for signal <t\_SManP$shift0001> created at line 191.

Found 1-bit register for signal <t\_SSignP>.

Summary:

inferred 61 D-type flip-flop(s).

inferred 1 Combinational logic shifter(s).

Unit <ShiftMan> synthesized.

Synthesizing Unit <CompareMan>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <t\_AddSub>.

Found 8-bit register for signal <t\_Exp>.

Found 25-bit register for signal <t\_LMan1>.

Found 25-bit comparator greater for signal <t\_LMan1$cmp\_gt0000> created at line 278.

Found 1-bit xor2 for signal <t\_LMan1$xor0000> created at line 272.

Found 1-bit register for signal <t\_RunO>.

Found 1-bit register for signal <t\_Sign>.

Found 25-bit register for signal <t\_SMan1>.

Summary:

inferred 61 D-type flip-flop(s).

inferred 1 Comparator(s).

Unit <CompareMan> synthesized.

Synthesizing Unit <AddSubMan>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 26-bit register for signal <UMan>.

Found 1-bit register for signal <RunO>.

Found 9-bit register for signal <UExp>.

Found 26-bit addsub for signal <UMan$mux0001>.

Summary:

inferred 36 D-type flip-flop(s).

inferred 1 Adder/Subtractor(s).

Unit <AddSubMan> synthesized.

Synthesizing Unit <Norm1>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 8-bit register for signal <ExpCor>.

Found 26-bit register for signal <OMan>.

Found 1-bit register for signal <RunO>.

Found 9-bit register for signal <OExp>.

Found 5-bit register for signal <ShfDst>.

Found 8-bit register for signal <ExpCorrect>.

Found 5-bit register for signal <ShiftDistance>.

Summary:

inferred 62 D-type flip-flop(s).

Unit <Norm1> synthesized.

Synthesizing Unit <Norm2>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 32-bit register for signal <Q>.

Found 1-bit register for signal <RunO>.

Found 8-bit adder carry in for signal <exp$mux0000> created at line 634.

Found 26-bit shifter logical left for signal <ManOut$shift0000> created at line 628.

Found 26-bit adder for signal <RoundMan$addsub0000> created at line 631.

Summary:

inferred 33 D-type flip-flop(s).

inferred 2 Adder/Subtractor(s).

inferred 1 Combinational logic shifter(s).

Unit <Norm2> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_FinalReg>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <sRun>.

Found 32-bit register for signal <sSumout>.

Summary:

inferred 33 D-type flip-flop(s).

Unit <ALEY\_GroupBryant\_FinalReg> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_FPADD\_VENDOR>.

Related source file is "/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_VENDOR.vhd".

WARNING:Xst:1780 - Signal <sshiftdistanceP> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <sSexpPP> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

Unit <ALEY\_GroupBryant\_FPADD\_VENDOR> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

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HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 4

26-bit adder : 1

26-bit addsub : 1

8-bit adder carry in : 1

8-bit subtractor : 1

# Registers : 49

1-bit register : 25

23-bit register : 4

25-bit register : 4

26-bit register : 2

32-bit register : 2

5-bit register : 3

8-bit register : 8

9-bit register : 1

# Comparators : 2

25-bit comparator greater : 1

9-bit comparator greater : 1

# Logic shifters : 2

25-bit shifter logical right : 1

26-bit shifter logical left : 1

# Xors : 1

1-bit xor2 : 1

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\* Advanced HDL Synthesis \*

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WARNING:Xst:1710 - FF/Latch <t\_LManP\_0> (without init value) has a constant value of 0 in block <InstALEY\_GroupBryant\_Shift\_MANTISSA>. This FF/Latch will be trimmed during the optimization process.

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Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 4

26-bit adder : 1

26-bit addsub : 1

5-bit subtractor : 1

8-bit adder carry in : 1

# Registers : 421

Flip-Flops : 421

# Comparators : 2

25-bit comparator greater : 1

9-bit comparator greater : 1

# Logic shifters : 2

25-bit shifter logical right : 1

26-bit shifter logical left : 1

# Xors : 1

1-bit xor2 : 1

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\* Low Level Synthesis \*

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WARNING:Xst:1710 - FF/Latch <t\_LManP\_0> (without init value) has a constant value of 0 in block <ShiftMan>. This FF/Latch will be trimmed during the optimization process.

Optimizing unit <ALEY\_GroupBryant\_FPADD\_VENDOR> ...

Optimizing unit <CompareExp> ...

Optimizing unit <ComputeShift> ...

Optimizing unit <ShiftMan> ...

Optimizing unit <CompareMan> ...

Optimizing unit <AddSubMan> ...

Optimizing unit <Norm1> ...

INFO:Xst:2261 - The FF/Latch <ExpCorrect\_5> in Unit <Norm1> is equivalent to the following 2 FFs/Latches, which will be removed : <ExpCorrect\_6> <ExpCorrect\_7>

INFO:Xst:2261 - The FF/Latch <ExpCor\_5> in Unit <Norm1> is equivalent to the following 2 FFs/Latches, which will be removed : <ExpCor\_6> <ExpCor\_7>

INFO:Xst:2261 - The FF/Latch <ExpCorrect\_5> in Unit <Norm1> is equivalent to the following 2 FFs/Latches, which will be removed : <ExpCorrect\_6> <ExpCorrect\_7>

INFO:Xst:2261 - The FF/Latch <ExpCor\_5> in Unit <Norm1> is equivalent to the following 2 FFs/Latches, which will be removed : <ExpCor\_6> <ExpCor\_7>

Optimizing unit <Norm2> ...

Optimizing unit <ALEY\_GroupBryant\_FinalReg> ...

WARNING:Xst:2677 - Node <InstALEY\_GroupBryant\_NORM1/OMan\_25> of sequential type is unconnected in block <ALEY\_GroupBryant\_FPADD\_VENDOR>.

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block ALEY\_GroupBryant\_FPADD\_VENDOR, actual ratio is 0.

Final Macro Processing ...

Processing Unit <ALEY\_GroupBryant\_FPADD\_VENDOR> :

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_7>.

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_6>.

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_5>.

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_4>.

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_3>.

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_2>.

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_1>.

Found 4-bit shift register for signal <InstALEY\_GroupBryant\_NORM1/OExp\_0>.

Found 7-bit shift register for signal <InstALEY\_GroupBryant\_NORM2/RunO>.

Unit <ALEY\_GroupBryant\_FPADD\_VENDOR> processed.

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Final Register Report

Macro Statistics

# Registers : 376

Flip-Flops : 376

# Shift Registers : 9

4-bit shift register : 8

7-bit shift register : 1

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : ALEY\_GroupBryant\_FPADD\_VENDOR.ngr

Top Level Output File Name : ALEY\_GroupBryant\_FPADD\_VENDOR

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 101

Cell Usage :

# BELS : 831

# GND : 1

# INV : 2

# LUT1 : 5

# LUT2 : 106

# LUT2\_D : 3

# LUT2\_L : 1

# LUT3 : 186

# LUT3\_D : 28

# LUT3\_L : 8

# LUT4 : 251

# LUT4\_D : 23

# LUT4\_L : 12

# MUXCY : 109

# MUXF5 : 33

# VCC : 1

# XORCY : 62

# FlipFlops/Latches : 400

# FD : 9

# FDE : 32

# FDR : 249

# FDRE : 106

# FDRS : 2

# FDRSE : 2

# Shift Registers : 9

# SRL16 : 9

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 100

# IBUF : 67

# OBUF : 33

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Device utilization summary:

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Selected Device : 4vlx100ff1148-12

Number of Slices: 374 out of 49152 0%

Number of Slice Flip Flops: 400 out of 98304 0%

Number of 4 input LUTs: 634 out of 98304 0%

Number used as logic: 625

Number used as Shift registers: 9

Number of IOs: 101

Number of bonded IOBs: 101 out of 768 13%

Number of GCLKs: 1 out of 32 3%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 409 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -12

Minimum period: 5.449ns (Maximum Frequency: 183.513MHz)

Minimum input arrival time before clock: 3.848ns

Maximum output required time after clock: 4.799ns

Maximum combinational path delay: No path found

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 5.449ns (frequency: 183.513MHz)

Total number of paths / destination ports: 25895 / 406

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Delay: 5.449ns (Levels of Logic = 27)

Source: InstALEY\_GroupBryant\_NORM1/ShfDst\_0 (FF)

Destination: InstALEY\_GroupBryant\_NORM2/Q\_30 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: InstALEY\_GroupBryant\_NORM1/ShfDst\_0 to InstALEY\_GroupBryant\_NORM2/Q\_30

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDRS:C->Q 30 0.272 0.802 InstALEY\_GroupBryant\_NORM1/ShfDst\_0 (InstALEY\_GroupBryant\_NORM1/ShfDst\_0)

LUT3\_D:I2->O 1 0.147 0.388 InstALEY\_GroupBryant\_NORM2/Sh10\_SW0 (N99)

LUT3:I2->O 4 0.147 0.446 InstALEY\_GroupBryant\_NORM2/Sh12 (InstALEY\_GroupBryant\_NORM2/Sh12)

LUT4:I2->O 1 0.147 0.000 InstALEY\_GroupBryant\_NORM2/Sh64\_f5\_F (N139)

MUXF5:I0->O 2 0.291 0.401 InstALEY\_GroupBryant\_NORM2/Sh64\_f5 (InstALEY\_GroupBryant\_NORM2/Sh64)

LUT1:I0->O 1 0.147 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12>\_rt (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12>\_rt)

MUXCY:S->O 1 0.278 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<13> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<13>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<14> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<14>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<15> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<15>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<16> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<16>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<17> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<17>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<18> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<18>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<19> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<19>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<20> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<20>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<21> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<21>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<22> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<22>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<23> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<23>)

MUXCY:CI->O 1 0.280 0.388 InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<24> (InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<24>)

LUT3:I2->O 1 0.147 0.266 InstALEY\_GroupBryant\_NORM2/RoundMan\_mux0000<25>1 (InstALEY\_GroupBryant\_NORM2/RoundMan\_mux0000<25>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<0> (InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<0>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<1> (InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<1>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<2> (InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<2>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<3> (InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<3>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<4> (InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<4>)

MUXCY:CI->O 1 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<5> (InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<5>)

MUXCY:CI->O 0 0.034 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<6> (InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<6>)

XORCY:CI->O 1 0.273 0.000 InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_xor<7> (InstALEY\_GroupBryant\_NORM2/exp\_mux0000<7>)

FDE:D 0.017 InstALEY\_GroupBryant\_NORM2/Q\_30

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Total 5.449ns (2.758ns logic, 2.691ns route)

(50.6% logic, 49.4% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 2187 / 522

-------------------------------------------------------------------------

Offset: 3.848ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: InstALEY\_GroupBryant\_NORM1/ExpCorrect\_5 (FF)

Destination Clock: clk rising

Data Path: reset to InstALEY\_GroupBryant\_NORM1/ExpCorrect\_5

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 349 0.754 1.772 reset\_IBUF (reset\_IBUF)

LUT2:I0->O 11 0.147 0.370 InstALEY\_GroupBryant\_NORM1/ShfDst\_or00001 (InstALEY\_GroupBryant\_NORM1/ShfDst\_or0000)

FDR:R 0.805 InstALEY\_GroupBryant\_NORM1/ShfDst\_1

----------------------------------------

Total 3.848ns (1.706ns logic, 2.142ns route)

(44.3% logic, 55.7% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 65 / 33

-------------------------------------------------------------------------

Offset: 4.799ns (Levels of Logic = 2)

Source: InstALEY\_GroupBryant\_FinalReg/sRun (FF)

Destination: SUM\_Q<31> (PAD)

Source Clock: clk rising

Data Path: InstALEY\_GroupBryant\_FinalReg/sRun to SUM\_Q<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDRE:C->Q 33 0.272 0.859 InstALEY\_GroupBryant\_FinalReg/sRun (InstALEY\_GroupBryant\_FinalReg/sRun)

LUT2:I0->O 1 0.147 0.266 SUM\_Q<9>1 (SUM\_Q\_9\_OBUF)

OBUF:I->O 3.255 SUM\_Q\_9\_OBUF (SUM\_Q<9>)

----------------------------------------

Total 4.799ns (3.674ns logic, 1.125ns route)

(76.6% logic, 23.4% route)

=========================================================================

Total REAL time to Xst completion: 21.00 secs

Total CPU time to Xst completion: 20.29 secs

-->

Total memory usage is 549824 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 5 ( 0 filtered)

Number of infos : 5 ( 0 filtered)

--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------ADDCORE REPORT----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

elease 14.7 - xst P.20131013 (lin64)

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-->

Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

-->

Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

-->

Reading design: ALEY\_GroupBryant\_FPADD\_ADDCORE.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Compilation

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "ALEY\_GroupBryant\_FPADD\_ADDCORE.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "ALEY\_GroupBryant\_FPADD\_ADDCORE"

Output Format : NGC

Target Device : xc4vlx100-12-ff1148

---- Source Options

Top Module Name : ALEY\_GroupBryant\_FPADD\_ADDCORE

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 32

Number of Regional Clock Buffers : 48

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd" in

Library work.

Entity <CompareExp> compiled.

Entity <CompareExp> (Architecture <RTL>) compiled.

Entity <ComputeShift> compiled.

Entity <ComputeShift> (Architecture <RTL>) compiled.

Entity <ShiftMan> compiled.

Entity <ShiftMan> (Architecture <RTL>) compiled.

Entity <CompareMan> compiled.

Entity <CompareMan> (Architecture <COMPARE>) compiled.

Entity <AddSubMan> compiled.

Entity <AddSubMan> (Architecture <RTL>) compiled.

Entity <AddSubPipeMan> compiled.

Entity <AddSubPipeMan> (Architecture <RTL>) compiled.

Entity <Norm1> compiled.

Entity <Norm1> (Architecture <RTL>) compiled.

Entity <Norm2> compiled.

Entity <Norm2> (Architecture <RTL>) compiled.

Entity <ALEY\_GroupBryant\_FinalReg> compiled.

Entity <ALEY\_GroupBryant\_FinalReg> (Architecture <reg16bit\_arch>) compiled.

Entity <ALEY\_GroupBryant\_First\_BSlice> compiled.

Entity <ALEY\_GroupBryant\_First\_BSlice> (Architecture <BEH\_first\_BS>) compiled.

Entity <ALEY\_GroupBryant\_GEN\_BSlice> compiled.

Entity <ALEY\_GroupBryant\_GEN\_BSlice> (Architecture <BEH\_BS>) compiled.

Entity <ALEY\_GroupBryant\_LastReg> compiled.

Entity <ALEY\_GroupBryant\_LastReg> (Architecture <reg16bit\_arch>) compiled.

Entity <ALEY\_GroupBryant\_FirstReg> compiled.

Entity <ALEY\_GroupBryant\_FirstReg> (Architecture <reg16bit\_arch>) compiled.

Entity <ALEY\_GroupBryant\_GenReg> compiled.

Entity <ALEY\_GroupBryant\_GenReg> (Architecture <reg16bit\_arch>) compiled.

Entity <ALEY\_GroupBryant\_RCA\_6B> compiled.

Entity <ALEY\_GroupBryant\_RCA\_6B> (Architecture <BEH>) compiled.

Entity <ALEY\_GroupBryant\_RCA\_GEN\_2B> compiled.

Entity <ALEY\_GroupBryant\_RCA\_GEN\_2B> (Architecture <beh\_gen\_2B>) compiled.

Entity <ALEY\_GroupBryant\_RCA\_First\_6B> compiled.

Entity <ALEY\_GroupBryant\_RCA\_First\_6B> (Architecture <beh\_first\_6B>) compiled.

Entity <ALEY\_GroupBryant\_RCA\_GEN\_6B> compiled.

Entity <ALEY\_GroupBryant\_RCA\_GEN\_6B> (Architecture <beh\_gen\_6B>) compiled.

Compiling vhdl file

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_ADDCORE.vhd" in

Library work.

Entity <ALEY\_GroupBryant\_FPADD\_ADDCORE> compiled.

Entity <ALEY\_GroupBryant\_FPADD\_ADDCORE> (Architecture <RTL>) compiled.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <ALEY\_GroupBryant\_FPADD\_ADDCORE> in library

<work> (architecture <RTL>).

Analyzing hierarchy for entity <CompareExp> in library <work> (architecture

<RTL>).

Analyzing hierarchy for entity <ComputeShift> in library <work> (architecture

<RTL>).

Analyzing hierarchy for entity <ShiftMan> in library <work> (architecture

<RTL>).

Analyzing hierarchy for entity <CompareMan> in library <work> (architecture

<COMPARE>).

Analyzing hierarchy for entity <AddSubPipeMan> in library <work> (architecture

<RTL>).

Analyzing hierarchy for entity <ALEY\_GroupBryant\_RCA\_6B> in library <work>

(architecture <BEH>) with generics.

W = 26

bbits = 6

Analyzing hierarchy for entity <Norm1> in library <work> (architecture <RTL>).

Analyzing hierarchy for entity <Norm2> in library <work> (architecture <RTL>).

Analyzing hierarchy for entity <ALEY\_GroupBryant\_FinalReg> in library <work>

(architecture <reg16bit\_arch>).

Analyzing hierarchy for entity <ALEY\_GroupBryant\_RCA\_First\_6B> in library

<work> (architecture <beh\_first\_6B>) with generics.

BITS6 = 6

Analyzing hierarchy for entity <ALEY\_GroupBryant\_FirstReg> in library <work>

(architecture <reg16bit\_arch>) with generics.

bbits = 6

w = 20

Analyzing hierarchy for entity <ALEY\_GroupBryant\_RCA\_GEN\_6B> in library <work>

(architecture <beh\_gen\_6B>) with generics.

BITS6 = 6

Analyzing hierarchy for entity <ALEY\_GroupBryant\_GenReg> in library <work>

(architecture <reg16bit\_arch>) with generics.

bbits = 6

prevbbits = 6

sumsize = 12

w = 14

Analyzing hierarchy for entity <ALEY\_GroupBryant\_GenReg> in library <work>

(architecture <reg16bit\_arch>) with generics.

bbits = 6

prevbbits = 12

sumsize = 18

w = 8

Analyzing hierarchy for entity <ALEY\_GroupBryant\_GenReg> in library <work>

(architecture <reg16bit\_arch>) with generics.

bbits = 6

prevbbits = 18

sumsize = 24

w = 2

Analyzing hierarchy for entity <ALEY\_GroupBryant\_RCA\_GEN\_2B> in library <work>

(architecture <beh\_gen\_2B>) with generics.

BITS2 = 2

Analyzing hierarchy for entity <ALEY\_GroupBryant\_LastReg> in library <work>

(architecture <reg16bit\_arch>) with generics.

bbits = 2

prevbbits = 24

sumsize = 26

Analyzing hierarchy for entity <ALEY\_GroupBryant\_First\_BSlice> in library

<work> (architecture <BEH\_first\_BS>).

Analyzing hierarchy for entity <ALEY\_GroupBryant\_GEN\_BSlice> in library <work>

(architecture <BEH\_BS>).

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing Entity <ALEY\_GroupBryant\_FPADD\_ADDCORE> in library <work>

(Architecture <RTL>).

Entity <ALEY\_GroupBryant\_FPADD\_ADDCORE> analyzed. Unit

<ALEY\_GroupBryant\_FPADD\_ADDCORE> generated.

Analyzing Entity <CompareExp> in library <work> (Architecture <RTL>).

Entity <CompareExp> analyzed. Unit <CompareExp> generated.

Analyzing Entity <ComputeShift> in library <work> (Architecture <RTL>).

Entity <ComputeShift> analyzed. Unit <ComputeShift> generated.

Analyzing Entity <ShiftMan> in library <work> (Architecture <RTL>).

Entity <ShiftMan> analyzed. Unit <ShiftMan> generated.

Analyzing Entity <CompareMan> in library <work> (Architecture <COMPARE>).

Entity <CompareMan> analyzed. Unit <CompareMan> generated.

Analyzing Entity <AddSubPipeMan> in library <work> (Architecture <RTL>).

Entity <AddSubPipeMan> analyzed. Unit <AddSubPipeMan> generated.

Analyzing generic Entity <ALEY\_GroupBryant\_RCA\_6B> in library <work>

(Architecture <BEH>).

W = 26

bbits = 6

Entity <ALEY\_GroupBryant\_RCA\_6B> analyzed. Unit <ALEY\_GroupBryant\_RCA\_6B>

generated.

Analyzing generic Entity <ALEY\_GroupBryant\_RCA\_First\_6B> in library <work>

(Architecture <beh\_first\_6B>).

BITS6 = 6

Entity <ALEY\_GroupBryant\_RCA\_First\_6B> analyzed. Unit

<ALEY\_GroupBryant\_RCA\_First\_6B> generated.

Analyzing Entity <ALEY\_GroupBryant\_First\_BSlice> in library <work>

(Architecture <BEH\_first\_BS>).

Entity <ALEY\_GroupBryant\_First\_BSlice> analyzed. Unit

<ALEY\_GroupBryant\_First\_BSlice> generated.

Analyzing Entity <ALEY\_GroupBryant\_GEN\_BSlice> in library <work> (Architecture

<BEH\_BS>).

Entity <ALEY\_GroupBryant\_GEN\_BSlice> analyzed. Unit

<ALEY\_GroupBryant\_GEN\_BSlice> generated.

Analyzing generic Entity <ALEY\_GroupBryant\_FirstReg> in library <work>

(Architecture <reg16bit\_arch>).

bbits = 6

w = 20

Entity <ALEY\_GroupBryant\_FirstReg> analyzed. Unit <ALEY\_GroupBryant\_FirstReg>

generated.

Analyzing generic Entity <ALEY\_GroupBryant\_RCA\_GEN\_6B> in library <work>

(Architecture <beh\_gen\_6B>).

BITS6 = 6

Entity <ALEY\_GroupBryant\_RCA\_GEN\_6B> analyzed. Unit

<ALEY\_GroupBryant\_RCA\_GEN\_6B> generated.

Analyzing generic Entity <ALEY\_GroupBryant\_GenReg.1> in library <work>

(Architecture <reg16bit\_arch>).

bbits = 6

prevbbits = 6

sumsize = 12

w = 14

Entity <ALEY\_GroupBryant\_GenReg.1> analyzed. Unit <ALEY\_GroupBryant\_GenReg.1>

generated.

Analyzing generic Entity <ALEY\_GroupBryant\_GenReg.2> in library <work>

(Architecture <reg16bit\_arch>).

bbits = 6

prevbbits = 12

sumsize = 18

w = 8

Entity <ALEY\_GroupBryant\_GenReg.2> analyzed. Unit <ALEY\_GroupBryant\_GenReg.2>

generated.

Analyzing generic Entity <ALEY\_GroupBryant\_GenReg.3> in library <work>

(Architecture <reg16bit\_arch>).

bbits = 6

prevbbits = 18

sumsize = 24

w = 2

Entity <ALEY\_GroupBryant\_GenReg.3> analyzed. Unit <ALEY\_GroupBryant\_GenReg.3>

generated.

Analyzing generic Entity <ALEY\_GroupBryant\_RCA\_GEN\_2B> in library <work>

(Architecture <beh\_gen\_2B>).

BITS2 = 2

Entity <ALEY\_GroupBryant\_RCA\_GEN\_2B> analyzed. Unit

<ALEY\_GroupBryant\_RCA\_GEN\_2B> generated.

Analyzing generic Entity <ALEY\_GroupBryant\_LastReg> in library <work>

(Architecture <reg16bit\_arch>).

bbits = 2

prevbbits = 24

sumsize = 26

Entity <ALEY\_GroupBryant\_LastReg> analyzed. Unit <ALEY\_GroupBryant\_LastReg>

generated.

Analyzing Entity <Norm1> in library <work> (Architecture <RTL>).

Entity <Norm1> analyzed. Unit <Norm1> generated.

Analyzing Entity <Norm2> in library <work> (Architecture <RTL>).

Entity <Norm2> analyzed. Unit <Norm2> generated.

Analyzing Entity <ALEY\_GroupBryant\_FinalReg> in library <work> (Architecture

<reg16bit\_arch>).

Entity <ALEY\_GroupBryant\_FinalReg> analyzed. Unit <ALEY\_GroupBryant\_FinalReg>

generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <CompareExp>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <SSign>.

Found 23-bit register for signal <LMan>.

Found 8-bit register for signal <SExp>.

Found 1-bit register for signal <RunO>.

Found 1-bit register for signal <LSign>.

Found 23-bit register for signal <Sman>.

Found 8-bit register for signal <LExp>.

Found 9-bit comparator greater for signal <LMan$cmp\_gt0000> created at

line 43.

Summary:

inferred 65 D-type flip-flop(s).

inferred 1 Comparator(s).

Unit <CompareExp> synthesized.

Synthesizing Unit <ComputeShift>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <LSignP>.

Found 8-bit register for signal <SExpP>.

Found 5-bit register for signal <shiftdistance>.

Found 23-bit register for signal <SManP>.

Found 1-bit register for signal <RunO>.

Found 1-bit register for signal <SSignP>.

Found 8-bit register for signal <LExpP>.

Found 23-bit register for signal <LManP>.

Found 8-bit subtractor for signal <sdistance$sub0000> created at line 115.

Summary:

inferred 70 D-type flip-flop(s).

inferred 1 Adder/Subtractor(s).

Unit <ComputeShift> synthesized.

Synthesizing Unit <ShiftMan>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 8-bit register for signal <t\_LExpP>.

Found 25-bit register for signal <t\_LManP>.

Found 1-bit register for signal <t\_LSignP>.

Found 1-bit register for signal <t\_RunO>.

Found 25-bit register for signal <t\_SManP>.

Found 25-bit shifter logical right for signal <t\_SManP$shift0001> created

at line 191.

Found 1-bit register for signal <t\_SSignP>.

Summary:

inferred 61 D-type flip-flop(s).

inferred 1 Combinational logic shifter(s).

Unit <ShiftMan> synthesized.

Synthesizing Unit <CompareMan>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <t\_AddSub>.

Found 8-bit register for signal <t\_Exp>.

Found 25-bit register for signal <t\_LMan1>.

Found 25-bit comparator greater for signal <t\_LMan1$cmp\_gt0000> created at

line 278.

Found 1-bit xor2 for signal <t\_LMan1$xor0000> created at line 272.

Found 1-bit register for signal <t\_RunO>.

Found 1-bit register for signal <t\_Sign>.

Found 25-bit register for signal <t\_SMan1>.

Summary:

inferred 61 D-type flip-flop(s).

inferred 1 Comparator(s).

Unit <CompareMan> synthesized.

Synthesizing Unit <AddSubPipeMan>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 26-bit register for signal <manOutA>.

Found 1-bit register for signal <RunO>.

Found 26-bit register for signal <manOutB>.

Found 9-bit register for signal <UExp>.

Found 26-bit adder for signal <manOutB$addsub0000> created at line 420.

Summary:

inferred 62 D-type flip-flop(s).

inferred 1 Adder/Subtractor(s).

Unit <AddSubPipeMan> synthesized.

Synthesizing Unit <Norm1>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 8-bit register for signal <ExpCor>.

Found 26-bit register for signal <OMan>.

Found 1-bit register for signal <RunO>.

Found 9-bit register for signal <OExp>.

Found 5-bit register for signal <ShfDst>.

Found 8-bit register for signal <ExpCorrect>.

Found 5-bit register for signal <ShiftDistance>.

Summary:

inferred 62 D-type flip-flop(s).

Unit <Norm1> synthesized.

Synthesizing Unit <Norm2>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 32-bit register for signal <Q>.

Found 1-bit register for signal <RunO>.

Found 8-bit adder carry in for signal <exp$mux0000> created at line 634.

Found 26-bit shifter logical left for signal <ManOut$shift0000> created at

line 628.

Found 26-bit adder for signal <RoundMan$addsub0000> created at line 631.

Summary:

inferred 33 D-type flip-flop(s).

inferred 2 Adder/Subtractor(s).

inferred 1 Combinational logic shifter(s).

Unit <Norm2> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_FinalReg>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <sRun>.

Found 32-bit register for signal <sSumout>.

Summary:

inferred 33 D-type flip-flop(s).

Unit <ALEY\_GroupBryant\_FinalReg> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_FirstReg>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 20-bit register for signal <sAout>.

Found 20-bit register for signal <sBout>.

Found 1-bit register for signal <scarryout>.

Found 1-bit register for signal <sRun>.

Found 6-bit register for signal <sSumout>.

Found 9-bit register for signal <sUExp>.

Summary:

inferred 57 D-type flip-flop(s).

Unit <ALEY\_GroupBryant\_FirstReg> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_GenReg\_1>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 14-bit register for signal <sAout>.

Found 14-bit register for signal <sBout>.

Found 1-bit register for signal <scarryout>.

Found 1-bit register for signal <sRun>.

Found 12-bit register for signal <sSumout>.

Found 9-bit register for signal <sUExp>.

Summary:

inferred 51 D-type flip-flop(s).

Unit <ALEY\_GroupBryant\_GenReg\_1> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_GenReg\_2>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 8-bit register for signal <sAout>.

Found 8-bit register for signal <sBout>.

Found 1-bit register for signal <scarryout>.

Found 1-bit register for signal <sRun>.

Found 18-bit register for signal <sSumout>.

Found 9-bit register for signal <sUExp>.

Summary:

inferred 45 D-type flip-flop(s).

Unit <ALEY\_GroupBryant\_GenReg\_2> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_GenReg\_3>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 2-bit register for signal <sAout>.

Found 2-bit register for signal <sBout>.

Found 1-bit register for signal <scarryout>.

Found 1-bit register for signal <sRun>.

Found 24-bit register for signal <sSumout>.

Found 9-bit register for signal <sUExp>.

Summary:

inferred 39 D-type flip-flop(s).

Unit <ALEY\_GroupBryant\_GenReg\_3> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_LastReg>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit register for signal <scarryout>.

Found 1-bit register for signal <sRun>.

Found 26-bit register for signal <sSumout>.

Found 9-bit register for signal <sUExp>.

Summary:

inferred 37 D-type flip-flop(s).

Unit <ALEY\_GroupBryant\_LastReg> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_First\_BSlice>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit xor2 for signal <SUM\_Q>.

Unit <ALEY\_GroupBryant\_First\_BSlice> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_GEN\_BSlice>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Found 1-bit xor2 for signal <SUM\_Q>.

Found 1-bit xor2 for signal <Carry\_Q$xor0000> created at line 744.

Unit <ALEY\_GroupBryant\_GEN\_BSlice> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_RCA\_First\_6B>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Unit <ALEY\_GroupBryant\_RCA\_First\_6B> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_RCA\_GEN\_6B>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Unit <ALEY\_GroupBryant\_RCA\_GEN\_6B> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_RCA\_GEN\_2B>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

Unit <ALEY\_GroupBryant\_RCA\_GEN\_2B> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_RCA\_6B>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_COMPONENTS.vhd".

WARNING:Xst:1780 - Signal <sUExp10> is never used or assigned. This

unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <Run5> is never used or assigned. This unconnected

signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <Rs5> is never used or assigned. This unconnected

signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <Rc5> is never used or assigned. This unconnected

signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <RBout5> is never used or assigned. This unconnected

signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <RAout5> is never used or assigned. This unconnected

signal will be trimmed during the optimization process.

Unit <ALEY\_GroupBryant\_RCA\_6B> synthesized.

Synthesizing Unit <ALEY\_GroupBryant\_FPADD\_ADDCORE>.

Related source file is

"/home/ise/ALEY\_GroupBryant\_FPADD/ALEY\_GroupBryant\_FPADD\_ADDCORE.vhd".

WARNING:Xst:1780 - Signal <sUMan> is never used or assigned. This unconnected

signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <sNewManFront> is never used or assigned. This

unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <carryoutP> is never used or assigned. This

unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <carryout> is assigned but never used. This

unconnected signal will be trimmed during the optimization process.

Unit <ALEY\_GroupBryant\_FPADD\_ADDCORE> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some

arithmetic operations in this design can share the same physical resources for

reduced device utilization. For improved clock frequency you may try to

disable resource sharing.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 4

26-bit adder : 2

8-bit adder carry in : 1

8-bit subtractor : 1

# Registers : 78

1-bit register : 35

12-bit register : 1

14-bit register : 2

18-bit register : 1

2-bit register : 2

20-bit register : 2

23-bit register : 4

24-bit register : 1

25-bit register : 4

26-bit register : 4

32-bit register : 2

5-bit register : 3

6-bit register : 1

8-bit register : 10

9-bit register : 6

# Comparators : 2

25-bit comparator greater : 1

9-bit comparator greater : 1

# Logic shifters : 2

25-bit shifter logical right : 1

26-bit shifter logical left : 1

# Xors : 52

1-bit xor2 : 52

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

WARNING:Xst:1710 - FF/Latch <t\_LManP\_0> (without init value) has a constant

value of 0 in block <InstALEY\_GroupBryant\_Shift\_MANTISSA>. This FF/Latch will

be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <manOutA\_25> (without init value) has a constant

value of 0 in block <InstALEY\_GroupBryant\_SIMPLEADDSUB>. This FF/Latch will be

trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_19> (without init value) has a constant

value of 0 in block <InstALEY\_GroupBryant\_RCA\_GEN\_REG1>. This FF/Latch will be

trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_13> (without init value) has a constant

value of 0 in block <InstALEY\_GroupBryant\_RCA\_GEN\_REG2>. This FF/Latch will be

trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_7> (without init value) has a constant

value of 0 in block <InstALEY\_GroupBryant\_RCA\_GEN\_REG3>. This FF/Latch will be

trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <sAout\_1> (without init value) has a constant

value of 0 in block <InstALEY\_GroupBryant\_RCA\_GEN\_REG4>. This FF/Latch will be

trimmed during the optimization process.

WARNING:Xst:2404 - FFs/Latches <manOutA<25:25>> (without init value) have a

constant value of 0 in block <AddSubPipeMan>.

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 4

26-bit adder : 2

5-bit subtractor : 1

8-bit adder carry in : 1

# Registers : 675

Flip-Flops : 675

# Comparators : 2

25-bit comparator greater : 1

9-bit comparator greater : 1

# Logic shifters : 2

25-bit shifter logical right : 1

26-bit shifter logical left : 1

# Xors : 52

1-bit xor2 : 52

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

WARNING:Xst:1710 - FF/Latch <t\_LManP\_0> (without init value) has a constant

value of 0 in block <ShiftMan>. This FF/Latch will be trimmed during the

optimization process.

Optimizing unit <ALEY\_GroupBryant\_FPADD\_ADDCORE> ...

Optimizing unit <CompareExp> ...

Optimizing unit <ComputeShift> ...

Optimizing unit <ShiftMan> ...

Optimizing unit <CompareMan> ...

Optimizing unit <AddSubPipeMan> ...

Optimizing unit <Norm1> ...

INFO:Xst:2261 - The FF/Latch <ExpCorrect\_5> in Unit <Norm1> is equivalent to

the following 2 FFs/Latches, which will be removed : <ExpCorrect\_6>

<ExpCorrect\_7>

INFO:Xst:2261 - The FF/Latch <ExpCor\_5> in Unit <Norm1> is equivalent to the

following 2 FFs/Latches, which will be removed : <ExpCor\_6> <ExpCor\_7>

INFO:Xst:2261 - The FF/Latch <ExpCorrect\_5> in Unit <Norm1> is equivalent to

the following 2 FFs/Latches, which will be removed : <ExpCorrect\_6>

<ExpCorrect\_7>

INFO:Xst:2261 - The FF/Latch <ExpCor\_5> in Unit <Norm1> is equivalent to the

following 2 FFs/Latches, which will be removed : <ExpCor\_6> <ExpCor\_7>

Optimizing unit <Norm2> ...

Optimizing unit <ALEY\_GroupBryant\_FinalReg> ...

Optimizing unit <ALEY\_GroupBryant\_FirstReg> ...

Optimizing unit <ALEY\_GroupBryant\_GenReg\_1> ...

Optimizing unit <ALEY\_GroupBryant\_GenReg\_2> ...

Optimizing unit <ALEY\_GroupBryant\_GenReg\_3> ...

Optimizing unit <ALEY\_GroupBryant\_LastReg> ...

Optimizing unit <ALEY\_GroupBryant\_RCA\_6B> ...

WARNING:Xst:1710 - FF/Latch

<InstALEY\_GroupBryant\_RCA\_6B\_ADDER/InstALEY\_GroupBryant\_RCA\_GEN\_REG1/sAout\_19>

(without init value) has a constant value of 0 in block

<ALEY\_GroupBryant\_FPADD\_ADDCORE>. This FF/Latch will be trimmed during the

optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<InstALEY\_GroupBryant\_RCA\_6B\_ADDER/InstALEY\_GroupBryant\_RCA\_GEN\_REG2/sAout\_13>

(without init value) has a constant value of 0 in block

<ALEY\_GroupBryant\_FPADD\_ADDCORE>. This FF/Latch will be trimmed during the

optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<InstALEY\_GroupBryant\_RCA\_6B\_ADDER/InstALEY\_GroupBryant\_RCA\_GEN\_REG3/sAout\_7>

(without init value) has a constant value of 0 in block

<ALEY\_GroupBryant\_FPADD\_ADDCORE>. This FF/Latch will be trimmed during the

optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<InstALEY\_GroupBryant\_RCA\_6B\_ADDER/InstALEY\_GroupBryant\_RCA\_GEN\_REG4/sAout\_1>

(without init value) has a constant value of 0 in block

<ALEY\_GroupBryant\_FPADD\_ADDCORE>. This FF/Latch will be trimmed during the

optimization process.

WARNING:Xst:2677 - Node <InstALEY\_GroupBryant\_NORM1/OMan\_25> of sequential

type is unconnected in block <ALEY\_GroupBryant\_FPADD\_ADDCORE>.

WARNING:Xst:2677 - Node

<InstALEY\_GroupBryant\_RCA\_6B\_ADDER/InstALEY\_GroupBryant\_RCA\_Last\_REG1/scarryout>

of sequential type is unconnected in block <ALEY\_GroupBryant\_FPADD\_ADDCORE>.

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block

ALEY\_GroupBryant\_FPADD\_ADDCORE, actual ratio is 1.

Final Macro Processing ...

Processing Unit <ALEY\_GroupBryant\_FPADD\_ADDCORE> :

Found 5-bit shift register for signal

<InstALEY\_GroupBryant\_SIMPLEADDSUB/RunO>.

Unit <ALEY\_GroupBryant\_FPADD\_ADDCORE> processed.

=========================================================================

Final Register Report

Macro Statistics

# Registers : 659

Flip-Flops : 659

# Shift Registers : 1

5-bit shift register : 1

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : ALEY\_GroupBryant\_FPADD\_ADDCORE.ngr

Top Level Output File Name : ALEY\_GroupBryant\_FPADD\_ADDCORE

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 101

Cell Usage :

# BELS : 899

# BUF : 1

# GND : 1

# INV : 26

# LUT1 : 5

# LUT2 : 100

# LUT2\_D : 3

# LUT2\_L : 1

# LUT3 : 219

# LUT3\_D : 40

# LUT3\_L : 8

# LUT4 : 255

# LUT4\_D : 24

# LUT4\_L : 12

# MUXCY : 109

# MUXF5 : 32

# VCC : 1

# XORCY : 62

# FlipFlops/Latches : 665

# FD : 1

# FDE : 32

# FDR : 298

# FDRE : 330

# FDRS : 2

# FDRSE : 2

# Shift Registers : 1

# SRL16 : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 100

# IBUF : 67

# OBUF : 33

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 4vlx100ff1148-12

Number of Slices: 550 out of 49152 1%

Number of Slice Flip Flops: 665 out of 98304 0%

Number of 4 input LUTs: 694 out of 98304 0%

Number used as logic: 693

Number used as Shift registers: 1

Number of IOs: 101

Number of bonded IOBs: 101 out of 768 13%

Number of GCLKs: 1 out of 32 3%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

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=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 666 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -12

Minimum period: 5.449ns (Maximum Frequency: 183.513MHz)

Minimum input arrival time before clock: 4.815ns

Maximum output required time after clock: 4.799ns

Maximum combinational path delay: No path found

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 5.449ns (frequency: 183.513MHz)

Total number of paths / destination ports: 25593 / 882

-------------------------------------------------------------------------

Delay: 5.449ns (Levels of Logic = 27)

Source: InstALEY\_GroupBryant\_NORM1/ShfDst\_0 (FF)

Destination: InstALEY\_GroupBryant\_NORM2/Q\_30 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: InstALEY\_GroupBryant\_NORM1/ShfDst\_0 to

InstALEY\_GroupBryant\_NORM2/Q\_30

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDRS:C->Q 30 0.272 0.802

InstALEY\_GroupBryant\_NORM1/ShfDst\_0 (InstALEY\_GroupBryant\_NORM1/ShfDst\_0)

LUT3\_D:I2->O 1 0.147 0.388

InstALEY\_GroupBryant\_NORM2/Sh10\_SW0 (N92)

LUT3:I2->O 4 0.147 0.446 InstALEY\_GroupBryant\_NORM2/Sh12

(InstALEY\_GroupBryant\_NORM2/Sh12)

LUT4:I2->O 1 0.147 0.000

InstALEY\_GroupBryant\_NORM2/Sh64\_f5\_F (N136)

MUXF5:I0->O 2 0.291 0.401

InstALEY\_GroupBryant\_NORM2/Sh64\_f5 (InstALEY\_GroupBryant\_NORM2/Sh64)

LUT1:I0->O 1 0.147 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12>\_rt

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12>\_rt)

MUXCY:S->O 1 0.278 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<12>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<13>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<13>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<14>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<14>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<15>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<15>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<16>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<16>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<17>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<17>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<18>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<18>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<19>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<19>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<20>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<20>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<21>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<21>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<22>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<22>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<23>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<23>)

MUXCY:CI->O 1 0.280 0.388

InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<24>

(InstALEY\_GroupBryant\_NORM2/Madd\_RoundMan\_addsub0000\_cy<24>)

LUT3:I2->O 1 0.147 0.266

InstALEY\_GroupBryant\_NORM2/RoundMan\_mux0000<25>1

(InstALEY\_GroupBryant\_NORM2/RoundMan\_mux0000<25>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<0>

(InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<0>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<1>

(InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<1>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<2>

(InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<2>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<3>

(InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<3>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<4>

(InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<4>)

MUXCY:CI->O 1 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<5>

(InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<5>)

MUXCY:CI->O 0 0.034 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<6>

(InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_cy<6>)

XORCY:CI->O 1 0.273 0.000

InstALEY\_GroupBryant\_NORM2/Madd\_exp\_mux0000\_xor<7>

(InstALEY\_GroupBryant\_NORM2/exp\_mux0000<7>)

FDE:D 0.017 InstALEY\_GroupBryant\_NORM2/Q\_30

----------------------------------------

Total 5.449ns (2.758ns logic, 2.691ns route)

(50.6% logic, 49.4% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 2460 / 795

-------------------------------------------------------------------------

Offset: 4.815ns (Levels of Logic = 2)

Source: reset (PAD)

Destination: InstALEY\_GroupBryant\_Shift\_MANTISSA/t\_SManP\_24 (FF)

Destination Clock: clk rising

Data Path: reset to InstALEY\_GroupBryant\_Shift\_MANTISSA/t\_SManP\_24

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 313 0.754 1.498 reset\_IBUF (reset\_IBUF)

BUF:I->O 310 0.269 1.489 reset\_IBUF\_1 (reset\_IBUF\_1)

FDR:R 0.805

InstALEY\_GroupBryant\_SIMPLEADDSUB/UExp\_8

----------------------------------------

Total 4.815ns (1.828ns logic, 2.987ns route)

(38.0% logic, 62.0% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 65 / 33

-------------------------------------------------------------------------

Offset: 4.799ns (Levels of Logic = 2)

Source: InstALEY\_GroupBryant\_FinalReg/sRun (FF)

Destination: SUM\_Q<31> (PAD)

Source Clock: clk rising

Data Path: InstALEY\_GroupBryant\_FinalReg/sRun to SUM\_Q<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDRE:C->Q 33 0.272 0.859

InstALEY\_GroupBryant\_FinalReg/sRun (InstALEY\_GroupBryant\_FinalReg/sRun)

LUT2:I0->O 1 0.147 0.266 SUM\_Q<9>1 (SUM\_Q\_9\_OBUF)

OBUF:I->O 3.255 SUM\_Q\_9\_OBUF (SUM\_Q<9>)

----------------------------------------

Total 4.799ns (3.674ns logic, 1.125ns route)

(76.6% logic, 23.4% route)

=========================================================================

Total REAL time to Xst completion: 24.00 secs

Total CPU time to Xst completion: 22.82 secs

-->

Total memory usage is 555216 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 24 ( 0 filtered)

Number of infos : 5 ( 0 filtered)