Adv Digital Design III

Dr. Michaela Amoo

Assigned: 02/25/2020

Due:3/5/20202

Hunter Bryant @02777748

Braxton Dula @02784592

Jordan Aley @02864549

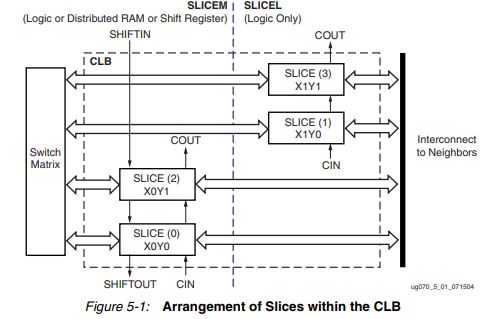
Harena Yemane @02838537

Homework #4

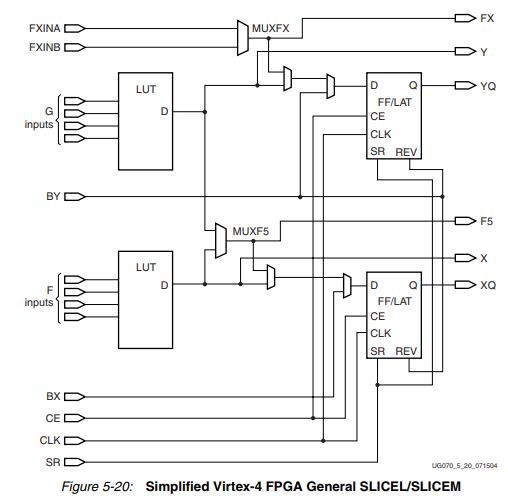
**Component Definition Critical Path Analysis:**

This section defines the components used by the synthesis tool to synthesize the five multipliers. This section also describes the critical paths of the multipliers in terms of their components.

* CLB: Configurable Logic Blocks (CLBs) are the main logic resource for implementing sequential as well as combinatorial circuits. A CLB element contains four interconnected slices grouped in pairs organized as columns. SLICEM indicates the pair of slices in the left column, and SLICEL designates the pair of slices in the right column. Each pair in a column has an independent carry chain; however, only the slices in SLICEM have a common shift chain.



* SLICE: Slices (SLICEM and SLICEL) are made up of two LUTS (look-up tables), two storage elements, wide-function multiplexers, carry logic, and arithmetic gates. These elements are used by both SLICEM and SLICEL to provide logic, arithmetic, and ROM functions. SLICEM supports two additional functions: storing data using distributed RAM and shifting data with 16-bit registers.



DSPs

* DSP48:18x18 Signed Multiplier Followed by a Three-Input Adder with Optional Pipeline Registers

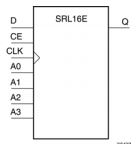
BELS:

* BUF: non inverting General Purpose Buffer
* LUT1: 1-Bit Look-Up Table with General Output
* LUT2: 2-Bit Look-Up Table with General Output
* LUT2\_D: 2-Bit Look-Up Table with Dual Output
* LUT3: 3-Bit Look-Up Table with General Output
* LUT4: 4-Bit Look-Up Table with General Output
* LUT4\_D: 4-Bit Look-Up Table with Dual Output
* LUT4\_L: 4-Bit Look-Up Table with Local Output
  + Local outputs connect to a output in the same slice
* MUXCY: 2-to-1 Multiplexer for Carry Logic with General Output
  + 2 inputs DI(direct input) and CI(carry input)
  + Select bit is driven by a LUT
* MUXF5: 2-to-1 Look-Up Table Multiplexer with General Output
  + selects between two local LUT outputs
  + Select bit is internal net
* XORCY: : XOR for Carry Logic with General Output

Flip Flops

* FDE: : D Flip-Flop with Clock Enable
* FDRE: : D Flip-Flop with Clock Enable and Synchronous Reset

Shift Registers

* SRL16E: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable
  + inputs A3, A2, A1, and A0 select the output length of the shift register, CE: clock enable, D: Data
  + can be of a fixed, static length or it can be dynamically adjusted.

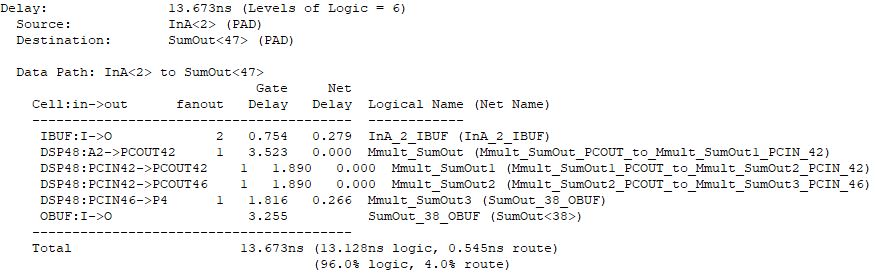
Clock Buffers

* BUFGP: : Global Clock Buffer

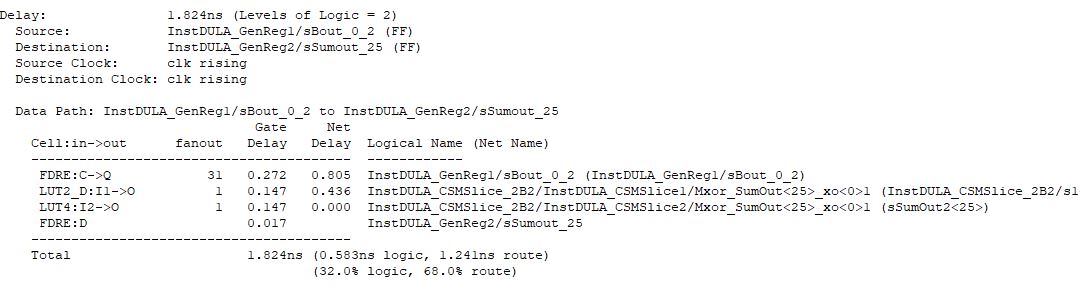
IO Buffers

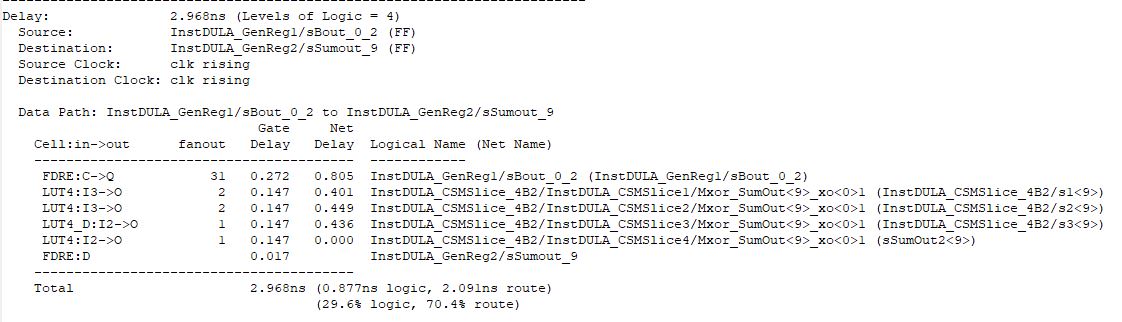
* IBUF: Input Buffer
  + automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input
* OBUF: Output Buffer
  + simple output buffer used to drive output signals to the FPGA

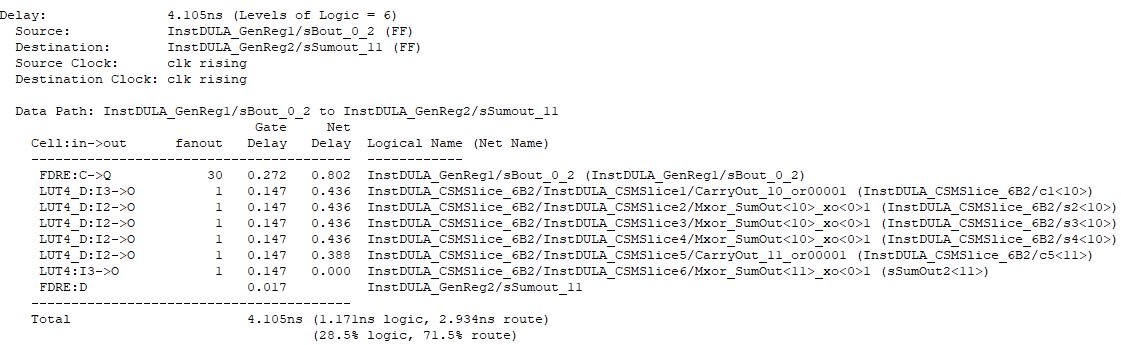
The Combinational design longest delay shown below is from the input pad to output pad. The path is made up of the input buffer IBUF, four DSP48’s, the output buffer OBUF and takes 13.673ns.

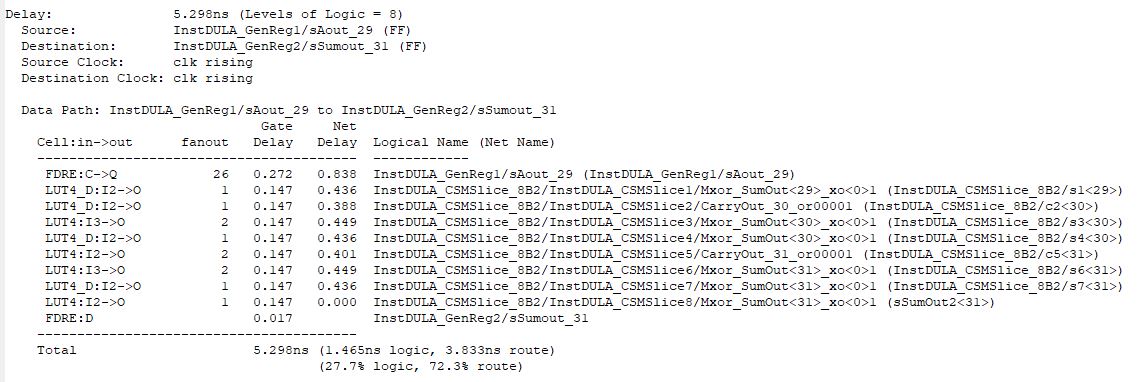


The CSM\_2B design critical path shown below is from the output of Register 1 to the outputs of Register 2. The path is made up of a FDRE flip-flop, two LUTS(LUT2\_D and LUT4), another FDRE flip-flop and takes 1.824ns.



The CSM\_4B design critical path shown below is from the output of Register 1 to the outputs of Register 2. The path is made up of a FDRE flip-flop, four LUTS(LUT4\_D and LUT4), another FDRE flip-flop and takes 2.968ns.

The CSM\_6B design critical path shown below is from the output of Register 1 to the outputs of Register 2. The path is made up of a FDRE flip-flop, six LUTS(LUT4\_D and LUT4), another FDRE flip-flop and takes 4.105ns.

The CSM\_8B design critical path shown below is from the output of Register 1 to the outputs of Register 2. The path is made up of a FDRE flip-flop, eight LUTS(LUT4\_D and LUT4), another FDRE flip-flop and takes 5.298ns.

**Comparison Of Five Designs:**

In this section the five multipliers are compared in terms of usage, critical paths and Frequency. The differences in logic and routing usage is also analysed.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Slices | Slice Flip Flops | LUT\_4s | Max Freq | Crit path route% | Crit path logic% |
| COMB | N/A | N/A | N/A | N/A | 4.0% | 96.0% |
| CSM\_2B | 795/49152  1.62% | 969/98304  0.99% | 1191/98304  1.21% | 548.264MHz | 68.0% | 32.0% |
| CSM\_4B | 629/49152  1.28% | 517/ 98304  0.53% | 1179/ 98304  1.20% | 336.979MHz | 70.4% | 29.6% |
| CSM\_6B | 619/49152  1.26% | 358/98304  0.36% | 1183/98304  1.20% | 243.591MHz | 71.5% | 28.5% |
| CSM\_8B | 631/49152  1.28% | 262/98304  0.26% | 1193/98304  1.20% | 188.749MHz | 72.3% | 27.7% |

All four of the clocked designs use roughly the same amount of LUT\_4s(~1.20%). CSM\_2B uses the most Slices and Slice flip flops but with its usage being less than 2% and 1% respectively it is not a concern. All four clocked designs have roughly the same amount of critical path route usage and logic usage with CSM\_2B having the lowest route usage and highest logic usage. What separates the four clocked designs the most is the max operating frequency with CSM\_2B having the highest at 548.264MHz. From these results CSM\_2B is the best design out of the clocked designs. Comparing the Combinational design it is much slower than the clocked designs in terms of time(13.673ns). While the Combinational design does have the lowest route usage, this is only because of the DSP48 primitives used by the COMB design. The COMB design can be done completely on one slice using only these primitives greatly reducing %route usage. However there are only 96 DSP48’s limiting the size of a combinational multiplier. Also its non-complex design(using the “x” operand) will make the operating speed vary depending on the technology on the part. Therefore out of all five designs the CSM\_2B is the best overall.

The reason the difference between the usage in routing and logic decreases as more registers are added to the design is because more registers allows for more logic to be done on a single Slice. With less registers such as the CSM\_8B, less logic can be done per Slice requiring Slices to be wired together increasing route usage. As more registers are added to a design the routing falls and the logic usage rises closing the gap.