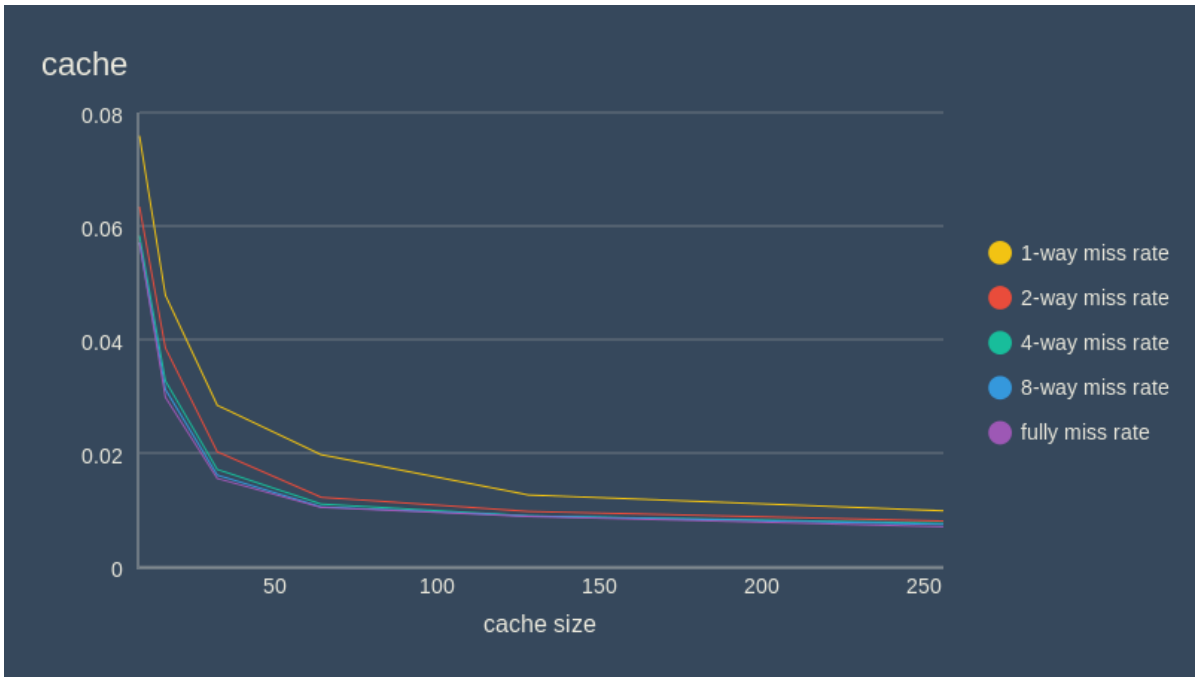
由於對於 1 種測資的測定，無法具有有效的說服力去證明 cache size 與 miss rate 的關係，所以以 gcc.din 及 spice.din 兩種測資做實驗:

1.固定參數 block size = 32,input file = gcc.din,replaced policy = FIFO

	A	B	C	D	E	F
1	cache size	1-way miss rate	2-way miss rate	4-way miss rate	8-way miss rate	full miss rate
2	8	0.0759	0.0634	0.0583	0.0571	0.0571
3	16	0.0478	0.0385	0.0327	0.0312	0.0298
4	32	0.0284	0.0202	0.0171	0.0161	0.0155
5	64	0.0197	0.0122	0.011	0.0105	0.0104
6	128	0.0126	0.0097	0.0089	0.0089	0.0088
7	256	0.0098	0.008	0.0076	0.0074	0.007



1. 固定參數 block size = 32,input file = spice.din,replaced policy = FIFO

	A	B	C	D	E	F
1	cache size	1-way miss rate	2-way miss rate	4-way miss rate	8-way miss rate	fully miss rate
2	8	0.0462	0.0298	0.0214	0.0188	0.0192
3	16	0.024	0.0111	0.0074	0.0063	0.0044
4	32	0.0099	0.0048	0.0036	0.0029	0.0027
5	64	0.004	0.0025	0.0023	0.0023	0.0021
6	128	0.0032	0.0022	0.0021	0.0021	0.0021
7	256	0.003	0.0021	0.0021	0.0021	0.0021