# dg_dtec_odf

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|---|---|---|---|---|
| 1.3.9 | reg : machineconstants_clst_thr_pkval_low_perc | 0x000007AE | 0xA0020020 | 67 |
| 1.3.10 | reg : machineconstants_clst_thr_neighbor_perc | 0x00000CCD | 0xA0020024 | 67 |
| 1.3.11 | reg : machineconstants_clst_thr_dist2antinode_perc | 0x0000599A | 0xA0020028 | 67 |
| 1.3.12 | reg : machineconstants_clst_km_nearcluster | 0x0000599A | 0xA002002C | 68 |
| 1.3.13 | reg : machineconstants_clst_em_wt_pkpos | 0x0000C000 | 0xA0020030 | 68 |
| 1.3.14 | reg : machineconstants_clst_em_centroiddist | 0x0000199A | 0xA0020034 | 68 |
| 1.3.15 | reg : machineconstants_clst_em_thr_pkval_pivot_perc | 0x0000C000 | 0xA0020038 | 68 |
| 1.3.16 | reg : machineconstants_clst_em_maxclustersize | 0x0000B333 | 0xA002003C | 68 |
| 1.3.17 | reg : machineconstants_clst_em_ds500 | 0x00009000 | 0xA0020040 | 68 |
| 1.3.18 | reg : machineconstants_clst_em_ds2m | 0x00004829 | 0xA0020044 | 68 |
| 1.3.19 | reg : machineconstants_clst_em_minclustersize | 0x00003333 | 0xA0020048 | 69 |
| 1.3.20 | reg : machineconstants_clst_em_maxdist2clustercenter_pkpos | 0x00000CCD | 0xA002004C | 69 |
| 1.3.21 | reg : machineconstants_clst_em_delta_pkpos | 0x0000028F | 0xA0020050 | 69 |
| 1.3.22 | reg : machineconstants_clst_fl_thr_pkval_2m_smaller_bound | 0x00000FF3 | 0xA0020054 | 69 |
| 1.3.23 | reg : machineconstants_clst_fl_thr_pkval_500_2m_bound | 0x00002DCC | 0xA0020058 | 69 |
| 1.3.24 | reg : machineconstants_clst_bpam_fsamp | 0x07735940 | 0xA002005C | 69 |
| 1.3.25 | reg : machineconstants_clst_thr_pkval_low_ddm_perc | 0x000007AE | 0xA0020060 | 70 |
| 1.3.26 | reg : machineconstants_clst_thr_neighbor_ddm_perc | 0x00002E14 | 0xA0020064 | 70 |
| 1.3.27 | reg : machineconstants_clst_thr_dist2antinode_ddm_perc | 0x00007333 | 0xA0020068 | 70 |
| 1.3.28 | reg : machineconstants_clst_fl_thr_pkval_500_2m_ddm_boud | 0x00002DCC | 0xA002006C | 70 |
| 1.3.29 | reg : machineconstants_clst_thr_pkval_low_tfdcm_perc | 0x0000199A | 0xA0020070 | 70 |
| 1.3.30 | reg : machineconstants_clst_thr_dist2antinode_tfdcm_perc | 0x00008000 | 0xA0020074 | 70 |
| 1.3.31 | reg : machineconstants_clst_multsatrate_dthr | 0x00000000 | 0xA0020078 | 71 |
| 1.3.32 | reg : machineconstants_clst_dcm_pkvalue_max | 0x00020000 | 0xA002007C | 71 |
| 1.3.33 | reg : machineconstants_clst_ddm_pkvalue_max | 0x00020000 | 0xA0020080 | 71 |
| 1.3.34 | reg : atomic_group1_en | 0x00000000 | 0xA0020084 | 71 |
| 1.3.35 | reg : req_func | 0x00000000 | 0xA0020088 | 71 |
| 1.3.36 | reg : idcb_manual | 0x00000000 | 0xA002008C | 71 |
| 1.3.37 | reg : events_in_events_bank1_ack | 0x00000000 | 0xA0020090 | 71 |
| 1.3.38 | reg : events_in_events_bank2_ack | 0x00000000 | 0xA0020094 | 72 |
| 1.3.39 | reg : disable_intermitent_tuning | 0x00000000 | 0xA0020098 | 72 |
| 1.3.40 | reg : ps2pl_cal_bdo_f2_opt | 0x00000000 | 0xA002009C | 72 |
| 1.3.41 | reg : ps2pl_cal_bdo_dc_opt | 0x00000000 | 0xA00200A0 | 72 |
| 1.3.42 | reg : ps2pl_cal_dcm_qc_pass | 0x00000001 | 0xA00200A4 | 72 |
| 1.3.43 | reg : ps2pl_cal_ps_general_error_reg | 0x00000000 | 0xA00200A8 | 72 |

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| 1.3.44 | reg : ps2pl_cal_advcmd | 0x00000000 | 0xA00200AC | 72 |
| 1.3.45 | reg : ps2pl_cal_spare1 | 0x00000000 | 0xA00200B0 | 72 |
| 1.3.46 | reg : ps2pl_cal_spare2 | 0x00000000 | 0xA00200B4 | 73 |
| 1.3.47 | reg : ps2pl_cal_spare3 | 0x00000000 | 0xA00200B8 | 73 |
| 1.3.48 | reg : machineconstants_idc_dphi1 | 0x00000666 | 0xA00200BC | 73 |
| 1.3.49 | reg : machineconstants_idc_dphi0 | 0x00000666 | 0xA00200C0 | 73 |
| 1.3.50 | reg : machineconstants_idc_presubthershold | 0x00000CCD | 0xA00200C4 | 73 |
| 1.3.51 | reg : machineconstants_idc_presubaveragethershold | 0x0147AE14 | 0xA00200C8 | 73 |
| 1.3.52 | reg : machineconstants_idc_xint3sigmaaveragedthershold | 0x00006666 | 0xA00200CC | 73 |
| 1.3.53 | reg : machineconstants_idc_satratioaveragethreshold_off | 0x0147AE14 | 0xA00200D0 | 74 |
| 1.3.54 | reg : machineconstants_idc_satratiothreshold | 0x00000CCD | 0xA00200D4 | 74 |
| 1.3.55 | reg : machineconstants_idc_monitoringcountermax | 0x000927C0 | 0xA00200D8 | 74 |
| 1.3.56 | reg : machineconstants_idc_monitorinitialcounter | 0x0000000A | 0xA00200DC | 74 |
| 1.3.57 | reg : machineconstants_idc_kl | 0x00004000 | 0xA00200E0 | 74 |
| 1.3.58 | reg : machineconstants_idc_kt | 0x00004000 | 0xA00200E4 | 74 |
| 1.3.59 | reg : machineconstants_idc_kc | 0xFFFFC000 | 0xA00200E8 | 74 |
| 1.3.60 | reg : machineconstants_idc_kd | 0xFFFFC000 | 0xA00200EC | 75 |
| 1.3.61 | reg : machineconstants_idc_lt | 0x00004000 | 0xA00200F0 | 75 |
| 1.3.62 | reg : machineconstants_idc_tt | 0x00002000 | 0xA00200F4 | 75 |
| 1.3.63 | reg : machineconstants_idc_ct | 0x00004000 | 0xA00200F8 | 75 |
| 1.3.64 | reg : machineconstants_idc_dt | 0xFFFFF000 | 0xA00200FC | 75 |
| 1.3.65 | reg : machineconstants_idc_td | 0xFFFFE666 | 0xA0020100 | 75 |
| 1.3.66 | reg : machineconstants_idc_d_thr | 0x00000000 | 0xA0020104 | 75 |
| 1.3.67 | reg : machineconstants_idc_maincliteration | 0x00000064 | 0xA0020108 | 75 |
| 1.3.68 | reg : machineconstants_idc_tuningintervalstimemax | 0x0000000A | 0xA002010C | 76 |
| 1.3.69 | reg : machineconstants_idc_phasecorrectionphi0 | 0x0000019A | 0xA0020110 | 76 |
| 1.3.70 | reg : machineconstants_idc_phasecorrectionphi1 | 0x0000019A | 0xA0020114 | 76 |
| 1.3.71 | reg : machineconstants_idc_amplitudereduction | 0x0000039A | 0xA0020118 | 76 |
| 1.3.72 | reg : machineconstants_idc_a0max | 0x00005000 | 0xA002011C | 76 |
| 1.3.73 | reg : machineconstants_idc_a0min | 0x00000066 | 0xA0020120 | 76 |
| 1.3.74 | reg : machineconstants_idc_a1max | 0x00005000 | 0xA0020124 | 76 |
| 1.3.75 | reg : machineconstants_idc_a1min | 0x00000066 | 0xA0020128 | 77 |
| 1.3.76 | reg : machineconstants_idc_voltagemax | 0x00010400 | 0xA002012C | 77 |
| 1.3.77 | reg : machineconstants_idc_lmargin | 0x0000028F | 0xA0020130 | 77 |
| 1.3.78 | reg : machineconstants_idc_tmargin | 0x0000028F | 0xA0020134 | 77 |
| 1.3.79 | reg : machineconstants_idc_cmargin | 0x0000028F | 0xA0020138 | 77 |

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| 1.3.80 | reg : machineconstants_idc_dmargin | 0x0000028F | 0xA002013C | 77 |
| 1.3.81 | reg : machineconstants_idc_subclcountermax | 0x0000000A | 0xA0020140 | 77 |
| 1.3.82 | reg : machineconstants_idc_peakmissedratethreshold | 0x00000CCD | 0xA0020144 | 78 |
| 1.3.83 | reg : machineconstants_idc_multsatratiothreshold | 0x00000CCD | 0xA0020148 | 78 |
| 1.3.84 | reg : machineconstants_idc_sigmacthreshold | 0x00000CCD | 0xA002014C | 78 |
| 1.3.85 | reg : machineconstants_idc_sigmalthreshold | 0x00000148 | 0xA0020150 | 78 |
| 1.3.86 | reg : machineconstants_idc_falltimedetectionmax | 0x000003E8 | 0xA0020154 | 78 |
| 1.3.87 | reg : machineconstants_idc_averaginglength | 0x000007D0 | 0xA0020158 | 78 |
| 1.3.88 | reg : machineconstants_idc_maincl_holdoffcounter | 0x00000007 | 0xA002015C | 78 |
| 1.3.89 | reg : machineconstants_idc_subclopt_holdoffcounter | 0x00000005 | 0xA0020160 | 79 |
| 1.3.90 | reg : machineconstants_idc_subclbk_holdoffcounter | 0x00000007 | 0xA0020164 | 79 |
| 1.3.91 | reg : machineconstants_idc_exposure_earlyexposurethreshold | 0x00000000 | 0xA0020168 | 79 |
| 1.3.92 | reg : machineconstants_idc_idcbtriggerconfig | 0x00000000 | 0xA002016C | 79 |
| 1.3.93 | reg : machineconstants_idc_monitoringcountersafedamp | 0x0000000B | 0xA0020170 | 79 |
| 1.3.94 | reg : machineconstants_idc_exposuremonitoringcountermax | 0x0000000A | 0xA0020174 | 79 |
| 1.3.95 | reg : machineconstants_idc_dcmbpam2dtec_crcerrthr | 0x00000006 | 0xA0020178 | 80 |
| 1.3.96 | reg : machineconstants_idc_ddmbpam2dtec_crcerrthr | 0x00000006 | 0xA002017C | 80 |
| 1.3.97 | reg : machineconstants_idc_dcmbpam2dtec_minnumvalidpkshr | 0x00000032 | 0xA0020180 | 80 |
| 1.3.98 | reg : machineconstants_idc_ddmbpam2dtec_minnumvalidpkshr | 0x00000032 | 0xA0020184 | 80 |
| 1.3.99 | reg : machineconstants_idc_dcm_signallevel_min | 0x00006666 | 0xA0020188 | 80 |
| 1.3.100 | reg : machineconstants_idc_ddm_signallevel_min | 0x00004CCD | 0xA002018C | 80 |
| 1.3.101 | reg : machineconstants_idc_phi0marginholdoff | 0x00124F80 | 0xA0020190 | 80 |
| 1.3.102 | reg : machineconstants_idc_dcmqualitycountermax | 0x0000000A | 0xA0020194 | 81 |
| 1.3.103 | reg : machineconstants_idc_ddmqualitycountermax | 0x0000000A | 0xA0020198 | 81 |
| 1.3.104 | reg : machineconstants_idc_healthsignals_config | 0x000000FF | 0xA002019C | 81 |
| 1.3.105 | reg : machineconstants_idc_oavsub_phi1marginres | 0x000000CD | 0xA00201A0 | 81 |
| 1.3.106 | reg : machineconstants_idc_oavsub_phi1marginnum | 0x00000005 | 0xA00201A4 | 81 |
| 1.3.107 | reg : machineconstants_idc_oavsub_ddmlatency | 0x00000003 | 0xA00201A8 | 81 |
| 1.3.108 | reg : machineconstants_idc_oavmain_phi0marginres | 0x000000CD | 0xA00201AC | 81 |
| 1.3.109 | reg : machineconstants_idc_oavmain_phi0marginnum | 0x00000005 | 0xA00201B0 | 82 |
| 1.3.110 | reg : machineconstants_idc_oav_config | 0x00000000 | 0xA00201B4 | 82 |
| 1.3.111 | reg : machineconstants_idc_coveragesourcereprate_perc | 0x0000199A | 0xA00201B8 | 82 |
| 1.3.112 | reg : machineconstants_idc_t | 0x0000199A | 0xA00201BC | 82 |

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| | f_coverage_operatingband_thr | | | |
| 1.3.113 | reg : machineconstants_idc_workingsubclfreqs | 0x00000001 | 0xA00201C0 | 82 |
| 1.3.114 | reg : machineconstants_idc_workingsubclvoltage_thr | 0x00000001 | 0xA00201C4 | 82 |
| 1.3.115 | reg : machineconstants_idc_satratioaveragethreshold_on | 0x9999999A | 0xA00201C8 | 83 |
| 1.3.116 | reg : machineconstants_idc_ddmdowntime | 0x000927C0 | 0xA00201CC | 83 |
| 1.3.117 | reg : machineconstants_idc_dcm_bl_thr | 0x00010000 | 0xA00201D0 | 83 |
| 1.3.118 | reg : machineconstants_idc_ddm_bl_thr | 0x00010000 | 0xA00201D4 | 83 |
| 1.3.119 | reg : machineconstants_idc_dcm_missingdroplets_thr | 0x0000000A | 0xA00201D8 | 83 |
| 1.3.120 | reg : machineconstants_idc_ddm_missingdroplets_thr | 0x0000000A | 0xA00201DC | 83 |
| 1.3.121 | reg : machineconstants_idc_exposureoff_holdoffcounter | 0x00000001 | 0xA00201E0 | 83 |
| 1.3.122 | reg : machineconstants_idc_exposureon_holdoffcounter | 0x00000001 | 0xA00201E4 | 84 |
| 1.3.123 | reg : machineconstants_idc_dcm_pksaturation_thr | 0x00010000 | 0xA00201E8 | 84 |
| 1.3.124 | reg : machineconstants_idc_ddm_pksaturation_thr | 0x00010000 | 0xA00201EC | 84 |
| 1.3.125 | reg : machineconstants_idc_spcfg_03 | 0x00000003 | 0xA00201F0 | 84 |
| 1.3.126 | reg : machineconstants_idc_spcfg_04 | 0x00000001 | 0xA00201F4 | 84 |
| 1.3.127 | reg : machineconstants_idc_spcfg_05 | 0x00000008 | 0xA00201F8 | 84 |
| 1.3.128 | reg : machineconstants_idc_spcfg_06 | 0x0000EA60 | 0xA00201FC | 84 |
| 1.3.129 | reg : machineconstants_idc_spcfg_07 | 0x00000008 | 0xA0020200 | 85 |
| 1.3.130 | reg : machineconstants_idc_spcfg_08 | 0x000493E0 | 0xA0020204 | 85 |
| 1.3.131 | reg : machineconstants_idc_spcfg_09 | 0x00000003 | 0xA0020208 | 85 |
| 1.3.132 | reg : machineconstants_idc_spcfg_10 | 0x0000EA60 | 0xA002020C | 85 |
| 1.3.133 | reg : machineconstants_idc_spcfg_11 | 0x0000000A | 0xA0020210 | 85 |
| 1.3.134 | reg : machineconstants_idc_spcfg_12 | 0x000A1220 | 0xA0020214 | 85 |
| 1.3.135 | reg : machineconstants_idc_spcfg_13 | 0x00000000 | 0xA0020218 | 85 |
| 1.3.136 | reg : machineconstants_idc_spcfg_14 | 0x0000000A | 0xA002021C | 86 |
| 1.3.137 | reg : machineconstants_idc_spcfg_15 | 0x000927C0 | 0xA0020220 | 86 |
| 1.3.138 | reg : machineconstants_idc_spcfg_16 | 0x00000000 | 0xA0020224 | 86 |
| 1.3.139 | reg : machineconstants_idc_spcfg_17 | 0x00000000 | 0xA0020228 | 86 |
| 1.3.140 | reg : machineconstants_idc_spcfg_18 | 0x00000000 | 0xA002022C | 86 |
| 1.3.141 | reg : machineconstants_idc_spcfg_19 | 0x00000000 | 0xA0020230 | 86 |
| 1.3.142 | reg : machineconstants_idc_spcfg_20 | 0x00000000 | 0xA0020234 | 86 |
| 1.3.143 | reg : machineconstants_cmd_manualtuningwaveformtype | 0x00000000 | 0xA0020238 | 86 |
| 1.3.144 | reg : machineconstants_cmd_tssw_dutycycle | 0x0000000A | 0xA002023C | 87 |
| 1.3.145 | reg : machineconstants_cmd_t | 0x00000000 | 0xA0020240 | 87 |

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| | ssw_risetime | | | |
| 1.3.146 | reg : machineconstants_cmd_tssw_sineamplitude0 | 0x00001400 | 0xA0020244 | 87 |
| 1.3.147 | reg : machineconstants_cmd_tssw_sineamplitude1 | 0x00001400 | 0xA0020248 | 87 |
| 1.3.148 | reg : machineconstants_cmd_tssw_sinefrequency | 0x03A98000 | 0xA002024C | 87 |
| 1.3.149 | reg : machineconstants_cmd_tssw_sinefrequencymultiplier | 0x00002800 | 0xA0020250 | 87 |
| 1.3.150 | reg : machineconstants_cmd_tssw_sinephase0 | 0x00000000 | 0xA0020254 | 88 |
| 1.3.151 | reg : machineconstants_cmd_tssw_sinephase1 | 0x00000000 | 0xA0020258 | 88 |
| 1.3.152 | reg : machineconstants_cmd_tssw_squareamplitude | 0x00000800 | 0xA002025C | 88 |
| 1.3.153 | reg : machineconstants_cmd_tssw_squarefrequencymultiplier | 0x00001000 | 0xA0020260 | 88 |
| 1.3.154 | reg : machineconstants_cmd_stup_dutycycle | 0x0000000A | 0xA0020264 | 88 |
| 1.3.155 | reg : machineconstants_cmd_stup_risetime | 0x00000000 | 0xA0020268 | 88 |
| 1.3.156 | reg : machineconstants_cmd_stup_sineamplitude0 | 0x00000400 | 0xA002026C | 88 |
| 1.3.157 | reg : machineconstants_cmd_stup_sineamplitude1 | 0x00000400 | 0xA0020270 | 89 |
| 1.3.158 | reg : machineconstants_cmd_stup_sinefrequency | 0x03C8C000 | 0xA0020274 | 89 |
| 1.3.159 | reg : machineconstants_cmd_stup_sinefrequencymultiplier | 0x00002800 | 0xA0020278 | 89 |
| 1.3.160 | reg : machineconstants_cmd_stup_sinephase0 | 0x00000000 | 0xA002027C | 89 |
| 1.3.161 | reg : machineconstants_cmd_stup_sinephase1 | 0x00000000 | 0xA0020280 | 89 |
| 1.3.162 | reg : machineconstants_cmd_stup_squareamplitude | 0x00001000 | 0xA0020284 | 89 |
| 1.3.163 | reg : machineconstants_cmd_stup_squarefrequencymultiplier | 0x00001000 | 0xA0020288 | 89 |
| 1.3.164 | reg : machineconstants_cmd_hw_dutycycle | 0x0000000A | 0xA002028C | 90 |
| 1.3.165 | reg : machineconstants_cmd_hw_risetime | 0x02AF31DC | 0xA0020290 | 90 |
| 1.3.166 | reg : machineconstants_cmd_hw_sineamplitude | 0x00001400 | 0xA0020294 | 90 |
| 1.3.167 | reg : machineconstants_cmd_hw_sinefrequency | 0x03A98000 | 0xA0020298 | 90 |
| 1.3.168 | reg : machineconstants_cmd_hw_squareamplitude | 0x00000800 | 0xA002029C | 90 |
| 1.3.169 | reg : machineconstants_cmd_hw_squarefrequencymultiplier | 0x00001000 | 0xA00202A0 | 90 |
| 1.3.170 | reg : machineconstants_cmd_hw_squarephase | 0x00000000 | 0xA00202A4 | 91 |
| 1.3.171 | reg : machineconstants_cmd_sw_dutycycle | 0x0000000A | 0xA00202A8 | 91 |
| 1.3.172 | reg : machineconstants_cmd_sw_risetime | 0x0044B830 | 0xA00202AC | 91 |
| 1.3.173 | reg : machineconstants_cmd_sw_squareamplitude | 0x00001400 | 0xA00202B0 | 91 |
| 1.3.174 | reg : machineconstants_cmd_sw_squarefrequency | 0x03A98000 | 0xA00202B4 | 91 |
| 1.3.175 | reg : machineconstants_cmd_waveform_enable | 0x00000001 | 0xA00202B8 | 91 |
| 1.3.176 | reg : machineconstants_slt_solutiontype | 0x00000000 | 0xA00202BC | 91 |
| 1.3.177 | reg : machineconstants_slt_hyperparameters_1 | 0x03A98000 | 0xA00202C0 | 92 |

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| 1.3.178 | reg : machineconstants_slt_hyperparameters_2 | 0x00002800 | 0xA00202C4 | 92 |
| 1.3.179 | reg : machineconstants_slt_hyperparameters_3 | 0x00001000 | 0xA00202C8 | 92 |
| 1.3.180 | reg : machineconstants_slt_hyperparameters_4 | 0x00000800 | 0xA00202CC | 92 |
| 1.3.181 | reg : machineconstants_slt_sineamps_1 | 0x00001400 | 0xA00202D0 | 92 |
| 1.3.182 | reg : machineconstants_slt_sineamps_2 | 0x00001400 | 0xA00202D4 | 92 |
| 1.3.183 | reg : machineconstants_slt_phi0_1 | 0x00000000 | 0xA00202D8 | 92 |
| 1.3.184 | reg : machineconstants_slt_phi0_2 | 0x00000000 | 0xA00202DC | 93 |
| 1.3.185 | reg : machineconstants_slt_phi0_3 | 0x00000000 | 0xA00202E0 | 93 |
| 1.3.186 | reg : machineconstants_slt_phi0_4 | 0x00000000 | 0xA00202E4 | 93 |
| 1.3.187 | reg : machineconstants_slt_phi0_5 | 0x00000000 | 0xA00202E8 | 93 |
| 1.3.188 | reg : machineconstants_slt_phi0_6 | 0x00000000 | 0xA00202EC | 93 |
| 1.3.189 | reg : machineconstants_slt_phi0_7 | 0x00000000 | 0xA00202F0 | 93 |
| 1.3.190 | reg : machineconstants_slt_phi0_8 | 0x00000000 | 0xA00202F4 | 93 |
| 1.3.191 | reg : machineconstants_slt_phi0_9 | 0x00000000 | 0xA00202F8 | 93 |
| 1.3.192 | reg : machineconstants_slt_phi0_10 | 0x00000000 | 0xA00202FC | 94 |
| 1.3.193 | reg : machineconstants_slt_phi0_11 | 0x00000000 | 0xA0020300 | 94 |
| 1.3.194 | reg : machineconstants_slt_phi0_12 | 0x00000000 | 0xA0020304 | 94 |
| 1.3.195 | reg : machineconstants_slt_phi0_13 | 0x00000000 | 0xA0020308 | 94 |
| 1.3.196 | reg : machineconstants_slt_phi0_14 | 0x00000000 | 0xA002030C | 94 |
| 1.3.197 | reg : machineconstants_slt_phi0_15 | 0x00000000 | 0xA0020310 | 94 |
| 1.3.198 | reg : machineconstants_slt_phi0_16 | 0x00000000 | 0xA0020314 | 94 |
| 1.3.199 | reg : machineconstants_slt_phi0_17 | 0x00000000 | 0xA0020318 | 94 |
| 1.3.200 | reg : machineconstants_slt_phi0_18 | 0x00000000 | 0xA002031C | 95 |
| 1.3.201 | reg : machineconstants_slt_phi0_19 | 0x00000000 | 0xA0020320 | 95 |
| 1.3.202 | reg : machineconstants_slt_phi1_1 | 0x00000000 | 0xA0020324 | 95 |
| 1.3.203 | reg : machineconstants_slt_phi1_2 | 0x00000000 | 0xA0020328 | 95 |
| 1.3.204 | reg : machineconstants_slt_phi1_3 | 0x00000000 | 0xA002032C | 95 |
| 1.3.205 | reg : machineconstants_slt_phi1_4 | 0x00000000 | 0xA0020330 | 95 |
| 1.3.206 | reg : machineconstants_slt_phi1_5 | 0x00000000 | 0xA0020334 | 95 |
| 1.3.207 | reg : machineconstants_slt_phi1_6 | 0x00000000 | 0xA0020338 | 96 |
| 1.3.208 | reg : machineconstants_slt_phi1_7 | 0x00000000 | 0xA002033C | 96 |
| 1.3.209 | reg : machineconstants_slt_phi1_8 | 0x00000000 | 0xA0020340 | 96 |
| 1.3.210 | reg : machineconstants_slt_phi1_9 | 0x00000000 | 0xA0020344 | 96 |
| 1.3.211 | reg : machineconstants_slt_phi1_10 | 0x00000000 | 0xA0020348 | 96 |

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| 1.3.212 | reg : machineconstants_slt_phi1_11 | 0x00000000 | 0xA002034C | 96 |
| 1.3.213 | reg : machineconstants_slt_phi1_12 | 0x00000000 | 0xA0020350 | 96 |
| 1.3.214 | reg : machineconstants_slt_phi1_13 | 0x00000000 | 0xA0020354 | 96 |
| 1.3.215 | reg : machineconstants_slt_phi1_14 | 0x00000000 | 0xA0020358 | 97 |
| 1.3.216 | reg : machineconstants_slt_phi1_15 | 0x00000000 | 0xA002035C | 97 |
| 1.3.217 | reg : machineconstants_slt_phi1_16 | 0x00000000 | 0xA0020360 | 97 |
| 1.3.218 | reg : machineconstants_slt_phi1_17 | 0x00000000 | 0xA0020364 | 97 |
| 1.3.219 | reg : machineconstants_slt_phi1_18 | 0x00000000 | 0xA0020368 | 97 |
| 1.3.220 | reg : machineconstants_slt_phi1_19 | 0x00000000 | 0xA002036C | 97 |
| 1.3.221 | reg : machineconstants_slt_presubcoal_flag_1 | 0x00000001 | 0xA0020370 | 97 |
| 1.3.222 | reg : machineconstants_slt_presubcoal_flag_2 | 0x00000001 | 0xA0020374 | 98 |
| 1.3.223 | reg : machineconstants_slt_presubcoal_flag_3 | 0x00000001 | 0xA0020378 | 98 |
| 1.3.224 | reg : machineconstants_slt_presubcoal_flag_4 | 0x00000001 | 0xA002037C | 98 |
| 1.3.225 | reg : machineconstants_slt_presubcoal_flag_5 | 0x00000001 | 0xA0020380 | 98 |
| 1.3.226 | reg : machineconstants_slt_presubcoal_flag_6 | 0x00000001 | 0xA0020384 | 98 |
| 1.3.227 | reg : machineconstants_slt_presubcoal_flag_7 | 0x00000001 | 0xA0020388 | 98 |
| 1.3.228 | reg : machineconstants_slt_presubcoal_flag_8 | 0x00000001 | 0xA002038C | 98 |
| 1.3.229 | reg : machineconstants_slt_presubcoal_flag_9 | 0x00000001 | 0xA0020390 | 99 |
| 1.3.230 | reg : machineconstants_slt_presubcoal_flag_10 | 0x00000001 | 0xA0020394 | 99 |
| 1.3.231 | reg : machineconstants_slt_presubcoal_flag_11 | 0x00000001 | 0xA0020398 | 99 |
| 1.3.232 | reg : machineconstants_slt_presubcoal_flag_12 | 0x00000001 | 0xA002039C | 99 |
| 1.3.233 | reg : machineconstants_slt_presubcoal_flag_13 | 0x00000001 | 0xA00203A0 | 99 |
| 1.3.234 | reg : machineconstants_slt_presubcoal_flag_14 | 0x00000001 | 0xA00203A4 | 99 |
| 1.3.235 | reg : machineconstants_slt_presubcoal_flag_15 | 0x00000001 | 0xA00203A8 | 99 |
| 1.3.236 | reg : machineconstants_slt_presubcoal_flag_16 | 0x00000001 | 0xA00203AC | 100 |
| 1.3.237 | reg : machineconstants_slt_presubcoal_flag_17 | 0x00000001 | 0xA00203B0 | 100 |
| 1.3.238 | reg : machineconstants_slt_presubcoal_flag_18 | 0x00000001 | 0xA00203B4 | 100 |
| 1.3.239 | reg : machineconstants_slt_presubcoal_flag_19 | 0x00000001 | 0xA00203B8 | 100 |
| 1.3.240 | reg : machineconstants_slt_jitter_1 | 0x00000000 | 0xA00203BC | 100 |
| 1.3.241 | reg : machineconstants_slt_jitter_2 | 0x00000000 | 0xA00203C0 | 100 |
| 1.3.242 | reg : machineconstants_slt_jitter_3 | 0x00000000 | 0xA00203C4 | 100 |
| 1.3.243 | reg : machineconstants_slt_jitter_4 | 0x00000000 | 0xA00203C8 | 101 |
| 1.3.244 | reg : machineconstants_slt_jitter_5 | 0x00000000 | 0xA00203CC | 101 |
| 1.3.245 | reg : machineconstants_slt_jitter_6 | 0x00000000 | 0xA00203D0 | 101 |

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|---|---|---|---|---|
| 1.3.246 | reg : machineconstants_slt_jitter_7 | 0x00000000 | 0xA00203D4 | 101 |
| 1.3.247 | reg : machineconstants_slt_jitter_8 | 0x00000000 | 0xA00203D8 | 101 |
| 1.3.248 | reg : machineconstants_slt_jitter_9 | 0x00000000 | 0xA00203DC | 101 |
| 1.3.249 | reg : machineconstants_slt_jitter_10 | 0x00000000 | 0xA00203E0 | 101 |
| 1.3.250 | reg : machineconstants_slt_jitter_11 | 0x00000000 | 0xA00203E4 | 101 |
| 1.3.251 | reg : machineconstants_slt_jitter_12 | 0x00000000 | 0xA00203E8 | 102 |
| 1.3.252 | reg : machineconstants_slt_jitter_13 | 0x00000000 | 0xA00203EC | 102 |
| 1.3.253 | reg : machineconstants_slt_jitter_14 | 0x00000000 | 0xA00203F0 | 102 |
| 1.3.254 | reg : machineconstants_slt_jitter_15 | 0x00000000 | 0xA00203F4 | 102 |
| 1.3.255 | reg : machineconstants_slt_jitter_16 | 0x00000000 | 0xA00203F8 | 102 |
| 1.3.256 | reg : machineconstants_slt_jitter_17 | 0x00000000 | 0xA00203FC | 102 |
| 1.3.257 | reg : machineconstants_slt_jitter_18 | 0x00000000 | 0xA0020400 | 102 |
| 1.3.258 | reg : machineconstants_slt_jitter_19 | 0x00000000 | 0xA0020404 | 102 |
| 1.3.259 | reg : machineconstants_slt_multpresubrate_1 | 0x00000000 | 0xA0020408 | 103 |
| 1.3.260 | reg : machineconstants_slt_multpresubrate_2 | 0x00000000 | 0xA002040C | 103 |
| 1.3.261 | reg : machineconstants_slt_multpresubrate_3 | 0x00000000 | 0xA0020410 | 103 |
| 1.3.262 | reg : machineconstants_slt_multpresubrate_4 | 0x00000000 | 0xA0020414 | 103 |
| 1.3.263 | reg : machineconstants_slt_multpresubrate_5 | 0x00000000 | 0xA0020418 | 103 |
| 1.3.264 | reg : machineconstants_slt_multpresubrate_6 | 0x00000000 | 0xA002041C | 103 |
| 1.3.265 | reg : machineconstants_slt_multpresubrate_7 | 0x00000000 | 0xA0020420 | 103 |
| 1.3.266 | reg : machineconstants_slt_multpresubrate_8 | 0x00000000 | 0xA0020424 | 104 |
| 1.3.267 | reg : machineconstants_slt_multpresubrate_9 | 0x00000000 | 0xA0020428 | 104 |
| 1.3.268 | reg : machineconstants_slt_multpresubrate_10 | 0x00000000 | 0xA002042C | 104 |
| 1.3.269 | reg : machineconstants_slt_multpresubrate_11 | 0x00000000 | 0xA0020430 | 104 |
| 1.3.270 | reg : machineconstants_slt_multpresubrate_12 | 0x00000000 | 0xA0020434 | 104 |
| 1.3.271 | reg : machineconstants_slt_multpresubrate_13 | 0x00000000 | 0xA0020438 | 104 |
| 1.3.272 | reg : machineconstants_slt_multpresubrate_14 | 0x00000000 | 0xA002043C | 105 |
| 1.3.273 | reg : machineconstants_slt_multpresubrate_15 | 0x00000000 | 0xA0020440 | 105 |
| 1.3.274 | reg : machineconstants_slt_multpresubrate_16 | 0x00000000 | 0xA0020444 | 105 |
| 1.3.275 | reg : machineconstants_slt_multpresubrate_17 | 0x00000000 | 0xA0020448 | 105 |
| 1.3.276 | reg : machineconstants_slt_multpresubrate_18 | 0x00000000 | 0xA002044C | 105 |
| 1.3.277 | reg : machineconstants_slt_multpresubrate_19 | 0x00000000 | 0xA0020450 | 105 |
| 1.3.278 | reg : machineconstants_slt_presubrate_1 | 0x00000000 | 0xA0020454 | 105 |
| 1.3.279 | reg : machineconstants_slt_presubrate_2 | 0x00000000 | 0xA0020458 | 106 |

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|---|---|---|---|---|
| 1.3.280 | reg : machineconstants_slt_presubrate_3 | 0x00000000 | 0xA002045C | 106 |
| 1.3.281 | reg : machineconstants_slt_presubrate_4 | 0x00000000 | 0xA0020460 | 106 |
| 1.3.282 | reg : machineconstants_slt_presubrate_5 | 0x00000000 | 0xA0020464 | 106 |
| 1.3.283 | reg : machineconstants_slt_presubrate_6 | 0x00000000 | 0xA0020468 | 106 |
| 1.3.284 | reg : machineconstants_slt_presubrate_7 | 0x00000000 | 0xA002046C | 106 |
| 1.3.285 | reg : machineconstants_slt_presubrate_8 | 0x00000000 | 0xA0020470 | 106 |
| 1.3.286 | reg : machineconstants_slt_presubrate_9 | 0x00000000 | 0xA0020474 | 107 |
| 1.3.287 | reg : machineconstants_slt_presubrate_10 | 0x00000000 | 0xA0020478 | 107 |
| 1.3.288 | reg : machineconstants_slt_presubrate_11 | 0x00000000 | 0xA002047C | 107 |
| 1.3.289 | reg : machineconstants_slt_presubrate_12 | 0x00000000 | 0xA0020480 | 107 |
| 1.3.290 | reg : machineconstants_slt_presubrate_13 | 0x00000000 | 0xA0020484 | 107 |
| 1.3.291 | reg : machineconstants_slt_presubrate_14 | 0x00000000 | 0xA0020488 | 107 |
| 1.3.292 | reg : machineconstants_slt_presubrate_15 | 0x00000000 | 0xA002048C | 107 |
| 1.3.293 | reg : machineconstants_slt_presubrate_16 | 0x00000000 | 0xA0020490 | 108 |
| 1.3.294 | reg : machineconstants_slt_presubrate_17 | 0x00000000 | 0xA0020494 | 108 |
| 1.3.295 | reg : machineconstants_slt_presubrate_18 | 0x00000000 | 0xA0020498 | 108 |
| 1.3.296 | reg : machineconstants_slt_presubrate_19 | 0x00000000 | 0xA002049C | 108 |
| 1.3.297 | reg : machineconstants_slt_cm_1 | 0x00000000 | 0xA00204A0 | 108 |
| 1.3.298 | reg : machineconstants_slt_cm_2 | 0x00000000 | 0xA00204A4 | 108 |
| 1.3.299 | reg : machineconstants_slt_cm_3 | 0x00000000 | 0xA00204A8 | 108 |
| 1.3.300 | reg : machineconstants_slt_cm_4 | 0x00000000 | 0xA00204AC | 109 |
| 1.3.301 | reg : machineconstants_slt_cm_5 | 0x00000000 | 0xA00204B0 | 109 |
| 1.3.302 | reg : machineconstants_slt_cm_6 | 0x00000000 | 0xA00204B4 | 109 |
| 1.3.303 | reg : machineconstants_slt_cm_7 | 0x00000000 | 0xA00204B8 | 109 |
| 1.3.304 | reg : machineconstants_slt_cm_8 | 0x00000000 | 0xA00204BC | 109 |
| 1.3.305 | reg : machineconstants_slt_cm_9 | 0x00000000 | 0xA00204C0 | 109 |
| 1.3.306 | reg : machineconstants_slt_cm_10 | 0x00000000 | 0xA00204C4 | 109 |
| 1.3.307 | reg : machineconstants_slt_cm_11 | 0x00000000 | 0xA00204C8 | 109 |
| 1.3.308 | reg : machineconstants_slt_cm_12 | 0x00000000 | 0xA00204CC | 110 |
| 1.3.309 | reg : machineconstants_slt_cm_13 | 0x00000000 | 0xA00204D0 | 110 |
| 1.3.310 | reg : machineconstants_slt_cm_14 | 0x00000000 | 0xA00204D4 | 110 |
| 1.3.311 | reg : machineconstants_slt_cm_15 | 0x00000000 | 0xA00204D8 | 110 |
| 1.3.312 | reg : machineconstants_slt_cm_16 | 0x00000000 | 0xA00204DC | 110 |
| 1.3.313 | reg : machineconstants_slt_cm_17 | 0x00000000 | 0xA00204E0 | 110 |

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| 1.3.314 | reg : machineconstants_slt_cm_18 | 0x00000000 | 0xA00204E4 | 110 |
| 1.3.315 | reg : machineconstants_slt_cm_19 | 0x00000000 | 0xA00204E8 | 110 |
| 1.3.316 | reg : machineconstants_slt_dm_1 | 0x00000000 | 0xA00204EC | 111 |
| 1.3.317 | reg : machineconstants_slt_dm_2 | 0x00000000 | 0xA00204F0 | 111 |
| 1.3.318 | reg : machineconstants_slt_dm_3 | 0x00000000 | 0xA00204F4 | 111 |
| 1.3.319 | reg : machineconstants_slt_dm_4 | 0x00000000 | 0xA00204F8 | 111 |
| 1.3.320 | reg : machineconstants_slt_dm_5 | 0x00000000 | 0xA00204FC | 111 |
| 1.3.321 | reg : machineconstants_slt_dm_6 | 0x00000000 | 0xA0020500 | 111 |
| 1.3.322 | reg : machineconstants_slt_dm_7 | 0x00000000 | 0xA0020504 | 111 |
| 1.3.323 | reg : machineconstants_slt_dm_8 | 0x00000000 | 0xA0020508 | 112 |
| 1.3.324 | reg : machineconstants_slt_dm_9 | 0x00000000 | 0xA002050C | 112 |
| 1.3.325 | reg : machineconstants_slt_dm_10 | 0x00000000 | 0xA0020510 | 112 |
| 1.3.326 | reg : machineconstants_slt_dm_11 | 0x00000000 | 0xA0020514 | 112 |
| 1.3.327 | reg : machineconstants_slt_dm_12 | 0x00000000 | 0xA0020518 | 112 |
| 1.3.328 | reg : machineconstants_slt_dm_13 | 0x00000000 | 0xA002051C | 112 |
| 1.3.329 | reg : machineconstants_slt_dm_14 | 0x00000000 | 0xA0020520 | 112 |
| 1.3.330 | reg : machineconstants_slt_dm_15 | 0x00000000 | 0xA0020524 | 112 |
| 1.3.331 | reg : machineconstants_slt_dm_16 | 0x00000000 | 0xA0020528 | 113 |
| 1.3.332 | reg : machineconstants_slt_dm_17 | 0x00000000 | 0xA002052C | 113 |
| 1.3.333 | reg : machineconstants_slt_dm_18 | 0x00000000 | 0xA0020530 | 113 |
| 1.3.334 | reg : machineconstants_slt_dm_19 | 0x00000000 | 0xA0020534 | 113 |
| 1.3.335 | reg : machineconstants_slt_dcdphi | 0x00000000 | 0xA0020538 | 113 |
| 1.3.336 | reg : machineconstants_slt_phi1margin_1 | 0x00000000 | 0xA002053C | 113 |
| 1.3.337 | reg : machineconstants_slt_phi1margin_2 | 0x00000000 | 0xA0020540 | 113 |
| 1.3.338 | reg : machineconstants_slt_phi1margin_3 | 0x00000000 | 0xA0020544 | 114 |
| 1.3.339 | reg : machineconstants_slt_phi1margin_4 | 0x00000000 | 0xA0020548 | 114 |
| 1.3.340 | reg : machineconstants_slt_phi1margin_5 | 0x00000000 | 0xA002054C | 114 |
| 1.3.341 | reg : machineconstants_slt_phi1margin_6 | 0x00000000 | 0xA0020550 | 114 |
| 1.3.342 | reg : machineconstants_slt_phi1margin_7 | 0x00000000 | 0xA0020554 | 114 |
| 1.3.343 | reg : machineconstants_slt_phi1margin_8 | 0x00000000 | 0xA0020558 | 114 |
| 1.3.344 | reg : machineconstants_slt_phi1margin_9 | 0x00000000 | 0xA002055C | 114 |
| 1.3.345 | reg : machineconstants_slt_phi1margin_10 | 0x00000000 | 0xA0020560 | 115 |
| 1.3.346 | reg : machineconstants_slt_phi1margin_11 | 0x00000000 | 0xA0020564 | 115 |
| 1.3.347 | reg : machineconstants_slt_phi1margin_12 | 0x00000000 | 0xA0020568 | 115 |

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| 1.3.348 | reg : machineconstants_slt_phi1margin_13 | 0x00000000 | 0xA002056C | 115 |
| 1.3.349 | reg : machineconstants_slt_phi1margin_14 | 0x00000000 | 0xA0020570 | 115 |
| 1.3.350 | reg : machineconstants_slt_phi1margin_15 | 0x00000000 | 0xA0020574 | 115 |
| 1.3.351 | reg : machineconstants_slt_phi1margin_16 | 0x00000000 | 0xA0020578 | 115 |
| 1.3.352 | reg : machineconstants_slt_phi1margin_17 | 0x00000000 | 0xA002057C | 116 |
| 1.3.353 | reg : machineconstants_slt_phi1margin_18 | 0x00000000 | 0xA0020580 | 116 |
| 1.3.354 | reg : machineconstants_slt_phi1margin_19 | 0x00000000 | 0xA0020584 | 116 |
| 1.3.355 | reg : machineconstants_slt_phi0margin | 0x00000000 | 0xA0020588 | 116 |
| 1.3.356 | reg : machineconstants_slt_satrateavg_off | 0x00000000 | 0xA002058C | 116 |
| 1.3.357 | reg : machineconstants_slt_satrateavg_on | 0x00000000 | 0xA0020590 | 116 |
| 1.3.358 | reg : machineconstants_slt_xint3sigma_avg | 0x00000000 | 0xA0020594 | 116 |
| 1.3.359 | reg : machineconstants_slt_presubrate_avg | 0x00000000 | 0xA0020598 | 117 |
| 1.3.360 | reg : machineconstants_slt_opt_sol | 0x00000002 | 0xA002059C | 117 |
| 1.3.361 | reg : machineconstants_slt_bk_sol | 0x00000002 | 0xA00205A0 | 117 |
| 1.3.362 | reg : machineconstants_damp_damp2piezo_gain | 0x00000A3D | 0xA00205A4 | 117 |
| 1.3.363 | reg : machineconstants_damp_waveform_debug_setup_aoch1 | 0x00000000 | 0xA00205A8 | 117 |
| 1.3.364 | reg : machineconstants_damp_waveform_debug_setup_aoch2 | 0x00000000 | 0xA00205AC | 117 |
| 1.3.365 | reg : machineconstants_damp_waveform_debug_setup_aoch3 | 0x00000000 | 0xA00205B0 | 117 |
| 1.3.366 | reg : machineconstants_damp_waveform_debug_setup_aoch4 | 0x00000000 | 0xA00205B4 | 118 |
| 1.3.367 | reg : machineconstants_damp_deltan | 0x00000000 | 0xA00205B8 | 118 |
| 1.3.368 | reg : machineconstants_damp_ditherbits | 0x00000000 | 0xA00205BC | 118 |
| 1.3.369 | reg : machineconstants_cal_bdo_basefreqmin | 0x2A4C2000 | 0xA00205C0 | 118 |
| 1.3.370 | reg : machineconstants_cal_bdo_basefreqnumber | 0x00000003 | 0xA00205C4 | 118 |
| 1.3.371 | reg : machineconstants_cal_bdo_basefreqres | 0x03D86000 | 0xA00205C8 | 118 |
| 1.3.372 | reg : machineconstants_cal_sqrampltf | 0x00001000 | 0xA00205CC | 119 |
| 1.3.373 | reg : machineconstants_cal_mainfreqvec_min | 0x03C8C000 | 0xA00205D0 | 119 |
| 1.3.374 | reg : machineconstants_cal_mainfreqvec_number | 0x00000015 | 0xA00205D4 | 119 |
| 1.3.375 | reg : machineconstants_cal_mainfreqvec_res | 0x00019000 | 0xA00205D8 | 119 |
| 1.3.376 | reg : machineconstants_cal_subfreqmultvec_min | 0x00001C00 | 0xA00205DC | 119 |
| 1.3.377 | reg : machineconstants_cal_subfreqmultvec_number | 0x00000004 | 0xA00205E0 | 119 |
| 1.3.378 | reg : machineconstants_cal_subfreqmultvec_res | 0x00000400 | 0xA00205E4 | 119 |
| 1.3.379 | reg : machineconstants_cal_sineampltfmin | 0x00000066 | 0xA00205E8 | 120 |
| 1.3.380 | reg : machineconstants_cal_sineampltfres | 0x00000066 | 0xA00205EC | 120 |
| 1.3.381 | reg : machineconstants_cal_sineampltfnumber | 0x00000014 | 0xA00205F0 | 120 |

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|---|---|---|---|---|
| 1.3.382 | reg : machineconstants_cal_mainfreqdiag_min | 0x030D4000 | 0xA00205F4 | 120 |
| 1.3.383 | reg : machineconstants_cal_mainfreqdiag_res | 0x00019000 | 0xA00205F8 | 120 |
| 1.3.384 | reg : machineconstants_cal_mainfreqdiag_number | 0x000000C9 | 0xA00205FC | 120 |
| 1.3.385 | reg : machineconstants_cal_bdo_holdoff | 0x0000000A | 0xA0020600 | 120 |
| 1.3.386 | reg : machineconstants_cal_tfm_holdoff | 0x0000000A | 0xA0020604 | 121 |
| 1.3.387 | reg : machineconstants_cal_ddmmainpeakvalthr | 0x00002000 | 0xA0020608 | 121 |
| 1.3.388 | reg : machineconstants_cal_ddmsnrthr | 0x00000500 | 0xA002060C | 121 |
| 1.3.389 | reg : machineconstants_cal_ddmwidththr | 0x000004CD | 0xA0020610 | 121 |
| 1.3.390 | reg : machineconstants_cal_ddmqc_holdoff | 0x00000005 | 0xA0020614 | 121 |
| 1.3.391 | reg : machineconstants_cal_dcmqc_holdoff | 0x00000005 | 0xA0020618 | 121 |
| 1.3.392 | reg : machineconstants_cal_dcmmainpeakvalthr | 0x00002000 | 0xA002061C | 121 |
| 1.3.393 | reg : machineconstants_cal_dcmsnrthr | 0x00000500 | 0xA0020620 | 122 |
| 1.3.394 | reg : machineconstants_cal_dcmwidththr | 0x000004CD | 0xA0020624 | 122 |
| 1.3.395 | reg : machineconstants_cal_dcmcheckiter | 0x00000004 | 0xA0020628 | 122 |
| 1.3.396 | reg : machineconstants_cal_ddmcheckiter | 0x00000004 | 0xA002062C | 122 |
| 1.3.397 | reg : machineconstants_cal_targetcl | 0x0000012C | 0xA0020630 | 122 |
| 1.3.398 | reg : machineconstants_cal_targetsubcl_initial | 0x0000001E | 0xA0020634 | 122 |
| 1.3.399 | reg : machineconstants_cal_targetsubcl_res | 0x00000014 | 0xA0020638 | 122 |
| 1.3.400 | reg : machineconstants_cal_targetsubcl_num | 0x00000002 | 0xA002063C | 123 |
| 1.3.401 | reg : machineconstants_cal_targetscl_optimized | 0x00000022 | 0xA0020640 | 123 |
| 1.3.402 | reg : machineconstants_cal_tferrthr | 0x00008000 | 0xA0020644 | 123 |
| 1.3.403 | reg : machineconstants_cal_totalvoltage | 0x00010400 | 0xA0020648 | 123 |
| 1.3.404 | reg : machineconstants_cal_cost_weight_p0 | 0x00010000 | 0xA002064C | 123 |
| 1.3.405 | reg : machineconstants_cal_cost_weight_p1 | 0x00010000 | 0xA0020650 | 123 |
| 1.3.406 | reg : machineconstants_cal_cost_weight_p2 | 0x00010000 | 0xA0020654 | 123 |
| 1.3.407 | reg : machineconstants_cal_cost_weight_p3 | 0x00010000 | 0xA0020658 | 124 |
| 1.3.408 | reg : machineconstants_cal_cost_weight_p4 | 0x00010000 | 0xA002065C | 124 |
| 1.3.409 | reg : machineconstants_cal_cost_weight_p5 | 0x00010000 | 0xA0020660 | 124 |
| 1.3.410 | reg : machineconstants_cal_costfunctiondswthr | 0x0000CCCD | 0xA0020664 | 124 |
| 1.3.411 | reg : machineconstants_cal_costfunctionhwthr | 0x0000CCCD | 0xA0020668 | 124 |
| 1.3.412 | reg : machineconstants_cal_freqdiagnosticnumber | 0x00000003 | 0xA002066C | 124 |
| 1.3.413 | reg : machineconstants_cal_freqdiagnosticres | 0x00002710 | 0xA0020670 | 124 |
| 1.3.414 | reg : machineconstants_cal_maindropletdiameter | 0x001B4CCD | 0xA0020674 | 125 |
| 1.3.415 | reg : machineconstants_cal_maindropletvelocity | 0x00820000 | 0xA0020678 | 125 |

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| 1.3.416 | reg : machineconstants_cal_satellitediametermindcm | 0x00040000 | 0xA002067C | 125 |
| 1.3.417 | reg : machineconstants_cal_satellitediameterminddm | 0x00060000 | 0xA0020680 | 125 |
| 1.3.418 | reg : machineconstants_cal_dcmlocation | 0x00000046 | 0xA0020684 | 125 |
| 1.3.419 | reg : machineconstants_cal_errorratiothreshold | 0x00008000 | 0xA0020688 | 125 |
| 1.3.420 | reg : machineconstants_cal_bdo_dc_res | 0x0000000A | 0xA002068C | 125 |
| 1.3.421 | reg : machineconstants_cal_dragcte | 0x00000001 | 0xA0020690 | 126 |
| 1.3.422 | reg : machineconstants_cal_num_candidate_soln | 0x00000015 | 0xA0020694 | 126 |
| 1.3.423 | reg : machineconstants_cal_spcfg_4 | 0x00000007 | 0xA0020698 | 126 |
| 1.3.424 | reg : machineconstants_cal_spcfg_5 | 0x00000001 | 0xA002069C | 126 |
| 1.3.425 | reg : machineconstants_cal_spcfg_6 | 0x00000014 | 0xA00206A0 | 126 |
| 1.3.426 | reg : machineconstants_cal_mainfreqopt_type | 0x00000000 | 0xA00206A4 | 126 |
| 1.3.427 | reg : machineconstants_cal_spcfg_8 | 0x00000001 | 0xA00206A8 | 126 |
| 1.3.428 | reg : machineconstants_cal_pkuniformitymax | 0x0000199A | 0xA00206AC | 127 |
| 1.3.429 | reg : machineconstants_cal_spcfg_10 | 0x00000001 | 0xA00206B0 | 127 |
| 1.3.430 | reg : machineconstants_cal_spcfg_11 | 0x0000001E | 0xA00206B4 | 127 |
| 1.3.431 | reg : machineconstants_cal_spcfg_12 | 0x00000000 | 0xA00206B8 | 127 |
| 1.3.432 | reg : machineconstants_cal_jmpbnddelay | 0x00000001 | 0xA00206BC | 127 |
| 1.3.433 | reg : machineconstants_cal_spcfg_14 | 0x00000003 | 0xA00206C0 | 127 |
| 1.3.434 | reg : machineconstants_cal_spcfg_15 | 0x00000000 | 0xA00206C4 | 127 |
| 1.3.435 | reg : machineconstants_cal_spcfg_16 | 0x00000000 | 0xA00206C8 | 127 |
| 1.4 | block : algo_egr_registers_srdl | | 0xA0030000 - 0xA003D07F | 128 |
| 1.4.1 | reg : algo_egress_module_name | 0x6F616C67 | 0xA0030000 | 128 |
| 1.4.2 | reg : algo_egress_module_version | 0x00000000 | 0xA0030004 | 128 |
| 1.4.3 | reg : algo_egress_page_properties | 0x80001001 | 0xA0030008 | 128 |
| 1.4.4 | reg : algo_egress_scratchregister | 0x12345678 | 0xA003000C | 128 |
| 1.4.5 | reg : algo_egress_irq_enable | 0x00000000 | 0xA0030010 | 128 |
| 1.4.6 | reg : algo_egress_irq_pending | 0x00000000 | 0xA0030014 | 128 |
| 1.4.7 | reg : algo_egress_irq_raw | 0x00000000 | 0xA0030018 | 129 |
| 1.4.8 | reg : algo_egress_irq_force | 0x00000000 | 0xA003001C | 129 |
| 1.4.9 | reg : region_1_start_tag | 0x00000000 | 0xA0031000 | 129 |
| 1.4.10 | reg : region_1_dtec_tod_lsbs | 0x00000000 | 0xA0031004 | 129 |
| 1.4.11 | reg : region_1_dtec_tod_msbs | 0x00000000 | 0xA0031008 | 129 |
| 1.4.12 | reg : region_1_dtec_lts | 0x00000000 | 0xA003100C | 129 |
| 1.4.13 | reg : dtec_algo_rev_revision_major | 0x00000000 | 0xA0031010 | 129 |
| 1.4.14 | reg : dtec_algo_rev_revision_minor | 0x00000000 | 0xA0031014 | 130 |
| 1.4.15 | reg : dtec_algo_rev_revision_patch | 0x00000000 | 0xA0031018 | 130 |
| 1.4.16 | reg : spares_spare_uint_1 | 0x00000000 | 0xA003101C | 130 |
| 1.4.17 | reg : spares_spare_uint_2 | 0x00000000 | 0xA0031020 | 130 |

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|---|---|---|---|---|
| 1.4.18 | reg : spares_spare_uint_3 | 0x00000000 | 0xA0031024 | 130 |
| 1.4.19 | reg : spares_spare_uint_4 | 0x00000000 | 0xA0031028 | 130 |
| 1.4.20 | reg : spares_spare_uint_5 | 0x00000000 | 0xA003102C | 130 |
| 1.4.21 | reg : spares_spare_uint_6 | 0x00000000 | 0xA0031030 | 130 |
| 1.4.22 | reg : spares_spare_uint_7 | 0x00000000 | 0xA0031034 | 131 |
| 1.4.23 | reg : spares_spare_uint_8 | 0x00000000 | 0xA0031038 | 131 |
| 1.4.24 | reg : spares_spare_uint_9 | 0x00000000 | 0xA003103C | 131 |
| 1.4.25 | reg : spares_spare_uint_10 | 0x00000000 | 0xA0031040 | 131 |
| 1.4.26 | reg : spares_spare_uint_11 | 0x00000000 | 0xA0031044 | 131 |
| 1.4.27 | reg : spares_spare_uint_12 | 0x00000000 | 0xA0031048 | 131 |
| 1.4.28 | reg : spares_spare_uint_13 | 0x00000000 | 0xA003104C | 131 |
| 1.4.29 | reg : spares_spare_uint_14 | 0x00000000 | 0xA0031050 | 131 |
| 1.4.30 | reg : spares_spare_uint_15 | 0x00000000 | 0xA0031054 | 132 |
| 1.4.31 | reg : spares_spare_uint_16 | 0x00000000 | 0xA0031058 | 132 |
| 1.4.32 | reg : spares_spare_int_1 | 0x00000000 | 0xA003105C | 132 |
| 1.4.33 | reg : spares_spare_int_2 | 0x00000000 | 0xA0031060 | 132 |
| 1.4.34 | reg : spares_spare_int_3 | 0x00000000 | 0xA0031064 | 132 |
| 1.4.35 | reg : spares_spare_int_4 | 0x00000000 | 0xA0031068 | 132 |
| 1.4.36 | reg : spares_spare_int_5 | 0x00000000 | 0xA003106C | 132 |
| 1.4.37 | reg : spares_spare_int_6 | 0x00000000 | 0xA0031070 | 133 |
| 1.4.38 | reg : spares_spare_int_7 | 0x00000000 | 0xA0031074 | 133 |
| 1.4.39 | reg : spares_spare_int_8 | 0x00000000 | 0xA0031078 | 133 |
| 1.4.40 | reg : spares_spare_int_9 | 0x00000000 | 0xA003107C | 133 |
| 1.4.41 | reg : spares_spare_int_10 | 0x00000000 | 0xA0031080 | 133 |
| 1.4.42 | reg : spares_spare_int_11 | 0x00000000 | 0xA0031084 | 133 |
| 1.4.43 | reg : spares_spare_int_12 | 0x00000000 | 0xA0031088 | 133 |
| 1.4.44 | reg : spares_spare_int_13 | 0x00000000 | 0xA003108C | 133 |
| 1.4.45 | reg : spares_spare_int_14 | 0x00000000 | 0xA0031090 | 134 |
| 1.4.46 | reg : spares_spare_int_15 | 0x00000000 | 0xA0031094 | 134 |
| 1.4.47 | reg : spares_spare_int_16 | 0x00000000 | 0xA0031098 | 134 |
| 1.4.48 | reg : spares_spare_ufi_1 | 0x00000000 | 0xA003109C | 134 |
| 1.4.49 | reg : spares_spare_ufi_2 | 0x00000000 | 0xA00310A0 | 134 |
| 1.4.50 | reg : spares_spare_ufi_3 | 0x00000000 | 0xA00310A4 | 134 |
| 1.4.51 | reg : spares_spare_ufi_4 | 0x00000000 | 0xA00310A8 | 134 |
| 1.4.52 | reg : spares_spare_ufi_5 | 0x00000000 | 0xA00310AC | 134 |
| 1.4.53 | reg : spares_spare_ufi_6 | 0x00000000 | 0xA00310B0 | 135 |
| 1.4.54 | reg : spares_spare_ufi_7 | 0x00000000 | 0xA00310B4 | 135 |
| 1.4.55 | reg : spares_spare_ufi_8 | 0x00000000 | 0xA00310B8 | 135 |
| 1.4.56 | reg : spares_spare_ufi_9 | 0x00000000 | 0xA00310BC | 135 |
| 1.4.57 | reg : spares_spare_ufi_10 | 0x00000000 | 0xA00310C0 | 135 |
| 1.4.58 | reg : spares_spare_ufi_11 | 0x00000000 | 0xA00310C4 | 135 |
| 1.4.59 | reg : spares_spare_ufi_12 | 0x00000000 | 0xA00310C8 | 135 |
| 1.4.60 | reg : spares_spare_ufi_13 | 0x00000000 | 0xA00310CC | 136 |
| 1.4.61 | reg : spares_spare_ufi_14 | 0x00000000 | 0xA00310D0 | 136 |
| 1.4.62 | reg : spares_spare_ufi_15 | 0x00000000 | 0xA00310D4 | 136 |
| 1.4.63 | reg : spares_spare_ufi_16 | 0x00000000 | 0xA00310D8 | 136 |
| 1.4.64 | reg : spares_spare_sfi_1 | 0x00000000 | 0xA00310DC | 136 |
| 1.4.65 | reg : spares_spare_sfi_2 | 0x00000000 | 0xA00310E0 | 136 |
| 1.4.66 | reg : spares_spare_sfi_3 | 0x00000000 | 0xA00310E4 | 136 |
| 1.4.67 | reg : spares_spare_sfi_4 | 0x00000000 | 0xA00310E8 | 136 |
| 1.4.68 | reg : spares_spare_sfi_5 | 0x00000000 | 0xA00310EC | 137 |
| 1.4.69 | reg : spares_spare_sfi_6 | 0x00000000 | 0xA00310F0 | 137 |
| 1.4.70 | reg : spares_spare_sfi_7 | 0x00000000 | 0xA00310F4 | 137 |
| 1.4.71 | reg : spares_spare_sfi_8 | 0x00000000 | 0xA00310F8 | 137 |
| 1.4.72 | reg : spares_spare_sfi_9 | 0x00000000 | 0xA00310FC | 137 |
| 1.4.73 | reg : spares_spare_sfi_10 | 0x00000000 | 0xA0031100 | 137 |
| 1.4.74 | reg : spares_spare_sfi_11 | 0x00000000 | 0xA0031104 | 137 |
| 1.4.75 | reg : spares_spare_sfi_12 | 0x00000000 | 0xA0031108 | 137 |
| 1.4.76 | reg : spares_spare_sfi_13 | 0x00000000 | 0xA003110C | 138 |
| 1.4.77 | reg : spares_spare_sfi_14 | 0x00000000 | 0xA0031110 | 138 |
| 1.4.78 | reg : spares_spare_sfi_15 | 0x00000000 | 0xA0031114 | 138 |
| 1.4.79 | reg : spares_spare_sfi_16 | 0x00000000 | 0xA0031118 | 138 |
| 1.4.80 | reg : region_1_end_tag | 0x00000000 | 0xA003111C | 138 |
| 1.4.81 | reg : region_4_start_tag | 0x00000000 | 0xA0034000 | 138 |
| 1.4.82 | reg : region_4_dtec_tod_lsbs | 0x00000000 | 0xA0034004 | 138 |
| 1.4.83 | reg : region_4_dtec_tod_msbs | 0x00000000 | 0xA0034008 | 139 |

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|---|---|---|---|---|
| 1.4.84 | reg : region_4_dtec_lts | 0x00000000 | 0xA003400C | 139 |
| 1.4.85 | reg : dcm_fb_metrics_fb_lm | 0x00000000 | 0xA0034010 | 139 |
| 1.4.86 | reg : dcm_fb_metrics_fb_tm | 0x00000000 | 0xA0034014 | 139 |
| 1.4.87 | reg : dcm_fb_metrics_fb_cm | 0x00000000 | 0xA0034018 | 139 |
| 1.4.88 | reg : dcm_fb_metrics_fb_dm | 0x00000000 | 0xA003401C | 139 |
| 1.4.89 | reg : dcm_fb_metrics_sigmal | 0x00000000 | 0xA0034020 | 139 |
| 1.4.90 | reg : dcm_fb_metrics_sigmat | 0x00000000 | 0xA0034024 | 139 |
| 1.4.91 | reg : dcm_fb_metrics_sigmac | 0x00000000 | 0xA0034028 | 140 |
| 1.4.92 | reg : dcm_fb_metrics_sigmad | 0x00000000 | 0xA003402C | 140 |
| 1.4.93 | reg : dcm_fb_metrics_maindropletnumber | 0x00000000 | 0xA0034030 | 140 |
| 1.4.94 | reg : dcm_fb_metrics_presubnumber | 0x00000000 | 0xA0034034 | 140 |
| 1.4.95 | reg : dcm_fb_metrics_multpresubnumber | 0x00000000 | 0xA0034038 | 140 |
| 1.4.96 | reg : dcm_fb_metrics_leftpeakmissednumber | 0x00000000 | 0xA003403C | 140 |
| 1.4.97 | reg : dcm_fb_metrics_rightpeakmissednumber | 0x00000000 | 0xA0034040 | 140 |
| 1.4.98 | reg : dcm_fb_metrics_timestamp_tod_lsb | 0x00000000 | 0xA0034044 | 141 |
| 1.4.99 | reg : dcm_fb_metrics_timestamp_tod_msb | 0x00000000 | 0xA0034048 | 141 |
| 1.4.100 | reg : dcm_fb_metrics_timestamp_lts | 0x00000000 | 0xA003404C | 141 |
| 1.4.101 | reg : region_4_end_tag | 0x00000000 | 0xA0034050 | 141 |
| 1.4.102 | reg : region_5_start_tag | 0x00000000 | 0xA0035000 | 141 |
| 1.4.103 | reg : region_5_dtec_tod_lsbs | 0x00000000 | 0xA0035004 | 141 |
| 1.4.104 | reg : region_5_dtec_tod_msbs | 0x00000000 | 0xA0035008 | 141 |
| 1.4.105 | reg : region_5_dtec_lts | 0x00000000 | 0xA003500C | 141 |
| 1.4.106 | reg : ddm_fb_metrics_maindropletnumber | 0x00000000 | 0xA0035010 | 142 |
| 1.4.107 | reg : ddm_fb_metrics_satelliterate | 0x00000000 | 0xA0035014 | 142 |
| 1.4.108 | reg : ddm_fb_metrics_xint3sigma | 0x00000000 | 0xA0035018 | 142 |
| 1.4.109 | reg : ddm_fb_metrics_xintmean | 0x00000000 | 0xA003501C | 142 |
| 1.4.110 | reg : ddm_fb_metrics_mainpeak | 0x00000000 | 0xA0035020 | 142 |
| 1.4.111 | reg : ddm_fb_metrics_pf_exposuredc | 0x00000000 | 0xA0035024 | 142 |
| 1.4.112 | reg : ddm_fb_metrics_signalquality | 0x00000000 | 0xA0035028 | 142 |
| 1.4.113 | reg : ddm_fb_metrics_timestamp_tod_lsb | 0x00000000 | 0xA003502C | 143 |
| 1.4.114 | reg : ddm_fb_metrics_timestamp_tod_msb | 0x00000000 | 0xA0035030 | 143 |
| 1.4.115 | reg : ddm_fb_metrics_timestamp_lts | 0x00000000 | 0xA0035034 | 143 |
| 1.4.116 | reg : region_5_end_tag | 0x00000000 | 0xA0035038 | 143 |
| 1.4.117 | reg : region_6_start_tag | 0x00000000 | 0xA0036000 | 143 |
| 1.4.118 | reg : region_6_dtec_tod_lsbs | 0x00000000 | 0xA0036004 | 143 |
| 1.4.119 | reg : region_6_dtec_tod_msbs | 0x00000000 | 0xA0036008 | 143 |
| 1.4.120 | reg : region_6_dtec_lts | 0x00000000 | 0xA003600C | 143 |
| 1.4.121 | reg : damp_waveformparamspkg_damp_signals_1 | 0x00000000 | 0xA0036010 | 144 |
| 1.4.122 | reg : damp_waveformparamspkg_damp_signals_2 | 0x00000000 | 0xA0036014 | 144 |
| 1.4.123 | reg : damp_waveformparamspkg_damp_signals_3 | 0x00000000 | 0xA0036018 | 144 |
| 1.4.124 | reg : damp_waveformparamspkg_damp_signals_4 | 0x00000000 | 0xA003601C | 144 |

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|---|---|---|---|---|
| 1.4.125 | reg : damp_waveformparamspkg _damp_signals_5 | 0x00000000 | 0xA0036020 | 144 |
| 1.4.126 | reg : damp_waveformparamspkg _damp_signals_6 | 0x00000000 | 0xA0036024 | 144 |
| 1.4.127 | reg : damp_waveformparamspkg _damp_signals_7 | 0x00000000 | 0xA0036028 | 144 |
| 1.4.128 | reg : damp_waveformparamspkg _damp_signals_8 | 0x00000000 | 0xA003602C | 145 |
| 1.4.129 | reg : damp_waveformparamspkg _damp_signals_9 | 0x00000000 | 0xA0036030 | 145 |
| 1.4.130 | reg : damp_waveformparamspkg _damp_signals_10 | 0x00000000 | 0xA0036034 | 145 |
| 1.4.131 | reg : damp_waveformparamspkg _damp_signals_11 | 0x00000000 | 0xA0036038 | 145 |
| 1.4.132 | reg : damp_waveformparamspkg _damp_signals_12 | 0x00000000 | 0xA003603C | 145 |
| 1.4.133 | reg : damp_waveformparamspkg _damp_signals_13 | 0x00000000 | 0xA0036040 | 145 |
| 1.4.134 | reg : damp_waveformparamspkg _damp_signals_14 | 0x00000000 | 0xA0036044 | 146 |
| 1.4.135 | reg : damp_waveformparamspkg _damp_signals_15 | 0x00000000 | 0xA0036048 | 146 |
| 1.4.136 | reg : damp_waveformparamspkg _damp_signals_16 | 0x00000000 | 0xA003604C | 146 |
| 1.4.137 | reg : damp_waveformparamspkg _damp_signals_17 | 0x00000000 | 0xA0036050 | 146 |
| 1.4.138 | reg : damp_waveformparamspkg _damp_signals_18 | 0x00000000 | 0xA0036054 | 146 |
| 1.4.139 | reg : damp_waveformparamspkg _damp_signals_19 | 0x00000000 | 0xA0036058 | 146 |
| 1.4.140 | reg : damp_waveformparamspkg _damp_signals_20 | 0x00000000 | 0xA003605C | 146 |
| 1.4.141 | reg : damp_waveformparamspkg _damp_signals_21 | 0x00000000 | 0xA0036060 | 147 |
| 1.4.142 | reg : damp_waveformparamspkg _damp_signals_22 | 0x00000000 | 0xA0036064 | 147 |
| 1.4.143 | reg : damp_waveformparamspkg _damp_signals_23 | 0x00000000 | 0xA0036068 | 147 |
| 1.4.144 | reg : damp_waveformparamspkg _damp_signals_24 | 0x00000000 | 0xA003606C | 147 |
| 1.4.145 | reg : damp_waveformparamspkg _damp_signals_25 | 0x00000000 | 0xA0036070 | 147 |
| 1.4.146 | reg : damp_waveformparamspkg _damp_signals_26 | 0x00000000 | 0xA0036074 | 147 |
| 1.4.147 | reg : damp_waveformparamspkg _damp_signals_27 | 0x00000000 | 0xA0036078 | 147 |

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|---|---|---|---|---|
| 1.4.148 | reg : damp_waveformparamspkg_damp_signals_28 | 0x00000000 | 0xA003607C | 148 |
| 1.4.149 | reg : damp_waveformparamspkg_damp_signals_29 | 0x00000000 | 0xA0036080 | 148 |
| 1.4.150 | reg : damp_waveformparamspkg_damp_signals_30 | 0x00000000 | 0xA0036084 | 148 |
| 1.4.151 | reg : damp_waveformparamspkg_damp_signals_31 | 0x00000000 | 0xA0036088 | 148 |
| 1.4.152 | reg : damp_waveformparamspkg_damp_signals_32 | 0x00000000 | 0xA003608C | 148 |
| 1.4.153 | reg : damp_waveformparamspkg_damp_signals_33 | 0x00000000 | 0xA0036090 | 148 |
| 1.4.154 | reg : damp_waveformparamspkg_damp_signals_34 | 0x00000000 | 0xA0036094 | 148 |
| 1.4.155 | reg : damp_waveformparamspkg_damp_signals_35 | 0x00000000 | 0xA0036098 | 149 |
| 1.4.156 | reg : damp_waveformparamspkg_damp_signals_36 | 0x00000000 | 0xA003609C | 149 |
| 1.4.157 | reg : damp_waveformparamspkg_damp_signals_37 | 0x00000000 | 0xA00360A0 | 149 |
| 1.4.158 | reg : damp_waveformparamspkg_damp_signals_38 | 0x00000000 | 0xA00360A4 | 149 |
| 1.4.159 | reg : damp_waveformparamspkg_damp_signals_39 | 0x00000000 | 0xA00360A8 | 149 |
| 1.4.160 | reg : damp_waveformparamspkg_damp_signals_40 | 0x00000000 | 0xA00360AC | 149 |
| 1.4.161 | reg : damp_waveformparamspkg_damp_signals_41 | 0x00000000 | 0xA00360B0 | 149 |
| 1.4.162 | reg : damp_waveformparamspkg_damp_signals_42 | 0x00000000 | 0xA00360B4 | 150 |
| 1.4.163 | reg : damp_waveformparamspkg_damp_signals_43 | 0x00000000 | 0xA00360B8 | 150 |
| 1.4.164 | reg : damp_waveformparamspkg_damp_signals_44 | 0x00000000 | 0xA00360BC | 150 |
| 1.4.165 | reg : damp_waveformparamspkg_damp_signals_45 | 0x00000000 | 0xA00360C0 | 150 |
| 1.4.166 | reg : damp_waveformparamspkg_damp_signals_46 | 0x00000000 | 0xA00360C4 | 150 |
| 1.4.167 | reg : damp_waveformparamspkg_damp_signals_47 | 0x00000000 | 0xA00360C8 | 150 |
| 1.4.168 | reg : damp_waveformparamspkg_damp_signals_48 | 0x00000000 | 0xA00360CC | 150 |
| 1.4.169 | reg : damp_waveformparamspkg_damp_signals_49 | 0x00000000 | 0xA00360D0 | 151 |
| 1.4.170 | reg : damp_waveformparamspkg_damp_signals_50 | 0x00000000 | 0xA00360D4 | 151 |

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|---|---|---|---|---|
| 1.4.171 | reg : damp_waveformparamspkg _damp_signals_51 | 0x00000000 | 0xA00360D8 | 151 |
| 1.4.172 | reg : damp_waveformparamspkg _damp_signals_52 | 0x00000000 | 0xA00360DC | 151 |
| 1.4.173 | reg : damp_waveformparamspkg _damp_signals_53 | 0x00000000 | 0xA00360E0 | 151 |
| 1.4.174 | reg : damp_waveformparamspkg _damp_signals_54 | 0x00000000 | 0xA00360E4 | 151 |
| 1.4.175 | reg : damp_waveformparamspkg _damp_signals_55 | 0x00000000 | 0xA00360E8 | 151 |
| 1.4.176 | reg : damp_waveformparamspkg _damp_signals_56 | 0x00000000 | 0xA00360EC | 152 |
| 1.4.177 | reg : damp_waveformparamspkg _damp_signals_57 | 0x00000000 | 0xA00360F0 | 152 |
| 1.4.178 | reg : damp_waveformparamspkg _damp_signals_58 | 0x00000000 | 0xA00360F4 | 152 |
| 1.4.179 | reg : damp_waveformparamspkg _damp_signals_59 | 0x00000000 | 0xA00360F8 | 152 |
| 1.4.180 | reg : damp_waveformparamspkg _damp_signals_60 | 0x00000000 | 0xA00360FC | 152 |
| 1.4.181 | reg : damp_waveformparamspkg _damp_signals_61 | 0x00000000 | 0xA0036100 | 152 |
| 1.4.182 | reg : damp_waveformparamspkg _damp_signals_62 | 0x00000000 | 0xA0036104 | 153 |
| 1.4.183 | reg : damp_waveformparamspkg _damp_signals_63 | 0x00000000 | 0xA0036108 | 153 |
| 1.4.184 | reg : damp_waveformparamspkg _damp_signals_64 | 0x00000000 | 0xA003610C | 153 |
| 1.4.185 | reg : damp_waveformparamspkg _damp_signals_65 | 0x00000000 | 0xA0036110 | 153 |
| 1.4.186 | reg : damp_waveformparamspkg _damp_signals_66 | 0x00000000 | 0xA0036114 | 153 |
| 1.4.187 | reg : damp_waveformparamspkg _damp_signals_67 | 0x00000000 | 0xA0036118 | 153 |
| 1.4.188 | reg : damp_waveformparamspkg _damp_signals_68 | 0x00000000 | 0xA003611C | 153 |
| 1.4.189 | reg : damp_waveformparamspkg _damp_signals_69 | 0x00000000 | 0xA0036120 | 154 |
| 1.4.190 | reg : damp_waveformparamspkg _damp_signals_70 | 0x00000000 | 0xA0036124 | 154 |
| 1.4.191 | reg : damp_waveformparamspkg _damp_signals_71 | 0x00000000 | 0xA0036128 | 154 |
| 1.4.192 | reg : damp_waveformparamspkg _damp_signals_72 | 0x00000000 | 0xA003612C | 154 |
| 1.4.193 | reg : damp_waveformparamspkg _damp_signals_73 | 0x00000000 | 0xA0036130 | 154 |

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|---|---|---|---|---|
| 1.4.194 | reg : damp_waveformparamspkg_damp_signals_74 | 0x00000000 | 0xA0036134 | 154 |
| 1.4.195 | reg : damp_waveformparamspkg_damp_signals_75 | 0x00000000 | 0xA0036138 | 154 |
| 1.4.196 | reg : damp_waveformparamspkg_damp_signals_76 | 0x00000000 | 0xA003613C | 155 |
| 1.4.197 | reg : damp_waveformparamspkg_damp_signals_77 | 0x00000000 | 0xA0036140 | 155 |
| 1.4.198 | reg : damp_waveformparamspkg_damp_signals_78 | 0x00000000 | 0xA0036144 | 155 |
| 1.4.199 | reg : damp_waveformparamspkg_damp_signals_79 | 0x00000000 | 0xA0036148 | 155 |
| 1.4.200 | reg : damp_waveformparamspkg_damp_signals_80 | 0x00000000 | 0xA003614C | 155 |
| 1.4.201 | reg : damp_waveformparamspkg_damp_signals_81 | 0x00000000 | 0xA0036150 | 155 |
| 1.4.202 | reg : damp_waveformparamspkg_damp_signals_82 | 0x00000000 | 0xA0036154 | 155 |
| 1.4.203 | reg : damp_waveformparamspkg_damp_signals_83 | 0x00000000 | 0xA0036158 | 156 |
| 1.4.204 | reg : damp_waveformparamspkg_damp_signals_84 | 0x00000000 | 0xA003615C | 156 |
| 1.4.205 | reg : damp_waveformparamspkg_damp_signals_85 | 0x00000000 | 0xA0036160 | 156 |
| 1.4.206 | reg : damp_waveformparamspkg_damp_signals_86 | 0x00000000 | 0xA0036164 | 156 |
| 1.4.207 | reg : damp_waveformparamspkg_damp_signals_87 | 0x00000000 | 0xA0036168 | 156 |
| 1.4.208 | reg : damp_waveformparamspkg_damp_signals_88 | 0x00000000 | 0xA003616C | 156 |
| 1.4.209 | reg : damp_waveformparamspkg_damp_signals_89 | 0x00000000 | 0xA0036170 | 156 |
| 1.4.210 | reg : damp_waveformparamspkg_damp_signals_90 | 0x00000000 | 0xA0036174 | 157 |
| 1.4.211 | reg : damp_waveformparamspkg_damp_signals_91 | 0x00000000 | 0xA0036178 | 157 |
| 1.4.212 | reg : damp_waveformparamspkg_damp_signals_92 | 0x00000000 | 0xA003617C | 157 |
| 1.4.213 | reg : damp_waveformparamspkg_damp_signals_93 | 0x00000000 | 0xA0036180 | 157 |
| 1.4.214 | reg : damp_waveformparamspkg_damp_signals_94 | 0x00000000 | 0xA0036184 | 157 |
| 1.4.215 | reg : damp_waveformparamspkg_damp_signals_95 | 0x00000000 | 0xA0036188 | 157 |
| 1.4.216 | reg : damp_waveformparamspkg_damp_signals_96 | 0x00000000 | 0xA003618C | 157 |

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|---|---|---|---|---|
| 1.4.217 | reg : damp_waveformparamspkg _damp_signals_97 | 0x00000000 | 0xA0036190 | 158 |
| 1.4.218 | reg : damp_waveformparamspkg _damp_signals_98 | 0x00000000 | 0xA0036194 | 158 |
| 1.4.219 | reg : damp_waveformparamspkg _damp_signals_99 | 0x00000000 | 0xA0036198 | 158 |
| 1.4.220 | reg : damp_waveformparamspkg _damp_signals_100 | 0x00000000 | 0xA003619C | 158 |
| 1.4.221 | reg : damp_waveformparamspkg _damp_signals_101 | 0x00000000 | 0xA00361A0 | 158 |
| 1.4.222 | reg : damp_waveformparamspkg _damp_signals_102 | 0x00000000 | 0xA00361A4 | 158 |
| 1.4.223 | reg : damp_waveformparamspkg _damp_signals_103 | 0x00000000 | 0xA00361A8 | 158 |
| 1.4.224 | reg : damp_waveformparamspkg _damp_signals_104 | 0x00000000 | 0xA00361AC | 159 |
| 1.4.225 | reg : damp_waveformparamspkg _damp_signals_105 | 0x00000000 | 0xA00361B0 | 159 |
| 1.4.226 | reg : damp_waveformparamspkg _damp_signals_106 | 0x00000000 | 0xA00361B4 | 159 |
| 1.4.227 | reg : damp_waveformparamspkg _damp_signals_107 | 0x00000000 | 0xA00361B8 | 159 |
| 1.4.228 | reg : damp_waveformparamspkg _damp_signals_108 | 0x00000000 | 0xA00361BC | 159 |
| 1.4.229 | reg : damp_waveformparamspkg _damp_signals_109 | 0x00000000 | 0xA00361C0 | 159 |
| 1.4.230 | reg : damp_waveformparamspkg _damp_signals_110 | 0x00000000 | 0xA00361C4 | 160 |
| 1.4.231 | reg : damp_waveformparamspkg _damp_signals_111 | 0x00000000 | 0xA00361C8 | 160 |
| 1.4.232 | reg : damp_waveformparamspkg _damp_signals_112 | 0x00000000 | 0xA00361CC | 160 |
| 1.4.233 | reg : damp_waveformparamspkg _damp_signals_113 | 0x00000000 | 0xA00361D0 | 160 |
| 1.4.234 | reg : damp_waveformparamspkg _damp_signals_114 | 0x00000000 | 0xA00361D4 | 160 |
| 1.4.235 | reg : damp_waveformparamspkg _damp_signals_115 | 0x00000000 | 0xA00361D8 | 160 |
| 1.4.236 | reg : damp_waveformparamspkg _damp_signals_116 | 0x00000000 | 0xA00361DC | 160 |
| 1.4.237 | reg : damp_waveformparamspkg _damp_signals_117 | 0x00000000 | 0xA00361E0 | 161 |
| 1.4.238 | reg : damp_waveformparamspkg _damp_signals_118 | 0x00000000 | 0xA00361E4 | 161 |
| 1.4.239 | reg : damp_waveformparamspkg _damp_signals_119 | 0x00000000 | 0xA00361E8 | 161 |

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|---|---|---|---|---|
| 1.4.240 | reg : damp_waveformparamspkg_damp_signals_120 | 0x00000000 | 0xA00361EC | 161 |
| 1.4.241 | reg : damp_waveformparamspkg_damp_signals_121 | 0x00000000 | 0xA00361F0 | 161 |
| 1.4.242 | reg : damp_waveformparamspkg_damp_signals_122 | 0x00000000 | 0xA00361F4 | 161 |
| 1.4.243 | reg : damp_waveformparamspkg_damp_signals_123 | 0x00000000 | 0xA00361F8 | 161 |
| 1.4.244 | reg : damp_waveformparamspkg_damp_signals_124 | 0x00000000 | 0xA00361FC | 162 |
| 1.4.245 | reg : damp_waveformparamspkg_damp_signals_125 | 0x00000000 | 0xA0036200 | 162 |
| 1.4.246 | reg : damp_waveformparamspkg_damp_signals_126 | 0x00000000 | 0xA0036204 | 162 |
| 1.4.247 | reg : damp_waveformparamspkg_damp_signals_127 | 0x00000000 | 0xA0036208 | 162 |
| 1.4.248 | reg : damp_waveformparamspkg_damp_signals_128 | 0x00000000 | 0xA003620C | 162 |
| 1.4.249 | reg : region_6_end_tag | 0x00000000 | 0xA0036210 | 162 |
| 1.4.250 | reg : region_7_start_tag | 0x00000000 | 0xA0037000 | 162 |
| 1.4.251 | reg : region_7_dtec_tod_lsbs | 0x00000000 | 0xA0037004 | 163 |
| 1.4.252 | reg : region_7_dtec_tod_msbs | 0x00000000 | 0xA0037008 | 163 |
| 1.4.253 | reg : region_7_dtec_lts | 0x00000000 | 0xA003700C | 163 |
| 1.4.254 | reg : solutiontable_out_solutiontype | 0x00000000 | 0xA0037010 | 163 |
| 1.4.255 | reg : solutiontable_out_hyperparameters_1 | 0x00000000 | 0xA0037014 | 163 |
| 1.4.256 | reg : solutiontable_out_hyperparameters_2 | 0x00000000 | 0xA0037018 | 163 |
| 1.4.257 | reg : solutiontable_out_hyperparameters_3 | 0x00000000 | 0xA003701C | 164 |
| 1.4.258 | reg : solutiontable_out_hyperparameters_4 | 0x00000000 | 0xA0037020 | 164 |
| 1.4.259 | reg : solutiontable_out_sineamps_1 | 0x00000000 | 0xA0037024 | 164 |
| 1.4.260 | reg : solutiontable_out_sineamps_2 | 0x00000000 | 0xA0037028 | 164 |
| 1.4.261 | reg : solutiontable_out_phi0_1 | 0x00000000 | 0xA003702C | 164 |
| 1.4.262 | reg : solutiontable_out_phi0_2 | 0x00000000 | 0xA0037030 | 164 |
| 1.4.263 | reg : solutiontable_out_phi0_3 | 0x00000000 | 0xA0037034 | 165 |
| 1.4.264 | reg : solutiontable_out_phi0_4 | 0x00000000 | 0xA0037038 | 165 |
| 1.4.265 | reg : solutiontable_out_phi0_5 | 0x00000000 | 0xA003703C | 165 |
| 1.4.266 | reg : solutiontable_out_phi0_6 | 0x00000000 | 0xA0037040 | 165 |
| 1.4.267 | reg : solutiontable_out_phi0_7 | 0x00000000 | 0xA0037044 | 165 |
| 1.4.268 | reg : solutiontable_out_phi0_8 | 0x00000000 | 0xA0037048 | 165 |
| 1.4.269 | reg : solutiontable_out_phi0_9 | 0x00000000 | 0xA003704C | 165 |
| 1.4.270 | reg : solutiontable_out_phi0_10 | 0x00000000 | 0xA0037050 | 166 |
| 1.4.271 | reg : solutiontable_out_phi0_11 | 0x00000000 | 0xA0037054 | 166 |

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| 1.4.272 | reg : solutiontable_out_phi0_12 | 0x00000000 | 0xA0037058 | 166 |
| 1.4.273 | reg : solutiontable_out_phi0_13 | 0x00000000 | 0xA003705C | 166 |
| 1.4.274 | reg : solutiontable_out_phi0_14 | 0x00000000 | 0xA0037060 | 166 |
| 1.4.275 | reg : solutiontable_out_phi0_15 | 0x00000000 | 0xA0037064 | 166 |
| 1.4.276 | reg : solutiontable_out_phi0_16 | 0x00000000 | 0xA0037068 | 166 |
| 1.4.277 | reg : solutiontable_out_phi0_17 | 0x00000000 | 0xA003706C | 166 |
| 1.4.278 | reg : solutiontable_out_phi0_18 | 0x00000000 | 0xA0037070 | 167 |
| 1.4.279 | reg : solutiontable_out_phi0_19 | 0x00000000 | 0xA0037074 | 167 |
| 1.4.280 | reg : solutiontable_out_phi1_1 | 0x00000000 | 0xA0037078 | 167 |
| 1.4.281 | reg : solutiontable_out_phi1_2 | 0x00000000 | 0xA003707C | 167 |
| 1.4.282 | reg : solutiontable_out_phi1_3 | 0x00000000 | 0xA0037080 | 167 |
| 1.4.283 | reg : solutiontable_out_phi1_4 | 0x00000000 | 0xA0037084 | 167 |
| 1.4.284 | reg : solutiontable_out_phi1_5 | 0x00000000 | 0xA0037088 | 167 |
| 1.4.285 | reg : solutiontable_out_phi1_6 | 0x00000000 | 0xA003708C | 168 |
| 1.4.286 | reg : solutiontable_out_phi1_7 | 0x00000000 | 0xA0037090 | 168 |
| 1.4.287 | reg : solutiontable_out_phi1_8 | 0x00000000 | 0xA0037094 | 168 |
| 1.4.288 | reg : solutiontable_out_phi1_9 | 0x00000000 | 0xA0037098 | 168 |
| 1.4.289 | reg : solutiontable_out_phi1_10 | 0x00000000 | 0xA003709C | 168 |
| 1.4.290 | reg : solutiontable_out_phi1_11 | 0x00000000 | 0xA00370A0 | 168 |
| 1.4.291 | reg : solutiontable_out_phi1_12 | 0x00000000 | 0xA00370A4 | 169 |
| 1.4.292 | reg : solutiontable_out_phi1_13 | 0x00000000 | 0xA00370A8 | 169 |
| 1.4.293 | reg : solutiontable_out_phi1_14 | 0x00000000 | 0xA00370AC | 169 |
| 1.4.294 | reg : solutiontable_out_phi1_15 | 0x00000000 | 0xA00370B0 | 169 |
| 1.4.295 | reg : solutiontable_out_phi1_16 | 0x00000000 | 0xA00370B4 | 169 |
| 1.4.296 | reg : solutiontable_out_phi1_17 | 0x00000000 | 0xA00370B8 | 169 |
| 1.4.297 | reg : solutiontable_out_phi1_18 | 0x00000000 | 0xA00370BC | 170 |
| 1.4.298 | reg : solutiontable_out_phi1_19 | 0x00000000 | 0xA00370C0 | 170 |
| 1.4.299 | reg : solutiontable_out_prescoal_flag_1 | 0x00000000 | 0xA00370C4 | 170 |
| 1.4.300 | reg : solutiontable_out_prescoal_flag_2 | 0x00000000 | 0xA00370C8 | 170 |
| 1.4.301 | reg : solutiontable_out_prescoal_flag_3 | 0x00000000 | 0xA00370CC | 170 |
| 1.4.302 | reg : solutiontable_out_prescoal_flag_4 | 0x00000000 | 0xA00370D0 | 170 |
| 1.4.303 | reg : solutiontable_out_prescoal_flag_5 | 0x00000000 | 0xA00370D4 | 171 |
| 1.4.304 | reg : solutiontable_out_prescoal_flag_6 | 0x00000000 | 0xA00370D8 | 171 |
| 1.4.305 | reg : solutiontable_out_prescoal_flag_7 | 0x00000000 | 0xA00370DC | 171 |

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| 1.4.306 | reg : solutiontable_out_prescubcoal_flag_8 | 0x00000000 | 0xA00370E0 | 171 |
| 1.4.307 | reg : solutiontable_out_prescubcoal_flag_9 | 0x00000000 | 0xA00370E4 | 171 |
| 1.4.308 | reg : solutiontable_out_prescubcoal_flag_10 | 0x00000000 | 0xA00370E8 | 171 |
| 1.4.309 | reg : solutiontable_out_prescubcoal_flag_11 | 0x00000000 | 0xA00370EC | 172 |
| 1.4.310 | reg : solutiontable_out_prescubcoal_flag_12 | 0x00000000 | 0xA00370F0 | 172 |
| 1.4.311 | reg : solutiontable_out_prescubcoal_flag_13 | 0x00000000 | 0xA00370F4 | 172 |
| 1.4.312 | reg : solutiontable_out_prescubcoal_flag_14 | 0x00000000 | 0xA00370F8 | 172 |
| 1.4.313 | reg : solutiontable_out_prescubcoal_flag_15 | 0x00000000 | 0xA00370FC | 172 |
| 1.4.314 | reg : solutiontable_out_prescubcoal_flag_16 | 0x00000000 | 0xA0037100 | 172 |
| 1.4.315 | reg : solutiontable_out_prescubcoal_flag_17 | 0x00000000 | 0xA0037104 | 173 |
| 1.4.316 | reg : solutiontable_out_prescubcoal_flag_18 | 0x00000000 | 0xA0037108 | 173 |
| 1.4.317 | reg : solutiontable_out_prescubcoal_flag_19 | 0x00000000 | 0xA003710C | 173 |
| 1.4.318 | reg : solutiontable_out_jitter_1 | 0x00000000 | 0xA0037110 | 173 |
| 1.4.319 | reg : solutiontable_out_jitter_2 | 0x00000000 | 0xA0037114 | 173 |
| 1.4.320 | reg : solutiontable_out_jitter_3 | 0x00000000 | 0xA0037118 | 174 |
| 1.4.321 | reg : solutiontable_out_jitter_4 | 0x00000000 | 0xA003711C | 174 |
| 1.4.322 | reg : solutiontable_out_jitter_5 | 0x00000000 | 0xA0037120 | 174 |
| 1.4.323 | reg : solutiontable_out_jitter_6 | 0x00000000 | 0xA0037124 | 174 |
| 1.4.324 | reg : solutiontable_out_jitter_7 | 0x00000000 | 0xA0037128 | 175 |
| 1.4.325 | reg : solutiontable_out_jitter_8 | 0x00000000 | 0xA003712C | 175 |
| 1.4.326 | reg : solutiontable_out_jitter_9 | 0x00000000 | 0xA0037130 | 175 |
| 1.4.327 | reg : solutiontable_out_jitter_10 | 0x00000000 | 0xA0037134 | 175 |
| 1.4.328 | reg : solutiontable_out_jitter_11 | 0x00000000 | 0xA0037138 | 176 |
| 1.4.329 | reg : solutiontable_out_jitter_12 | 0x00000000 | 0xA003713C | 176 |
| 1.4.330 | reg : solutiontable_out_jitter_13 | 0x00000000 | 0xA0037140 | 176 |
| 1.4.331 | reg : solutiontable_out_jitter_14 | 0x00000000 | 0xA0037144 | 176 |
| 1.4.332 | reg : solutiontable_out_jitter_15 | 0x00000000 | 0xA0037148 | 177 |
| 1.4.333 | reg : solutiontable_out_jitter_16 | 0x00000000 | 0xA003714C | 177 |
| 1.4.334 | reg : solutiontable_out_jitter_17 | 0x00000000 | 0xA0037150 | 177 |
| 1.4.335 | reg : solutiontable_out_jitter_18 | 0x00000000 | 0xA0037154 | 177 |
| 1.4.336 | reg : solutiontable_out_jitter_19 | 0x00000000 | 0xA0037158 | 178 |
| 1.4.337 | reg : solutiontable_out_multpresubrate_1 | 0x00000000 | 0xA003715C | 178 |
| 1.4.338 | reg : solutiontable_out_multpresubrate_2 | 0x00000000 | 0xA0037160 | 178 |
| 1.4.339 | reg : solutiontable_out_multpresubrate_3 | 0x00000000 | 0xA0037164 | 178 |

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| 1.4.340 | reg : solutiontable_out_mult presubrate_4 | 0x00000000 | 0xA0037168 | 178 |
| 1.4.341 | reg : solutiontable_out_mult presubrate_5 | 0x00000000 | 0xA003716C | 178 |
| 1.4.342 | reg : solutiontable_out_mult presubrate_6 | 0x00000000 | 0xA0037170 | 179 |
| 1.4.343 | reg : solutiontable_out_mult presubrate_7 | 0x00000000 | 0xA0037174 | 179 |
| 1.4.344 | reg : solutiontable_out_mult presubrate_8 | 0x00000000 | 0xA0037178 | 179 |
| 1.4.345 | reg : solutiontable_out_mult presubrate_9 | 0x00000000 | 0xA003717C | 179 |
| 1.4.346 | reg : solutiontable_out_mult presubrate_10 | 0x00000000 | 0xA0037180 | 179 |
| 1.4.347 | reg : solutiontable_out_mult presubrate_11 | 0x00000000 | 0xA0037184 | 179 |
| 1.4.348 | reg : solutiontable_out_mult presubrate_12 | 0x00000000 | 0xA0037188 | 179 |
| 1.4.349 | reg : solutiontable_out_mult presubrate_13 | 0x00000000 | 0xA003718C | 180 |
| 1.4.350 | reg : solutiontable_out_mult presubrate_14 | 0x00000000 | 0xA0037190 | 180 |
| 1.4.351 | reg : solutiontable_out_mult presubrate_15 | 0x00000000 | 0xA0037194 | 180 |
| 1.4.352 | reg : solutiontable_out_mult presubrate_16 | 0x00000000 | 0xA0037198 | 180 |
| 1.4.353 | reg : solutiontable_out_mult presubrate_17 | 0x00000000 | 0xA003719C | 180 |
| 1.4.354 | reg : solutiontable_out_mult presubrate_18 | 0x00000000 | 0xA00371A0 | 180 |
| 1.4.355 | reg : solutiontable_out_mult presubrate_19 | 0x00000000 | 0xA00371A4 | 180 |
| 1.4.356 | reg : solutiontable_out_pres ubrate_1 | 0x00000000 | 0xA00371A8 | 181 |
| 1.4.357 | reg : solutiontable_out_pres ubrate_2 | 0x00000000 | 0xA00371AC | 181 |
| 1.4.358 | reg : solutiontable_out_pres ubrate_3 | 0x00000000 | 0xA00371B0 | 181 |
| 1.4.359 | reg : solutiontable_out_pres ubrate_4 | 0x00000000 | 0xA00371B4 | 181 |
| 1.4.360 | reg : solutiontable_out_pres ubrate_5 | 0x00000000 | 0xA00371B8 | 181 |
| 1.4.361 | reg : solutiontable_out_pres ubrate_6 | 0x00000000 | 0xA00371BC | 181 |
| 1.4.362 | reg : solutiontable_out_pres ubrate_7 | 0x00000000 | 0xA00371C0 | 181 |
| 1.4.363 | reg : solutiontable_out_pres ubrate_8 | 0x00000000 | 0xA00371C4 | 181 |
| 1.4.364 | reg : solutiontable_out_pres ubrate_9 | 0x00000000 | 0xA00371C8 | 182 |
| 1.4.365 | reg : solutiontable_out_pres ubrate_10 | 0x00000000 | 0xA00371CC | 182 |
| 1.4.366 | reg : solutiontable_out_pres ubrate_11 | 0x00000000 | 0xA00371D0 | 182 |
| 1.4.367 | reg : solutiontable_out_pres ubrate_12 | 0x00000000 | 0xA00371D4 | 182 |
| 1.4.368 | reg : solutiontable_out_pres ubrate_13 | 0x00000000 | 0xA00371D8 | 182 |
| 1.4.369 | reg : solutiontable_out_pres ubrate_14 | 0x00000000 | 0xA00371DC | 182 |
| 1.4.370 | reg : solutiontable_out_pres ubrate_15 | 0x00000000 | 0xA00371E0 | 182 |
| 1.4.371 | reg : solutiontable_out_pres ubrate_16 | 0x00000000 | 0xA00371E4 | 183 |
| 1.4.372 | reg : solutiontable_out_pres ubrate_17 | 0x00000000 | 0xA00371E8 | 183 |
| 1.4.373 | reg : solutiontable_out_pres ubrate_18 | 0x00000000 | 0xA00371EC | 183 |

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| 1.4.374 | reg : solutiontable_out_prescubrate_19 | 0x00000000 | 0xA00371F0 | 183 |
| 1.4.375 | reg : solutiontable_out_cm_1 | 0x00000000 | 0xA00371F4 | 183 |
| 1.4.376 | reg : solutiontable_out_cm_2 | 0x00000000 | 0xA00371F8 | 183 |
| 1.4.377 | reg : solutiontable_out_cm_3 | 0x00000000 | 0xA00371FC | 183 |
| 1.4.378 | reg : solutiontable_out_cm_4 | 0x00000000 | 0xA0037200 | 184 |
| 1.4.379 | reg : solutiontable_out_cm_5 | 0x00000000 | 0xA0037204 | 184 |
| 1.4.380 | reg : solutiontable_out_cm_6 | 0x00000000 | 0xA0037208 | 184 |
| 1.4.381 | reg : solutiontable_out_cm_7 | 0x00000000 | 0xA003720C | 184 |
| 1.4.382 | reg : solutiontable_out_cm_8 | 0x00000000 | 0xA0037210 | 184 |
| 1.4.383 | reg : solutiontable_out_cm_9 | 0x00000000 | 0xA0037214 | 184 |
| 1.4.384 | reg : solutiontable_out_cm_10 | 0x00000000 | 0xA0037218 | 184 |
| 1.4.385 | reg : solutiontable_out_cm_11 | 0x00000000 | 0xA003721C | 184 |
| 1.4.386 | reg : solutiontable_out_cm_12 | 0x00000000 | 0xA0037220 | 185 |
| 1.4.387 | reg : solutiontable_out_cm_13 | 0x00000000 | 0xA0037224 | 185 |
| 1.4.388 | reg : solutiontable_out_cm_14 | 0x00000000 | 0xA0037228 | 185 |
| 1.4.389 | reg : solutiontable_out_cm_15 | 0x00000000 | 0xA003722C | 185 |
| 1.4.390 | reg : solutiontable_out_cm_16 | 0x00000000 | 0xA0037230 | 185 |
| 1.4.391 | reg : solutiontable_out_cm_17 | 0x00000000 | 0xA0037234 | 185 |
| 1.4.392 | reg : solutiontable_out_cm_18 | 0x00000000 | 0xA0037238 | 185 |
| 1.4.393 | reg : solutiontable_out_cm_19 | 0x00000000 | 0xA003723C | 186 |
| 1.4.394 | reg : solutiontable_out_dm_1 | 0x00000000 | 0xA0037240 | 186 |
| 1.4.395 | reg : solutiontable_out_dm_2 | 0x00000000 | 0xA0037244 | 186 |
| 1.4.396 | reg : solutiontable_out_dm_3 | 0x00000000 | 0xA0037248 | 186 |
| 1.4.397 | reg : solutiontable_out_dm_4 | 0x00000000 | 0xA003724C | 186 |
| 1.4.398 | reg : solutiontable_out_dm_5 | 0x00000000 | 0xA0037250 | 186 |
| 1.4.399 | reg : solutiontable_out_dm_6 | 0x00000000 | 0xA0037254 | 186 |
| 1.4.400 | reg : solutiontable_out_dm_7 | 0x00000000 | 0xA0037258 | 186 |
| 1.4.401 | reg : solutiontable_out_dm_8 | 0x00000000 | 0xA003725C | 187 |
| 1.4.402 | reg : solutiontable_out_dm_9 | 0x00000000 | 0xA0037260 | 187 |
| 1.4.403 | reg : solutiontable_out_dm_10 | 0x00000000 | 0xA0037264 | 187 |
| 1.4.404 | reg : solutiontable_out_dm_11 | 0x00000000 | 0xA0037268 | 187 |
| 1.4.405 | reg : solutiontable_out_dm_12 | 0x00000000 | 0xA003726C | 187 |
| 1.4.406 | reg : solutiontable_out_dm_13 | 0x00000000 | 0xA0037270 | 187 |
| 1.4.407 | reg : solutiontable_out_dm_14 | 0x00000000 | 0xA0037274 | 187 |
| 1.4.408 | reg : solutiontable_out_dm_15 | 0x00000000 | 0xA0037278 | 187 |
| 1.4.409 | reg : solutiontable_out_dm_16 | 0x00000000 | 0xA003727C | 188 |
| 1.4.410 | reg : solutiontable_out_dm_17 | 0x00000000 | 0xA0037280 | 188 |
| 1.4.411 | reg : solutiontable_out_dm_18 | 0x00000000 | 0xA0037284 | 188 |
| 1.4.412 | reg : solutiontable_out_dm_19 | 0x00000000 | 0xA0037288 | 188 |
| 1.4.413 | reg : solutiontable_out_dcdphi | 0x00000000 | 0xA003728C | 188 |
| 1.4.414 | reg : solutiontable_out_phi1margin_1 | 0x00000000 | 0xA0037290 | 188 |
| 1.4.415 | reg : solutiontable_out_phi1margin_2 | 0x00000000 | 0xA0037294 | 188 |
| 1.4.416 | reg : solutiontable_out_phi1margin_3 | 0x00000000 | 0xA0037298 | 189 |

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|---|---|---|---|---|
| 1.4.417 | reg : solutiontable_out_phi1 margin_4 | 0x00000000 | 0xA003729C | 189 |
| 1.4.418 | reg : solutiontable_out_phi1 margin_5 | 0x00000000 | 0xA00372A0 | 189 |
| 1.4.419 | reg : solutiontable_out_phi1 margin_6 | 0x00000000 | 0xA00372A4 | 189 |
| 1.4.420 | reg : solutiontable_out_phi1 margin_7 | 0x00000000 | 0xA00372A8 | 189 |
| 1.4.421 | reg : solutiontable_out_phi1 margin_8 | 0x00000000 | 0xA00372AC | 189 |
| 1.4.422 | reg : solutiontable_out_phi1 margin_9 | 0x00000000 | 0xA00372B0 | 190 |
| 1.4.423 | reg : solutiontable_out_phi1 margin_10 | 0x00000000 | 0xA00372B4 | 190 |
| 1.4.424 | reg : solutiontable_out_phi1 margin_11 | 0x00000000 | 0xA00372B8 | 190 |
| 1.4.425 | reg : solutiontable_out_phi1 margin_12 | 0x00000000 | 0xA00372BC | 190 |
| 1.4.426 | reg : solutiontable_out_phi1 margin_13 | 0x00000000 | 0xA00372C0 | 190 |
| 1.4.427 | reg : solutiontable_out_phi1 margin_14 | 0x00000000 | 0xA00372C4 | 190 |
| 1.4.428 | reg : solutiontable_out_phi1 margin_15 | 0x00000000 | 0xA00372C8 | 190 |
| 1.4.429 | reg : solutiontable_out_phi1 margin_16 | 0x00000000 | 0xA00372CC | 191 |
| 1.4.430 | reg : solutiontable_out_phi1 margin_17 | 0x00000000 | 0xA00372D0 | 191 |
| 1.4.431 | reg : solutiontable_out_phi1 margin_18 | 0x00000000 | 0xA00372D4 | 191 |
| 1.4.432 | reg : solutiontable_out_phi1 margin_19 | 0x00000000 | 0xA00372D8 | 191 |
| 1.4.433 | reg : solutiontable_out_phi0 margin | 0x00000000 | 0xA00372DC | 191 |
| 1.4.434 | reg : solutiontable_out_satr ateavg_off | 0x00000000 | 0xA00372E0 | 191 |
| 1.4.435 | reg : solutiontable_out_satr ateavg_on | 0x00000000 | 0xA00372E4 | 192 |
| 1.4.436 | reg : solutiontable_out_xint 3sigma_avg | 0x00000000 | 0xA00372E8 | 192 |
| 1.4.437 | reg : solutiontable_out_pres ubrate_avg | 0x00000000 | 0xA00372EC | 192 |
| 1.4.438 | reg : solutiontable_out_opt_ solution | 0x00000000 | 0xA00372F0 | 192 |
| 1.4.439 | reg : solutiontable_out_bk_s olution | 0x00000000 | 0xA00372F4 | 192 |
| 1.4.440 | reg : region_7_end_tag | 0x00000000 | 0xA00372F8 | 192 |
| 1.4.441 | reg : region_8_start_tag | 0x00000000 | 0xA0038000 | 192 |
| 1.4.442 | reg : region_8_dtec_tod_lsbs | 0x00000000 | 0xA0038004 | 193 |
| 1.4.443 | reg : region_8_dtec_tod_msbs | 0x00000000 | 0xA0038008 | 193 |
| 1.4.444 | reg : region_8_dtec_lts | 0x00000000 | 0xA003800C | 193 |
| 1.4.445 | reg : req_func_out | 0x00000000 | 0xA0038010 | 193 |
| 1.4.446 | reg : state | 0x00000000 | 0xA0038014 | 193 |
| 1.4.447 | reg : test_probes_probe1 | 0x00000000 | 0xA0038018 | 193 |
| 1.4.448 | reg : test_probes_probe2 | 0x00000000 | 0xA003801C | 193 |
| 1.4.449 | reg : test_probes_probe3 | 0x00000000 | 0xA0038020 | 193 |
| 1.4.450 | reg : internal_clst_done_lat ched | 0x00000000 | 0xA0038024 | 194 |
| 1.4.451 | reg : diag_exposure_preriset ime | 0x00000000 | 0xA0038028 | 194 |
| 1.4.452 | reg : diag_exposure_exposure _flag | 0x00000000 | 0xA003802C | 194 |
| 1.4.453 | reg : diag_exposure_falltime _flag | 0x00000000 | 0xA0038030 | 194 |
| 1.4.454 | reg : diag_exposure_risetime _flag | 0x00000000 | 0xA0038034 | 194 |
| 1.4.455 | reg : diag_state_diag | 0x00000000 | 0xA0038038 | 194 |
| 1.4.456 | reg : xer_out_xer_bank1 | 0x00000000 | 0xA003803C | 194 |

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| 1.4.457 | reg : xer_out_xer_bank2 | 0x00000000 | 0xA0038040 | 195 |
| 1.4.458 | reg : events_out_events_bank 1 | 0x00000000 | 0xA0038044 | 195 |
| 1.4.459 | reg : events_out_events_bank 2 | 0x00000000 | 0xA0038048 | 195 |
| 1.4.460 | reg : warnings_out_warnings_ bank1 | 0x00000000 | 0xA003804C | 195 |
| 1.4.461 | reg : warnings_out_warnings_ bank2 | 0x00000000 | 0xA0038050 | 195 |
| 1.4.462 | reg : region_8_end_tag | 0x00000000 | 0xA0038054 | 195 |
| 1.4.463 | reg : region_9_start_tag | 0x00000000 | 0xA0039000 | 195 |
| 1.4.464 | reg : region_9_dtec_tod_lsbs | 0x00000000 | 0xA0039004 | 195 |
| 1.4.465 | reg : region_9_dtec_tod_msbs | 0x00000000 | 0xA0039008 | 196 |
| 1.4.466 | reg : region_9_dtec_lts | 0x00000000 | 0xA003900C | 196 |
| 1.4.467 | reg : dcm_diag_missing_dropl ets | 0x00000000 | 0xA0039010 | 196 |
| 1.4.468 | reg : dcm_diag_pklabels_roi1 _1 | 0x00000000 | 0xA0039014 | 196 |
| 1.4.469 | reg : dcm_diag_pklabels_roi1 _2 | 0x00000000 | 0xA0039018 | 196 |
| 1.4.470 | reg : dcm_diag_pklabels_roi1 _3 | 0x00000000 | 0xA003901C | 196 |
| 1.4.471 | reg : dcm_diag_pklabels_roi1 _4 | 0x00000000 | 0xA0039020 | 196 |
| 1.4.472 | reg : dcm_diag_pklabels_roi1 _5 | 0x00000000 | 0xA0039024 | 196 |
| 1.4.473 | reg : dcm_diag_pklabels_roi1 _6 | 0x00000000 | 0xA0039028 | 197 |
| 1.4.474 | reg : dcm_diag_pklabels_roi1 _7 | 0x00000000 | 0xA003902C | 197 |
| 1.4.475 | reg : dcm_diag_pklabels_roi1 _8 | 0x00000000 | 0xA0039030 | 197 |
| 1.4.476 | reg : dcm_diag_pklabels_roi1 _9 | 0x00000000 | 0xA0039034 | 197 |
| 1.4.477 | reg : dcm_diag_pklabels_roi1 _10 | 0x00000000 | 0xA0039038 | 197 |
| 1.4.478 | reg : dcm_diag_pklabels_roi1 _11 | 0x00000000 | 0xA003903C | 197 |
| 1.4.479 | reg : dcm_diag_pklabels_roi1 _12 | 0x00000000 | 0xA0039040 | 197 |
| 1.4.480 | reg : dcm_diag_pklabels_roi1 _13 | 0x00000000 | 0xA0039044 | 198 |
| 1.4.481 | reg : dcm_diag_pklabels_roi1 _14 | 0x00000000 | 0xA0039048 | 198 |
| 1.4.482 | reg : dcm_diag_pklabels_roi1 _15 | 0x00000000 | 0xA003904C | 198 |
| 1.4.483 | reg : dcm_diag_pklabels_roi1 _16 | 0x00000000 | 0xA0039050 | 198 |
| 1.4.484 | reg : dcm_diag_pklabels_roi1 _17 | 0x00000000 | 0xA0039054 | 198 |
| 1.4.485 | reg : dcm_diag_pklabels_roi1 _18 | 0x00000000 | 0xA0039058 | 198 |
| 1.4.486 | reg : dcm_diag_pklabels_roi1 _19 | 0x00000000 | 0xA003905C | 198 |
| 1.4.487 | reg : dcm_diag_pklabels_roi1 _20 | 0x00000000 | 0xA0039060 | 198 |
| 1.4.488 | reg : dcm_diag_pklabels_roi1 _21 | 0x00000000 | 0xA0039064 | 199 |
| 1.4.489 | reg : dcm_diag_pklabels_roi1 _22 | 0x00000000 | 0xA0039068 | 199 |
| 1.4.490 | reg : dcm_diag_pklabels_roi1 _23 | 0x00000000 | 0xA003906C | 199 |
| 1.4.491 | reg : dcm_diag_pklabels_roi1 _24 | 0x00000000 | 0xA0039070 | 199 |
| 1.4.492 | reg : dcm_diag_pkposglobal_r oi1_1 | 0x00000000 | 0xA0039074 | 199 |
| 1.4.493 | reg : dcm_diag_pkposglobal_r oi1_2 | 0x00000000 | 0xA0039078 | 199 |

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|---|---|---|---|---|
| 1.4.494 | reg : dcm_diag_pkposglobal_roi1_3 | 0x00000000 | 0xA003907C | 199 |
| 1.4.495 | reg : dcm_diag_pkposglobal_roi1_4 | 0x00000000 | 0xA0039080 | 199 |
| 1.4.496 | reg : dcm_diag_pkposglobal_roi1_5 | 0x00000000 | 0xA0039084 | 200 |
| 1.4.497 | reg : dcm_diag_pkposglobal_roi1_6 | 0x00000000 | 0xA0039088 | 200 |
| 1.4.498 | reg : dcm_diag_pkposglobal_roi1_7 | 0x00000000 | 0xA003908C | 200 |
| 1.4.499 | reg : dcm_diag_pkposglobal_roi1_8 | 0x00000000 | 0xA0039090 | 200 |
| 1.4.500 | reg : dcm_diag_pkposglobal_roi1_9 | 0x00000000 | 0xA0039094 | 200 |
| 1.4.501 | reg : dcm_diag_pkposglobal_roi1_10 | 0x00000000 | 0xA0039098 | 200 |
| 1.4.502 | reg : dcm_diag_pkposglobal_roi1_11 | 0x00000000 | 0xA003909C | 200 |
| 1.4.503 | reg : dcm_diag_pkposglobal_roi1_12 | 0x00000000 | 0xA00390A0 | 201 |
| 1.4.504 | reg : dcm_diag_pkposglobal_roi1_13 | 0x00000000 | 0xA00390A4 | 201 |
| 1.4.505 | reg : dcm_diag_pkposglobal_roi1_14 | 0x00000000 | 0xA00390A8 | 201 |
| 1.4.506 | reg : dcm_diag_pkposglobal_roi1_15 | 0x00000000 | 0xA00390AC | 201 |
| 1.4.507 | reg : dcm_diag_pkposglobal_roi1_16 | 0x00000000 | 0xA00390B0 | 201 |
| 1.4.508 | reg : dcm_diag_pkposglobal_roi1_17 | 0x00000000 | 0xA00390B4 | 201 |
| 1.4.509 | reg : dcm_diag_pkposglobal_roi1_18 | 0x00000000 | 0xA00390B8 | 201 |
| 1.4.510 | reg : dcm_diag_pkposglobal_roi1_19 | 0x00000000 | 0xA00390BC | 201 |
| 1.4.511 | reg : dcm_diag_pkposglobal_roi1_20 | 0x00000000 | 0xA00390C0 | 202 |
| 1.4.512 | reg : dcm_diag_pkposglobal_roi1_21 | 0x00000000 | 0xA00390C4 | 202 |
| 1.4.513 | reg : dcm_diag_pkposglobal_roi1_22 | 0x00000000 | 0xA00390C8 | 202 |
| 1.4.514 | reg : dcm_diag_pkposglobal_roi1_23 | 0x00000000 | 0xA00390CC | 202 |
| 1.4.515 | reg : dcm_diag_pkposglobal_roi1_24 | 0x00000000 | 0xA00390D0 | 202 |
| 1.4.516 | reg : region_9_end_tag | 0x00000000 | 0xA00390D4 | 202 |
| 1.4.517 | reg : region_10_start_tag | 0x00000000 | 0xA003A000 | 202 |
| 1.4.518 | reg : region_10_dtec_tod_lsbs | 0x00000000 | 0xA003A004 | 202 |
| 1.4.519 | reg : region_10_dtec_tod_msbs | 0x00000000 | 0xA003A008 | 203 |
| 1.4.520 | reg : region_10_dtec_lts | 0x00000000 | 0xA003A00C | 203 |
| 1.4.521 | reg : clustering_dcm_diag_pkval_median_updated_label2 | 0x00000000 | 0xA003A010 | 203 |
| 1.4.522 | reg : clustering_dcm_diag_pkval_std_updated_label2 | 0x00000000 | 0xA003A014 | 203 |
| 1.4.523 | reg : clustering_dcm_diag_pkval_median_updated_label3 | 0x00000000 | 0xA003A018 | 203 |
| 1.4.524 | reg : clustering_dcm_diag_pkval_std_updated_label3 | 0x00000000 | 0xA003A01C | 203 |
| 1.4.525 | reg : clustering_dcm_diag_pkwidth_median_updated_label2 | 0x00000000 | 0xA003A020 | 204 |
| 1.4.526 | reg : clustering_dcm_diag_pkwidth_std_updated_label2 | 0x00000000 | 0xA003A024 | 204 |
| 1.4.527 | reg : clustering_dcm_diag_pkwidth_median_updated_label3 | 0x00000000 | 0xA003A028 | 204 |
| 1.4.528 | reg : clustering_dcm_diag_pkwidth_std_updated_label3 | 0x00000000 | 0xA003A02C | 204 |
| 1.4.529 | reg : clustering_dcm_diag_sa | 0x00000000 | 0xA003A030 | 204 |

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|---|---|---|---|---|
| | trate_dcm_small | | | |
| 1.4.530 | reg : clustering_dcm_diag_noise_level_updated_std | 0x00000000 | 0xA003A034 | 204 |
| 1.4.531 | reg : clustering_dcm_diag_jitter_dcm_main | 0x00000000 | 0xA003A038 | 205 |
| 1.4.532 | reg : clustering_dcm_diag_jitter_dcm_subcl_a | 0x00000000 | 0xA003A03C | 205 |
| 1.4.533 | reg : clustering_dcm_diag_jitter_dcm_presubcl | 0x00000000 | 0xA003A040 | 205 |
| 1.4.534 | reg : clustering_dcm_diag_pksaturaterate | 0x00000000 | 0xA003A044 | 205 |
| 1.4.535 | reg : clustering_dcm_diag_pkoscilevel | 0x00000000 | 0xA003A048 | 205 |
| 1.4.536 | reg : clustering_dcm_diag_siglevel_presubcl | 0x00000000 | 0xA003A04C | 205 |
| 1.4.537 | reg : clustering_dcm_diag_bl_mean | 0x00000000 | 0xA003A050 | 205 |
| 1.4.538 | reg : clustering_dcm_diag_pkval_median_updated_label1 | 0x00000000 | 0xA003A054 | 206 |
| 1.4.539 | reg : clustering_dcm_diag_pkwidth_median_updated_label1 | 0x00000000 | 0xA003A058 | 206 |
| 1.4.540 | reg : clustering_dcm_diag_pkwidth_median_updated_label0 | 0x00000000 | 0xA003A05C | 206 |
| 1.4.541 | reg : clustering_ddm_diag_bl_mean | 0x00000000 | 0xA003A060 | 206 |
| 1.4.542 | reg : clustering_ddm_diag_pkval_median_updated_label3 | 0x00000000 | 0xA003A064 | 206 |
| 1.4.543 | reg : clustering_ddm_diag_pkval_std_updated_label3 | 0x00000000 | 0xA003A068 | 206 |
| 1.4.544 | reg : clustering_ddm_diag_pkwidth_median_updated_label3 | 0x00000000 | 0xA003A06C | 207 |
| 1.4.545 | reg : clustering_ddm_diag_pkwidth_std_updated_label3 | 0x00000000 | 0xA003A070 | 207 |
| 1.4.546 | reg : clustering_ddm_diag_satrate_ddm | 0x00000000 | 0xA003A074 | 207 |
| 1.4.547 | reg : clustering_ddm_diag_noise_level_updated_std | 0x00000000 | 0xA003A078 | 207 |
| 1.4.548 | reg : clustering_ddm_diag_pksaturaterate | 0x00000000 | 0xA003A07C | 207 |
| 1.4.549 | reg : clustering_ddm_diag_pkoscilevel | 0x00000000 | 0xA003A080 | 207 |
| 1.4.550 | reg : region_10_end_tag | 0x00000000 | 0xA003A084 | 208 |
| 1.4.551 | reg : region_12_start_tag | 0x00000000 | 0xA003C000 | 208 |
| 1.4.552 | reg : region_12_dtec_tod_lsbs | 0x00000000 | 0xA003C004 | 208 |
| 1.4.553 | reg : region_12_dtec_tod_msbs | 0x00000000 | 0xA003C008 | 208 |
| 1.4.554 | reg : region_12_dtec_lts | 0x00000000 | 0xA003C00C | 208 |
| 1.4.555 | reg : idcb_triggers_idcb_trigger_ch1 | 0x00000000 | 0xA003C010 | 208 |
| 1.4.556 | reg : idcb_triggers_idcb_trigger_ch2 | 0x00000000 | 0xA003C014 | 208 |
| 1.4.557 | reg : idcb_triggers_idcb_trigger_ch7 | 0x00000000 | 0xA003C018 | 208 |
| 1.4.558 | reg : idcb_triggers_idcb_trigger_ch9 | 0x00000000 | 0xA003C01C | 209 |
| 1.4.559 | reg : idcb_triggers_idcb_trigger_ch10 | 0x00000000 | 0xA003C020 | 209 |
| 1.4.560 | reg : idcb_triggers_idcb_trigger_ch12 | 0x00000000 | 0xA003C024 | 209 |
| 1.4.561 | reg : region_12_end_tag | 0x00000000 | 0xA003C028 | 209 |
| 1.4.562 | reg : region_13_start_tag | 0x00000000 | 0xA003D000 | 209 |
| 1.4.563 | reg : region_13_dtec_tod_lsbs | 0x00000000 | 0xA003D004 | 209 |
| 1.4.564 | reg : region_13_dtec_tod_msbs | 0x00000000 | 0xA003D008 | 209 |
| 1.4.565 | reg : region_13_dtec_lts | 0x00000000 | 0xA003D00C | 209 |
| 1.4.566 | reg : state_duplicate4reg13 | 0x00000000 | 0xA003D010 | 210 |

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|---|---|---|---|---|
| 1.4.567 | reg : cal_lf_basedropsetting | 0x00000000 | 0xA003D014 | 210 |
| 1.4.568 | reg : cal_lf_basedropiteration | 0x00000000 | 0xA003D018 | 210 |
| 1.4.569 | reg : cal_lf_costfuncoptsetting | 0x00000000 | 0xA003D01C | 210 |
| 1.4.570 | reg : cal_lf_costfunciteration | 0x00000000 | 0xA003D020 | 210 |
| 1.4.571 | reg : cal_lf_stateupdate | 0x00000000 | 0xA003D024 | 210 |
| 1.4.572 | reg : cal_lf_spare5 | 0x00000000 | 0xA003D028 | 210 |
| 1.4.573 | reg : cal_lf_spare6 | 0x00000000 | 0xA003D02C | 211 |
| 1.4.574 | reg : cal_lf_spare7 | 0x00000000 | 0xA003D030 | 211 |
| 1.4.575 | reg : cal_lf_spare8 | 0x00000000 | 0xA003D034 | 211 |
| 1.4.576 | reg : cal_lf_spare9 | 0x00000000 | 0xA003D038 | 211 |
| 1.4.577 | reg : cal_hf_du | 0x00000000 | 0xA003D03C | 211 |
| 1.4.578 | reg : cal_hf_alpha1 | 0x00000000 | 0xA003D040 | 211 |
| 1.4.579 | reg : cal_hf_alpha2 | 0x00000000 | 0xA003D044 | 211 |
| 1.4.580 | reg : cal_hf_alpha0 | 0x00000000 | 0xA003D048 | 211 |
| 1.4.581 | reg : cal_hf_beta | 0x00000000 | 0xA003D04C | 211 |
| 1.4.582 | reg : cal_hf_clockcorrectionfactor | 0x00000000 | 0xA003D050 | 212 |
| 1.4.583 | reg : cal_hf_spare1 | 0x00000000 | 0xA003D054 | 212 |
| 1.4.584 | reg : cal_hf_spare2 | 0x00000000 | 0xA003D058 | 212 |
| 1.4.585 | reg : cal_hf_spare3 | 0x00000000 | 0xA003D05C | 212 |
| 1.4.586 | reg : cal_hf_spare4 | 0x00000000 | 0xA003D060 | 212 |
| 1.4.587 | reg : clustering_dcm_diag_pkval_median_updated_label3_duplicate4reg13 | 0x00000000 | 0xA003D064 | 212 |
| 1.4.588 | reg : clustering_dcm_diag_pkwidth_median_updated_label3_duplicate4reg13 | 0x00000000 | 0xA003D068 | 212 |
| 1.4.589 | reg : clustering_dcm_diag_noise_level_updated_std_duplicate4reg13 | 0x00000000 | 0xA003D06C | 213 |
| 1.4.590 | reg : clustering_ddm_diag_pkval_median_updated_label3_duplicate4reg13 | 0x00000000 | 0xA003D070 | 213 |
| 1.4.591 | reg : clustering_ddm_diag_pkwidth_median_updated_label3_duplicate4reg13 | 0x00000000 | 0xA003D074 | 213 |
| 1.4.592 | reg : clustering_ddm_diag_noise_level_updated_std_duplicate4reg13 | 0x00000000 | 0xA003D078 | 213 |
| 1.4.593 | reg : region_13_end_tag | 0x00000000 | 0xA003D07C | 213 |
| 1.5 | block : algo_csr_registers_srdl | | 0xA0050000 - 0xA0050173 | 213 |
| 1.5.1 | reg : algo_csr_module_name | 0x616C6749 | 0xA0050000 | 213 |
| 1.5.2 | reg : algo_csr_module_version | 0x05210320 | 0xA0050004 | 214 |
| 1.5.3 | reg : algo_csr_page_properties | 0x80000101 | 0xA0050008 | 214 |
| 1.5.4 | reg : algo_csr_scratchregister | 0x12345678 | 0xA005000C | 214 |
| 1.5.5 | reg : algo_csr_irq_enable | 0x00000000 | 0xA0050010 | 214 |
| 1.5.6 | reg : algo_csr_irq_pending | 0x00000000 | 0xA0050014 | 214 |
| 1.5.7 | reg : algo_csr_irq_raw | 0x00000000 | 0xA0050018 | 214 |
| 1.5.8 | reg : algo_csr_irq_force | 0x00000000 | 0xA005001C | 214 |
| 1.5.9 | reg : dcm_status_reg | 0x00000000 | 0xA0050020 | 215 |
| 1.5.10 | reg : ddm_status_reg | 0x00000000 | 0xA0050024 | 215 |
| 1.5.11 | reg : ch3_xfer_count | 0x00000000 | 0xA0050100 | 215 |
| 1.5.12 | reg : ch3_drop_count | 0x00000000 | 0xA0050104 | 215 |
| 1.5.13 | reg : ch4_xfer_count | 0x00000000 | 0xA0050108 | 215 |
| 1.5.14 | reg : ch4_drop_count | 0x00000000 | 0xA005010C | 215 |
| 1.5.15 | reg : ch5_xfer_count | 0x00000000 | 0xA0050110 | 215 |
| 1.5.16 | reg : ch5_drop_count | 0x00000000 | 0xA0050114 | 216 |
| 1.5.17 | reg : ch6_xfer_count | 0x00000000 | 0xA0050118 | 216 |
| 1.5.18 | reg : ch6_drop_count | 0x00000000 | 0xA005011C | 216 |
| 1.5.19 | reg : ch7_xfer_count | 0x00000000 | 0xA0050120 | 216 |

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| 1.5.20 | reg : ch7_drop_count | 0x00000000 | 0xA0050124 | 216 |
| 1.5.21 | reg : ch8_xfer_count | 0x00000000 | 0xA0050128 | 216 |
| 1.5.22 | reg : ch8_drop_count | 0x00000000 | 0xA005012C | 216 |
| 1.5.23 | reg : ch9_xfer_count | 0x00000000 | 0xA0050130 | 216 |
| 1.5.24 | reg : ch9_drop_count | 0x00000000 | 0xA0050134 | 216 |
| 1.5.25 | reg : ch10_xfer_count | 0x00000000 | 0xA0050138 | 217 |
| 1.5.26 | reg : ch10_drop_count | 0x00000000 | 0xA005013C | 217 |
| 1.5.27 | reg : ch12_xfer_count | 0x00000000 | 0xA0050140 | 217 |
| 1.5.28 | reg : ch12_drop_count | 0x00000000 | 0xA0050144 | 217 |
| 1.5.29 | reg : algo_to_damp_xfer_count | 0x00000000 | 0xA0050150 | 217 |
| 1.5.30 | reg : algo_to_damp_drop_count | 0x00000000 | 0xA0050154 | 217 |
| 1.5.31 | reg : dcm_pkts_inframe_cnt | 0x00000000 | 0xA0050158 | 217 |
| 1.5.32 | reg : dcm_pkts_crc_err_cnt | 0x00000000 | 0xA005015C | 217 |
| 1.5.33 | reg : dcm_pkts_lgth_err_cnt | 0x00000000 | 0xA0050160 | 218 |
| 1.5.34 | reg : ddm_pkts_inframe_cnt | 0x00000000 | 0xA0050164 | 218 |
| 1.5.35 | reg : ddm_pkts_crc_err_cnt | 0x00000000 | 0xA0050168 | 218 |
| 1.5.36 | reg : ddm_pkts_lgth_err_cnt | 0x00000000 | 0xA005016C | 218 |
| 1.5.37 | reg : pulse_1ms_phase_delay | 0x00000100 | 0xA0050170 | 218 |
| 1.6 | block : tsel_if_bridge_srdl | | 0xA0080000 - 0xA00867FF | 218 |
| 1.6.1 | reg : MODULE_NAME | 0x52363335 | 0xA0080000 | 218 |
| 1.6.2 | reg : MODULE_VERSION | 0x00000000 | 0xA0080004 | 218 |
| 1.6.3 | reg : HEADER_INFO | 0x00000004 | 0xA0080008 | 219 |
| 1.6.4 | reg : SCRATCHPAD | 0x00000000 | 0xA008000C | 219 |
| 1.6.5 | reg : IRQ_ENABLE | 0x00000000 | 0xA0080010 | 219 |
| 1.6.6 | reg : IRQ_PENDING | 0x00000000 | 0xA0080014 | 219 |
| 1.6.7 | reg : IRQ_RAW | 0x00000000 | 0xA0080018 | 219 |
| 1.6.8 | reg : IRQ_FORCE | 0x00000000 | 0xA008001C | 220 |
| 1.6.9 | reg : BUILD_INFO | 0x00000000 | 0xA0080040 | 220 |
| 1.6.10 | reg : BUILD_INFO1 | 0x00000000 | 0xA0080044 | 220 |
| 1.6.11 | reg : BUILD_INFO2 | 0x00000000 | 0xA0080048 | 220 |
| 1.6.12 | reg : TSEL_CTRL | 0x00000000 | 0xA0080060 | 220 |
| 1.6.13 | reg : TSEL_CLIENT_TX_MAC_INSERT_MSB | 0x00001234 | 0xA0080064 | 221 |
| 1.6.14 | reg : TSEL_CLIENT_TX_MAC_INSERT_LSB | 0x56789ABC | 0xA0080068 | 221 |
| 1.6.15 | reg : TSEL_CLIENT_TX_ETH_TYPE | 0x00008000 | 0xA008006C | 221 |
| 1.6.16 | reg : TSEL_CLIENT_RX_SRC_MAC_MSB | 0x00000000 | 0xA0080070 | 221 |
| 1.6.17 | reg : TSEL_CLIENT_RX_SRC_MAC_LSB | 0x00000000 | 0xA0080074 | 221 |
| 1.6.18 | reg : TSEL_CLIENT_RX_SRC_ETH_TYPE | 0x00000000 | 0xA0080078 | 221 |
| 1.6.19 | reg : CPU_INSERT_BUFFER_CTRL | 0x00000000 | 0xA0080080 | 221 |
| 1.6.20 | reg : CPU_CAPTURE_BUFFER_CTL | 0x00000000 | 0xA0080084 | 222 |
| 1.6.21 | reg : CPU_CAPTURE_BUFFER_CTL2 | 0x00000000 | 0xA0080088 | 222 |
| 1.6.22 | reg : TSEL_GDB_STATUS | 0x00000000 | 0xA00800A0 | 222 |
| 1.6.23 | reg : TSEL_DEBUG_CTRL | 0x00000000 | 0xA00800A4 | 222 |
| 1.6.24 | reg : TSEL_DEBUG_CTRL2 | 0x00000020 | 0xA00800A8 | 223 |
| 1.6.25 | reg : DEBUG | 0x00000000 | 0xA00800AC | 223 |
| 1.6.26 | reg : DEBUG_LINK_UP_OVERWRITE | 0x00000000 | 0xA00800B0 | 223 |
| 1.6.27 | reg : TSEL_CLK_FREQ | 0x00000000 | 0xA00800B4 | 223 |

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|---|---|---|---|---|
| 1.6.28 | reg : TSEL_DEBUG_IF_SUPPRESS | 0x00000000 | 0xA00800B8 | 223 |
| 1.6.29 | reg : RX_STATS_ENGINE_CTRL | 0x00000000 | 0xA00800C0 | 223 |
| 1.6.30 | reg : RX_STATS_ENGINE_STATUS | 0x00000000 | 0xA00800C4 | 223 |
| 1.6.31 | reg : TX_STATS_ENGINE_CTRL | 0x00000000 | 0xA00800C8 | 224 |
| 1.6.32 | reg : TX_STATS_ENGINE_STATUS | 0x00000000 | 0xA00800CC | 224 |
| 1.6.33 | reg : PACKET_GEN_CTRL0 | 0x00000000 | 0xA00800E0 | 224 |
| 1.6.34 | reg : PACKET_GEN_CTRL1 | 0x00000000 | 0xA00800E4 | 224 |
| 1.6.35 | reg : PACKET_GEN_CTRL2 | 0x00000000 | 0xA00800E8 | 224 |
| 1.6.36 | reg : PACKET_GEN_CHECKER_CTL0 | 0x00000000 | 0xA00800EC | 224 |
| 1.6.37 | reg : PACKET_GEN_CHECKER_CTL1 | 0x00000000 | 0xA00800F0 | 225 |
| 1.6.38 | reg : PKT_COUNT_RX_TOTAL | 0x00000000 | 0xA0080100 | 225 |
| 1.6.39 | reg : BYTE_COUNT_RX_TOTAL | 0x00000000 | 0xA0080104 | 225 |
| 1.6.40 | reg : PKT_COUNT_RX_FCS_ERRO | 0x00000000 | 0xA0080108 | 225 |
| 1.6.41 | reg : BYTE_COUNT_RXTX_LPBK_ERROR | 0x00000000 | 0xA008010C | 225 |
| 1.6.42 | reg : PKT_COUNT_TX_TOTAL | 0x00000000 | 0xA0080120 | 225 |
| 1.6.43 | reg : BYTE_COUNT_TX_TOTAL | 0x00000000 | 0xA0080124 | 225 |
| 1.6.44 | reg : PKT_COUNT_TX_BUS_ERRO | 0x00000000 | 0xA0080128 | 226 |
| 1.6.45 | reg : PKT_COUNT_TX_DATA_ERR R | 0x00000000 | 0xA008012C | 226 |
| 1.6.46 | reg : PKT_COUNT_TX_TOO_SHOR _ERROR | 0x00000000 | 0xA0080130 | 226 |
| 1.6.47 | reg : PKT_COUNT_TX_TOO_LONG ERROR | 0x00000000 | 0xA0080134 | 226 |
| 1.6.48 | reg : CPU_INSERT_BUFFER_CNT | 0x00000000 | 0xA0080140 | 226 |
| 1.6.49 | reg : CPU_CAPTURE_BUFFER_CN | 0x00000000 | 0xA0080144 | 226 |
| 1.6.50 | reg : CPU_CAPTURE_BUFFER_CN 1 | 0x00000000 | 0xA0080148 | 226 |
| 1.6.51 | reg : LINK_DOWN_COUNT | 0x00000000 | 0xA0080150 | 227 |
| 1.6.52 | reg : PACKET_GEN_STATUS0 | 0x00000000 | 0xA0080180 | 227 |
| 1.6.53 | reg : PACKET_GEN_CHECKER_ST TUS0 | 0x00000000 | 0xA0080184 | 227 |
| 1.6.54 | reg : PACKET_GEN_STATUS1 | 0x00000000 | 0xA0080188 | 227 |
| 1.6.55 | reg : PACKET_GEN_CHECKER_ST TUS1 | 0x00000000 | 0xA008018C | 227 |
| 1.6.56 | reg : PACKET_GEN_CHECKER_ST TUS2 | 0x00000000 | 0xA0080190 | 227 |
| 1.6.57 | reg : PACKET_GEN_CHECKER_ST TUS3 | 0x00000000 | 0xA0080194 | 227 |

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|---|---|---|---|---|
| 1.6.58 | reg : PACKET_GEN_CHECKER_STATUS4 | 0x00000000 | 0xA0080198 | 227 |
| 1.6.59 | reg : PACKET_GEN_CHECKER_STATUS5 | 0x00000000 | 0xA008019C | 228 |
| 1.6.60 | memory : CPU_INSERT_BUFFER | | 0xA0081000, 0xA0081004 ... 0xA00817FF | 228 |
| 1.6.60.1 | reg : CPU_INSERT_BUFFER | 0x00000000 | 0xA0081000, 0x0000000000... | |
| 1.6.61 | memory : CPU_CAPTURE_BUFFER | | 0xA0081800, 0xA0081804 ... 0xA0081FFF | 228 |
| 1.6.61.1 | reg : CPU_CAPTURE_BUFFER | 0x00000000 | 0xA0081800, 0x0000000000... | |
| 1.6.62 | memory : RX_STATS_ENGINE | | 0xA0084000, 0xA0084004 ... 0xA00847FF | 228 |
| 1.6.62.1 | reg : RX_STATS_ENGINE | 0x00000000 | 0xA0084000, 0x0000000000... | |
| 1.6.63 | memory : TX_STATS_ENGINE | | 0xA0086000, 0xA0086004 ... 0xA00867FF | 228 |
| 1.6.63.1 | reg : TX_STATS_ENGINE | 0x00000000 | 0xA0086000, 0x0000000000... | |
| 1.7 | block : tsel_if_client_srdl | | 0xA0090000 - 0xA00967FF | 228 |
| 1.7.1 | reg : MODULE_NAME | 0x52363335 | 0xA0090000 | 228 |
| 1.7.2 | reg : MODULE_VERSION | 0x00000000 | 0xA0090004 | 229 |
| 1.7.3 | reg : HEADER_INFO | 0x00000004 | 0xA0090008 | 229 |
| 1.7.4 | reg : SCRATCHPAD | 0x00000000 | 0xA009000C | 229 |
| 1.7.5 | reg : IRQ_ENABLE | 0x00000000 | 0xA0090010 | 229 |
| 1.7.6 | reg : IRQ_PENDING | 0x00000000 | 0xA0090014 | 229 |
| 1.7.7 | reg : IRQ_RAW | 0x00000000 | 0xA0090018 | 230 |
| 1.7.8 | reg : IRQ_FORCE | 0x00000000 | 0xA009001C | 230 |
| 1.7.9 | reg : BUILD_INFO | 0x00000000 | 0xA0090040 | 230 |
| 1.7.10 | reg : BUILD_INFO1 | 0x00000000 | 0xA0090044 | 230 |
| 1.7.11 | reg : BUILD_INFO2 | 0x00000000 | 0xA0090048 | 231 |
| 1.7.12 | reg : TSEL_CTRL | 0x00000000 | 0xA0090060 | 231 |
| 1.7.13 | reg : TSEL_CLIENT_TX_MAC_INSERT_MSB | 0x00001234 | 0xA0090064 | 231 |
| 1.7.14 | reg : TSEL_CLIENT_TX_MAC_INSERT_LSB | 0x56789ABC | 0xA0090068 | 231 |
| 1.7.15 | reg : TSEL_CLIENT_TX_ETH_TYPE | 0x00008000 | 0xA009006C | 231 |
| 1.7.16 | reg : TSEL_CLIENT_RX_SRC_MAC_MSB | 0x00000000 | 0xA0090070 | 231 |
| 1.7.17 | reg : TSEL_CLIENT_RX_SRC_MAC_LSB | 0x00000000 | 0xA0090074 | 231 |
| 1.7.18 | reg : TSEL_CLIENT_RX_SRC_ETH_TYPE | 0x00000000 | 0xA0090078 | 232 |
| 1.7.19 | reg : CPU_INSERT_BUFFER_CTRL | 0x00000000 | 0xA0090080 | 232 |
| 1.7.20 | reg : CPU_CAPTURE_BUFFER_CTL | 0x00000000 | 0xA0090084 | 232 |
| 1.7.21 | reg : CPU_CAPTURE_BUFFER_CTL2 | 0x00000000 | 0xA0090088 | 232 |
| 1.7.22 | reg : TSEL_GDB_STATUS | 0x00000000 | 0xA00900A0 | 232 |
| 1.7.23 | reg : TSEL_DEBUG_CTRL | 0x00000000 | 0xA00900A4 | 233 |
| 1.7.24 | reg : TSEL_DEBUG_CTRL2 | 0x00000020 | 0xA00900A8 | 233 |
| 1.7.25 | reg : DEBUG | 0x00000000 | 0xA00900AC | 233 |
| 1.7.26 | reg : DEBUG_LINK_UP_OVERWRITE | 0x00000000 | 0xA00900B0 | 233 |
| 1.7.27 | reg : TSEL_CLK_FREQ | 0x00000000 | 0xA00900B4 | 233 |
| 1.7.28 | reg : TSEL_DEBUG_IF_SUPPRESS | 0x00000000 | 0xA00900B8 | 233 |

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|---|---|---|---|---|
| 1.7.29 | reg : RX_STATS_ENGINE_CTRL | 0x00000000 | 0xA00900C0 | 234 |
| 1.7.30 | reg : RX_STATS_ENGINE_STATUS | 0x00000000 | 0xA00900C4 | 234 |
| 1.7.31 | reg : TX_STATS_ENGINE_CTRL | 0x00000000 | 0xA00900C8 | 234 |
| 1.7.32 | reg : TX_STATS_ENGINE_STATUS | 0x00000000 | 0xA00900CC | 234 |
| 1.7.33 | reg : PACKET_GEN_CTRL0 | 0x00000000 | 0xA00900E0 | 234 |
| 1.7.34 | reg : PACKET_GEN_CTRL1 | 0x00000000 | 0xA00900E4 | 234 |
| 1.7.35 | reg : PACKET_GEN_CTRL2 | 0x00000000 | 0xA00900E8 | 234 |
| 1.7.36 | reg : PACKET_GEN_CHECKER_CTL0 | 0x00000000 | 0xA00900EC | 235 |
| 1.7.37 | reg : PACKET_GEN_CHECKER_CTL1 | 0x00000000 | 0xA00900F0 | 235 |
| 1.7.38 | reg : PKT_COUNT_RX_TOTAL | 0x00000000 | 0xA0090100 | 235 |
| 1.7.39 | reg : BYTE_COUNT_RX_TOTAL | 0x00000000 | 0xA0090104 | 235 |
| 1.7.40 | reg : PKT_COUNT_RX_FCS_ERRO | 0x00000000 | 0xA0090108 | 235 |
| 1.7.41 | reg : BYTE_COUNT_RXTX_LPBK_ERROR | 0x00000000 | 0xA009010C | 235 |
| 1.7.42 | reg : PKT_COUNT_TX_TOTAL | 0x00000000 | 0xA0090120 | 236 |
| 1.7.43 | reg : BYTE_COUNT_TX_TOTAL | 0x00000000 | 0xA0090124 | 236 |
| 1.7.44 | reg : PKT_COUNT_TX_BUS_ERRO | 0x00000000 | 0xA0090128 | 236 |
| 1.7.45 | reg : PKT_COUNT_TX_DATA_ERR( R | 0x00000000 | 0xA009012C | 236 |
| 1.7.46 | reg : PKT_COUNT_TX_TOO_SHOR _ERROR | 0x00000000 | 0xA0090130 | 236 |
| 1.7.47 | reg : PKT_COUNT_TX_TOO_LONG ERROR | 0x00000000 | 0xA0090134 | 236 |
| 1.7.48 | reg : CPU_INSERT_BUFFER_CNT | 0x00000000 | 0xA0090140 | 236 |
| 1.7.49 | reg : CPU_CAPTURE_BUFFER_CN | 0x00000000 | 0xA0090144 | 237 |
| 1.7.50 | reg : CPU_CAPTURE_BUFFER_CN 1 | 0x00000000 | 0xA0090148 | 237 |
| 1.7.51 | reg : LINK_DOWN_COUNT | 0x00000000 | 0xA0090150 | 237 |
| 1.7.52 | reg : PACKET_GEN_STATUS0 | 0x00000000 | 0xA0090180 | 237 |
| 1.7.53 | reg : PACKET_GEN_CHECKER_STTUS0 | 0x00000000 | 0xA0090184 | 237 |
| 1.7.54 | reg : PACKET_GEN_STATUS1 | 0x00000000 | 0xA0090188 | 237 |
| 1.7.55 | reg : PACKET_GEN_CHECKER_STTUS1 | 0x00000000 | 0xA009018C | 237 |
| 1.7.56 | reg : PACKET_GEN_CHECKER_STTUS2 | 0x00000000 | 0xA0090190 | 237 |
| 1.7.57 | reg : PACKET_GEN_CHECKER_STTUS3 | 0x00000000 | 0xA0090194 | 238 |
| 1.7.58 | reg : PACKET_GEN_CHECKER_STTUS4 | 0x00000000 | 0xA0090198 | 238 |

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|---|---|---|---|---|
| 1.7.59 | reg : PACKET_GEN_CHECKER_STATUS5 | 0x00000000 | 0xA009019C | 238 |
| 1.7.60 | memory : CPU_INSERT_BUFFER | | 0xA0091000, 0xA0091004 ... 0xA00917FF | 238 |
| 1.7.60.1 | reg : CPU_INSERT_BUFFER | 0x00000000 | 0xA0091000, 0x0000000000... | |
| 1.7.61 | memory : CPU_CAPTURE_BUFFER | | 0xA0091800, 0xA0091804 ... 0xA0091FFF | 238 |
| 1.7.61.1 | reg : CPU_CAPTURE_BUFFER | 0x00000000 | 0xA0091800, 0x0000000000... | |
| 1.7.62 | memory : RX_STATS_ENGINE | | 0xA0094000, 0xA0094004 ... 0xA00947FF | 238 |
| 1.7.62.1 | reg : RX_STATS_ENGINE | 0x00000000 | 0xA0094000, 0x0000000000... | |
| 1.7.63 | memory : TX_STATS_ENGINE | | 0xA0096000, 0xA0096004 ... 0xA00967FF | 238 |
| 1.7.63.1 | reg : TX_STATS_ENGINE | 0x00000000 | 0xA0096000, 0x0000000000... | |
| 1.8 | block : tselclient_appl_registers_srdl | | 0xA00A0000 - 0xA00A00EB | 239 |
| 1.8.1 | reg : tselclient_module_name | 0x74636C69 | 0xA00A0000 | 239 |
| 1.8.2 | reg : tselclient_module_version | 0x00000000 | 0xA00A0004 | 239 |
| 1.8.3 | reg : tselclient_page_properties | 0x80000101 | 0xA00A0008 | 239 |
| 1.8.4 | reg : tselclient_scratchregister | 0x12345678 | 0xA00A000C | 239 |
| 1.8.5 | reg : tselclient_irq_enable | 0x00000000 | 0xA00A0010 | 239 |
| 1.8.6 | reg : tselclient_irq_pending | 0x00000000 | 0xA00A0014 | 240 |
| 1.8.7 | reg : tselclient_irq_raw | 0x00000000 | 0xA00A0018 | 240 |
| 1.8.8 | reg : tselclient_irq_force | 0x00000000 | 0xA00A001C | 240 |
| 1.8.9 | reg : rt_data_handler_stat | 0x00000000 | 0xA00A0060 | 240 |
| 1.8.10 | reg : tx_fsm_dg_kpi_ctrl | 0x00000001 | 0xA00A0064 | 241 |
| 1.8.11 | section : pkt1 | | 0xA00A0068 - 0xA00A008F | 241 |
| 1.8.11.1 | reg : tag1 | 0x00000000 | 0xA00A0068 | 241 |
| 1.8.11.2 | reg : timestamp_data | 0x00000000 | 0xA00A006C | 241 |
| 1.8.11.3 | reg : sync_stat_data | 0x00000000 | 0xA00A0070 | 242 |
| 1.8.11.4 | reg : shot_id_data | 0x00000000 | 0xA00A0074 | 242 |
| 1.8.11.5 | reg : burst_id_data | 0x00000000 | 0xA00A0078 | 242 |
| 1.8.11.6 | reg : msec_id_data | 0x00000000 | 0xA00A007C | 242 |
| 1.8.11.7 | reg : lc_diag_data | 0x00000007 | 0xA00A0080 | 242 |
| 1.8.11.8 | reg : pp2mp_tfire_totaldelay_data | 0x00000000 | 0xA00A0084 | 243 |
| 1.8.11.9 | reg : euv_value_data | 0x00000000 | 0xA00A0088 | 243 |
| 1.8.11.10 | reg : tag2 | 0x00000000 | 0xA00A008C | 243 |
| 1.8.12 | reg : ddm_bpam_send7_crc_err_cnt | 0x00000000 | 0xA00A0090 | 243 |
| 1.8.13 | reg : ddm_data_lost_cnt | 0x00000000 | 0xA00A0094 | 243 |
| 1.8.14 | reg : ddm_data_bytes_err_cnt | 0x00000000 | 0xA00A0098 | 243 |
| 1.8.15 | reg : rx_fsm_pkt_lgth_field_err_cnt | 0x00000000 | 0xA00A009C | 243 |
| 1.8.16 | reg : rx_fsm_pload_err_cnt | 0x00000000 | 0xA00A00A0 | 243 |
| 1.8.17 | reg : unknown_pkt_rx_cnt | 0x00000000 | 0xA00A00A4 | 244 |
| 1.8.18 | reg : pkt1_sync_hdr_err_cnt | 0x00000000 | 0xA00A00A8 | 244 |
| 1.8.19 | reg : pkt1_etecflags_hdr_err_cnt | 0x00000000 | 0xA00A00AC | 244 |
| 1.8.20 | reg : pkt1_zeropad_hdr_err_cnt | 0x00000000 | 0xA00A00B0 | 244 |
| 1.8.21 | reg : rx_fsm_eot_err_cnt | 0x00000000 | 0xA00A00B4 | 244 |
| 1.8.22 | reg : pkt1_seq_err_cnt | 0x00000000 | 0xA00A00B8 | 244 |
| 1.8.23 | reg : pkt2_seq_err_cnt | 0x00000000 | 0xA00A00BC | 244 |
| 1.8.24 | reg : rx_fsm_eop_err_cnt | 0x00000000 | 0xA00A00C0 | 244 |
| 1.8.25 | reg : rx_fsm_wdog_err_cnt | 0x00000000 | 0xA00A00C4 | 244 |
| 1.8.26 | reg : pkt2_axis_fsm_wdog_err_cnt | 0x00000000 | 0xA00A00C8 | 245 |
| 1.8.27 | reg : reserved_byte_err_cnt | 0x00000000 | 0xA00A00CC | 245 |
| 1.8.28 | reg : pkt2_zeropad_hdr_err_cnt | 0x00000000 | 0xA00A00D0 | 245 |

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|---|---|---|---|---|
| 1.8.29 | reg : tx_fsm_wdog_err_cnt | 0x00000000 | 0xA00A00D4 | 245 |
| 1.8.30 | reg : pkt1_rx_cnt | 0x00000000 | 0xA00A00D8 | 245 |
| 1.8.31 | reg : pkt2_rx_cnt | 0x00000000 | 0xA00A00DC | 245 |
| 1.8.32 | reg : good_pkt1_rx_cnt | 0x00000000 | 0xA00A00E0 | 245 |
| 1.8.33 | reg : good_pkt2_rx_cnt | 0x00000000 | 0xA00A00E4 | 245 |
| 1.8.34 | reg : good_pkt2_lost_cnt | 0x00000000 | 0xA00A00E8 | 246 |
| 1.9 | block : tselbridge_appl_registers_srdl | | 0xA00A1000 - 0xA00A110F | 246 |
| 1.9.1 | reg : tselbridge_module_name | 0x74627267 | 0xA00A1000 | 246 |
| 1.9.2 | reg : tselbridge_module_version | 0x00000000 | 0xA00A1004 | 246 |
| 1.9.3 | reg : tselbridge_page_properties | 0x80000101 | 0xA00A1008 | 246 |
| 1.9.4 | reg : tselbridge_scratchregister | 0x12345678 | 0xA00A100C | 246 |
| 1.9.5 | reg : tselbridge_irq_enable | 0x00000000 | 0xA00A1010 | 246 |
| 1.9.6 | reg : tselbridge_irq_pending | 0x00000000 | 0xA00A1014 | 247 |
| 1.9.7 | reg : tselbridge_irq_raw | 0x00000000 | 0xA00A1018 | 247 |
| 1.9.8 | reg : tselbridge_irq_force | 0x00000000 | 0xA00A101C | 247 |
| 1.9.9 | reg : rt_data_handler_algo_rx_stat | 0x00000000 | 0xA00A1060 | 247 |
| 1.9.10 | reg : rt_data_handler_boot_rx_stat | 0x00000000 | 0xA00A1064 | 247 |
| 1.9.11 | reg : rt_data_handler_diag_rx_stat | 0x00000000 | 0xA00A1068 | 248 |
| 1.9.12 | reg : rt_data_handler_wfm_reg_rx_stat | 0x00000000 | 0xA00A106C | 249 |
| 1.9.13 | reg : rt_data_handler_vol_wfm_samp_rx_stat | 0x00000000 | 0xA00A1070 | 249 |
| 1.9.14 | reg : rt_data_handler_amp_wfm_samp_rx_stat | 0x00000000 | 0xA00A1074 | 250 |
| 1.9.15 | reg : rt_data_handler_tx_stat | 0x00000000 | 0xA00A1078 | 251 |
| 1.9.16 | reg : ps_por_b | 0x00000000 | 0xA00A107C | 251 |
| 1.9.17 | reg : ps_srst_b | 0x00000000 | 0xA00A1080 | 251 |
| 1.9.18 | reg : enb_wfm_cap | 0x00000000 | 0xA00A1084 | 251 |
| 1.9.19 | reg : direct_boot_offset_set | 0x00000000 | 0xA00A1088 | 252 |
| 1.9.20 | reg : cntrl_pkt_rate_ctrl | 0x03B9ACA0 | 0xA00A108C | 252 |
| 1.9.21 | reg : algo_data_good_frame_cnt | 0x00000000 | 0xA00A1090 | 252 |
| 1.9.22 | reg : algo_data_bad_frame_cnt | 0x00000000 | 0xA00A1094 | 252 |
| 1.9.23 | reg : goodalgo_tsel_pkt_lost_cnt | 0x00000000 | 0xA00A1098 | 252 |
| 1.9.24 | reg : boot_data_good_frame_cnt | 0x00000000 | 0xA00A109C | 252 |
| 1.9.25 | reg : boot_data_bad_frame_cnt | 0x00000000 | 0xA00A10A0 | 252 |
| 1.9.26 | reg : boot_tsel_pkt_lost_cnt | 0x00000000 | 0xA00A10A4 | 252 |
| 1.9.27 | reg : diag_data_good_frame_cnt | 0x00000000 | 0xA00A10A8 | 253 |
| 1.9.28 | reg : diag_data_bad_frame_cnt | 0x00000000 | 0xA00A10AC | 253 |
| 1.9.29 | reg : diag_tsel_pkt_lost_cnt | 0x00000000 | 0xA00A10B0 | 253 |
| 1.9.30 | reg : wfm_reg_data_good_frame_cnt | 0x00000000 | 0xA00A10B4 | 253 |
| 1.9.31 | reg : wfm_reg_data_bad_frame_cnt | 0x00000000 | 0xA00A10B8 | 253 |
| 1.9.32 | reg : wfm_reg_tsel_pkt_lost_cnt | 0x00000000 | 0xA00A10BC | 253 |
| 1.9.33 | reg : vol_wfm_samp_data_good_frame_cnt | 0x00000000 | 0xA00A10C0 | 253 |
| 1.9.34 | reg : vol_wfm_samp_data_bad_frame_cnt | 0x00000000 | 0xA00A10C4 | 253 |
| 1.9.35 | reg : vol_wfm_samp_tsel_pkt_lost_cnt | 0x00000000 | 0xA00A10C8 | 254 |

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|---|---|---|---|---|
| 1.9.36 | reg : amp_wfm_samp_data_good_frame_cnt | 0x00000000 | 0xA00A10CC | 254 |
| 1.9.37 | reg : amp_wfm_samp_data_bad_frame_cnt | 0x00000000 | 0xA00A10D0 | 254 |
| 1.9.38 | reg : amp_wfm_samp_tsel_pkt_lost_cnt | 0x00000000 | 0xA00A10D4 | 254 |
| 1.9.39 | reg : wfm_samp_data_bad_frame_cnt | 0x00000000 | 0xA00A10D8 | 254 |
| 1.9.40 | reg : unknown_pkt_cnt | 0x00000000 | 0xA00A10DC | 254 |
| 1.9.41 | reg : boot_data_sop_err_cnt | 0x00000000 | 0xA00A10E0 | 254 |
| 1.9.42 | reg : boot_data_eop_err_cnt | 0x00000000 | 0xA00A10E4 | 254 |
| 1.9.43 | reg : boot_data_seg_out_of_order_cnt | 0x00000000 | 0xA00A10E8 | 255 |
| 1.9.44 | reg : diag_data_sop_err_cnt | 0x00000000 | 0xA00A10EC | 255 |
| 1.9.45 | reg : diag_data_eop_err_cnt | 0x00000000 | 0xA00A10F0 | 255 |
| 1.9.46 | reg : diag_data_seg_out_of_order_cnt | 0x00000000 | 0xA00A10F4 | 255 |
| 1.9.47 | reg : amp_wfm_samp_sop_err_cnt | 0x00000000 | 0xA00A10F8 | 255 |
| 1.9.48 | reg : amp_wfm_samp_eop_err_cnt | 0x00000000 | 0xA00A10FC | 255 |
| 1.9.49 | reg : amp_wfm_samp_seg_out_of_order_cnt | 0x00000000 | 0xA00A1100 | 255 |
| 1.9.50 | reg : vol_wfm_samp_sop_err_cnt | 0x00000000 | 0xA00A1104 | 255 |
| 1.9.51 | reg : vol_wfm_samp_eop_err_cnt | 0x00000000 | 0xA00A1108 | 256 |
| 1.9.52 | reg : vol_wfm_samp_seg_out_of_order_cnt | 0x00000000 | 0xA00A110C | 256 |
| 1.10 | block : ipi_scratchpad | | 0xA00C0000 - 0xA00FFFFF | 256 |
| 1.10.1 | memory : ram_256kb_inst | | 0xA00C0000, 0xA00C0004 ... 0xA00FFFFF | 256 |
| 1.10.1.1 | reg : ram_256kb_inst | 0x00000000 | 0xA00C0000, 0x0000000000... | |
| 1.11 | block : esm_common_registers | | 0xA0210000 - 0xA021171F | 256 |
| 1.11.1 | reg : esmi_ctl1 | 0x00000001 | 0xA0210000 | 256 |
| 1.11.2 | reg : esmi_cmd1 | 0x00000000 | 0xA0210004 | 258 |
| 1.11.3 | reg : esmi_32dat1 | 0x00000000 | 0xA0210008 | 258 |
| 1.11.4 | reg : esmi_tdly1 | 0x00000021 | 0xA021000C | 259 |
| 1.11.5 | reg : esmi_fncmd1 | 0x00000000 | 0xA0210014 | 259 |
| 1.11.6 | reg : esmi_iacmd1 | 0x00000000 | 0xA0210018 | 259 |
| 1.11.7 | reg : esmi_extdat1 | 0x00000000 | 0xA021001C | 260 |
| 1.11.8 | reg : esmi_ctl2 | 0x00000001 | 0xA0210030 | 260 |
| 1.11.9 | reg : esmi_cmd2 | 0x00000000 | 0xA0210034 | 261 |
| 1.11.10 | reg : esmi_32dat2 | 0x00000000 | 0xA0210038 | 262 |
| 1.11.11 | reg : esmi_tdly2 | 0x00000021 | 0xA021003C | 263 |
| 1.11.12 | reg : esmi_fncmd2 | 0x00000000 | 0xA0210044 | 263 |
| 1.11.13 | reg : esmi_iacmd2 | 0x00000000 | 0xA0210048 | 263 |
| 1.11.14 | reg : esmi_extdat2 | 0x00000000 | 0xA021004C | 263 |
| 1.11.15 | reg : esmi_ctl3 | 0x00000001 | 0xA0210060 | 264 |
| 1.11.16 | reg : esmi_cmd3 | 0x00000000 | 0xA0210064 | 265 |
| 1.11.17 | reg : esmi_32dat3 | 0x00000000 | 0xA0210068 | 266 |
| 1.11.18 | reg : esmi_tdly3 | 0x00000021 | 0xA021006C | 266 |
| 1.11.19 | reg : esmi_fncmd3 | 0x00000000 | 0xA0210074 | 267 |
| 1.11.20 | reg : esmi_iacmd3 | 0x00000000 | 0xA0210078 | 267 |
| 1.11.21 | reg : esmi_extdat3 | 0x00000000 | 0xA021007C | 267 |
| 1.11.22 | reg : esmi_ctl4 | 0x00000001 | 0xA0210090 | 267 |
| 1.11.23 | reg : esmi_cmd4 | 0x00000000 | 0xA0210094 | 269 |
| 1.11.24 | reg : esmi_32dat4 | 0x00000000 | 0xA0210098 | 269 |
| 1.11.25 | reg : esmi_tdly4 | 0x00000021 | 0xA021009C | 270 |

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|---|---|---|---|---|
| 1.11.26 | reg : esmi_fncmd4 | 0x00000000 | 0xA02100A4 | 271 |
| 1.11.27 | reg : esmi_iacmd4 | 0x00000000 | 0xA02100A8 | 271 |
| 1.11.28 | reg : esmi_extdat4 | 0x00000000 | 0xA02100AC | 271 |
| 1.11.29 | reg : esmi_ctl5 | 0x00000001 | 0xA02100C0 | 271 |
| 1.11.30 | reg : esmi_cmd5 | 0x00000000 | 0xA02100C4 | 273 |
| 1.11.31 | reg : esmi_32dat5 | 0x00000000 | 0xA02100C8 | 273 |
| 1.11.32 | reg : esmi_tdly5 | 0x00000021 | 0xA02100CC | 274 |
| 1.11.33 | reg : esmi_fncmd5 | 0x00000000 | 0xA02100D4 | 274 |
| 1.11.34 | reg : esmi_iacmd5 | 0x00000000 | 0xA02100D8 | 275 |
| 1.11.35 | reg : esmi_extdat5 | 0x00000000 | 0xA02100DC | 275 |
| 1.11.36 | reg : esmi_ctl6 | 0x00000001 | 0xA02100F0 | 275 |
| 1.11.37 | reg : esmi_cmd6 | 0x00000000 | 0xA02100F4 | 276 |
| 1.11.38 | reg : esmi_32dat6 | 0x00000000 | 0xA02100F8 | 277 |
| 1.11.39 | reg : esmi_tdly6 | 0x00000021 | 0xA02100FC | 278 |
| 1.11.40 | reg : esmi_fncmd6 | 0x00000000 | 0xA0210104 | 278 |
| 1.11.41 | reg : esmi_iacmd6 | 0x00000000 | 0xA0210108 | 278 |
| 1.11.42 | reg : esmi_extdat6 | 0x00000000 | 0xA021010C | 279 |
| 1.11.43 | reg : esmi_ctl7 | 0x00000001 | 0xA0210120 | 279 |
| 1.11.44 | reg : esmi_cmd7 | 0x00000000 | 0xA0210124 | 280 |
| 1.11.45 | reg : esmi_32dat7 | 0x00000000 | 0xA0210128 | 281 |
| 1.11.46 | reg : esmi_tdly7 | 0x00000021 | 0xA021012C | 282 |
| 1.11.47 | reg : esmi_fncmd7 | 0x00000000 | 0xA0210134 | 282 |
| 1.11.48 | reg : esmi_iacmd7 | 0x00000000 | 0xA0210138 | 282 |
| 1.11.49 | reg : esmi_extdat7 | 0x00000000 | 0xA021013C | 282 |
| 1.11.50 | reg : esmi_ctl8 | 0x00000001 | 0xA0210150 | 283 |
| 1.11.51 | reg : esmi_cmd8 | 0x00000000 | 0xA0210154 | 284 |
| 1.11.52 | reg : esmi_32dat8 | 0x00000000 | 0xA0210158 | 284 |
| 1.11.53 | reg : esmi_tdly8 | 0x00000021 | 0xA021015C | 285 |
| 1.11.54 | reg : esmi_fncmd8 | 0x00000000 | 0xA0210164 | 286 |
| 1.11.55 | reg : esmi_iacmd8 | 0x00000000 | 0xA0210168 | 286 |
| 1.11.56 | reg : esmi_extdat8 | 0x00000000 | 0xA021016C | 286 |
| 1.11.57 | reg : esmi_ctl9 | 0x00000001 | 0xA0210180 | 286 |
| 1.11.58 | reg : esmi_cmd9 | 0x00000000 | 0xA0210184 | 288 |
| 1.11.59 | reg : esmi_32dat9 | 0x00000000 | 0xA0210188 | 288 |
| 1.11.60 | reg : esmi_tdly9 | 0x00000021 | 0xA021018C | 289 |
| 1.11.61 | reg : esmi_fncmd9 | 0x00000000 | 0xA0210194 | 289 |
| 1.11.62 | reg : esmi_iacmd9 | 0x00000000 | 0xA0210198 | 290 |
| 1.11.63 | reg : esmi_extdat9 | 0x00000000 | 0xA021019C | 290 |
| 1.11.64 | reg : esmi_ctl10 | 0x00000001 | 0xA02101B0 | 290 |
| 1.11.65 | reg : esmi_cmd10 | 0x00000000 | 0xA02101B4 | 292 |
| 1.11.66 | reg : esmi_32dat10 | 0x00000000 | 0xA02101B8 | 292 |
| 1.11.67 | reg : esmi_tdly10 | 0x00000021 | 0xA02101BC | 293 |
| 1.11.68 | reg : esmi_fncmd10 | 0x00000000 | 0xA02101C4 | 293 |
| 1.11.69 | reg : esmi_iacmd10 | 0x00000000 | 0xA02101C8 | 293 |
| 1.11.70 | reg : esmi_extdat10 | 0x00000000 | 0xA02101CC | 294 |
| 1.11.71 | reg : esmi_ctl11 | 0x00000001 | 0xA02101E0 | 294 |
| 1.11.72 | reg : esmi_cmd11 | 0x00000000 | 0xA02101E4 | 295 |
| 1.11.73 | reg : esmi_32dat11 | 0x00000000 | 0xA02101E8 | 296 |
| 1.11.74 | reg : esmi_tdly11 | 0x00000021 | 0xA02101EC | 297 |
| 1.11.75 | reg : esmi_fncmd11 | 0x00000000 | 0xA02101F4 | 297 |
| 1.11.76 | reg : esmi_iacmd11 | 0x00000000 | 0xA02101F8 | 297 |
| 1.11.77 | reg : esmi_extdat11 | 0x00000000 | 0xA02101FC | 297 |
| 1.11.78 | reg : esmi_ctl12 | 0x00000001 | 0xA0210210 | 298 |
| 1.11.79 | reg : esmi_cmd12 | 0x00000000 | 0xA0210214 | 299 |
| 1.11.80 | reg : esmi_32dat12 | 0x00000000 | 0xA0210218 | 299 |
| 1.11.81 | reg : esmi_tdly12 | 0x00000021 | 0xA021021C | 300 |
| 1.11.82 | reg : esmi_fncmd12 | 0x00000000 | 0xA0210224 | 301 |
| 1.11.83 | reg : esmi_iacmd12 | 0x00000000 | 0xA0210228 | 301 |
| 1.11.84 | reg : esmi_extdat12 | 0x00000000 | 0xA021022C | 301 |
| 1.11.85 | reg : esmi_ctl13 | 0x00000001 | 0xA0210240 | 301 |
| 1.11.86 | reg : esmi_cmd13 | 0x00000000 | 0xA0210244 | 303 |
| 1.11.87 | reg : esmi_32dat13 | 0x00000000 | 0xA0210248 | 303 |
| 1.11.88 | reg : esmi_tdly13 | 0x00000021 | 0xA021024C | 304 |
| 1.11.89 | reg : esmi_fncmd13 | 0x00000000 | 0xA0210254 | 304 |
| 1.11.90 | reg : esmi_iacmd13 | 0x00000000 | 0xA0210258 | 305 |
| 1.11.91 | reg : esmi_extdat13 | 0x00000000 | 0xA021025C | 305 |

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|---|---|---|---|---|
| 1.11.92 | reg : esmi_ctl14 | 0x00000001 | 0xA0210270 | 305 |
| 1.11.93 | reg : esmi_cmd14 | 0x00000000 | 0xA0210274 | 307 |
| 1.11.94 | reg : esmi_32dat14 | 0x00000000 | 0xA0210278 | 307 |
| 1.11.95 | reg : esmi_tdly14 | 0x00000021 | 0xA021027C | 308 |
| 1.11.96 | reg : esmi_fncmd14 | 0x00000000 | 0xA0210284 | 308 |
| 1.11.97 | reg : esmi_iacmd14 | 0x00000000 | 0xA0210288 | 308 |
| 1.11.98 | reg : esmi_extdat14 | 0x00000000 | 0xA021028C | 309 |
| 1.11.99 | reg : esmi_ctl15 | 0x00000001 | 0xA02102A0 | 309 |
| 1.11.100 | reg : esmi_cmd15 | 0x00000000 | 0xA02102A4 | 310 |
| 1.11.101 | reg : esmi_32dat15 | 0x00000000 | 0xA02102A8 | 311 |
| 1.11.102 | reg : esmi_tdly15 | 0x00000021 | 0xA02102AC | 312 |
| 1.11.103 | reg : esmi_fncmd15 | 0x00000000 | 0xA02102B4 | 312 |
| 1.11.104 | reg : esmi_iacmd15 | 0x00000000 | 0xA02102B8 | 312 |
| 1.11.105 | reg : esmi_extdat15 | 0x00000000 | 0xA02102BC | 312 |
| 1.11.106 | reg : esmi_ctl16 | 0x00000001 | 0xA02102D0 | 313 |
| 1.11.107 | reg : esmi_cmd16 | 0x00000000 | 0xA02102D4 | 314 |
| 1.11.108 | reg : esmi_32dat16 | 0x00000000 | 0xA02102D8 | 315 |
| 1.11.109 | reg : esmi_tdly16 | 0x00000021 | 0xA02102DC | 315 |
| 1.11.110 | reg : esmi_fncmd16 | 0x00000000 | 0xA02102E4 | 316 |
| 1.11.111 | reg : esmi_iacmd16 | 0x00000000 | 0xA02102E8 | 316 |
| 1.11.112 | reg : esmi_extdat16 | 0x00000000 | 0xA02102EC | 316 |
| 1.11.113 | reg : esmi_ctl17 | 0x00000001 | 0xA0210300 | 316 |
| 1.11.114 | reg : esmi_cmd17 | 0x00000000 | 0xA0210304 | 318 |
| 1.11.115 | reg : esmi_32dat17 | 0x00000000 | 0xA0210308 | 318 |
| 1.11.116 | reg : esmi_tdly17 | 0x00000021 | 0xA021030C | 319 |
| 1.11.117 | reg : esmi_fncmd17 | 0x00000000 | 0xA0210314 | 320 |
| 1.11.118 | reg : esmi_iacmd17 | 0x00000000 | 0xA0210318 | 320 |
| 1.11.119 | reg : esmi_extdat17 | 0x00000000 | 0xA021031C | 320 |
| 1.11.120 | reg : esmi_ctl18 | 0x00000001 | 0xA0210330 | 320 |
| 1.11.121 | reg : esmi_cmd18 | 0x00000000 | 0xA0210334 | 322 |
| 1.11.122 | reg : esmi_32dat18 | 0x00000000 | 0xA0210338 | 322 |
| 1.11.123 | reg : esmi_tdly18 | 0x00000021 | 0xA021033C | 323 |
| 1.11.124 | reg : esmi_fncmd18 | 0x00000000 | 0xA0210344 | 323 |
| 1.11.125 | reg : esmi_iacmd18 | 0x00000000 | 0xA0210348 | 324 |
| 1.11.126 | reg : esmi_extdat18 | 0x00000000 | 0xA021034C | 324 |
| 1.11.127 | reg : esmi_ctl19 | 0x00000001 | 0xA0210360 | 324 |
| 1.11.128 | reg : esmi_cmd19 | 0x00000000 | 0xA0210364 | 325 |
| 1.11.129 | reg : esmi_32dat19 | 0x00000000 | 0xA0210368 | 326 |
| 1.11.130 | reg : esmi_tdly19 | 0x00000021 | 0xA021036C | 327 |
| 1.11.131 | reg : esmi_fncmd19 | 0x00000000 | 0xA0210374 | 327 |
| 1.11.132 | reg : esmi_iacmd19 | 0x00000000 | 0xA0210378 | 327 |
| 1.11.133 | reg : esmi_extdat19 | 0x00000000 | 0xA021037C | 328 |
| 1.11.134 | reg : esmi_ctl20 | 0x00000001 | 0xA0210390 | 328 |
| 1.11.135 | reg : esmi_cmd20 | 0x00000000 | 0xA0210394 | 329 |
| 1.11.136 | reg : esmi_32dat20 | 0x00000000 | 0xA0210398 | 330 |
| 1.11.137 | reg : esmi_tdly20 | 0x00000021 | 0xA021039C | 331 |
| 1.11.138 | reg : esmi_fncmd20 | 0x00000000 | 0xA02103A4 | 331 |
| 1.11.139 | reg : esmi_iacmd20 | 0x00000000 | 0xA02103A8 | 331 |
| 1.11.140 | reg : esmi_extdat20 | 0x00000000 | 0xA02103AC | 331 |
| 1.11.141 | reg : esmi_crc | 0x00000000 | 0xA0210700 | 332 |
| 1.11.142 | reg : esmi_crc_sel | 0x00000000 | 0xA0210704 | 332 |
| 1.11.143 | reg : esmi_crc_cnt | 0x00000000 | 0xA0210708 | 332 |
| 1.11.144 | reg : esmi_cab | 0x00000000 | 0xA0210710 | 332 |
| 1.11.145 | reg : spm_cab | 0x00000000 | 0xA0210714 | 332 |
| 1.11.146 | reg : t9_esmi | 0x00000000 | 0xA0210718 | 332 |
| 1.11.147 | reg : nrgy_a1 | 0x00000000 | 0xA0210800 | 332 |
| 1.11.148 | reg : pkamp_a1_pktime_a1 | 0x00000000 | 0xA0210804 | 333 |
| 1.11.149 | reg : nrgy_b1 | 0x00000000 | 0xA0210808 | 334 |
| 1.11.150 | reg : pkamp_b1_pktime_b1 | 0x00000000 | 0xA021080C | 335 |
| 1.11.151 | reg : nrgy_c1 | 0x00000000 | 0xA0210810 | 335 |
| 1.11.152 | reg : pkamp_c1_pktime_c1 | 0x00000000 | 0xA0210814 | 336 |
| 1.11.153 | reg : nrgy_a2 | 0x00000000 | 0xA0210818 | 337 |
| 1.11.154 | reg : pkamp_a2_pktime_a2 | 0x00000000 | 0xA021081C | 338 |
| 1.11.155 | reg : nrgy_b2 | 0x00000000 | 0xA0210820 | 339 |
| 1.11.156 | reg : pkamp_b2_pktime_b2 | 0x00000000 | 0xA0210824 | 339 |
| 1.11.157 | reg : nrgy_c2 | 0x00000000 | 0xA0210828 | 340 |

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|---|---|---|---|---|
| 1.11.158 | reg : pkamp_c2_pktime_c2 | 0x00000000 | 0xA021082C | 341 |
| 1.11.159 | reg : nrgy_a3 | 0x00000000 | 0xA0210830 | 342 |
| 1.11.160 | reg : pkamp_a3_pktime_a3 | 0x00000000 | 0xA0210834 | 342 |
| 1.11.161 | reg : nrgy_b3 | 0x00000000 | 0xA0210838 | 343 |
| 1.11.162 | reg : pkamp_b3_pktime_b3 | 0x00000000 | 0xA021083C | 344 |
| 1.11.163 | reg : nrgy_c3 | 0x00000000 | 0xA0210840 | 345 |
| 1.11.164 | reg : pkamp_c3_pktime_c3 | 0x00000000 | 0xA0210844 | 345 |
| 1.11.165 | reg : nrgy_a4 | 0x00000000 | 0xA0210848 | 346 |
| 1.11.166 | reg : pkamp_a4_pktime_a4 | 0x00000000 | 0xA021084C | 347 |
| 1.11.167 | reg : nrgy_b4 | 0x00000000 | 0xA0210850 | 348 |
| 1.11.168 | reg : pkamp_b4_pktime_b4 | 0x00000000 | 0xA0210854 | 348 |
| 1.11.169 | reg : nrgy_c4 | 0x00000000 | 0xA0210858 | 349 |
| 1.11.170 | reg : pkamp_c4_pktime_c4 | 0x00000000 | 0xA021085C | 350 |
| 1.11.171 | reg : nrgy_a5 | 0x00000000 | 0xA0210860 | 351 |
| 1.11.172 | reg : pkamp_a5_pktime_a5 | 0x00000000 | 0xA0210864 | 351 |
| 1.11.173 | reg : nrgy_b5 | 0x00000000 | 0xA0210868 | 352 |
| 1.11.174 | reg : pkamp_b5_pktime_b5 | 0x00000000 | 0xA021086C | 353 |
| 1.11.175 | reg : nrgy_c5 | 0x00000000 | 0xA0210870 | 354 |
| 1.11.176 | reg : pkamp_c5_pktime_c5 | 0x00000000 | 0xA0210874 | 355 |
| 1.11.177 | reg : nrgy_a6 | 0x00000000 | 0xA0210878 | 355 |
| 1.11.178 | reg : pkamp_a6_pktime_a6 | 0x00000000 | 0xA021087C | 356 |
| 1.11.179 | reg : nrgy_b6 | 0x00000000 | 0xA0210880 | 357 |
| 1.11.180 | reg : pkamp_b6_pktime_b6 | 0x00000000 | 0xA0210884 | 358 |
| 1.11.181 | reg : nrgy_c6 | 0x00000000 | 0xA0210888 | 358 |
| 1.11.182 | reg : pkamp_c6_pktime_c6 | 0x00000000 | 0xA021088C | 359 |
| 1.11.183 | reg : nrgy_a7 | 0x00000000 | 0xA0210890 | 360 |
| 1.11.184 | reg : pkamp_a7_pktime_a7 | 0x00000000 | 0xA0210894 | 361 |
| 1.11.185 | reg : nrgy_b7 | 0x00000000 | 0xA0210898 | 361 |
| 1.11.186 | reg : pkamp_b7_pktime_b7 | 0x00000000 | 0xA021089C | 362 |
| 1.11.187 | reg : nrgy_c7 | 0x00000000 | 0xA02108A0 | 363 |
| 1.11.188 | reg : pkamp_c7_pktime_c7 | 0x00000000 | 0xA02108A4 | 364 |
| 1.11.189 | reg : nrgy_a8 | 0x00000000 | 0xA02108A8 | 365 |
| 1.11.190 | reg : pkamp_a8_pktime_a8 | 0x00000000 | 0xA02108AC | 365 |
| 1.11.191 | reg : nrgy_b8 | 0x00000000 | 0xA02108B0 | 366 |
| 1.11.192 | reg : pkamp_b8_pktime_b8 | 0x00000000 | 0xA02108B4 | 367 |
| 1.11.193 | reg : nrgy_c8 | 0x00000000 | 0xA02108B8 | 368 |
| 1.11.194 | reg : pkamp_c8_pktime_c8 | 0x00000000 | 0xA02108BC | 368 |
| 1.11.195 | reg : nrgy_a9 | 0x00000000 | 0xA02108C0 | 369 |
| 1.11.196 | reg : pkamp_a9_pktime_a9 | 0x00000000 | 0xA02108C4 | 370 |
| 1.11.197 | reg : nrgy_b9 | 0x00000000 | 0xA02108C8 | 371 |
| 1.11.198 | reg : pkamp_b9_pktime_b9 | 0x00000000 | 0xA02108CC | 371 |
| 1.11.199 | reg : nrgy_c9 | 0x00000000 | 0xA02108D0 | 372 |
| 1.11.200 | reg : pkamp_c9_pktime_c9 | 0x00000000 | 0xA02108D4 | 373 |
| 1.11.201 | reg : nrgy_a10 | 0x00000000 | 0xA02108D8 | 374 |
| 1.11.202 | reg : pkamp_a10_pktime_a10 | 0x00000000 | 0xA02108DC | 374 |
| 1.11.203 | reg : nrgy_b10 | 0x00000000 | 0xA02108E0 | 375 |
| 1.11.204 | reg : pkamp_b10_pktime_b10 | 0x00000000 | 0xA02108E4 | 376 |
| 1.11.205 | reg : nrgy_c10 | 0x00000000 | 0xA02108E8 | 377 |
| 1.11.206 | reg : pkamp_c10_pktime_c10 | 0x00000000 | 0xA02108EC | 377 |
| 1.11.207 | reg : nrgy_a11 | 0x00000000 | 0xA02108F0 | 378 |
| 1.11.208 | reg : pkamp_a11_pktime_a11 | 0x00000000 | 0xA02108F4 | 379 |
| 1.11.209 | reg : nrgy_b11 | 0x00000000 | 0xA02108F8 | 380 |
| 1.11.210 | reg : pkamp_b11_pktime_b11 | 0x00000000 | 0xA02108FC | 381 |
| 1.11.211 | reg : nrgy_c11 | 0x00000000 | 0xA0210900 | 381 |
| 1.11.212 | reg : pkamp_c11_pktime_c11 | 0x00000000 | 0xA0210904 | 382 |
| 1.11.213 | reg : nrgy_a12 | 0x00000000 | 0xA0210908 | 383 |
| 1.11.214 | reg : pkamp_a12_pktime_a12 | 0x00000000 | 0xA021090C | 384 |
| 1.11.215 | reg : nrgy_b12 | 0x00000000 | 0xA0210910 | 384 |
| 1.11.216 | reg : pkamp_b12_pktime_b12 | 0x00000000 | 0xA0210914 | 385 |
| 1.11.217 | reg : nrgy_c12 | 0x00000000 | 0xA0210918 | 386 |
| 1.11.218 | reg : pkamp_c12_pktime_c12 | 0x00000000 | 0xA021091C | 387 |
| 1.11.219 | reg : nrgy_a13 | 0x00000000 | 0xA0210920 | 387 |
| 1.11.220 | reg : pkamp_a13_pktime_a13 | 0x00000000 | 0xA0210924 | 388 |
| 1.11.221 | reg : nrgy_b13 | 0x00000000 | 0xA0210928 | 389 |
| 1.11.222 | reg : pkamp_b13_pktime_b13 | 0x00000000 | 0xA021092C | 390 |
| 1.11.223 | reg : nrgy_c13 | 0x00000000 | 0xA0210930 | 391 |

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| 1.11.224 | reg : pkamp_c13_pktime_c13 | 0x00000000 | 0xA0210934 | 391 |
| 1.11.225 | reg : nrgy_a14 | 0x00000000 | 0xA0210938 | 392 |
| 1.11.226 | reg : pkamp_a14_pktime_a14 | 0x00000000 | 0xA021093C | 393 |
| 1.11.227 | reg : nrgy_b14 | 0x00000000 | 0xA0210940 | 394 |
| 1.11.228 | reg : pkamp_b14_pktime_b14 | 0x00000000 | 0xA0210944 | 394 |
| 1.11.229 | reg : nrgy_c14 | 0x00000000 | 0xA0210948 | 395 |
| 1.11.230 | reg : pkamp_c14_pktime_c14 | 0x00000000 | 0xA021094C | 396 |
| 1.11.231 | reg : nrgy_a15 | 0x00000000 | 0xA0210950 | 397 |
| 1.11.232 | reg : pkamp_a15_pktime_a15 | 0x00000000 | 0xA0210954 | 397 |
| 1.11.233 | reg : nrgy_b15 | 0x00000000 | 0xA0210958 | 398 |
| 1.11.234 | reg : pkamp_b15_pktime_b15 | 0x00000000 | 0xA021095C | 399 |
| 1.11.235 | reg : nrgy_c15 | 0x00000000 | 0xA0210960 | 400 |
| 1.11.236 | reg : pkamp_c15_pktime_c15 | 0x00000000 | 0xA0210964 | 400 |
| 1.11.237 | reg : nrgy_a16 | 0x00000000 | 0xA0210968 | 401 |
| 1.11.238 | reg : pkamp_a16_pktime_a16 | 0x00000000 | 0xA021096C | 402 |
| 1.11.239 | reg : nrgy_b16 | 0x00000000 | 0xA0210970 | 403 |
| 1.11.240 | reg : pkamp_b16_pktime_b16 | 0x00000000 | 0xA0210974 | 403 |
| 1.11.241 | reg : nrgy_c16 | 0x00000000 | 0xA0210978 | 404 |
| 1.11.242 | reg : pkamp_c16_pktime_c16 | 0x00000000 | 0xA021097C | 405 |
| 1.11.243 | reg : nrgy_a17 | 0x00000000 | 0xA0210980 | 406 |
| 1.11.244 | reg : pkamp_a17_pktime_a17 | 0x00000000 | 0xA0210984 | 407 |
| 1.11.245 | reg : nrgy_b17 | 0x00000000 | 0xA0210988 | 407 |
| 1.11.246 | reg : pkamp_b17_pktime_b17 | 0x00000000 | 0xA021098C | 408 |
| 1.11.247 | reg : nrgy_c17 | 0x00000000 | 0xA0210990 | 409 |
| 1.11.248 | reg : pkamp_c17_pktime_c17 | 0x00000000 | 0xA0210994 | 410 |
| 1.11.249 | reg : nrgy_a18 | 0x00000000 | 0xA0210998 | 410 |
| 1.11.250 | reg : pkamp_a18_pktime_a18 | 0x00000000 | 0xA021099C | 411 |
| 1.11.251 | reg : nrgy_b18 | 0x00000000 | 0xA02109A0 | 412 |
| 1.11.252 | reg : pkamp_b18_pktime_b18 | 0x00000000 | 0xA02109A4 | 413 |
| 1.11.253 | reg : nrgy_c18 | 0x00000000 | 0xA02109A8 | 413 |
| 1.11.254 | reg : pkamp_c18_pktime_c18 | 0x00000000 | 0xA02109AC | 414 |
| 1.11.255 | reg : nrgy_a19 | 0x00000000 | 0xA02109B0 | 415 |
| 1.11.256 | reg : pkamp_a19_pktime_a19 | 0x00000000 | 0xA02109B4 | 416 |
| 1.11.257 | reg : nrgy_b19 | 0x00000000 | 0xA02109B8 | 417 |
| 1.11.258 | reg : pkamp_b19_pktime_b19 | 0x00000000 | 0xA02109BC | 417 |
| 1.11.259 | reg : nrgy_c19 | 0x00000000 | 0xA02109C0 | 418 |
| 1.11.260 | reg : pkamp_c19_pktime_c19 | 0x00000000 | 0xA02109C4 | 419 |
| 1.11.261 | reg : nrgy_a20 | 0x00000000 | 0xA02109C8 | 420 |
| 1.11.262 | reg : pkamp_a20_pktime_a20 | 0x00000000 | 0xA02109CC | 420 |
| 1.11.263 | reg : nrgy_b20 | 0x00000000 | 0xA02109D0 | 421 |
| 1.11.264 | reg : pkamp_b20_pktime_b20 | 0x00000000 | 0xA02109D4 | 422 |
| 1.11.265 | reg : nrgy_c20 | 0x00000000 | 0xA02109D8 | 423 |
| 1.11.266 | reg : pkamp_c20_pktime_c20 | 0x00000000 | 0xA02109DC | 423 |
| 1.11.267 | reg : ffa_lk | 0x00000000 | 0xA0210FCC | 424 |
| 1.11.268 | reg : ffa_s1_x | 0x00000000 | 0xA0210FD0 | 425 |
| 1.11.269 | reg : ffa_s1_y | 0x00000000 | 0xA0210FD4 | 425 |
| 1.11.270 | reg : ffa_s1_sum | 0x00000000 | 0xA0210FD8 | 425 |
| 1.11.271 | reg : ffa_s2_x | 0x00000000 | 0xA0210FDC | 425 |
| 1.11.272 | reg : ffa_s2_y | 0x00000000 | 0xA0210FE0 | 425 |
| 1.11.273 | reg : ffa_s2_sum | 0x00000000 | 0xA0210FE4 | 425 |
| 1.11.274 | reg : quadcell_read_sel | 0x00000000 | 0xA0210FE8 | 426 |
| 1.11.275 | reg : debug_wave | 0x00000000 | 0xA0210FEC | 426 |
| 1.11.276 | reg : wave_pkt_cnt | 0x00000000 | 0xA0210FF0 | 426 |
| 1.11.277 | reg : map4_hop | 0x00000000 | 0xA0210FF4 | 426 |
| 1.11.278 | reg : map4_latch_time | 0x00000000 | 0xA0210FF8 | 426 |
| 1.11.279 | reg : map4_keep_time | 0x000007D0 | 0xA0210FFC | 426 |
| 1.11.280 | reg : esmi_s0_cnt1 | 0x00000000 | 0xA0211000 | 427 |
| 1.11.281 | reg : esmi_s0_crc1 | 0x00000000 | 0xA0211004 | 427 |
| 1.11.282 | reg : esmi_s1_cnt1 | 0x00000000 | 0xA0211008 | 427 |
| 1.11.283 | reg : esmi_s1_crc1 | 0x00000000 | 0xA021100C | 427 |
| 1.11.284 | reg : esmi_s2_cnt1 | 0x00000000 | 0xA0211010 | 427 |
| 1.11.285 | reg : esmi_s2_crc1 | 0x00000000 | 0xA0211014 | 427 |
| 1.11.286 | reg : esmi_s7_cnt1 | 0x00000000 | 0xA0211018 | 427 |
| 1.11.287 | reg : esmi_s7_crc1 | 0x00000000 | 0xA021101C | 428 |
| 1.11.288 | reg : esmi_rd_cnt1 | 0x00000000 | 0xA0211020 | 428 |
| 1.11.289 | reg : esmi_rd_crc1 | 0x00000000 | 0xA0211024 | 428 |

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|---|---|---|---|---|
| 1.11.290 | reg : esmi_da_cnt1 | 0x00000000 | 0xA0211028 | 428 |
| 1.11.291 | reg : esmi_ia_cnt1 | 0x00000000 | 0xA021102C | 428 |
| 1.11.292 | reg : esmi_tcmd_cnt1 | 0x00000000 | 0xA0211030 | 428 |
| 1.11.293 | reg : esmi_twcmd_cnt1 | 0x00000000 | 0xA0211034 | 428 |
| 1.11.294 | reg : esmi_dm_cnt1 | 0x00000000 | 0xA0211038 | 429 |
| 1.11.295 | reg : esmi_s0_cnt2 | 0x00000000 | 0xA0211040 | 429 |
| 1.11.296 | reg : esmi_s0_crc2 | 0x00000000 | 0xA0211044 | 429 |
| 1.11.297 | reg : esmi_s1_cnt2 | 0x00000000 | 0xA0211048 | 429 |
| 1.11.298 | reg : esmi_s1_crc2 | 0x00000000 | 0xA021104C | 429 |
| 1.11.299 | reg : esmi_s2_cnt2 | 0x00000000 | 0xA0211050 | 429 |
| 1.11.300 | reg : esmi_s2_crc2 | 0x00000000 | 0xA0211054 | 429 |
| 1.11.301 | reg : esmi_s7_cnt2 | 0x00000000 | 0xA0211058 | 429 |
| 1.11.302 | reg : esmi_s7_crc2 | 0x00000000 | 0xA021105C | 430 |
| 1.11.303 | reg : esmi_rd_cnt2 | 0x00000000 | 0xA0211060 | 430 |
| 1.11.304 | reg : esmi_rd_crc2 | 0x00000000 | 0xA0211064 | 430 |
| 1.11.305 | reg : esmi_da_cnt2 | 0x00000000 | 0xA0211068 | 430 |
| 1.11.306 | reg : esmi_ia_cnt2 | 0x00000000 | 0xA021106C | 430 |
| 1.11.307 | reg : esmi_tcmd_cnt2 | 0x00000000 | 0xA0211070 | 430 |
| 1.11.308 | reg : esmi_twcmd_cnt2 | 0x00000000 | 0xA0211074 | 430 |
| 1.11.309 | reg : esmi_dm_cnt2 | 0x00000000 | 0xA0211078 | 430 |
| 1.11.310 | reg : esmi_s0_cnt3 | 0x00000000 | 0xA0211080 | 431 |
| 1.11.311 | reg : esmi_s0_crc3 | 0x00000000 | 0xA0211084 | 431 |
| 1.11.312 | reg : esmi_s1_cnt3 | 0x00000000 | 0xA0211088 | 431 |
| 1.11.313 | reg : esmi_s1_crc3 | 0x00000000 | 0xA021108C | 431 |
| 1.11.314 | reg : esmi_s2_cnt3 | 0x00000000 | 0xA0211090 | 431 |
| 1.11.315 | reg : esmi_s2_crc3 | 0x00000000 | 0xA0211094 | 431 |
| 1.11.316 | reg : esmi_s7_cnt3 | 0x00000000 | 0xA0211098 | 431 |
| 1.11.317 | reg : esmi_s7_crc3 | 0x00000000 | 0xA021109C | 432 |
| 1.11.318 | reg : esmi_rd_cnt3 | 0x00000000 | 0xA02110A0 | 432 |
| 1.11.319 | reg : esmi_rd_crc3 | 0x00000000 | 0xA02110A4 | 432 |
| 1.11.320 | reg : esmi_da_cnt3 | 0x00000000 | 0xA02110A8 | 432 |
| 1.11.321 | reg : esmi_ia_cnt3 | 0x00000000 | 0xA02110AC | 432 |
| 1.11.322 | reg : esmi_tcmd_cnt3 | 0x00000000 | 0xA02110B0 | 432 |
| 1.11.323 | reg : esmi_twcmd_cnt3 | 0x00000000 | 0xA02110B4 | 432 |
| 1.11.324 | reg : esmi_dm_cnt3 | 0x00000000 | 0xA02110B8 | 432 |
| 1.11.325 | reg : esmi_s0_cnt4 | 0x00000000 | 0xA02110C0 | 433 |
| 1.11.326 | reg : esmi_s0_crc4 | 0x00000000 | 0xA02110C4 | 433 |
| 1.11.327 | reg : esmi_s1_cnt4 | 0x00000000 | 0xA02110C8 | 433 |
| 1.11.328 | reg : esmi_s1_crc4 | 0x00000000 | 0xA02110CC | 433 |
| 1.11.329 | reg : esmi_s2_cnt4 | 0x00000000 | 0xA02110D0 | 433 |
| 1.11.330 | reg : esmi_s2_crc4 | 0x00000000 | 0xA02110D4 | 433 |
| 1.11.331 | reg : esmi_s7_cnt4 | 0x00000000 | 0xA02110D8 | 433 |
| 1.11.332 | reg : esmi_s7_crc4 | 0x00000000 | 0xA02110DC | 433 |
| 1.11.333 | reg : esmi_rd_cnt4 | 0x00000000 | 0xA02110E0 | 434 |
| 1.11.334 | reg : esmi_rd_crc4 | 0x00000000 | 0xA02110E4 | 434 |
| 1.11.335 | reg : esmi_da_cnt4 | 0x00000000 | 0xA02110E8 | 434 |
| 1.11.336 | reg : esmi_ia_cnt4 | 0x00000000 | 0xA02110EC | 434 |
| 1.11.337 | reg : esmi_tcmd_cnt4 | 0x00000000 | 0xA02110F0 | 434 |
| 1.11.338 | reg : esmi_twcmd_cnt4 | 0x00000000 | 0xA02110F4 | 434 |
| 1.11.339 | reg : esmi_dm_cnt4 | 0x00000000 | 0xA02110F8 | 434 |
| 1.11.340 | reg : esmi_s0_cnt5 | 0x00000000 | 0xA0211100 | 435 |
| 1.11.341 | reg : esmi_s0_crc5 | 0x00000000 | 0xA0211104 | 435 |
| 1.11.342 | reg : esmi_s1_cnt5 | 0x00000000 | 0xA0211108 | 435 |
| 1.11.343 | reg : esmi_s1_crc5 | 0x00000000 | 0xA021110C | 435 |
| 1.11.344 | reg : esmi_s2_cnt5 | 0x00000000 | 0xA0211110 | 435 |
| 1.11.345 | reg : esmi_s2_crc5 | 0x00000000 | 0xA0211114 | 435 |
| 1.11.346 | reg : esmi_s7_cnt5 | 0x00000000 | 0xA0211118 | 435 |
| 1.11.347 | reg : esmi_s7_crc5 | 0x00000000 | 0xA021111C | 435 |
| 1.11.348 | reg : esmi_rd_cnt5 | 0x00000000 | 0xA0211120 | 436 |
| 1.11.349 | reg : esmi_rd_crc5 | 0x00000000 | 0xA0211124 | 436 |
| 1.11.350 | reg : esmi_da_cnt5 | 0x00000000 | 0xA0211128 | 436 |
| 1.11.351 | reg : esmi_ia_cnt5 | 0x00000000 | 0xA021112C | 436 |
| 1.11.352 | reg : esmi_tcmd_cnt5 | 0x00000000 | 0xA0211130 | 436 |
| 1.11.353 | reg : esmi_twcmd_cnt5 | 0x00000000 | 0xA0211134 | 436 |
| 1.11.354 | reg : esmi_dm_cnt5 | 0x00000000 | 0xA0211138 | 436 |
| 1.11.355 | reg : esmi_s0_cnt6 | 0x00000000 | 0xA0211140 | 436 |

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|---|---|---|---|---|
| 1.11.356 | reg : esmi_s0_crc6 | 0x00000000 | 0xA0211144 | 437 |
| 1.11.357 | reg : esmi_s1_cnt6 | 0x00000000 | 0xA0211148 | 437 |
| 1.11.358 | reg : esmi_s1_crc6 | 0x00000000 | 0xA021114C | 437 |
| 1.11.359 | reg : esmi_s2_cnt6 | 0x00000000 | 0xA0211150 | 437 |
| 1.11.360 | reg : esmi_s2_crc6 | 0x00000000 | 0xA0211154 | 437 |
| 1.11.361 | reg : esmi_s7_cnt6 | 0x00000000 | 0xA0211158 | 437 |
| 1.11.362 | reg : esmi_s7_crc6 | 0x00000000 | 0xA021115C | 437 |
| 1.11.363 | reg : esmi_rd_cnt6 | 0x00000000 | 0xA0211160 | 438 |
| 1.11.364 | reg : esmi_rd_crc6 | 0x00000000 | 0xA0211164 | 438 |
| 1.11.365 | reg : esmi_da_cnt6 | 0x00000000 | 0xA0211168 | 438 |
| 1.11.366 | reg : esmi_ia_cnt6 | 0x00000000 | 0xA021116C | 438 |
| 1.11.367 | reg : esmi_tcmd_cnt6 | 0x00000000 | 0xA0211170 | 438 |
| 1.11.368 | reg : esmi_twcmd_cnt6 | 0x00000000 | 0xA0211174 | 438 |
| 1.11.369 | reg : esmi_dm_cnt6 | 0x00000000 | 0xA0211178 | 438 |
| 1.11.370 | reg : esmi_s0_cnt7 | 0x00000000 | 0xA0211180 | 438 |
| 1.11.371 | reg : esmi_s0_crc7 | 0x00000000 | 0xA0211184 | 439 |
| 1.11.372 | reg : esmi_s1_cnt7 | 0x00000000 | 0xA0211188 | 439 |
| 1.11.373 | reg : esmi_s1_crc7 | 0x00000000 | 0xA021118C | 439 |
| 1.11.374 | reg : esmi_s2_cnt7 | 0x00000000 | 0xA0211190 | 439 |
| 1.11.375 | reg : esmi_s2_crc7 | 0x00000000 | 0xA0211194 | 439 |
| 1.11.376 | reg : esmi_s7_cnt7 | 0x00000000 | 0xA0211198 | 439 |
| 1.11.377 | reg : esmi_s7_crc7 | 0x00000000 | 0xA021119C | 439 |
| 1.11.378 | reg : esmi_rd_cnt7 | 0x00000000 | 0xA02111A0 | 439 |
| 1.11.379 | reg : esmi_rd_crc7 | 0x00000000 | 0xA02111A4 | 440 |
| 1.11.380 | reg : esmi_da_cnt7 | 0x00000000 | 0xA02111A8 | 440 |
| 1.11.381 | reg : esmi_ia_cnt7 | 0x00000000 | 0xA02111AC | 440 |
| 1.11.382 | reg : esmi_tcmd_cnt7 | 0x00000000 | 0xA02111B0 | 440 |
| 1.11.383 | reg : esmi_twcmd_cnt7 | 0x00000000 | 0xA02111B4 | 440 |
| 1.11.384 | reg : esmi_dm_cnt7 | 0x00000000 | 0xA02111B8 | 440 |
| 1.11.385 | reg : esmi_s0_cnt8 | 0x00000000 | 0xA02111C0 | 440 |
| 1.11.386 | reg : esmi_s0_crc8 | 0x00000000 | 0xA02111C4 | 441 |
| 1.11.387 | reg : esmi_s1_cnt8 | 0x00000000 | 0xA02111C8 | 441 |
| 1.11.388 | reg : esmi_s1_crc8 | 0x00000000 | 0xA02111CC | 441 |
| 1.11.389 | reg : esmi_s2_cnt8 | 0x00000000 | 0xA02111D0 | 441 |
| 1.11.390 | reg : esmi_s2_crc8 | 0x00000000 | 0xA02111D4 | 441 |
| 1.11.391 | reg : esmi_s7_cnt8 | 0x00000000 | 0xA02111D8 | 441 |
| 1.11.392 | reg : esmi_s7_crc8 | 0x00000000 | 0xA02111DC | 441 |
| 1.11.393 | reg : esmi_rd_cnt8 | 0x00000000 | 0xA02111E0 | 441 |
| 1.11.394 | reg : esmi_rd_crc8 | 0x00000000 | 0xA02111E4 | 442 |
| 1.11.395 | reg : esmi_da_cnt8 | 0x00000000 | 0xA02111E8 | 442 |
| 1.11.396 | reg : esmi_ia_cnt8 | 0x00000000 | 0xA02111EC | 442 |
| 1.11.397 | reg : esmi_tcmd_cnt8 | 0x00000000 | 0xA02111F0 | 442 |
| 1.11.398 | reg : esmi_twcmd_cnt8 | 0x00000000 | 0xA02111F4 | 442 |
| 1.11.399 | reg : esmi_dm_cnt8 | 0x00000000 | 0xA02111F8 | 442 |
| 1.11.400 | reg : esmi_s0_cnt9 | 0x00000000 | 0xA0211200 | 442 |
| 1.11.401 | reg : esmi_s0_crc9 | 0x00000000 | 0xA0211204 | 442 |
| 1.11.402 | reg : esmi_s1_cnt9 | 0x00000000 | 0xA0211208 | 443 |
| 1.11.403 | reg : esmi_s1_crc9 | 0x00000000 | 0xA021120C | 443 |
| 1.11.404 | reg : esmi_s2_cnt9 | 0x00000000 | 0xA0211210 | 443 |
| 1.11.405 | reg : esmi_s2_crc9 | 0x00000000 | 0xA0211214 | 443 |
| 1.11.406 | reg : esmi_s7_cnt9 | 0x00000000 | 0xA0211218 | 443 |
| 1.11.407 | reg : esmi_s7_crc9 | 0x00000000 | 0xA021121C | 443 |
| 1.11.408 | reg : esmi_rd_cnt9 | 0x00000000 | 0xA0211220 | 443 |
| 1.11.409 | reg : esmi_rd_crc9 | 0x00000000 | 0xA0211224 | 444 |
| 1.11.410 | reg : esmi_da_cnt9 | 0x00000000 | 0xA0211228 | 444 |
| 1.11.411 | reg : esmi_ia_cnt9 | 0x00000000 | 0xA021122C | 444 |
| 1.11.412 | reg : esmi_tcmd_cnt9 | 0x00000000 | 0xA0211230 | 444 |
| 1.11.413 | reg : esmi_twcmd_cnt9 | 0x00000000 | 0xA0211234 | 444 |
| 1.11.414 | reg : esmi_dm_cnt9 | 0x00000000 | 0xA0211238 | 444 |
| 1.11.415 | reg : esmi_s0_cnt10 | 0x00000000 | 0xA0211240 | 444 |
| 1.11.416 | reg : esmi_s0_crc10 | 0x00000000 | 0xA0211244 | 444 |
| 1.11.417 | reg : esmi_s1_cnt10 | 0x00000000 | 0xA0211248 | 445 |
| 1.11.418 | reg : esmi_s1_crc10 | 0x00000000 | 0xA021124C | 445 |
| 1.11.419 | reg : esmi_s2_cnt10 | 0x00000000 | 0xA0211250 | 445 |
| 1.11.420 | reg : esmi_s2_crc10 | 0x00000000 | 0xA0211254 | 445 |
| 1.11.421 | reg : esmi_s7_cnt10 | 0x00000000 | 0xA0211258 | 445 |

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|---|---|---|---|---|
| 1.11.422 | reg : esmi_s7_crc10 | 0x00000000 | 0xA021125C | 445 |
| 1.11.423 | reg : esmi_rd_cnt10 | 0x00000000 | 0xA0211260 | 445 |
| 1.11.424 | reg : esmi_rd_crc10 | 0x00000000 | 0xA0211264 | 445 |
| 1.11.425 | reg : esmi_da_cnt10 | 0x00000000 | 0xA0211268 | 446 |
| 1.11.426 | reg : esmi_ia_cnt10 | 0x00000000 | 0xA021126C | 446 |
| 1.11.427 | reg : esmi_tcmd_cnt10 | 0x00000000 | 0xA0211270 | 446 |
| 1.11.428 | reg : esmi_twcmd_cnt10 | 0x00000000 | 0xA0211274 | 446 |
| 1.11.429 | reg : esmi_dm_cnt10 | 0x00000000 | 0xA0211278 | 446 |
| 1.11.430 | reg : esmi_s0_cnt11 | 0x00000000 | 0xA0211280 | 446 |
| 1.11.431 | reg : esmi_s0_crc11 | 0x00000000 | 0xA0211284 | 446 |
| 1.11.432 | reg : esmi_s1_cnt11 | 0x00000000 | 0xA0211288 | 447 |
| 1.11.433 | reg : esmi_s1_crc11 | 0x00000000 | 0xA021128C | 447 |
| 1.11.434 | reg : esmi_s2_cnt11 | 0x00000000 | 0xA0211290 | 447 |
| 1.11.435 | reg : esmi_s2_crc11 | 0x00000000 | 0xA0211294 | 447 |
| 1.11.436 | reg : esmi_s7_cnt11 | 0x00000000 | 0xA0211298 | 447 |
| 1.11.437 | reg : esmi_s7_crc11 | 0x00000000 | 0xA021129C | 447 |
| 1.11.438 | reg : esmi_rd_cnt11 | 0x00000000 | 0xA02112A0 | 447 |
| 1.11.439 | reg : esmi_rd_crc11 | 0x00000000 | 0xA02112A4 | 447 |
| 1.11.440 | reg : esmi_da_cnt11 | 0x00000000 | 0xA02112A8 | 448 |
| 1.11.441 | reg : esmi_ia_cnt11 | 0x00000000 | 0xA02112AC | 448 |
| 1.11.442 | reg : esmi_tcmd_cnt11 | 0x00000000 | 0xA02112B0 | 448 |
| 1.11.443 | reg : esmi_twcmd_cnt11 | 0x00000000 | 0xA02112B4 | 448 |
| 1.11.444 | reg : esmi_dm_cnt11 | 0x00000000 | 0xA02112B8 | 448 |
| 1.11.445 | reg : esmi_s0_cnt12 | 0x00000000 | 0xA02112C0 | 448 |
| 1.11.446 | reg : esmi_s0_crc12 | 0x00000000 | 0xA02112C4 | 448 |
| 1.11.447 | reg : esmi_s1_cnt12 | 0x00000000 | 0xA02112C8 | 448 |
| 1.11.448 | reg : esmi_s1_crc12 | 0x00000000 | 0xA02112CC | 449 |
| 1.11.449 | reg : esmi_s2_cnt12 | 0x00000000 | 0xA02112D0 | 449 |
| 1.11.450 | reg : esmi_s2_crc12 | 0x00000000 | 0xA02112D4 | 449 |
| 1.11.451 | reg : esmi_s7_cnt12 | 0x00000000 | 0xA02112D8 | 449 |
| 1.11.452 | reg : esmi_s7_crc12 | 0x00000000 | 0xA02112DC | 449 |
| 1.11.453 | reg : esmi_rd_cnt12 | 0x00000000 | 0xA02112E0 | 449 |
| 1.11.454 | reg : esmi_rd_crc12 | 0x00000000 | 0xA02112E4 | 449 |
| 1.11.455 | reg : esmi_da_cnt12 | 0x00000000 | 0xA02112E8 | 450 |
| 1.11.456 | reg : esmi_ia_cnt12 | 0x00000000 | 0xA02112EC | 450 |
| 1.11.457 | reg : esmi_tcmd_cnt12 | 0x00000000 | 0xA02112F0 | 450 |
| 1.11.458 | reg : esmi_twcmd_cnt12 | 0x00000000 | 0xA02112F4 | 450 |
| 1.11.459 | reg : esmi_dm_cnt12 | 0x00000000 | 0xA02112F8 | 450 |
| 1.11.460 | reg : esmi_s0_cnt13 | 0x00000000 | 0xA0211300 | 450 |
| 1.11.461 | reg : esmi_s0_crc13 | 0x00000000 | 0xA0211304 | 450 |
| 1.11.462 | reg : esmi_s1_cnt13 | 0x00000000 | 0xA0211308 | 450 |
| 1.11.463 | reg : esmi_s1_crc13 | 0x00000000 | 0xA021130C | 451 |
| 1.11.464 | reg : esmi_s2_cnt13 | 0x00000000 | 0xA0211310 | 451 |
| 1.11.465 | reg : esmi_s2_crc13 | 0x00000000 | 0xA0211314 | 451 |
| 1.11.466 | reg : esmi_s7_cnt13 | 0x00000000 | 0xA0211318 | 451 |
| 1.11.467 | reg : esmi_s7_crc13 | 0x00000000 | 0xA021131C | 451 |
| 1.11.468 | reg : esmi_rd_cnt13 | 0x00000000 | 0xA0211320 | 451 |
| 1.11.469 | reg : esmi_rd_crc13 | 0x00000000 | 0xA0211324 | 451 |
| 1.11.470 | reg : esmi_da_cnt13 | 0x00000000 | 0xA0211328 | 451 |
| 1.11.471 | reg : esmi_ia_cnt13 | 0x00000000 | 0xA021132C | 452 |
| 1.11.472 | reg : esmi_tcmd_cnt13 | 0x00000000 | 0xA0211330 | 452 |
| 1.11.473 | reg : esmi_twcmd_cnt13 | 0x00000000 | 0xA0211334 | 452 |
| 1.11.474 | reg : esmi_dm_cnt13 | 0x00000000 | 0xA0211338 | 452 |
| 1.11.475 | reg : esmi_s0_cnt14 | 0x00000000 | 0xA0211340 | 452 |
| 1.11.476 | reg : esmi_s0_crc14 | 0x00000000 | 0xA0211344 | 452 |
| 1.11.477 | reg : esmi_s1_cnt14 | 0x00000000 | 0xA0211348 | 452 |
| 1.11.478 | reg : esmi_s1_crc14 | 0x00000000 | 0xA021134C | 453 |
| 1.11.479 | reg : esmi_s2_cnt14 | 0x00000000 | 0xA0211350 | 453 |
| 1.11.480 | reg : esmi_s2_crc14 | 0x00000000 | 0xA0211354 | 453 |
| 1.11.481 | reg : esmi_s7_cnt14 | 0x00000000 | 0xA0211358 | 453 |
| 1.11.482 | reg : esmi_s7_crc14 | 0x00000000 | 0xA021135C | 453 |
| 1.11.483 | reg : esmi_rd_cnt14 | 0x00000000 | 0xA0211360 | 453 |
| 1.11.484 | reg : esmi_rd_crc14 | 0x00000000 | 0xA0211364 | 453 |
| 1.11.485 | reg : esmi_da_cnt14 | 0x00000000 | 0xA0211368 | 453 |
| 1.11.486 | reg : esmi_ia_cnt14 | 0x00000000 | 0xA021136C | 454 |
| 1.11.487 | reg : esmi_tcmd_cnt14 | 0x00000000 | 0xA0211370 | 454 |

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|---|---|---|---|---|
| 1.11.488 | reg : esmi_twcmd_cnt14 | 0x00000000 | 0xA0211374 | 454 |
| 1.11.489 | reg : esmi_dm_cnt14 | 0x00000000 | 0xA0211378 | 454 |
| 1.11.490 | reg : esmi_s0_cnt15 | 0x00000000 | 0xA0211380 | 454 |
| 1.11.491 | reg : esmi_s0_crc15 | 0x00000000 | 0xA0211384 | 454 |
| 1.11.492 | reg : esmi_s1_cnt15 | 0x00000000 | 0xA0211388 | 454 |
| 1.11.493 | reg : esmi_s1_crc15 | 0x00000000 | 0xA021138C | 454 |
| 1.11.494 | reg : esmi_s2_cnt15 | 0x00000000 | 0xA0211390 | 455 |
| 1.11.495 | reg : esmi_s2_crc15 | 0x00000000 | 0xA0211394 | 455 |
| 1.11.496 | reg : esmi_s7_cnt15 | 0x00000000 | 0xA0211398 | 455 |
| 1.11.497 | reg : esmi_s7_crc15 | 0x00000000 | 0xA021139C | 455 |
| 1.11.498 | reg : esmi_rd_cnt15 | 0x00000000 | 0xA02113A0 | 455 |
| 1.11.499 | reg : esmi_rd_crc15 | 0x00000000 | 0xA02113A4 | 455 |
| 1.11.500 | reg : esmi_da_cnt15 | 0x00000000 | 0xA02113A8 | 455 |
| 1.11.501 | reg : esmi_ia_cnt15 | 0x00000000 | 0xA02113AC | 456 |
| 1.11.502 | reg : esmi_tcmd_cnt15 | 0x00000000 | 0xA02113B0 | 456 |
| 1.11.503 | reg : esmi_twcmd_cnt15 | 0x00000000 | 0xA02113B4 | 456 |
| 1.11.504 | reg : esmi_dm_cnt15 | 0x00000000 | 0xA02113B8 | 456 |
| 1.11.505 | reg : esmi_s0_cnt16 | 0x00000000 | 0xA02113C0 | 456 |
| 1.11.506 | reg : esmi_s0_crc16 | 0x00000000 | 0xA02113C4 | 456 |
| 1.11.507 | reg : esmi_s1_cnt16 | 0x00000000 | 0xA02113C8 | 456 |
| 1.11.508 | reg : esmi_s1_crc16 | 0x00000000 | 0xA02113CC | 456 |
| 1.11.509 | reg : esmi_s2_cnt16 | 0x00000000 | 0xA02113D0 | 457 |
| 1.11.510 | reg : esmi_s2_crc16 | 0x00000000 | 0xA02113D4 | 457 |
| 1.11.511 | reg : esmi_s7_cnt16 | 0x00000000 | 0xA02113D8 | 457 |
| 1.11.512 | reg : esmi_s7_crc16 | 0x00000000 | 0xA02113DC | 457 |
| 1.11.513 | reg : esmi_rd_cnt16 | 0x00000000 | 0xA02113E0 | 457 |
| 1.11.514 | reg : esmi_rd_crc16 | 0x00000000 | 0xA02113E4 | 457 |
| 1.11.515 | reg : esmi_da_cnt16 | 0x00000000 | 0xA02113E8 | 457 |
| 1.11.516 | reg : esmi_ia_cnt16 | 0x00000000 | 0xA02113EC | 457 |
| 1.11.517 | reg : esmi_tcmd_cnt16 | 0x00000000 | 0xA02113F0 | 458 |
| 1.11.518 | reg : esmi_twcmd_cnt16 | 0x00000000 | 0xA02113F4 | 458 |
| 1.11.519 | reg : esmi_dm_cnt16 | 0x00000000 | 0xA02113F8 | 458 |
| 1.11.520 | reg : esmi_s0_cnt17 | 0x00000000 | 0xA0211400 | 458 |
| 1.11.521 | reg : esmi_s0_crc17 | 0x00000000 | 0xA0211404 | 458 |
| 1.11.522 | reg : esmi_s1_cnt17 | 0x00000000 | 0xA0211408 | 458 |
| 1.11.523 | reg : esmi_s1_crc17 | 0x00000000 | 0xA021140C | 458 |
| 1.11.524 | reg : esmi_s2_cnt17 | 0x00000000 | 0xA0211410 | 459 |
| 1.11.525 | reg : esmi_s2_crc17 | 0x00000000 | 0xA0211414 | 459 |
| 1.11.526 | reg : esmi_s7_cnt17 | 0x00000000 | 0xA0211418 | 459 |
| 1.11.527 | reg : esmi_s7_crc17 | 0x00000000 | 0xA021141C | 459 |
| 1.11.528 | reg : esmi_rd_cnt17 | 0x00000000 | 0xA0211420 | 459 |
| 1.11.529 | reg : esmi_rd_crc17 | 0x00000000 | 0xA0211424 | 459 |
| 1.11.530 | reg : esmi_da_cnt17 | 0x00000000 | 0xA0211428 | 459 |
| 1.11.531 | reg : esmi_ia_cnt17 | 0x00000000 | 0xA021142C | 459 |
| 1.11.532 | reg : esmi_tcmd_cnt17 | 0x00000000 | 0xA0211430 | 460 |
| 1.11.533 | reg : esmi_twcmd_cnt17 | 0x00000000 | 0xA0211434 | 460 |
| 1.11.534 | reg : esmi_dm_cnt17 | 0x00000000 | 0xA0211438 | 460 |
| 1.11.535 | reg : esmi_s0_cnt18 | 0x00000000 | 0xA0211440 | 460 |
| 1.11.536 | reg : esmi_s0_crc18 | 0x00000000 | 0xA0211444 | 460 |
| 1.11.537 | reg : esmi_s1_cnt18 | 0x00000000 | 0xA0211448 | 460 |
| 1.11.538 | reg : esmi_s1_crc18 | 0x00000000 | 0xA021144C | 460 |
| 1.11.539 | reg : esmi_s2_cnt18 | 0x00000000 | 0xA0211450 | 460 |
| 1.11.540 | reg : esmi_s2_crc18 | 0x00000000 | 0xA0211454 | 461 |
| 1.11.541 | reg : esmi_s7_cnt18 | 0x00000000 | 0xA0211458 | 461 |
| 1.11.542 | reg : esmi_s7_crc18 | 0x00000000 | 0xA021145C | 461 |
| 1.11.543 | reg : esmi_rd_cnt18 | 0x00000000 | 0xA0211460 | 461 |
| 1.11.544 | reg : esmi_rd_crc18 | 0x00000000 | 0xA0211464 | 461 |
| 1.11.545 | reg : esmi_da_cnt18 | 0x00000000 | 0xA0211468 | 461 |
| 1.11.546 | reg : esmi_ia_cnt18 | 0x00000000 | 0xA021146C | 461 |
| 1.11.547 | reg : esmi_tcmd_cnt18 | 0x00000000 | 0xA0211470 | 462 |
| 1.11.548 | reg : esmi_twcmd_cnt18 | 0x00000000 | 0xA0211474 | 462 |
| 1.11.549 | reg : esmi_dm_cnt18 | 0x00000000 | 0xA0211478 | 462 |
| 1.11.550 | reg : esmi_s0_cnt19 | 0x00000000 | 0xA0211480 | 462 |
| 1.11.551 | reg : esmi_s0_crc19 | 0x00000000 | 0xA0211484 | 462 |
| 1.11.552 | reg : esmi_s1_cnt19 | 0x00000000 | 0xA0211488 | 462 |
| 1.11.553 | reg : esmi_s1_crc19 | 0x00000000 | 0xA021148C | 462 |

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|---|---|---|---|---|
| 1.11.554 | reg : esmi_s2_cnt19 | 0x00000000 | 0xA0211490 | 462 |
| 1.11.555 | reg : esmi_s2_crc19 | 0x00000000 | 0xA0211494 | 463 |
| 1.11.556 | reg : esmi_s7_cnt19 | 0x00000000 | 0xA0211498 | 463 |
| 1.11.557 | reg : esmi_s7_crc19 | 0x00000000 | 0xA021149C | 463 |
| 1.11.558 | reg : esmi_rd_cnt19 | 0x00000000 | 0xA02114A0 | 463 |
| 1.11.559 | reg : esmi_rd_crc19 | 0x00000000 | 0xA02114A4 | 463 |
| 1.11.560 | reg : esmi_da_cnt19 | 0x00000000 | 0xA02114A8 | 463 |
| 1.11.561 | reg : esmi_ia_cnt19 | 0x00000000 | 0xA02114AC | 463 |
| 1.11.562 | reg : esmi_tcmd_cnt19 | 0x00000000 | 0xA02114B0 | 463 |
| 1.11.563 | reg : esmi_twcmd_cnt19 | 0x00000000 | 0xA02114B4 | 464 |
| 1.11.564 | reg : esmi_dm_cnt19 | 0x00000000 | 0xA02114B8 | 464 |
| 1.11.565 | reg : esmi_s0_cnt20 | 0x00000000 | 0xA02114C0 | 464 |
| 1.11.566 | reg : esmi_s0_crc20 | 0x00000000 | 0xA02114C4 | 464 |
| 1.11.567 | reg : esmi_s1_cnt20 | 0x00000000 | 0xA02114C8 | 464 |
| 1.11.568 | reg : esmi_s1_crc20 | 0x00000000 | 0xA02114CC | 464 |
| 1.11.569 | reg : esmi_s2_cnt20 | 0x00000000 | 0xA02114D0 | 464 |
| 1.11.570 | reg : esmi_s2_crc20 | 0x00000000 | 0xA02114D4 | 465 |
| 1.11.571 | reg : esmi_s7_cnt20 | 0x00000000 | 0xA02114D8 | 465 |
| 1.11.572 | reg : esmi_s7_crc20 | 0x00000000 | 0xA02114DC | 465 |
| 1.11.573 | reg : esmi_rd_cnt20 | 0x00000000 | 0xA02114E0 | 465 |
| 1.11.574 | reg : esmi_rd_crc20 | 0x00000000 | 0xA02114E4 | 465 |
| 1.11.575 | reg : esmi_da_cnt20 | 0x00000000 | 0xA02114E8 | 465 |
| 1.11.576 | reg : esmi_ia_cnt20 | 0x00000000 | 0xA02114EC | 465 |
| 1.11.577 | reg : esmi_tcmd_cnt20 | 0x00000000 | 0xA02114F0 | 465 |
| 1.11.578 | reg : esmi_twcmd_cnt20 | 0x00000000 | 0xA02114F4 | 466 |
| 1.11.579 | reg : esmi_dm_cnt20 | 0x00000000 | 0xA02114F8 | 466 |
| 1.11.580 | reg : esmi_tref_int1 | 0x00000000 | 0xA0211500 | 466 |
| 1.11.581 | reg : esmi_tref_freq1 | 0x00000824 | 0xA0211504 | 466 |
| 1.11.582 | reg : esmi_clk_type1 | 0x00000000 | 0xA0211508 | 466 |
| 1.11.583 | reg : esmi_tref_int2 | 0x00000000 | 0xA021150C | 467 |
| 1.11.584 | reg : esmi_tref_freq2 | 0x00000824 | 0xA0211510 | 467 |
| 1.11.585 | reg : esmi_clk_type2 | 0x00000000 | 0xA0211514 | 467 |
| 1.11.586 | reg : esmi_tref_int3 | 0x00000000 | 0xA0211518 | 467 |
| 1.11.587 | reg : esmi_tref_freq3 | 0x00000824 | 0xA021151C | 467 |
| 1.11.588 | reg : esmi_clk_type3 | 0x00000000 | 0xA0211520 | 467 |
| 1.11.589 | reg : esmi_tref_int4 | 0x00000000 | 0xA0211524 | 468 |
| 1.11.590 | reg : esmi_tref_freq4 | 0x00000824 | 0xA0211528 | 468 |
| 1.11.591 | reg : esmi_clk_type4 | 0x00000000 | 0xA021152C | 468 |
| 1.11.592 | reg : esmi_tref_int5 | 0x00000000 | 0xA0211530 | 469 |
| 1.11.593 | reg : esmi_tref_freq5 | 0x00000824 | 0xA0211534 | 469 |
| 1.11.594 | reg : esmi_clk_type5 | 0x00000000 | 0xA0211538 | 469 |
| 1.11.595 | reg : esmi_tref_int6 | 0x00000000 | 0xA021153C | 469 |
| 1.11.596 | reg : esmi_tref_freq6 | 0x00000824 | 0xA0211540 | 469 |
| 1.11.597 | reg : esmi_clk_type6 | 0x00000000 | 0xA0211544 | 469 |
| 1.11.598 | reg : esmi_tref_int7 | 0x00000000 | 0xA0211548 | 470 |
| 1.11.599 | reg : esmi_tref_freq7 | 0x00000824 | 0xA021154C | 470 |
| 1.11.600 | reg : esmi_clk_type7 | 0x00000000 | 0xA0211550 | 470 |
| 1.11.601 | reg : esmi_tref_int8 | 0x00000000 | 0xA0211554 | 471 |
| 1.11.602 | reg : esmi_tref_freq8 | 0x00000824 | 0xA0211558 | 471 |
| 1.11.603 | reg : esmi_clk_type8 | 0x00000000 | 0xA021155C | 471 |
| 1.11.604 | reg : esmi_tref_int9 | 0x00000000 | 0xA0211560 | 471 |
| 1.11.605 | reg : esmi_tref_freq9 | 0x00000824 | 0xA0211564 | 471 |
| 1.11.606 | reg : esmi_clk_type9 | 0x00000000 | 0xA0211568 | 472 |
| 1.11.607 | reg : esmi_tref_int10 | 0x00000000 | 0xA021156C | 472 |
| 1.11.608 | reg : esmi_tref_freq10 | 0x00000824 | 0xA0211570 | 472 |
| 1.11.609 | reg : esmi_clk_type10 | 0x00000000 | 0xA0211574 | 472 |
| 1.11.610 | reg : esmi_tref_int11 | 0x00000000 | 0xA0211578 | 473 |
| 1.11.611 | reg : esmi_tref_freq11 | 0x00000824 | 0xA021157C | 473 |
| 1.11.612 | reg : esmi_clk_type11 | 0x00000000 | 0xA0211580 | 473 |
| 1.11.613 | reg : esmi_tref_int12 | 0x00000000 | 0xA0211584 | 473 |
| 1.11.614 | reg : esmi_tref_freq12 | 0x00000824 | 0xA0211588 | 473 |
| 1.11.615 | reg : esmi_clk_type12 | 0x00000000 | 0xA021158C | 474 |
| 1.11.616 | reg : esmi_tref_int13 | 0x00000000 | 0xA0211590 | 474 |
| 1.11.617 | reg : esmi_tref_freq13 | 0x00000824 | 0xA0211594 | 474 |
| 1.11.618 | reg : esmi_clk_type13 | 0x00000000 | 0xA0211598 | 474 |
| 1.11.619 | reg : esmi_tref_int14 | 0x00000000 | 0xA021159C | 475 |

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|---|---|---|---|---|
| 1.11.620 | reg : esmi_tref_freq14 | 0x00000824 | 0xA02115A0 | 475 |
| 1.11.621 | reg : esmi_clk_type14 | 0x00000000 | 0xA02115A4 | 475 |
| 1.11.622 | reg : esmi_tref_int15 | 0x00000000 | 0xA02115A8 | 475 |
| 1.11.623 | reg : esmi_tref_freq15 | 0x00000824 | 0xA02115AC | 475 |
| 1.11.624 | reg : esmi_clk_type15 | 0x00000000 | 0xA02115B0 | 476 |
| 1.11.625 | reg : esmi_tref_int16 | 0x00000000 | 0xA02115B4 | 476 |
| 1.11.626 | reg : esmi_tref_freq16 | 0x00000824 | 0xA02115B8 | 476 |
| 1.11.627 | reg : esmi_clk_type16 | 0x00000000 | 0xA02115BC | 476 |
| 1.11.628 | reg : esmi_tref_int17 | 0x00000000 | 0xA02115C0 | 477 |
| 1.11.629 | reg : esmi_tref_freq17 | 0x00000824 | 0xA02115C4 | 477 |
| 1.11.630 | reg : esmi_clk_type17 | 0x00000000 | 0xA02115C8 | 477 |
| 1.11.631 | reg : esmi_tref_int18 | 0x00000000 | 0xA02115CC | 477 |
| 1.11.632 | reg : esmi_tref_freq18 | 0x00000824 | 0xA02115D0 | 477 |
| 1.11.633 | reg : esmi_clk_type18 | 0x00000000 | 0xA02115D4 | 478 |
| 1.11.634 | reg : esmi_tref_int19 | 0x00000000 | 0xA02115D8 | 478 |
| 1.11.635 | reg : esmi_tref_freq19 | 0x00000824 | 0xA02115DC | 478 |
| 1.11.636 | reg : esmi_clk_type19 | 0x00000000 | 0xA02115E0 | 478 |
| 1.11.637 | reg : esmi_tref_int20 | 0x00000000 | 0xA02115E4 | 479 |
| 1.11.638 | reg : esmi_tref_freq20 | 0x00000824 | 0xA02115E8 | 479 |
| 1.11.639 | reg : esmi_clk_type20 | 0x00000000 | 0xA02115EC | 479 |
| 1.11.640 | reg : euv_sim1 | 0x00000000 | 0xA02115F0 | 479 |
| 1.11.641 | reg : euv_sim2 | 0x00000000 | 0xA02115F4 | 480 |
| 1.11.642 | reg : euv_sim3 | 0x00000000 | 0xA02115F8 | 480 |
| 1.11.643 | reg : euv_sim4 | 0x00000000 | 0xA02115FC | 480 |
| 1.11.644 | reg : euv_sim5 | 0x00000000 | 0xA0211600 | 480 |
| 1.11.645 | reg : euv_sim6 | 0x00000000 | 0xA0211604 | 480 |
| 1.11.646 | reg : euv_sim7 | 0x00000000 | 0xA0211608 | 480 |
| 1.11.647 | reg : euv_sim8 | 0x00000000 | 0xA021160C | 480 |
| 1.11.648 | reg : euv_sim9 | 0x00000000 | 0xA0211610 | 480 |
| 1.11.649 | reg : euv_sim10 | 0x00000000 | 0xA0211614 | 480 |
| 1.11.650 | reg : euv_sim11 | 0x00000000 | 0xA0211618 | 481 |
| 1.11.651 | reg : euv_sim12 | 0x00000000 | 0xA021161C | 481 |
| 1.11.652 | reg : euv_sim13 | 0x00000000 | 0xA0211620 | 481 |
| 1.11.653 | reg : euv_sim14 | 0x00000000 | 0xA0211624 | 481 |
| 1.11.654 | reg : euv_sim15 | 0x00000000 | 0xA0211628 | 481 |
| 1.11.655 | reg : euv_sim16 | 0x00000000 | 0xA021162C | 481 |
| 1.11.656 | reg : euv_sim17 | 0x00000000 | 0xA0211630 | 481 |
| 1.11.657 | reg : euv_sim18 | 0x00000000 | 0xA0211634 | 481 |
| 1.11.658 | reg : euv_sim19 | 0x00000000 | 0xA0211638 | 481 |
| 1.11.659 | reg : euv_sim20 | 0x00000000 | 0xA021163C | 482 |
| 1.11.660 | reg : esmi_scratch | 0x00000000 | 0xA0211640 | 482 |
| 1.11.661 | reg : esmi_s7_1ms_cnt | 0x00000000 | 0xA0211644 | 482 |
| 1.11.662 | reg : esmi_xpam_bw_ovld | 0x00000000 | 0xA0211648 | 482 |
| 1.11.663 | reg : esmi_xpam_init_err | 0x00000000 | 0xA021164C | 482 |
| 1.11.664 | reg : esmi_xlam_cab_disc | 0x00000000 | 0xA0211650 | 482 |
| 1.11.665 | reg : esmi_adc_clip_cnt1 | 0x00000000 | 0xA0211680 | 482 |
| 1.11.666 | reg : esmi_adc_clip_cnt2 | 0x00000000 | 0xA0211684 | 482 |
| 1.11.667 | reg : esmi_adc_clip_cnt3 | 0x00000000 | 0xA0211688 | 483 |
| 1.11.668 | reg : esmi_adc_clip_cnt4 | 0x00000000 | 0xA021168C | 483 |
| 1.11.669 | reg : esmi_adc_clip_cnt5 | 0x00000000 | 0xA0211690 | 483 |
| 1.11.670 | reg : esmi_adc_clip_cnt6 | 0x00000000 | 0xA0211694 | 483 |
| 1.11.671 | reg : esmi_adc_clip_cnt7 | 0x00000000 | 0xA0211698 | 483 |
| 1.11.672 | reg : esmi_adc_clip_cnt8 | 0x00000000 | 0xA021169C | 483 |
| 1.11.673 | reg : esmi_adc_clip_cnt9 | 0x00000000 | 0xA02116A0 | 483 |
| 1.11.674 | reg : esmi_adc_clip_cnt10 | 0x00000000 | 0xA02116A4 | 483 |
| 1.11.675 | reg : esmi_adc_clip_cnt11 | 0x00000000 | 0xA02116A8 | 484 |
| 1.11.676 | reg : esmi_adc_clip_cnt12 | 0x00000000 | 0xA02116AC | 484 |
| 1.11.677 | reg : esmi_adc_clip_cnt13 | 0x00000000 | 0xA02116B0 | 484 |
| 1.11.678 | reg : esmi_adc_clip_cnt14 | 0x00000000 | 0xA02116B4 | 484 |
| 1.11.679 | reg : esmi_adc_clip_cnt15 | 0x00000000 | 0xA02116B8 | 484 |
| 1.11.680 | reg : esmi_adc_clip_cnt16 | 0x00000000 | 0xA02116BC | 484 |
| 1.11.681 | reg : esmi_adc_clip_cnt17 | 0x00000000 | 0xA02116C0 | 484 |
| 1.11.682 | reg : esmi_adc_clip_cnt18 | 0x00000000 | 0xA02116C4 | 484 |
| 1.11.683 | reg : esmi_adc_clip_cnt19 | 0x00000000 | 0xA02116C8 | 484 |
| 1.11.684 | reg : esmi_adc_clip_cnt20 | 0x00000000 | 0xA02116CC | 485 |
| 1.11.685 | reg : esmi_dat1 | 0x00000000 | 0xA02116D0 | 485 |

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|---|---|---|---|---|
| 1.11.686 | reg : esmi_dat2 | 0x00000000 | 0xA02116D4 | 485 |
| 1.11.687 | reg : esmi_dat3 | 0x00000000 | 0xA02116D8 | 485 |
| 1.11.688 | reg : esmi_dat4 | 0x00000000 | 0xA02116DC | 486 |
| 1.11.689 | reg : esmi_dat5 | 0x00000000 | 0xA02116E0 | 486 |
| 1.11.690 | reg : esmi_dat6 | 0x00000000 | 0xA02116E4 | 487 |
| 1.11.691 | reg : esmi_dat7 | 0x00000000 | 0xA02116E8 | 487 |
| 1.11.692 | reg : esmi_dat8 | 0x00000000 | 0xA02116EC | 487 |
| 1.11.693 | reg : esmi_dat9 | 0x00000000 | 0xA02116F0 | 488 |
| 1.11.694 | reg : esmi_dat10 | 0x00000000 | 0xA02116F4 | 488 |
| 1.11.695 | reg : esmi_dat11 | 0x00000000 | 0xA02116F8 | 488 |
| 1.11.696 | reg : esmi_dat12 | 0x00000000 | 0xA02116FC | 489 |
| 1.11.697 | reg : esmi_dat13 | 0x00000000 | 0xA0211700 | 489 |
| 1.11.698 | reg : esmi_dat14 | 0x00000000 | 0xA0211704 | 490 |
| 1.11.699 | reg : esmi_dat15 | 0x00000000 | 0xA0211708 | 490 |
| 1.11.700 | reg : esmi_dat16 | 0x00000000 | 0xA021170C | 490 |
| 1.11.701 | reg : esmi_dat17 | 0x00000000 | 0xA0211710 | 491 |
| 1.11.702 | reg : esmi_dat18 | 0x00000000 | 0xA0211714 | 491 |
| 1.11.703 | reg : esmi_dat19 | 0x00000000 | 0xA0211718 | 492 |
| 1.11.704 | reg : esmi_dat20 | 0x00000000 | 0xA021171C | 492 |
| 1.12 | block : mcdma_feed_registers_srdl | | 0xA0240000 - 0xA0240F73 | 492 |
| 1.12.1 | reg : mcdma_feed_module_name | 0x77687765 | 0xA0240000 | 492 |
| 1.12.2 | reg : mcdma_feed_module_version | 0x05210301 | 0xA0240004 | 493 |
| 1.12.3 | reg : mcdma_feed_page_properties | 0x80000101 | 0xA0240008 | 493 |
| 1.12.4 | reg : mcdma_feed_scratchregister | 0x12345678 | 0xA024000C | 493 |
| 1.12.5 | reg : mcdma_feed_irq_enable | 0x00000000 | 0xA0240010 | 493 |
| 1.12.6 | reg : mcdma_feed_irq_pending | 0x00000000 | 0xA0240014 | 493 |
| 1.12.7 | reg : mcdma_feed_irq_raw | 0x00000000 | 0xA0240018 | 493 |
| 1.12.8 | reg : mcdma_feed_irq_force | 0x00000000 | 0xA024001C | 493 |
| 1.12.9 | reg : streamtpg_en_ctrl | 0x0000FFFF | 0xA0240020 | 494 |
| 1.12.10 | reg : streamsx16_err_stat | 0x00000000 | 0xA0240024 | 494 |
| 1.12.11 | reg : tpg0_packet_rate_clks_ctrl | 0x00000823 | 0xA0240034 | 494 |
| 1.12.12 | reg : tpg0_packet_size_clks_ctrl | 0x00000040 | 0xA0240038 | 495 |
| 1.12.13 | reg : stream0_expsize_dis_ctrl | 0x0000004D | 0xA024003C | 495 |
| 1.12.14 | reg : stream0_exprate_dis_ctrl | 0x007F0040 | 0xA0240040 | 495 |
| 1.12.15 | reg : stream0_err_stat | 0x00000000 | 0xA0240044 | 495 |
| 1.12.16 | reg : stream0_err_expsize_cntr_stat | 0x00000000 | 0xA0240048 | 495 |
| 1.12.17 | reg : stream0_err_pfifofull_cntr_stat | 0x00000000 | 0xA024004C | 496 |
| 1.12.18 | reg : stream0_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240050 | 496 |
| 1.12.19 | reg : stream0_err_maxsize_cntr_stat | 0x00000000 | 0xA0240054 | 496 |
| 1.12.20 | reg : stream0_err_minsize_cntr_stat | 0x00000000 | 0xA0240058 | 496 |
| 1.12.21 | reg : stream0_err_notlast_cntr_stat | 0x00000000 | 0xA024005C | 496 |
| 1.12.22 | reg : stream0_err_minipg_cntr_stat | 0x00000000 | 0xA0240060 | 496 |
| 1.12.23 | reg : stream0_err_watchdog_cntr_stat | 0x00000000 | 0xA0240064 | 496 |
| 1.12.24 | reg : stream0_exc_exprate_cntr_stat | 0x00000000 | 0xA0240068 | 497 |
| 1.12.25 | reg : stream0_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024006C | 497 |

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|---|---|---|---|---|
| 1.12.26 | reg : stream0_rate_measured_stat | 0x00000000 | 0xA0240070 | 497 |
| 1.12.27 | reg : tpg1_packet_rate_clks_ctrl | 0x00000823 | 0xA0240134 | 497 |
| 1.12.28 | reg : tpg1_packet_size_clks_ctrl | 0x00000040 | 0xA0240138 | 497 |
| 1.12.29 | reg : stream1_expsize_dis_ctrl | 0x0000002C | 0xA024013C | 497 |
| 1.12.30 | reg : stream1_exprate_dis_ctrl | 0x007F0040 | 0xA0240140 | 498 |
| 1.12.31 | reg : stream1_err_stat | 0x00000000 | 0xA0240144 | 498 |
| 1.12.32 | reg : stream1_err_expsize_cntr_stat | 0x00000000 | 0xA0240148 | 498 |
| 1.12.33 | reg : stream1_err_pfifofull_cntr_stat | 0x00000000 | 0xA024014C | 498 |
| 1.12.34 | reg : stream1_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240150 | 498 |
| 1.12.35 | reg : stream1_err_maxsize_cntr_stat | 0x00000000 | 0xA0240154 | 498 |
| 1.12.36 | reg : stream1_err_minsize_cntr_stat | 0x00000000 | 0xA0240158 | 499 |
| 1.12.37 | reg : stream1_err_notlast_cntr_stat | 0x00000000 | 0xA024015C | 499 |
| 1.12.38 | reg : stream1_err_minipg_cntr_stat | 0x00000000 | 0xA0240160 | 499 |
| 1.12.39 | reg : stream1_err_watchdog_cntr_stat | 0x00000000 | 0xA0240164 | 499 |
| 1.12.40 | reg : stream1_exc_exprate_cntr_stat | 0x00000000 | 0xA0240168 | 499 |
| 1.12.41 | reg : stream1_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024016C | 499 |
| 1.12.42 | reg : stream1_rate_measured_stat | 0x00000000 | 0xA0240170 | 500 |
| 1.12.43 | reg : tpg2_packet_rate_clks_ctrl | 0x00000823 | 0xA0240234 | 500 |
| 1.12.44 | reg : tpg2_packet_size_clks_ctrl | 0x00000040 | 0xA0240238 | 500 |
| 1.12.45 | reg : stream2_expsize_dis_ctrl | 0x00000013 | 0xA024023C | 500 |
| 1.12.46 | reg : stream2_exprate_dis_ctrl | 0x007F0040 | 0xA0240240 | 500 |
| 1.12.47 | reg : stream2_err_stat | 0x00000000 | 0xA0240244 | 500 |
| 1.12.48 | reg : stream2_err_expsize_cntr_stat | 0x00000000 | 0xA0240248 | 501 |
| 1.12.49 | reg : stream2_err_pfifofull_cntr_stat | 0x00000000 | 0xA024024C | 501 |
| 1.12.50 | reg : stream2_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240250 | 501 |
| 1.12.51 | reg : stream2_err_maxsize_cntr_stat | 0x00000000 | 0xA0240254 | 501 |
| 1.12.52 | reg : stream2_err_minsize_cntr_stat | 0x00000000 | 0xA0240258 | 501 |
| 1.12.53 | reg : stream2_err_notlast_cntr_stat | 0x00000000 | 0xA024025C | 501 |
| 1.12.54 | reg : stream2_err_minipg_cntr_stat | 0x00000000 | 0xA0240260 | 502 |
| 1.12.55 | reg : stream2_err_watchdog_cntr_stat | 0x00000000 | 0xA0240264 | 502 |
| 1.12.56 | reg : stream2_exc_exprate_cntr_stat | 0x00000000 | 0xA0240268 | 502 |
| 1.12.57 | reg : stream2_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024026C | 502 |
| 1.12.58 | reg : stream2_rate_measured_stat | 0x00000000 | 0xA0240270 | 502 |
| 1.12.59 | reg : tpg3_packet_rate_clks_ctrl | 0x00000823 | 0xA0240334 | 502 |
| 1.12.60 | reg : tpg3_packet_size_clks_ctrl | 0x00000040 | 0xA0240338 | 502 |

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|---|---|---|---|---|
| 1.12.61 | reg : stream3_expsize_dis_ctrl | 0x0000000D | 0xA024033C | 503 |
| 1.12.62 | reg : stream3_exprate_dis_ctrl | 0x007F0040 | 0xA0240340 | 503 |
| 1.12.63 | reg : stream3_err_stat | 0x00000000 | 0xA0240344 | 503 |
| 1.12.64 | reg : stream3_err_expsize_cntr_stat | 0x00000000 | 0xA0240348 | 503 |
| 1.12.65 | reg : stream3_err_pfifofull_cntr_stat | 0x00000000 | 0xA024034C | 504 |
| 1.12.66 | reg : stream3_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240350 | 504 |
| 1.12.67 | reg : stream3_err_maxsize_cntr_stat | 0x00000000 | 0xA0240354 | 504 |
| 1.12.68 | reg : stream3_err_minsize_cntr_stat | 0x00000000 | 0xA0240358 | 504 |
| 1.12.69 | reg : stream3_err_notlast_cntr_stat | 0x00000000 | 0xA024035C | 504 |
| 1.12.70 | reg : stream3_err_minipg_cntr_stat | 0x00000000 | 0xA0240360 | 504 |
| 1.12.71 | reg : stream3_err_watchdog_cntr_stat | 0x00000000 | 0xA0240364 | 504 |
| 1.12.72 | reg : stream3_exc_exprate_cntr_stat | 0x00000000 | 0xA0240368 | 504 |
| 1.12.73 | reg : stream3_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024036C | 505 |
| 1.12.74 | reg : stream3_rate_measured_stat | 0x00000000 | 0xA0240370 | 505 |
| 1.12.75 | reg : tpg4_packet_rate_clks_ctrl | 0x00000823 | 0xA0240434 | 505 |
| 1.12.76 | reg : tpg4_packet_size_clks_ctrl | 0x00000040 | 0xA0240438 | 505 |
| 1.12.77 | reg : stream4_expsize_dis_ctrl | 0x0000000C | 0xA024043C | 505 |
| 1.12.78 | reg : stream4_exprate_dis_ctrl | 0x007F0040 | 0xA0240440 | 505 |
| 1.12.79 | reg : stream4_err_stat | 0x00000000 | 0xA0240444 | 506 |
| 1.12.80 | reg : stream4_err_expsize_cntr_stat | 0x00000000 | 0xA0240448 | 506 |
| 1.12.81 | reg : stream4_err_pfifofull_cntr_stat | 0x00000000 | 0xA024044C | 506 |
| 1.12.82 | reg : stream4_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240450 | 506 |
| 1.12.83 | reg : stream4_err_maxsize_cntr_stat | 0x00000000 | 0xA0240454 | 506 |
| 1.12.84 | reg : stream4_err_minsize_cntr_stat | 0x00000000 | 0xA0240458 | 507 |
| 1.12.85 | reg : stream4_err_notlast_cntr_stat | 0x00000000 | 0xA024045C | 507 |
| 1.12.86 | reg : stream4_err_minipg_cntr_stat | 0x00000000 | 0xA0240460 | 507 |
| 1.12.87 | reg : stream4_err_watchdog_cntr_stat | 0x00000000 | 0xA0240464 | 507 |
| 1.12.88 | reg : stream4_exc_exprate_cntr_stat | 0x00000000 | 0xA0240468 | 507 |
| 1.12.89 | reg : stream4_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024046C | 507 |
| 1.12.90 | reg : stream4_rate_measured_stat | 0x00000000 | 0xA0240470 | 507 |
| 1.12.91 | reg : tpg5_packet_rate_clks_ctrl | 0x00000823 | 0xA0240534 | 508 |
| 1.12.92 | reg : tpg5_packet_size_clks_ctrl | 0x00000040 | 0xA0240538 | 508 |
| 1.12.93 | reg : stream5_expsize_dis_ctrl | 0x0000007A | 0xA024053C | 508 |
| 1.12.94 | reg : stream5_exprate_dis_ctrl | 0x007F0040 | 0xA0240540 | 508 |
| 1.12.95 | reg : stream5_err_stat | 0x00000000 | 0xA0240544 | 508 |
| 1.12.96 | reg : stream5_err_expsize_cn | 0x00000000 | 0xA0240548 | 509 |

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|---|---|---|---|---|
| | tr_stat | | | |
| 1.12.97 | reg : stream5_err_pfifofull_cntr_stat | 0x00000000 | 0xA024054C | 509 |
| 1.12.98 | reg : stream5_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240550 | 509 |
| 1.12.99 | reg : stream5_err_maxsize_cntr_stat | 0x00000000 | 0xA0240554 | 509 |
| 1.12.100 | reg : stream5_err_minsize_cntr_stat | 0x00000000 | 0xA0240558 | 509 |
| 1.12.101 | reg : stream5_err_notlast_cntr_stat | 0x00000000 | 0xA024055C | 509 |
| 1.12.102 | reg : stream5_err_minipg_cntr_stat | 0x00000000 | 0xA0240560 | 509 |
| 1.12.103 | reg : stream5_err_watchdog_cntr_stat | 0x00000000 | 0xA0240564 | 510 |
| 1.12.104 | reg : stream5_exc_exprate_cntr_stat | 0x00000000 | 0xA0240568 | 510 |
| 1.12.105 | reg : stream5_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024056C | 510 |
| 1.12.106 | reg : stream5_rate_measured_stat | 0x00000000 | 0xA0240570 | 510 |
| 1.12.107 | reg : tpg6_packet_rate_clks_ctrl | 0x00000823 | 0xA0240634 | 510 |
| 1.12.108 | reg : tpg6_packet_size_clks_ctrl | 0x00000040 | 0xA0240638 | 510 |
| 1.12.109 | reg : stream6_expsize_dis_ctrl | 0x000000BD | 0xA024063C | 511 |
| 1.12.110 | reg : stream6_exprate_dis_ctrl | 0x007F0040 | 0xA0240640 | 511 |
| 1.12.111 | reg : stream6_err_stat | 0x00000000 | 0xA0240644 | 511 |
| 1.12.112 | reg : stream6_err_expsize_cntr_stat | 0x00000000 | 0xA0240648 | 511 |
| 1.12.113 | reg : stream6_err_pfifofull_cntr_stat | 0x00000000 | 0xA024064C | 511 |
| 1.12.114 | reg : stream6_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240650 | 512 |
| 1.12.115 | reg : stream6_err_maxsize_cntr_stat | 0x00000000 | 0xA0240654 | 512 |
| 1.12.116 | reg : stream6_err_minsize_cntr_stat | 0x00000000 | 0xA0240658 | 512 |
| 1.12.117 | reg : stream6_err_notlast_cntr_stat | 0x00000000 | 0xA024065C | 512 |
| 1.12.118 | reg : stream6_err_minipg_cntr_stat | 0x00000000 | 0xA0240660 | 512 |
| 1.12.119 | reg : stream6_err_watchdog_cntr_stat | 0x00000000 | 0xA0240664 | 512 |
| 1.12.120 | reg : stream6_exc_exprate_cntr_stat | 0x00000000 | 0xA0240668 | 512 |
| 1.12.121 | reg : stream6_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024066C | 513 |
| 1.12.122 | reg : stream6_rate_measured_stat | 0x00000000 | 0xA0240670 | 513 |
| 1.12.123 | reg : tpg7_packet_rate_clks_ctrl | 0x00000823 | 0xA0240734 | 513 |
| 1.12.124 | reg : tpg7_packet_size_clks_ctrl | 0x00000040 | 0xA0240738 | 513 |
| 1.12.125 | reg : stream7_expsize_dis_ctrl | 0x0000001D | 0xA024073C | 513 |
| 1.12.126 | reg : stream7_exprate_dis_ctrl | 0x007F0040 | 0xA0240740 | 513 |
| 1.12.127 | reg : stream7_err_stat | 0x00000000 | 0xA0240744 | 514 |
| 1.12.128 | reg : stream7_err_expsize_cntr_stat | 0x00000000 | 0xA0240748 | 514 |
| 1.12.129 | reg : stream7_err_pfifofull_cntr_stat | 0x00000000 | 0xA024074C | 514 |
| 1.12.130 | reg : stream7_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240750 | 514 |
| 1.12.131 | reg : stream7_err_maxsize_cn | 0x00000000 | 0xA0240754 | 514 |

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|---|---|---|---|---|
| | tr_stat | | | |
| 1.12.132 | reg : stream7_err_minsize_cntr_stat | 0x00000000 | 0xA0240758 | 514 |
| 1.12.133 | reg : stream7_err_notlast_cntr_stat | 0x00000000 | 0xA024075C | 515 |
| 1.12.134 | reg : stream7_err_minipg_cntr_stat | 0x00000000 | 0xA0240760 | 515 |
| 1.12.135 | reg : stream7_err_watchdog_cntr_stat | 0x00000000 | 0xA0240764 | 515 |
| 1.12.136 | reg : stream7_exc_exprate_cntr_stat | 0x00000000 | 0xA0240768 | 515 |
| 1.12.137 | reg : stream7_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024076C | 515 |
| 1.12.138 | reg : stream7_rate_measured_stat | 0x00000000 | 0xA0240770 | 515 |
| 1.12.139 | reg : tpg8_packet_rate_clks_ctrl | 0x00000823 | 0xA0240834 | 516 |
| 1.12.140 | reg : tpg8_packet_size_clks_ctrl | 0x00000040 | 0xA0240838 | 516 |
| 1.12.141 | reg : stream8_expsize_dis_ctrl | 0x00000110 | 0xA024083C | 516 |
| 1.12.142 | reg : stream8_exprate_dis_ctrl | 0x007F0040 | 0xA0240840 | 516 |
| 1.12.143 | reg : stream8_err_stat | 0x00000000 | 0xA0240844 | 516 |
| 1.12.144 | reg : stream8_err_expsize_cntr_stat | 0x00000000 | 0xA0240848 | 517 |
| 1.12.145 | reg : stream8_err_pfifofull_cntr_stat | 0x00000000 | 0xA024084C | 517 |
| 1.12.146 | reg : stream8_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240850 | 517 |
| 1.12.147 | reg : stream8_err_maxsize_cntr_stat | 0x00000000 | 0xA0240854 | 517 |
| 1.12.148 | reg : stream8_err_minsize_cntr_stat | 0x00000000 | 0xA0240858 | 517 |
| 1.12.149 | reg : stream8_err_notlast_cntr_stat | 0x00000000 | 0xA024085C | 517 |
| 1.12.150 | reg : stream8_err_minipg_cntr_stat | 0x00000000 | 0xA0240860 | 517 |
| 1.12.151 | reg : stream8_err_watchdog_cntr_stat | 0x00000000 | 0xA0240864 | 518 |
| 1.12.152 | reg : stream8_exc_exprate_cntr_stat | 0x00000000 | 0xA0240868 | 518 |
| 1.12.153 | reg : stream8_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024086C | 518 |
| 1.12.154 | reg : stream8_rate_measured_stat | 0x00000000 | 0xA0240870 | 518 |
| 1.12.155 | reg : tpg9_packet_rate_clks_ctrl | 0x00000823 | 0xA0240934 | 518 |
| 1.12.156 | reg : tpg9_packet_size_clks_ctrl | 0x00000040 | 0xA0240938 | 518 |
| 1.12.157 | reg : stream9_expsize_dis_ctrl | 0x00000034 | 0xA024093C | 519 |
| 1.12.158 | reg : stream9_exprate_dis_ctrl | 0x007F0040 | 0xA0240940 | 519 |
| 1.12.159 | reg : stream9_err_stat | 0x00000000 | 0xA0240944 | 519 |
| 1.12.160 | reg : stream9_err_expsize_cntr_stat | 0x00000000 | 0xA0240948 | 519 |
| 1.12.161 | reg : stream9_err_pfifofull_cntr_stat | 0x00000000 | 0xA024094C | 519 |
| 1.12.162 | reg : stream9_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240950 | 520 |
| 1.12.163 | reg : stream9_err_maxsize_cntr_stat | 0x00000000 | 0xA0240954 | 520 |
| 1.12.164 | reg : stream9_err_minsize_cntr_stat | 0x00000000 | 0xA0240958 | 520 |
| 1.12.165 | reg : stream9_err_notlast_cntr_stat | 0x00000000 | 0xA024095C | 520 |
| 1.12.166 | reg : stream9_err_minipg_cnt | 0x00000000 | 0xA0240960 | 520 |

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|---|---|---|---|---|
| | r_stat | | | |
| 1.12.167 | reg : stream9_err_watchdog_cntr_stat | 0x00000000 | 0xA0240964 | 520 |
| 1.12.168 | reg : stream9_exc_exprate_cntr_stat | 0x00000000 | 0xA0240968 | 520 |
| 1.12.169 | reg : stream9_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA024096C | 520 |
| 1.12.170 | reg : stream9_rate_measured_stat | 0x00000000 | 0xA0240970 | 521 |
| 1.12.171 | reg : tpg10_packet_rate_clks_ctrl | 0x00000823 | 0xA0240A34 | 521 |
| 1.12.172 | reg : tpg10_packet_size_clks_ctrl | 0x00000040 | 0xA0240A38 | 521 |
| 1.12.173 | reg : stream10_expsize_dis_ctrl | 0x00000083 | 0xA0240A3C | 521 |
| 1.12.174 | reg : stream10_exprate_dis_ctrl | 0x007F0040 | 0xA0240A40 | 521 |
| 1.12.175 | reg : stream10_err_stat | 0x00000000 | 0xA0240A44 | 522 |
| 1.12.176 | reg : stream10_err_expsize_cntr_stat | 0x00000000 | 0xA0240A48 | 522 |
| 1.12.177 | reg : stream10_err_pfifofull_cntr_stat | 0x00000000 | 0xA0240A4C | 522 |
| 1.12.178 | reg : stream10_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240A50 | 522 |
| 1.12.179 | reg : stream10_err_maxsize_cntr_stat | 0x00000000 | 0xA0240A54 | 522 |
| 1.12.180 | reg : stream10_err_minsize_cntr_stat | 0x00000000 | 0xA0240A58 | 522 |
| 1.12.181 | reg : stream10_err_notlast_cntr_stat | 0x00000000 | 0xA0240A5C | 523 |
| 1.12.182 | reg : stream10_err_minipg_cntr_stat | 0x00000000 | 0xA0240A60 | 523 |
| 1.12.183 | reg : stream10_err_watchdog_cntr_stat | 0x00000000 | 0xA0240A64 | 523 |
| 1.12.184 | reg : stream10_exc_exprate_cntr_stat | 0x00000000 | 0xA0240A68 | 523 |
| 1.12.185 | reg : stream10_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA0240A6C | 523 |
| 1.12.186 | reg : stream10_rate_measured_stat | 0x00000000 | 0xA0240A70 | 523 |
| 1.12.187 | reg : tpg11_packet_rate_clks_ctrl | 0x00000823 | 0xA0240B34 | 523 |
| 1.12.188 | reg : tpg11_packet_size_clks_ctrl | 0x00000040 | 0xA0240B38 | 524 |
| 1.12.189 | reg : stream11_expsize_dis_ctrl | 0x0000001E | 0xA0240B3C | 524 |
| 1.12.190 | reg : stream11_exprate_dis_ctrl | 0x007F0040 | 0xA0240B40 | 524 |
| 1.12.191 | reg : stream11_err_stat | 0x00000000 | 0xA0240B44 | 524 |
| 1.12.192 | reg : stream11_err_expsize_cntr_stat | 0x00000000 | 0xA0240B48 | 525 |
| 1.12.193 | reg : stream11_err_pfifofull_cntr_stat | 0x00000000 | 0xA0240B4C | 525 |
| 1.12.194 | reg : stream11_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240B50 | 525 |
| 1.12.195 | reg : stream11_err_maxsize_cntr_stat | 0x00000000 | 0xA0240B54 | 525 |
| 1.12.196 | reg : stream11_err_minsize_cntr_stat | 0x00000000 | 0xA0240B58 | 525 |
| 1.12.197 | reg : stream11_err_notlast_cntr_stat | 0x00000000 | 0xA0240B5C | 525 |
| 1.12.198 | reg : stream11_err_minipg_cntr_stat | 0x00000000 | 0xA0240B60 | 525 |
| 1.12.199 | reg : stream11_err_watchdog_cntr_stat | 0x00000000 | 0xA0240B64 | 525 |
| 1.12.200 | reg : stream11_exc_exprate_cntr_stat | 0x00000000 | 0xA0240B68 | 526 |
| 1.12.201 | reg : stream11_exc_expratede | 0x00000000 | 0xA0240B6C | 526 |

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|---|---|---|---|---|
| | viate_cntr_stat | | | |
| 1.12.202 | reg : stream11_rate_measured_stat | 0x00000000 | 0xA0240B70 | 526 |
| 1.12.203 | reg : tpg12_packet_rate_clks_ctrl | 0x00000823 | 0xA0240C34 | 526 |
| 1.12.204 | reg : tpg12_packet_size_clks_ctrl | 0x00000040 | 0xA0240C38 | 526 |
| 1.12.205 | reg : stream12_expsize_dis_ctrl | 0x00000040 | 0xA0240C3C | 526 |
| 1.12.206 | reg : stream12_exprate_dis_ctrl | 0x007F0040 | 0xA0240C40 | 527 |
| 1.12.207 | reg : stream12_err_stat | 0x00000000 | 0xA0240C44 | 527 |
| 1.12.208 | reg : stream12_err_expsize_cntr_stat | 0x00000000 | 0xA0240C48 | 527 |
| 1.12.209 | reg : stream12_err_pfifofull_cntr_stat | 0x00000000 | 0xA0240C4C | 527 |
| 1.12.210 | reg : stream12_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240C50 | 528 |
| 1.12.211 | reg : stream12_err_maxsize_cntr_stat | 0x00000000 | 0xA0240C54 | 528 |
| 1.12.212 | reg : stream12_err_minsize_cntr_stat | 0x00000000 | 0xA0240C58 | 528 |
| 1.12.213 | reg : stream12_err_notlast_cntr_stat | 0x00000000 | 0xA0240C5C | 528 |
| 1.12.214 | reg : stream12_err_minipg_cntr_stat | 0x00000000 | 0xA0240C60 | 528 |
| 1.12.215 | reg : stream12_err_watchdog_cntr_stat | 0x00000000 | 0xA0240C64 | 528 |
| 1.12.216 | reg : stream12_exc_exprate_cntr_stat | 0x00000000 | 0xA0240C68 | 528 |
| 1.12.217 | reg : stream12_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA0240C6C | 528 |
| 1.12.218 | reg : stream12_rate_measured_stat | 0x00000000 | 0xA0240C70 | 529 |
| 1.12.219 | reg : tpg13_packet_rate_clks_ctrl | 0x00000823 | 0xA0240D34 | 529 |
| 1.12.220 | reg : tpg13_packet_size_clks_ctrl | 0x00000040 | 0xA0240D38 | 529 |
| 1.12.221 | reg : stream13_expsize_dis_ctrl | 0x00000040 | 0xA0240D3C | 529 |
| 1.12.222 | reg : stream13_exprate_dis_ctrl | 0x007F0040 | 0xA0240D40 | 529 |
| 1.12.223 | reg : stream13_err_stat | 0x00000000 | 0xA0240D44 | 530 |
| 1.12.224 | reg : stream13_err_expsize_cntr_stat | 0x00000000 | 0xA0240D48 | 530 |
| 1.12.225 | reg : stream13_err_pfifofull_cntr_stat | 0x00000000 | 0xA0240D4C | 530 |
| 1.12.226 | reg : stream13_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240D50 | 530 |
| 1.12.227 | reg : stream13_err_maxsize_cntr_stat | 0x00000000 | 0xA0240D54 | 530 |
| 1.12.228 | reg : stream13_err_minsize_cntr_stat | 0x00000000 | 0xA0240D58 | 530 |
| 1.12.229 | reg : stream13_err_notlast_cntr_stat | 0x00000000 | 0xA0240D5C | 531 |
| 1.12.230 | reg : stream13_err_minipg_cntr_stat | 0x00000000 | 0xA0240D60 | 531 |
| 1.12.231 | reg : stream13_err_watchdog_cntr_stat | 0x00000000 | 0xA0240D64 | 531 |
| 1.12.232 | reg : stream13_exc_exprate_cntr_stat | 0x00000000 | 0xA0240D68 | 531 |
| 1.12.233 | reg : stream13_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA0240D6C | 531 |
| 1.12.234 | reg : stream13_rate_measured_stat | 0x00000000 | 0xA0240D70 | 531 |
| 1.12.235 | reg : tpg14_packet_rate_clks_ctrl | 0x00000823 | 0xA0240E34 | 532 |
| 1.12.236 | reg : tpg14_packet_size_clks | 0x00000040 | 0xA0240E38 | 532 |

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|---|---|---|---|---|
| | _ctrl | | | |
| 1.12.237 | reg : stream14_expsize_dis_ctrl | 0x00000040 | 0xA0240E3C | 532 |
| 1.12.238 | reg : stream14_exprate_dis_ctrl | 0x007F0040 | 0xA0240E40 | 532 |
| 1.12.239 | reg : stream14_err_stat | 0x00000000 | 0xA0240E44 | 532 |
| 1.12.240 | reg : stream14_err_expsize_cntr_stat | 0x00000000 | 0xA0240E48 | 533 |
| 1.12.241 | reg : stream14_err_pfifofull_cntr_stat | 0x00000000 | 0xA0240E4C | 533 |
| 1.12.242 | reg : stream14_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240E50 | 533 |
| 1.12.243 | reg : stream14_err_maxsize_cntr_stat | 0x00000000 | 0xA0240E54 | 533 |
| 1.12.244 | reg : stream14_err_minsize_cntr_stat | 0x00000000 | 0xA0240E58 | 533 |
| 1.12.245 | reg : stream14_err_notlast_cntr_stat | 0x00000000 | 0xA0240E5C | 533 |
| 1.12.246 | reg : stream14_err_minipg_cntr_stat | 0x00000000 | 0xA0240E60 | 533 |
| 1.12.247 | reg : stream14_err_watchdog_cntr_stat | 0x00000000 | 0xA0240E64 | 534 |
| 1.12.248 | reg : stream14_exc_exprate_cntr_stat | 0x00000000 | 0xA0240E68 | 534 |
| 1.12.249 | reg : stream14_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA0240E6C | 534 |
| 1.12.250 | reg : stream14_rate_measured_stat | 0x00000000 | 0xA0240E70 | 534 |
| 1.12.251 | reg : tpg15_packet_rate_clks_ctrl | 0x00000823 | 0xA0240F34 | 534 |
| 1.12.252 | reg : tpg15_packet_size_clks_ctrl | 0x00000040 | 0xA0240F38 | 534 |
| 1.12.253 | reg : stream15_expsize_dis_ctrl | 0x00000040 | 0xA0240F3C | 535 |
| 1.12.254 | reg : stream15_exprate_dis_ctrl | 0x007F0040 | 0xA0240F40 | 535 |
| 1.12.255 | reg : stream15_err_stat | 0x00000000 | 0xA0240F44 | 535 |
| 1.12.256 | reg : stream15_err_expsize_cntr_stat | 0x00000000 | 0xA0240F48 | 535 |
| 1.12.257 | reg : stream15_err_pfifofull_cntr_stat | 0x00000000 | 0xA0240F4C | 535 |
| 1.12.258 | reg : stream15_err_bfifofull_cntr_stat | 0x00000000 | 0xA0240F50 | 536 |
| 1.12.259 | reg : stream15_err_maxsize_cntr_stat | 0x00000000 | 0xA0240F54 | 536 |
| 1.12.260 | reg : stream15_err_minsize_cntr_stat | 0x00000000 | 0xA0240F58 | 536 |
| 1.12.261 | reg : stream15_err_notlast_cntr_stat | 0x00000000 | 0xA0240F5C | 536 |
| 1.12.262 | reg : stream15_err_minipg_cntr_stat | 0x00000000 | 0xA0240F60 | 536 |
| 1.12.263 | reg : stream15_err_watchdog_cntr_stat | 0x00000000 | 0xA0240F64 | 536 |
| 1.12.264 | reg : stream15_exc_exprate_cntr_stat | 0x00000000 | 0xA0240F68 | 536 |
| 1.12.265 | reg : stream15_exc_expratedeviate_cntr_stat | 0x00000000 | 0xA0240F6C | 537 |
| 1.12.266 | reg : stream15_rate_measured_stat | 0x00000000 | 0xA0240F70 | 537 |
| 1.13 | block : ipi_mcdma_axilite_pg288 | | 0xA1000000 - 0xA1001FFF | 537 |
| 1.13.1 | memory : ram_8kb_inst | | 0xA1000000, 0xA1000004 ... 0xA1001FFF | 537 |
| 1.13.1.1 | reg : ram_8kb_inst | 0x00000000 | 0xA1000000, 0x0000000000... | |
| 1.14 | block : ipi_gpio_cache_control | | 0xA2000000 - 0xA2000003 | 537 |
| 1.14.1 | reg : gpio_cache_control_inst | 0x0000002B | 0xA2000000 | 537 |
| 1.15 | block : ipi_mcdma_bd_ram | | 0xAA000000 - 0xAA007FFF | 537 |

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|---|---|---|---|---|
| 1.15.1 | memory : ram_32kb_inst | | 0xAA000000, 0xAA000004 ... 0xAA007FFF | 537 |
| 1.15.1.1 | reg : ram_32kb_inst | 0x00000000 | 0xAA000000, 0x0000000000... | |
| 1.16 | block : ipi_mcdma_debug_ram | | 0xAB000000 - 0xAB007FFF | 538 |
| 1.16.1 | memory : ram_32kb_inst | | 0xAB000000, 0xAB000004 ... 0xAB007FFF | 538 |
| 1.16.1.1 | reg : ram_32kb_inst | 0x00000000 | 0xAB000000, 0x0000000000... | |

## 1 dg_dtec_odf

Chip | 0x00000000 - 0xFFFFFFFFFF

Complete Register map HSI document for DTEC PL.

## 1.1 id_registers

Block | 0xA0000000 - 0xA000001B

### 1.1.1 proj_id

Reg. | 0xA0000000

This register defines the Project ID value

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | project_id | ro | na | 0x54726F6E | ASCII value for TRON |

### 1.1.2 firm_id

Reg. | 0xA0000004

This register defines the Firmware ID

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | firmware_id | ro | wo | X | Firmware ID for xTEC |

### 1.1.3 firm_build

Reg. | 0xA0000008

This register defines the Firmware build ID

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | firmware_build_id | ro | wo | X | This register is currently undefined in D000741068. Will be set after FPGA is built. |

### 1.1.4 fpga_id

Reg. | 0xA000000C

This regiser define the FPGA firmware image identifier. For example: F70.02.00 for a cTEC image for NXE 3800 phase 2 first release

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | fpga_type | ro | wo | X | Major product identifier. This field only identifies the major product and is treated and displayed as an ASCII character. cTEC is 0x46 or ASCII F |
| 23:16 | configuration | ro | wo | X | Major generation identification. This hex field is displayed as a decimal value by SW. NXE3800 is hex 0x46 or decimal 70. |
| 15:8 | major_revision | ro | wo | X | New features or capabilities definition. This hex field is displayed as a decimal value by SW. For phase 0 this value will be 00 in decimal. For phase 1 this value will be 01 in decimal. etc. |
| 7:0 | minor_revision | ro | wo | X | Minor revision definition. This field indicates bug fixes have been applied. For any new features/capabilities increment this field. |

### 1.1.5 fpga_build

Reg. | 0xA0000010

This register defines the FPGA_BUILD in ASCII

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | fpga_build_fiel d | ro | wo | X | |

### 1.1.6 tec_id

Reg. 0xA0000014

This register defines the TEC_ID to identify major product identifier and variations

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | major_product_i d | ro | wo | X | Major product identifier. This field only identifies the major product and is treated and displayed as an ASCII character. 0x43 for cTEC. 0x45 for eTEC |
| 23:16 | variation | ro | na | 0x0 | Variation field currently undefined. Shall be set to 0x00 |
| 15:8 | sub_variation | ro | na | 0x0 | Sub variation field currently undefined. Shall be set to 0x00 |
| 7:0 | spare | ro | na | 0x0 | Spare field currently undefined. Shall be set to 0x00 |

### 1.1.7 context_id

Reg. 0xA0000018

This register represents the CONTEXT ID value for port X76 of the cTEC

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | CID | ro | wo | X | 4-bit field for the context ID that is connected. 4'b1110 = eTEC, 4'b1101 = cTEC, 4'b1011 = dTEC |

## 1.2 core_registers_srdl

Block 0xA0010000 - 0xA0017FFF

Register map used to access and control global FPGA functionality

### 1.2.1 core_module_name

Reg. 0xA0010000

Defines the module name

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | module_name | ro | na | 0x636F7265 | ASCII code for module name - top module(core) = core |

### 1.2.2 core_module_version

Reg. 0xA0010004

Module version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | major_revision | ro | wo | 0x0 | Major Revisoin of module - New features or capabilities definition have been added. |
| 7:0 | minor_revision | ro | wo | 0x0 | Minor Revision of module. This field indicates bug fixes have been applied. For any new features/capabilities increment, this field will reset to zero. |

### 1.2.3 core_page_properties

Reg. 0xA0010008

Address page properties

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | present | ro | wo | 0x1 | Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not. |
| 30:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | page_size | ro | na | 0x1 | Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enetr here. |
| 7:0 | unified_header_ rev | ro | na | 0x1 | Unified Header Format common registers revision. |

### 1.2.4 core_scratchregister

Reg. 0xA001000C

Scratchregister register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchregister | rw | na | 0x12345678 | SW can write to it and read from it for test purposes. |

### 1.2.5 core_irq_enable

Reg. 0xA0010010

Interrupt Requests Enable/Mask Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_enable | rw | ro | 0x0 | IRQ0 enable bit. Used by MCDMA CH1 S2MM IRQ. Not in use in DTEC. |
| 1 | irq1_enable | rw | ro | 0x0 | IRQ1 enable bit. Used by MCDMA CH2 S2MM IRQ. Not in use in DTEC. |
| 2 | irq2_enable | rw | ro | 0x0 | IRQ2 enable bit. Used by MCDMA CH3 S2MM IRQ. Not in use in DTEC. |
| 3 | irq3_enable | rw | ro | 0x0 | IRQ3 enable bit. Used by MCDMA CH4 S2MM IRQ. Not in use in DTEC. |
| 4 | irq4_enable | rw | ro | 0x0 | IRQ4 enable bit. Used by MCDMA CH5 S2MM IRQ. Not in use in DTEC. |
| 5 | irq5_enable | rw | ro | 0x0 | IRQ5 enable bit. Used by MCDMA CH6 S2MM IRQ. Not in use in DTEC. |
| 6 | irq6_enable | rw | ro | 0x0 | IRQ6 enable bit. Used by MCDMA CH7 S2MM IRQ. Not in use in DTEC. |
| 7 | irq7_enable | rw | ro | 0x0 | IRQ7 enable bit. Used by MCDMA CH8 S2MM IRQ. Not in use in DTEC. |
| 8 | irq8_enable | rw | ro | 0x0 | IRQ8 enable bit. Used by MCDMA CH8 S2MM IRQ. Not in use in DTEC. |
| 9 | irq9_enable | rw | ro | 0x0 | IRQ9 enable bit. Used by MCDMA CH9 S2MM IRQ. Not in use in DTEC. |
| 10 | irq10_enable | rw | ro | 0x0 | IRQ10 enable bit. Used by MCDMA CH10 S2MM IRQ. Not in use in DTEC. |
| 11 | irq11_enable | rw | ro | 0x0 | IRQ11 enable bit. Used by MCDMA CH11 S2MM IRQ. Not in use in DTEC. |
| 12 | irq12_enable | rw | ro | 0x0 | IRQ12 enable bit. Used by MCDMA CH12 S2MM IRQ. Not in use in DTEC. |
| 13 | irq13_enable | rw | ro | 0x0 | IRQ13 enable bit. Used by MCDMA CH13 S2MM IRQ. Not in use in DTEC. |
| 14 | irq14_enable | rw | ro | 0x0 | IRQ14 enable bit. Used by MCDMA CH14 S2MM IRQ. Not in use in DTEC. |
| 15 | irq15_enable | rw | ro | 0x0 | IRQ15 enable bit. Used by MCDMA CH15 S2MM IRQ. Not in use in DTEC. |

### 1.2.6 core_irq_pending

Reg. 0xA0010014

Interrupt Pending Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_pending | r/w1c | wo | 0x0 | IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH1 S2MM IRQ. Not in use in DTEC. |
| 1 | irq1_pending | r/w1c | wo | 0x0 | IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH2 S2MM IRQ. Not in use in DTEC. |
| 2 | irq2_pending | r/w1c | wo | 0x0 | IRQ2 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH3 S2MM IRQ. Not in use in DTEC. |
| 3 | irq3_pending | r/w1c | wo | 0x0 | IRQ3 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH4 S2MM IRQ. Not in use in DTEC. |
| 4 | irq4_pending | r/w1c | wo | 0x0 | IRQ4 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH5 S2MM IRQ. Not in use in DTEC. |

| | | | | | |
|---|---|---|---|---|---|
| 5 | irq5_pending | r/w1c | wo | 0x0 | IRQ5 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH6 S2MM IRQ. Not in use in DTEC. |
| 6 | irq6_pending | r/w1c | wo | 0x0 | IRQ6 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH7 S2MM IRQ. Not in use in DTEC. |
| 7 | irq7_pending | r/w1c | wo | 0x0 | IRQ7 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH8 S2MM IRQ. Not in use in DTEC. |
| 8 | irq8_pending | r/w1c | wo | 0x0 | IRQ8 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH9 S2MM IRQ. Not in use in DTEC. |
| 9 | irq9_pending | r/w1c | wo | 0x0 | IRQ9 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH10 S2MM IRQ. Not in use in DTEC. |
| 10 | irq10_pending | r/w1c | wo | 0x0 | IRQ10 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH11 S2MM IRQ. Not in use in DTEC. |
| 11 | irq11_pending | r/w1c | wo | 0x0 | IRQ11 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH12 S2MM IRQ. Not in use in DTEC. |
| 12 | irq12_pending | r/w1c | wo | 0x0 | IRQ12 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH13 S2MM IRQ. Not in use in DTEC. |
| 13 | irq13_pending | r/w1c | wo | 0x0 | IRQ13 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH14 S2MM IRQ. Not in use in DTEC. |
| 14 | irq14_pending | r/w1c | wo | 0x0 | IRQ14 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH15 S2MM IRQ. Not in use in DTEC. |
| 15 | irq15_pending | r/w1c | wo | 0x0 | IRQ15 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH16 S2MM IRQ. Not in use in DTEC. |

### 1.2.7 core_irq_raw

Reg.

0xA0010018

Interrupt Raw Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_raw | ro | wo | 0x0 | IRQ0 raw status bit. Used by MCDMA CH1 S2MM IRQ. |
| 1 | irq1_raw | ro | wo | 0x0 | IRQ1 raw status bit.Used by MCDMA CH1 S2MM IRQ. |
| 2 | irq2_raw | ro | wo | 0x0 | IRQ2 raw status bit. Used by MCDMA CH3 S2MM IRQ. |
| 3 | irq3_raw | ro | wo | 0x0 | IRQ3 raw status bit.Used by MCDMA CH4 S2MM IRQ. |
| 4 | irq4_raw | ro | wo | 0x0 | IRQ4 raw status bit. Used by MCDMA CH5 S2MM IRQ. |
| 5 | irq5_raw | ro | wo | 0x0 | IRQ5 raw status bit.Used by MCDMA CH6 S2MM IRQ. |
| 6 | irq6_raw | ro | wo | 0x0 | IRQ6 raw status bit. Used by MCDMA CH6 S2MM IRQ. |
| 7 | irq7_raw | ro | wo | 0x0 | IRQ7 raw status bit.Used by MCDMA CH8 S2MM IRQ. |
| 8 | irq8_raw | ro | wo | 0x0 | IRQ8 raw status bit. Used by MCDMA CH9 S2MM IRQ. |
| 9 | irq9_raw | ro | wo | 0x0 | IRQ9 raw status bit.Used by MCDMA CH10 S2MM IRQ. |
| 10 | irq10_raw | ro | wo | 0x0 | IRQ10 raw status bit. Used by MCDMA CH11 S2MM IRQ. |
| 11 | irq11_raw | ro | wo | 0x0 | IRQ11 raw status bit.Used by MCDMA CH12 S2MM IRQ. |
| 12 | irq12_raw | ro | wo | 0x0 | IRQ12 raw status bit. Used by MCDMA CH13 S2MM IRQ. |
| 13 | irq13_raw | ro | wo | 0x0 | IRQ13 raw status bit.Used by MCDMA CH14 S2MM IRQ. |
| 14 | irq14_raw | ro | wo | 0x0 | IRQ14 raw status bit. Used by MCDMA CH15 S2MM IRQ. |
| 15 | irq15_raw | ro | wo | 0x0 | IRQ15 raw status bit.Used by MCDMA CH16 S2MM IRQ. |

### 1.2.8 core_irq_force

Reg.

0xA001001C

Interrupt Force Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH1 S2MM IRQ. Not in use on DTEC. |

| | | | | | |
|---|---|---|---|---|---|
| 1 | irq1_force | rw | ro | 0x0 | IRQ1 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH2 S2MM IRQ. Not in use on DTEC. |
| 2 | irq2_force | rw | ro | 0x0 | IRQ2 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH3 S2MM IRQ. Not in use on DTEC. |
| 3 | irq3_force | rw | ro | 0x0 | IRQ3 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH4 S2MM IRQ. Not in use on DTEC. |
| 4 | irq4_force | rw | ro | 0x0 | IRQ force bit. SW to write '1' to emulate an interrupt. Write '5' to clear. Used by MCDMA CH5 S2MM IRQ. Not in use on DTEC. |
| 5 | irq5_force | rw | ro | 0x0 | IRQ5 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH6 S2MM IRQ. Not in use on DTEC. |
| 6 | irq6_force | rw | ro | 0x0 | IRQ6 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH7 S2MM IRQ. Not in use on DTEC. |
| 7 | irq7_force | rw | ro | 0x0 | IRQ7 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH8 S2MM IRQ. Not in use on DTEC. |
| 8 | irq8_force | rw | ro | 0x0 | IRQ8 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH9 S2MM IRQ. Not in use on DTEC. |
| 9 | irq9_force | rw | ro | 0x0 | IRQ9 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH10 S2MM IRQ. Not in use on DTEC. |
| 10 | irq10_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH11 S2MM IRQ. Not in use on DTEC. |
| 11 | irq11_force | rw | ro | 0x0 | IRQ11 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH12 S2MM IRQ. Not in use on DTEC. |
| 12 | irq12_force | rw | ro | 0x0 | IRQ12 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH13 S2MM IRQ. Not in use on DTEC. |
| 13 | irq13_force | rw | ro | 0x0 | IRQ13 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH14 S2MM IRQ. Not in use on DTEC. |
| 14 | irq14_force | rw | ro | 0x0 | IRQ14 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH15 S2MM IRQ. Not in use on DTEC. |
| 15 | irq15_force | rw | ro | 0x0 | IRQ15 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH16 S2MM IRQ. Not in use on DTEC. |

### 1.2.9 build_time


0xA0010040

FPGA Build Time

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | build_time | ro | na | 0xDEADC0DE | FPGA Build time hh-mm-ss using 24h format. All numbers are decimal but stored without conversion to hex. Automatically generated during compilation. |

### 1.2.10 build_date


0xA0010044

FPGA Build Date

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | build_date | ro | na | 0xDEADC0DE | FPGA Build Date yy-mm-dd. All numbers are decimal but stored without conversion to hex. Automatically generated during compilation. |

### 1.2.11 build_githash


0xA0010048

FPGA Build GIT Hash

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | build_githash | ro | na | 0xDEADC0DE | FPGA Build GIT hash, the first 8 Bytes of the commit hash. All numbers are in hex. Automatically generated during comilation. |

### 1.2.12 uptime

Reg. 0xA0010054

Uptime

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | uptime | ro | na | 0x0 | Uptime - measured in seconds |

### 1.2.13 freerun_counter_stat

Reg. 0xA0010060

Free running counter status

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | freerun_counter | rw | na | 0x0 | Current free running counter at 125MHz. Can be used for software profiling. |

### 1.2.14 resets_ctrl

Reg. 0xA0010064

Major DTEC modules resets, controlled by SW

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | resets | rw | ro | 0x0 | Major DTEC modules resets controlled by SW, check DTEC EDS D001264457 for details.<br>Reset signal - 1 = reset / 0 = no reset<br>Bit Reset Signal name Signal Clock Domain Module Name Short Description<br>0 core_reset ps_clk125 Core DTEC Core module, deisgn top level equivalent<br>1 algo_reset ps_clk125 Algo Matalb algorithm and interfaces status and control<br>2 clkalgo_reset ps_clkalgo Algo Matlab algorithm slow clock logic<br>3 tselclient_reset ps_clk125 TSEL Client TSEL Client facing ETEC status and control<br>4 tselbridge_reset ps_clk125 TSEL Bridge TSEL Bridge facing DAMP status and control<br>5 clk50_reset ps_clk50 TSEL GDB TSEL GDB reconfiguration clock domain<br>6 eth1ge_reset ps_clk125 1G Ethernet 1GE interface towards LC<br>7 mcdma_reset ps_clk125 MCDMA IP Xilinx MCDMA IP<br>8 mcdmafeed_reset ps_clk125 MCDMA Feed MCDMA streams shaping logic<br>9 bpam2dcm_reset ps_clk125 BPAM2 DCM BPAM 2 (DCM) interface status and control<br>10 bpam3mmdc_reset ps_clk125 BPAM3 MMDC BPAM 3 (MMDC) interface status and control<br>11 todlts_reset ps_clk125 TOD LTS TOD and LTS maintaing<br>12 dampregs_reset ps_clk125 DAMP Registers data received from DAMP<br>13-31 <reserved><br>Writing to this register '1' will apply reset, writing '0' will remove the reset.<br>Reading the register will indicate the reset status, it might be updated a few clocks later after it is manipulted by SW. |

### 1.2.15 refclk_freq50mhz_stat

Reg. 0xA0010068

50MHz Clock pulses, measured for 1s.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | refclk_freq50mhz | ro | wo | 0x0 | Frequency of 50MHz clock in Hz. Represents the number of clocks captured for 1 second. Has to be converted from Hex to decimal. |

### 1.2.16 refclk_freqalgo_stat

Reg. 0xA001006C

Algo Clock pulses, measured for 1s.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | refclk_freqalgo | ro | wo | 0x0 | Frequency of Algo clock in Hz. Represents the number of clocks captured for 1 second. Has to be converted from Hex to decimal. |

### 1.2.17 debug_ctrl

Reg. 0xA0010070

Debug Control

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | debug | rw | ro | 0x0 | Current debug bus driven value - for temporary debug functionality |

### 1.2.18 debug_stat

Reg. 0xA0010074

Debug Status

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | debug | ro | wo | 0x0 | current debug bus status - NOTE: software should debounce the read value |

### 1.2.19 tod_load_low

Reg. 0xA0010080

TOD Load Low

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tod_load_low | rw | ro | 0x0 | Lower 32 bits written to TOD by PS |

### 1.2.20 tod_load_high

Reg. 0xA0010084

TOD Load High

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tod_load_high | rw | ro | 0x0 | Upper 32 bits written to TOD by PS |

### 1.2.21 tod_cntr_low

Reg. 0xA0010088

TOD Counter Low

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tod_cntr_low | ro | wo | 0x0 | Lower 32 bits of TOD counter read by PS. Caution: these lower 32 bits rollover every second. No mechanism is currently implemented to make this read coherent with tod_cntr_high. |

### 1.2.22 tod_cntr_high

Reg. 0xA001008C

TOD Counter High

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tod_cntr_high | ro | wo | 0x0 | Upper 32 bits of TOD counter read by PS |

### 1.2.23 lts_cntr

Reg. 0xA0010090

LTS Counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lts_cntr | ro | wo | 0x0 | LTS counter read by PS |

### 1.2.24 tod_incr

Reg. 0xA0010094

TOD Increment

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tod_incr | rw | ro | 0x225C01 | Number of LSBs to increment the TOD counter each clock period. Resolution is 2^-48 sec/LSB. 32'h00225C17 ~= 8ns per clock. |

### 1.2.25 led_control

Reg. 0xA00100A0

LED Control

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:6 | status_led | rw | ro | 0x2 | Status LED: 0x0 = OFF, 0x1 = Red, 0x2 = Green, 0x3 = Orange |
| 5:4 | state_led | rw | ro | 0x2 | State LED: 0x0 = OFF, 0x1 = Red, 0x2 = Green, 0x3 = Orange |
| 3:2 | fault_led | rw | ro | 0x2 | Fault LED: 0x0 = OFF, 0x1 = Red, 0x2 = Green, 0x3 = Orange |
| 1:0 | master_led | rw | ro | 0x2 | Master LED: 0x0 = OFF, 0x1 = Red, 0x2 = Green, 0x3 = Orange |

### 1.2.26 damp_to_algo_snoop_xfer_count

Reg. 0xA00100B0

Counts the number of AXIS Snooper Output Packets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Counter |

### 1.2.27 damp_to_algo_snoop_drop_count

Reg. 0xA00100B4

Counts the number of AXIS Snooper Dropped Packets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Counter |

### 1.2.28 damp_to_algo_snoop_tout_count

Reg. 0xA00100B8

Counts the number of AXIS Snooper Timeouts Packets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Counter |

### 1.2.29 esm_to_algo_snoop_xfer_count

Reg. 0xA00100BC

Counts the number of AXIS Snooper Output Packets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Counter |

### 1.2.30 esm_to_algo_snoop_drop_count

Reg. 0xA00100C0

Counts the number of AXIS Snooper Dropped Packets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Counter |

### 1.2.31 esm_to_algo_snoop_tout_count

Reg. 0xA00100C4

Counts the number of AXIS Snooper Timeouts Packets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Counter |

### 1.2.32 damp_diag_region

damp_diag_region 0xA0014000, 0xA0014004 ... 0xA0017FFF

| offset | | depth | 4096 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to read DAMP Diagnostic Data from the TSEL Bridge

## 1.3 algo_ing_registers_srdl

Block 0xA0020000 - 0xA00206CB

Register map of the ingress algo registers

### 1.3.1 algo_ingress_module_name

Reg. 0xA0020000

Defines the module name

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | module_name | ro | na | 0x69616C67 | ASCII code for module name - top module(core) = core |

### 1.3.2 algo_ingress_module_version

Reg. 0xA0020004

Module version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:16 | rfu | ro | na | 0x0 | Reserved for Future Use - RFU |
| 15:8 | major_revision | ro | na | 0x0 | Major Revision |
| 7:0 | minor_revision | ro | na | 0x0 | Minor Revision |

### 1.3.3 algo_ingress_page_properties

Reg. 0xA0020008

Address page properties

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | present | ro | wo | 0x1 | Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not. |
| 30:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | page_size | ro | na | 0x1 | Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enter here. |
| 7:0 | unified_header_rev | ro | na | 0x1 | Unified Header Format common registers revision. |

### 1.3.4 algo_ingress_scratchregister

Reg. 0xA002000C

Scratchregister register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchregister | rw | na | 0x12345678 | SW can write to it and read from it for test purposes. |

### 1.3.5 algo_ingress_irq_enable

Reg. 0xA0020010

Interrupt Requests Enable/Mask Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_enable | rw | ro | 0x0 | IRQ0 enable bit. Not implemented here/DTEC |
| 1 | irq1_enable | rw | ro | 0x0 | IRQ1 enable bit. Not implemented here/DTEC |

### 1.3.6 algo_ingress_irq_pending

Reg. 0xA0020014

Interrupt Pending Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_pending | r/w1c | wo | 0x0 | IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |
| 1 | irq1_pending | r/w1c | wo | 0x0 | IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |

### 1.3.7 algo_ingress_irq_raw

Reg. 0xA0020018

Interrupt Raw Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_raw | ro | wo | 0x0 | IRQ0 raw status bit. Not implemented here/DTEC |
| 1 | irq1_raw | ro | wo | 0x0 | IRQ1 raw status bit. Not implemented here/DTEC |

### 1.3.8 algo_ingress_irq_force

Reg. 0xA002001C

Interrupt Force Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC |
| 1 | irq1_force | rw | ro | 0x0 | IRQ1 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC |

### 1.3.9 machineconstants_clst_thr_pkval_low_perc

Reg. 0xA0020020

For small peak removal after main droplets clustering. This is the 2nd time of applying such threshold, refer to table 2.2 for 1st time;

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_pkval_low_perc | rw | ro | 0x7AE | For small peak removal after main droplets clustering. This is the 2nd time of applying such threshold, refer to table 2.2 for 1st time; |

### 1.3.10 machineconstants_clst_thr_neighbor_perc

Reg. 0xA0020024

For main droplets peak clustering, window size around new pivots; if the module is performing TF measurement, this parameter need to be modified, refer to section 5 (Calibration CPD)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_neighbor_perc | rw | ro | 0xCCD | For main droplets peak clustering, window size around new pivots; if the module is performing TF measurement, this parameter need to be modified, refer to section 5 (Calibration CPD) |

### 1.3.11 machineconstants_clst_thr_dist2antinode_perc

Reg. 0xA0020028

Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_dist2antinode_perc | rw | ro | 0x599A | Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing |

### 1.3.12 machineconstants_clst_km_nearcluster

Reg. 0xA002002C

pkVal ratio for merging close-by clusters for K-mean algorithm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_km_nearcluster | rw | ro | 0x599A | pkVal ratio for merging close-by clusters for K-mean algorithm |

### 1.3.13 machineconstants_clst_em_wt_pkpos

Reg. 0xA0020030

Weight factor for the peak position term in the GMM probability distribution used in EM;

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_wt_pkpos | rw | ro | 0xC000 | Weight factor for the peak position term in the GMM probability distribution used in EM; |

### 1.3.14 machineconstants_clst_em_centroiddist

Reg. 0xA0020034

Centroid distance for merging clusters;

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_centroiddist | rw | ro | 0x199A | Centroid distance for merging clusters; |

### 1.3.15 machineconstants_clst_em_thr_pkval_pivot_perc

Reg. 0xA0020038

Terminate condition for main droplets clustering.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_thr_pkval_pivot_perc | rw | ro | 0xC000 | Terminate condition for main droplets clustering. |

### 1.3.16 machineconstants_clst_em_maxclustersize

Reg. 0xA002003C

Cluster size threshold for merging clusters;

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_maxclustersize | rw | ro | 0xB333 | Cluster size threshold for merging clusters; |

### 1.3.17 machineconstants_clst_em_ds500

Reg. 0xA0020040

Threshold (% of DS) for relabel close by intermediate droplet clusters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_ds500 | rw | ro | 0x9000 | Threshold (% of DS) for relabel close by intermediate droplet clusters |

### 1.3.18 machineconstants_clst_em_ds2m

Reg. 0xA0020044

Threshold (% of DS) for relabel close by intermediate droplet clusters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_ds2m | rw | ro | 0x4829 | Threshold (% of DS) for relabel close by intermediate droplet clusters |

### 1.3.19 machineconstants_clst_em_minclustersize

Reg. 0xA0020048

Cluster size threshold for merging clusters;

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_minclustersize | rw | ro | 0x3333 | Cluster size threshold for merging clusters; |

### 1.3.20 machineconstants_clst_em_maxdist2clustercenter_pkpos

Reg. 0xA002004C

Distance to centroid for merging clusters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_maxdist2clustercenter_pkpos | rw | ro | 0xCCD | Distance to centroid for merging clusters |

### 1.3.21 machineconstants_clst_em_delta_pkpos

Reg. 0xA0020050

Criteria for merging clusters based on pkPos

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_em_delta_pkpos | rw | ro | 0x28F | Criteria for merging clusters based on pkPos |

### 1.3.22 machineconstants_clst_fl_thr_pkval_2m_smaller_bound

Reg. 0xA0020054

Threshold for relabeling outliers as presubdroplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_fl_thr_pkval_2m_smaller_bound | rw | ro | 0xFF3 | Threshold for relabeling outliers as presubdroplets |

### 1.3.23 machineconstants_clst_fl_thr_pkval_500_2m_bound

Reg. 0xA0020058

Threshold for relabeling outliers as subdroplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_fl_thr_pkval_500_2m_bound | rw | ro | 0x2DCC | Threshold for relabeling outliers as subdroplets |

### 1.3.24 machineconstants_clst_bpam_fsamp

Reg. 0xA002005C

Sampling frequency from DCM BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_bpam_fsa | rw | ro | 0x7735940 | Sampling frequency from DCM BPAM |

| | | | | | |
|---|---|---|---|---|---|
| | mp | | | | |

### 1.3.25 machineconstants_clst_thr_pkval_low_ddm_perc

Reg. 0xA0020060

For small peak removal after main droplets clustering. This is the 2nd time of applying such threshold, refer to table 2.2 for 1st time;

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_pkval_low_ddm_perc | rw | ro | 0x7AE | For small peak removal after main droplets clustering. This is the 2nd time of applying such threshold, refer to table 2.2 for 1st time; |

### 1.3.26 machineconstants_clst_thr_neighbor_ddm_perc

Reg. 0xA0020064

For main droplets peak clustering, window size around new pivots; if the module is performing TF measurement, this parameter need to be modified, refer to section 5 (Calibration CPD)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_neighbor_ddm_perc | rw | ro | 0x2E14 | For main droplets peak clustering, window size around new pivots; if the module is performing TF measurement, this parameter need to be modified, refer to section 5 (Calibration CPD) |

### 1.3.27 machineconstants_clst_thr_dist2antinode_ddm_perc

Reg. 0xA0020068

Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_dist2antinode_ddm_perc | rw | ro | 0x7333 | Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing |

### 1.3.28 machineconstants_clst_fl_thr_pkval_500_2m_ddm_bound

Reg. 0xA002006C

Threshold for labeling ddm peaks as subdroplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_fl_thr_pkval_500_2m_ddm_bound | rw | ro | 0x2DCC | Threshold for labeling ddm peaks as subdroplets |

### 1.3.29 machineconstants_clst_thr_pkval_low_tfdcm_perc

Reg. 0xA0020070

For small peak removal after main droplets clustering in TF mode for DCM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_pkval_low_tfdcm_perc | rw | ro | 0x199A | For small peak removal after main droplets clustering in TF mode for DCM |

### 1.3.30 machineconstants_clst_thr_dist2antinode_tfdcm_perc

Reg. 0xA0020074

Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing, DCM, TF mode

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_thr_dist2antinode_tfdcm_perc | rw | ro | 0x8000 | Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing, DCM, TF mode |

### 1.3.31 machineconstants_clst_multsatrate_dthr

Reg. 0xA0020078

Threshold for D to calculate mult-satellite ratio

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_multsatrate_dthr | rw | ro | 0x0 | Threshold for D to calculate mult-satellite ratio |

### 1.3.32 machineconstants_clst_dcm_pkvalue_max

Reg. 0xA002007C

Maximum allowed pkValue before detecting pkSaturation

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_dcm_pkvalue_max | rw | ro | 0x20000 | Maximum allowed pkValue before detecting pkSaturation |

### 1.3.33 machineconstants_clst_ddm_pkvalue_max

Reg. 0xA0020080

Maximum allowed pkValue before detecting pkSaturation

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_clst_ddm_pkvalue_max | rw | ro | 0x20000 | Maximum allowed pkValue before detecting pkSaturation |

### 1.3.34 atomic_group1_en

Reg. 0xA0020084

Atomic Group1 Enable SW writes 0x0000_0001 to transfer atomic group data to algo

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | atomic_group1_en | rw | rw | 0x0 | Atomic Group1 Enable SW writes 0x0000_0001 to transfer atomic group data to algo |

### 1.3.35 req_func

Reg. 0xA0020088

MSC requested function

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | req_func | rw | ro | 0x0 | MSC requested function |

### 1.3.36 idcb_manual

Reg. 0xA002008C

Manual trigger signal for IDCB channels

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | idcb_manual | rw | ro | 0x0 | Manual trigger signal for IDCB channels |

### 1.3.37 events_in_events_bank1_ack

Reg. 0xA0020090

Acknowledgement signal from PS to clear events in bank1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | events_in_events_bank1_ack | rw | ro | 0x0 | Acknowledgement signal from PS to clear events in bank1 |

### 1.3.38 events_in_events_bank2_ack

Reg. 0xA0020094

Acknowledgement signal from PS to clear events in bank2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | events_in_events_bank2_ack | rw | ro | 0x0 | Acknowledgement signal from PS to clear events in bank2 |

### 1.3.39 disable_intermitent_tuning

Reg. 0xA0020098

Disables subclupdates that may interfere with other CPDS

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | disable_intermitent_tuning | rw | ro | 0x0 | Disables subclupdates that may interfere with other CPDS |

### 1.3.40 ps2pl_cal_bdo_f2_opt

Reg. 0xA002009C

Base droplet optimization Optimal f2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_bdo_f2_opt | rw | ro | 0x0 | Base droplet optimization Optimal f2 |

### 1.3.41 ps2pl_cal_bdo_dc_opt

Reg. 0xA00200A0

Base Droplet Optimization Optimum Duty Cycle

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_bdo_dc_opt | rw | ro | 0x0 | Base Droplet Optimization Optimum Duty Cycle |

### 1.3.42 ps2pl_cal_dcm_qc_pass

Reg. 0xA00200A4

DCM Quality Check. 1-Pass, 0-Fail

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_dcm_qc_pass | rw | ro | 0x1 | DCM Quality Check. 1-Pass, 0-Fail |

### 1.3.43 ps2pl_cal_ps_general_error_reg

Reg. 0xA00200A8

PS General Error Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_ps_general_error_reg | rw | ro | 0x0 | PS General Error Register |

### 1.3.44 ps2pl_cal_advcmd

Reg. 0xA00200AC

Advanced command

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_advcmd | rw | ro | 0x0 | Advanced command |

### 1.3.45 ps2pl_cal_spare1

Reg. 0xA00200B0

PS2PL spare signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_spare 1 | rw | ro | 0x0 | PS2PL spare signal |

### 1.3.46 ps2pl_cal_spare2

Reg. 0xA00200B4

PS2PL spare signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_spare 2 | rw | ro | 0x0 | PS2PL spare signal |

### 1.3.47 ps2pl_cal_spare3

Reg. 0xA00200B8

PS2PL spare signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ps2pl_cal_spare 3 | rw | ro | 0x0 | PS2PL spare signal |

### 1.3.48 machineconstants_idc_dphi1

Reg. 0xA00200BC

Inline Tuning parameter: dphi1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_dphi1 | rw | ro | 0x666 | Inline Tuning parameter: dphi1 |

### 1.3.49 machineconstants_idc_dphi0

Reg. 0xA00200C0

Inline Tuning parameter: dphi0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_dphi0 | rw | ro | 0x666 | Inline Tuning parameter: dphi0 |

### 1.3.50 machineconstants_idc_presubthershold

Reg. 0xA00200C4

Inline Tuning parameter: preSubThershold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_presubthe rshold | rw | ro | 0xCCD | Inline Tuning parameter: preSubThershold |

### 1.3.51 machineconstants_idc_presubaveragethershold

Reg. 0xA00200C8

Inline Tuning parameter: preSubAverageThershold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_presubave ragethershold | rw | ro | 0x147AE14 | Inline Tuning parameter: preSubAverageThershold |

### 1.3.52 machineconstants_idc_xint3sigmaaveragedthershold

Reg. 0xA00200CC

Inline Tuning parameter: xint3SigmaAveragedThershold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_xint3sigm aaveragedthersh | rw | ro | 0x6666 | Inline Tuning parameter: xint3SigmaAveragedThershold |

| | | | | | |
|---|---|---|---|---|---|
| | old | | | | |

### 1.3.53 machineconstants_idc_satratioaveragethreshold_off

Reg. 0xA00200D0

Inline Tuning parameter: satRatioAverageThreshold off droplet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_satratioaveragethreshold_off | rw | ro | 0x147AE14 | Inline Tuning parameter: satRatioAverageThreshold off droplet |

### 1.3.54 machineconstants_idc_satratiothreshold

Reg. 0xA00200D4

Inline Tuning parameter: satRatioThreshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_satratiothreshold | rw | ro | 0xCCD | Inline Tuning parameter: satRatioThreshold |

### 1.3.55 machineconstants_idc_monitoringcountermax

Reg. 0xA00200D8

Inline Tuning parameter: monitoringCounterMax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_monitoringcountermax | rw | ro | 0x927C0 | Inline Tuning parameter: monitoringCounterMax |

### 1.3.56 machineconstants_idc_monitorinitialcounter

Reg. 0xA00200DC

Inline Tuning parameter: monitorInitialCounter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_monitorinitialcounter | rw | ro | 0xA | Inline Tuning parameter: monitorInitialCounter |

### 1.3.57 machineconstants_idc_kl

Reg. 0xA00200E0

Inline Tuning parameter: KL

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_kl | rw | ro | 0x4000 | Inline Tuning parameter: KL |

### 1.3.58 machineconstants_idc_kt

Reg. 0xA00200E4

Inline Tuning parameter: KT

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_kt | rw | ro | 0x4000 | Inline Tuning parameter: KT |

### 1.3.59 machineconstants_idc_kc

Reg. 0xA00200E8

Inline Tuning parameter: KC

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant | rw | ro | 0xFFFFC000 | Inline Tuning parameter: KC |

| | | | | | |
|---|---|---|---|---|---|
| | s_idc_kc | | | | |

### 1.3.60 machineconstants_idc_kd

Reg. 0xA00200EC

Inline Tuning parameter: KD

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_kd | rw | ro | 0xFFFFC000 | Inline Tuning parameter: KD |

### 1.3.61 machineconstants_idc_lt

Reg. 0xA00200F0

Inline Tuning parameter: LT

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_lt | rw | ro | 0x4000 | Inline Tuning parameter: LT |

### 1.3.62 machineconstants_idc_tt

Reg. 0xA00200F4

Inline Tuning parameter: TT

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_tt | rw | ro | 0x2000 | Inline Tuning parameter: TT |

### 1.3.63 machineconstants_idc_ct

Reg. 0xA00200F8

Inline Tuning parameter: cT

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ct | rw | ro | 0x4000 | Inline Tuning parameter: cT |

### 1.3.64 machineconstants_idc_dt

Reg. 0xA00200FC

Inline Tuning parameter: Target for DC/DPHI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dt | rw | ro | 0xFFFFF000 | Inline Tuning parameter: Target for DC/DPHI |

### 1.3.65 machineconstants_idc_td

Reg. 0xA0020100

Inline Tuning parameter: Desired DC/DPHI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_td | rw | ro | 0xFFFFE666 | Inline Tuning parameter: Desired DC/DPHI |

### 1.3.66 machineconstants_idc_d_thr

Reg. 0xA0020104

Inline Tuning parameter: d Threshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_d_thr | rw | ro | 0x0 | Inline Tuning parameter: d Threshold |

### 1.3.67 machineconstants_idc_maincliteration

Reg. 0xA0020108

Inline Tuning parameter: MainCLIteration

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_mainclite ration | rw | ro | 0x64 | Inline Tuning parameter: MainCLIteration |

### 1.3.68 machineconstants_idc_tuningintervalstimemax

Reg. 0xA002010C

Inline Tuning parameter: tuningIntervalsTimeMax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_tuningintervalstimemax | rw | ro | 0xA | Inline Tuning parameter: tuningIntervalsTimeMax |

### 1.3.69 machineconstants_idc_phasecorrectionphi0

Reg. 0xA0020110

Inline Tuning parameter: phaseCorrectionPhi0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_phasecorrectionphi0 | rw | ro | 0x19A | Inline Tuning parameter: phaseCorrectionPhi0 |

### 1.3.70 machineconstants_idc_phasecorrectionphi1

Reg. 0xA0020114

Inline Tuning parameter: phaseCorrectionPhi1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_phasecorrectionphi1 | rw | ro | 0x19A | Inline Tuning parameter: phaseCorrectionPhi1 |

### 1.3.71 machineconstants_idc_amplitudereduction

Reg. 0xA0020118

Inline Tuning parameter: amplitudeReduction

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_amplitudereduction | rw | ro | 0x39A | Inline Tuning parameter: amplitudeReduction |

### 1.3.72 machineconstants_idc_a0max

Reg. 0xA002011C

Inline Tuning parameter: A0Max

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_a0max | rw | ro | 0x5000 | Inline Tuning parameter: A0Max |

### 1.3.73 machineconstants_idc_a0min

Reg. 0xA0020120

Inline Tuning parameter: A0Min

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_a0min | rw | ro | 0x66 | Inline Tuning parameter: A0Min |

### 1.3.74 machineconstants_idc_a1max

Reg. 0xA0020124

Inline Tuning parameter: A1Max

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_a1max | rw | ro | 0x5000 | Inline Tuning parameter: A1Max |

### 1.3.75 machineconstants_idc_a1min

Reg. 0xA0020128

Inline Tuning parameter: A1Min

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_a1min | rw | ro | 0x66 | Inline Tuning parameter: A1Min |

### 1.3.76 machineconstants_idc_voltagemax

Reg. 0xA002012C

Inline Tuning parameter: voltageMax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_voltagemax | rw | ro | 0x10400 | Inline Tuning parameter: voltageMax |

### 1.3.77 machineconstants_idc_lmargin

Reg. 0xA0020130

Inline Tuning parameter: LMargin

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_lmargin | rw | ro | 0x28F | Inline Tuning parameter: LMargin |

### 1.3.78 machineconstants_idc_tmargin

Reg. 0xA0020134

Inline Tuning parameter: TMargin

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_tmargin | rw | ro | 0x28F | Inline Tuning parameter: TMargin |

### 1.3.79 machineconstants_idc_cmargin

Reg. 0xA0020138

Inline Tuning parameter: CMargin

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_cmargin | rw | ro | 0x28F | Inline Tuning parameter: CMargin |

### 1.3.80 machineconstants_idc_dmargin

Reg. 0xA002013C

Inline Tuning parameter: Margin for DCDPHI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dmargin | rw | ro | 0x28F | Inline Tuning parameter: Margin for DCDPHI |

### 1.3.81 machineconstants_idc_subclcountermax

Reg. 0xA0020140

Inline Tuning parameter: subCLCounterMax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_subclcountermax | rw | ro | 0xA | Inline Tuning parameter: subCLCounterMax |

### 1.3.82 machineconstants_idc_peakmissedratethreshold

Reg. 0xA0020144

Inline Tuning parameter: peakMissedRateThreshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_peakmissedratethreshold | rw | ro | 0xCCD | Inline Tuning parameter: peakMissedRateThreshold |

### 1.3.83 machineconstants_idc_multsatratiothreshold

Reg. 0xA0020148

Inline Tuning parameter: multSatRatioThreshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_multsatratiothreshold | rw | ro | 0xCCD | Inline Tuning parameter: multSatRatioThreshold |

### 1.3.84 machineconstants_idc_sigmacthreshold

Reg. 0xA002014C

Inline Tuning parameter: sigmaCThreshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_sigmacthreshold | rw | ro | 0xCCD | Inline Tuning parameter: sigmaCThreshold |

### 1.3.85 machineconstants_idc_sigmalthreshold

Reg. 0xA0020150

Inline Tuning parameter: sigmaLThreshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_sigmalthreshold | rw | ro | 0x148 | Inline Tuning parameter: sigmaLThreshold |

### 1.3.86 machineconstants_idc_falltimedetectionmax

Reg. 0xA0020154

Inline Tuning parameter: exposureMonitorIterationMax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_falltimedetectionmax | rw | ro | 0x3E8 | Inline Tuning parameter: exposureMonitorIterationMax |

### 1.3.87 machineconstants_idc_averaginglength

Reg. 0xA0020158

Inline Tuning parameter: Averaging Length

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_averaginglength | rw | ro | 0x7D0 | Inline Tuning parameter: Averaging Length |

### 1.3.88 machineconstants_idc_maincl_holdoffcounter

Reg. 0xA002015C

Inline Tuning parameter: MainCL update holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_maincl_holdoffcounter | rw | ro | 0x7 | Inline Tuning parameter: MainCL update holdoff |

### 1.3.89 machineconstants_idc_subclopt_holdoffcounter

Reg. 0xA0020160

Inline Tuning parameter: SubCL Update Opt Holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_subclopt_holdoffcounter | rw | ro | 0x5 | Inline Tuning parameter: SubCL Update Opt Holdoff |

### 1.3.90 machineconstants_idc_subclbk_holdoffcounter

Reg. 0xA0020164

Inline Tuning parameter: SubCL Bk Update Holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_subclbk_holdoffcounter | rw | ro | 0x7 | Inline Tuning parameter: SubCL Bk Update Holdoff |

### 1.3.91 machineconstants_idc_exposure_earlyexposurethreshold

Reg. 0xA0020168

Exposure parameter: Early Exposure Threshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_exposure_earlyexposurethreshold | rw | ro | 0x0 | Exposure parameter: Early Exposure Threshold |

### 1.3.92 machineconstants_idc_idcbtriggerconfig

Reg. 0xA002016C

Configuration word for IDCB Triggers

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_idcbtriggerconfig | rw | ro | 0x0 | Configuration word for IDCB Triggers |

### 1.3.93 machineconstants_idc_monitoringcountersafedamp

Reg. 0xA0020170

Number of iterations to wait in monitoring before updating SafeDAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_monitoringcountersafedamp | rw | ro | 0xB | Number of iterations to wait in monitoring before updating SafeDAMP |

### 1.3.94 machineconstants_idc_exposuremonitoringcountermax

Reg. 0xA0020174

Number of iterations to wait for exposure signal to go high

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_exposuremonitoringcountermax | rw | ro | 0xA | Number of iterations to wait for exposure signal to go high |

### 1.3.95 machineconstants_idc_dcmbpam2dtec_crcerrthr

Reg. 0xA0020178

Threshold for CRC errors coming from DCM BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dcmbpam2dtec_crcerrthr | rw | ro | 0x6 | Threshold for CRC errors coming from DCM BPAM |

### 1.3.96 machineconstants_idc_ddmbpam2dtec_crcerrthr

Reg. 0xA002017C

Threshold for CRC errors coming from DDM BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ddmbpam2dtec_crcerrthr | rw | ro | 0x6 | Threshold for CRC errors coming from DDM BPAM |

### 1.3.97 machineconstants_idc_dcmbpam2dtec_minnumvalidpks_thr

Reg. 0xA0020180

Threshold for minimum number of valid PDS packets coming from DCM BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dcmbpam2dtec_minnumvalidpks_thr | rw | ro | 0x32 | Threshold for minimum number of valid PDS packets coming from DCM BPAM |

### 1.3.98 machineconstants_idc_ddmbpam2dtec_minnumvalidpks_thr

Reg. 0xA0020184

Threshold for minimum number of valid PDS packets coming from DDM BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ddmbpam2dtec_minnumvalidpks_thr | rw | ro | 0x32 | Threshold for minimum number of valid PDS packets coming from DDM BPAM |

### 1.3.99 machineconstants_idc_dcm_signallevel_min

Reg. 0xA0020188

Threshold for lower value for median of main peaks for DCM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dcm_signallevel_min | rw | ro | 0x6666 | Threshold for lower value for median of main peaks for DCM |

### 1.3.100 machineconstants_idc_ddm_signallevel_min

Reg. 0xA002018C

Threshold for lower value for median of main peaks for DDM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ddm_signallevel_min | rw | ro | 0x4CCD | Threshold for lower value for median of main peaks for DDM |

### 1.3.101 machineconstants_idc_phi0marginholdoff

Reg. 0xA0020190

Holdoff before triggering the next offaxismain check

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant | rw | ro | 0x124F80 | Holdoff before triggering the next offaxismain check |

| | | | | | |
|---|---|---|---|---|---|
| | s_idc_phi0margi nholdoff | | | | |

### 1.3.102 machineconstants_idc_dcmqualitycountermax

Reg. 0xA0020194

Number of consecutive DCM Quality fails allowed in monitoring

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_dcmqualit ycountermax | rw | ro | 0xA | Number of consecutive DCM Quality fails allowed in moni- toring |

### 1.3.103 machineconstants_idc_ddmqualitycountermax

Reg. 0xA0020198

Number of consecutive DDM Quality fails allowed in monitoring

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_ddmqualit ycountermax | rw | ro | 0xA | Number of consecutive DDM Quality fails allowed in moni- toring |

### 1.3.104 machineconstants_idc_healthsignals_config

Reg. 0xA002019C

Enables/Disables HW communication and health checks

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_healthsig nals_config | rw | ro | 0xFF | Enables/Disables HW communication and health checks |

### 1.3.105 machineconstants_idc_oavsub_phi1marginres

Reg. 0xA00201A0

Off Axis Sub: idc_oavsub_phi1marginres

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_oavsub_ph i1marginres | rw | ro | 0xCD | Off Axis Sub: idc_oavsub_phi1marginres |

### 1.3.106 machineconstants_idc_oavsub_phi1marginnum

Reg. 0xA00201A4

Off Axis Sub: idc_oavsub_phi1marginnum

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_oavsub_ph i1marginnum | rw | ro | 0x5 | Off Axis Sub: idc_oavsub_phi1marginnum |

### 1.3.107 machineconstants_idc_oavsub_ddmlatency

Reg. 0xA00201A8

Off Axis Sub: idc_oavsub_ddmlatency

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant s_idc_oavsub_dd mlatency | rw | ro | 0x3 | Off Axis Sub: idc_oavsub_ddmlatency |

### 1.3.108 machineconstants_idc_oavmain_phi0marginres

Reg. 0xA00201AC

Off Axis Main: idc_oavmain_phi0marginres

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_oavmain_phi0marginres | rw | ro | 0xCD | Off Axis Main: idc_oavmain_phi0marginres |

### 1.3.109 machineconstants_idc_oavmain_phi0marginnum

Reg. 0xA00201B0

Off Axis Main: idc_oavmain_phi0marginnum

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_oavmain_phi0marginnum | rw | ro | 0x5 | Off Axis Main: idc_oavmain_phi0marginnum |

### 1.3.110 machineconstants_idc_oav_config

Reg. 0xA00201B4

Off axis velocity state configuration word. Enables or disable new off axis states

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_oav_config | rw | ro | 0x0 | Off axis velocity state configuration word. Enables or disable new off axis states |

### 1.3.111 machineconstants_idc_coveragesourcereprate_perc

Reg. 0xA00201B8

Percentage coverage of source rep rate band with nozzle operating band (at TF = idc_TF_coverage_operatingband_thr)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_coveragesourcereprate_perc | rw | ro | 0x199A | Percentage coverage of source rep rate band with nozzle operating band (at TF = idc_TF_coverage_operatingband_thr) |

### 1.3.112 machineconstants_idc_tf_coverage_operatingband_thr

Reg. 0xA00201BC

Threshold for coverage of source rep rate band with nozzle operating band

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_tf_coverage_operatingband_thr | rw | ro | 0x199A | Threshold for coverage of source rep rate band with nozzle operating band |

### 1.3.113 machineconstants_idc_workingsubclfreqs

Reg. 0xA00201C0

Number of working sub-coalescence frequencies after initial calibration (voltage > idc_workingsubclvoltage_thr)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_workingsubclfreqs | rw | ro | 0x1 | Number of working sub-coalescence frequencies after initial calibration (voltage > idc_workingsubclvoltage_thr) |

### 1.3.114 machineconstants_idc_workingsubclvoltage_thr

Reg. 0xA00201C4

Threshold for voltage of working sub-cl frequencies after initial calibration

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_workingsubclvoltage_thr | rw | ro | 0x1 | Threshold for voltage of working sub-cl frequencies after initial calibration |

### 1.3.115 machineconstants_idc_satratioaveragethreshold_on

Reg. 0xA00201C8

Inline Tuning parameter: satRatioAverageThreshold on droplet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_satratioaveragethreshold_on | rw | ro | 0x9999999A | Inline Tuning parameter: satRatioAverageThreshold on droplet |

### 1.3.116 machineconstants_idc_ddmdowntime

Reg. 0xA00201CC

Time in ms that DDM can be down before rising an error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ddmdowntime | rw | ro | 0x927C0 | Time in ms that DDM can be down before rising an error |

### 1.3.117 machineconstants_idc_dcm_bl_thr

Reg. 0xA00201D0

Treshold for DCM BL value before reporting an error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dcm_bl_thr | rw | ro | 0x10000 | Treshold for DCM BL value before reporting an error |

### 1.3.118 machineconstants_idc_ddm_bl_thr

Reg. 0xA00201D4

Treshold for DDM BL value before reporting an error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ddm_bl_thr | rw | ro | 0x10000 | Treshold for DDM BL value before reporting an error |

### 1.3.119 machineconstants_idc_dcm_missingdroplets_thr

Reg. 0xA00201D8

Treshold for DCM number of missed main droplets value before reporting an error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dcm_missingdroplets_thr | rw | ro | 0xA | Treshold for DCM number of missed main droplets value before reporting an error |

### 1.3.120 machineconstants_idc_ddm_missingdroplets_thr

Reg. 0xA00201DC

Treshold for DDM number of missed main droplets value before reporting an error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ddm_missingdroplets_thr | rw | ro | 0xA | Treshold for DDM number of missed main droplets value before reporting an error |

### 1.3.121 machineconstants_idc_exposureoff_holdoffcounter

Reg. 0xA00201E0

Amount of time the satrate will be ignored before starting the satrateaverage for off droplet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_exposureoff_holdoffcounter | rw | ro | 0x1 | Amount of time the satrate will be ignored before starting the satrateaverage for off droplet |

### 1.3.122 machineconstants_idc_exposureon_holdoffcounter

Reg. 0xA00201E4

Amount of time before risetime that satrate would be ignored to calculate satrate off droplet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_exposureon_holdoffcounter | rw | ro | 0x1 | Amount of time before risetime that satrate would be ignored to calculate satrate off droplet |

### 1.3.123 machineconstants_idc_dcm_pksaturation_thr

Reg. 0xA00201E8

PkSaturation Rate threshold used to measure dcm quality

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_dcm_pksaturation_thr | rw | ro | 0x10000 | PkSaturation Rate threshold used to measure dcm quality |

### 1.3.124 machineconstants_idc_ddm_pksaturation_thr

Reg. 0xA00201EC

PkSaturation Rate threshold used to measure ddm quality

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_ddm_pksaturation_thr | rw | ro | 0x10000 | PkSaturation Rate threshold used to measure ddm quality |

### 1.3.125 machineconstants_idc_spcfg_03

Reg. 0xA00201F0

idc_enable_ddm_violations

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_03 | rw | ro | 0x3 | idc_enable_ddm_violations |

### 1.3.126 machineconstants_idc_spcfg_04

Reg. 0xA00201F4

clst_enable_dcm_signallevel

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_04 | rw | ro | 0x1 | clst_enable_dcm_signallevel |

### 1.3.127 machineconstants_idc_spcfg_05

Reg. 0xA00201F8

idc_offaxissub_holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_05 | rw | ro | 0x8 | idc_offaxissub_holdoff |

### 1.3.128 machineconstants_idc_spcfg_06

Reg. 0xA00201FC

idc_recovery_holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_06 | rw | ro | 0xEA60 | idc_recovery_holdoff |

### 1.3.129 machineconstants_idc_spcfg_07

Reg. 0xA0020200

idc_offaxismain_holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_07 | rw | ro | 0x8 | idc_offaxismain_holdoff |

### 1.3.130 machineconstants_idc_spcfg_08

Reg. 0xA0020204

idc_timebetweenrecoveries_thr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_08 | rw | ro | 0x493E0 | idc_timebetweenrecoveries_thr |

### 1.3.131 machineconstants_idc_spcfg_09

Reg. 0xA0020208

idc_allowedrecoveries_thr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_09 | rw | ro | 0x3 | idc_allowedrecoveries_thr |

### 1.3.132 machineconstants_idc_spcfg_10

Reg. 0xA002020C

idc_monitoringdcrejection_time

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_10 | rw | ro | 0xEA60 | idc_monitoringdcrejection_time |

### 1.3.133 machineconstants_idc_spcfg_11

Reg. 0xA0020210

idc_exposurerecoverytransition_countermax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_11 | rw | ro | 0xA | idc_exposurerecoverytransition_countermax |

### 1.3.134 machineconstants_idc_spcfg_12

Reg. 0xA0020214

idc_timebetweenrecoveries_etecnok_thr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_12 | rw | ro | 0xA1220 | idc_timebetweenrecoveries_etecnok_thr |

### 1.3.135 machineconstants_idc_spcfg_13

Reg. 0xA0020218

idc_workingdcperc

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_13 | rw | ro | 0x0 | idc_workingdcperc |

### 1.3.136 machineconstants_idc_spcfg_14

Reg. 0xA002021C

idc_expmon_qualitycountermax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_14 | rw | ro | 0xA | idc_expmon_qualitycountermax |

### 1.3.137 machineconstants_idc_spcfg_15

Reg. 0xA0020220

idc_countfromlastsubclupmax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_15 | rw | ro | 0x927C0 | idc_countfromlastsubclupmax |

### 1.3.138 machineconstants_idc_spcfg_16

Reg. 0xA0020224

Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_16 | rw | ro | 0x0 | Spare Signal |

### 1.3.139 machineconstants_idc_spcfg_17

Reg. 0xA0020228

Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_17 | rw | ro | 0x0 | Spare Signal |

### 1.3.140 machineconstants_idc_spcfg_18

Reg. 0xA002022C

Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_18 | rw | ro | 0x0 | Spare Signal |

### 1.3.141 machineconstants_idc_spcfg_19

Reg. 0xA0020230

Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_19 | rw | ro | 0x0 | Spare Signal |

### 1.3.142 machineconstants_idc_spcfg_20

Reg. 0xA0020234

mvp_ignoreexpgate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_idc_spcfg_20 | rw | ro | 0x0 | mvp_ignoreexpgate |

### 1.3.143 machineconstants_cmd_manualtuningwaveformtype

Reg. 0xA0020238

Sets the waveform type during manual mode

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_manualtuningwaveformtype | rw | ro | 0x0 | Sets the waveform type during manual mode |

### 1.3.144 machineconstants_cmd_tssw_dutycycle

Reg. 0xA002023C

2sine-square Waveform duty cycle

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_dutycycle | rw | ro | 0xA | 2sine-square Waveform duty cycle |

### 1.3.145 machineconstants_cmd_tssw_risetime

Reg. 0xA0020240

2sine-square Waveform RiseTime

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_risetime | rw | ro | 0x0 | 2sine-square Waveform RiseTime |

### 1.3.146 machineconstants_cmd_tssw_sineamplitude0

Reg. 0xA0020244

2sine-square Waveform SineAmpliude0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_sineamplitude0 | rw | ro | 0x1400 | 2sine-square Waveform SineAmpliude0 |

### 1.3.147 machineconstants_cmd_tssw_sineamplitude1

Reg. 0xA0020248

2sine-square Waveform SineAmpliude1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_sineamplitude1 | rw | ro | 0x1400 | 2sine-square Waveform SineAmpliude1 |

### 1.3.148 machineconstants_cmd_tssw_sinefrequency

Reg. 0xA002024C

2sine-square Waveform SineFrequency

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_sinefrequency | rw | ro | 0x3A98000 | 2sine-square Waveform SineFrequency |

### 1.3.149 machineconstants_cmd_tssw_sinefrequencymultiplier

Reg. 0xA0020250

2sine-square Waveform SineFrequencyMultiplier

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_sinefrequencymultiplier | rw | ro | 0x2800 | 2sine-square Waveform SineFrequencyMultiplier |

### 1.3.150 machineconstants_cmd_tssw_sinephase0

Reg. 0xA0020254

2sine-square Waveform SinePhase0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_sinephase0 | rw | ro | 0x0 | 2sine-square Waveform SinePhase0 |

### 1.3.151 machineconstants_cmd_tssw_sinephase1

Reg. 0xA0020258

2sine-square Waveform SinePhase1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_sinephase1 | rw | ro | 0x0 | 2sine-square Waveform SinePhase1 |

### 1.3.152 machineconstants_cmd_tssw_squareamplitude

Reg. 0xA002025C

2sine-square Waveform SquareAmplitude

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_squareamplitude | rw | ro | 0x800 | 2sine-square Waveform SquareAmplitude |

### 1.3.153 machineconstants_cmd_tssw_squarefrequencymultiplier

Reg. 0xA0020260

2sine-square Waveform SquareFrequencyMultiplier

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_tssw_squarefrequencymultiplier | rw | ro | 0x1000 | 2sine-square Waveform SquareFrequencyMultiplier |

### 1.3.154 machineconstants_cmd_stup_dutycycle

Reg. 0xA0020264

Startup Waveform duty cycle

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_dutycycle | rw | ro | 0xA | Startup Waveform duty cycle |

### 1.3.155 machineconstants_cmd_stup_risetime

Reg. 0xA0020268

Startup Waveform RiseTime

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_risetime | rw | ro | 0x0 | Startup Waveform RiseTime |

### 1.3.156 machineconstants_cmd_stup_sineamplitude0

Reg. 0xA002026C

Startup Waveform SineAmpliude0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_sineamplitude0 | rw | ro | 0x400 | Startup Waveform SineAmpliude0 |

### 1.3.157 machineconstants_cmd_stup_sineamplitude1

Reg. 0xA0020270

Startup Waveform SineAmpliude1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_sineamplitude1 | rw | ro | 0x400 | Startup Waveform SineAmpliude1 |

### 1.3.158 machineconstants_cmd_stup_sinefrequency

Reg. 0xA0020274

Startup Waveform SineFrequency

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_sinefrequency | rw | ro | 0x3C8C000 | Startup Waveform SineFrequency |

### 1.3.159 machineconstants_cmd_stup_sinefrequencymultiplier

Reg. 0xA0020278

Startup Waveform SineFrequencyMultiplier

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_sinefrequencymultiplier | rw | ro | 0x2800 | Startup Waveform SineFrequencyMultiplier |

### 1.3.160 machineconstants_cmd_stup_sinephase0

Reg. 0xA002027C

Startup Waveform SinePhase0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_sinephase0 | rw | ro | 0x0 | Startup Waveform SinePhase0 |

### 1.3.161 machineconstants_cmd_stup_sinephase1

Reg. 0xA0020280

Startup Waveform SinePhase1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_sinephase1 | rw | ro | 0x0 | Startup Waveform SinePhase1 |

### 1.3.162 machineconstants_cmd_stup_squareamplitude

Reg. 0xA0020284

Startup Waveform SquareAmplitude

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_squareamplitude | rw | ro | 0x1000 | Startup Waveform SquareAmplitude |

### 1.3.163 machineconstants_cmd_stup_squarefrequencymultiplier

Reg. 0xA0020288

Startup Waveform SquareFrequencyMultiplier

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_stup_squarefrequencymultiplier | rw | ro | 0x1000 | Startup Waveform SquareFrequencyMultiplier |

### 1.3.164 machineconstants_cmd_hw_dutycycle

Reg. 0xA002028C

Hybrid waveform DutyCycle

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_hw_dutycycle | rw | ro | 0xA | Hybrid waveform DutyCycle |

### 1.3.165 machineconstants_cmd_hw_risetime

Reg. 0xA0020290

Hybrid waveform RiseTime

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_hw_risetime | rw | ro | 0x2AF31DC | Hybrid waveform RiseTime |

### 1.3.166 machineconstants_cmd_hw_sineamplitude

Reg. 0xA0020294

Hybrid waveform SineAmplitude

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_hw_sineamplitude | rw | ro | 0x1400 | Hybrid waveform SineAmplitude |

### 1.3.167 machineconstants_cmd_hw_sinefrequency

Reg. 0xA0020298

Hybrid waveform SineFrequency

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_hw_sinefrequency | rw | ro | 0x3A98000 | Hybrid waveform SineFrequency |

### 1.3.168 machineconstants_cmd_hw_squareamplitude

Reg. 0xA002029C

Hybrid waveform SquareAmplitude

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_hw_squareamplitude | rw | ro | 0x800 | Hybrid waveform SquareAmplitude |

### 1.3.169 machineconstants_cmd_hw_squarefrequencymultiplier

Reg. 0xA00202A0

Hybrid waveform SquareFrequencyMultiplier

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_hw_squarefrequencymultiplier | rw | ro | 0x1000 | Hybrid waveform SquareFrequencyMultiplier |

### 1.3.170 machineconstants_cmd_hw_squarephase

0xA00202A4

Hybrid waveform SquarePhase

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_hw_squarephase | rw | ro | 0x0 | Hybrid waveform SquarePhase |

### 1.3.171 machineconstants_cmd_sw_dutycycle

0xA00202A8

Square DutyCycle

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_sw_dutycycle | rw | ro | 0xA | Square DutyCycle |

### 1.3.172 machineconstants_cmd_sw_risetime

0xA00202AC

Square RiseTime

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_sw_risetime | rw | ro | 0x44B830 | Square RiseTime |

### 1.3.173 machineconstants_cmd_sw_squareamplitude

0xA00202B0

Square SquareAmplitude

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_sw_squareamplitude | rw | ro | 0x1400 | Square SquareAmplitude |

### 1.3.174 machineconstants_cmd_sw_squarefrequency

0xA00202B4

Square SquareFrequency

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_sw_squarefrequency | rw | ro | 0x3A98000 | Square SquareFrequency |

### 1.3.175 machineconstants_cmd_waveform_enable

0xA00202B8

Waveform enable external cmd

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cmd_waveform_enable | rw | ro | 0x1 | Waveform enable external cmd |

### 1.3.176 machineconstants_slt_solutiontype

0xA00202BC

Solution Table type: 0:2sineSquare, 1:HWO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_solutiontype | rw | ro | 0x0 | Solution Table type: 0:2sineSquare, 1:HWO |

### 1.3.177 machineconstants_slt_hyperparameters_1

Reg. 0xA00202C0

Solution Table f0, N0, N1, As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_hyperparameters_1 | rw | ro | 0x3A98000 | Solution Table f0, N0, N1, As |

### 1.3.178 machineconstants_slt_hyperparameters_2

Reg. 0xA00202C4

Solution Table f0, N0, N1, As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_hyperparameters_2 | rw | ro | 0x2800 | Solution Table f0, N0, N1, As |

### 1.3.179 machineconstants_slt_hyperparameters_3

Reg. 0xA00202C8

Solution Table f0, N0, N1, As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_hyperparameters_3 | rw | ro | 0x1000 | Solution Table f0, N0, N1, As |

### 1.3.180 machineconstants_slt_hyperparameters_4

Reg. 0xA00202CC

Solution Table f0, N0, N1, As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_hyperparameters_4 | rw | ro | 0x800 | Solution Table f0, N0, N1, As |

### 1.3.181 machineconstants_slt_sineamps_1

Reg. 0xA00202D0

Solution Table A0, A1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_sineamps_1 | rw | ro | 0x1400 | Solution Table A0, A1 |

### 1.3.182 machineconstants_slt_sineamps_2

Reg. 0xA00202D4

Solution Table A0, A1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_sineamps_2 | rw | ro | 0x1400 | Solution Table A0, A1 |

### 1.3.183 machineconstants_slt_phi0_1

Reg. 0xA00202D8

Solution table, phi0. DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_1 | rw | ro | 0x0 | Solution table, phi0. DC 5 |

### 1.3.184 machineconstants_slt_phi0_2

Reg. 0xA00202DC

Solution table, phi0. DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_2 | rw | ro | 0x0 | Solution table, phi0. DC 10 |

### 1.3.185 machineconstants_slt_phi0_3

Reg. 0xA00202E0

Solution table, phi0. DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_3 | rw | ro | 0x0 | Solution table, phi0. DC 15 |

### 1.3.186 machineconstants_slt_phi0_4

Reg. 0xA00202E4

Solution table, phi0. DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_4 | rw | ro | 0x0 | Solution table, phi0. DC 20 |

### 1.3.187 machineconstants_slt_phi0_5

Reg. 0xA00202E8

Solution table, phi0. DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_5 | rw | ro | 0x0 | Solution table, phi0. DC 25 |

### 1.3.188 machineconstants_slt_phi0_6

Reg. 0xA00202EC

Solution table, phi0. DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_6 | rw | ro | 0x0 | Solution table, phi0. DC 30 |

### 1.3.189 machineconstants_slt_phi0_7

Reg. 0xA00202F0

Solution table, phi0. DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_7 | rw | ro | 0x0 | Solution table, phi0. DC 35 |

### 1.3.190 machineconstants_slt_phi0_8

Reg. 0xA00202F4

Solution table, phi0. DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_8 | rw | ro | 0x0 | Solution table, phi0. DC 40 |

### 1.3.191 machineconstants_slt_phi0_9

Reg. 0xA00202F8

Solution table, phi0. DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_9 | rw | ro | 0x0 | Solution table, phi0. DC 45 |

### 1.3.192 machineconstants_slt_phi0_10

Reg. 0xA00202FC

Solution table, phi0. DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_10 | rw | ro | 0x0 | Solution table, phi0. DC 50 |

### 1.3.193 machineconstants_slt_phi0_11

Reg. 0xA0020300

Solution table, phi0. DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_11 | rw | ro | 0x0 | Solution table, phi0. DC 55 |

### 1.3.194 machineconstants_slt_phi0_12

Reg. 0xA0020304

Solution table, phi0. DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_12 | rw | ro | 0x0 | Solution table, phi0. DC 60 |

### 1.3.195 machineconstants_slt_phi0_13

Reg. 0xA0020308

Solution table, phi0. DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_13 | rw | ro | 0x0 | Solution table, phi0. DC 65 |

### 1.3.196 machineconstants_slt_phi0_14

Reg. 0xA002030C

Solution table, phi0. DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_14 | rw | ro | 0x0 | Solution table, phi0. DC 70 |

### 1.3.197 machineconstants_slt_phi0_15

Reg. 0xA0020310

Solution table, phi0. DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_15 | rw | ro | 0x0 | Solution table, phi0. DC 75 |

### 1.3.198 machineconstants_slt_phi0_16

Reg. 0xA0020314

Solution table, phi0. DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_16 | rw | ro | 0x0 | Solution table, phi0. DC 80 |

### 1.3.199 machineconstants_slt_phi0_17

Reg. 0xA0020318

Solution table, phi0. DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_17 | rw | ro | 0x0 | Solution table, phi0. DC 85 |

### 1.3.200 machineconstants_slt_phi0_18

Reg. 0xA002031C

Solution table, phi0. DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_18 | rw | ro | 0x0 | Solution table, phi0. DC 90 |

### 1.3.201 machineconstants_slt_phi0_19

Reg. 0xA0020320

Solution table, phi0. DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0_19 | rw | ro | 0x0 | Solution table, phi0. DC 95 |

### 1.3.202 machineconstants_slt_phi1_1

Reg. 0xA0020324

Solution Table, phi1 DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_1 | rw | ro | 0x0 | Solution Table, phi1 DC 5 |

### 1.3.203 machineconstants_slt_phi1_2

Reg. 0xA0020328

Solution Table, phi1 DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_2 | rw | ro | 0x0 | Solution Table, phi1 DC 10 |

### 1.3.204 machineconstants_slt_phi1_3

Reg. 0xA002032C

Solution Table, phi1 DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_3 | rw | ro | 0x0 | Solution Table, phi1 DC 15 |

### 1.3.205 machineconstants_slt_phi1_4

Reg. 0xA0020330

Solution Table, phi1 DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_4 | rw | ro | 0x0 | Solution Table, phi1 DC 20 |

### 1.3.206 machineconstants_slt_phi1_5

Reg. 0xA0020334

Solution Table, phi1 DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_5 | rw | ro | 0x0 | Solution Table, phi1 DC 25 |

### 1.3.207 machineconstants_slt_phi1_6

Reg. 0xA0020338

Solution Table, phi1 DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_6 | rw | ro | 0x0 | Solution Table, phi1 DC 30 |

### 1.3.208 machineconstants_slt_phi1_7

Reg. 0xA002033C

Solution Table, phi1 DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_7 | rw | ro | 0x0 | Solution Table, phi1 DC 35 |

### 1.3.209 machineconstants_slt_phi1_8

Reg. 0xA0020340

Solution Table, phi1 DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_8 | rw | ro | 0x0 | Solution Table, phi1 DC 40 |

### 1.3.210 machineconstants_slt_phi1_9

Reg. 0xA0020344

Solution Table, phi1 DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_9 | rw | ro | 0x0 | Solution Table, phi1 DC 45 |

### 1.3.211 machineconstants_slt_phi1_10

Reg. 0xA0020348

Solution Table, phi1 DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_10 | rw | ro | 0x0 | Solution Table, phi1 DC 50 |

### 1.3.212 machineconstants_slt_phi1_11

Reg. 0xA002034C

Solution Table, phi1 DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_11 | rw | ro | 0x0 | Solution Table, phi1 DC 55 |

### 1.3.213 machineconstants_slt_phi1_12

Reg. 0xA0020350

Solution Table, phi1 DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_12 | rw | ro | 0x0 | Solution Table, phi1 DC 60 |

### 1.3.214 machineconstants_slt_phi1_13

Reg. 0xA0020354

Solution Table, phi1 DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_13 | rw | ro | 0x0 | Solution Table, phi1 DC 65 |

### 1.3.215 machineconstants_slt_phi1_14

0xA0020358

Solution Table, phi1 DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_14 | rw | ro | 0x0 | Solution Table, phi1 DC 70 |

### 1.3.216 machineconstants_slt_phi1_15

0xA002035C

Solution Table, phi1 DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_15 | rw | ro | 0x0 | Solution Table, phi1 DC 75 |

### 1.3.217 machineconstants_slt_phi1_16

0xA0020360

Solution Table, phi1 DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_16 | rw | ro | 0x0 | Solution Table, phi1 DC 80 |

### 1.3.218 machineconstants_slt_phi1_17

0xA0020364

Solution Table, phi1 DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_17 | rw | ro | 0x0 | Solution Table, phi1 DC 85 |

### 1.3.219 machineconstants_slt_phi1_18

0xA0020368

Solution Table, phi1 DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_18 | rw | ro | 0x0 | Solution Table, phi1 DC 90 |

### 1.3.220 machineconstants_slt_phi1_19

0xA002036C

Solution Table, phi1 DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1_19 | rw | ro | 0x0 | Solution Table, phi1 DC 95 |

### 1.3.221 machineconstants_slt_presubcoal_flag_1

0xA0020370

Solution Table, pre-subcoal flag DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_1 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 5 |

### 1.3.222 machineconstants_slt_presubcoal_flag_2

0xA0020374

Solution Table, pre-subcoal flag DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_2 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 10 |

### 1.3.223 machineconstants_slt_presubcoal_flag_3

0xA0020378

Solution Table, pre-subcoal flag DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_3 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 15 |

### 1.3.224 machineconstants_slt_presubcoal_flag_4

0xA002037C

Solution Table, pre-subcoal flag DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_4 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 20 |

### 1.3.225 machineconstants_slt_presubcoal_flag_5

0xA0020380

Solution Table, pre-subcoal flag DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_5 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 25 |

### 1.3.226 machineconstants_slt_presubcoal_flag_6

0xA0020384

Solution Table, pre-subcoal flag DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_6 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 30 |

### 1.3.227 machineconstants_slt_presubcoal_flag_7

0xA0020388

Solution Table, pre-subcoal flag DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_7 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 35 |

### 1.3.228 machineconstants_slt_presubcoal_flag_8

0xA002038C

Solution Table, pre-subcoal flag DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_8 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 40 |

### 1.3.229 machineconstants_slt_presubcoal_flag_9

Reg. 0xA0020390

Solution Table, pre-subcoal flag DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_9 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 45 |

### 1.3.230 machineconstants_slt_presubcoal_flag_10

Reg. 0xA0020394

Solution Table, pre-subcoal flag DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_10 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 50 |

### 1.3.231 machineconstants_slt_presubcoal_flag_11

Reg. 0xA0020398

Solution Table, pre-subcoal flag DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_11 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 55 |

### 1.3.232 machineconstants_slt_presubcoal_flag_12

Reg. 0xA002039C

Solution Table, pre-subcoal flag DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_12 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 60 |

### 1.3.233 machineconstants_slt_presubcoal_flag_13

Reg. 0xA00203A0

Solution Table, pre-subcoal flag DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_13 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 65 |

### 1.3.234 machineconstants_slt_presubcoal_flag_14

Reg. 0xA00203A4

Solution Table, pre-subcoal flag DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_14 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 70 |

### 1.3.235 machineconstants_slt_presubcoal_flag_15

Reg. 0xA00203A8

Solution Table, pre-subcoal flag DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoa | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 75 |

| | | | | | |
|---|---|---|---|---|---|
| | l_flag_15 | | | | |

### 1.3.236 machineconstants_slt_presubcoal_flag_16

Reg. 0xA00203AC

Solution Table, pre-subcoal flag DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_16 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 80 |

### 1.3.237 machineconstants_slt_presubcoal_flag_17

Reg. 0xA00203B0

Solution Table, pre-subcoal flag DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_17 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 85 |

### 1.3.238 machineconstants_slt_presubcoal_flag_18

Reg. 0xA00203B4

Solution Table, pre-subcoal flag DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_18 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 90 |

### 1.3.239 machineconstants_slt_presubcoal_flag_19

Reg. 0xA00203B8

Solution Table, pre-subcoal flag DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubcoal_flag_19 | rw | ro | 0x1 | Solution Table, pre-subcoal flag DC 95 |

### 1.3.240 machineconstants_slt_jitter_1

Reg. 0xA00203BC

Solution Table, Jitter Metric DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_1 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 5 |

### 1.3.241 machineconstants_slt_jitter_2

Reg. 0xA00203C0

Solution Table, Jitter Metric DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_2 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 10 |

### 1.3.242 machineconstants_slt_jitter_3

Reg. 0xA00203C4

Solution Table, Jitter Metric DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_3 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 15 |

### 1.3.243 machineconstants_slt_jitter_4

Reg. 0xA00203C8

Solution Table, Jitter Metric DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_4 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 20 |

### 1.3.244 machineconstants_slt_jitter_5

Reg. 0xA00203CC

Solution Table, Jitter Metric DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_5 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 25 |

### 1.3.245 machineconstants_slt_jitter_6

Reg. 0xA00203D0

Solution Table, Jitter Metric DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_6 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 30 |

### 1.3.246 machineconstants_slt_jitter_7

Reg. 0xA00203D4

Solution Table, Jitter Metric DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_7 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 35 |

### 1.3.247 machineconstants_slt_jitter_8

Reg. 0xA00203D8

Solution Table, Jitter Metric DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_8 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 40 |

### 1.3.248 machineconstants_slt_jitter_9

Reg. 0xA00203DC

Solution Table, Jitter Metric DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_9 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 45 |

### 1.3.249 machineconstants_slt_jitter_10

Reg. 0xA00203E0

Solution Table, Jitter Metric DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_10 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 50 |

### 1.3.250 machineconstants_slt_jitter_11

Reg. 0xA00203E4

Solution Table, Jitter Metric DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_11 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 55 |

### 1.3.251 machineconstants_slt_jitter_12

Reg. 0xA00203E8

Solution Table, Jitter Metric DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_12 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 60 |

### 1.3.252 machineconstants_slt_jitter_13

Reg. 0xA00203EC

Solution Table, Jitter Metric DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_13 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 65 |

### 1.3.253 machineconstants_slt_jitter_14

Reg. 0xA00203F0

Solution Table, Jitter Metric DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_14 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 70 |

### 1.3.254 machineconstants_slt_jitter_15

Reg. 0xA00203F4

Solution Table, Jitter Metric DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_15 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 75 |

### 1.3.255 machineconstants_slt_jitter_16

Reg. 0xA00203F8

Solution Table, Jitter Metric DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_16 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 80 |

### 1.3.256 machineconstants_slt_jitter_17

Reg. 0xA00203FC

Solution Table, Jitter Metric DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_17 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 85 |

### 1.3.257 machineconstants_slt_jitter_18

Reg. 0xA0020400

Solution Table, Jitter Metric DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_18 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 90 |

### 1.3.258 machineconstants_slt_jitter_19

Reg. 0xA0020404

Solution Table, Jitter Metric DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_jitter_19 | rw | ro | 0x0 | Solution Table, Jitter Metric DC 95 |

### 1.3.259 machineconstants_slt_multpresubrate_1

Reg. 0xA0020408

Solution Table, multPresubRate DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_1 | rw | ro | 0x0 | Solution Table, multPresubRate DC 5 |

### 1.3.260 machineconstants_slt_multpresubrate_2

Reg. 0xA002040C

Solution Table, multPresubRate DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_2 | rw | ro | 0x0 | Solution Table, multPresubRate DC 10 |

### 1.3.261 machineconstants_slt_multpresubrate_3

Reg. 0xA0020410

Solution Table, multPresubRate DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_3 | rw | ro | 0x0 | Solution Table, multPresubRate DC 15 |

### 1.3.262 machineconstants_slt_multpresubrate_4

Reg. 0xA0020414

Solution Table, multPresubRate DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_4 | rw | ro | 0x0 | Solution Table, multPresubRate DC 20 |

### 1.3.263 machineconstants_slt_multpresubrate_5

Reg. 0xA0020418

Solution Table, multPresubRate DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_5 | rw | ro | 0x0 | Solution Table, multPresubRate DC 25 |

### 1.3.264 machineconstants_slt_multpresubrate_6

Reg. 0xA002041C

Solution Table, multPresubRate DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_6 | rw | ro | 0x0 | Solution Table, multPresubRate DC 30 |

### 1.3.265 machineconstants_slt_multpresubrate_7

Reg. 0xA0020420

Solution Table, multPresubRate DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_7 | rw | ro | 0x0 | Solution Table, multPresubRate DC 35 |

### 1.3.266 machineconstants_slt_multpresubrate_8

0xA0020424

Solution Table, multPresubRate DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_8 | rw | ro | 0x0 | Solution Table, multPresubRate DC 40 |

### 1.3.267 machineconstants_slt_multpresubrate_9

0xA0020428

Solution Table, multPresubRate DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_9 | rw | ro | 0x0 | Solution Table, multPresubRate DC 45 |

### 1.3.268 machineconstants_slt_multpresubrate_10

0xA002042C

Solution Table, multPresubRate DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_10 | rw | ro | 0x0 | Solution Table, multPresubRate DC 50 |

### 1.3.269 machineconstants_slt_multpresubrate_11

0xA0020430

Solution Table, multPresubRate DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_11 | rw | ro | 0x0 | Solution Table, multPresubRate DC 55 |

### 1.3.270 machineconstants_slt_multpresubrate_12

0xA0020434

Solution Table, multPresubRate DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_12 | rw | ro | 0x0 | Solution Table, multPresubRate DC 60 |

### 1.3.271 machineconstants_slt_multpresubrate_13

0xA0020438

Solution Table, multPresubRate DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_13 | rw | ro | 0x0 | Solution Table, multPresubRate DC 65 |

### 1.3.272 machineconstants_slt_multpresubrate_14

Reg. 0xA002043C

Solution Table, multPresubRate DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_14 | rw | ro | 0x0 | Solution Table, multPresubRate DC 70 |

### 1.3.273 machineconstants_slt_multpresubrate_15

Reg. 0xA0020440

Solution Table, multPresubRate DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_15 | rw | ro | 0x0 | Solution Table, multPresubRate DC 75 |

### 1.3.274 machineconstants_slt_multpresubrate_16

Reg. 0xA0020444

Solution Table, multPresubRate DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_16 | rw | ro | 0x0 | Solution Table, multPresubRate DC 80 |

### 1.3.275 machineconstants_slt_multpresubrate_17

Reg. 0xA0020448

Solution Table, multPresubRate DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_17 | rw | ro | 0x0 | Solution Table, multPresubRate DC 85 |

### 1.3.276 machineconstants_slt_multpresubrate_18

Reg. 0xA002044C

Solution Table, multPresubRate DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_18 | rw | ro | 0x0 | Solution Table, multPresubRate DC 90 |

### 1.3.277 machineconstants_slt_multpresubrate_19

Reg. 0xA0020450

Solution Table, multPresubRate DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_multpresubrate_19 | rw | ro | 0x0 | Solution Table, multPresubRate DC 95 |

### 1.3.278 machineconstants_slt_presubrate_1

Reg. 0xA0020454

Solution Table,PreSubRate DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_1 | rw | ro | 0x0 | Solution Table,PreSubRate DC 5 |

### 1.3.279 machineconstants_slt_presubrate_2

Reg. 0xA0020458

Solution Table,PreSubRate DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_2 | rw | ro | 0x0 | Solution Table,PreSubRate DC 10 |

### 1.3.280 machineconstants_slt_presubrate_3

Reg. 0xA002045C

Solution Table,PreSubRate DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_3 | rw | ro | 0x0 | Solution Table,PreSubRate DC 15 |

### 1.3.281 machineconstants_slt_presubrate_4

Reg. 0xA0020460

Solution Table,PreSubRate DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_4 | rw | ro | 0x0 | Solution Table,PreSubRate DC 20 |

### 1.3.282 machineconstants_slt_presubrate_5

Reg. 0xA0020464

Solution Table,PreSubRate DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_5 | rw | ro | 0x0 | Solution Table,PreSubRate DC 25 |

### 1.3.283 machineconstants_slt_presubrate_6

Reg. 0xA0020468

Solution Table,PreSubRate DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_6 | rw | ro | 0x0 | Solution Table,PreSubRate DC 30 |

### 1.3.284 machineconstants_slt_presubrate_7

Reg. 0xA002046C

Solution Table,PreSubRate DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_7 | rw | ro | 0x0 | Solution Table,PreSubRate DC 35 |

### 1.3.285 machineconstants_slt_presubrate_8

Reg. 0xA0020470

Solution Table,PreSubRate DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrat | rw | ro | 0x0 | Solution Table,PreSubRate DC 40 |

| | | | | | |
|---|---|---|---|---|---|
| | e_8 | | | | |

### 1.3.286 machineconstants_slt_presubrate_9

Reg. 0xA0020474

Solution Table,PreSubRate DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_9 | rw | ro | 0x0 | Solution Table,PreSubRate DC 45 |

### 1.3.287 machineconstants_slt_presubrate_10

Reg. 0xA0020478

Solution Table,PreSubRate DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_10 | rw | ro | 0x0 | Solution Table,PreSubRate DC 50 |

### 1.3.288 machineconstants_slt_presubrate_11

Reg. 0xA002047C

Solution Table,PreSubRate DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_11 | rw | ro | 0x0 | Solution Table,PreSubRate DC 55 |

### 1.3.289 machineconstants_slt_presubrate_12

Reg. 0xA0020480

Solution Table,PreSubRate DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_12 | rw | ro | 0x0 | Solution Table,PreSubRate DC 60 |

### 1.3.290 machineconstants_slt_presubrate_13

Reg. 0xA0020484

Solution Table,PreSubRate DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_13 | rw | ro | 0x0 | Solution Table,PreSubRate DC 65 |

### 1.3.291 machineconstants_slt_presubrate_14

Reg. 0xA0020488

Solution Table,PreSubRate DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_14 | rw | ro | 0x0 | Solution Table,PreSubRate DC 70 |

### 1.3.292 machineconstants_slt_presubrate_15

Reg. 0xA002048C

Solution Table,PreSubRate DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant | rw | ro | 0x0 | Solution Table,PreSubRate DC 75 |

| | | | | | |
|---|---|---|---|---|---|
| | s_slt_presubrat<br>e_15 | | | | |

### 1.3.293 machineconstants_slt_presubrate_16

Reg. 0xA0020490

Solution Table,PreSubRate DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant<br>s_slt_presubrat<br>e_16 | rw | ro | 0x0 | Solution Table,PreSubRate DC 80 |

### 1.3.294 machineconstants_slt_presubrate_17

Reg. 0xA0020494

Solution Table,PreSubRate DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant<br>s_slt_presubrat<br>e_17 | rw | ro | 0x0 | Solution Table,PreSubRate DC 85 |

### 1.3.295 machineconstants_slt_presubrate_18

Reg. 0xA0020498

Solution Table,PreSubRate DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant<br>s_slt_presubrat<br>e_18 | rw | ro | 0x0 | Solution Table,PreSubRate DC 90 |

### 1.3.296 machineconstants_slt_presubrate_19

Reg. 0xA002049C

Solution Table,PreSubRate DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant<br>s_slt_presubrat<br>e_19 | rw | ro | 0x0 | Solution Table,PreSubRate DC 95 |

### 1.3.297 machineconstants_slt_cm_1

Reg. 0xA00204A0

Solution Table, CM DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant<br>s_slt_cm_1 | rw | ro | 0x0 | Solution Table, CM DC 5 |

### 1.3.298 machineconstants_slt_cm_2

Reg. 0xA00204A4

Solution Table, CM DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant<br>s_slt_cm_2 | rw | ro | 0x0 | Solution Table, CM DC 10 |

### 1.3.299 machineconstants_slt_cm_3

Reg. 0xA00204A8

Solution Table, CM DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant<br>s_slt_cm_3 | rw | ro | 0x0 | Solution Table, CM DC 15 |

### 1.3.300 machineconstants_slt_cm_4

Reg. 0xA00204AC

Solution Table, CM DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_4 | rw | ro | 0x0 | Solution Table, CM DC 20 |

### 1.3.301 machineconstants_slt_cm_5

Reg. 0xA00204B0

Solution Table, CM DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_5 | rw | ro | 0x0 | Solution Table, CM DC 25 |

### 1.3.302 machineconstants_slt_cm_6

Reg. 0xA00204B4

Solution Table, CM DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_6 | rw | ro | 0x0 | Solution Table, CM DC 30 |

### 1.3.303 machineconstants_slt_cm_7

Reg. 0xA00204B8

Solution Table, CM DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_7 | rw | ro | 0x0 | Solution Table, CM DC 35 |

### 1.3.304 machineconstants_slt_cm_8

Reg. 0xA00204BC

Solution Table, CM DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_8 | rw | ro | 0x0 | Solution Table, CM DC 40 |

### 1.3.305 machineconstants_slt_cm_9

Reg. 0xA00204C0

Solution Table, CM DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_9 | rw | ro | 0x0 | Solution Table, CM DC 45 |

### 1.3.306 machineconstants_slt_cm_10

Reg. 0xA00204C4

Solution Table, CM DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_10 | rw | ro | 0x0 | Solution Table, CM DC 50 |

### 1.3.307 machineconstants_slt_cm_11

Reg. 0xA00204C8

Solution Table, CM DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_11 | rw | ro | 0x0 | Solution Table, CM DC 55 |

### 1.3.308 machineconstants_slt_cm_12

Reg. 0xA00204CC

Solution Table, CM DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_12 | rw | ro | 0x0 | Solution Table, CM DC 60 |

### 1.3.309 machineconstants_slt_cm_13

Reg. 0xA00204D0

Solution Table, CM DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_13 | rw | ro | 0x0 | Solution Table, CM DC 65 |

### 1.3.310 machineconstants_slt_cm_14

Reg. 0xA00204D4

Solution Table, CM DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_14 | rw | ro | 0x0 | Solution Table, CM DC 70 |

### 1.3.311 machineconstants_slt_cm_15

Reg. 0xA00204D8

Solution Table, CM DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_15 | rw | ro | 0x0 | Solution Table, CM DC 75 |

### 1.3.312 machineconstants_slt_cm_16

Reg. 0xA00204DC

Solution Table, CM DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_16 | rw | ro | 0x0 | Solution Table, CM DC 80 |

### 1.3.313 machineconstants_slt_cm_17

Reg. 0xA00204E0

Solution Table, CM DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_17 | rw | ro | 0x0 | Solution Table, CM DC 85 |

### 1.3.314 machineconstants_slt_cm_18

Reg. 0xA00204E4

Solution Table, CM DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_18 | rw | ro | 0x0 | Solution Table, CM DC 90 |

### 1.3.315 machineconstants_slt_cm_19

Reg. 0xA00204E8

Solution Table, CM DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_cm_19 | rw | ro | 0x0 | Solution Table, CM DC 95 |

### 1.3.316 machineconstants_slt_dm_1

Reg. 0xA00204EC

Solution Table, DM DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_1 | rw | ro | 0x0 | Solution Table, DM DC 5 |

### 1.3.317 machineconstants_slt_dm_2

Reg. 0xA00204F0

Solution Table, DM DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_2 | rw | ro | 0x0 | Solution Table, DM DC 10 |

### 1.3.318 machineconstants_slt_dm_3

Reg. 0xA00204F4

Solution Table, DM DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_3 | rw | ro | 0x0 | Solution Table, DM DC 15 |

### 1.3.319 machineconstants_slt_dm_4

Reg. 0xA00204F8

Solution Table, DM DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_4 | rw | ro | 0x0 | Solution Table, DM DC 20 |

### 1.3.320 machineconstants_slt_dm_5

Reg. 0xA00204FC

Solution Table, DM DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_5 | rw | ro | 0x0 | Solution Table, DM DC 25 |

### 1.3.321 machineconstants_slt_dm_6

Reg. 0xA0020500

Solution Table, DM DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_6 | rw | ro | 0x0 | Solution Table, DM DC 30 |

### 1.3.322 machineconstants_slt_dm_7

Reg. 0xA0020504

Solution Table, DM DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_7 | rw | ro | 0x0 | Solution Table, DM DC 35 |

### 1.3.323 machineconstants_slt_dm_8

Reg. 0xA0020508

Solution Table, DM DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_8 | rw | ro | 0x0 | Solution Table, DM DC 40 |

### 1.3.324 machineconstants_slt_dm_9

Reg. 0xA002050C

Solution Table, DM DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_9 | rw | ro | 0x0 | Solution Table, DM DC 45 |

### 1.3.325 machineconstants_slt_dm_10

Reg. 0xA0020510

Solution Table, DM DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_10 | rw | ro | 0x0 | Solution Table, DM DC 50 |

### 1.3.326 machineconstants_slt_dm_11

Reg. 0xA0020514

Solution Table, DM DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_11 | rw | ro | 0x0 | Solution Table, DM DC 55 |

### 1.3.327 machineconstants_slt_dm_12

Reg. 0xA0020518

Solution Table, DM DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_12 | rw | ro | 0x0 | Solution Table, DM DC 60 |

### 1.3.328 machineconstants_slt_dm_13

Reg. 0xA002051C

Solution Table, DM DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_13 | rw | ro | 0x0 | Solution Table, DM DC 65 |

### 1.3.329 machineconstants_slt_dm_14

Reg. 0xA0020520

Solution Table, DM DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_14 | rw | ro | 0x0 | Solution Table, DM DC 70 |

### 1.3.330 machineconstants_slt_dm_15

Reg. 0xA0020524

Solution Table, DM DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_15 | rw | ro | 0x0 | Solution Table, DM DC 75 |

### 1.3.331 machineconstants_slt_dm_16

Reg. 0xA0020528

Solution Table, DM DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_16 | rw | ro | 0x0 | Solution Table, DM DC 80 |

### 1.3.332 machineconstants_slt_dm_17

Reg. 0xA002052C

Solution Table, DM DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_17 | rw | ro | 0x0 | Solution Table, DM DC 85 |

### 1.3.333 machineconstants_slt_dm_18

Reg. 0xA0020530

Solution Table, DM DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_18 | rw | ro | 0x0 | Solution Table, DM DC 90 |

### 1.3.334 machineconstants_slt_dm_19

Reg. 0xA0020534

Solution Table, DM DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dm_19 | rw | ro | 0x0 | Solution Table, DM DC 95 |

### 1.3.335 machineconstants_slt_dcdphi

Reg. 0xA0020538

Solution Table, DM DCDPhi

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_dcdphi | rw | ro | 0x0 | Solution Table, DM DCDPhi |

### 1.3.336 machineconstants_slt_phi1margin_1

Reg. 0xA002053C

Solution table, phi1Margin DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_1 | rw | ro | 0x0 | Solution table, phi1Margin DC 5 |

### 1.3.337 machineconstants_slt_phi1margin_2

Reg. 0xA0020540

Solution table, phi1Margin DC 10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_2 | rw | ro | 0x0 | Solution table, phi1Margin DC 10 |

### 1.3.338 machineconstants_slt_phi1margin_3

Reg. 0xA0020544

Solution table, phi1Margin DC 15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_3 | rw | ro | 0x0 | Solution table, phi1Margin DC 15 |

### 1.3.339 machineconstants_slt_phi1margin_4

Reg. 0xA0020548

Solution table, phi1Margin DC 20

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_4 | rw | ro | 0x0 | Solution table, phi1Margin DC 20 |

### 1.3.340 machineconstants_slt_phi1margin_5

Reg. 0xA002054C

Solution table, phi1Margin DC 25

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_5 | rw | ro | 0x0 | Solution table, phi1Margin DC 25 |

### 1.3.341 machineconstants_slt_phi1margin_6

Reg. 0xA0020550

Solution table, phi1Margin DC 30

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_6 | rw | ro | 0x0 | Solution table, phi1Margin DC 30 |

### 1.3.342 machineconstants_slt_phi1margin_7

Reg. 0xA0020554

Solution table, phi1Margin DC 35

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_7 | rw | ro | 0x0 | Solution table, phi1Margin DC 35 |

### 1.3.343 machineconstants_slt_phi1margin_8

Reg. 0xA0020558

Solution table, phi1Margin DC 40

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_8 | rw | ro | 0x0 | Solution table, phi1Margin DC 40 |

### 1.3.344 machineconstants_slt_phi1margin_9

Reg. 0xA002055C

Solution table, phi1Margin DC 45

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_9 | rw | ro | 0x0 | Solution table, phi1Margin DC 45 |

### 1.3.345 machineconstants_slt_phi1margin_10

Reg. 0xA0020560

Solution table, phi1Margin DC 50

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_10 | rw | ro | 0x0 | Solution table, phi1Margin DC 50 |

### 1.3.346 machineconstants_slt_phi1margin_11

Reg. 0xA0020564

Solution table, phi1Margin DC 55

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_11 | rw | ro | 0x0 | Solution table, phi1Margin DC 55 |

### 1.3.347 machineconstants_slt_phi1margin_12

Reg. 0xA0020568

Solution table, phi1Margin DC 60

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_12 | rw | ro | 0x0 | Solution table, phi1Margin DC 60 |

### 1.3.348 machineconstants_slt_phi1margin_13

Reg. 0xA002056C

Solution table, phi1Margin DC 65

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_13 | rw | ro | 0x0 | Solution table, phi1Margin DC 65 |

### 1.3.349 machineconstants_slt_phi1margin_14

Reg. 0xA0020570

Solution table, phi1Margin DC 70

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_14 | rw | ro | 0x0 | Solution table, phi1Margin DC 70 |

### 1.3.350 machineconstants_slt_phi1margin_15

Reg. 0xA0020574

Solution table, phi1Margin DC 75

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_15 | rw | ro | 0x0 | Solution table, phi1Margin DC 75 |

### 1.3.351 machineconstants_slt_phi1margin_16

Reg. 0xA0020578

Solution table, phi1Margin DC 80

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin | rw | ro | 0x0 | Solution table, phi1Margin DC 80 |

| | | | | | |
|---|---|---|---|---|---|
| | n_16 | | | | |

### 1.3.352 machineconstants_slt_phi1margin_17

Reg. 0xA002057C

Solution table, phi1Margin DC 85

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_17 | rw | ro | 0x0 | Solution table, phi1Margin DC 85 |

### 1.3.353 machineconstants_slt_phi1margin_18

Reg. 0xA0020580

Solution table, phi1Margin DC 90

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_18 | rw | ro | 0x0 | Solution table, phi1Margin DC 90 |

### 1.3.354 machineconstants_slt_phi1margin_19

Reg. 0xA0020584

Solution table, phi1Margin DC 95

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi1margin_19 | rw | ro | 0x0 | Solution table, phi1Margin DC 95 |

### 1.3.355 machineconstants_slt_phi0margin

Reg. 0xA0020588

Solution Table, phi0Margin DC 5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_phi0margin | rw | ro | 0x0 | Solution Table, phi0Margin DC 5 |

### 1.3.356 machineconstants_slt_satrateavg_off

Reg. 0xA002058C

Satrate average, DDM, off droplet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_satrateavg_off | rw | ro | 0x0 | Satrate average, DDM, off droplet |

### 1.3.357 machineconstants_slt_satrateavg_on

Reg. 0xA0020590

Satrate average, DDM, on droplet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_satrateavg_on | rw | ro | 0x0 | Satrate average, DDM, on droplet |

### 1.3.358 machineconstants_slt_xint3sigma_avg

Reg. 0xA0020594

Solution table xint3sigma_avg

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstant | rw | ro | 0x0 | Solution table xint3sigma_avg |

| | | | | | |
|---|---|---|---|---|---|
| | s_slt_xint3sigma_avg | | | | |

### 1.3.359 machineconstants_slt_presubrate_avg

Reg. 0xA0020598

presubrateavg, monitor state, for OPT DC

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_presubrate_avg | rw | ro | 0x0 | presubrateavg, monitor state, for OPT DC |

### 1.3.360 machineconstants_slt_opt_sol

Reg. 0xA002059C

Index of the Optimal solution in the solution table

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_opt_sol | rw | ro | 0x2 | Index of the Optimal solution in the solution table |

### 1.3.361 machineconstants_slt_bk_sol

Reg. 0xA00205A0

Index of the next Backup solution in the solution table

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_slt_bk_sol | rw | ro | 0x2 | Index of the next Backup solution in the solution table |

### 1.3.362 machineconstants_damp_damp2piezo_gain

Reg. 0xA00205A4

DAMP Gain adjustment

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_damp_damp2piezo_gain | rw | ro | 0xA3D | DAMP Gain adjustment |

### 1.3.363 machineconstants_damp_waveform_debug_setup_aoch1

Reg. 0xA00205A8

planned for MVP only. They setup debug mode for the analog outputs for the DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_damp_waveform_debug_setup_aoch1 | rw | ro | 0x0 | planned for MVP only. They setup debug mode for the analog outputs for the DAMP |

### 1.3.364 machineconstants_damp_waveform_debug_setup_aoch2

Reg. 0xA00205AC

planned for MVP only. They setup debug mode for the analog outputs for the DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_damp_waveform_debug_setup_aoch2 | rw | ro | 0x0 | planned for MVP only. They setup debug mode for the analog outputs for the DAMP |

### 1.3.365 machineconstants_damp_waveform_debug_setup_aoch3

Reg. 0xA00205B0

planned for MVP only. They setup debug mode for the analog outputs for the DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_damp_waveform_debug_setup_aoch3 | rw | ro | 0x0 | planned for MVP only. They setup debug mode for the analog outputs for the DAMP |

### 1.3.366 machineconstants_damp_waveform_debug_setup_aoch4

Reg. 0xA00205B4

planned for MVP only. They setup debug mode for the analog outputs for the DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_damp_waveform_debug_setup_aoch4 | rw | ro | 0x0 | planned for MVP only. They setup debug mode for the analog outputs for the DAMP |

### 1.3.367 machineconstants_damp_deltan

Reg. 0xA00205B8

DAMP deltaN is samples

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_damp_deltan | rw | ro | 0x0 | DAMP deltaN is samples |

### 1.3.368 machineconstants_damp_ditherbits

Reg. 0xA00205BC

DAMP ditherbits is samples

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_damp_ditherbits | rw | ro | 0x0 | DAMP ditherbits is samples |

### 1.3.369 machineconstants_cal_bdo_basefreqmin

Reg. 0xA00205C0

Base Frequency Min for Base Droplet Optimization

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_bdo_basefreqmin | rw | ro | 0x2A4C2000 | Base Frequency Min for Base Droplet Optimization |

### 1.3.370 machineconstants_cal_bdo_basefreqnumber

Reg. 0xA00205C4

Base Frequency Number for Base Droplet Optimization

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_bdo_basefreqnumber | rw | ro | 0x3 | Base Frequency Number for Base Droplet Optimization |

### 1.3.371 machineconstants_cal_bdo_basefreqres

Reg. 0xA00205C8

Base Frequency Resolution for Base Droplet Optimization

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_bdo_basefreqres | rw | ro | 0x3D86000 | Base Frequency Resolution for Base Droplet Optimization |

### 1.3.372 machineconstants_cal_sqrampltf

Reg. 0xA00205CC

Square Amplitude for TFM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_sqrampltf | rw | ro | 0x1000 | Square Amplitude for TFM |

### 1.3.373 machineconstants_cal_mainfreqvec_min

Reg. 0xA00205D0

Calibration parameter: cal_mainfreqvec_min

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_mainfreqvec_min | rw | ro | 0x3C8C000 | Calibration parameter: cal_mainfreqvec_min |

### 1.3.374 machineconstants_cal_mainfreqvec_number

Reg. 0xA00205D4

Calibration parameter: cal_mainfreqvec_number

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_mainfreqvec_number | rw | ro | 0x15 | Calibration parameter: cal_mainfreqvec_number |

### 1.3.375 machineconstants_cal_mainfreqvec_res

Reg. 0xA00205D8

Calibration parameter: cal_mainfreqvec_res

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_mainfreqvec_res | rw | ro | 0x19000 | Calibration parameter: cal_mainfreqvec_res |

### 1.3.376 machineconstants_cal_subfreqmultvec_min

Reg. 0xA00205DC

Calibration parameter: cal_subfreqmultvec_min

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_subfreqmultvec_min | rw | ro | 0x1C00 | Calibration parameter: cal_subfreqmultvec_min |

### 1.3.377 machineconstants_cal_subfreqmultvec_number

Reg. 0xA00205E0

Calibration parameter: cal_subfreqmultvec_number

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_subfreqmultvec_number | rw | ro | 0x4 | Calibration parameter: cal_subfreqmultvec_number |

### 1.3.378 machineconstants_cal_subfreqmultvec_res

Reg. 0xA00205E4

Calibration parameter: cal_subfreqmultvec_res

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_subfreqmultvec_res | rw | ro | 0x400 | Calibration parameter: cal_subfreqmultvec_res |

### 1.3.379 machineconstants_cal_sineampltfmin

Reg. 0xA00205E8

Calibration parameter: cal_sineampltfmin

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_sineampltfmin | rw | ro | 0x66 | Calibration parameter: cal_sineampltfmin |

### 1.3.380 machineconstants_cal_sineampltfres

Reg. 0xA00205EC

Calibration parameter: cal_sineampltfres

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_sineampltfres | rw | ro | 0x66 | Calibration parameter: cal_sineampltfres |

### 1.3.381 machineconstants_cal_sineampltfnumber

Reg. 0xA00205F0

Calibration parameter: cal_sineampltfnumber

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_sineampltfnumber | rw | ro | 0x14 | Calibration parameter: cal_sineampltfnumber |

### 1.3.382 machineconstants_cal_mainfreqdiag_min

Reg. 0xA00205F4

Calibration parameter: cal_mainfreqdiag_min

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_mainfreqdiag_min | rw | ro | 0x30D4000 | Calibration parameter: cal_mainfreqdiag_min |

### 1.3.383 machineconstants_cal_mainfreqdiag_res

Reg. 0xA00205F8

Calibration parameter: cal_mainfreqdiag_res

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_mainfreqdiag_res | rw | ro | 0x19000 | Calibration parameter: cal_mainfreqdiag_res |

### 1.3.384 machineconstants_cal_mainfreqdiag_number

Reg. 0xA00205FC

Calibration parameter: cal_mainfreqdiag_number

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_mainfreqdiag_number | rw | ro | 0xC9 | Calibration parameter: cal_mainfreqdiag_number |

### 1.3.385 machineconstants_cal_bdo_holdoff

Reg. 0xA0020600

Calibration parameter: cal_bdo_holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_bdo_holdo | rw | ro | 0xA | Calibration parameter: cal_bdo_holdoff |

| | | | | | |
|---|---|---|---|---|---|
| | ff | | | | |

### 1.3.386 machineconstants_cal_tfm_holdoff

Reg. 0xA0020604

Calibration parameter: cal_tfm_holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_tfm_holdoff | rw | ro | 0xA | Calibration parameter: cal_tfm_holdoff |

### 1.3.387 machineconstants_cal_ddmmainpeakvalthr

Reg. 0xA0020608

Calibration parameter: cal_ddmmainpeakvalthr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_ddmmainpeakvalthr | rw | ro | 0x2000 | Calibration parameter: cal_ddmmainpeakvalthr |

### 1.3.388 machineconstants_cal_ddmsnrthr

Reg. 0xA002060C

Calibration parameter: cal_ddmsnrthr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_ddmsnrthr | rw | ro | 0x500 | Calibration parameter: cal_ddmsnrthr |

### 1.3.389 machineconstants_cal_ddmwidththr

Reg. 0xA0020610

Calibration parameter: cal_ddmwidththr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_ddmwidththr | rw | ro | 0x4CD | Calibration parameter: cal_ddmwidththr |

### 1.3.390 machineconstants_cal_ddmqc_holdoff

Reg. 0xA0020614

Calibration parameter: cal_ddmqc_holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_ddmqc_holdoff | rw | ro | 0x5 | Calibration parameter: cal_ddmqc_holdoff |

### 1.3.391 machineconstants_cal_dcmqc_holdoff

Reg. 0xA0020618

Calibration parameter: cal_dcmqc_holdoff

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_dcmqc_holdoff | rw | ro | 0x5 | Calibration parameter: cal_dcmqc_holdoff |

### 1.3.392 machineconstants_cal_dcmmainpeakvalthr

Reg. 0xA002061C

Calibration parameter: cal_dcmmainpeakvalthr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_dcmmainpe | rw | ro | 0x2000 | Calibration parameter: cal_dcmmainpeakvalthr |

| | | | | | |
|---|---|---|---|---|---|
| | akvalthr | | | | |

### 1.3.393 machineconstants_cal_dcmsnrthr

Reg. 0xA0020620

Calibration parameter: cal_dcmsnrthr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_dcmsnrthr | rw | ro | 0x500 | Calibration parameter: cal_dcmsnrthr |

### 1.3.394 machineconstants_cal_dcmwidththr

Reg. 0xA0020624

Calibration parameter: cal_dcmwidththr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_dcmwidththr | rw | ro | 0x4CD | Calibration parameter: cal_dcmwidththr |

### 1.3.395 machineconstants_cal_dcmcheckiter

Reg. 0xA0020628

Calibration parameter: cal_dcmcheckiter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_dcmcheckiter | rw | ro | 0x4 | Calibration parameter: cal_dcmcheckiter |

### 1.3.396 machineconstants_cal_ddmcheckiter

Reg. 0xA002062C

Calibration parameter: cal_ddmcheckiter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_ddmcheckiter | rw | ro | 0x4 | Calibration parameter: cal_ddmcheckiter |

### 1.3.397 machineconstants_cal_targetcl

Reg. 0xA0020630

To support KPI phase 3. Target Coalescence

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_targetcl | rw | ro | 0x12C | To support KPI phase 3. Target Coalescence |

### 1.3.398 machineconstants_cal_targetsubcl_initial

Reg. 0xA0020634

Calibration parameter: cal_targetsubcl_initial

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_targetsubcl_initial | rw | ro | 0x1E | Calibration parameter: cal_targetsubcl_initial |

### 1.3.399 machineconstants_cal_targetsubcl_res

Reg. 0xA0020638

Calibration parameter: cal_targetsubcl_res

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_targetsubcl_res | rw | ro | 0x14 | Calibration parameter: cal_targetsubcl_res |

### 1.3.400 machineconstants_cal_targetsubcl_num

Reg. 0xA002063C

Calibration parameter: cal_targetsubcl_num

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_targetsubcl_num | rw | ro | 0x2 | Calibration parameter: cal_targetsubcl_num |

### 1.3.401 machineconstants_cal_targetscl_optimized

Reg. 0xA0020640

To support KPI phase 3. Target Sub-Coalescence Optimized

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_targetscl_optimized | rw | ro | 0x22 | To support KPI phase 3. Target Sub-Coalescence Optimized |

### 1.3.402 machineconstants_cal_tferrthr

Reg. 0xA0020644

Calibration parameter: cal_tferrthr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_tferrthr | rw | ro | 0x8000 | Calibration parameter: cal_tferrthr |

### 1.3.403 machineconstants_cal_totalvoltage

Reg. 0xA0020648

Calibration parameter: cal_totalvoltage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_totalvoltage | rw | ro | 0x10400 | Calibration parameter: cal_totalvoltage |

### 1.3.404 machineconstants_cal_cost_weight_p0

Reg. 0xA002064C

Calibration parameter: cal_cost_weight_p0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_cost_weight_p0 | rw | ro | 0x10000 | Calibration parameter: cal_cost_weight_p0 |

### 1.3.405 machineconstants_cal_cost_weight_p1

Reg. 0xA0020650

Calibration parameter: cal_cost_weight_p1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_cost_weight_p1 | rw | ro | 0x10000 | Calibration parameter: cal_cost_weight_p1 |

### 1.3.406 machineconstants_cal_cost_weight_p2

Reg. 0xA0020654

Calibration parameter: cal_cost_weight_p2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_cost_weight_p2 | rw | ro | 0x10000 | Calibration parameter: cal_cost_weight_p2 |

### 1.3.407 machineconstants_cal_cost_weight_p3

Reg. 0xA0020658

Calibration parameter: cal_cost_weight_p3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_cost_weight_p3 | rw | ro | 0x10000 | Calibration parameter: cal_cost_weight_p3 |

### 1.3.408 machineconstants_cal_cost_weight_p4

Reg. 0xA002065C

Calibration parameter: cal_cost_weight_p4

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_cost_weight_p4 | rw | ro | 0x10000 | Calibration parameter: cal_cost_weight_p4 |

### 1.3.409 machineconstants_cal_cost_weight_p5

Reg. 0xA0020660

Calibration parameter: cal_cost_weight_p5

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_cost_weight_p5 | rw | ro | 0x10000 | Calibration parameter: cal_cost_weight_p5 |

### 1.3.410 machineconstants_cal_costfunctiondswthr

Reg. 0xA0020664

Calibration parameter: cal_costfunctiondswthr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_costfunctiondswthr | rw | ro | 0xCCCD | Calibration parameter: cal_costfunctiondswthr |

### 1.3.411 machineconstants_cal_costfunctionhwthr

Reg. 0xA0020668

Calibration parameter: cal_costfunctionhwthr

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_costfunctionhwthr | rw | ro | 0xCCCD | Calibration parameter: cal_costfunctionhwthr |

### 1.3.412 machineconstants_cal_freqdiagnosticnumber

Reg. 0xA002066C

Calibration parameter: cal_freqdiagnosticnumber

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_freqdiagnosticnumber | rw | ro | 0x3 | Calibration parameter: cal_freqdiagnosticnumber |

### 1.3.413 machineconstants_cal_freqdiagnosticres

Reg. 0xA0020670

Calibration parameter: cal_freqdiagnosticres

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_freqdiagn | rw | ro | 0x2710 | Calibration parameter: cal_freqdiagnosticres |

| | | | | | |
|---|---|---|---|---|---|
| | osticres | | | | |

### 1.3.414 machineconstants_cal_maindropletdiameter

Reg. 0xA0020674

Diameter for main droplets in um

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_maindropletdiameter | rw | ro | 0x1B4CCD | Diameter for main droplets in um |

### 1.3.415 machineconstants_cal_maindropletvelocity

Reg. 0xA0020678

Main droplet velocity

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_maindropletvelocity | rw | ro | 0x820000 | Main droplet velocity |

### 1.3.416 machineconstants_cal_satellitediametermindcm

Reg. 0xA002067C

Calibration parameter: cal_satellitediametermindcm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_satellitediametermindcm | rw | ro | 0x40000 | Calibration parameter: cal_satellitediametermindcm |

### 1.3.417 machineconstants_cal_satellitediametermindddm

Reg. 0xA0020680

Calibration parameter: cal_satellitediameterminddm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_satellitediameterminddm | rw | ro | 0x60000 | Calibration parameter: cal_satellitediameterminddm |

### 1.3.418 machineconstants_cal_dcmlocation

Reg. 0xA0020684

DCM location

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_dcmlocation | rw | ro | 0x46 | DCM location |

### 1.3.419 machineconstants_cal_errorratiothreshold

Reg. 0xA0020688

TF Error ratio threshold

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_errorratiothreshold | rw | ro | 0x8000 | TF Error ratio threshold |

### 1.3.420 machineconstants_cal_bdo_dc_res

Reg. 0xA002068C

Duty Cycle resolution while performing BDO scan

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_bdo_dc_res | rw | ro | 0xA | Duty Cycle resolution while performing BDO scan |

### 1.3.421 machineconstants_cal_dragcte

Reg. 0xA0020690

Drag coefficient

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_dragcte | rw | ro | 0x1 | Drag coefficient |

### 1.3.422 machineconstants_cal_num_candidate_soln

Reg. 0xA0020694

Number of candidate solutions

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_num_candidate_soln | rw | ro | 0x15 | Number of candidate solutions |

### 1.3.423 machineconstants_cal_spcfg_4

Reg. 0xA0020698

cal_dcm_qualcheck

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_4 | rw | ro | 0x7 | cal_dcm_qualcheck |

### 1.3.424 machineconstants_cal_spcfg_5

Reg. 0xA002069C

cal_targetsubcl_num_MX

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_5 | rw | ro | 0x1 | cal_targetsubcl_num_MX |

### 1.3.425 machineconstants_cal_spcfg_6

Reg. 0xA00206A0

cal_targetsubcl_res_MX

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_6 | rw | ro | 0x14 | cal_targetsubcl_res_MX |

### 1.3.426 machineconstants_cal_mainfreqopt_type

Reg. 0xA00206A4

Main frequency optimization type: 0-Main freqiency optimization, do extended calibration on failure; 1-Only main freq opt; 2-Only extended calibration

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_mainfreqopt_type | rw | ro | 0x0 | Main frequency optimization type: 0-Main freqiency optimization, do extended calibration on failure; 1-Only main freq opt; 2-Only extended calibration |

### 1.3.427 machineconstants_cal_spcfg_8

Reg. 0xA00206A8

cal_mainfreqopt_type_MX

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_8 | rw | ro | 0x1 | cal_mainfreqopt_type_MX |

### 1.3.428 machineconstants_cal_pkuniformitymax

Reg. 0xA00206AC

Maximum peakuniformity

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_pkuniformitymax | rw | ro | 0x199A | Maximum peakuniformity |

### 1.3.429 machineconstants_cal_spcfg_10

Reg. 0xA00206B0

cal_num_candidate_soln_MX

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_10 | rw | ro | 0x1 | cal_num_candidate_soln_MX |

### 1.3.430 machineconstants_cal_spcfg_11

Reg. 0xA00206B4

cal_targetsubcl_initial_MX

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_11 | rw | ro | 0x1E | cal_targetsubcl_initial_MX |

### 1.3.431 machineconstants_cal_spcfg_12

Reg. 0xA00206B8

Calibration parameter: cal_spcfg_12

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_12 | rw | ro | 0x0 | Calibration parameter: cal_spcfg_12 |

### 1.3.432 machineconstants_cal_jmpbnddelay

Reg. 0xA00206BC

Jump boundary delay

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_jmpbnddelay | rw | ro | 0x1 | Jump boundary delay |

### 1.3.433 machineconstants_cal_spcfg_14

Reg. 0xA00206C0

cal_monitoringqualcheckcountermax

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_14 | rw | ro | 0x3 | cal_monitoringqualcheckcountermax |

### 1.3.434 machineconstants_cal_spcfg_15

Reg. 0xA00206C4

Calibration parameter: cal_spcfg_15

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_15 | rw | ro | 0x0 | Calibration parameter: cal_spcfg_15 |

### 1.3.435 machineconstants_cal_spcfg_16

Reg. 0xA00206C8

Calibration parameter: cal_spcfg_16

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | machineconstants_cal_spcfg_16 | rw | ro | 0x0 | Calibration parameter: cal_spcfg_16 |

## 1.4 algo_egr_registers_srdl

Block 0xA0030000 - 0xA003D07F

Register map of the egress algo registers

### 1.4.1 algo_egress_module_name

Reg. 0xA0030000

Defines the module name

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | module_name | ro | na | 0x6F616C67 | ASCII code for module name - top module(core) = core |

### 1.4.2 algo_egress_module_version

Reg. 0xA0030004

Module version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:16 | rfu | ro | na | 0x0 | Reserved for Future Use - RFU |
| 15:8 | major_revision | ro | na | 0x0 | Major Revision |
| 7:0 | minor_revision | ro | na | 0x0 | Minor Revision |

### 1.4.3 algo_egress_page_properties

Reg. 0xA0030008

Address page properties

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | present | ro | wo | 0x1 | Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not. |
| 30:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | page_size | ro | na | 0x10 | Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enter here. |
| 7:0 | unified_header_rev | ro | na | 0x1 | Unified Header Format common registers revision. |

### 1.4.4 algo_egress_scratchregister

Reg. 0xA003000C

Scratchregister register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchregister | rw | na | 0x12345678 | SW can write to it and read from it for test purposes. |

### 1.4.5 algo_egress_irq_enable

Reg. 0xA0030010

Interrupt Requests Enable/Mask Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_enable | rw | ro | 0x0 | IRQ0 enable bit. Not implemented here/DTEC |
| 1 | irq1_enable | rw | ro | 0x0 | IRQ1 enable bit. Not implemented here/DTEC |

### 1.4.6 algo_egress_irq_pending

Reg. 0xA0030014

Interrupt Pending Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 0 | irq0_pending | r/w1c | wo | 0x0 | IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |
| 1 | irq1_pending | r/w1c | wo | 0x0 | IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |

### 1.4.7 algo_egress_irq_raw

Reg. 0xA0030018

Interrupt Raw Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_raw | ro | wo | 0x0 | IRQ0 raw status bit. Not implemented here/DTEC |
| 1 | irq1_raw | ro | wo | 0x0 | IRQ1 raw status bit. Not implemented here/DTEC |

### 1.4.8 algo_egress_irq_force

Reg. 0xA003001C

Interrupt Force Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC |
| 1 | irq1_force | rw | ro | 0x0 | IRQ1 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC |

### 1.4.9 region_1_start_tag

Reg. 0xA0031000

region_1_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_1_start_tag | ro | wo | X | region_1_start_tag |

### 1.4.10 region_1_dtec_tod_lsbs

Reg. 0xA0031004

region_1_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_1_dtec_tod_lsbs | ro | wo | X | region_1_dtec_tod_lsbs |

### 1.4.11 region_1_dtec_tod_msbs

Reg. 0xA0031008

region_1_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_1_dtec_tod_msbs | ro | wo | X | region_1_dtec_tod_msbs |

### 1.4.12 region_1_dtec_lts

Reg. 0xA003100C

region_1_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_1_dtec_lts | ro | wo | X | region_1_dtec_lts |

### 1.4.13 dtec_algo_rev_revision_major

Reg. 0xA0031010

Major version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dtec_algo_rev_revision_major | ro | wo | X | Major version |

### 1.4.14 dtec_algo_rev_revision_minor

Reg. 0xA0031014

Minor version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dtec_algo_rev_revision_minor | ro | wo | X | Minor version |

### 1.4.15 dtec_algo_rev_revision_patch

Reg. 0xA0031018

Patch version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dtec_algo_rev_revision_patch | ro | wo | X | Patch version |

### 1.4.16 spares_spare_uint_1

Reg. 0xA003101C

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_1 | ro | wo | X | Spare unsigned integer |

### 1.4.17 spares_spare_uint_2

Reg. 0xA0031020

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_2 | ro | wo | X | Spare unsigned integer |

### 1.4.18 spares_spare_uint_3

Reg. 0xA0031024

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_3 | ro | wo | X | Spare unsigned integer |

### 1.4.19 spares_spare_uint_4

Reg. 0xA0031028

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_4 | ro | wo | X | Spare unsigned integer |

### 1.4.20 spares_spare_uint_5

Reg. 0xA003102C

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_5 | ro | wo | X | Spare unsigned integer |

### 1.4.21 spares_spare_uint_6

Reg. 0xA0031030

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_6 | ro | wo | X | Spare unsigned integer |

### 1.4.22 spares_spare_uint_7

Reg. 0xA0031034

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_7 | ro | wo | X | Spare unsigned integer |

### 1.4.23 spares_spare_uint_8

Reg. 0xA0031038

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_8 | ro | wo | X | Spare unsigned integer |

### 1.4.24 spares_spare_uint_9

Reg. 0xA003103C

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_9 | ro | wo | X | Spare unsigned integer |

### 1.4.25 spares_spare_uint_10

Reg. 0xA0031040

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_10 | ro | wo | X | Spare unsigned integer |

### 1.4.26 spares_spare_uint_11

Reg. 0xA0031044

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_11 | ro | wo | X | Spare unsigned integer |

### 1.4.27 spares_spare_uint_12

Reg. 0xA0031048

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_12 | ro | wo | X | Spare unsigned integer |

### 1.4.28 spares_spare_uint_13

Reg. 0xA003104C

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_13 | ro | wo | X | Spare unsigned integer |

### 1.4.29 spares_spare_uint_14

Reg. 0xA0031050

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_14 | ro | wo | X | Spare unsigned integer |

### 1.4.30 spares_spare_uint_15

0xA0031054

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_15 | ro | wo | X | Spare unsigned integer |

### 1.4.31 spares_spare_uint_16

0xA0031058

Spare unsigned integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_uint_16 | ro | wo | X | Spare unsigned integer |

### 1.4.32 spares_spare_int_1

0xA003105C

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_1 | ro | wo | X | Spare signed integer |

### 1.4.33 spares_spare_int_2

0xA0031060

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_2 | ro | wo | X | Spare signed integer |

### 1.4.34 spares_spare_int_3

0xA0031064

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_3 | ro | wo | X | Spare signed integer |

### 1.4.35 spares_spare_int_4

0xA0031068

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_4 | ro | wo | X | Spare signed integer |

### 1.4.36 spares_spare_int_5

0xA003106C

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_5 | ro | wo | X | Spare signed integer |

### 1.4.37 spares_spare_int_6

Reg. 0xA0031070

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_6 | ro | wo | X | Spare signed integer |

### 1.4.38 spares_spare_int_7

Reg. 0xA0031074

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_7 | ro | wo | X | Spare signed integer |

### 1.4.39 spares_spare_int_8

Reg. 0xA0031078

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_8 | ro | wo | X | Spare signed integer |

### 1.4.40 spares_spare_int_9

Reg. 0xA003107C

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_9 | ro | wo | X | Spare signed integer |

### 1.4.41 spares_spare_int_10

Reg. 0xA0031080

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_10 | ro | wo | X | Spare signed integer |

### 1.4.42 spares_spare_int_11

Reg. 0xA0031084

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_11 | ro | wo | X | Spare signed integer |

### 1.4.43 spares_spare_int_12

Reg. 0xA0031088

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_12 | ro | wo | X | Spare signed integer |

### 1.4.44 spares_spare_int_13

Reg. 0xA003108C

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_13 | ro | wo | X | Spare signed integer |

### 1.4.45 spares_spare_int_14

Reg. 0xA0031090

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_14 | ro | wo | X | Spare signed integer |

### 1.4.46 spares_spare_int_15

Reg. 0xA0031094

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_15 | ro | wo | X | Spare signed integer |

### 1.4.47 spares_spare_int_16

Reg. 0xA0031098

Spare signed integer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_int_16 | ro | wo | X | Spare signed integer |

### 1.4.48 spares_spare_ufi_1

Reg. 0xA003109C

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_1 | ro | wo | X | Spare unsigned fixed point |

### 1.4.49 spares_spare_ufi_2

Reg. 0xA00310A0

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_2 | ro | wo | X | Spare unsigned fixed point |

### 1.4.50 spares_spare_ufi_3

Reg. 0xA00310A4

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_3 | ro | wo | X | Spare unsigned fixed point |

### 1.4.51 spares_spare_ufi_4

Reg. 0xA00310A8

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_4 | ro | wo | X | Spare unsigned fixed point |

### 1.4.52 spares_spare_ufi_5

Reg. 0xA00310AC

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_5 | ro | wo | X | Spare unsigned fixed point |

### 1.4.53 spares_spare_ufi_6

Reg. 0xA00310B0

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_6 | ro | wo | X | Spare unsigned fixed point |

### 1.4.54 spares_spare_ufi_7

Reg. 0xA00310B4

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_7 | ro | wo | X | Spare unsigned fixed point |

### 1.4.55 spares_spare_ufi_8

Reg. 0xA00310B8

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_8 | ro | wo | X | Spare unsigned fixed point |

### 1.4.56 spares_spare_ufi_9

Reg. 0xA00310BC

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_9 | ro | wo | X | Spare unsigned fixed point |

### 1.4.57 spares_spare_ufi_10

Reg. 0xA00310C0

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_10 | ro | wo | X | Spare unsigned fixed point |

### 1.4.58 spares_spare_ufi_11

Reg. 0xA00310C4

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_11 | ro | wo | X | Spare unsigned fixed point |

### 1.4.59 spares_spare_ufi_12

Reg. 0xA00310C8

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_12 | ro | wo | X | Spare unsigned fixed point |

### 1.4.60 spares_spare_ufi_13

Reg. 0xA00310CC

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_13 | ro | wo | X | Spare unsigned fixed point |

### 1.4.61 spares_spare_ufi_14

Reg. 0xA00310D0

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_14 | ro | wo | X | Spare unsigned fixed point |

### 1.4.62 spares_spare_ufi_15

Reg. 0xA00310D4

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_15 | ro | wo | X | Spare unsigned fixed point |

### 1.4.63 spares_spare_ufi_16

Reg. 0xA00310D8

Spare unsigned fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_ufi_16 | ro | wo | X | Spare unsigned fixed point |

### 1.4.64 spares_spare_sfi_1

Reg. 0xA00310DC

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_1 | ro | wo | X | Spare signed fixed point |

### 1.4.65 spares_spare_sfi_2

Reg. 0xA00310E0

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_2 | ro | wo | X | Spare signed fixed point |

### 1.4.66 spares_spare_sfi_3

Reg. 0xA00310E4

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_3 | ro | wo | X | Spare signed fixed point |

### 1.4.67 spares_spare_sfi_4

Reg. 0xA00310E8

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_4 | ro | wo | X | Spare signed fixed point |

### 1.4.68 spares_spare_sfi_5

Reg. 0xA00310EC

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_5 | ro | wo | X | Spare signed fixed point |

### 1.4.69 spares_spare_sfi_6

Reg. 0xA00310F0

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_6 | ro | wo | X | Spare signed fixed point |

### 1.4.70 spares_spare_sfi_7

Reg. 0xA00310F4

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_7 | ro | wo | X | Spare signed fixed point |

### 1.4.71 spares_spare_sfi_8

Reg. 0xA00310F8

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_8 | ro | wo | X | Spare signed fixed point |

### 1.4.72 spares_spare_sfi_9

Reg. 0xA00310FC

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_9 | ro | wo | X | Spare signed fixed point |

### 1.4.73 spares_spare_sfi_10

Reg. 0xA0031100

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_10 | ro | wo | X | Spare signed fixed point |

### 1.4.74 spares_spare_sfi_11

Reg. 0xA0031104

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_11 | ro | wo | X | Spare signed fixed point |

### 1.4.75 spares_spare_sfi_12

Reg. 0xA0031108

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_12 | ro | wo | X | Spare signed fixed point |

### 1.4.76 spares_spare_sfi_13

Reg. 0xA003110C

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_13 | ro | wo | X | Spare signed fixed point |

### 1.4.77 spares_spare_sfi_14

Reg. 0xA0031110

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_14 | ro | wo | X | Spare signed fixed point |

### 1.4.78 spares_spare_sfi_15

Reg. 0xA0031114

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_15 | ro | wo | X | Spare signed fixed point |

### 1.4.79 spares_spare_sfi_16

Reg. 0xA0031118

Spare signed fixed point

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | spares_spare_sfi_16 | ro | wo | X | Spare signed fixed point |

### 1.4.80 region_1_end_tag

Reg. 0xA003111C

region_1_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_1_end_tag | ro | wo | X | region_1_end_tag |

### 1.4.81 region_4_start_tag

Reg. 0xA0034000

region_4_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_4_start_tag | ro | wo | X | region_4_start_tag |

### 1.4.82 region_4_dtec_tod_lsbs

Reg. 0xA0034004

region_4_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_4_dtec_tod_lsbs | ro | wo | X | region_4_dtec_tod_lsbs |

### 1.4.83 region_4_dtec_tod_msbs

Reg. 0xA0034008

region_4_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_4_dtec_tod_msbs | ro | wo | X | region_4_dtec_tod_msbs |

### 1.4.84 region_4_dtec_lts

Reg. 0xA003400C

region_4_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_4_dtec_lts | ro | wo | X | region_4_dtec_lts |

### 1.4.85 dcm_fb_metrics_fb_lm

Reg. 0xA0034010

Median of L

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_fb_lm | ro | wo | X | Median of L |

### 1.4.86 dcm_fb_metrics_fb_tm

Reg. 0xA0034014

Median of T

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_fb_tm | ro | wo | X | Median of T |

### 1.4.87 dcm_fb_metrics_fb_cm

Reg. 0xA0034018

Median of C

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_fb_cm | ro | wo | X | Median of C |

### 1.4.88 dcm_fb_metrics_fb_dm

Reg. 0xA003401C

Median of D

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_fb_dm | ro | wo | X | Median of D |

### 1.4.89 dcm_fb_metrics_sigmal

Reg. 0xA0034020

Std of L

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_sigmal | ro | wo | X | Std of L |

### 1.4.90 dcm_fb_metrics_sigmat

Reg. 0xA0034024

std of T

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_sigmat | ro | wo | X | std of T |

### 1.4.91 dcm_fb_metrics_sigmac

Reg. 0xA0034028

std of C

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_sigmac | ro | wo | X | std of C |

### 1.4.92 dcm_fb_metrics_sigmad

Reg. 0xA003402C

std of D

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_sigmad | ro | wo | X | std of D |

### 1.4.93 dcm_fb_metrics_maindropletnumber

Reg. 0xA0034030

# main-droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_maindropletnumber | ro | wo | X | # main-droplets |

### 1.4.94 dcm_fb_metrics_presubnumber

Reg. 0xA0034034

# pre-sub-coalesced droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_presubnumber | ro | wo | X | # pre-sub-coalesced droplets |

### 1.4.95 dcm_fb_metrics_multpresubnumber

Reg. 0xA0034038

# droplets with more than 1 pre-sub-coalesced droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_multpresubnumber | ro | wo | X | # droplets with more than 1 pre-sub-coalesced droplets |

### 1.4.96 dcm_fb_metrics_leftpeakmissednumber

Reg. 0xA003403C

# no intermediate droplets before antinode/ # main droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_leftpeakmissednumber | ro | wo | X | # no intermediate droplets before antinode/ # main droplets |

### 1.4.97 dcm_fb_metrics_rightpeakmissednumber

Reg. 0xA0034040

# no intermediate droplets after antinode/ # main droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_rightpeakmissednumber | ro | wo | X | # no intermediate droplets after antinode/ # main droplets |

### 1.4.98 dcm_fb_metrics_timestamp_tod_lsb

Reg. 0xA0034044

Time of Day register. it increments at 8ns resolution for the first PDS packet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_timestamp_tod_lsb | ro | wo | X | Time of Day register. it increments at 8ns resolution for the first PDS packet |

### 1.4.99 dcm_fb_metrics_timestamp_tod_msb

Reg. 0xA0034048

Time of Day register. it increments at 8ns resolution for the first PDS packet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_timestamp_tod_msb | ro | wo | X | Time of Day register. it increments at 8ns resolution for the first PDS packet |

### 1.4.100 dcm_fb_metrics_timestamp_lts

Reg. 0xA003404C

Local Time Stamp. Synchronized with 32bit eTEC timestamp.for the first PDS packet

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_fb_metrics_timestamp_lts | ro | wo | X | Local Time Stamp. Synchronized with 32bit eTEC timestamp.for the first PDS packet |

### 1.4.101 region_4_end_tag

Reg. 0xA0034050

region_4_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_4_end_tag | ro | wo | X | region_4_end_tag |

### 1.4.102 region_5_start_tag

Reg. 0xA0035000

region_5_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_5_start_tag | ro | wo | X | region_5_start_tag |

### 1.4.103 region_5_dtec_tod_lsbs

Reg. 0xA0035004

region_5_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_5_dtec_tod_lsbs | ro | wo | X | region_5_dtec_tod_lsbs |

### 1.4.104 region_5_dtec_tod_msbs

Reg. 0xA0035008

region_5_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_5_dtec_tod_msbs | ro | wo | X | region_5_dtec_tod_msbs |

### 1.4.105 region_5_dtec_lts

Reg. 0xA003500C

region_5_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_5_dtec_lts | ro | wo | X | region_5_dtec_lts |

### 1.4.106 ddm_fb_metrics_maindropletnumber

Reg. 0xA0035010

# main-droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_maindropletnumber | ro | wo | X | # main-droplets |

### 1.4.107 ddm_fb_metrics_satelliterate

Reg. 0xA0035014

# pre-sub-coalesced droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_satelliterate | ro | wo | X | # pre-sub-coalesced droplets |

### 1.4.108 ddm_fb_metrics_xint3sigma

Reg. 0xA0035018

3-sigma of crossing intervals

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_xint3sigma | ro | wo | X | 3-sigma of crossing intervals |

### 1.4.109 ddm_fb_metrics_xintmean

Reg. 0xA003501C

3-sigma of crossing intervals

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_xintmean | ro | wo | X | 3-sigma of crossing intervals |

### 1.4.110 ddm_fb_metrics_mainpeak

Reg. 0xA0035020

3-sigma of crossing intervals

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_mainpeak | ro | wo | X | 3-sigma of crossing intervals |

### 1.4.111 ddm_fb_metrics_pf_exposuredc

Reg. 0xA0035024

3-sigma of crossing intervals

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_pf_exposuredc | ro | wo | X | 3-sigma of crossing intervals |

### 1.4.112 ddm_fb_metrics_signalquality

Reg. 0xA0035028

Signal quality calculated using width, value, and noise

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_signalquality | ro | wo | X | Signal quality calculated using width, value, and noise |

### 1.4.113 ddm_fb_metrics_timestamp_tod_lsb

Reg. 0xA003502C

Time of Day register. it increments at 8ns resolution

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_timestamp_tod_lsb | ro | wo | X | Time of Day register. it increments at 8ns resolution |

### 1.4.114 ddm_fb_metrics_timestamp_tod_msb

Reg. 0xA0035030

Time of Day register. it increments at 8ns resolution

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_timestamp_tod_msb | ro | wo | X | Time of Day register. it increments at 8ns resolution |

### 1.4.115 ddm_fb_metrics_timestamp_lts

Reg. 0xA0035034

Local Time Stamp. Synchronized with 32bit eTEC timestamp.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ddm_fb_metrics_timestamp_lts | ro | wo | X | Local Time Stamp. Synchronized with 32bit eTEC timestamp. |

### 1.4.116 region_5_end_tag

Reg. 0xA0035038

region_5_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_5_end_tag | ro | wo | X | region_5_end_tag |

### 1.4.117 region_6_start_tag

Reg. 0xA0036000

region_6_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_6_start_tag | ro | wo | X | region_6_start_tag |

### 1.4.118 region_6_dtec_tod_lsbs

Reg. 0xA0036004

region_6_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_6_dtec_tod_lsbs | ro | wo | X | region_6_dtec_tod_lsbs |

### 1.4.119 region_6_dtec_tod_msbs

Reg. 0xA0036008

region_6_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_6_dtec_tod_msbs | ro | wo | X | region_6_dtec_tod_msbs |

### 1.4.120 region_6_dtec_lts

Reg. 0xA003600C

region_6_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_6_dtec_lts | ro | wo | X | region_6_dtec_lts |

### 1.4.121 damp_waveformparamspkg_damp_signals_1

Reg. 0xA0036010

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_1 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.122 damp_waveformparamspkg_damp_signals_2

Reg. 0xA0036014

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_2 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.123 damp_waveformparamspkg_damp_signals_3

Reg. 0xA0036018

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_3 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.124 damp_waveformparamspkg_damp_signals_4

Reg. 0xA003601C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_4 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.125 damp_waveformparamspkg_damp_signals_5

Reg. 0xA0036020

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_5 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.126 damp_waveformparamspkg_damp_signals_6

Reg. 0xA0036024

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_6 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.127 damp_waveformparamspkg_damp_signals_7

Reg. 0xA0036028

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_7 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.128 damp_waveformparamspkg_damp_signals_8

Reg. 0xA003602C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_8 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.129 damp_waveformparamspkg_damp_signals_9

Reg. 0xA0036030

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_9 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.130 damp_waveformparamspkg_damp_signals_10

Reg. 0xA0036034

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_10 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.131 damp_waveformparamspkg_damp_signals_11

Reg. 0xA0036038

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_11 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.132 damp_waveformparamspkg_damp_signals_12

Reg. 0xA003603C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_12 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.133 damp_waveformparamspkg_damp_signals_13

Reg. 0xA0036040

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_13 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.134 damp_waveformparamspkg_damp_signals_14

Reg. 0xA0036044

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_14 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.135 damp_waveformparamspkg_damp_signals_15

Reg. 0xA0036048

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_15 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.136 damp_waveformparamspkg_damp_signals_16

Reg. 0xA003604C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_16 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.137 damp_waveformparamspkg_damp_signals_17

Reg. 0xA0036050

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_17 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.138 damp_waveformparamspkg_damp_signals_18

Reg. 0xA0036054

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_18 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.139 damp_waveformparamspkg_damp_signals_19

Reg. 0xA0036058

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_19 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.140 damp_waveformparamspkg_damp_signals_20

Reg. 0xA003605C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_20 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.141 damp_waveformparamspkg_damp_signals_21

Reg. 0xA0036060

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_21 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.142 damp_waveformparamspkg_damp_signals_22

Reg. 0xA0036064

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_22 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.143 damp_waveformparamspkg_damp_signals_23

Reg. 0xA0036068

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_23 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.144 damp_waveformparamspkg_damp_signals_24

Reg. 0xA003606C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_24 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.145 damp_waveformparamspkg_damp_signals_25

Reg. 0xA0036070

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_25 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.146 damp_waveformparamspkg_damp_signals_26

Reg. 0xA0036074

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_26 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.147 damp_waveformparamspkg_damp_signals_27

Reg. 0xA0036078

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_si | ro | wo | X | 512 bytes from dTEC 2 DAMP |

| | | | | | |
|---|---|---|---|---|---|
| | gnals_27 | | | | |

### 1.4.148 damp_waveformparamspkg_damp_signals_28

Reg. 0xA003607C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_28 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.149 damp_waveformparamspkg_damp_signals_29

Reg. 0xA0036080

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_29 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.150 damp_waveformparamspkg_damp_signals_30

Reg. 0xA0036084

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_30 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.151 damp_waveformparamspkg_damp_signals_31

Reg. 0xA0036088

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_31 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.152 damp_waveformparamspkg_damp_signals_32

Reg. 0xA003608C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_32 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.153 damp_waveformparamspkg_damp_signals_33

Reg. 0xA0036090

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_33 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.154 damp_waveformparamspkg_damp_signals_34

Reg. 0xA0036094

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformpa | ro | wo | X | 512 bytes from dTEC 2 DAMP |

| | | | | | |
|---|---|---|---|---|---|
| | ramspkg_damp_signals_34 | | | | |

### 1.4.155 damp_waveformparamspkg_damp_signals_35

Reg. 0xA0036098

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_35 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.156 damp_waveformparamspkg_damp_signals_36

Reg. 0xA003609C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_36 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.157 damp_waveformparamspkg_damp_signals_37

Reg. 0xA00360A0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_37 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.158 damp_waveformparamspkg_damp_signals_38

Reg. 0xA00360A4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_38 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.159 damp_waveformparamspkg_damp_signals_39

Reg. 0xA00360A8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_39 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.160 damp_waveformparamspkg_damp_signals_40

Reg. 0xA00360AC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_40 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.161 damp_waveformparamspkg_damp_signals_41

Reg. 0xA00360B0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_41 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.162 damp_waveformparamspkg_damp_signals_42

Reg. 0xA00360B4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_42 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.163 damp_waveformparamspkg_damp_signals_43

Reg. 0xA00360B8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_43 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.164 damp_waveformparamspkg_damp_signals_44

Reg. 0xA00360BC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_44 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.165 damp_waveformparamspkg_damp_signals_45

Reg. 0xA00360C0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_45 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.166 damp_waveformparamspkg_damp_signals_46

Reg. 0xA00360C4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_46 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.167 damp_waveformparamspkg_damp_signals_47

Reg. 0xA00360C8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_47 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.168 damp_waveformparamspkg_damp_signals_48

Reg. 0xA00360CC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_48 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.169 damp_waveformparamspkg_damp_signals_49

Reg. 0xA00360D0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_49 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.170 damp_waveformparamspkg_damp_signals_50

Reg. 0xA00360D4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_50 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.171 damp_waveformparamspkg_damp_signals_51

Reg. 0xA00360D8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_51 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.172 damp_waveformparamspkg_damp_signals_52

Reg. 0xA00360DC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_52 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.173 damp_waveformparamspkg_damp_signals_53

Reg. 0xA00360E0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_53 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.174 damp_waveformparamspkg_damp_signals_54

Reg. 0xA00360E4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_54 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.175 damp_waveformparamspkg_damp_signals_55

Reg. 0xA00360E8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_55 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.176 damp_waveformparamspkg_damp_signals_56

Reg. 0xA00360EC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_56 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.177 damp_waveformparamspkg_damp_signals_57

Reg. 0xA00360F0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_57 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.178 damp_waveformparamspkg_damp_signals_58

Reg. 0xA00360F4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_58 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.179 damp_waveformparamspkg_damp_signals_59

Reg. 0xA00360F8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_59 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.180 damp_waveformparamspkg_damp_signals_60

Reg. 0xA00360FC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_60 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.181 damp_waveformparamspkg_damp_signals_61

Reg. 0xA0036100

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_61 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.182 damp_waveformparamspkg_damp_signals_62

Reg. 0xA0036104

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_62 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.183 damp_waveformparamspkg_damp_signals_63

Reg. 0xA0036108

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_63 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.184 damp_waveformparamspkg_damp_signals_64

Reg. 0xA003610C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_64 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.185 damp_waveformparamspkg_damp_signals_65

Reg. 0xA0036110

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_65 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.186 damp_waveformparamspkg_damp_signals_66

Reg. 0xA0036114

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_66 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.187 damp_waveformparamspkg_damp_signals_67

Reg. 0xA0036118

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_67 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.188 damp_waveformparamspkg_damp_signals_68

Reg. 0xA003611C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_68 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.189 damp_waveformparamspkg_damp_signals_69

Reg. 0xA0036120

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_69 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.190 damp_waveformparamspkg_damp_signals_70

Reg. 0xA0036124

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_70 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.191 damp_waveformparamspkg_damp_signals_71

Reg. 0xA0036128

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_71 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.192 damp_waveformparamspkg_damp_signals_72

Reg. 0xA003612C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_72 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.193 damp_waveformparamspkg_damp_signals_73

Reg. 0xA0036130

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_73 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.194 damp_waveformparamspkg_damp_signals_74

Reg. 0xA0036134

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_74 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.195 damp_waveformparamspkg_damp_signals_75

Reg. 0xA0036138

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_75 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

| | | | | | |
|---|---|---|---|---|---|
| | gnals_75 | | | | |

### 1.4.196 damp_waveformparamspkg_damp_signals_76

Reg. 0xA003613C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_76 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.197 damp_waveformparamspkg_damp_signals_77

Reg. 0xA0036140

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_77 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.198 damp_waveformparamspkg_damp_signals_78

Reg. 0xA0036144

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_78 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.199 damp_waveformparamspkg_damp_signals_79

Reg. 0xA0036148

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_79 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.200 damp_waveformparamspkg_damp_signals_80

Reg. 0xA003614C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_80 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.201 damp_waveformparamspkg_damp_signals_81

Reg. 0xA0036150

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_81 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.202 damp_waveformparamspkg_damp_signals_82

Reg. 0xA0036154

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformpa | ro | wo | X | 512 bytes from dTEC 2 DAMP |

| | | | | | |
|---|---|---|---|---|---|
| | ramspkg_damp_signals_82 | | | | |

### 1.4.203 damp_waveformparamspkg_damp_signals_83

Reg. 0xA0036158

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_83 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.204 damp_waveformparamspkg_damp_signals_84

Reg. 0xA003615C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_84 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.205 damp_waveformparamspkg_damp_signals_85

Reg. 0xA0036160

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_85 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.206 damp_waveformparamspkg_damp_signals_86

Reg. 0xA0036164

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_86 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.207 damp_waveformparamspkg_damp_signals_87

Reg. 0xA0036168

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_87 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.208 damp_waveformparamspkg_damp_signals_88

Reg. 0xA003616C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_88 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.209 damp_waveformparamspkg_damp_signals_89

Reg. 0xA0036170

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_89 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.210 damp_waveformparamspkg_damp_signals_90

Reg. 0xA0036174

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_90 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.211 damp_waveformparamspkg_damp_signals_91

Reg. 0xA0036178

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_91 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.212 damp_waveformparamspkg_damp_signals_92

Reg. 0xA003617C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_92 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.213 damp_waveformparamspkg_damp_signals_93

Reg. 0xA0036180

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_93 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.214 damp_waveformparamspkg_damp_signals_94

Reg. 0xA0036184

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_94 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.215 damp_waveformparamspkg_damp_signals_95

Reg. 0xA0036188

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_95 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.216 damp_waveformparamspkg_damp_signals_96

Reg. 0xA003618C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_96 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.217 damp_waveformparamspkg_damp_signals_97

Reg. 0xA0036190

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_97 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.218 damp_waveformparamspkg_damp_signals_98

Reg. 0xA0036194

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_98 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.219 damp_waveformparamspkg_damp_signals_99

Reg. 0xA0036198

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_99 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.220 damp_waveformparamspkg_damp_signals_100

Reg. 0xA003619C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_100 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.221 damp_waveformparamspkg_damp_signals_101

Reg. 0xA00361A0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_101 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.222 damp_waveformparamspkg_damp_signals_102

Reg. 0xA00361A4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_102 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.223 damp_waveformparamspkg_damp_signals_103

Reg. 0xA00361A8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_103 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.224 damp_waveformparamspkg_damp_signals_104

Reg. 0xA00361AC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_104 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.225 damp_waveformparamspkg_damp_signals_105

Reg. 0xA00361B0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_105 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.226 damp_waveformparamspkg_damp_signals_106

Reg. 0xA00361B4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_106 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.227 damp_waveformparamspkg_damp_signals_107

Reg. 0xA00361B8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_107 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.228 damp_waveformparamspkg_damp_signals_108

Reg. 0xA00361BC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_108 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.229 damp_waveformparamspkg_damp_signals_109

Reg. 0xA00361C0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_109 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.230 damp_waveformparamspkg_damp_signals_110

0xA00361C4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_110 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.231 damp_waveformparamspkg_damp_signals_111

0xA00361C8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_111 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.232 damp_waveformparamspkg_damp_signals_112

0xA00361CC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_112 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.233 damp_waveformparamspkg_damp_signals_113

0xA00361D0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_113 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.234 damp_waveformparamspkg_damp_signals_114

0xA00361D4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_114 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.235 damp_waveformparamspkg_damp_signals_115

0xA00361D8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_115 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.236 damp_waveformparamspkg_damp_signals_116

0xA00361DC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_116 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.237 damp_waveformparamspkg_damp_signals_117

Reg. 0xA00361E0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_117 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.238 damp_waveformparamspkg_damp_signals_118

Reg. 0xA00361E4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_118 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.239 damp_waveformparamspkg_damp_signals_119

Reg. 0xA00361E8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_119 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.240 damp_waveformparamspkg_damp_signals_120

Reg. 0xA00361EC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_120 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.241 damp_waveformparamspkg_damp_signals_121

Reg. 0xA00361F0

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_121 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.242 damp_waveformparamspkg_damp_signals_122

Reg. 0xA00361F4

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_122 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.243 damp_waveformparamspkg_damp_signals_123

Reg. 0xA00361F8

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_si | ro | wo | X | 512 bytes from dTEC 2 DAMP |

| | | | | | |
|---|---|---|---|---|---|
| | gnals_123 | | | | |

### 1.4.244 damp_waveformparamspkg_damp_signals_124

Reg. 0xA00361FC

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_124 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.245 damp_waveformparamspkg_damp_signals_125

Reg. 0xA0036200

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_125 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.246 damp_waveformparamspkg_damp_signals_126

Reg. 0xA0036204

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_126 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.247 damp_waveformparamspkg_damp_signals_127

Reg. 0xA0036208

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_127 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.248 damp_waveformparamspkg_damp_signals_128

Reg. 0xA003620C

512 bytes from dTEC 2 DAMP

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | damp_waveformparamspkg_damp_signals_128 | ro | wo | X | 512 bytes from dTEC 2 DAMP |

### 1.4.249 region_6_end_tag

Reg. 0xA0036210

region_6_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_6_end_tag | ro | wo | X | region_6_end_tag |

### 1.4.250 region_7_start_tag

Reg. 0xA0037000

region_7_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_7_start_tag | ro | wo | X | region_7_start_tag |

### 1.4.251 region_7_dtec_tod_lsbs

Reg. 0xA0037004

region_7_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_7_dtec_tod_lsbs | ro | wo | X | region_7_dtec_tod_lsbs |

### 1.4.252 region_7_dtec_tod_msbs

Reg. 0xA0037008

region_7_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_7_dtec_tod_msbs | ro | wo | X | region_7_dtec_tod_msbs |

### 1.4.253 region_7_dtec_lts

Reg. 0xA003700C

region_7_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_7_dtec_lts | ro | wo | X | region_7_dtec_lts |

### 1.4.254 solutiontable_out_solutiontype

Reg. 0xA0037010

0: 2 sine square waveform
1: HWO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_solutiontype | ro | wo | X | 0: 2 sine square waveform<br>1: HWO |

### 1.4.255 solutiontable_out_hyperparameters_1

Reg. 0xA0037014

Vector of HyperParameters:
1. f0
2. N0
3. N1
4. As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_hyperparameters_1 | ro | wo | X | Vector of HyperParameters:<br>1. f0<br>2. N0<br>3. N1<br>4. As |

### 1.4.256 solutiontable_out_hyperparameters_2

Reg. 0xA0037018

Vector of HyperParameters:
1. f0
2. N0
3. N1
4. As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_hyperparameters_2 | ro | wo | X | Vector of HyperParameters:<br>1. f0<br>2. N0<br>3. N1<br>4. As |

### 1.4.257 solutiontable_out_hyperparameters_3

Reg. 0xA003701C

Vector of HyperParameters:
1. f0
2. N0
3. N1
4. As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_hyperparameters_3 | ro | wo | X | Vector of HyperParameters:<br>1. f0<br>2. N0<br>3. N1<br>4. As |

### 1.4.258 solutiontable_out_hyperparameters_4

Reg. 0xA0037020

Vector of HyperParameters:
1. f0
2. N0
3. N1
4. As

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_hyperparameters_4 | ro | wo | X | Vector of HyperParameters:<br>1. f0<br>2. N0<br>3. N1<br>4. As |

### 1.4.259 solutiontable_out_sineamps_1

Reg. 0xA0037024

Sine Amplitudes:
1. A0
2. A1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_sineamps_1 | ro | wo | X | Sine Amplitudes:<br>1. A0<br>2. A1 |

### 1.4.260 solutiontable_out_sineamps_2

Reg. 0xA0037028

Sine Amplitudes:
1. A0
2. A1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_sineamps_2 | ro | wo | X | Sine Amplitudes:<br>1. A0<br>2. A1 |

### 1.4.261 solutiontable_out_phi0_1

Reg. 0xA003702C

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_1 | ro | wo | X | Solution table phi0 column |

### 1.4.262 solutiontable_out_phi0_2

Reg. 0xA0037030

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_2 | ro | wo | X | Solution table phi0 column |

### 1.4.263 solutiontable_out_phi0_3

Reg. 0xA0037034

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_3 | ro | wo | X | Solution table phi0 column |

### 1.4.264 solutiontable_out_phi0_4

Reg. 0xA0037038

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_4 | ro | wo | X | Solution table phi0 column |

### 1.4.265 solutiontable_out_phi0_5

Reg. 0xA003703C

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_5 | ro | wo | X | Solution table phi0 column |

### 1.4.266 solutiontable_out_phi0_6

Reg. 0xA0037040

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_6 | ro | wo | X | Solution table phi0 column |

### 1.4.267 solutiontable_out_phi0_7

Reg. 0xA0037044

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_7 | ro | wo | X | Solution table phi0 column |

### 1.4.268 solutiontable_out_phi0_8

Reg. 0xA0037048

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_8 | ro | wo | X | Solution table phi0 column |

### 1.4.269 solutiontable_out_phi0_9

Reg. 0xA003704C

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_9 | ro | wo | X | Solution table phi0 column |

### 1.4.270 solutiontable_out_phi0_10

Reg. 0xA0037050

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_10 | ro | wo | X | Solution table phi0 column |

### 1.4.271 solutiontable_out_phi0_11

Reg. 0xA0037054

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_11 | ro | wo | X | Solution table phi0 column |

### 1.4.272 solutiontable_out_phi0_12

Reg. 0xA0037058

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_12 | ro | wo | X | Solution table phi0 column |

### 1.4.273 solutiontable_out_phi0_13

Reg. 0xA003705C

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_13 | ro | wo | X | Solution table phi0 column |

### 1.4.274 solutiontable_out_phi0_14

Reg. 0xA0037060

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_14 | ro | wo | X | Solution table phi0 column |

### 1.4.275 solutiontable_out_phi0_15

Reg. 0xA0037064

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_15 | ro | wo | X | Solution table phi0 column |

### 1.4.276 solutiontable_out_phi0_16

Reg. 0xA0037068

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_16 | ro | wo | X | Solution table phi0 column |

### 1.4.277 solutiontable_out_phi0_17

Reg. 0xA003706C

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_17 | ro | wo | X | Solution table phi0 column |

### 1.4.278 solutiontable_out_phi0_18

Reg. 0xA0037070

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_18 | ro | wo | X | Solution table phi0 column |

### 1.4.279 solutiontable_out_phi0_19

Reg. 0xA0037074

Solution table phi0 column

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0_19 | ro | wo | X | Solution table phi0 column |

### 1.4.280 solutiontable_out_phi1_1

Reg. 0xA0037078

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_1 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.281 solutiontable_out_phi1_2

Reg. 0xA003707C

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_2 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.282 solutiontable_out_phi1_3

Reg. 0xA0037080

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_3 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.283 solutiontable_out_phi1_4

Reg. 0xA0037084

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_4 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.284 solutiontable_out_phi1_5

Reg. 0xA0037088

Solution table phi1 column.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_5 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.285 solutiontable_out_phi1_6

Reg. 0xA003708C

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_6 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.286 solutiontable_out_phi1_7

Reg. 0xA0037090

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_7 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.287 solutiontable_out_phi1_8

Reg. 0xA0037094

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_8 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.288 solutiontable_out_phi1_9

Reg. 0xA0037098

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_9 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.289 solutiontable_out_phi1_10

Reg. 0xA003709C

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_10 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.290 solutiontable_out_phi1_11

Reg. 0xA00370A0

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_o | ro | wo | X | Solution table phi1 column. |

| | | | | | |
|---|---|---|---|---|---|
| | ut_phi1_11 | | | | Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.291 solutiontable_out_phi1_12

Reg. 0xA00370A4

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_12 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.292 solutiontable_out_phi1_13

Reg. 0xA00370A8

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_13 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.293 solutiontable_out_phi1_14

Reg. 0xA00370AC

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_14 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.294 solutiontable_out_phi1_15

Reg. 0xA00370B0

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_15 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.295 solutiontable_out_phi1_16

Reg. 0xA00370B4

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_16 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.296 solutiontable_out_phi1_17

Reg. 0xA00370B8

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_17 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.297 solutiontable_out_phi1_18

Reg. 0xA00370BC

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_18 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.298 solutiontable_out_phi1_19

Reg. 0xA00370C0

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1_19 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.299 solutiontable_out_presubcoal_flag_1

Reg. 0xA00370C4

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_1 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.300 solutiontable_out_presubcoal_flag_2

Reg. 0xA00370C8

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_2 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.301 solutiontable_out_presubcoal_flag_3

Reg. 0xA00370CC

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_3 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.302 solutiontable_out_presubcoal_flag_4

Reg. 0xA00370D0

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_4 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.303 solutiontable_out_presubcoal_flag_5

Reg. 0xA00370D4

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_5 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.304 solutiontable_out_presubcoal_flag_6

Reg. 0xA00370D8

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_6 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.305 solutiontable_out_presubcoal_flag_7

Reg. 0xA00370DC

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_7 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.306 solutiontable_out_presubcoal_flag_8

Reg. 0xA00370E0

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_8 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.307 solutiontable_out_presubcoal_flag_9

Reg. 0xA00370E4

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_9 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.308 solutiontable_out_presubcoal_flag_10

Reg. 0xA00370E8

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_10 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. |

| | | | | | |
|---|---|---|---|---|---|
| | lag_10 | | | | Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.309 solutiontable_out_presubcoal_flag_11

Reg. 0xA00370EC

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_11 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.310 solutiontable_out_presubcoal_flag_12

Reg. 0xA00370F0

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_12 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.311 solutiontable_out_presubcoal_flag_13

Reg. 0xA00370F4

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_13 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.312 solutiontable_out_presubcoal_flag_14

Reg. 0xA00370F8

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_14 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.313 solutiontable_out_presubcoal_flag_15

Reg. 0xA00370FC

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_15 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.314 solutiontable_out_presubcoal_flag_16

Reg. 0xA0037100

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_16 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.315 solutiontable_out_presubcoal_flag_17

Reg. 0xA0037104

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_17 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.316 solutiontable_out_presubcoal_flag_18

Reg. 0xA0037108

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_18 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.317 solutiontable_out_presubcoal_flag_19

Reg. 0xA003710C

Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubcoal_flag_19 | ro | wo | X | Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.318 solutiontable_out_jitter_1

Reg. 0xA0037110

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_1 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.319 solutiontable_out_jitter_2

Reg. 0xA0037114

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_2 | ro | wo | X | Solution table sigmaC column. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.320 solutiontable_out_jitter_3

Reg. 0xA0037118

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_3 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.321 solutiontable_out_jitter_4

Reg. 0xA003711C

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_4 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.322 solutiontable_out_jitter_5

Reg. 0xA0037120

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_5 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.323 solutiontable_out_jitter_6

Reg. 0xA0037124

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_6 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.324 solutiontable_out_jitter_7

Reg. 0xA0037128

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_7 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.325 solutiontable_out_jitter_8

Reg. 0xA003712C

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_8 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.326 solutiontable_out_jitter_9

Reg. 0xA0037130

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_9 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.327 solutiontable_out_jitter_10

Reg. 0xA0037134

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_10 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.328 solutiontable_out_jitter_11

Reg. 0xA0037138

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_11 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.329 solutiontable_out_jitter_12

Reg. 0xA003713C

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_12 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.330 solutiontable_out_jitter_13

Reg. 0xA0037140

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_13 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.331 solutiontable_out_jitter_14

Reg. 0xA0037144

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_14 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.332 solutiontable_out_jitter_15

Reg.

0xA0037148

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_15 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.333 solutiontable_out_jitter_16

Reg.

0xA003714C

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_16 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.334 solutiontable_out_jitter_17

Reg.

0xA0037150

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_17 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.335 solutiontable_out_jitter_18

Reg.

0xA0037154

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_18 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.336 solutiontable_out_jitter_19

Reg. 0xA0037158

Solution table sigmaC column.
Std of C signal during subCL update which quantifies natural jitter.
This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_jitter_19 | ro | wo | X | Solution table sigmaC column.<br>Std of C signal during subCL update which quantifies natural jitter.<br>This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.337 solutiontable_out_multpresubrate_1

Reg. 0xA003715C

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_1 | ro | wo | X | ILT Multpresubrate |

### 1.4.338 solutiontable_out_multpresubrate_2

Reg. 0xA0037160

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_2 | ro | wo | X | ILT Multpresubrate |

### 1.4.339 solutiontable_out_multpresubrate_3

Reg. 0xA0037164

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_3 | ro | wo | X | ILT Multpresubrate |

### 1.4.340 solutiontable_out_multpresubrate_4

Reg. 0xA0037168

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_4 | ro | wo | X | ILT Multpresubrate |

### 1.4.341 solutiontable_out_multpresubrate_5

Reg. 0xA003716C

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_5 | ro | wo | X | ILT Multpresubrate |

### 1.4.342 solutiontable_out_multpresubrate_6

Reg. 0xA0037170

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_6 | ro | wo | X | ILT Multpresubrate |

### 1.4.343 solutiontable_out_multpresubrate_7

Reg. 0xA0037174

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_7 | ro | wo | X | ILT Multpresubrate |

### 1.4.344 solutiontable_out_multpresubrate_8

Reg. 0xA0037178

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_8 | ro | wo | X | ILT Multpresubrate |

### 1.4.345 solutiontable_out_multpresubrate_9

Reg. 0xA003717C

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_9 | ro | wo | X | ILT Multpresubrate |

### 1.4.346 solutiontable_out_multpresubrate_10

Reg. 0xA0037180

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_10 | ro | wo | X | ILT Multpresubrate |

### 1.4.347 solutiontable_out_multpresubrate_11

Reg. 0xA0037184

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_11 | ro | wo | X | ILT Multpresubrate |

### 1.4.348 solutiontable_out_multpresubrate_12

Reg. 0xA0037188

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_12 | ro | wo | X | ILT Multpresubrate |

### 1.4.349 solutiontable_out_multpresubrate_13

Reg. 0xA003718C

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_13 | ro | wo | X | ILT Multpresubrate |

### 1.4.350 solutiontable_out_multpresubrate_14

Reg. 0xA0037190

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_14 | ro | wo | X | ILT Multpresubrate |

### 1.4.351 solutiontable_out_multpresubrate_15

Reg. 0xA0037194

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_15 | ro | wo | X | ILT Multpresubrate |

### 1.4.352 solutiontable_out_multpresubrate_16

Reg. 0xA0037198

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_16 | ro | wo | X | ILT Multpresubrate |

### 1.4.353 solutiontable_out_multpresubrate_17

Reg. 0xA003719C

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_17 | ro | wo | X | ILT Multpresubrate |

### 1.4.354 solutiontable_out_multpresubrate_18

Reg. 0xA00371A0

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubrate_18 | ro | wo | X | ILT Multpresubrate |

### 1.4.355 solutiontable_out_multpresubrate_19

Reg. 0xA00371A4

ILT Multpresubrate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_multpresubra | ro | wo | X | ILT Multpresubrate |

| | | | | | |
|---|---|---|---|---|---|
| | te_19 | | | | |

### 1.4.356 solutiontable_out_presubrate_1

Reg. 0xA00371A8

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_1 | ro | wo | X | ILT PreSubRate |

### 1.4.357 solutiontable_out_presubrate_2

Reg. 0xA00371AC

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_2 | ro | wo | X | ILT PreSubRate |

### 1.4.358 solutiontable_out_presubrate_3

Reg. 0xA00371B0

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_3 | ro | wo | X | ILT PreSubRate |

### 1.4.359 solutiontable_out_presubrate_4

Reg. 0xA00371B4

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_4 | ro | wo | X | ILT PreSubRate |

### 1.4.360 solutiontable_out_presubrate_5

Reg. 0xA00371B8

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_5 | ro | wo | X | ILT PreSubRate |

### 1.4.361 solutiontable_out_presubrate_6

Reg. 0xA00371BC

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_6 | ro | wo | X | ILT PreSubRate |

### 1.4.362 solutiontable_out_presubrate_7

Reg. 0xA00371C0

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_7 | ro | wo | X | ILT PreSubRate |

### 1.4.363 solutiontable_out_presubrate_8

Reg. 0xA00371C4

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_8 | ro | wo | X | ILT PreSubRate |

### 1.4.364 solutiontable_out_presubrate_9

Reg. 0xA00371C8

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_9 | ro | wo | X | ILT PreSubRate |

### 1.4.365 solutiontable_out_presubrate_10

Reg. 0xA00371CC

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_10 | ro | wo | X | ILT PreSubRate |

### 1.4.366 solutiontable_out_presubrate_11

Reg. 0xA00371D0

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_11 | ro | wo | X | ILT PreSubRate |

### 1.4.367 solutiontable_out_presubrate_12

Reg. 0xA00371D4

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_12 | ro | wo | X | ILT PreSubRate |

### 1.4.368 solutiontable_out_presubrate_13

Reg. 0xA00371D8

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_13 | ro | wo | X | ILT PreSubRate |

### 1.4.369 solutiontable_out_presubrate_14

Reg. 0xA00371DC

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_14 | ro | wo | X | ILT PreSubRate |

### 1.4.370 solutiontable_out_presubrate_15

Reg. 0xA00371E0

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_15 | ro | wo | X | ILT PreSubRate |

## 1.4.371 solutiontable_out_presubrate_16

Reg. 0xA00371E4

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_16 | ro | wo | X | ILT PreSubRate |

## 1.4.372 solutiontable_out_presubrate_17

Reg. 0xA00371E8

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_17 | ro | wo | X | ILT PreSubRate |

## 1.4.373 solutiontable_out_presubrate_18

Reg. 0xA00371EC

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_18 | ro | wo | X | ILT PreSubRate |

## 1.4.374 solutiontable_out_presubrate_19

Reg. 0xA00371F0

ILT PreSubRate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_19 | ro | wo | X | ILT PreSubRate |

## 1.4.375 solutiontable_out_cm_1

Reg. 0xA00371F4

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_1 | ro | wo | X | ILT CM |

## 1.4.376 solutiontable_out_cm_2

Reg. 0xA00371F8

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_2 | ro | wo | X | ILT CM |

## 1.4.377 solutiontable_out_cm_3

Reg. 0xA00371FC

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_o | ro | wo | X | ILT CM |

| | | | | | |
|---|---|---|---|---|---|
| | ut_cm_3 | | | | |

### 1.4.378 solutiontable_out_cm_4

Reg. 0xA0037200

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_4 | ro | wo | X | ILT CM |

### 1.4.379 solutiontable_out_cm_5

Reg. 0xA0037204

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_5 | ro | wo | X | ILT CM |

### 1.4.380 solutiontable_out_cm_6

Reg. 0xA0037208

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_6 | ro | wo | X | ILT CM |

### 1.4.381 solutiontable_out_cm_7

Reg. 0xA003720C

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_7 | ro | wo | X | ILT CM |

### 1.4.382 solutiontable_out_cm_8

Reg. 0xA0037210

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_8 | ro | wo | X | ILT CM |

### 1.4.383 solutiontable_out_cm_9

Reg. 0xA0037214

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_9 | ro | wo | X | ILT CM |

### 1.4.384 solutiontable_out_cm_10

Reg. 0xA0037218

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_10 | ro | wo | X | ILT CM |

### 1.4.385 solutiontable_out_cm_11

Reg. 0xA003721C

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_11 | ro | wo | X | ILT CM |

### 1.4.386 solutiontable_out_cm_12

Reg. 0xA0037220

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_12 | ro | wo | X | ILT CM |

### 1.4.387 solutiontable_out_cm_13

Reg. 0xA0037224

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_13 | ro | wo | X | ILT CM |

### 1.4.388 solutiontable_out_cm_14

Reg. 0xA0037228

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_14 | ro | wo | X | ILT CM |

### 1.4.389 solutiontable_out_cm_15

Reg. 0xA003722C

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_15 | ro | wo | X | ILT CM |

### 1.4.390 solutiontable_out_cm_16

Reg. 0xA0037230

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_16 | ro | wo | X | ILT CM |

### 1.4.391 solutiontable_out_cm_17

Reg. 0xA0037234

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_17 | ro | wo | X | ILT CM |

### 1.4.392 solutiontable_out_cm_18

Reg. 0xA0037238

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_18 | ro | wo | X | ILT CM |

### 1.4.393 solutiontable_out_cm_19

Reg. 0xA003723C

ILT CM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_cm_19 | ro | wo | X | ILT CM |

### 1.4.394 solutiontable_out_dm_1

Reg. 0xA0037240

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_1 | ro | wo | X | ILT DM |

### 1.4.395 solutiontable_out_dm_2

Reg. 0xA0037244

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_2 | ro | wo | X | ILT DM |

### 1.4.396 solutiontable_out_dm_3

Reg. 0xA0037248

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_3 | ro | wo | X | ILT DM |

### 1.4.397 solutiontable_out_dm_4

Reg. 0xA003724C

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_4 | ro | wo | X | ILT DM |

### 1.4.398 solutiontable_out_dm_5

Reg. 0xA0037250

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_5 | ro | wo | X | ILT DM |

### 1.4.399 solutiontable_out_dm_6

Reg. 0xA0037254

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_6 | ro | wo | X | ILT DM |

### 1.4.400 solutiontable_out_dm_7

Reg. 0xA0037258

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_7 | ro | wo | X | ILT DM |

### 1.4.401 solutiontable_out_dm_8

Reg. 0xA003725C

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_8 | ro | wo | X | ILT DM |

### 1.4.402 solutiontable_out_dm_9

Reg. 0xA0037260

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_9 | ro | wo | X | ILT DM |

### 1.4.403 solutiontable_out_dm_10

Reg. 0xA0037264

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_10 | ro | wo | X | ILT DM |

### 1.4.404 solutiontable_out_dm_11

Reg. 0xA0037268

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_11 | ro | wo | X | ILT DM |

### 1.4.405 solutiontable_out_dm_12

Reg. 0xA003726C

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_12 | ro | wo | X | ILT DM |

### 1.4.406 solutiontable_out_dm_13

Reg. 0xA0037270

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_13 | ro | wo | X | ILT DM |

### 1.4.407 solutiontable_out_dm_14

Reg. 0xA0037274

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_14 | ro | wo | X | ILT DM |

### 1.4.408 solutiontable_out_dm_15

Reg. 0xA0037278

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_15 | ro | wo | X | ILT DM |

### 1.4.409 solutiontable_out_dm_16

0xA003727C

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_16 | ro | wo | X | ILT DM |

### 1.4.410 solutiontable_out_dm_17

0xA0037280

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_17 | ro | wo | X | ILT DM |

### 1.4.411 solutiontable_out_dm_18

0xA0037284

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_18 | ro | wo | X | ILT DM |

### 1.4.412 solutiontable_out_dm_19

0xA0037288

ILT DM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dm_19 | ro | wo | X | ILT DM |

### 1.4.413 solutiontable_out_dcdphi

0xA003728C

ILT DCDPhi

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_dcdphi | ro | wo | X | ILT DCDPhi |

### 1.4.414 solutiontable_out_phi1margin_1

0xA0037290

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_1 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.415 solutiontable_out_phi1margin_2

0xA0037294

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_2 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.416 solutiontable_out_phi1margin_3

Reg. 0xA0037298

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_3 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.417 solutiontable_out_phi1margin_4

Reg. 0xA003729C

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_4 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.418 solutiontable_out_phi1margin_5

Reg. 0xA00372A0

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_5 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.419 solutiontable_out_phi1margin_6

Reg. 0xA00372A4

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_6 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.420 solutiontable_out_phi1margin_7

Reg. 0xA00372A8

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_7 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.421 solutiontable_out_phi1margin_8

Reg. 0xA00372AC

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_8 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.422 solutiontable_out_phi1margin_9

Reg. 0xA00372B0

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_9 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.423 solutiontable_out_phi1margin_10

Reg. 0xA00372B4

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_10 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.424 solutiontable_out_phi1margin_11

Reg. 0xA00372B8

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_11 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.425 solutiontable_out_phi1margin_12

Reg. 0xA00372BC

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_12 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.426 solutiontable_out_phi1margin_13

Reg. 0xA00372C0

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_13 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.427 solutiontable_out_phi1margin_14

Reg. 0xA00372C4

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_14 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.428 solutiontable_out_phi1margin_15

Reg. 0xA00372C8

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_15 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.429 solutiontable_out_phi1margin_16

Reg. 0xA00372CC

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_16 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.430 solutiontable_out_phi1margin_17

Reg. 0xA00372D0

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_17 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.431 solutiontable_out_phi1margin_18

Reg. 0xA00372D4

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_18 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.432 solutiontable_out_phi1margin_19

Reg. 0xA00372D8

Solution table phi1 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi1margin_19 | ro | wo | X | Solution table phi1 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.433 solutiontable_out_phi0margin

Reg. 0xA00372DC

Solution table phi0 column.
Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_phi0margin | ro | wo | X | Solution table phi0 column.<br>Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. |

### 1.4.434 solutiontable_out_satrateavg_off

Reg. 0xA00372E0

Solution table satrateavg_off

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_satrateavg_off | ro | wo | X | Solution table satrateavg_off |

### 1.4.435 solutiontable_out_satrateavg_on

Reg. 0xA00372E4

Solution table satrateavg_on

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_satrateavg_on | ro | wo | X | Solution table satrateavg_on |

### 1.4.436 solutiontable_out_xint3sigma_avg

Reg. 0xA00372E8

Solution table xint3sigma_avg

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_xint3sigma_avg | ro | wo | X | Solution table xint3sigma_avg |

### 1.4.437 solutiontable_out_presubrate_avg

Reg. 0xA00372EC

Solution table presubrate_avg

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_presubrate_avg | ro | wo | X | Solution table presubrate_avg |

### 1.4.438 solutiontable_out_opt_solution

Reg. 0xA00372F0

Optimum Solution

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_opt_solution | ro | wo | X | Optimum Solution |

### 1.4.439 solutiontable_out_bk_solution

Reg. 0xA00372F4

Backuo Solution Index

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | solutiontable_out_bk_solution | ro | wo | X | Backuo Solution Index |

### 1.4.440 region_7_end_tag

Reg. 0xA00372F8

region_7_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_7_end_tag | ro | wo | X | region_7_end_tag |

### 1.4.441 region_8_start_tag

Reg. 0xA0038000

region_8_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_8_start_tag | ro | wo | X | region_8_start_tag |

### 1.4.442 region_8_dtec_tod_lsbs

0xA0038004

region_8_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_8_dtec_tod_lsbs | ro | wo | X | region_8_dtec_tod_lsbs |

### 1.4.443 region_8_dtec_tod_msbs

0xA0038008

region_8_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_8_dtec_tod_msbs | ro | wo | X | region_8_dtec_tod_msbs |

### 1.4.444 region_8_dtec_lts

0xA003800C

region_8_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_8_dtec_lts | ro | wo | X | region_8_dtec_lts |

### 1.4.445 req_func_out

0xA0038010

Readback of diagnostics signature for main CL algo block

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | req_func_out | ro | wo | X | Readback of diagnostics signature for main CL algo block |

### 1.4.446 state

0xA0038014

Readback of diagnostics signature for monitor algo block

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | state | ro | wo | X | Readback of diagnostics signature for monitor algo block |

### 1.4.447 test_probes_probe1

0xA0038018

Generic Test Probe 1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | test_probes_probe1 | ro | wo | X | Generic Test Probe 1 |

### 1.4.448 test_probes_probe2

0xA003801C

Generic Test Probe 2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | test_probes_probe2 | ro | wo | X | Generic Test Probe 2 |

### 1.4.449 test_probes_probe3

0xA0038020

Generic Test Probe 3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | test_probes_probe3 | ro | wo | X | Generic Test Probe 3 |

### 1.4.450 internal_clst_done_latched

Reg. 0xA0038024

Determines if CLST algo has converged for any given milisecond

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | internal_clst_done_latched | ro | wo | X | Determines if CLST algo has converged for any given milisecond |

### 1.4.451 diag_exposure_prerisetime

Reg. 0xA0038028

Rise time within 20ms (ETEC to DTEC)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | diag_exposure_prerisetime | ro | wo | X | Rise time within 20ms (ETEC to DTEC) |

### 1.4.452 diag_exposure_exposure_flag

Reg. 0xA003802C

Exposure gate signal into the dTEC algo to be 2 bit wide, with MSB being a write flag indicating new data written (1 = new data written) and LSB is the 1 bit Exposure Gate Signal.
Expand the buffer and dTEC algo for the exposure gate to receive up to 70 values in 1ms timeframe.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | diag_exposure_exposure_flag | ro | wo | X | Exposure gate signal into the dTEC algo to be 2 bit wide, with MSB being a write flag indicating new data written (1 = new data written) and LSB is the 1 bit Exposure Gate Signal.<br>Expand the buffer and dTEC algo for the exposure gate to receive up to 70 values in 1ms timeframe. |

### 1.4.453 diag_exposure_falltime_flag

Reg. 0xA0038030

Fall-time detected for exposure signals.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | diag_exposure_falltime_flag | ro | wo | X | Fall-time detected for exposure signals. |

### 1.4.454 diag_exposure_risetime_flag

Reg. 0xA0038034

Rise-time detected for exposure signals.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | diag_exposure_risetime_flag | ro | wo | X | Rise-time detected for exposure signals. |

### 1.4.455 diag_state_diag

Reg. 0xA0038038

Readback of diagnostics signature for current state

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | diag_state_diag | ro | wo | X | Readback of diagnostics signature for current state |

### 1.4.456 xer_out_xer_bank1

Reg. 0xA003803C

XER Bank 1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | xer_out_xer_bank1 | ro | wo | X | XER Bank 1 |

### 1.4.457 xer_out_xer_bank2

Reg. 0xA0038040

XER bank2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | xer_out_xer_bank2 | ro | wo | X | XER bank2 |

### 1.4.458 events_out_events_bank1

Reg. 0xA0038044

Events Bank1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | events_out_events_bank1 | ro | wo | X | Events Bank1 |

### 1.4.459 events_out_events_bank2

Reg. 0xA0038048

Events Bank2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | events_out_events_bank2 | ro | wo | X | Events Bank2 |

### 1.4.460 warnings_out_warnings_bank1

Reg. 0xA003804C

Warnings Bank1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | warnings_out_warnings_bank1 | ro | wo | X | Warnings Bank1 |

### 1.4.461 warnings_out_warnings_bank2

Reg. 0xA0038050

Warnings Bank2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | warnings_out_warnings_bank2 | ro | wo | X | Warnings Bank2 |

### 1.4.462 region_8_end_tag

Reg. 0xA0038054

region_8_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_8_end_tag | ro | wo | X | region_8_end_tag |

### 1.4.463 region_9_start_tag

Reg. 0xA0039000

region_9_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_9_start_tag | ro | wo | X | region_9_start_tag |

### 1.4.464 region_9_dtec_tod_lsbs

Reg. 0xA0039004

region_9_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | region_9_dtec_tod_lsbs | ro | wo | X | region_9_dtec_tod_lsbs |

### 1.4.465 region_9_dtec_tod_msbs

Reg. 0xA0039008

region_9_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_9_dtec_tod_msbs | ro | wo | X | region_9_dtec_tod_msbs |

### 1.4.466 region_9_dtec_lts

Reg. 0xA003900C

region_9_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_9_dtec_lts | ro | wo | X | region_9_dtec_lts |

### 1.4.467 dcm_diag_missing_droplets

Reg. 0xA0039010

Missing main droplets in 1ms

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_missing_droplets | ro | wo | X | Missing main droplets in 1ms |

### 1.4.468 dcm_diag_pklabels_roi1_1

Reg. 0xA0039014

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_1 | ro | wo | X | Labels for first ROI |

### 1.4.469 dcm_diag_pklabels_roi1_2

Reg. 0xA0039018

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_2 | ro | wo | X | Labels for first ROI |

### 1.4.470 dcm_diag_pklabels_roi1_3

Reg. 0xA003901C

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_3 | ro | wo | X | Labels for first ROI |

### 1.4.471 dcm_diag_pklabels_roi1_4

Reg. 0xA0039020

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_4 | ro | wo | X | Labels for first ROI |

### 1.4.472 dcm_diag_pklabels_roi1_5

Reg. 0xA0039024

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_5 | ro | wo | X | Labels for first ROI |

### 1.4.473 dcm_diag_pklabels_roi1_6

Reg. 0xA0039028

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_6 | ro | wo | X | Labels for first ROI |

### 1.4.474 dcm_diag_pklabels_roi1_7

Reg. 0xA003902C

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_7 | ro | wo | X | Labels for first ROI |

### 1.4.475 dcm_diag_pklabels_roi1_8

Reg. 0xA0039030

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_8 | ro | wo | X | Labels for first ROI |

### 1.4.476 dcm_diag_pklabels_roi1_9

Reg. 0xA0039034

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_9 | ro | wo | X | Labels for first ROI |

### 1.4.477 dcm_diag_pklabels_roi1_10

Reg. 0xA0039038

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_10 | ro | wo | X | Labels for first ROI |

### 1.4.478 dcm_diag_pklabels_roi1_11

Reg. 0xA003903C

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_11 | ro | wo | X | Labels for first ROI |

### 1.4.479 dcm_diag_pklabels_roi1_12

Reg. 0xA0039040

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_12 | ro | wo | X | Labels for first ROI |

### 1.4.480 dcm_diag_pklabels_roi1_13

Reg. 0xA0039044

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_13 | ro | wo | X | Labels for first ROI |

### 1.4.481 dcm_diag_pklabels_roi1_14

Reg. 0xA0039048

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_14 | ro | wo | X | Labels for first ROI |

### 1.4.482 dcm_diag_pklabels_roi1_15

Reg. 0xA003904C

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_15 | ro | wo | X | Labels for first ROI |

### 1.4.483 dcm_diag_pklabels_roi1_16

Reg. 0xA0039050

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_16 | ro | wo | X | Labels for first ROI |

### 1.4.484 dcm_diag_pklabels_roi1_17

Reg. 0xA0039054

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_17 | ro | wo | X | Labels for first ROI |

### 1.4.485 dcm_diag_pklabels_roi1_18

Reg. 0xA0039058

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_18 | ro | wo | X | Labels for first ROI |

### 1.4.486 dcm_diag_pklabels_roi1_19

Reg. 0xA003905C

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_19 | ro | wo | X | Labels for first ROI |

### 1.4.487 dcm_diag_pklabels_roi1_20

Reg. 0xA0039060

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_20 | ro | wo | X | Labels for first ROI |

### 1.4.488 dcm_diag_pklabels_roi1_21

Reg. 0xA0039064

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_21 | ro | wo | X | Labels for first ROI |

### 1.4.489 dcm_diag_pklabels_roi1_22

Reg. 0xA0039068

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_22 | ro | wo | X | Labels for first ROI |

### 1.4.490 dcm_diag_pklabels_roi1_23

Reg. 0xA003906C

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_23 | ro | wo | X | Labels for first ROI |

### 1.4.491 dcm_diag_pklabels_roi1_24

Reg. 0xA0039070

Labels for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pklabels_roi1_24 | ro | wo | X | Labels for first ROI |

### 1.4.492 dcm_diag_pkposglobal_roi1_1

Reg. 0xA0039074

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_1 | ro | wo | X | Global pk positions for first ROI |

### 1.4.493 dcm_diag_pkposglobal_roi1_2

Reg. 0xA0039078

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_2 | ro | wo | X | Global pk positions for first ROI |

### 1.4.494 dcm_diag_pkposglobal_roi1_3

Reg. 0xA003907C

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_3 | ro | wo | X | Global pk positions for first ROI |

### 1.4.495 dcm_diag_pkposglobal_roi1_4

Reg. 0xA0039080

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_4 | ro | wo | X | Global pk positions for first ROI |

### 1.4.496 dcm_diag_pkposglobal_roi1_5

Reg. 0xA0039084

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_5 | ro | wo | X | Global pk positions for first ROI |

### 1.4.497 dcm_diag_pkposglobal_roi1_6

Reg. 0xA0039088

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_6 | ro | wo | X | Global pk positions for first ROI |

### 1.4.498 dcm_diag_pkposglobal_roi1_7

Reg. 0xA003908C

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_7 | ro | wo | X | Global pk positions for first ROI |

### 1.4.499 dcm_diag_pkposglobal_roi1_8

Reg. 0xA0039090

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_8 | ro | wo | X | Global pk positions for first ROI |

### 1.4.500 dcm_diag_pkposglobal_roi1_9

Reg. 0xA0039094

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_9 | ro | wo | X | Global pk positions for first ROI |

### 1.4.501 dcm_diag_pkposglobal_roi1_10

Reg. 0xA0039098

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_10 | ro | wo | X | Global pk positions for first ROI |

### 1.4.502 dcm_diag_pkposglobal_roi1_11

Reg. 0xA003909C

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_11 | ro | wo | X | Global pk positions for first ROI |

### 1.4.503 dcm_diag_pkposglobal_roi1_12

Reg. 0xA00390A0

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_12 | ro | wo | X | Global pk positions for first ROI |

### 1.4.504 dcm_diag_pkposglobal_roi1_13

Reg. 0xA00390A4

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_13 | ro | wo | X | Global pk positions for first ROI |

### 1.4.505 dcm_diag_pkposglobal_roi1_14

Reg. 0xA00390A8

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_14 | ro | wo | X | Global pk positions for first ROI |

### 1.4.506 dcm_diag_pkposglobal_roi1_15

Reg. 0xA00390AC

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_15 | ro | wo | X | Global pk positions for first ROI |

### 1.4.507 dcm_diag_pkposglobal_roi1_16

Reg. 0xA00390B0

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_16 | ro | wo | X | Global pk positions for first ROI |

### 1.4.508 dcm_diag_pkposglobal_roi1_17

Reg. 0xA00390B4

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_17 | ro | wo | X | Global pk positions for first ROI |

### 1.4.509 dcm_diag_pkposglobal_roi1_18

Reg. 0xA00390B8

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_18 | ro | wo | X | Global pk positions for first ROI |

### 1.4.510 dcm_diag_pkposglobal_roi1_19

Reg. 0xA00390BC

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_19 | ro | wo | X | Global pk positions for first ROI |

### 1.4.511 dcm_diag_pkposglobal_roi1_20

Reg. 0xA00390C0

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_20 | ro | wo | X | Global pk positions for first ROI |

### 1.4.512 dcm_diag_pkposglobal_roi1_21

Reg. 0xA00390C4

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_21 | ro | wo | X | Global pk positions for first ROI |

### 1.4.513 dcm_diag_pkposglobal_roi1_22

Reg. 0xA00390C8

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_22 | ro | wo | X | Global pk positions for first ROI |

### 1.4.514 dcm_diag_pkposglobal_roi1_23

Reg. 0xA00390CC

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_23 | ro | wo | X | Global pk positions for first ROI |

### 1.4.515 dcm_diag_pkposglobal_roi1_24

Reg. 0xA00390D0

Global pk positions for first ROI

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dcm_diag_pkposglobal_roi1_24 | ro | wo | X | Global pk positions for first ROI |

### 1.4.516 region_9_end_tag

Reg. 0xA00390D4

region_9_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_9_end_tag | ro | wo | X | region_9_end_tag |

### 1.4.517 region_10_start_tag

Reg. 0xA003A000

region_10_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_10_start_tag | ro | wo | X | region_10_start_tag |

### 1.4.518 region_10_dtec_tod_lsbs

Reg. 0xA003A004

region_10_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_10_dtec_tod_lsbs | ro | wo | X | region_10_dtec_tod_lsbs |

### 1.4.519 region_10_dtec_tod_msbs

Reg. 0xA003A008

region_10_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_10_dtec_tod_msbs | ro | wo | X | region_10_dtec_tod_msbs |

### 1.4.520 region_10_dtec_lts

Reg. 0xA003A00C

region_10_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_10_dtec_lts | ro | wo | X | region_10_dtec_lts |

### 1.4.521 clustering_dcm_diag_pkval_median_updated_label2

Reg. 0xA003A010

Median of PkVal for label2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkval_median_updated_label2 | ro | wo | X | Median of PkVal for label2 |

### 1.4.522 clustering_dcm_diag_pkval_std_updated_label2

Reg. 0xA003A014

std of PkVal for label2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkval_std_updated_label2 | ro | wo | X | std of PkVal for label2 |

### 1.4.523 clustering_dcm_diag_pkval_median_updated_label3

Reg. 0xA003A018

Median of PkVal for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkval_median_updated_label3 | ro | wo | X | Median of PkVal for label3 |

### 1.4.524 clustering_dcm_diag_pkval_std_updated_label3

Reg. 0xA003A01C

std of PkVal for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkval_std_updated_label3 | ro | wo | X | std of PkVal for label3 |

### 1.4.525 clustering_dcm_diag_pkwidth_median_updated_label2

Reg. 0xA003A020

Median of pkWidth for label2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkwidth_median_updated_label2 | ro | wo | X | Median of pkWidth for label2 |

### 1.4.526 clustering_dcm_diag_pkwidth_std_updated_label2

Reg. 0xA003A024

std of pkWidth for label2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkwidth_std_updated_label2 | ro | wo | X | std of pkWidth for label2 |

### 1.4.527 clustering_dcm_diag_pkwidth_median_updated_label3

Reg. 0xA003A028

Median of pkWidth for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkwidth_median_updated_label3 | ro | wo | X | Median of pkWidth for label3 |

### 1.4.528 clustering_dcm_diag_pkwidth_std_updated_label3

Reg. 0xA003A02C

std of pkWidth for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkwidth_std_updated_label3 | ro | wo | X | std of pkWidth for label3 |

### 1.4.529 clustering_dcm_diag_satrate_dcm_small

Reg. 0xA003A030

the rate for small (breakup) droplets shall be used as one of the criteria for square uptime acceptance / rejection

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_satrate_dcm_small | ro | wo | X | the rate for small (breakup) droplets shall be used as one of the criteria for square uptime acceptance / rejection |

### 1.4.530 clustering_dcm_diag_noise_level_updated_std

Reg. 0xA003A034

Updated noise level (at output of clustering algo)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_noise_level_updated_std | ro | wo | X | Updated noise level (at output of clustering algo) |

### 1.4.531 clustering_dcm_diag_jitter_dcm_main

Reg. 0xA003A038

Sigma of XInt

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_jitter_dcm_main | ro | wo | X | Sigma of XInt |

### 1.4.532 clustering_dcm_diag_jitter_dcm_subcl_a

Reg. 0xA003A03C

std of A

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_jitter_dcm_subcl_a | ro | wo | X | std of A |

### 1.4.533 clustering_dcm_diag_jitter_dcm_presubcl

Reg. 0xA003A040

std of C

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_jitter_dcm_presubcl | ro | wo | X | std of C |

### 1.4.534 clustering_dcm_diag_pksaturaterate

Reg. 0xA003A044

Peak saturation rate for main droplets. Saturation is defined as if peak amplitude of main droplet exceed THR.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pksaturaterate | ro | wo | X | Peak saturation rate for main droplets. Saturation is defined as if peak amplitude of main droplet exceed THR. |

### 1.4.535 clustering_dcm_diag_pkoscilevel

Reg. 0xA003A048

Peak oscillation level for main droplets, i.e. std of the peak amplitude for main droplets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkoscilevel | ro | wo | X | Peak oscillation level for main droplets, i.e. std of the peak amplitude for main droplets. |

### 1.4.536 clustering_dcm_diag_siglevel_presubcl

Reg. 0xA003A04C

Signal level for main / subCL / preSubCL droplets

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_siglevel_presubcl | ro | wo | X | Signal level for main / subCL / preSubCL droplets |

### 1.4.537 clustering_dcm_diag_bl_mean

Reg. 0xA003A050

Baseline mean

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_bl_mean | ro | wo | X | Baseline mean |

### 1.4.538 clustering_dcm_diag_pkval_median_updated_label1

Reg. 0xA003A054

Median of PkVal for label1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkval_median_updated_label1 | ro | wo | X | Median of PkVal for label1 |

### 1.4.539 clustering_dcm_diag_pkwidth_median_updated_label1

Reg. 0xA003A058

Median of pkWidth for label1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkwidth_median_updated_label1 | ro | wo | X | Median of pkWidth for label1 |

### 1.4.540 clustering_dcm_diag_pkwidth_median_updated_label0

Reg. 0xA003A05C

Median of pkWidth for label0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkwidth_median_updated_label0 | ro | wo | X | Median of pkWidth for label0 |

### 1.4.541 clustering_ddm_diag_bl_mean

Reg. 0xA003A060

Baseline mean

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_bl_mean | ro | wo | X | Baseline mean |

### 1.4.542 clustering_ddm_diag_pkval_median_updated_label3

Reg. 0xA003A064

Median of PkVal for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pkval_median_updated_label3 | ro | wo | X | Median of PkVal for label3 |

### 1.4.543 clustering_ddm_diag_pkval_std_updated_label3

Reg. 0xA003A068

std of PkVal for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pkval_std_updated_label3 | ro | wo | X | std of PkVal for label3 |

### 1.4.544 clustering_ddm_diag_pkwidth_median_updated_label3

Reg. 0xA003A06C

Median of pkWidth for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pkwidth_median_updated_label3 | ro | wo | X | Median of pkWidth for label3 |

### 1.4.545 clustering_ddm_diag_pkwidth_std_updated_label3

Reg. 0xA003A070

std of pkWidth for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pkwidth_std_updated_label3 | ro | wo | X | std of pkWidth for label3 |

### 1.4.546 clustering_ddm_diag_satrate_ddm

Reg. 0xA003A074

Together with cross interval standard derivation, the satellite rate should be used to provide primary focus metrics for current setting to inline tuning module at the monitoring state

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_satrate_ddm | ro | wo | X | Together with cross interval standard derivation, the satellite rate should be used to provide primary focus metrics for current setting to inline tuning module at the monitoring state |

### 1.4.547 clustering_ddm_diag_noise_level_updated_std

Reg. 0xA003A078

Updated noise level (at output of clustering algo)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_noise_level_updated_std | ro | wo | X | Updated noise level (at output of clustering algo) |

### 1.4.548 clustering_ddm_diag_pksaturaterate

Reg. 0xA003A07C

Peak saturation rate for main droplets. Saturation is defined as if peak amplitude of main droplet exceed THR.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pksaturaterate | ro | wo | X | Peak saturation rate for main droplets. Saturation is defined as if peak amplitude of main droplet exceed THR. |

### 1.4.549 clustering_ddm_diag_pkoscilevel

Reg. 0xA003A080

Peak oscillation level for main droplets, i.e. std of the peak amplitude for main droplets.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pkoscilevel | ro | wo | X | Peak oscillation level for main droplets, i.e. std of the peak amplitude for main droplets. |

### 1.4.550 region_10_end_tag

Reg. 0xA003A084

region_10_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_10_end_tag | ro | wo | X | region_10_end_tag |

### 1.4.551 region_12_start_tag

Reg. 0xA003C000

region_12_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_12_start_tag | ro | wo | X | region_12_start_tag |

### 1.4.552 region_12_dtec_tod_lsbs

Reg. 0xA003C004

region_12_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_12_dtec_tod_lsbs | ro | wo | X | region_12_dtec_tod_lsbs |

### 1.4.553 region_12_dtec_tod_msbs

Reg. 0xA003C008

region_12_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_12_dtec_tod_msbs | ro | wo | X | region_12_dtec_tod_msbs |

### 1.4.554 region_12_dtec_lts

Reg. 0xA003C00C

region_12_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_12_dtec_lts | ro | wo | X | region_12_dtec_lts |

### 1.4.555 idcb_triggers_idcb_trigger_ch1

Reg. 0xA003C010

IDCB trigger for ch1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | idcb_triggers_idcb_trigger_ch1 | ro | wo | X | IDCB trigger for ch1 |

### 1.4.556 idcb_triggers_idcb_trigger_ch2

Reg. 0xA003C014

IDCB trigger for ch2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | idcb_triggers_idcb_trigger_ch2 | ro | wo | X | IDCB trigger for ch2 |

### 1.4.557 idcb_triggers_idcb_trigger_ch7

Reg. 0xA003C018

IDCB trigger for ch7

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | idcb_triggers_idcb_trigger_ch7 | ro | wo | X | IDCB trigger for ch7 |

### 1.4.558 idcb_triggers_idcb_trigger_ch9

Reg. 0xA003C01C

IDCB trigger for ch9

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | idcb_triggers_idcb_trigger_ch9 | ro | wo | X | IDCB trigger for ch9 |

### 1.4.559 idcb_triggers_idcb_trigger_ch10

Reg. 0xA003C020

IDCB trigger for ch10

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | idcb_triggers_idcb_trigger_ch10 | ro | wo | X | IDCB trigger for ch10 |

### 1.4.560 idcb_triggers_idcb_trigger_ch12

Reg. 0xA003C024

IDCB trigger for ch12

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | idcb_triggers_idcb_trigger_ch12 | ro | wo | X | IDCB trigger for ch12 |

### 1.4.561 region_12_end_tag

Reg. 0xA003C028

region_12_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_12_end_tag | ro | wo | X | region_12_end_tag |

### 1.4.562 region_13_start_tag

Reg. 0xA003D000

region_13_start_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_13_start_tag | ro | wo | X | region_13_start_tag |

### 1.4.563 region_13_dtec_tod_lsbs

Reg. 0xA003D004

region_13_dtec_tod_lsbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_13_dtec_tod_lsbs | ro | wo | X | region_13_dtec_tod_lsbs |

### 1.4.564 region_13_dtec_tod_msbs

Reg. 0xA003D008

region_13_dtec_tod_msbs

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_13_dtec_tod_msbs | ro | wo | X | region_13_dtec_tod_msbs |

### 1.4.565 region_13_dtec_lts

Reg. 0xA003D00C

region_13_dtec_lts

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_13_dtec_lts | ro | wo | X | region_13_dtec_lts |

### 1.4.566 state_duplicate4reg13

Reg. 0xA003D010

Readback of diagnostics signature for monitor algo block

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | state_duplicate4reg13 | ro | wo | X | Readback of diagnostics signature for monitor algo block |

### 1.4.567 cal_lf_basedropsetting

Reg. 0xA003D014

Setting being tested during Base Droplet Optimization

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_basedropsetting | ro | wo | X | Setting being tested during Base Droplet Optimization |

### 1.4.568 cal_lf_basedropiteration

Reg. 0xA003D018

Iteration of current Setting being tested during Base Droplet Optimization

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_basedropiteration | ro | wo | X | Iteration of current Setting being tested during Base Droplet Optimization |

### 1.4.569 cal_lf_costfuncoptsetting

Reg. 0xA003D01C

Setting being tested during Cost Function Optimization

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_costfuncoptsetting | ro | wo | X | Setting being tested during Cost Function Optimization |

### 1.4.570 cal_lf_costfunciteration

Reg. 0xA003D020

Iteration of current Setting being tested during Cost Function optimization

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_costfunciteration | ro | wo | X | Iteration of current Setting being tested during Cost Function optimization |

### 1.4.571 cal_lf_stateupdate

Reg. 0xA003D024

Flag that indicates when a calibration state is done

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_stateupdate | ro | wo | X | Flag that indicates when a calibration state is done |

### 1.4.572 cal_lf_spare5

Reg. 0xA003D028

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_spare5 | ro | wo | X | Calibration Spare Signal |

### 1.4.573 cal_lf_spare6

Reg. 0xA003D02C

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_spare6 | ro | wo | X | Calibration Spare Signal |

### 1.4.574 cal_lf_spare7

Reg. 0xA003D030

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_spare7 | ro | wo | X | Calibration Spare Signal |

### 1.4.575 cal_lf_spare8

Reg. 0xA003D034

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_spare8 | ro | wo | X | Calibration Spare Signal |

### 1.4.576 cal_lf_spare9

Reg. 0xA003D038

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_lf_spare9 | ro | wo | X | Calibration Spare Signal |

### 1.4.577 cal_hf_du

Reg. 0xA003D03C

Sine fit signal DU

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_du | ro | wo | X | Sine fit signal DU |

### 1.4.578 cal_hf_alpha1

Reg. 0xA003D040

Sine Fit metrics alpha1

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_alpha1 | ro | wo | X | Sine Fit metrics alpha1 |

### 1.4.579 cal_hf_alpha2

Reg. 0xA003D044

Sine fit metrics alpha2

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_alpha2 | ro | wo | X | Sine fit metrics alpha2 |

### 1.4.580 cal_hf_alpha0

Reg. 0xA003D048

Sine Fit signal alpha0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_alpha0 | ro | wo | X | Sine Fit signal alpha0 |

### 1.4.581 cal_hf_beta

Reg. 0xA003D04C

sine fit signal beta

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_beta | ro | wo | X | sine fit signal beta |

### 1.4.582 cal_hf_clockcorrectionfactor

Reg. 0xA003D050

SineFit Algo clockCorrectionFactor

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_clockcorrectionfactor | ro | wo | X | SineFit Algo clockCorrectionFactor |

### 1.4.583 cal_hf_spare1

Reg. 0xA003D054

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_spare1 | ro | wo | X | Calibration Spare Signal |

### 1.4.584 cal_hf_spare2

Reg. 0xA003D058

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_spare2 | ro | wo | X | Calibration Spare Signal |

### 1.4.585 cal_hf_spare3

Reg. 0xA003D05C

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_spare3 | ro | wo | X | Calibration Spare Signal |

### 1.4.586 cal_hf_spare4

Reg. 0xA003D060

Calibration Spare Signal

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | cal_hf_spare4 | ro | wo | X | Calibration Spare Signal |

### 1.4.587 clustering_dcm_diag_pkval_median_updated_label3_duplicate4reg13

Reg. 0xA003D064

Median of PkVal for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkval_median_updated_label3_duplicate4reg13 | ro | wo | X | Median of PkVal for label3 |

### 1.4.588 clustering_dcm_diag_pkwidth_median_updated_label3_duplicate4reg13

Reg. 0xA003D068

Median of pkWidth for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_pkwidth_median_updated_label3_duplicate4reg13 | ro | wo | X | Median of pkWidth for label3 |

### 1.4.589 clustering_dcm_diag_noise_level_updated_std_duplicate4reg13

Reg. 0xA003D06C

Updated noise level (at output of clustering algo)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_dcm_diag_noise_level_updated_std_duplicate4reg13 | ro | wo | X | Updated noise level (at output of clustering algo) |

### 1.4.590 clustering_ddm_diag_pkval_median_updated_label3_duplicate4reg13

Reg. 0xA003D070

Median of PkVal for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pkval_median_updated_label3_duplicate4reg13 | ro | wo | X | Median of PkVal for label3 |

### 1.4.591 clustering_ddm_diag_pkwidth_median_updated_label3_duplicate4reg13

Reg. 0xA003D074

Median of pkWidth for label3

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_pkwidth_median_updated_label3_duplicate4reg13 | ro | wo | X | Median of pkWidth for label3 |

### 1.4.592 clustering_ddm_diag_noise_level_updated_std_duplicate4reg13

Reg. 0xA003D078

Updated noise level (at output of clustering algo)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | clustering_ddm_diag_noise_level_updated_std_duplicate4reg13 | ro | wo | X | Updated noise level (at output of clustering algo) |

### 1.4.593 region_13_end_tag

Reg. 0xA003D07C

region_13_end_tag

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | region_13_end_tag | ro | wo | X | region_13_end_tag |

### 1.5 algo_csr_registers_srdl

Block 0xA0050000 - 0xA0050173

Register map of the Algo Control and Status registers

### 1.5.1 algo_csr_module_name

Reg. 0xA0050000

Defines the module name

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | module_name | ro | na | 0x616C6749 | ASCII code for module name - top module(core) = core |

### 1.5.2 algo_csr_module_version

Reg. 0xA0050004

Module version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:16 | rfu | ro | na | 0x521 | Algo IO Date |
| 15:8 | major_revision | ro | na | 0x3 | Memory Map number - Decimal - Thousands/Hundreds |
| 7:0 | minor_revision | ro | na | 0x20 | Memoru Mao number - Decimal - Tens/Ones |

### 1.5.3 algo_csr_page_properties

Reg. 0xA0050008

Address page properties

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | present | ro | wo | 0x1 | Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not. |
| 30:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | page_size | ro | na | 0x1 | Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enetr here. |
| 7:0 | unified_header_rev | ro | na | 0x1 | Unified Header Format common registers revision. |

### 1.5.4 algo_csr_scratchregister

Reg. 0xA005000C

Scratchregister register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchregister | rw | na | 0x12345678 | SW can write to it and read from it for test purposes. |

### 1.5.5 algo_csr_irq_enable

Reg. 0xA0050010

Interrupt Requests Enable/Mask Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_enable | rw | ro | 0x0 | IRQ0 enable bit. Not implemented here/DTEC |
| 1 | irq1_enable | rw | ro | 0x0 | IRQ1 enable bit. Not implemented here/DTEC |

### 1.5.6 algo_csr_irq_pending

Reg. 0xA0050014

Interrupt Pending Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_pending | r/w1c | wo | 0x0 | IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |
| 1 | irq1_pending | r/w1c | wo | 0x0 | IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |

### 1.5.7 algo_csr_irq_raw

Reg. 0xA0050018

Interrupt Raw Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_raw | ro | wo | 0x0 | IRQ0 raw status bit. Not implemented here/DTEC |
| 1 | irq1_raw | ro | wo | 0x0 | IRQ1 raw status bit. Not implemented here/DTEC |

### 1.5.8 algo_csr_irq_force

Reg. 0xA005001C

Interrupt Force Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC |
| 1 | irq1_force | rw | ro | 0x0 | IRQ1 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC |

### 1.5.9 dcm_status_reg

Reg. 0xA0050020

Algo Buffer Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | status_reg | ro | wo | 0x0 | [31:4]: unused<br>[3]: CRC Error<br>[2]: FIFO Not Ready<br>[1]: FSM Watchdog<br>[0]: Packet Length Error |

### 1.5.10 ddm_status_reg

Reg. 0xA0050024

Algo Buffer Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | status_reg | ro | wo | 0x0 | [31:4]: unused<br>[3]: CRC Error<br>[2]: FIFO Not Ready<br>[1]: FSM Watchdog<br>[0]: Packet Length Error |

### 1.5.11 ch3_xfer_count

Reg. 0xA0050100

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.12 ch3_drop_count

Reg. 0xA0050104

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.13 ch4_xfer_count

Reg. 0xA0050108

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.14 ch4_drop_count

Reg. 0xA005010C

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.15 ch5_xfer_count

Reg. 0xA0050110

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.16 ch5_drop_count

Reg. 0xA0050114

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.17 ch6_xfer_count

Reg. 0xA0050118

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.18 ch6_drop_count

Reg. 0xA005011C

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.19 ch7_xfer_count

Reg. 0xA0050120

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.20 ch7_drop_count

Reg. 0xA0050124

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.21 ch8_xfer_count

Reg. 0xA0050128

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.22 ch8_drop_count

Reg. 0xA005012C

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.23 ch9_xfer_count

Reg. 0xA0050130

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.24 ch9_drop_count

Reg. 0xA0050134

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.25 ch10_xfer_count

Reg. 0xA0050138

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.26 ch10_drop_count

Reg. 0xA005013C

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.27 ch12_xfer_count

Reg. 0xA0050140

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.28 ch12_drop_count

Reg. 0xA0050144

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.29 algo_to_damp_xfer_count

Reg. 0xA0050150

Count of how many sets of DMA data have been loaded into the FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.30 algo_to_damp_drop_count

Reg. 0xA0050154

Count of how many sets of DMA data have been dropped due to non-empty FIFO

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | counter | ro | wo | 0x0 | Count |

### 1.5.31 dcm_pkts_inframe_cnt

Reg. 0xA0050158

register used to return the count of number of packets in 1msec time frame

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rx_cnt | ro | wo | 0x0 | gives the count every 1msec |

### 1.5.32 dcm_pkts_crc_err_cnt

Reg. 0xA005015C

register used to return the count of number of crc error packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected an crc error packet |

### 1.5.33 dcm_pkts_lgth_err_cnt

Reg. 0xA0050160

register used to return the count of number of packets received with packet length error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a packet with unexpected length |

### 1.5.34 ddm_pkts_inframe_cnt

Reg. 0xA0050164

register used to return the count of number of packets in 1msec time frame

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rx_cnt | ro | wo | 0x0 | gives the count every 1msec |

### 1.5.35 ddm_pkts_crc_err_cnt

Reg. 0xA0050168

register used to return the count of number of crc error packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected an crc error packet |

### 1.5.36 ddm_pkts_lgth_err_cnt

Reg. 0xA005016C

register used to return the count of number of packets received with packet length error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a packet with unexpected length |

### 1.5.37 pulse_1ms_phase_delay

Reg. 0xA0050170

Phase delay the 1ms algo pulse (used for 1ms clock enable, cluster_start, channel 12 dma capture, etc).

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | ro | 0x100 | Number of clocks (in 125 MHz core clock domain) to phase delay the 1ms algo pulse.<br>The algo team informed that the max time that the algo takes should be ~240 clock cycles. |

## 1.6 tsel_if_bridge_srdl

Block 0xA0080000 - 0xA00867FF

Registers used to configure / control tsel interface

### 1.6.1 MODULE_NAME

Reg. 0xA0080000

Module info register 0 - used to return module name. This register can be used for automated module discovery and to ensure
we are on the expected page in memory

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | data | ro | na | 0x52363335 | ASCII Module name (TSEl Wrapper) - TSEW |

### 1.6.2 MODULE_VERSION

Reg. 0xA0080004

Module info register 1 - used to return module version.
Note: this register might change from build to build and might be used for future backwards compatibility

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:8 | major | ro | wo | 0x0 | Module version major |

| | | | | | |
|---|---|---|---|---|---|
| 7:0 | minor | ro | wo | 0x0 | Module version minor |

### 1.6.3 HEADER_INFO

Reg. 0xA0080008

Module info register 2 - used to return module memory page size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | block_size | ro | na | 0x4 | Addressable address space in 4k pages (1 = 4096 bytes / 2 = 8192 ...) |
| 31:16 | unified_header_ver | ro | na | 0x0 | Version of unified module memory header - used for any future changes to the header |

### 1.6.4 SCRATCHPAD

Reg. 0xA008000C

Module info register 3 - scratchpad register used for testing module read / write access.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchpad | rw | na | 0x0 | scratchpad register - can be read and written by software at any time |

### 1.6.5 IRQ_ENABLE

Reg. 0xA0080010

Register used to enable individual IRQs. If defined bit is set and interrupt occurs, interrupt pin will toggle, otherwise IRQ pin will not change.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full | rw | na | 0x0 | IRQ enable - cpu insert buffer full. |
| 1 | cpu_insert_buffer_fifo_empty | rw | na | 0x0 | IRQ enable - cpu insert buffer empty. |
| 2 | cpu_capture_buffer_pkt_avail | rw | na | 0x0 | IRQ enable - cpu capture buffer pkt available. |
| 3 | cpu_capture_buffer_overflow | rw | na | 0x0 | IRQ enable - cpu capture buffer overflow. |
| 4 | link_up | rw | na | 0x0 | IRQ enable - link up. |
| 5 | link_down | rw | na | 0x0 | IRQ enable - link down. |

### 1.6.6 IRQ_PENDING

Reg. 0xA0080014

Register used to return currently pending IRQs.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full | r/w1c | wo | 0x0 | IRQ pending - cpu insert buffer full indication. TBD - do we want this level sensitive? |
| 1 | cpu_insert_buffer_fifo_empty | r/w1c | wo | 0x0 | IRQ pending - cpu insert buffer empty indication. TBD - do we want this level sensitive? |
| 2 | cpu_capture_buffer_pkt_avail | r/w1c | wo | 0x0 | IRQ pending - cpu capture buffer pkt available. |
| 3 | cpu_capture_buffer_overflow | r/w1c | wo | 0x0 | IRQ pending - cpu capture buffer overflow (capture buffer full) |
| 4 | link_up | r/w1c | wo | 0x0 | IRQ pending - link up |
| 5 | link_down | r/w1c | wo | 0x0 | IRQ pending - link down |

### 1.6.7 IRQ_RAW

Reg. 0xA0080018

Register used to return current value of IRQ input signals

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full | ro | wo | 0x0 | current value of - cpu insert buffer full indication. |
| 1 | cpu_insert_buffer_fifo_empty | ro | wo | 0x0 | current value of - cpu insert buffer empty indication. |
| 2 | cpu_capture_buffer_pkt_avail | ro | wo | 0x0 | current value of - cpu capture buffer pkt available. |

| | | | | | |
|---|---|---|---|---|---|
| 3 | cpu_capture_buffer_overflow | ro | wo | 0x0 | current value of - cpu_capture_buffer_overflow. |
| 4 | link_up | ro | wo | 0x0 | current value of - link status (0 = down / 1 = up). |
| 5 | link_down | ro | wo | 0x0 | current value of - link status (0 = down / 1 = up). |

### 1.6.8 IRQ_FORCE

Reg. 0xA008001C

Register used to force interrupts via software - this register is to be used for debugging interrupts only. Important, if the user goes and
manually forces an interrupt via any fields in this register (by setting a field to 1), the IRQ routine needs to clear the forced field otherwise the interrupt
will never clear and we will be stuck in an interrupt loop. Additionally, forcing an interrupt that is not enabled, will not result in interrupt pin being toggled.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full_force | rw | na | 0x0 | register used to force IRQ-cpu_insert_buffer_fifo_full_force. |
| 1 | cpu_insert_buffer_fifo_empty_force | rw | na | 0x0 | register used to force IRQ-cpu_insert_buffer_fifo_empty. |
| 2 | cpu_capture_buffer_pkt_avail_force | rw | na | 0x0 | register used to force IRQ-cpu_capture_buffer_pkt_avail. |
| 3 | cpu_capture_buffer_overflow_force | rw | na | 0x0 | register used to force IRQ-cpu_capture_buffer_overflow. |
| 4 | link_up_force | rw | na | 0x0 | register used to force IRQ-link_up |
| 5 | link_down_force | rw | na | 0x0 | register used to force IRQ-link_down |

### 1.6.9 BUILD_INFO

Reg. 0xA0080040

register used to return TSEL GDB info

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | build_type | ro | wo | 0x0 | TSEL build type: 0 = tsel client / 1 = tsel bridge / others - reserved |
| 15:8 | tsel_index | ro | wo | 0x0 | TSEL index - used to confirm memory map to tsel client / bridge instance number |

### 1.6.10 BUILD_INFO1

Reg. 0xA0080044

register used to return TSEL Unified build info

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | rx_stats_engine_size | ro | wo | 0x0 | number of entries used in rx stats engine. Only use rx_stats_engine if this field > 0 |
| 31:16 | tx_stats_engine_size | ro | wo | 0x0 | number of entries used in tx stats engine. Only use tx_stats_engine if this field > 0 |

### 1.6.11 BUILD_INFO2

Reg. 0xA0080048

register used to return TSEL Unified build info

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | cpu_buf_addr_width | ro | wo | 0x0 | address size of each CPU buffer; CPU buffer word size is 2^cpu_buf_addr_width |
| 15:8 | cpu_buf_depth | ro | wo | 0x0 | number of buffers in CPU packet FIFO |
| 16 | stats_bin_type | ro | wo | 0x0 | source used for stats binning, RX/TX_STATS_ENGINE; 0 - payload type, 1 - header type |

### 1.6.12 TSEL_CTRL

Reg. 0xA0080060

register used to control tsel gdb

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | reset_force | rw | ro | 0x0 | field used to allow software ability to reset tsel GDB. 1=gdb reset / 0= gdb not reset |
| 4 | tsel_client_mac_address_valid | rw | ro | 0x0 | field used to allow software ability to change mac address, client only. TBD - this might have to be set before core is being reset |
| 5 | tsel_client_eth_type_valid | rw | ro | 0x0 | field used to allow software ability to change ethernet type. TBD - this might have to be set before core is being reset |

### 1.6.13 TSEL_CLIENT_TX_MAC_INSERT_MSB

Reg. 0xA0080064

register used to control tsel gdb mac address insertion on the way out, client only

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | msb | rw | ro | 0x1234 | register used to assign mac address when external prom is not being used - bits [47:32] |

### 1.6.14 TSEL_CLIENT_TX_MAC_INSERT_LSB

Reg. 0xA0080068

register used to control tsel gdb mac address insertion on the way out, client only

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lsb | rw | ro | 0x56789ABC | register used to assign mac address when external prom is not being used - bits [31:0] |

### 1.6.15 TSEL_CLIENT_TX_ETH_TYPE

Reg. 0xA008006C

register used to control tsel gdb ethernet type on the way out

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | insert | rw | ro | 0x8000 | register used to assign ethernet type |

### 1.6.16 TSEL_CLIENT_RX_SRC_MAC_MSB

Reg. 0xA0080070

register used to return last packet src mac address (MSB).
Reading this register latches value in tsel_client_rx_mac_insert_lsb and tsel_client_rx_eth_type

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | msb | ro | wo | 0x0 | src mac address - bits [47:32] |

### 1.6.17 TSEL_CLIENT_RX_SRC_MAC_LSB

Reg. 0xA0080074

register used to return last packet src mac address (LSB)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lsb | ro | wo | 0x0 | src mac address - bits [31:0] |

### 1.6.18 TSEL_CLIENT_RX_SRC_ETH_TYPE

Reg. 0xA0080078

register used to return last packet ethernet type - this register is for Client TSEL GDB only

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | received | ro | wo | 0x0 | register used to assign ethernet type |

### 1.6.19 CPU_INSERT_BUFFER_CTRL

Reg. 0xA0080080

register used to control insert buffer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | fifo_push | rw | ro | 0x0 | write 1 to perform insert buffer push |

### 1.6.20 CPU_CAPTURE_BUFFER_CTRL

Reg. 0xA0080084

cpu capture buffer control register.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 1 | fifo_pop | rw | ro | 0x0 | write 1 to perform capture buffer fifo pop |

### 1.6.21 CPU_CAPTURE_BUFFER_CTRL2

Reg. 0xA0080088

cpu capture buffer control register 2.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | en | rw | ro | 0x0 | packet capture enable. 1 = enabled / 0 = disabled. |
| 1 | capture_src_ctrl | rw | ro | 0x0 | packet capture src enable. 1 = capture data from TX path / 0 = capture data from RX path. |
| 5:4 | capture_mode | rw | ro | 0x0 | packet capture mode.<br>00: capture first packets received<br>01: capture first packets with pkt_type match<br>10: capture first pacekts with pkt_typt and header_type match<br>11: reserved. |
| 23:8 | capture_pkt_type | rw | ro | 0x0 | packet capture type (used in mode 01 and 10) |
| 31:24 | capture_header_type | rw | ro | 0x0 | packet capture header type (used in mode 10) |

### 1.6.22 TSEL_GDB_STATUS

Reg. 0xA00800A0

register used to return tsel GDB status.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tsel_link_status | ro | wo | 0x0 | tsel gdb link status (active high) |
| 1 | diag_enable | ro | wo | 0x0 | diag_enable --> signal from GDB. |
| 2 | wdog_failure | ro | wo | 0x0 | sfp tsel_wdog_failure --> driven by GDB |
| 8 | tsel_led_red | ro | wo | 0x0 | led red - on and yellow=off and green=off => Power-on, or TSEL GDB detects errors that shall lead to board replacement |
| 9 | tsel_led_yellow | ro | wo | 0x0 | led yellow - on and red=off and green=off => TSEL GDB detect issues on the link (link loss, remote fault) |
| 10 | tsel_led_green | ro | wo | 0x0 | led green - on and yellow=off and red=off => TSEL GDB is initialized, link is up and communication with partner is working fine |
| 12 | sfp_present_n | ro | wo | 0x0 | sfp present_n --> active low |
| 13 | sfp_tx_fault | ro | wo | 0x0 | sfp sfp_tx_fault --> signal from SFP transceiver. |
| 14 | sfp_rx_los | ro | wo | 0x0 | sfp rx los --> signal from SFP transceiver. |
| 15 | sfp_tx_disable | ro | wo | 0x0 | sfp sfp_tx_disable --> signal from SFP transceiver. |
| 16 | led_tsel_if_red | ro | wo | 0x0 | tsel instance specific led red - on and yellow=off and green=off => Power-on, or TSEL client detects errors that shall lead to board replacement |
| 17 | led_tsel_if_yellow | ro | wo | 0x0 | tsel instance specific led yellow - on and red=off and green=off => TSEL client detect issues on the link (link loss, remote fault) |
| 18 | led_tsel_if_green | ro | wo | 0x0 | tsel instance specific led green - on and yellow=off and red=off => TSEL client is initialized, link is up and communication with host is working fine |

### 1.6.23 TSEL_DEBUG_CTRL

Reg. 0xA00800A4

register used to change default data flow

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 0 | tx_pkt_loopback | rw | ro | 0x0 | register used to route tsel TX path to RX. This is a debug feature that allows for stand alone testing where CPU packet inserter can be used drive RX data path. 0=default tx path. 1=tx_packets are looped back to rx |
| 1 | rx_pkt_loopback | rw | ro | 0x0 | register used to route tsel RX path to TX. This is a debug feature that allows for testing TSEL GDB packet loopback. 0=default tx path. 1=rx_packets are looped back to tx |

### 1.6.24 TSEL_DEBUG_CTRL2

Reg. 0xA00800A8

register used to change internal parameters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | interpacket_gap | rw | ro | 0x20 | change min spacing between packets. DO NOT TOUCH UNLESS YOU KNOW WHAT YOU ARE DOING! |

### 1.6.25 DEBUG

Reg. 0xA00800AC

reserved

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ctrl | rw | ro | 0x0 | connects to general-purpose module output port |

### 1.6.26 DEBUG_LINK_UP_OVERWRITE

Reg. 0xA00800B0

register used to overwrite link status - allows to fake out a connection that tsel is connected to a partner.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | data | rw | ro | 0x0 | debug feature only - do not use unless you know what you are doing! |

### 1.6.27 TSEL_CLK_FREQ

Reg. 0xA00800B4

frequency of recovered clock, TSEL GTH

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | val | ro | wo | 0x0 | frequency reading (Hz) |

### 1.6.28 TSEL_DEBUG_IF_SUPPRESS

Reg. 0xA00800B8

register used to suppress interface activity, debug feature

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | disable_if_gmii_tx | rw | ro | 0x0 | set to disable output TX GMII I/F to GDB, silently discards TX packets |
| 1 | disable_if_gmii_rx | rw | ro | 0x0 | set to disable input RX GMII I/F from GDB, silently discards packet at RX input |
| 2 | disable_if_axis_rx | rw | ro | 0x0 | set to disable output RX AXI-S I/F, silently discards packet at RX output |
| 23:8 | disable_if_axis_tx | rw | ro | 0x0 | set to disable selected TX AXI-S I/F source input (bit[8]=>src0, bit[9]=>src1, etc), holds TREADY low |

### 1.6.29 RX_STATS_ENGINE_CTRL

Reg. 0xA00800C0

register used to control stats engine.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | table_clear | rw | ro | 0x0 | write 1 to perform stats engine table clear |

### 1.6.30 RX_STATS_ENGINE_STATUS

Reg. 0xA00800C4

register used to return stats engine state

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | busy | ro | wo | 0x0 | table_not_ready - when 1, stats table is busy (being cleared). Do not read stats engine until zero |
| 1 | oor | ro | wo | 0x0 | out of range entry detected - when 1 it indicates stats engine was too small to capture statistics for input / outout packet type. reset by clearing stats table |
| 31:16 | oor_pkt_type | ro | wo | 0x0 | out of range entry detected - last packet type that was out of range. reset by clearing stats table |

### 1.6.31 TX_STATS_ENGINE_CTRL

Reg. 0xA00800C8

register used to control stats engine.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | table_clear | rw | ro | 0x0 | write 1 to perform stats engine table clear |

### 1.6.32 TX_STATS_ENGINE_STATUS

Reg. 0xA00800CC

register used to return stats engine state

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | busy | ro | wo | 0x0 | table_not_ready - when 1, stats table is busy (being cleared). Do not read stats engine until zero |
| 1 | oor | ro | wo | 0x0 | out of range entry detected - when 1 it indicates stats engine was too small to capture statistics for input / outout packet type. reset by clearing stats table |
| 31:16 | oor_pkt_type | ro | wo | 0x0 | out of range entry detected - last packet type that was out of range. reset by clearing stats table |

### 1.6.33 PACKET_GEN_CTRL0

Reg. 0xA00800E0

register used to control packet generator rate control.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rate_ctrl | rw | ro | 0x0 | rate control to space packets. Rate = 2**33 / value |

### 1.6.34 PACKET_GEN_CTRL1

Reg. 0xA00800E4

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | packet_type | rw | ro | 0x0 | packet generator packet type used in generating traffic. |
| 23:16 | header_type | rw | ro | 0x0 | header type used for packet generation. |

### 1.6.35 PACKET_GEN_CTRL2

Reg. 0xA00800E8

register used to control packet generator.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | enable | rw | ro | 0x0 | enable. 0 = off / 1 = on |
| 1 | mode | rw | ro | 0x0 | packet generator mode. 0 = fixed size (as defined in bits 31:15) / 1 = incremental 46 to 1500, incrementing by 1 on every packet |
| 15:8 | seed | rw | ro | 0x0 | seed used for packet generator. Do not touch unless you know what you are doing |
| 31:16 | packet_length | rw | ro | 0x0 | packet length used in mode 0 packet generator. Must be in range of 46 to 1500 |

### 1.6.36 PACKET_GEN_CHECKER_CTRL0

Reg. 0xA00800EC

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 15:0 | packet_type | rw | ro | 0x0 | packet generator checker packet type used in checking traffic. |
| 23:16 | header_type | rw | ro | 0x0 | header type used for packet checking. |

### 1.6.37 PACKET_GEN_CHECKER_CTRL1

Reg. 0xA00800F0

register used to control generator checker.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | enable | rw | ro | 0x0 | enable. 0 = off / 1 = on |
| 15:8 | seed | rw | ro | 0x0 | seed used for packet generator. Do not touch unless you know what you are doing |

### 1.6.38 PKT_COUNT_RX_TOTAL

Reg. 0xA0080100

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.39 BYTE_COUNT_RX_TOTAL

Reg. 0xA0080104

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.40 PKT_COUNT_RX_FCS_ERROR

Reg. 0xA0080108

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.41 BYTE_COUNT_RXTX_LPBK_ERROR

Reg. 0xA008010C

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.42 PKT_COUNT_TX_TOTAL

Reg. 0xA0080120

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.43 BYTE_COUNT_TX_TOTAL

Reg. 0xA0080124

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.44 PKT_COUNT_TX_BUS_ERROR

Reg. 0xA0080128

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.45 PKT_COUNT_TX_DATA_ERROR

Reg. 0xA008012C

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.46 PKT_COUNT_TX_TOO_SHORT_ERROR

Reg. 0xA0080130

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.47 PKT_COUNT_TX_TOO_LONG_ERROR

Reg. 0xA0080134

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.48 CPU_INSERT_BUFFER_CNT

Reg. 0xA0080140

register used to return insert buffer counters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | success | rw | na | 0x0 | successful packet insertion counter |

### 1.6.49 CPU_CAPTURE_BUFFER_CNT

Reg. 0xA0080144

register used to return capture buffer counters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | success | rw | na | 0x0 | successful packet capture counter |

### 1.6.50 CPU_CAPTURE_BUFFER_CNT1

Reg. 0xA0080148

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | overflow | rw | na | 0x0 | number of packets not captured due to CPU capture buffer being full. |

### 1.6.51 LINK_DOWN_COUNT

Reg. 0xA0080150

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.6.52 PACKET_GEN_STATUS0

Reg. 0xA0080180

register used to return packet generator info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | pkt_count | ro | wo | 0x0 | number of packets inserted by the packet generator |

### 1.6.53 PACKET_GEN_CHECKER_STATUS0

Reg. 0xA0080184

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | pkt_count | ro | wo | 0x0 | number of packets checked |

### 1.6.54 PACKET_GEN_STATUS1

Reg. 0xA0080188

register used to return packet generator info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bytes_count | ro | wo | 0x0 | number of bytes inserted by the packet generator |

### 1.6.55 PACKET_GEN_CHECKER_STATUS1

Reg. 0xA008018C

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bytes_count | ro | wo | 0x0 | number of bytes checked by the packet generator |

### 1.6.56 PACKET_GEN_CHECKER_STATUS2

Reg. 0xA0080190

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | pkt_errors | ro | wo | 0x0 | number of packets with errors |

### 1.6.57 PACKET_GEN_CHECKER_STATUS3

Reg. 0xA0080194

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | byte_errors | ro | wo | 0x0 | number of bytes with errors |

### 1.6.58 PACKET_GEN_CHECKER_STATUS4

Reg. 0xA0080198

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | length_errors | ro | wo | 0x0 | number of packets with length errors |

### 1.6.59 PACKET_GEN_CHECKER_STATUS5

Reg. 0xA008019C

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | sequence_errors | ro | wo | 0x0 | number of packets with sequnce errors |

### 1.6.60 CPU_INSERT_BUFFER

CPU_INSERT_BUFFER 0xA0081000, 0xA0081004 ... 0xA00817FF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to insert packets into TSEL GDB. This memory is implemented as a 4 packet FIFO that allows CPU to insert packets between 1 and 2044 bytes. Important: it is CPU responsibility to ensure inserted packet is in the correct format (i.e. ethernet packet) The following steps are to be performed in order for CPU to insert a packets: 1) check that insert packet FIFO is not full FIFO by reading IRQ_RAW->cpu_insert_buffer_fifo_full = 0 (not full). 2) write insertion length in bytes (between 1-2044) to insert buffer entry [0] 3) write insertion data (between 1-2044 bytes) to insert buffer entries [1:511] 4) issue FIFO push by writting 1 to CPU_INSERT_BUFFER_CTRL->fifo_push. Packet will be inserted as soon as bus access is granted.

### 1.6.61 CPU_CAPTURE_BUFFER

CPU_CAPTURE_BUFFER 0xA0081800, 0xA0081804 ... 0xA0081FFF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to capture packets from TSEL GDB. The capture buffer is implemented as a 4 packet FIFO that allows CPU capture packets between 1 and 2044 bytes in length. The following steps are to be performed in order for CPU to capture packets: 1) set capture filter (TBD - not implemented yet) and enable capture engine CPU_INSERT_BUFFER_CTRL->en = 1 2) wait for packet by reading IRQ_RAW-cpu_capture_buffer_pkt_avail = 1 (or set up interrupt) 3) read capture buffer entry [0]. This entry holds the length of the captured packet in range of 1-2044 bytes 4) read captured data (between 1-2044 bytes form step 3) from capture buffer entries [1:511] 5) issue capture buffer FIFO pop by writting 1 to CPU_INSERT_BUFFER_CTRL->cpu_capture_buffer_ctrl.

### 1.6.62 RX_STATS_ENGINE

RX_STATS_ENGINE 0xA0084000, 0xA0084004 ... 0xA00847FF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

### 1.6.63 TX_STATS_ENGINE

TX_STATS_ENGINE 0xA0086000, 0xA0086004 ... 0xA00867FF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

## 1.7 tsel_if_client_srdl

Block 0xA0090000 - 0xA00967FF

Registers used to configure / control tsel interface

### 1.7.1 MODULE_NAME

Reg. 0xA0090000

Module info register 0 - used to return module name. This register can be used for automated module discovery and to ensure
we are on the expected page in memory

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | data | ro | na | 0x52363335 | ASCII Module name (TSEl Wrapper) - TSEW |

### 1.7.2 MODULE_VERSION

Reg. 0xA0090004

Module info register 1 - used to return module version.
Note: this register might change from build to build and might be used for future backwards compatibility

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:8 | major | ro | wo | 0x0 | Module version major |
| 7:0 | minor | ro | wo | 0x0 | Module version minor |

### 1.7.3 HEADER_INFO

Reg. 0xA0090008

Module info register 2 - used to return module memory page size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | block_size | ro | na | 0x4 | Addressable address space in 4k pages (1 = 4096 bytes / 2 = 8192 ...) |
| 31:16 | unified_header_ver | ro | na | 0x0 | Version of unified module memory header - used for any future changes to the header |

### 1.7.4 SCRATCHPAD

Reg. 0xA009000C

Module info register 3 - scratchpad register used for testing module read / write access.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchpad | rw | na | 0x0 | scratchpad register - can be read and written by software at any time |

### 1.7.5 IRQ_ENABLE

Reg. 0xA0090010

Register used to enable individual IRQs. If defined bit is set and interrupt occurs, interrupt pin will toggle, otherwise IRQ pin will not change.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full | rw | na | 0x0 | IRQ enable - cpu insert buffer full. |
| 1 | cpu_insert_buffer_fifo_empty | rw | na | 0x0 | IRQ enable - cpu insert buffer empty. |
| 2 | cpu_capture_buffer_pkt_avail | rw | na | 0x0 | IRQ enable - cpu capture buffer pkt available. |
| 3 | cpu_capture_buffer_overflow | rw | na | 0x0 | IRQ enable - cpu capture buffer overflow. |
| 4 | link_up | rw | na | 0x0 | IRQ enable - link up. |
| 5 | link_down | rw | na | 0x0 | IRQ enable - link down. |

### 1.7.6 IRQ_PENDING

Reg. 0xA0090014

Register used to return currently pending IRQs.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full | r/w1c | wo | 0x0 | IRQ pending - cpu insert buffer full indication. TBD - do we want this level sensitive? |
| 1 | cpu_insert_buffer_fifo_empty | r/w1c | wo | 0x0 | IRQ pending - cpu insert buffer empty indication. TBD - do we want this level sensitive? |
| 2 | cpu_capture_buffer_pkt_avail | r/w1c | wo | 0x0 | IRQ pending - cpu capture buffer pkt available. |
| 3 | cpu_capture_buffer_overflow | r/w1c | wo | 0x0 | IRQ pending - cpu capture buffer overflow (capture buffer full) |

| | | | | | |
|---|---|---|---|---|---|
| 4 | link_up | r/w1c | wo | 0x0 | IRQ pending - link up |
| 5 | link_down | r/w1c | wo | 0x0 | IRQ pending - link down |

### 1.7.7 IRQ_RAW

Reg. 0xA0090018

Register used to return current value of IRQ input signals

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full | ro | wo | 0x0 | current value of - cpu insert buffer full indication. |
| 1 | cpu_insert_buffer_fifo_empty | ro | wo | 0x0 | current value of - cpu insert buffer empty indication. |
| 2 | cpu_capture_buffer_pkt_avail | ro | wo | 0x0 | current value of - cpu capture buffer pkt available. |
| 3 | cpu_capture_buffer_overflow | ro | wo | 0x0 | current value of - cpu_capture_buffer_overflow. |
| 4 | link_up | ro | wo | 0x0 | current value of - link status (0 = down / 1 = up). |
| 5 | link_down | ro | wo | 0x0 | current value of - link status (0 = down / 1 = up). |

### 1.7.8 IRQ_FORCE

Reg. 0xA009001C

Register used to force interrupts via software - this register is to be used for debugging interrupts only. Important, if the user goes and
manually forces an interrupt via any fields in this register (by setting a field to 1), the IRQ routine needs to clear the forced field otherwise the interrupt
will never clear and we will be stuck in an interrupt loop. Additionally, forcing an interrupt that is not enabled, will not result in interrupt pin being toggled.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | cpu_insert_buffer_fifo_full_force | rw | na | 0x0 | register used to force IRQ-cpu_insert_buffer_fifo_full_force. |
| 1 | cpu_insert_buffer_fifo_empty_force | rw | na | 0x0 | register used to force IRQ-cpu_insert_buffer_fifo_empty. |
| 2 | cpu_capture_buffer_pkt_avail_force | rw | na | 0x0 | register used to force IRQ-cpu_capture_buffer_pkt_avail. |
| 3 | cpu_capture_buffer_overflow_force | rw | na | 0x0 | register used to force IRQ-cpu_capture_buffer_overflow. |
| 4 | link_up_force | rw | na | 0x0 | register used to force IRQ-link_up |
| 5 | link_down_force | rw | na | 0x0 | register used to force IRQ-link_down |

### 1.7.9 BUILD_INFO

Reg. 0xA0090040

register used to return TSEL GDB info

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | build_type | ro | wo | 0x0 | TSEL build type: 0 = tsel client / 1 = tsel bridge / others - reserved |
| 15:8 | tsel_index | ro | wo | 0x0 | TSEL index - used to confirm memory map to tsel client / bridge instance number |

### 1.7.10 BUILD_INFO1

Reg. 0xA0090044

register used to return TSEL Unified build info

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | rx_stats_engine_size | ro | wo | 0x0 | number of entries used in rx stats engine. Only use rx_stats_engine if this field > 0 |
| 31:16 | tx_stats_engine_size | ro | wo | 0x0 | number of entries used in tx stats engine. Only use tx_stats_engine if this field > 0 |

### 1.7.11 BUILD_INFO2

Reg. 0xA0090048

register used to return TSEL Unified build info

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | cpu_buf_addr_width | ro | wo | 0x0 | address size of each CPU buffer; CPU buffer word size is 2^cpu_buf_addr_width |
| 15:8 | cpu_buf_depth | ro | wo | 0x0 | number of buffers in CPU packet FIFO |
| 16 | stats_bin_type | ro | wo | 0x0 | source used for stats binning, RX/TX_STATS_ENGINE; 0 - payload type, 1 - header type |

### 1.7.12 TSEL_CTRL

Reg. 0xA0090060

register used to control tsel gdb

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | reset_force | rw | ro | 0x0 | field used to allow software ability to reset tsel GDB. 1=gdb reset / 0= gdb not reset |
| 4 | tsel_client_mac_address_valid | rw | ro | 0x0 | field used to allow software ability to change mac address, client only. TBD - this might have to be set before core is being reset |
| 5 | tsel_client_eth_type_valid | rw | ro | 0x0 | field used to allow software ability to change ethernet type. TBD - this might have to be set before core is being reset |

### 1.7.13 TSEL_CLIENT_TX_MAC_INSERT_MSB

Reg. 0xA0090064

register used to control tsel gdb mac address insertion on the way out, client only

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | msb | rw | ro | 0x1234 | register used to assign mac address when external prom is not being used - bits [47:32] |

### 1.7.14 TSEL_CLIENT_TX_MAC_INSERT_LSB

Reg. 0xA0090068

register used to control tsel gdb mac address insertion on the way out, client only

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lsb | rw | ro | 0x56789ABC | register used to assign mac address when external prom is not being used - bits [31:0] |

### 1.7.15 TSEL_CLIENT_TX_ETH_TYPE

Reg. 0xA009006C

register used to control tsel gdb ethernet type on the way out

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | insert | rw | ro | 0x8000 | register used to assign ethernet type |

### 1.7.16 TSEL_CLIENT_RX_SRC_MAC_MSB

Reg. 0xA0090070

register used to return last packet src mac address (MSB).
Reading this register latches value in tsel_client_rx_mac_insert_lsb and tsel_client_rx_eth_type

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | msb | ro | wo | 0x0 | src mac address - bits [47:32] |

### 1.7.17 TSEL_CLIENT_RX_SRC_MAC_LSB

Reg. 0xA0090074

register used to return last packet src mac address (LSB)

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lsb | ro | wo | 0x0 | src mac address - bits [31:0] |

### 1.7.18 TSEL_CLIENT_RX_SRC_ETH_TYPE

Reg. 0xA0090078

register used to return last packet ethernet type - this register is for Client TSEL GDB only

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | received | ro | wo | 0x0 | register used to assign ethernet type |

### 1.7.19 CPU_INSERT_BUFFER_CTRL

Reg. 0xA0090080

register used to control insert buffer

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | fifo_push | rw | ro | 0x0 | write 1 to perform insert buffer push |

### 1.7.20 CPU_CAPTURE_BUFFER_CTRL

Reg. 0xA0090084

cpu capture buffer control register.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 1 | fifo_pop | rw | ro | 0x0 | write 1 to perform capture buffer fifo pop |

### 1.7.21 CPU_CAPTURE_BUFFER_CTRL2

Reg. 0xA0090088

cpu capture buffer control register 2.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | en | rw | ro | 0x0 | packet capture enable. 1 = enabled / 0 = disabled. |
| 1 | capture_src_ctrl | rw | ro | 0x0 | packet capture src enable. 1 = capture data from TX path / 0 = capture data from RX path. |
| 5:4 | capture_mode | rw | ro | 0x0 | packet capture mode.<br>00: capture first packets received<br>01: capture first packets with pkt_type match<br>10: capture first pacekts with pkt_typt and header_type match<br>11: reserved. |
| 23:8 | capture_pkt_type | rw | ro | 0x0 | packet capture type (used in mode 01 and 10) |
| 31:24 | capture_header_type | rw | ro | 0x0 | packet capture header type (used in mode 10) |

### 1.7.22 TSEL_GDB_STATUS

Reg. 0xA00900A0

register used to return tsel GDB status.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tsel_link_status | ro | wo | 0x0 | tsel gdb link status (active high) |
| 1 | diag_enable | ro | wo | 0x0 | diag_enable --> signal from GDB. |
| 2 | wdog_failure | ro | wo | 0x0 | sfp tsel_wdog_failure --> driven by GDB |
| 8 | tsel_led_red | ro | wo | 0x0 | led red - on and yellow=off and green=off => Power-on, or TSEL GDB detects errors that shall lead to board replacement |
| 9 | tsel_led_yellow | ro | wo | 0x0 | led yellow - on and red=off and green=off => TSEL GDB detect issues on the link (link loss, remote fault) |
| 10 | tsel_led_green | ro | wo | 0x0 | led green - on and yellow=off and red=off => TSEL GDB is initialized, link is up and communication with partner is working fine |
| 12 | sfp_present_n | ro | wo | 0x0 | sfp present_n --> active low |
| 13 | sfp_tx_fault | ro | wo | 0x0 | sfp sfp_tx_fault --> signal from SFP transceiver. |
| 14 | sfp_rx_los | ro | wo | 0x0 | sfp rx los --> signal from SFP transceiver. |
| 15 | sfp_tx_disable | ro | wo | 0x0 | sfp sfp_tx_disable --> signal from SFP transceiver. |

| | | | | | |
|---|---|---|---|---|---|
| 16 | led_tsel_if_red | ro | wo | 0x0 | tsel instance specific led red - on and yellow=off and green=off => Power-on, or TSEL client detects errors that shall lead to board replacement |
| 17 | led_tsel_if_yellow | ro | wo | 0x0 | tsel instance specific led yellow - on and red=off and green=off => TSEL client detect issues on the link (link loss, remote fault) |
| 18 | led_tsel_if_green | ro | wo | 0x0 | tsel instance specific led green - on and yellow=off and red=off => TSEL client is initialized, link is up and communication with host is working fine |

### 1.7.23 TSEL_DEBUG_CTRL

Reg. 0xA00900A4

register used to change default data flow

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tx_pkt_loopback | rw | ro | 0x0 | register used to route tsel TX path to RX. This is a debug feature that allows for stand alone testing where CPU packet inserter can be used drive RX data path. 0=default tx path. 1=tx_packets are looped back to rx |
| 1 | rx_pkt_loopback | rw | ro | 0x0 | register used to route tsel RX path to TX. This is a debug feature that allows for testing TSEL GDB packet loopback. 0=default tx path. 1=rx_packets are looped back to tx |

### 1.7.24 TSEL_DEBUG_CTRL2

Reg. 0xA00900A8

register used to change internal parameters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | interpacket_gap | rw | ro | 0x20 | change min spacing between packets. DO NOT TOUCH UNLESS YOU KNOW WHAT YOU ARE DOING! |

### 1.7.25 DEBUG

Reg. 0xA00900AC

reserved

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ctrl | rw | ro | 0x0 | connects to general-purpose module output port |

### 1.7.26 DEBUG_LINK_UP_OVERWRITE

Reg. 0xA00900B0

register used to overwrite link status - allows to fake out a connection that tsel is connected to a partner.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | data | rw | ro | 0x0 | debug feature only - do not use unless you know what you are doing! |

### 1.7.27 TSEL_CLK_FREQ

Reg. 0xA00900B4

frequency of recovered clock, TSEL GTH

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | val | ro | wo | 0x0 | frequency reading (Hz) |

### 1.7.28 TSEL_DEBUG_IF_SUPPRESS

Reg. 0xA00900B8

register used to suppress interface activity, debug feature

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | disable_if_gmii_tx | rw | ro | 0x0 | set to disable output TX GMII I/F to GDB, silently discards TX packets |
| 1 | disable_if_gmii_rx | rw | ro | 0x0 | set to disable input RX GMII I/F from GDB, silently discards packet at RX input |

| | | | | | |
|---|---|---|---|---|---|
| 2 | disable_if_axis_rx | rw | ro | 0x0 | set to disable output RX AXI-S I/F, silently discards packet at RX output |
| 23:8 | disable_if_axis_tx | rw | ro | 0x0 | set to disable selected TX AXI-S I/F source input (bit[8]=>src0, bit[9]=>src1, etc), holds TREADY low |

### 1.7.29 RX_STATS_ENGINE_CTRL

Reg. 0xA00900C0

register used to control stats engine.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | table_clear | rw | ro | 0x0 | write 1 to perform stats engine table clear |

### 1.7.30 RX_STATS_ENGINE_STATUS

Reg. 0xA00900C4

register used to return stats engine state

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | busy | ro | wo | 0x0 | table_not_ready - when 1, stats table is busy (being cleared). Do not read stats engine until zero |
| 1 | oor | ro | wo | 0x0 | out of range entry detected - when 1 it indicates stats engine was too small to capture statistics for input / outout packet type. reset by clearing stats table |
| 31:16 | oor_pkt_type | ro | wo | 0x0 | out of range entry detected - last packet type that was out of range. reset by clearing stats table |

### 1.7.31 TX_STATS_ENGINE_CTRL

Reg. 0xA00900C8

register used to control stats engine.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | table_clear | rw | ro | 0x0 | write 1 to perform stats engine table clear |

### 1.7.32 TX_STATS_ENGINE_STATUS

Reg. 0xA00900CC

register used to return stats engine state

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | busy | ro | wo | 0x0 | table_not_ready - when 1, stats table is busy (being cleared). Do not read stats engine until zero |
| 1 | oor | ro | wo | 0x0 | out of range entry detected - when 1 it indicates stats engine was too small to capture statistics for input / outout packet type. reset by clearing stats table |
| 31:16 | oor_pkt_type | ro | wo | 0x0 | out of range entry detected - last packet type that was out of range. reset by clearing stats table |

### 1.7.33 PACKET_GEN_CTRL0

Reg. 0xA00900E0

register used to control packet generator rate control.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rate_ctrl | rw | ro | 0x0 | rate control to space packets. Rate = 2**33 / value |

### 1.7.34 PACKET_GEN_CTRL1

Reg. 0xA00900E4

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | packet_type | rw | ro | 0x0 | packet generator packet type used in generating traffic. |
| 23:16 | header_type | rw | ro | 0x0 | header type used for packet generation. |

### 1.7.35 PACKET_GEN_CTRL2

Reg. 0xA00900E8

register used to control packet generator.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | enable | rw | ro | 0x0 | enable. 0 = off / 1 = on |
| 1 | mode | rw | ro | 0x0 | packet generator mode. 0 = fixed size (as defined in bits 31:15) / 1 = incremental 46 to 1500, incrementing by 1 on every packet |
| 15:8 | seed | rw | ro | 0x0 | seed used for packet generator. Do not touch unless you know what you are doing |
| 31:16 | packet_length | rw | ro | 0x0 | packet length used in mode 0 packet generator. Must be in range of 46 to 1500 |

### 1.7.36 PACKET_GEN_CHECKER_CTRL0

Reg. 0xA00900EC

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | packet_type | rw | ro | 0x0 | packet generator checker packet type used in checking traffic. |
| 23:16 | header_type | rw | ro | 0x0 | header type used for packet checking. |

### 1.7.37 PACKET_GEN_CHECKER_CTRL1

Reg. 0xA00900F0

register used to control generator checker.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | enable | rw | ro | 0x0 | enable. 0 = off / 1 = on |
| 15:8 | seed | rw | ro | 0x0 | seed used for packet generator. Do not touch unless you know what you are doing |

### 1.7.38 PKT_COUNT_RX_TOTAL

Reg. 0xA0090100

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.39 BYTE_COUNT_RX_TOTAL

Reg. 0xA0090104

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.40 PKT_COUNT_RX_FCS_ERROR

Reg. 0xA0090108

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.41 BYTE_COUNT_RXTX_LPBK_ERROR

Reg. 0xA009010C

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.42 PKT_COUNT_TX_TOTAL

Reg. 0xA0090120

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.43 BYTE_COUNT_TX_TOTAL

Reg. 0xA0090124

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.44 PKT_COUNT_TX_BUS_ERROR

Reg. 0xA0090128

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.45 PKT_COUNT_TX_DATA_ERROR

Reg. 0xA009012C

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.46 PKT_COUNT_TX_TOO_SHORT_ERROR

Reg. 0xA0090130

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.47 PKT_COUNT_TX_TOO_LONG_ERROR

Reg. 0xA0090134

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.48 CPU_INSERT_BUFFER_CNT

Reg. 0xA0090140

register used to return insert buffer counters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | success | rw | na | 0x0 | successful packet insertion counter |

### 1.7.49 CPU_CAPTURE_BUFFER_CNT

Reg. 0xA0090144

register used to return capture buffer counters

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | success | rw | na | 0x0 | successful packet capture counter |

### 1.7.50 CPU_CAPTURE_BUFFER_CNT1

Reg. 0xA0090148

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | overflow | rw | na | 0x0 | number of packets not captured due to CPU capture buffer being full. |

### 1.7.51 LINK_DOWN_COUNT

Reg. 0xA0090150

generic free running counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear |

### 1.7.52 PACKET_GEN_STATUS0

Reg. 0xA0090180

register used to return packet generator info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | pkt_count | ro | wo | 0x0 | number of packets inserted by the packet generator |

### 1.7.53 PACKET_GEN_CHECKER_STATUS0

Reg. 0xA0090184

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | pkt_count | ro | wo | 0x0 | number of packets checked |

### 1.7.54 PACKET_GEN_STATUS1

Reg. 0xA0090188

register used to return packet generator info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bytes_count | ro | wo | 0x0 | number of bytes inserted by the packet generator |

### 1.7.55 PACKET_GEN_CHECKER_STATUS1

Reg. 0xA009018C

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bytes_count | ro | wo | 0x0 | number of bytes checked by the packet generator |

### 1.7.56 PACKET_GEN_CHECKER_STATUS2

Reg. 0xA0090190

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | pkt_errors | ro | wo | 0x0 | number of packets with errors |

### 1.7.57 PACKET_GEN_CHECKER_STATUS3

Reg. 0xA0090194

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | byte_errors | ro | wo | 0x0 | number of bytes with errors |

### 1.7.58 PACKET_GEN_CHECKER_STATUS4

Reg. 0xA0090198

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | length_errors | ro | wo | 0x0 | number of packets with length errors |

### 1.7.59 PACKET_GEN_CHECKER_STATUS5

Reg. 0xA009019C

register used to return packet checker info.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | sequence_errors | ro | wo | 0x0 | number of packets with sequnce errors |

### 1.7.60 CPU_INSERT_BUFFER

CPU_INSERT_BUFFER 0xA0091000, 0xA0091004 ... 0xA00917FF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to insert packets into TSEL GDB. This memory is implemented as a 4 packet FIFO that allows CPU to insert packets between 1 and 2044 bytes. Important: it is CPU responsibility to ensure inserted packet is in the correct format (i.e. ethernet packet) The following steps are to be performed in order for CPU to insert a packets: 1) check that insert packet FIFO is not full FIFO by reading IRQ_RAW->cpu_insert_buffer_fifo_full = 0 (not full). 2) write insertion length in bytes (between 1-2044) to insert buffer entry [0] 3) write insertion data (between 1-2044 bytes) to insert buffer entries [1:511] 4) issue FIFO push by writting 1 to CPU_INSERT_BUFFER_CTRL->fifo_push. Packet will be inserted as soon as bus access is granted.

### 1.7.61 CPU_CAPTURE_BUFFER

CPU_CAPTURE_BUFFER 0xA0091800, 0xA0091804 ... 0xA0091FFF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to capture packets from TSEL GDB. The capture buffer is implemented as a 4 packet FIFO that allows CPU capture packets between 1 and 2044 bytes in length. The following steps are to be performed in order for CPU to capture packets: 1) set capture filter (TBD - not implemented yet) and enable capture engine CPU_INSERT_BUFFER_CTRL->en = 1 2) wait for packet by reading IRQ_RAW-cpu_capture_buffer_pkt_avail = 1 (or set up interrupt) 3) read capture buffer entry [0]. This entry holds the length of the captured packet in range of 1-2044 bytes 4) read captured data (between 1-2044 bytes form step 3) from capture buffer entries [1:511] 5) issue capture buffer FIFO pop by writting 1 to CPU_INSERT_BUFFER_CTRL->cpu_capture_buffer_ctrl.

### 1.7.62 RX_STATS_ENGINE

RX_STATS_ENGINE 0xA0094000, 0xA0094004 ... 0xA00947FF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

### 1.7.63 TX_STATS_ENGINE

TX_STATS_ENGINE 0xA0096000, 0xA0096004 ... 0xA00967FF

| offset | | depth | 512 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

## 1.8 tselclient_appl_registers_srdl

Block 0xA00A0000 - 0xA00A00EB

Register map used to access and control global FPGA functionality

### 1.8.1 tselclient_module_name

Reg. 0xA00A0000

Defines the module name

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | module_name | ro | na | 0x74636C69 | ASCII code for module name - tsel client = tcli |

### 1.8.2 tselclient_module_version

Reg. 0xA00A0004

Module version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | major_revision | ro | wo | 0x0 | Major Revisoin of module - New features or capabilities definition have been added. |
| 7:0 | minor_revision | ro | wo | 0x0 | Minor Revision of module. This field indicates bug fixes have been applied. For any new features/capabilities increment, this field will reset to zero. |

### 1.8.3 tselclient_page_properties

Reg. 0xA00A0008

Address page properties

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | present | ro | wo | 0x1 | Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not. |
| 30:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | page_size | ro | na | 0x1 | Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enetr here. |
| 7:0 | unified_header_rev | ro | na | 0x1 | Unified Header Format common registers revision. |

### 1.8.4 tselclient_scratchregister

Reg. 0xA00A000C

Scratchregister register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchregister | rw | na | 0x12345678 | SW can write to it and read from it for test purposes. |

### 1.8.5 tselclient_irq_enable

Reg. 0xA00A0010

Interrupt Requests Enable/Mask Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_enable | rw | ro | 0x0 | IRQ0 enable bit. Not implemented here/DTEC |
| 1 | irq1_enable | rw | ro | 0x0 | IRQ1 enable bit. Not implemented here/DTEC |

### 1.8.6 tselclient_irq_pending

Reg. 0xA00A0014

Interrupt Pending Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_pending | r/w1c | wo | 0x0 | IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |
| 1 | irq1_pending | r/w1c | wo | 0x0 | IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |

### 1.8.7 tselclient_irq_raw

Reg. 0xA00A0018

Interrupt Raw Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_raw | ro | wo | 0x0 | IRQ0 raw status bit. Not implemented here/DTEC |
| 1 | irq1_raw | ro | wo | 0x0 | IRQ1 raw status bit. Not implemented here/DTEC |

### 1.8.8 tselclient_irq_force

Reg. 0xA00A001C

Interrupt Force Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Not implemented here/DTEC |
| 1 | irq1_force | rw | ro | 0x0 | IRQ1 force bit. SW to write '1' to emulate an interrupt. Not implemented here/DTEC |

### 1.8.9 rt_data_handler_stat

Reg. 0xA00A0060

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here. receive fsm receives 2 packets, packet1 and packet2 while tranmit fsm transmits acknowledement pkt for every packet1 received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | rx_fsm_pkt_lgth_field_err | r/w1c | wo | 0x0 | 1 = received a packet1/packet2 with length field not equal to 0x30/45 /0 = received packet with expected data in length filed. |
| 1 | rx_fsm_pload_err | r/w1c | wo | 0x0 | 1 = received a packet1/packet2 with pload type isn't 0x15 (ETEC sends DTEC) /0 = received packet with expected data in pload type field. |
| 2 | rx_fsm_e2d_hdr_err | r/w1c | wo | 0x0 | 1 = received a packet1 with e2d header is not 0x10/0x11 /0 = received packet with expected data in e2d header field. |
| 3 | pkt1_sync_hdr_err | r/w1c | wo | 0x0 | 1 = received a packet1 with sync id field not equal to 0x04 /0 = received packet with expected data in sync id header field. |
| 4 | pkt1_etecflags_hdr_err | r/w1c | wo | 0x0 | 1 = received a packet1 with etecflags header field not equal to 0x05 /0 = received packet with expected data in etecflags header field. |
| 5 | pkt1_zeropad_hdr_err | r/w1c | wo | 0x0 | 1 = received a packet1 with zeropad field not equal to zero/0 = received packet with expected zeros in zeropad field. |
| 6 | rx_fsm_eot_err | r/w1c | wo | 0x0 | 1 = received a packet1 with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. |
| 8:7 | pkt1_seq_err | r/w1c | wo | 0x0 | MSB 1 = received a packet1 with sequence number error/0 = received packet with expected sequence number. received packet1 should be received in order. after reset the lsb bit is always set to 1 and ignore this |
| 10:9 | pkt2_seq_err | r/w1c | wo | 0x0 | MSB 1 = received a packet2 with sequence number error/0 = received packet with expected sequence number. received packet2 should be received in order. after reset the lsb bit is always set to 1 and ignore this |
| 11 | rx_fsm_eop_err | r/w1c | wo | 0x0 | 1 = if packet1/packet2 received is terminated early or lasts longer than expected |
| 12 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. |
| 13 | rx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = real time receive fsm doesn't return to idle state within 100 clk cycles. |

| | | | | | |
|---|---|---|---|---|---|
| 14 | pkt1_wdog_err | r/w1c | wo | 0x0 | 1 = not received packet1 within 100us where it is expected to be recived every 60KHz |
| 15 | not_rx_rd_pkt2_axis | r/w1c | wo | 0x0 | 1 = pkt2 axis tx fsm has valid data but not received ready with in valid time of 80us |
| 16 | pkt2_axis_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = pkt2 axis tx fsm didn't return to idle within valid time of 100us |
| 17 | reserved_byte_err | r/w1c | wo | 0x0 | 1 = received a packet with reserved field not equal to zero/0 = received packet with expected zeros in reserved field. |
| 18 | pkt2_zeropad_hdr_err | r/w1c | wo | 0x0 | 1 = received a packet2 with zeropad field not equal to zero/0 = received packet with expected zeros in zeropad field. |
| 19 | pkt1_detected | r/w1c | wo | 0x0 | 1 = tsel client received packet1. these are provided to rdl counters to count how many packet1 being received |
| 20 | pkt2_detected | r/w1c | wo | 0x0 | 1 = tsel client received packet2. these are provided to rdl counters to count how many packet2 being received |
| 21 | good_pkt2_detected | r/w1c | wo | 0x0 | 1 = received good packet2. these are provided to rdl counters to count how many good packet2 being received |
| 22 | pkt2_data_lost | r/w1c | wo | 0x0 | 1 = received good packet2 but the data got lost before axi-streaming it out. the reasons can be the fsm is either waiting for the ready signal so it can axis depacketized packet2 or its in the process of tranmitting an older pkt2 |
| 24:23 | rx_fsm_reserved | r/w1c | wo | 0x0 | 2 bits reserved for receive fsm future use |
| 25 | tx_fsm_link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. same as the 12th bit, repeated again for easy redability(when testing tx fsm alone) |
| 26 | tx_fsm_axis_fifi_full | r/w1c | wo | 0x0 | transmit fsm tranmits the ack packtes to unified tsel interface through axis fifo.1= fifo is full/0 =fifo not full. |
| 27 | tx_fsm_internal_fifo_full | r/w1c | wo | 0x0 | transmit fsm receives input from receive fsm through interanl fifo. 1= fifo is full/0 =fifo not full. transmit fsm sends an acknowledement pkt for every packet1 received from etec, a fifo of depth 16 is added to store the response for packet1. |
| 28 | tx_fsm_internal_fifo_empty | r/w1c | wo | 0x0 | transmit fsm receives input from receive fsm through interanl fifo.1 = fifo is empty/0 = fifo not empty. transmit fsm sends an acknowledement pkt for every packet1 received from etec, a fifo of depth 16 is added to store the response for packet1. |
| 29 | tx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = real time transmit fsm doesn't return to idle state within 3ms |
| 31:30 | tx_fsm_reserved | r/w1c | wo | 0x0 | 3 bits reserved for transmit fsm future use |

### 1.8.10 tx_fsm_dg_kpi_ctrl

Reg. 0xA00A0064

ddm dg kpi enable control

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tx_dg_kpi | rw | ro | 0x1 | dtec requests etec to send ddm bpam1 metrics(send 7 ESM packets) through acknowledement packet sent using real time transmit fsm. 1 = send ddm bpam metrics / 0 = stop sending bpam metrics |

### 1.8.11 pkt1

RegGrp 0xA00A0068 - 0xA00A008F

received pkt1 data from etec after depacketisation. 25 bytes wide

#### 1.8.11.1 tag1

Reg. 0xA00A0068

tag for sowftare to make sure all the registers are read at same time

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tag | ro | wo | 0x0 | synchronization register |

#### 1.8.11.2 timestamp_data

Reg. 0xA00A006C

packet1 timestamp data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | timestamp | ro | wo | 0x0 | 4 bytes long timestamp |

### 1.8.11.3 sync_stat_data

Reg. 0xA00A0070

packet1 sync status data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | fire_droplet | ro | wo | 0x0 | ON -fire ON/OFF droplet |
| 1 | health_status | ro | wo | 0x0 | H-communication health status '1' |
| 2 | wc_trigger | ro | wo | 0x0 | waveform capture trigger |
| 3 | ppec | ro | wo | 0x0 | perform pre pulse energy control |
| 4 | early_exp_gate_ indicator | ro | wo | 0x0 | Early indicator of exposure gate |
| 5 | sync_stat_bit5 | ro | wo | 0x0 | spare |
| 6 | sync_stat_bit6 | ro | wo | 0x0 | spare |
| 7 | sync_stat_bit7 | ro | wo | 0x0 | spare |

### 1.8.11.4 shot_id_data

Reg. 0xA00A0074

packet1 shot ID data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | shot_id | ro | wo | 0x0 | 4 bytes long |

### 1.8.11.5 burst_id_data

Reg. 0xA00A0078

packet1 burst ID data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | burst_id | ro | wo | 0x0 | 4 bytes long |

### 1.8.11.6 msec_id_data

Reg. 0xA00A007C

packet1 msec ID data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | msec_id | ro | wo | 0x0 | 4 bytes long |

### 1.8.11.7 lc_diag_data

Reg. 0xA00A0080

packet1 lc diagnostics data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | fast_euv_gaten | ro | wo | 0x1 | active low fast euv gate |
| 1 | scanner_gaten | ro | wo | 0x1 | active low scanner gate |
| 2 | exp_gaten | ro | wo | 0x1 | active low exposure gate |
| 3 | lc_diag_bit3 | ro | wo | 0x0 | spare |
| 4 | lc_diag_bit4 | ro | wo | 0x0 | spare |
| 5 | lc_diag_bit5 | ro | wo | 0x0 | spare |
| 6 | lc_diag_bit6 | ro | wo | 0x0 | spare |
| 7 | lc_diag_bit7 | ro | wo | 0x0 | spare |
| 8 | lc_diag_bit8 | ro | wo | 0x0 | spare |
| 9 | lc_diag_bit9 | ro | wo | 0x0 | spare |
| 10 | lc_diag_bit10 | ro | wo | 0x0 | spare |
| 11 | lc_diag_bit11 | ro | wo | 0x0 | spare |
| 12 | lc_diag_bit12 | ro | wo | 0x0 | spare |
| 13 | lc_diag_bit13 | ro | wo | 0x0 | spare |
| 14 | lc_diag_bit14 | ro | wo | 0x0 | spare |
| 15 | lc_diag_bit15 | ro | wo | 0x0 | spare |

### 1.8.11.8 pp2mp_tfire_totaldelay_data

Reg. 0xA00A0084

packet1 pp2mp tfire totaldelay data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | pp2mp_tfire_totaldelay | ro | wo | 0x0 | 4 bytes long |

### 1.8.11.9 euv_value_data

Reg. 0xA00A0088

packet1 euv value data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | euv_value | ro | wo | 0x0 | 4 bytes long |

### 1.8.11.10 tag2

Reg. 0xA00A008C

tag for sowftare to make sure all the registers are read at same time

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tag | ro | wo | 0x0 | synchronization register |

End RegGroup

### 1.8.12 ddm_bpam_send7_crc_err_cnt

Reg. 0xA00A0090

register used to return count of ddm bpam send7 crc errors

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | this counter increments when the ddm bpam send7 crc error bit is 1 when good pkt2 is received |

### 1.8.13 ddm_data_lost_cnt

Reg. 0xA00A0094

register used to return count of ddm data lost

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | this counter increments when the ddm data received can't be saved to pkt mode fifo |

### 1.8.14 ddm_data_bytes_err_cnt

Reg. 0xA00A0098

register used to return count of ddm data bytes error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | this counter increments when the ddm data recived bytes is not as expected-67 bytes |

### 1.8.15 rx_fsm_pkt_lgth_field_err_cnt

Reg. 0xA00A009C

register used to return captured packet length field errror

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | received packet length field error capture counter |

### 1.8.16 rx_fsm_pload_err_cnt

Reg. 0xA00A00A0

register used to return captured packet payload field error

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | received packet payload field error capture counter |

### 1.8.17 unknown_pkt_rx_cnt

Reg. 0xA00A00A4

register used to return the count of unknown packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected an unknown packet |

### 1.8.18 pkt1_sync_hdr_err_cnt

Reg. 0xA00A00A8

register used to return captured packet1 sync header field errror

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | packet1 sync hdr field error capture counter |

### 1.8.19 pkt1_etecflags_hdr_err_cnt

Reg. 0xA00A00AC

register used to return captured packet1 etec flags header field errror

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | packet1 etec flags hdr field error capture counter |

### 1.8.20 pkt1_zeropad_hdr_err_cnt

Reg. 0xA00A00B0

register used to return captured packet1 zeropad field errror

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | packet1 zeropad field error capture counter |

### 1.8.21 rx_fsm_eot_err_cnt

Reg. 0xA00A00B4

register used to return captured packet errror in eot

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | received packet not terminated as expected |

### 1.8.22 pkt1_seq_err_cnt

Reg. 0xA00A00B8

register used to return captured packet1 sequence errror in eot

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | packet1 not recieved in order |

### 1.8.23 pkt2_seq_err_cnt

Reg. 0xA00A00BC

register used to return captured packet2 sequence errror in eot

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | packet2 not recieved in order |

### 1.8.24 rx_fsm_eop_err_cnt

Reg. 0xA00A00C0

register used to return captured packet terminated early or lasts longer than expecte

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | received packet terminated early or lasts longer |

### 1.8.25 rx_fsm_wdog_err_cnt

Reg. 0xA00A00C4

register used to return receive fsm wdog errror

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | real time receive fsm doesn't return to idle state within 3ms |

### 1.8.26 pkt2_axis_fsm_wdog_err_cnt

Reg. 0xA00A00C8

register used to return error when fsm used to axi stream packet2 doen't return to idle within valid time

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | pkt2 axis tx fsm didn't return to idle within valid time 100us |

### 1.8.27 reserved_byte_err_cnt

Reg. 0xA00A00CC

register used to return error when received pkt is missing the reserved byte

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | packet1 zeropad field error capture counter |

### 1.8.28 pkt2_zeropad_hdr_err_cnt

Reg. 0xA00A00D0

register used to return captured packet2 zeropad field errror

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | packet2 zeropad field error capture counter |

### 1.8.29 tx_fsm_wdog_err_cnt

Reg. 0xA00A00D4

register used to return transmit fsm wdog errror

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_count | rw | na | 0x0 | real time transmit fsm doesn't return to idle state within 3ms |

### 1.8.30 pkt1_rx_cnt

Reg. 0xA00A00D8

register used to return count of packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | +1 => new packet received |

### 1.8.31 pkt2_rx_cnt

Reg. 0xA00A00DC

register used to return count of packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | +1 => new packet received |

### 1.8.32 good_pkt1_rx_cnt

Reg. 0xA00A00E0

register used to return count of packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | +1 => new packet received |

### 1.8.33 good_pkt2_rx_cnt

Reg. 0xA00A00E4

register used to return count of packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | count | rw | na | 0x0 | +1 => new packet received |

### 1.8.34 good_pkt2_lost_cnt

Reg. 0xA00A00E8

register used to return the count when tsel pkt received is lost due to lack of storage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lost_cnt | rw | na | 0x0 | +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost |

## 1.9 tselbridge_appl_registers_srdl

Block 0xA00A1000 - 0xA00A110F

Register map used to access and control global FPGA functionality

### 1.9.1 tselbridge_module_name

Reg. 0xA00A1000

Defines the module name

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | module_name | ro | na | 0x74627267 | ASCII code for module name - tsel bridge = tbrg |

### 1.9.2 tselbridge_module_version

Reg. 0xA00A1004

Module version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | major_revision | ro | wo | 0x0 | Major Revisoin of module - New features or capabilities definition have been added. |
| 7:0 | minor_revision | ro | wo | 0x0 | Minor Revision of module. This field indicates bug fixes have been applied. For any new features/capabilities increment, this field will reset to zero. |

### 1.9.3 tselbridge_page_properties

Reg. 0xA00A1008

Address page properties

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | present | ro | wo | 0x1 | Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not. |
| 30:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | page_size | ro | na | 0x1 | Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enetr here. |
| 7:0 | unified_header_rev | ro | na | 0x1 | Unified Header Format common registers revision. |

### 1.9.4 tselbridge_scratchregister

Reg. 0xA00A100C

Scratchregister register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchregister | rw | na | 0x12345678 | SW can write to it and read from it for test purposes. |

### 1.9.5 tselbridge_irq_enable

Reg. 0xA00A1010

Interrupt Requests Enable/Mask Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_enable | rw | ro | 0x0 | IRQ0 enable bit. Not implemented here/DTEC |
| 1 | irq1_enable | rw | ro | 0x0 | IRQ1 enable bit. Not implemented here/DTEC |

### 1.9.6 tselbridge_irq_pending

Reg. 0xA00A1014

Interrupt Pending Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_pending | r/w1c | wo | 0x0 | IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |
| 1 | irq1_pending | r/w1c | wo | 0x0 | IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC |

### 1.9.7 tselbridge_irq_raw

Reg. 0xA00A1018

Interrupt Raw Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_raw | ro | wo | 0x0 | IRQ0 raw status bit. Not implemented here/DTEC |
| 1 | irq1_raw | ro | wo | 0x0 | IRQ1 raw status bit. Not implemented here/DTEC |

### 1.9.8 tselbridge_irq_force

Reg. 0xA00A101C

Interrupt Force Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Not implemented here/DTEC |
| 1 | irq1_force | rw | ro | 0x0 | IRQ1 force bit. SW to write '1' to emulate an interrupt. Not implemented here/DTEC |

### 1.9.9 rt_data_handler_algo_rx_stat

Reg. 0xA00A1060

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for algo pkt receive fsm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | damp_algo_data_lost | r/w1c | wo | 0x0 | 1 = new data arrived while sending the old damp algo data and the damp algo data is lost as there is no internal fifo |
| 1 | rx_fsm_eth_lgth_field_err | r/w1c | wo | 0x0 | 1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed. |
| 2 | rx_fsm_pload_err | r/w1c | wo | 0x0 | 1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field. |
| 3 | rx_fsm_eot_err | r/w1c | wo | 0x0 | 1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. |
| 4 | rx_fsm_reserved_byte_err | r/w1c | wo | 0x0 | 20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch |
| 5 | rx_fsm_eop_er | r/w1c | wo | 0x0 | 1 = tlast is received at unexpected byte position/0 = received a right size packet. |
| 6 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. GDB link status |
| 7 | damp_algo_seq_err | r/w1c | wo | 0x0 | 1 = damp algo pkt numbers are not in order |
| 8 | unknown_pkt_hdr_err | r/w1c | wo | 0x0 | 1 = pkt received is not a known type |
| 9 | nonpkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the good 512 bytes of algo data is full. |
| 10 | damp_algo_rx_rdy_wdog_err | r/w1c | wo | 0x0 | 1 = when a valid damp algo data is available to be transmitted and dtec simulink algo is not ready to receive within 2ms |
| 11 | damp_algo_rx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = receive fsm that receives the algo pkt doesn't return to the idle state with in 3msec |
| 15:12 | rx_fsm_reserved | r/w1c | wo | 0x0 | 3 bits reserved for receive fsm future use |

### 1.9.10 rt_data_handler_boot_rx_stat

Reg. 0xA00A1064

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for boot receive fsm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | boot_data_lost | r/w1c | wo | 0x0 | 1 = new data arrived while sending the old boot data and the damp boot data is lost as there is no internal fifo |
| 1 | rx_fsm_eth_lgth_field_err | r/w1c | wo | 0x0 | 1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed. |
| 2 | rx_fsm_pload_err | r/w1c | wo | 0x0 | 1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field. |
| 3 | rx_fsm_eot_err | r/w1c | wo | 0x0 | 1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. |
| 4 | zeropad_err | r/w1c | wo | 0x0 | 1 = zero padding error detected on the packet received |
| 5 | rx_fsm_reserved_byte_err | r/w1c | wo | 0x0 | 20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch |
| 6 | rx_fsm_eop_er | r/w1c | wo | 0x0 | 1 = tlast is received at unexpected byte position/0 = received a right size packet. |
| 7 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. GDB link status |
| 8 | boot_seq_err | r/w1c | wo | 0x0 | 1 = damp boot pkt numbers are not in order |
| 9 | boot_seg_seq_err | r/w1c | wo | 0x0 | 1 = damp boot segments (fragment pkt numbers) are not in order/sop err/eop err |
| 10 | unknown_pkt_hdr_err | r/w1c | wo | 0x0 | 1 = pkt received is not a known type |
| 11 | nonpkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the good 1024 bytes boot data from packet mode fifo is full. |
| 12 | pkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the boot data from unifed TSEL IF is full. pkt mode is enabled for this fifo |
| 13 | boot_rx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = receive fsm that receives the boot pkt doesn't return to the idle state with in 3msec |
| 14 | sop_err | r/w1c | wo | 0x0 | 1 = the boot pkt received has sop error => sop not set on 1st pkt or set on last pkt |
| 15 | eop_err | r/w1c | wo | 0x0 | 1 = the boot pkt received has eop error => eop not set on last pkt |
| 16 | seg_seq_out_of_order | r/w1c | wo | 0x0 | 1 = boot segments (fragment pkt numbers) are not in order |
| 31:17 | rx_fsm_reserved | r/w1c | wo | 0x0 | 15 bits reserved for receive fsm future use |

### 1.9.11 rt_data_handler_diag_rx_stat

Reg. 0xA00A1068

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for diag receive fsm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | diag_data_lost | r/w1c | wo | 0x0 | 1 = new data arrived while sending the old diag data and the damp diag data is lost as there is no internal fifo |
| 1 | rx_fsm_eth_lgth_field_err | r/w1c | wo | 0x0 | 1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed. |
| 2 | rx_fsm_pload_err | r/w1c | wo | 0x0 | 1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field. |
| 3 | rx_fsm_eot_err | r/w1c | wo | 0x0 | 1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. |
| 4 | zeropad_err | r/w1c | wo | 0x0 | 1 = zero padding error detected on the packet received |
| 5 | rx_fsm_reserved_byte_err | r/w1c | wo | 0x0 | 20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch |
| 6 | rx_fsm_eop_er | r/w1c | wo | 0x0 | 1 = tlast is received at unexpected byte position/0 = received a right size packet. |
| 7 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. GDB link status |
| 8 | diag_seq_err | r/w1c | wo | 0x0 | 1 = damp diagnostics pkt numbers are not in order |
| 9 | diag_seg_seq_err | r/w1c | wo | 0x0 | 1 = damp diag segments (fragment pkt numbers) are not in order/sop err/eop err |
| 10 | unknown_pkt_hdr_err | r/w1c | wo | 0x0 | 1 = pkt received is not a known type |
| 11 | nonpkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the good 512 bytes diag data from packet mode fifo is full. |

| | | | | | |
|---|---|---|---|---|---|
| 12 | pkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the diag data from unifed TSEL IF is full. pkt mode is enabled for this fifo |
| 13 | diag_rx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = receive fsm that receives the diag pkt doesn't return to the idle state with in 3msec |
| 14 | sop_err | r/w1c | wo | 0x0 | 1 = the diag pkt received has sop error => sop not set on 1st pkt or set on last pkt |
| 15 | eop_err | r/w1c | wo | 0x0 | 1 = the diag pkt received has eop error => eop not set on last pkt |
| 16 | seg_seq_out_of_order | r/w1c | wo | 0x0 | 1 = diag segments (fragment pkt numbers) are not in order |
| 31:17 | rx_fsm_reserved | r/w1c | wo | 0x0 | 15 bits reserved for receive fsm future use |

### 1.9.12 rt_data_handler_wfm_reg_rx_stat

Reg. 0xA00A106C

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for wfm reg pkt

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | wfm_reg_data_lost | r/w1c | wo | 0x0 | 1 = new data arrived while sending the old wfm reg data and the damp wfm reg data is lost as there is no internal fifo |
| 1 | rx_fsm_eth_lgth_field_err | r/w1c | wo | 0x0 | 1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed. |
| 2 | rx_fsm_pload_err | r/w1c | wo | 0x0 | 1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field. |
| 3 | rx_fsm_eot_err | r/w1c | wo | 0x0 | 1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. |
| 4 | zeropad_err | r/w1c | wo | 0x0 | 1 = zero padding error detected on the packet received |
| 5 | rx_fsm_reserved_byte_err | r/w1c | wo | 0x0 | 20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch |
| 6 | rx_fsm_eop_er | r/w1c | wo | 0x0 | 1 = tlast is received at unexpected byte position/0 = received a right size packet. |
| 7 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. GDB link status |
| 8 | wfm_reg_seq_err | r/w1c | wo | 0x0 | 1 = damp waveform register pkt numbers are not in order |
| 9 | wfm_reg_seg_seq_err | r/w1c | wo | 0x0 | 1 = damp waveform register segments (fragment pkt numbers) are not in order |
| 10 | unknown_pkt_hdr_err | r/w1c | wo | 0x0 | 1 = pkt received is not a known type |
| 11 | nonpkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the good 512 bytes wfm reg data from packet mode fifo is full. |
| 12 | pkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the diag data from unifed TSEL IF is full. pkt mode is enabled for this fifo |
| 13 | wfm_reg_rx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = receive fsm that receives the wfm reg pkt doesn't return to the idle state with in 3msec |
| 14 | sop_err | r/w1c | wo | 0x0 | 1 = the diag pkt received has sop error => sop not set on 1st pkt or set on last pkt |
| 15 | eop_err | r/w1c | wo | 0x0 | 1 = the diag pkt received has eop error => eop not set on last pkt |
| 16 | seg_seq_out_of_order | r/w1c | wo | 0x0 | 1 = diag segments (fragment pkt numbers) are not in order |
| 31:17 | rx_fsm_reserved | r/w1c | wo | 0x0 | 15 bits reserved for receive fsm future use |

### 1.9.13 rt_data_handler_vol_wfm_samp_rx_stat

Reg. 0xA00A1070

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for wfm samp receive fsm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | vol_wfm_samp_data_lost | r/w1c | wo | 0x0 | 1 = new data arrived while sending the old voltage wfm sample data and the damp voltage wfm sample data is lost as there is no internal fifo |
| 1 | rx_fsm_eth_lgth_field_err | r/w1c | wo | 0x0 | 1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed. |
| 2 | rx_fsm_pload_err | r/w1c | wo | 0x0 | 1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field. |

| | | | | | |
|---|---|---|---|---|---|
| 3 | rx_fsm_eot_err | r/w1c | wo | 0x0 | 1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. |
| 4 | zeropad_err | r/w1c | wo | 0x0 | 1 = zero padding error detected on the packet received |
| 5 | rx_fsm_reserved_byte_err | r/w1c | wo | 0x0 | 20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch |
| 6 | rx_fsm_eop_er | r/w1c | wo | 0x0 | 1 = tlast is received at unexpected byte position/0 = received a right size packet. |
| 7 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. GDB link status |
| 8 | wfm_samp_seq_err | r/w1c | wo | 0x0 | 1 = damp waveform sample pkt numbers are not in order |
| 9 | wfm_samp_seg_out_of_order | r/w1c | wo | 0x0 | 1 = damp voltage waveform sample segments (fragment pkt numbers) are not in order |
| 10 | vol_wfm_samp_seg_seq_err | r/w1c | wo | 0x0 | 1 = damp voltage waveform sample segments (fragment pkt numbers) are not in order/sop err/ eop err |
| 11 | unknown_wfm_samp_err | r/w1c | wo | 0x0 | 1 = damp waveform sample received is neither voltage nor current |
| 12 | unknown_pkt_hdr_err | r/w1c | wo | 0x0 | 1 = pkt received is not a known type |
| 13 | nonpkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the good 16384 vol data from packet mode fifo is full. |
| 14 | pkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the vol data from unifed TSEL IF is full. pkt mode is enabled for this fifo |
| 15 | vol_wfm_samp_rx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = receive fsm that receives the vol wfm samp pkt doesn't return to the idle state with in 3msec |
| 16 | amp_wfm_samp_sop_err | r/w1c | wo | 0x0 | 1 = the amp wfm samp pkt received has sop error => sop not set on 1st pkt or set on last pkt |
| 17 | amp_wfm_samp_eop_err | r/w1c | wo | 0x0 | 1 = the amp wfm samp pkt received has eop error => eop not set on last pkt |
| 31:18 | reserved | r/w1c | wo | 0x0 | reserved for future use |

### 1.9.14 rt_data_handler_amp_wfm_samp_rx_stat

Reg.

0xA00A1074

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for wfm samp receive fsm

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | amp_wfm_samp_data_lost | r/w1c | wo | 0x0 | 1 = new data arrived while sending the old current wfm sample data and the damp current wfm sample data is lost as there is no internal fifo |
| 1 | rx_fsm_eth_lgth_field_err | r/w1c | wo | 0x0 | 1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed. |
| 2 | rx_fsm_pload_err | r/w1c | wo | 0x0 | 1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field. |
| 3 | rx_fsm_eot_err | r/w1c | wo | 0x0 | 1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. |
| 4 | zeropad_err | r/w1c | wo | 0x0 | 1 = zero padding error detected on the packet received |
| 5 | rx_fsm_reserved_byte_err | r/w1c | wo | 0x0 | 20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch |
| 6 | rx_fsm_eop_er | r/w1c | wo | 0x0 | 1 = tlast is received at unexpected byte position/0 = received a right size packet. |
| 7 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. GDB link status |
| 8 | wfm_samp_seq_err | r/w1c | wo | 0x0 | 1 = damp waveform sample pkt numbers are not in order |
| 9 | wfm_samp_seg_seq_out_of_order | r/w1c | wo | 0x0 | 1 = damp current waveform sample segments (fragment pkt numbers) are not in order |
| 10 | amp_wfm_samp_seg_seq_err | r/w1c | wo | 0x0 | 1 = damp current waveform sample segments (fragment pkt numbers) are not in order/eop not set for last pkt/sop not set for 1st pkt |
| 11 | unknown_wfm_samp_err | r/w1c | wo | 0x0 | 1 = damp waveform sample received is neither voltage nor current |
| 12 | unknown_pkt_hdr_err | r/w1c | wo | 0x0 | 1 = pkt received is not a known type |
| 13 | nonpkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the good 16384 amp data from packet mode fifo is full. |
| 14 | pkt_mode_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo that receives the amp data from unifed TSEL IF is full. pkt mode is enabled for this fifo |

| | | | | | |
|---|---|---|---|---|---|
| 15 | amp_wfm_samp_rx_fsm_wdog_err | r/w1c | wo | 0x0 | 1 = receive fsm that receives the amp wfm samp pkt doesn't return to the idle state with in 3msec |
| 16 | amp_wfm_samp_sop_err | r/w1c | wo | 0x0 | 1 = the amp wfm samp pkt received has sop error => sop not set on 1st pkt or set on last pkt |
| 17 | amp_wfm_samp_eop_err | r/w1c | wo | 0x0 | 1 = the amp wfm samp pkt received has eop error => eop not set on last pkt |
| 31:18 | reserved | r/w1c | wo | 0x0 | reserved for future use |

### 1.9.15 rt_data_handler_tx_stat

Reg. 0xA00A1078

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here. the tranmit fsm transmits dtec algo data pkt and ctrl data pkt

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | link_loss | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. depulicated the GDB link status. can also be found at rt_data_handler_rx_stat register |
| 1 | tx_fsm_algo_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo connected to the unified tsel interface that is receiving dtec2damp simulink algo data pkt from transmit state machine is full (data is still written to the fifo even its full) /0 = fifo is not full |
| 2 | tx_fsm_dtec_algo_wdog_err | r/w1c | wo | 0x0 | 1 = the fsm that recives dtec algo data from dtec simulink algo doesn't return back to idle within 3ms(dtec alog packet not recived from dtec simulink algo with in 3ms after after tvalid goes high initially)/0 = after initial tvalid, tlast is seen within 3ms |
| 3 | tx_fsm_dtec_algo_data_err | r/w1c | wo | 0x0 | 1 = dtec algo data with unexpected size received |
| 4 | tx_fsm_dtec_algo_fifo_rx_rdy_err | r/w1c | wo | 0x0 | 1 = the fifo that receiving the dtec algo pkt is not ready for some reason while a part of data is received |
| 7:5 | tx_fsm_dtec_algo_reserved | r/w1c | wo | 0x0 | status bits reserved for dtec algo tx fsm |
| 8 | link_loss_dup | r/w1c | wo | 0x0 | 1 = link loss/0 = link is established. depulicated the GDB link status. can also be found at rt_data_handler_rx_stat register |
| 9 | tx_fsm_ctrl_fifo_full | r/w1c | wo | 0x0 | 1 = the fifo connected to the unified tsel interface that is receiving dtec2damp ctrl data pkt from transmit state machine is full (data is still written to the fifo even its full) /0 = fifo is not full |
| 10 | tx_fsm_dtec_ctrl_wdog_err | r/w1c | wo | 0x0 | 1 = the fsm that transmits the ctrl data pkt doesn't return back to idle within 3ms |
| 11 | tx_fsm_ctrl_fifo_rx_rdy_err | r/w1c | wo | 0x0 | 1 = the fifo that receiving the ctrl pkt is not ready for some reason while a part of data is received |
| 15:12 | tx_fsm_ctrl_reserved | r/w1c | wo | 0x0 | status bits reserved for control pkt tx fsm |

### 1.9.16 ps_por_b

Reg. 0xA00A107C

issue external por

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | external_reset | rw | ro | 0x0 | 1 => issue external reset to DAMP using control data pkt |

### 1.9.17 ps_srst_b

Reg. 0xA00A1080

issue remote system reset

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | remote_reset | rw | ro | 0x0 | 1 => issue remote reset to DAMP using control data pkt |

### 1.9.18 enb_wfm_cap

Reg. 0xA00A1084

enables the waveform capture

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 0 | waveform_cap | rw | ro | 0x0 | 1 => DAMP waveform capture feature is enabled using control data pkt |

### 1.9.19 direct_boot_offset_set

Reg. 0xA00A1088

boot offset settings

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | boot_offset | rw | ro | 0x0 | 32 bit boot offset for DAMP using control data pkt |

### 1.9.20 cntrl_pkt_rate_ctrl

Reg. 0xA00A108C

Control packet rate control register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rate_ctrl | rw | ro | 0x3B9ACA0 | 32 bit rate control register for Control data packet. Default value is 1sec. Clk used = 125MHz |

### 1.9.21 algo_data_good_frame_cnt

Reg. 0xA00A1090

register used to return the count for good frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | good_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a good frame |

### 1.9.22 algo_data_bad_frame_cnt

Reg. 0xA00A1094

register used to return the count for bad frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bad_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a bad frame |

### 1.9.23 goodalgo_tsel_pkt_lost_cnt

Reg. 0xA00A1098

register used to return the count when tsel pkt received is lost due to lack of storage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lost_cnt | rw | na | 0x0 | +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost |

### 1.9.24 boot_data_good_frame_cnt

Reg. 0xA00A109C

register used to return the count for good frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | good_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a good frame |

### 1.9.25 boot_data_bad_frame_cnt

Reg. 0xA00A10A0

register used to return the count for bad frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bad_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a bad frame |

### 1.9.26 boot_tsel_pkt_lost_cnt

Reg. 0xA00A10A4

register used to return the count when tsel pkt received is lost due to lack of storage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lost_cnt | rw | na | 0x0 | +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost |

### 1.9.27 diag_data_good_frame_cnt

Reg. 0xA00A10A8

register used to return the count for good frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | good_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a good frame |

### 1.9.28 diag_data_bad_frame_cnt

Reg. 0xA00A10AC

register used to return the count for bad frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bad_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a bad frame |

### 1.9.29 diag_tsel_pkt_lost_cnt

Reg. 0xA00A10B0

register used to return the count when tsel pkt received is lost due to lack of storage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lost_cnt | rw | na | 0x0 | +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost |

### 1.9.30 wfm_reg_data_good_frame_cnt

Reg. 0xA00A10B4

register used to return the count for good frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | good_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a good frame |

### 1.9.31 wfm_reg_data_bad_frame_cnt

Reg. 0xA00A10B8

register used to return the count for bad frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bad_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a bad frame |

### 1.9.32 wfm_reg_tsel_pkt_lost_cnt

Reg. 0xA00A10BC

register used to return the count when tsel pkt received is lost due to lack of storage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lost_cnt | rw | na | 0x0 | +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost |

### 1.9.33 vol_wfm_samp_data_good_frame_cnt

Reg. 0xA00A10C0

register used to return the count for good frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | good_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a good frame |

### 1.9.34 vol_wfm_samp_data_bad_frame_cnt

Reg. 0xA00A10C4

register used to return the count for bad frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bad_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a bad frame |

### 1.9.35 vol_wfm_samp_tsel_pkt_lost_cnt

Reg. 0xA00A10C8

register used to return the count when tsel pkt received is lost due to lack of storage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lost_cnt | rw | na | 0x0 | +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost |

### 1.9.36 amp_wfm_samp_data_good_frame_cnt

Reg. 0xA00A10CC

register used to return the count for good frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | good_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a good frame |

### 1.9.37 amp_wfm_samp_data_bad_frame_cnt

Reg. 0xA00A10D0

register used to return the count for bad frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bad_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a bad frame |

### 1.9.38 amp_wfm_samp_tsel_pkt_lost_cnt

Reg. 0xA00A10D4

register used to return the count when tsel pkt received is lost due to lack of storage

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | lost_cnt | rw | na | 0x0 | +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost |

### 1.9.39 wfm_samp_data_bad_frame_cnt

Reg. 0xA00A10D8

register used to return the count for bad frames received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | bad_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected a bad frame |

### 1.9.40 unknown_pkt_cnt

Reg. 0xA00A10DC

register used to return the count of unknown packets received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected an unknown packet |

### 1.9.41 boot_data_sop_err_cnt

Reg. 0xA00A10E0

register used to return the count of sop errors received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected sop not set on 1st pkt or set on last pkt |

### 1.9.42 boot_data_eop_err_cnt

Reg. 0xA00A10E4

register used to return the count of eop err received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected eop not set on last pkt |

### 1.9.43 boot_data_seg_out_of_order_cnt

Reg. 0xA00A10E8

register used to return the count of frames received out of order

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected segment of frames with pkt seq error |

### 1.9.44 diag_data_sop_err_cnt

Reg. 0xA00A10EC

register used to return the count of sop errors received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected sop not set on 1st pkt or set on last pkt |

### 1.9.45 diag_data_eop_err_cnt

Reg. 0xA00A10F0

register used to return the count of eop err received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected eop not set on last pkt |

### 1.9.46 diag_data_seg_out_of_order_cnt

Reg. 0xA00A10F4

register used to return the count of frames received out of order

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected segment of frames with pkt seq error |

### 1.9.47 amp_wfm_samp_sop_err_cnt

Reg. 0xA00A10F8

register used to return the count of sop errors received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected sop not set on 1st pkt or set on last pkt |

### 1.9.48 amp_wfm_samp_eop_err_cnt

Reg. 0xA00A10FC

register used to return the count of eop err received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected eop not set on last pkt |

### 1.9.49 amp_wfm_samp_seg_out_of_order_cnt

Reg. 0xA00A1100

register used to return the count of frames received out of order

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected segment of frames with pkt seq error |

### 1.9.50 vol_wfm_samp_sop_err_cnt

Reg. 0xA00A1104

register used to return the count of sop errors received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected sop not set on 1st pkt or set on last pkt |

### 1.9.51 vol_wfm_samp_eop_err_cnt

Reg. 0xA00A1108

register used to return the count of eop err received

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | err_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected eop not set on last pkt |

### 1.9.52 vol_wfm_samp_seg_out_of_order_cnt

Reg. 0xA00A110C

register used to return the count of frames received out of order

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | rx_cnt | rw | na | 0x0 | +1 => the fsm that recives the data, detected segment of frames with pkt seq error |

### 1.10 ipi_scratchpad

Block 0xA00C0000 - 0xA00FFFFF

Scratchpad RAM

### 1.10.1 ram_256kb_inst

ram_256kb_inst 0xA00C0000, 0xA00C0004 ... 0xA00FFFFF

| offset | | depth | 65536 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

### 1.11 esm_common_registers

Block 0xA0210000 - 0xA021171F

Register map used for ESMI_IF access

### 1.11.1 esmi_ctl1

Reg. 0xA0210000

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode |

| | | |
|---|---|---|
| enc2 | 2 | Reserved |
| enc3 | 3 | Reserved |

### 1.11.2 esmi_cmd1

Reg. 0xA0210004

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.3 esmi_32dat1

Reg. 0xA0210008

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |

| | | | | | |
|---|---|---|---|---|---|
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.4 esmi_tdly1

Reg. 0xA021000C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.5 esmi_fncmd1

Reg. 0xA0210014

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.6 esmi_iacmd1

Reg. 0xA0210018

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type: |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | 0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.7 esmi_extdat1

Reg. 0xA021001C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.8 esmi_ctl2

Reg. 0xA0210030

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |

| | | | | | |
|---|---|---|---|---|---|
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

### 1.11.9 esmi_cmd2

Reg. 0xA0210034

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 a |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | re 'don't c ares' for a read opera tion |
| | | | | | enc1 \| 1 \| Register wr ite |
| | | | | | enc2 \| 2 \| Tref with w ave sync (W aveform Cap ture) comma nd |
| | | | | | enc3 \| 3 \| Tref, no wa ve sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.10 esmi_32dat2

Reg. 0xA0210038

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br>enum:esmi_dat_t_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Framing or CRC error<br>enc5 \| 5 \| SPM cable n ot connecte d<br>enc8 \| 8 \| Normal, val id data<br>encE \| 14 \| ESM cable n |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ot connected |
| | | | | | encF 15 Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.11 esmi_tdly2

Reg. 0xA021003C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.12 esmi_fncmd2

Reg. 0xA0210044

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.13 esmi_iacmd2

Reg. 0xA0210048

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.14 esmi_extdat2

Reg. 0xA021004C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |

| | | | | | |
|---|---|---|---|---|---|
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.15 esmi_ctl3

Reg. 0xA0210060

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 o |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | peration (T 0 used as s ource)<br>enc1 \| 1 \| Reserved us ed by CTEC Operation<br>enc2 \| 2 \| normal MAP4 operation (droplet de tection use d as source )<br>enc3 \| 3 \| enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br>enum:esm_ctl_m_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Port disabl ed - No err ors will be reported; Energy will be set to zero<br>enc1 \| 1 \| Normal ESM mode<br>enc2 \| 2 \| Reserved<br>enc3 \| 3 \| Reserved |

## 1.11.16 esmi_cmd3

Reg.

0xA0210064

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br>enum:esmi_cmd_c_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion<br>enc1 \| 1 \| Register wr ite<br>enc2 \| 2 \| Tref with w ave sync (W aveform Cap ture) comma nd<br>enc3 \| 3 \| Tref, no wa ve sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.17 esmi_32dat3

Reg. 0xA0210068

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.18 esmi_tdly3

Reg. 0xA021006C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.19 esmi_fncmd3

Reg. 0xA0210074

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.20 esmi_iacmd3

Reg. 0xA0210078

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.21 esmi_extdat3

Reg. 0xA021007C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.22 esmi_ctl4

Reg. 0xA0210090

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.

The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source) |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc3 \| 3 \| enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br>enum:esm_ctl_m_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 \| 1 \| Normal ESM mode<br>enc2 \| 2 \| Reserved<br>enc3 \| 3 \| Reserved |

### 1.11.23 esmi_cmd4

Reg. 0xA0210094

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br>enum:esmi_cmd_c_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 \| 1 \| Register write<br>enc2 \| 2 \| Tref with wave sync (Waveform Capture) command<br>enc3 \| 3 \| Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.24 esmi_32dat4

Reg. 0xA0210098

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |

| | | | | | |
|---|---|---|---|---|---|
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.25 esmi_tdly4

Reg. 0xA021009C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.26 esmi_fncmd4

Reg. 0xA02100A4

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.27 esmi_iacmd4

Reg. 0xA02100A8

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.28 esmi_extdat4

Reg. 0xA02100AC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.29 esmi_ctl5

Reg. 0xA02100C0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabl |

| | | |
|---|---|---|
| | | ed - No errors will be reported; Energy will be set to zero |
| enc1 | 1 | Normal ESM mode |
| enc2 | 2 | Reserved |
| enc3 | 3 | Reserved |

### 1.11.30 esmi_cmd5

Reg. 0xA02100C4

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.31 esmi_32dat5

Reg. 0xA02100C8

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |

| | | | | | |
|---|---|---|---|---|---|
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.32 esmi_tdly5

Reg. 0xA02100CC

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.33 esmi_fncmd5

Reg. 0xA02100D4

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |

| | | | | | |
|---|---|---|---|---|---|
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.34 esmi_iacmd5

Reg. 0xA02100D8

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.35 esmi_extdat5

Reg. 0xA02100DC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.36 esmi_ctl6

Reg. 0xA02100F0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |

| | | | | | |
|---|---|---|---|---|---|
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.37 esmi_cmd6

Reg.

0xA02100F4

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.38 esmi_32dat6

Reg. 0xA02100F8

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Name: enc0, Value: 0, Description: Framing or CRC error<br>Name: enc5, Value: 5, Description: SPM cable not connected<br>Name: enc8, Value: 8, Description: Normal, valid data<br>Name: encE, Value: 14, Description: ESM cable not connected<br>Name: encF, Value: 15, Description: Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.39 esmi_tdly6

Reg. 0xA02100FC

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.40 esmi_fncmd6

Reg. 0xA0210104

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.41 esmi_iacmd6

Reg. 0xA0210108

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.42 esmi_extdat6

Reg. 0xA021010C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.43 esmi_ctl7

Reg. 0xA0210120

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |

| | | | | | |
|---|---|---|---|---|---|
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.44 esmi_cmd7

Reg. 0xA0210124

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (W |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | aveform Capture) command |
| | | | | | enc3 \| 3 \| Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.45 esmi_32dat7

Reg. 0xA0210128

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Framing or CRC error<br>enc5 \| 5 \| SPM cable not connected<br>enc8 \| 8 \| Normal, valid data<br>encE \| 14 \| ESM cable not connected<br>encF \| 15 \| Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.46 esmi_tdly7

Reg. 0xA021012C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.47 esmi_fncmd7

Reg. 0xA0210134

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.48 esmi_iacmd7

Reg. 0xA0210138

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.49 esmi_extdat7

Reg. 0xA021013C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

## 1.11.50 esmi_ctl8

Reg. | 0xA0210150

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | operation (droplet detection used as source) |
| | | | | | enc3 \| 3 \| enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 \| 1 \| Normal ESM mode<br>enc2 \| 2 \| Reserved<br>enc3 \| 3 \| Reserved |

## 1.11.51 esmi_cmd8

Reg. 0xA0210154

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 \| 1 \| Register write<br>enc2 \| 2 \| Tref with wave sync (Waveform Capture) command<br>enc3 \| 3 \| Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.52 esmi_32dat8

Reg. 0xA0210158

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |

| | | | | | |
|---|---|---|---|---|---|
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.53 esmi_tdly8

Reg. 0xA021015C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.54 esmi_fncmd8

Reg. 0xA0210164

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.55 esmi_iacmd8

Reg. 0xA0210168

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.56 esmi_extdat8

Reg. 0xA021016C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.57 esmi_ctl9

Reg. 0xA0210180

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |

| | | | | | |
|---|---|---|---|---|---|
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.58 esmi_cmd9

Reg. 0xA0210184

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.59 esmi_32dat9

Reg. 0xA0210188

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |

| | | | | | |
|---|---|---|---|---|---|
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.60 esmi_tdly9

Reg. 0xA021018C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

## 1.11.61 esmi_fncmd9

Reg. 0xA0210194

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |

| | | | | | |
|---|---|---|---|---|---|
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.62 esmi_iacmd9

Reg. 0xA0210198

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.63 esmi_extdat9

Reg. 0xA021019C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.64 esmi_ctl10

Reg. 0xA02101B0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

### 1.11.65 esmi_cmd10

Reg. 0xA02101B4

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.66 esmi_32dat10

Reg. 0xA02101B8

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |

| | | | | | |
|---|---|---|---|---|---|
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.67 esmi_tdly10

Reg. 0xA02101BC

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

## 1.11.68 esmi_fncmd10

Reg. 0xA02101C4

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

## 1.11.69 esmi_iacmd10

Reg. 0xA02101C8

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |

| | | | | | |
|---|---|---|---|---|---|
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.70 esmi_extdat10

Reg. 0xA02101CC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.71 esmi_ctl11

Reg. 0xA02101E0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |

| | | | | | |
|---|---|---|---|---|---|
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.72 esmi_cmd11

Reg.

0xA02101E4

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | read operation |
| | | | | | enc1 \| 1 \| Register write |
| | | | | | enc2 \| 2 \| Tref with wave sync (Waveform Capture) command |
| | | | | | enc3 \| 3 \| Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.73 esmi_32dat11

Reg. 0xA02101E8

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Framing or CRC error<br>enc5 \| 5 \| SPM cable not connected<br>enc8 \| 8 \| Normal, valid data<br>encE \| 14 \| ESM cable not connected |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | encF 15 Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.74 esmi_tdly11

Reg. 0xA02101EC

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

## 1.11.75 esmi_fncmd11

Reg. 0xA02101F4

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

## 1.11.76 esmi_iacmd11

Reg. 0xA02101F8

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

## 1.11.77 esmi_extdat11

Reg. 0xA02101FC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read OR |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

## 1.11.78 esmi_ctl12

Reg. 0xA0210210

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as s |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ource) |
| | | | | | enc1 \| 1 \| Reserved used by CTEC Operation<br>enc2 \| 2 \| normal MAP4 operation (droplet detection used as source)<br>enc3 \| 3 \| enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 \| 1 \| Normal ESM mode<br>enc2 \| 2 \| Reserved<br>enc3 \| 3 \| Reserved |

## 1.11.79 esmi_cmd12

Reg. 0xA0210214

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 \| 1 \| Register write<br>enc2 \| 2 \| Tref with wave sync (Waveform Capture) command<br>enc3 \| 3 \| Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.80 esmi_32dat12

Reg. 0xA0210218

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.81 esmi_tdly12

Reg. 0xA021021C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of

this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.82 esmi_fncmd12

Reg. 0xA0210224

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.83 esmi_iacmd12

Reg. 0xA0210228

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.84 esmi_extdat12

Reg. 0xA021022C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.85 esmi_ctl13

Reg. 0xA0210240

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |

| | | | | | |
|---|---|---|---|---|---|
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.86 esmi_cmd13

Reg. 0xA0210244

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.87 esmi_32dat13

Reg. 0xA0210248

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |

| | | | | | |
|---|---|---|---|---|---|
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.88 esmi_tdly13

Reg. 0xA021024C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

## 1.11.89 esmi_fncmd13

Reg. 0xA0210254

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |

| | | | | | |
|---|---|---|---|---|---|
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.90 esmi_iacmd13

Reg. 0xA0210258

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.91 esmi_extdat13

Reg. 0xA021025C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.92 esmi_ctl14

Reg. 0xA0210270

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode |

| | | |
|---|---|---|
| enc2 | 2 | Reserved |
| enc3 | 3 | Reserved |

## 1.11.93 esmi_cmd14

Reg. 0xA0210274

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.94 esmi_32dat14

Reg. 0xA0210278

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |

| | | | | | |
|---|---|---|---|---|---|
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.95 esmi_tdly14

Reg. 0xA021027C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

## 1.11.96 esmi_fncmd14

Reg. 0xA0210284

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

## 1.11.97 esmi_iacmd14

Reg. 0xA0210288

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type: |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | 0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.98 esmi_extdat14

Reg. 0xA021028C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.99 esmi_ctl15

Reg. 0xA02102A0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |

| | | | | | |
|---|---|---|---|---|---|
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.100 esmi_cmd15

Reg. 0xA02102A4

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 a |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | re 'don't c ares' for a read opera tion |
| | | | | | enc1 \| 1 \| Register wr ite |
| | | | | | enc2 \| 2 \| Tref with w ave sync (W aveform Cap ture) comma nd |
| | | | | | enc3 \| 3 \| Tref, no wa ve sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.101 esmi_32dat15

Reg. 0xA02102A8

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Framing or CRC error<br>enc5 \| 5 \| SPM cable n ot connecte d<br>enc8 \| 8 \| Normal, val id data<br>encE \| 14 \| ESM cable n |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ot connected |
| | | | | | encF 15 Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.102 esmi_tdly15

Reg. 0xA02102AC

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.103 esmi_fncmd15

Reg. 0xA02102B4

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.104 esmi_iacmd15

Reg. 0xA02102B8

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.105 esmi_extdat15

Reg. 0xA02102BC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |

| | | | | | |
|---|---|---|---|---|---|
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.106 esmi_ctl16

Reg. 0xA02102D0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 o |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | peration (T 0 used as s ource)<br>enc1 \| 1 \| Reserved us ed by CTEC Operation<br>enc2 \| 2 \| normal MAP4 operation (droplet de tection use d as source )<br>enc3 \| 3 \| enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br>enum:esm_ctl_m_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Port disabl ed - No err ors will be reported; Energy will be set to zero<br>enc1 \| 1 \| Normal ESM mode<br>enc2 \| 2 \| Reserved<br>enc3 \| 3 \| Reserved |

## 1.11.107 esmi_cmd16

Reg.

0xA02102D4

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br>enum:esmi_cmd_c_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion<br>enc1 \| 1 \| Register wr ite<br>enc2 \| 2 \| Tref with w ave sync (W aveform Cap ture) comma nd<br>enc3 \| 3 \| Tref, no wa ve sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.108 esmi_32dat16

Reg. 0xA02102D8

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.109 esmi_tdly16

Reg. 0xA02102DC

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.110 esmi_fncmd16

Reg. 0xA02102E4

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.111 esmi_iacmd16

Reg. 0xA02102E8

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.112 esmi_extdat16

Reg. 0xA02102EC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.113 esmi_ctl17

Reg. 0xA0210300

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.

The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source) |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc3 \| 3 \| enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 \| 1 \| Normal ESM mode<br>enc2 \| 2 \| Reserved<br>enc3 \| 3 \| Reserved |

### 1.11.114 esmi_cmd17

Reg. 0xA0210304

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 \| 1 \| Register write<br>enc2 \| 2 \| Tref with wave sync (Waveform Capture) command<br>enc3 \| 3 \| Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.115 esmi_32dat17

Reg. 0xA0210308

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |

| | | | | | |
|---|---|---|---|---|---|
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.116 esmi_tdly17

Reg. 0xA021030C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.117 esmi_fncmd17

Reg. 0xA0210314

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.118 esmi_iacmd17

Reg. 0xA0210318

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.119 esmi_extdat17

Reg. 0xA021031C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.120 esmi_ctl18

Reg. 0xA0210330

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabl |

| | | |
|---|---|---|
| | | ed - No errors will be reported; Energy will be set to zero |
| enc1 | 1 | Normal ESM mode |
| enc2 | 2 | Reserved |
| enc3 | 3 | Reserved |

### 1.11.121 esmi_cmd18

Reg. 0xA0210334

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Register Read. D7:D0 are 'don't cares' for a read operation |
| enc1 | 1 | Register write |
| enc2 | 2 | Tref with wave sync (Waveform Capture) command |
| enc3 | 3 | Tref, no wave sync |

| | | | | | |
|---|---|---|---|---|---|
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

### 1.11.122 esmi_32dat18

Reg. 0xA0210338

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |

| | | | | | |
|---|---|---|---|---|---|
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.123 esmi_tdly18

Reg. 0xA021033C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

## 1.11.124 esmi_fncmd18

Reg. 0xA0210344

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |

| | | | | | |
|---|---|---|---|---|---|
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.125 esmi_iacmd18

Reg. 0xA0210348

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.126 esmi_extdat18

Reg. 0xA021034C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.127 esmi_ctl19

Reg. 0xA0210360

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |

| | | | | | |
|---|---|---|---|---|---|
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.128 esmi_cmd19

Reg.

0xA0210364

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (Waveform Capture) command<br>enc3 / 3 / Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.129 esmi_32dat19

Reg. 0xA0210368

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Name: enc0, Value: 0, Description: Framing or CRC error<br>Name: enc5, Value: 5, Description: SPM cable not connected<br>Name: enc8, Value: 8, Description: Normal, valid data<br>Name: encE, Value: 14, Description: ESM cable not connected<br>Name: encF, Value: 15, Description: Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.130 esmi_tdly19

Reg. 0xA021036C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.131 esmi_fncmd19

Reg. 0xA0210374

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.132 esmi_iacmd19

Reg. 0xA0210378

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.133 esmi_extdat19

Reg. 0xA021037C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.134 esmi_ctl20

Reg. 0xA0210390

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words.
The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM_CMD register. The data returned from an ESM register read is available in the ESM_DAT register.
To write to an ESMI register that is not a funtion parameter, load ESM_CMD with
[C1:C0] = [0:1]
[A5:A0] = Address of ESM register to be written to
[D7:D0] = Data byte to be written to the byte wide register
Example:
To access the ESM's test register at ESM address 0x08:
Address Data
ESMI_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)
The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers
1) metric parameters
2) all other registers
The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.
Example:
If you want to write to any of the parameters affecting Function 1, you would write:
Address Data
ESMI_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)
ESMI_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)
ESMI_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)
Writes and reads to/from ESM registers are unrestricted when the TEM_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15 | ce | ro | wo | 0x0 | Flags a bad CRC on the latest received message. 1 = error |
| 14 | fe | ro | wo | 0x0 | Flags a framing error on the latest received message. 1 = error |
| 13 | iatmo | rw | wo | 0x0 | 1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally. |
| 12 | iardy | ro | wo | 0x0 | 1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored. |
| 11 | iarx | ro | wo | 0x0 | 1 = Indirect address read complete. 0 = Indirect read in progress. |
| 10 | to | rw | ro | 0x0 | Enables tref overide : used to ignore TREF signal to allow multiple read/writes |
| 9 | rx | ro | wo | 0x0 | Indicates when a receive message is in the ESM_DAT register. 1 = message available |
| 8 | tx | ro | wo | 0x0 | Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed. |
| 7 | es | rw | rw | 0x0 | Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample |

| | | | | | |
|---|---|---|---|---|---|
| 6:5 | tr | rw | ro | 0x0 | Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.<br><br>enum:esm_ctl_tr_encoding<br>Name / Value / Description<br>enc0 / 0 / normal T0 operation (T0 used as source)<br>enc1 / 1 / Reserved used by CTEC Operation<br>enc2 / 2 / normal MAP4 operation (droplet detection used as source)<br>enc3 / 3 / enhanced MAP4 operation (HOP mode - see MAP4 HOP register below) |
| 4 | fa | rw | ro | 0x0 | The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register. |
| 1:0 | m1_m0 | rw | ro | 0x1 | Mode bits set the operating mode for this RJ45 port.<br><br>enum:esm_ctl_m_encoding<br>Name / Value / Description<br>enc0 / 0 / Port disabled - No errors will be reported; Energy will be set to zero<br>enc1 / 1 / Normal ESM mode<br>enc2 / 2 / Reserved<br>enc3 / 3 / Reserved |

## 1.11.135 esmi_cmd20

Reg. 0xA0210394

The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:14 | c1_c0 | rw | ro | 0x0 | ESM/BPAM Command Type<br><br>enum:esmi_cmd_c_encoding<br>Name / Value / Description<br>enc0 / 0 / Register Read. D7:D0 are 'don't cares' for a read operation<br>enc1 / 1 / Register write<br>enc2 / 2 / Tref with wave sync (W |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | aveform Capture) command<br>enc3 3 Tref, no wave sync |
| 13:8 | a5_a0 | rw | ro | 0x0 | ESM Register Address |
| 7:0 | d7_d0 | rw | ro | 0x0 | ESM Optional Write Data Field |

## 1.11.136 esmi_32dat20

Reg. 0xA0210398

The bottom 16 bits of this register are a mirror of esmi_dat

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | ce3 | ro | wo | 0x0 | 1 = CRC error on highest received byte (BPAM indirect register read) |
| 30 | ce2 | ro | wo | 0x0 | 1 = CRC error on high received byte (BPAM indirect register read) |
| 29 | ce1 | ro | wo | 0x0 | 1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read) |
| 28 | ce0 | ro | wo | 0x0 | 1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 27 | fe3 | ro | wo | 0x0 | 1 = Frame error (timeout) on highest received byte (BPAM indirect register read) |
| 26 | fe2 | ro | wo | 0x0 | 1 = Frame error (timeout) on high received byte (BPAM indirect register read) |
| 25 | fe1 | ro | wo | 0x0 | 1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read) |
| 24 | fe0 | ro | wo | 0x0 | 1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read) |
| 23 | rx3 | ro | wo | 0x0 | 1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read) |
| 22 | rx2 | ro | wo | 0x0 | 1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read) |
| 21 | rx1 | ro | wo | 0x0 | 1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read) |
| 20 | rx0 | ro | wo | 0x0 | 1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)<br>or<br>1 = byte received in ESM_DAT[7:0] without error (direct register read) |
| 17 | txfe | ro | wo | 0x0 | 1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command. |
| 16 | tx8e | ro | wo | 0x0 | 1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions. |
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.137 esmi_tdly20

Reg. 0xA021039C

The ESM_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.
Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.
ESM_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | esm_tdly | rw | ro | 0x21 | 16-bit value for TDLY. Min 0x21. 8ns resolution. |

### 1.11.138 esmi_fncmd20

Reg. 0xA02103A4

This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 28 | fnc | rw | ro | 0x0 | ESM/BPAM FN Command type:<br>0 = FN parameter read<br>1 = FN parameter write |
| 27:26 | f1_f0 | rw | ro | 0x0 | FN access type:<br>10 = FN1 access (FN + 1 parameter byte)<br>11 = FN2 access (FN + 2 parameter bytes)<br>others = reserved |
| 25:22 | fn3_fn0 | rw | ro | 0x0 | ESM/BPAM Function Number to be accessed |
| 21:16 | fa5_fa0 | rw | ro | 0x0 | ESM/BPAM start direct address for the FN parameter |
| 15:8 | fd15_fd8 | rw | ro | 0x0 | ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access |
| 7:0 | fd7_fd0 | rw | ro | 0x0 | ESM/BPAM FN parameter low byte (FN2 or FN1 access) |

### 1.11.139 esmi_iacmd20

Reg. 0xA02103A8

This register contains the read/write access to indirect registers in BPAM.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 14 | iac | rw | ro | 0x0 | BPAM Indirect addressing Command type:<br>0 = Indirect register read<br>1 = Indirect register write |
| 13:0 | ia15_ia2 | rw | ro | 0x0 | BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero |

### 1.11.140 esmi_extdat20

Reg. 0xA02103AC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:24 | id31_id24 | rw | rw | 0x0 | highest byte data [31:24] for BPAM indirect register write or read |
| 23:16 | id23_id16 | rw | rw | 0x0 | high byte data [23:16] for BPAM indirect register write or read |
| 15:8 | ifd15_ifd8 | rw | rw | 0x0 | low byte data [15:8] for BPAM indirect register write or read<br>OR<br>low byte data [15:8] for FN2 parameter read |
| 7:0 | ifd7_ifd0 | rw | rw | 0x0 | lowest byte data [7:0] for BPAM indirect register write or read<br>OR<br>lowest byte data [7:0] for FN2 or FN1 parameter read |

### 1.11.141 esmi_crc

Reg. 0xA0210700

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 19:0 | esmi_crc | ro | wo | 0x0 | Latched CRC error indication for each of the twenty ESMs. Any CRC error detected on the associated ESM-to-xTEC link is latched in its bit position. All latched bits are cleared via the CR bit in the RESETS register. |

### 1.11.142 esmi_crc_sel

Reg. 0xA0210704

ESM CRC Error Select Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 4:0 | sel | rw | ro | 0x0 | Selects one of the 20 ESMs to source the CRC monitoring for the ESM_CRC_CNT. |

### 1.11.143 esmi_crc_cnt

Reg. 0xA0210708

ESM CRC Error Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 9:0 | cnt | ro | wo | 0x0 | CRC error count. The count increments with each CRC error detected on the ESM-to-xTEC link selected by ESM_CRC_SEL. The count freezes at 1,023, and is cleared via the CR bit in the RESETS register. |

### 1.11.144 esmi_cab

Reg. 0xA0210710

Indicates the status of the ESM cable connections for each of the twenty ESMs.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 19:0 | esmi_cab | ro | wo | 0x0 | ESM cable connect flag for each of the 20 ESMs. 1 is cable connected. |

### 1.11.145 spm_cab

Reg. 0xA0210714

Indicates the status of the cable connection for SPM to its respective ESMs. One bit per ESM/SPM channel.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 19:0 | spm_cab | ro | wo | 0x0 | SPM/CSPM cable connect flag for ESMs[20:1]. 1= cable connected |

### 1.11.146 t9_esmi

Reg. 0xA0210718

This register indicates that an invalid (outdated T9) version device for each of the ESM is connected. When T9 ESM is detected, the ESM_CAB flag will be set to zero. There could be up to three seconds delay once the cable is inserted.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 19:0 | t9_esmi | ro | wo | 0x0 | T9_ESM connect flags for each of the eight ESMs. 1=T9 (outdated, incompatible) ESM is connected. |

### 1.11.147 nrgy_a1

Reg. 0xA0210800

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.148 pkamp_a1_pktime_a1

Reg.

0xA0210804

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

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document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM framing |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | error or n o reply |
| | | | | | enc3 3 CRC error o n reply dat a from ESM/ xPAM |
| | | | | | enc4 4 SPM not con nected to E SM/xPAM |
| | | | | | enc5 5 ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 6 ESM/xPAM Da ta not vali d |
| | | | | | enc8 8 BPAM Extend ed: warning condition |
| | | | | | encF 15 ESM/xPAM po wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.149 nrgy_b1

Reg.

0xA0210808

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | d |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.150 pkamp_b1_pktime_b1

Reg.

0xA021080C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |
| | | | | | Name \| Value \| Description |
| | | | | | enc0 \| 0 \| Normal Energy or ESM/xPAM disabled |
| | | | | | enc1 \| 1 \| ESM/xPAM cable not connected |
| | | | | | enc2 \| 2 \| ESM framing error or no reply |
| | | | | | enc3 \| 3 \| CRC error on reply data from ESM/xPAM |
| | | | | | enc4 \| 4 \| SPM not connected to ESM/xPAM |
| | | | | | enc5 \| 5 \| ESM/xPAM ADC overload during integration |
| | | | | | enc6 \| 6 \| ESM/xPAM Data not valid |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.151 nrgy_c1

Reg.

0xA0210810

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.152 pkamp_c1_pktime_c1

Reg. 0xA0210814

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.153 nrgy_a2

Reg. 0xA0210818

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | during integration |
| | | | | enc6 | 6 ESM/xPAM Data not valid |
| | | | | enc8 | 8 BPAM Extended: warning condition |
| | | | | encF | 15 ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.154 pkamp_a2_pktime_a2

Reg. 0xA021081C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |
| | | | | | Name / Value / Description |
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled |
| | | | | | enc1 / 1 / ESM/xPAM cable not connected |
| | | | | | enc2 / 2 / ESM framing error or no reply |
| | | | | | enc3 / 3 / CRC error on reply data from ESM/xPAM |
| | | | | | enc4 / 4 / SPM not connected to ESM/xPAM |
| | | | | | enc5 / 5 / ESM/xPAM ADC overload during integration |
| | | | | | enc6 / 6 / ESM/xPAM Data not valid |
| | | | | | enc8 / 8 / BPAM Extended: warning condition |
| | | | | | encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.155 nrgy_b2

Reg. 0xA0210820

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.156 pkamp_b2_pktime_b2

Reg. 0xA0210824

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.157 nrgy_c2

Reg. 0xA0210828

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not con |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | nected to E SM/xPAM |
| | | | | enc5 | 5 ESM/xPAM AD C overload during inte gration |
| | | | | enc6 | 6 ESM/xPAM Da ta not vali d |
| | | | | enc8 | 8 BPAM Extend ed: warning condition |
| | | | | encF | 15 ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.158 pkamp_c2_pktime_c2

Reg.

0xA021082C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |
| encF | 15 | ESM/xPAM po wer up stat e |

| | | | | | |
|---|---|---|---|---|---|
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |

| | | | | | |
|---|---|---|---|---|---|
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.159 nrgy_a3

Reg. 0xA0210830

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

## 1.11.160 pkamp_a3_pktime_a3

Reg. 0xA0210834

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.161 nrgy_b3

Reg.

0xA0210838

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error o |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | n reply dat a from ESM/ xPAM |
| | | | | | enc4 4 SPM not con nected to E SM/xPAM |
| | | | | | enc5 5 ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 6 ESM/xPAM Da ta not vali d |
| | | | | | enc8 8 BPAM Extend ed: warning condition |
| | | | | | encF 15 ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.162 pkamp_b3_pktime_b3

Reg. 0xA021083C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |
| encF | 15 | ESM/xPAM po |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.163 nrgy_c3

Reg. 0xA0210840

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.164 pkamp_c3_pktime_c3

Reg. 0xA0210844

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.165 nrgy_a4

Reg. 0xA0210848

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.166 pkamp_a4_pktime_a4

Reg.

0xA021084C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extend |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ed: warning condition |
| | | | | | encF 15 ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.167 nrgy_b4

Reg. 0xA0210850

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.168 pkamp_b4_pktime_b4

Reg. 0xA0210854

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.169 nrgy_c4

Reg.

0xA0210858

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not con |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | nected |
| | | | | | enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| | | | | | enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| | | | | | enc4 | 4 | SPM not con nected to E SM/xPAM |
| | | | | | enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 | 6 | ESM/xPAM Da ta not vali d |
| | | | | | enc8 | 8 | BPAM Extend ed: warning condition |
| | | | | | encF | 15 | ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value | | |

### 1.11.170 pkamp_c4_pktime_c4

Reg.

0xA021085C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ta not vali<br>d |
| | | | | | enc8 \| 8 \| BPAM Extend<br>ed: warning<br>condition |
| | | | | | encF \| 15 \| ESM/xPAM po<br>wer up stat<br>e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.171 nrgy_a5

Reg.

0xA0210860

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Normal Ener<br>gy or ESM/x<br>PAM disable<br>d<br>enc1 \| 1 \| ESM/xPAM ca<br>ble not con<br>nected<br>enc2 \| 2 \| ESM/xPAM fr<br>aming error<br>or no repl<br>y<br>enc3 \| 3 \| CRC error o<br>n reply dat<br>a from ESM/<br>xPAM<br>enc4 \| 4 \| SPM not con<br>nected to E<br>SM/xPAM<br>enc5 \| 5 \| ESM/xPAM AD<br>C overload<br>during inte<br>gration<br>enc6 \| 6 \| ESM/xPAM Da<br>ta not vali<br>d<br>enc8 \| 8 \| BPAM Extend<br>ed: warning<br>condition<br>encF \| 15 \| ESM/xPAM po<br>wer up stat<br>e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.172 pkamp_a5_pktime_a5

Reg.

0xA0210864

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.173 nrgy_b5

Reg.

0xA0210868

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.174 pkamp_b5_pktime_b5

Reg.

0xA021086C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to E |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | SM/xPAM |
| | | | | | enc5 \| 5 \| ESM/xPAM ADC overload during integration |
| | | | | | enc6 \| 6 \| ESM/xPAM Data not valid |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.175 nrgy_c5

Reg.

0xA0210870

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Normal Energy or ESM/xPAM disabled<br>enc1 \| 1 \| ESM/xPAM cable not connected<br>enc2 \| 2 \| ESM/xPAM framing error or no repl y<br>enc3 \| 3 \| CRC error on reply data from ESM/xPAM<br>enc4 \| 4 \| SPM not connected to ESM/xPAM<br>enc5 \| 5 \| ESM/xPAM ADC overload during integration<br>enc6 \| 6 \| ESM/xPAM Data not valid<br>enc8 \| 8 \| BPAM Extended: warning condition<br>encF \| 15 \| ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.176 pkamp_c5_pktime_c5

Reg. 0xA0210874

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.177 nrgy_a6

Reg. 0xA0210878

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.178 pkamp_a6_pktime_a6

Reg. 0xA021087C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM framing error or no reply |
| enc3 | 3 | CRC error on reply dat |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | a from ESM/ xPAM |
| | | | | | enc4 4 SPM not con nected to E SM/xPAM |
| | | | | | enc5 5 ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 6 ESM/xPAM Da ta not vali d |
| | | | | | enc8 8 BPAM Extend ed: warning condition |
| | | | | | encF 15 ESM/xPAM po wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.179 nrgy_b6

Reg.

0xA0210880

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | encF 15 ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.180 pkamp_b6_pktime_b6

Reg. 0xA0210884

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.181 nrgy_c6

Reg. 0xA0210888

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.182 pkamp_c6_pktime_c6

Reg. 0xA021088C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM framing |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | error or n o reply |
| | | | | enc3 | 3 CRC error o n reply dat a from ESM/ xPAM |
| | | | | enc4 | 4 SPM not con nected to E SM/xPAM |
| | | | | enc5 | 5 ESM/xPAM AD C overload during inte gration |
| | | | | enc6 | 6 ESM/xPAM Da ta not vali d |
| | | | | enc8 | 8 BPAM Extend ed: warning condition |
| | | | | encF | 15 ESM/xPAM po wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.183 nrgy_a7

Reg.

0xA0210890

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | d |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.184 pkamp_a7_pktime_a7

Reg.

0xA0210894

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |
| | | | | | Name \| Value \| Description |
| | | | | | enc0 \| 0 \| Normal Energy or ESM/xPAM disabled |
| | | | | | enc1 \| 1 \| ESM/xPAM cable not connected |
| | | | | | enc2 \| 2 \| ESM framing error or no reply |
| | | | | | enc3 \| 3 \| CRC error on reply data from ESM/xPAM |
| | | | | | enc4 \| 4 \| SPM not connected to ESM/xPAM |
| | | | | | enc5 \| 5 \| ESM/xPAM ADC overload during integration |
| | | | | | enc6 \| 6 \| ESM/xPAM Data not valid |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.185 nrgy_b7

Reg.

0xA0210898

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.186 pkamp_b7_pktime_b7

Reg. 0xA021089C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.187 nrgy_c7

Reg. 0xA02108A0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | during integration |
| | | | | enc6 | 6 ESM/xPAM Data not valid |
| | | | | enc8 | 8 BPAM Extended: warning condition |
| | | | | encF | 15 ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.188 pkamp_c7_pktime_c7

Reg.

0xA02108A4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |
| | | | | | Name / Value / Description |
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled |
| | | | | | enc1 / 1 / ESM/xPAM cable not connected |
| | | | | | enc2 / 2 / ESM framing error or no reply |
| | | | | | enc3 / 3 / CRC error on reply data from ESM/xPAM |
| | | | | | enc4 / 4 / SPM not connected to ESM/xPAM |
| | | | | | enc5 / 5 / ESM/xPAM ADC overload during integration |
| | | | | | enc6 / 6 / ESM/xPAM Data not valid |
| | | | | | enc8 / 8 / BPAM Extended: warning condition |
| | | | | | encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.189 nrgy_a8

Reg. 0xA02108A8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

## 1.11.190 pkamp_a8_pktime_a8

Reg. 0xA02108AC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.191 nrgy_b8

Reg. 0xA02108B0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not con |

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td>
<table>
<tr><td></td><td></td><td>nected to E SM/xPAM</td></tr>
<tr><td>enc5</td><td>5</td><td>ESM/xPAM AD C overload during inte gration</td></tr>
<tr><td>enc6</td><td>6</td><td>ESM/xPAM Da ta not vali d</td></tr>
<tr><td>enc8</td><td>8</td><td>BPAM Extend ed: warning condition</td></tr>
<tr><td>encF</td><td>15</td><td>ESM/xPAM po wer up stat e</td></tr>
</table>
</td></tr>
<tr><td>23:0</td><td>e</td><td>ro</td><td>wo</td><td>0x0</td><td>24-bit energy value</td></tr>
</table>

## 1.11.192 pkamp_b8_pktime_b8

Reg.

0xA02108B4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

<table>
<tr><th>bits</th><th>name</th><th>s/w</th><th>h/w</th><th>default</th><th>description</th></tr>
<tr><td>31:28</td><td>f</td><td>ro</td><td>wo</td><td>0x0</td><td>
enum:esm_status_pkamp_encoding
<table>
<tr><th>Name</th><th>Value</th><th>Description</th></tr>
<tr><td>enc0</td><td>0</td><td>Normal Ener gy or ESM/x PAM disable d</td></tr>
<tr><td>enc1</td><td>1</td><td>ESM/xPAM ca ble not con nected</td></tr>
<tr><td>enc2</td><td>2</td><td>ESM framing error or n o reply</td></tr>
<tr><td>enc3</td><td>3</td><td>CRC error o n reply dat a from ESM/ xPAM</td></tr>
<tr><td>enc4</td><td>4</td><td>SPM not con nected to E SM/xPAM</td></tr>
<tr><td>enc5</td><td>5</td><td>ESM/xPAM AD C overload during inte gration</td></tr>
<tr><td>enc6</td><td>6</td><td>ESM/xPAM Da ta not vali d</td></tr>
<tr><td>enc8</td><td>8</td><td>BPAM Extend ed: warning condition</td></tr>
<tr><td>encF</td><td>15</td><td>ESM/xPAM po wer up stat e</td></tr>
</table>
</td></tr>
<tr><td>27:16</td><td>pkamp</td><td>ro</td><td>wo</td><td>0x0</td><td>12-bit amplitude value</td></tr>
</table>

| | | | | | |
|---|---|---|---|---|---|
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.193 nrgy_c8

Reg. 0xA02108B8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

## 1.11.194 pkamp_c8_pktime_c8

Reg. 0xA02108BC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.195 nrgy_a9

Reg. 0xA02108C0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error o |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | n reply dat a from ESM/ xPAM |
| | | | | | enc4 4 SPM not con nected to E SM/xPAM |
| | | | | | enc5 5 ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 6 ESM/xPAM Da ta not vali d |
| | | | | | enc8 8 BPAM Extend ed: warning condition |
| | | | | | encF 15 ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.196 pkamp_a9_pktime_a9

Reg.

0xA02108C4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |
| encF | 15 | ESM/xPAM po |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | wer up stat<br>e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.197 nrgy_b9

Reg. 0xA02108C8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.198 pkamp_b9_pktime_b9

Reg. 0xA02108CC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.199 nrgy_c9

Reg. 0xA02108D0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | or no repl<br>y |
| | | | | | enc3 \| 3 \| CRC error o<br>n reply dat<br>a from ESM/<br>xPAM |
| | | | | | enc4 \| 4 \| SPM not con<br>nected to E<br>SM/xPAM |
| | | | | | enc5 \| 5 \| ESM/xPAM AD<br>C overload<br>during inte<br>gration |
| | | | | | enc6 \| 6 \| ESM/xPAM Da<br>ta not vali<br>d |
| | | | | | enc8 \| 8 \| BPAM Extend<br>ed: warning<br>condition |
| | | | | | encF \| 15 \| ESM/xPAM po<br>wer up stat<br>e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.200 pkamp_c9_pktime_c9

Reg. 0xA02108D4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener<br>gy or ESM/x<br>PAM disable<br>d |
| enc1 | 1 | ESM/xPAM ca<br>ble not con<br>nected |
| enc2 | 2 | ESM framing<br>error or n<br>o reply |
| enc3 | 3 | CRC error o<br>n reply dat<br>a from ESM/<br>xPAM |
| enc4 | 4 | SPM not con<br>nected to E<br>SM/xPAM |
| enc5 | 5 | ESM/xPAM AD<br>C overload<br>during inte<br>gration |
| enc6 | 6 | ESM/xPAM Da<br>ta not vali<br>d |
| enc8 | 8 | BPAM Extend |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ed: warning condition |
| | | | | | encF 15 ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.201 nrgy_a10

Reg. 0xA02108D8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.202 pkamp_a10_pktime_a10

Reg. 0xA02108DC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.203 nrgy_b10

Reg.

0xA02108E0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not con |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | nected |
| | | | | | enc2 / 2 / ESM/xPAM framing error or no reply |
| | | | | | enc3 / 3 / CRC error on reply data from ESM/xPAM |
| | | | | | enc4 / 4 / SPM not connected to ESM/xPAM |
| | | | | | enc5 / 5 / ESM/xPAM ADC overload during integration |
| | | | | | enc6 / 6 / ESM/xPAM Data not valid |
| | | | | | enc8 / 8 / BPAM Extended: warning condition |
| | | | | | encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.204 pkamp_b10_pktime_b10

Reg.

0xA02108E4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Da |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ta not vali<br>d |
| | | | | | enc8 8 BPAM Extend<br>ed: warning<br>condition |
| | | | | | encF 15 ESM/xPAM po<br>wer up stat<br>e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.205 nrgy_c10

Reg. 0xA02108E8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name Value Description<br>enc0 0 Normal Energy or ESM/xPAM disabled<br>enc1 1 ESM/xPAM cable not connected<br>enc2 2 ESM/xPAM framing error or no reply<br>enc3 3 CRC error on reply data from ESM/xPAM<br>enc4 4 SPM not connected to ESM/xPAM<br>enc5 5 ESM/xPAM ADC overload during integration<br>enc6 6 ESM/xPAM Data not valid<br>enc8 8 BPAM Extended: warning condition<br>encF 15 ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.206 pkamp_c10_pktime_c10

Reg. 0xA02108EC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.207 nrgy_a11

Reg.

0xA02108F0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.208 pkamp_a11_pktime_a11

Reg.

0xA02108F4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to E |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | SM/xPAM |
| | | | | | enc5 \| 5 \| ESM/xPAM ADC overload during integration |
| | | | | | enc6 \| 6 \| ESM/xPAM Data not valid |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.209 nrgy_b11

Reg.

0xA02108F8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Normal Energy or ESM/xPAM disabled<br>enc1 \| 1 \| ESM/xPAM cable not connected<br>enc2 \| 2 \| ESM/xPAM framing error or no repl y<br>enc3 \| 3 \| CRC error on reply data from ESM/xPAM<br>enc4 \| 4 \| SPM not connected to ESM/xPAM<br>enc5 \| 5 \| ESM/xPAM ADC overload during integration<br>enc6 \| 6 \| ESM/xPAM Data not valid<br>enc8 \| 8 \| BPAM Extended: warning condition<br>encF \| 15 \| ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.210 pkamp_b11_pktime_b11

Reg. 0xA02108FC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.211 nrgy_c11

Reg. 0xA0210900

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.212 pkamp_c11_pktime_c11

Reg. 0xA0210904

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM framing error or no reply |
| enc3 | 3 | CRC error on reply dat |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | a from ESM/ xPAM |
| | | | | | enc4 4 SPM not con nected to E SM/xPAM |
| | | | | | enc5 5 ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 6 ESM/xPAM Da ta not vali d |
| | | | | | enc8 8 BPAM Extend ed: warning condition |
| | | | | | encF 15 ESM/xPAM po wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.213 nrgy_a12

Reg.

0xA0210908

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | encF 15 ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.214 pkamp_a12_pktime_a12

Reg. 0xA021090C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.215 nrgy_b12

Reg. 0xA0210910

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.216 pkamp_b12_pktime_b12

Reg.

0xA0210914

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM framing |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | error or n o reply |
| | | | | enc3 | 3 CRC error o n reply dat a from ESM/ xPAM |
| | | | | enc4 | 4 SPM not con nected to E SM/xPAM |
| | | | | enc5 | 5 ESM/xPAM AD C overload during inte gration |
| | | | | enc6 | 6 ESM/xPAM Da ta not vali d |
| | | | | enc8 | 8 BPAM Extend ed: warning condition |
| | | | | encF | 15 ESM/xPAM po wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.217 nrgy_c12

Reg.

0xA0210918

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | d |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.218 pkamp_c12_pktime_c12

Reg. 0xA021091C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Normal Energy or ESM/xPAM disabled<br>enc1 \| 1 \| ESM/xPAM cable not connected<br>enc2 \| 2 \| ESM framing error or no reply<br>enc3 \| 3 \| CRC error on reply data from ESM/xPAM<br>enc4 \| 4 \| SPM not connected to ESM/xPAM<br>enc5 \| 5 \| ESM/xPAM ADC overload during integration<br>enc6 \| 6 \| ESM/xPAM Data not valid<br>enc8 \| 8 \| BPAM Extended: warning condition<br>encF \| 15 \| ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.219 nrgy_a13

Reg. 0xA0210920

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.220 pkamp_a13_pktime_a13

Reg. 0xA0210924

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.221 nrgy_b13

Reg. 0xA0210928

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.222 pkamp_b13_pktime_b13

Reg.

0xA021092C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.223 nrgy_c13

Reg. 0xA0210930

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

## 1.11.224 pkamp_c13_pktime_c13

Reg. 0xA0210934

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.225 nrgy_a14

Reg.

0xA0210938

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not con |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | nected to E SM/xPAM |
| | | | | enc5 | 5 ESM/xPAM AD C overload during inte gration |
| | | | | enc6 | 6 ESM/xPAM Da ta not vali d |
| | | | | enc8 | 8 BPAM Extend ed: warning condition |
| | | | | encF | 15 ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.226 pkamp_a14_pktime_a14

Reg.

0xA021093C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |
| encF | 15 | ESM/xPAM po wer up stat e |

| | | | | | |
|---|---|---|---|---|---|
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |

| | | | | | |
|---|---|---|---|---|---|
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.227 nrgy_b14

Reg. 0xA0210940

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

enum:esm_status_nrgy_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

## 1.11.228 pkamp_b14_pktime_b14

Reg. 0xA0210944

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.229 nrgy_c14

Reg. 0xA0210948

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error o |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | n reply dat a from ESM/ xPAM |
| | | | | | enc4 4 SPM not con nected to E SM/xPAM |
| | | | | | enc5 5 ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 6 ESM/xPAM Da ta not vali d |
| | | | | | enc8 8 BPAM Extend ed: warning condition |
| | | | | | encF 15 ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.230 pkamp_c14_pktime_c14

Reg.

0xA021094C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |
| encF | 15 | ESM/xPAM po |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | wer up stat<br>e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.231 nrgy_a15

Reg. 0xA0210950

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.232 pkamp_a15_pktime_a15

Reg. 0xA0210954

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.233 nrgy_b15

Reg. 0xA0210958

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state<br>or no reply |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.234 pkamp_b15_pktime_b15

Reg.

0xA021095C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extend |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ed: warning condition |
| | | | | | encF 15 ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.235 nrgy_c15

Reg. 0xA0210960

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.236 pkamp_c15_pktime_c15

Reg. 0xA0210964

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.237 nrgy_a16

Reg.

0xA0210968

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not con |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | nected |
| | | | | enc2 | 2 ESM/xPAM fr aming error or no repl y |
| | | | | enc3 | 3 CRC error o n reply dat a from ESM/ xPAM |
| | | | | enc4 | 4 SPM not con nected to E SM/xPAM |
| | | | | enc5 | 5 ESM/xPAM AD C overload during inte gration |
| | | | | enc6 | 6 ESM/xPAM Da ta not vali d |
| | | | | enc8 | 8 BPAM Extend ed: warning condition |
| | | | | encF | 15 ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.238 pkamp_a16_pktime_a16

Reg.

0xA021096C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ta not vali<br>d |
| | | | | | enc8 8 BPAM Extend<br>ed: warning<br>condition |
| | | | | | encF 15 ESM/xPAM po<br>wer up stat<br>e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.239 nrgy_b16

Reg. 0xA0210970

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name Value Description<br>enc0 0 Normal Energy or ESM/xPAM disabled<br>enc1 1 ESM/xPAM cable not connected<br>enc2 2 ESM/xPAM framing error or no reply<br>enc3 3 CRC error on reply data from ESM/xPAM<br>enc4 4 SPM not connected to ESM/xPAM<br>enc5 5 ESM/xPAM ADC overload during integration<br>enc6 6 ESM/xPAM Data not valid<br>enc8 8 BPAM Extended: warning condition<br>encF 15 ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.240 pkamp_b16_pktime_b16

Reg. 0xA0210974

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.241 nrgy_c16

Reg.

0xA0210978

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.242 pkamp_c16_pktime_c16

Reg. 0xA021097C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to E |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | SM/xPAM |
| | | | | | enc5 \| 5 \| ESM/xPAM ADC overload during integration |
| | | | | | enc6 \| 6 \| ESM/xPAM Data not valid |
| | | | | | enc8 \| 8 \| BPAM Extended: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.243 nrgy_a17

Reg.

0xA0210980

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name \| Value \| Description<br>enc0 \| 0 \| Normal Energy or ESM/xPAM disabled<br>enc1 \| 1 \| ESM/xPAM cable not connected<br>enc2 \| 2 \| ESM/xPAM framing error or no repl y<br>enc3 \| 3 \| CRC error on reply data from ESM/xPAM<br>enc4 \| 4 \| SPM not connected to ESM/xPAM<br>enc5 \| 5 \| ESM/xPAM ADC overload during integration<br>enc6 \| 6 \| ESM/xPAM Data not valid<br>enc8 \| 8 \| BPAM Extended: warning condition<br>encF \| 15 \| ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.244 pkamp_a17_pktime_a17

Reg. 0xA0210984

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.245 nrgy_b17

Reg. 0xA0210988

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

### 1.11.246 pkamp_b17_pktime_b17

Reg.

0xA021098C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply dat |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | a from ESM/ xPAM |
| | | | | | enc4 4 SPM not con nected to E SM/xPAM |
| | | | | | enc5 5 ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 6 ESM/xPAM Da ta not vali d |
| | | | | | enc8 8 BPAM Extend ed: warning condition |
| | | | | | encF 15 ESM/xPAM po wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.247 nrgy_c17

Reg.

0xA0210990

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | encF 15 ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.248 pkamp_c17_pktime_c17

Reg. 0xA0210994

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.249 nrgy_a18

Reg. 0xA0210998

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.250 pkamp_a18_pktime_a18

Reg.

0xA021099C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM framing |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | error or n o reply |
| | | | | enc3 | 3 CRC error o n reply dat a from ESM/ xPAM |
| | | | | enc4 | 4 SPM not con nected to E SM/xPAM |
| | | | | enc5 | 5 ESM/xPAM AD C overload during inte gration |
| | | | | enc6 | 6 ESM/xPAM Da ta not vali d |
| | | | | enc8 | 8 BPAM Extend ed: warning condition |
| | | | | encF | 15 ESM/xPAM po wer up stat e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.251 nrgy_b18

Reg.

0xA02109A0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM/xPAM fr aming error or no repl y |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali |

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td>
<table>
<tr><td></td><td></td><td>d</td></tr>
<tr><td>enc8</td><td>8</td><td>BPAM Extended: warning condition</td></tr>
<tr><td>encF</td><td>15</td><td>ESM/xPAM power up state</td></tr>
</table>
</td></tr>
<tr><td>23:0</td><td>e</td><td>ro</td><td>wo</td><td>0x0</td><td>24-bit energy value</td></tr>
</table>

## 1.11.252 pkamp_b18_pktime_b18

Reg. 0xA02109A4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

<table>
<tr><th>bits</th><th>name</th><th>s/w</th><th>h/w</th><th>default</th><th>description</th></tr>
<tr><td>31:28</td><td>f</td><td>ro</td><td>wo</td><td>0x0</td><td>
enum:esm_status_pkamp_encoding
<table>
<tr><th>Name</th><th>Value</th><th>Description</th></tr>
<tr><td>enc0</td><td>0</td><td>Normal Energy or ESM/xPAM disabled</td></tr>
<tr><td>enc1</td><td>1</td><td>ESM/xPAM cable not connected</td></tr>
<tr><td>enc2</td><td>2</td><td>ESM framing error or no reply</td></tr>
<tr><td>enc3</td><td>3</td><td>CRC error on reply data from ESM/xPAM</td></tr>
<tr><td>enc4</td><td>4</td><td>SPM not connected to ESM/xPAM</td></tr>
<tr><td>enc5</td><td>5</td><td>ESM/xPAM ADC overload during integration</td></tr>
<tr><td>enc6</td><td>6</td><td>ESM/xPAM Data not valid</td></tr>
<tr><td>enc8</td><td>8</td><td>BPAM Extended: warning condition</td></tr>
<tr><td>encF</td><td>15</td><td>ESM/xPAM power up state</td></tr>
</table>
</td></tr>
<tr><td>27:16</td><td>pkamp</td><td>ro</td><td>wo</td><td>0x0</td><td>12-bit amplitude value</td></tr>
<tr><td>13:0</td><td>pktime</td><td>ro</td><td>wo</td><td>0x0</td><td>The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns</td></tr>
</table>

## 1.11.253 nrgy_c18

Reg. 0xA02109A8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.254 pkamp_c18_pktime_c18

Reg. 0xA02109AC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

### 1.11.255 nrgy_a19

Reg. 0xA02109B0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.256 pkamp_a19_pktime_a19

Reg.

0xA02109B4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.257 nrgy_b19

Reg. 0xA02109B8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no reply |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

## 1.11.258 pkamp_b19_pktime_b19

Reg. 0xA02109BC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.259 nrgy_c19

Reg. 0xA02109C0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not con |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | nected to E SM/xPAM |
| | | | | enc5 | 5 ESM/xPAM AD C overload during inte gration |
| | | | | enc6 | 6 ESM/xPAM Da ta not vali d |
| | | | | enc8 | 8 BPAM Extend ed: warning condition |
| | | | | encF | 15 ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.260 pkamp_c19_pktime_c19

Reg.

0xA02109C4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |
| encF | 15 | ESM/xPAM po wer up stat e |

| | | | | | |
|---|---|---|---|---|---|
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |

| | | | | | |
|---|---|---|---|---|---|
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.261 nrgy_a20

Reg. 0xA02109C8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

enum:esm_status_nrgy_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

## 1.11.262 pkamp_a20_pktime_a20

Reg. 0xA02109CC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.263 nrgy_b20

Reg. 0xA02109D0

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM/xPAM framing error or no repl y<br>enc3 / 3 / CRC error o |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | n reply dat a from ESM/ xPAM |
| | | | | | enc4 \| 4 \| SPM not con nected to E SM/xPAM |
| | | | | | enc5 \| 5 \| ESM/xPAM AD C overload during inte gration |
| | | | | | enc6 \| 6 \| ESM/xPAM Da ta not vali d |
| | | | | | enc8 \| 8 \| BPAM Extend ed: warning condition |
| | | | | | encF \| 15 \| ESM/xPAM po wer up stat e |
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.264 pkamp_b20_pktime_b20

Reg.

0xA02109D4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Ener gy or ESM/x PAM disable d |
| enc1 | 1 | ESM/xPAM ca ble not con nected |
| enc2 | 2 | ESM framing error or n o reply |
| enc3 | 3 | CRC error o n reply dat a from ESM/ xPAM |
| enc4 | 4 | SPM not con nected to E SM/xPAM |
| enc5 | 5 | ESM/xPAM AD C overload during inte gration |
| enc6 | 6 | ESM/xPAM Da ta not vali d |
| enc8 | 8 | BPAM Extend ed: warning condition |
| encF | 15 | ESM/xPAM po |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | wer up stat<br>e |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.265 nrgy_c20

Reg. 0xA02109D8

There are three energy registers (NRGY_a, NRGY_b, NRGY_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of
the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.
Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from
0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or
offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_nrgy_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Normal Energy or ESM/xPAM disabled |
| enc1 | 1 | ESM/xPAM cable not connected |
| enc2 | 2 | ESM/xPAM framing error or no repl<br>y |
| enc3 | 3 | CRC error on reply data from ESM/xPAM |
| enc4 | 4 | SPM not connected to ESM/xPAM |
| enc5 | 5 | ESM/xPAM ADC overload during integration |
| enc6 | 6 | ESM/xPAM Data not valid |
| enc8 | 8 | BPAM Extended: warning condition |
| encF | 15 | ESM/xPAM power up state |

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | e | ro | wo | 0x0 | 24-bit energy value |

## 1.11.266 pkamp_c20_pktime_c20

Reg. 0xA02109DC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected.
All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).
Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP_xx registers applies to the Peak Time values as well.
Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

document.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:28 | f | ro | wo | 0x0 | enum:esm_status_pkamp_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal Energy or ESM/xPAM disabled<br>enc1 / 1 / ESM/xPAM cable not connected<br>enc2 / 2 / ESM framing error or no reply<br>enc3 / 3 / CRC error on reply data from ESM/xPAM<br>enc4 / 4 / SPM not connected to ESM/xPAM<br>enc5 / 5 / ESM/xPAM ADC overload during integration<br>enc6 / 6 / ESM/xPAM Data not valid<br>enc8 / 8 / BPAM Extended: warning condition<br>encF / 15 / ESM/xPAM power up state |
| 27:16 | pkamp | ro | wo | 0x0 | 12-bit amplitude value |
| 13:0 | pktime | ro | wo | 0x0 | The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns |

## 1.11.267 ffa_lk

Reg. 0xA0210FCC

ESM/xPAM Channel 16 on the eTEC is a dedicated towards the EESA to gather the FFAQC data

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | ls | ro | wo | 0x0 | enum:eesa_status_lk_encoding<br>Name / Value / Description<br>enc0 / 0 / Normal or EESA disabled<br>enc1 / 1 / EESA cable not connected<br>enc2 / 2 / Framing error or no reply<br>enc3 / 3 / CRC error on reply data from EESA |
| 11:8 | l | ro | wo | 0x0 | L0 and L1 are interlock status. L2 and L3 are reserved |
| 5:4 | s2 | ro | wo | 0x0 | Sensor 2 data status: bit 1 is spare, bit 0, when 1, indicated that the sensor 2<br>data (FFA_S2_X, Y and SUM) are valid |
| 1:0 | s1 | ro | wo | 0x0 | Sensor 1 data status: bit 1 is spare, bit 0, when 1, indicated that the sensor 1 |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | data (FFA_S1_X, Y and SUM) are valid |

### 1.11.268 ffa_s1_x

Reg. 0xA0210FD0

FFA Sensor X x-axis

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | ffa_sx_x | ro | wo | 0x0 | Sensor1: Signed, fixed-point sixteen-bit X data value.<br>Range -1 to 1-1LSB).<br>Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates.<br>(1LSB = 4.593628 nm). |

### 1.11.269 ffa_s1_y

Reg. 0xA0210FD4

FFA Sensor X y-axis

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | ffa_sx_y | ro | wo | 0x0 | Sensor1: Signed, fixed-point sixteen-bit Y data value.<br>Range -1 to 1-1LSB).<br>Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates.<br>(1LSB = 4.593628 nm). |

### 1.11.270 ffa_s1_sum

Reg. 0xA0210FD8

FFA Sensor X Sum

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | ffa_sx_sum | ro | wo | 0x0 | Sensor1: Signed, fixed-point sixteen-bit Y data value.<br>Range -1 to 1-1LSB).<br>Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates.<br>(1LSB = 4.593628 nm). |

### 1.11.271 ffa_s2_x

Reg. 0xA0210FDC

FFA Sensor X x-axis

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | ffa_sx_x | ro | wo | 0x0 | Sensor1: Signed, fixed-point sixteen-bit X data value.<br>Range -1 to 1-1LSB).<br>Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates.<br>(1LSB = 4.593628 nm). |

### 1.11.272 ffa_s2_y

Reg. 0xA0210FE0

FFA Sensor X y-axis

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | ffa_sx_y | ro | wo | 0x0 | Sensor1: Signed, fixed-point sixteen-bit Y data value.<br>Range -1 to 1-1LSB).<br>Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates.<br>(1LSB = 4.593628 nm). |

### 1.11.273 ffa_s2_sum

Reg. 0xA0210FE4

FFA Sensor X Sum

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | ffa_sx_sum | ro | wo | 0x0 | Sensor1: Signed, fixed-point sixteen-bit Y data value.<br>Range -1 to 1-1LSB). |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates.<br>(1LSB = 4.593628 nm). |

### 1.11.274 quadcell_read_sel

Reg. 0xA0210FE8

quadcell_read_sel

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | quadcell_read_sel | ro | wo | 0x0 | quadcell_read_sel |

### 1.11.275 debug_wave

Reg. 0xA0210FEC

debug_wave

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | debug_wave | ro | wo | 0x0 | debug_wave |

### 1.11.276 wave_pkt_cnt

Reg. 0xA0210FF0

Waveform Packet Counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | wave_pkt_cnt | rw | na | 0x0 | Waveform Packet Counter |

### 1.11.277 map4_hop

Reg. 0xA0210FF4

The sixteen-bit MAP4_HOP register determines how many droplets (as developed by the Timestamp module) must occur after the beginning of an EUV Gate before an ESM configured for MAP4 HOP mode (via b[6:5] of ESM_CTL) initiates its next waveform capture.
Note that if any ESM is configured for TR1/TR0 = 11 (MAP4 HOP mode), then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation. The sequence is as follows:
1) wait for the next scanner EUV Gate to go active (low);
2) count the quantity of droplets as configured via the MAP4_HOP register;
3) wait for the next T0 -- waveform capture and subsequent upload occur for non-MAP4 ESMs;
4) wait for the next droplet detection -- waveform capture and subsequent upload occur for the MAP4 ESM (TR1/TR0 = 11).
Once a waveform has been captured by the ESMs, and uploaded to the TEM (265 droplets), then the ESMs again wait for the beginning of the next EUV Gate and MAP4_HOP count before capturing a next waveform. Note that there is an additional 500ms delay inserted between waveform captures (the EUV Gate/HOP register operation begins after the 500ms inter-waveform period expires).

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | hop | rw | ro | 0x0 | map4_hop |

### 1.11.278 map4_latch_time

Reg. 0xA0210FF8

This sixteen-bit register determines the span of time (units of 8ns) after a droplet detection event (sourced from the Timestamper module) until the up-loaded MAP4 ESM metric data is latched in preparation for P2 pushes to the LC. This register is analogous to TDFAST and TDSLOW, except that, whereas those registers define counts that begin from T0 events, this register defines counts that begin with a DDM event.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | latch_time | rw | ro | 0x0 | map4_latch_time |

### 1.11.279 map4_keep_time

Reg. 0xA0210FFC

In the absence of droplet detection events, this sixteen-bit register determines the amount of time before the FPGA switches to a keep-alive mode, whereby the TEM2 uses the internal T0 events to trigger the MAP4 ESM (instead of the normal MAP4 DDM event). When in this keep-alive mode, the MAP4 ESM is operating in tandem with the other non-MAP4 ESMs.

The resolution of this register is 10us. Thus, the keep-alive initiation timespan can be configured anywhere from 10us up to a maximum of 655ms, in increments of 10us. Writing a value of zero to this register disables the keep-alive mode, meaning that the TEM2 will never use T0 events for triggering the MAP4 ESM, and when droplet detection stops, the triggering of the DDM ESM stops as well.
This register powers-up with a value of 0x07D0, which corresponds to 20ms.
When the FPGA enters MAP4 keep-alive mode (i.e., when the keep-alive time is reached), the MAP4 HOP mode is automatically disabled. When this happens, waveform capture continues to operate normally.
Note that the waveform GUI update rate is unaffected by this operation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | keep_time | rw | ro | 0x7D0 | map4_keep_time |

### 1.11.280 esmi_s0_cnt1

Reg. 0xA0211000

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.281 esmi_s0_crc1

Reg. 0xA0211004

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.282 esmi_s1_cnt1

Reg. 0xA0211008

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.283 esmi_s1_crc1

Reg. 0xA021100C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.284 esmi_s2_cnt1

Reg. 0xA0211010

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.285 esmi_s2_crc1

Reg. 0xA0211014

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.286 esmi_s7_cnt1

Reg. 0xA0211018

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.287 esmi_s7_crc1

Reg. 0xA021101C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.288 esmi_rd_cnt1

Reg. 0xA0211020

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.289 esmi_rd_crc1

Reg. 0xA0211024

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.290 esmi_da_cnt1

Reg. 0xA0211028

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.291 esmi_ia_cnt1

Reg. 0xA021102C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.292 esmi_tcmd_cnt1

Reg. 0xA0211030

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.293 esmi_twcmd_cnt1

Reg. 0xA0211034

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.294 esmi_dm_cnt1

Reg. 0xA0211038

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.295 esmi_s0_cnt2

Reg. 0xA0211040

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.296 esmi_s0_crc2

Reg. 0xA0211044

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.297 esmi_s1_cnt2

Reg. 0xA0211048

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.298 esmi_s1_crc2

Reg. 0xA021104C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.299 esmi_s2_cnt2

Reg. 0xA0211050

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.300 esmi_s2_crc2

Reg. 0xA0211054

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.301 esmi_s7_cnt2

Reg. 0xA0211058

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.302 esmi_s7_crc2

Reg. 0xA021105C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.303 esmi_rd_cnt2

Reg. 0xA0211060

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.304 esmi_rd_crc2

Reg. 0xA0211064

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.305 esmi_da_cnt2

Reg. 0xA0211068

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.306 esmi_ia_cnt2

Reg. 0xA021106C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.307 esmi_tcmd_cnt2

Reg. 0xA0211070

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.308 esmi_twcmd_cnt2

Reg. 0xA0211074

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.309 esmi_dm_cnt2

Reg. 0xA0211078

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.310 esmi_s0_cnt3

Reg. 0xA0211080

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.311 esmi_s0_crc3

Reg. 0xA0211084

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.312 esmi_s1_cnt3

Reg. 0xA0211088

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.313 esmi_s1_crc3

Reg. 0xA021108C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.314 esmi_s2_cnt3

Reg. 0xA0211090

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.315 esmi_s2_crc3

Reg. 0xA0211094

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.316 esmi_s7_cnt3

Reg. 0xA0211098

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.317 esmi_s7_crc3

0xA021109C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.318 esmi_rd_cnt3

0xA02110A0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.319 esmi_rd_crc3

0xA02110A4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.320 esmi_da_cnt3

0xA02110A8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.321 esmi_ia_cnt3

0xA02110AC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.322 esmi_tcmd_cnt3

0xA02110B0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.323 esmi_twcmd_cnt3

0xA02110B4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.324 esmi_dm_cnt3

0xA02110B8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.325 esmi_s0_cnt4

Reg. 0xA02110C0

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.326 esmi_s0_crc4

Reg. 0xA02110C4

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.327 esmi_s1_cnt4

Reg. 0xA02110C8

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.328 esmi_s1_crc4

Reg. 0xA02110CC

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.329 esmi_s2_cnt4

Reg. 0xA02110D0

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.330 esmi_s2_crc4

Reg. 0xA02110D4

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.331 esmi_s7_cnt4

Reg. 0xA02110D8

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.332 esmi_s7_crc4

Reg. 0xA02110DC

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.333 esmi_rd_cnt4

Reg. 0xA02110E0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.334 esmi_rd_crc4

Reg. 0xA02110E4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.335 esmi_da_cnt4

Reg. 0xA02110E8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.336 esmi_ia_cnt4

Reg. 0xA02110EC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.337 esmi_tcmd_cnt4

Reg. 0xA02110F0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.338 esmi_twcmd_cnt4

Reg. 0xA02110F4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.339 esmi_dm_cnt4

Reg. 0xA02110F8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.340 esmi_s0_cnt5

Reg. 0xA0211100

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.341 esmi_s0_crc5

Reg. 0xA0211104

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.342 esmi_s1_cnt5

Reg. 0xA0211108

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.343 esmi_s1_crc5

Reg. 0xA021110C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.344 esmi_s2_cnt5

Reg. 0xA0211110

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.345 esmi_s2_crc5

Reg. 0xA0211114

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.346 esmi_s7_cnt5

Reg. 0xA0211118

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.347 esmi_s7_crc5

Reg. 0xA021111C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.348 esmi_rd_cnt5

Reg. 0xA0211120

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.349 esmi_rd_crc5

Reg. 0xA0211124

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.350 esmi_da_cnt5

Reg. 0xA0211128

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.351 esmi_ia_cnt5

Reg. 0xA021112C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.352 esmi_tcmd_cnt5

Reg. 0xA0211130

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.353 esmi_twcmd_cnt5

Reg. 0xA0211134

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.354 esmi_dm_cnt5

Reg. 0xA0211138

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.355 esmi_s0_cnt6

Reg. 0xA0211140

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.356 esmi_s0_crc6

Reg. 0xA0211144

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.357 esmi_s1_cnt6

Reg. 0xA0211148

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.358 esmi_s1_crc6

Reg. 0xA021114C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.359 esmi_s2_cnt6

Reg. 0xA0211150

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.360 esmi_s2_crc6

Reg. 0xA0211154

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.361 esmi_s7_cnt6

Reg. 0xA0211158

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.362 esmi_s7_crc6

Reg. 0xA021115C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.363 esmi_rd_cnt6

Reg. 0xA0211160

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.364 esmi_rd_crc6

Reg. 0xA0211164

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.365 esmi_da_cnt6

Reg. 0xA0211168

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.366 esmi_ia_cnt6

Reg. 0xA021116C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.367 esmi_tcmd_cnt6

Reg. 0xA0211170

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.368 esmi_twcmd_cnt6

Reg. 0xA0211174

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.369 esmi_dm_cnt6

Reg. 0xA0211178

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.370 esmi_s0_cnt7

Reg. 0xA0211180

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.371 esmi_s0_crc7

Reg. 0xA0211184

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.372 esmi_s1_cnt7

Reg. 0xA0211188

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.373 esmi_s1_crc7

Reg. 0xA021118C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.374 esmi_s2_cnt7

Reg. 0xA0211190

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.375 esmi_s2_crc7

Reg. 0xA0211194

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.376 esmi_s7_cnt7

Reg. 0xA0211198

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.377 esmi_s7_crc7

Reg. 0xA021119C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.378 esmi_rd_cnt7

Reg. 0xA02111A0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.379 esmi_rd_crc7

Reg. 0xA02111A4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.380 esmi_da_cnt7

Reg. 0xA02111A8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.381 esmi_ia_cnt7

Reg. 0xA02111AC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.382 esmi_tcmd_cnt7

Reg. 0xA02111B0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.383 esmi_twcmd_cnt7

Reg. 0xA02111B4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.384 esmi_dm_cnt7

Reg. 0xA02111B8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.385 esmi_s0_cnt8

Reg. 0xA02111C0

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.386 esmi_s0_crc8

Reg. 0xA02111C4

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.387 esmi_s1_cnt8

Reg. 0xA02111C8

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.388 esmi_s1_crc8

Reg. 0xA02111CC

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.389 esmi_s2_cnt8

Reg. 0xA02111D0

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.390 esmi_s2_crc8

Reg. 0xA02111D4

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.391 esmi_s7_cnt8

Reg. 0xA02111D8

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.392 esmi_s7_crc8

Reg. 0xA02111DC

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.393 esmi_rd_cnt8

Reg. 0xA02111E0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.394 esmi_rd_crc8

Reg. 0xA02111E4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.395 esmi_da_cnt8

Reg. 0xA02111E8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.396 esmi_ia_cnt8

Reg. 0xA02111EC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.397 esmi_tcmd_cnt8

Reg. 0xA02111F0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.398 esmi_twcmd_cnt8

Reg. 0xA02111F4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.399 esmi_dm_cnt8

Reg. 0xA02111F8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.400 esmi_s0_cnt9

Reg. 0xA0211200

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.401 esmi_s0_crc9

Reg. 0xA0211204

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.402 esmi_s1_cnt9

Reg. 0xA0211208

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.403 esmi_s1_crc9

Reg. 0xA021120C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.404 esmi_s2_cnt9

Reg. 0xA0211210

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.405 esmi_s2_crc9

Reg. 0xA0211214

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.406 esmi_s7_cnt9

Reg. 0xA0211218

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.407 esmi_s7_crc9

Reg. 0xA021121C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.408 esmi_rd_cnt9

Reg. 0xA0211220

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.409 esmi_rd_crc9

0xA0211224

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.410 esmi_da_cnt9

0xA0211228

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.411 esmi_ia_cnt9

0xA021122C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.412 esmi_tcmd_cnt9

0xA0211230

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.413 esmi_twcmd_cnt9

0xA0211234

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.414 esmi_dm_cnt9

0xA0211238

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.415 esmi_s0_cnt10

0xA0211240

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.416 esmi_s0_crc10

0xA0211244

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.417 esmi_s1_cnt10

Reg. 0xA0211248

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.418 esmi_s1_crc10

Reg. 0xA021124C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.419 esmi_s2_cnt10

Reg. 0xA0211250

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.420 esmi_s2_crc10

Reg. 0xA0211254

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.421 esmi_s7_cnt10

Reg. 0xA0211258

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.422 esmi_s7_crc10

Reg. 0xA021125C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.423 esmi_rd_cnt10

Reg. 0xA0211260

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.424 esmi_rd_crc10

Reg. 0xA0211264

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.425 esmi_da_cnt10

Reg. 0xA0211268

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.426 esmi_ia_cnt10

Reg. 0xA021126C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.427 esmi_tcmd_cnt10

Reg. 0xA0211270

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.428 esmi_twcmd_cnt10

Reg. 0xA0211274

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.429 esmi_dm_cnt10

Reg. 0xA0211278

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.430 esmi_s0_cnt11

Reg. 0xA0211280

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.431 esmi_s0_crc11

Reg. 0xA0211284

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.432 esmi_s1_cnt11

Reg. 0xA0211288

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.433 esmi_s1_crc11

Reg. 0xA021128C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.434 esmi_s2_cnt11

Reg. 0xA0211290

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.435 esmi_s2_crc11

Reg. 0xA0211294

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.436 esmi_s7_cnt11

Reg. 0xA0211298

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.437 esmi_s7_crc11

Reg. 0xA021129C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.438 esmi_rd_cnt11

Reg. 0xA02112A0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.439 esmi_rd_crc11

Reg. 0xA02112A4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.440 esmi_da_cnt11

Reg. 0xA02112A8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.441 esmi_ia_cnt11

Reg. 0xA02112AC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.442 esmi_tcmd_cnt11

Reg. 0xA02112B0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.443 esmi_twcmd_cnt11

Reg. 0xA02112B4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.444 esmi_dm_cnt11

Reg. 0xA02112B8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.445 esmi_s0_cnt12

Reg. 0xA02112C0

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.446 esmi_s0_crc12

Reg. 0xA02112C4

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.447 esmi_s1_cnt12

Reg. 0xA02112C8

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.448 esmi_s1_crc12

Reg. 0xA02112CC

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.449 esmi_s2_cnt12

Reg. 0xA02112D0

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.450 esmi_s2_crc12

Reg. 0xA02112D4

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.451 esmi_s7_cnt12

Reg. 0xA02112D8

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.452 esmi_s7_crc12

Reg. 0xA02112DC

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.453 esmi_rd_cnt12

Reg. 0xA02112E0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.454 esmi_rd_crc12

Reg. 0xA02112E4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.455 esmi_da_cnt12

0xA02112E8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.456 esmi_ia_cnt12

0xA02112EC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.457 esmi_tcmd_cnt12

0xA02112F0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.458 esmi_twcmd_cnt12

0xA02112F4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.459 esmi_dm_cnt12

0xA02112F8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.460 esmi_s0_cnt13

0xA0211300

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.461 esmi_s0_crc13

0xA0211304

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.462 esmi_s1_cnt13

0xA0211308

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.463 esmi_s1_crc13

Reg. 0xA021130C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.464 esmi_s2_cnt13

Reg. 0xA0211310

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.465 esmi_s2_crc13

Reg. 0xA0211314

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.466 esmi_s7_cnt13

Reg. 0xA0211318

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.467 esmi_s7_crc13

Reg. 0xA021131C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.468 esmi_rd_cnt13

Reg. 0xA0211320

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.469 esmi_rd_crc13

Reg. 0xA0211324

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.470 esmi_da_cnt13

Reg. 0xA0211328

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.471 esmi_ia_cnt13

Reg. 0xA021132C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.472 esmi_tcmd_cnt13

Reg. 0xA0211330

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.473 esmi_twcmd_cnt13

Reg. 0xA0211334

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.474 esmi_dm_cnt13

Reg. 0xA0211338

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.475 esmi_s0_cnt14

Reg. 0xA0211340

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.476 esmi_s0_crc14

Reg. 0xA0211344

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.477 esmi_s1_cnt14

Reg. 0xA0211348

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.478 esmi_s1_crc14

Reg. 0xA021134C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.479 esmi_s2_cnt14

Reg. 0xA0211350

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.480 esmi_s2_crc14

Reg. 0xA0211354

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.481 esmi_s7_cnt14

Reg. 0xA0211358

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.482 esmi_s7_crc14

Reg. 0xA021135C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.483 esmi_rd_cnt14

Reg. 0xA0211360

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.484 esmi_rd_crc14

Reg. 0xA0211364

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.485 esmi_da_cnt14

Reg. 0xA0211368

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.486 esmi_ia_cnt14

Reg. 0xA021136C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.487 esmi_tcmd_cnt14

Reg. 0xA0211370

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.488 esmi_twcmd_cnt14

Reg. 0xA0211374

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.489 esmi_dm_cnt14

Reg. 0xA0211378

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.490 esmi_s0_cnt15

Reg. 0xA0211380

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.491 esmi_s0_crc15

Reg. 0xA0211384

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.492 esmi_s1_cnt15

Reg. 0xA0211388

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.493 esmi_s1_crc15

Reg. 0xA021138C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.494 esmi_s2_cnt15

Reg. 0xA0211390

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.495 esmi_s2_crc15

Reg. 0xA0211394

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.496 esmi_s7_cnt15

Reg. 0xA0211398

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.497 esmi_s7_crc15

Reg. 0xA021139C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.498 esmi_rd_cnt15

Reg. 0xA02113A0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.499 esmi_rd_crc15

Reg. 0xA02113A4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.500 esmi_da_cnt15

Reg. 0xA02113A8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.501 esmi_ia_cnt15

Reg. 0xA02113AC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.502 esmi_tcmd_cnt15

Reg. 0xA02113B0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.503 esmi_twcmd_cnt15

Reg. 0xA02113B4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.504 esmi_dm_cnt15

Reg. 0xA02113B8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.505 esmi_s0_cnt16

Reg. 0xA02113C0

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.506 esmi_s0_crc16

Reg. 0xA02113C4

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.507 esmi_s1_cnt16

Reg. 0xA02113C8

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.508 esmi_s1_crc16

Reg. 0xA02113CC

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.509 esmi_s2_cnt16

Reg. 0xA02113D0

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.510 esmi_s2_crc16

Reg. 0xA02113D4

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.511 esmi_s7_cnt16

Reg. 0xA02113D8

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.512 esmi_s7_crc16

Reg. 0xA02113DC

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.513 esmi_rd_cnt16

Reg. 0xA02113E0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.514 esmi_rd_crc16

Reg. 0xA02113E4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.515 esmi_da_cnt16

Reg. 0xA02113E8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.516 esmi_ia_cnt16

Reg. 0xA02113EC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.517 esmi_tcmd_cnt16

Reg. 0xA02113F0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.518 esmi_twcmd_cnt16

Reg. 0xA02113F4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.519 esmi_dm_cnt16

Reg. 0xA02113F8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.520 esmi_s0_cnt17

Reg. 0xA0211400

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.521 esmi_s0_crc17

Reg. 0xA0211404

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.522 esmi_s1_cnt17

Reg. 0xA0211408

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.523 esmi_s1_crc17

Reg. 0xA021140C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.524 esmi_s2_cnt17

Reg. 0xA0211410

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.525 esmi_s2_crc17

Reg. 0xA0211414

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.526 esmi_s7_cnt17

Reg. 0xA0211418

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.527 esmi_s7_crc17

Reg. 0xA021141C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.528 esmi_rd_cnt17

Reg. 0xA0211420

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.529 esmi_rd_crc17

Reg. 0xA0211424

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.530 esmi_da_cnt17

Reg. 0xA0211428

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.531 esmi_ia_cnt17

Reg. 0xA021142C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.532 esmi_tcmd_cnt17

Reg. 0xA0211430

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.533 esmi_twcmd_cnt17

Reg. 0xA0211434

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.534 esmi_dm_cnt17

Reg. 0xA0211438

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.535 esmi_s0_cnt18

Reg. 0xA0211440

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.536 esmi_s0_crc18

Reg. 0xA0211444

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.537 esmi_s1_cnt18

Reg. 0xA0211448

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.538 esmi_s1_crc18

Reg. 0xA021144C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.539 esmi_s2_cnt18

Reg. 0xA0211450

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.540 esmi_s2_crc18

Reg. 0xA0211454

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.541 esmi_s7_cnt18

Reg. 0xA0211458

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.542 esmi_s7_crc18

Reg. 0xA021145C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.543 esmi_rd_cnt18

Reg. 0xA0211460

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.544 esmi_rd_crc18

Reg. 0xA0211464

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.545 esmi_da_cnt18

Reg. 0xA0211468

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.546 esmi_ia_cnt18

Reg. 0xA021146C

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.547 esmi_tcmd_cnt18

Reg. 0xA0211470

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.548 esmi_twcmd_cnt18

Reg. 0xA0211474

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.549 esmi_dm_cnt18

Reg. 0xA0211478

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.550 esmi_s0_cnt19

Reg. 0xA0211480

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.551 esmi_s0_crc19

Reg. 0xA0211484

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.552 esmi_s1_cnt19

Reg. 0xA0211488

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.553 esmi_s1_crc19

Reg. 0xA021148C

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.554 esmi_s2_cnt19

Reg. 0xA0211490

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.555 esmi_s2_crc19

Reg. 0xA0211494

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.556 esmi_s7_cnt19

Reg. 0xA0211498

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.557 esmi_s7_crc19

Reg. 0xA021149C

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.558 esmi_rd_cnt19

Reg. 0xA02114A0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.559 esmi_rd_crc19

Reg. 0xA02114A4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.560 esmi_da_cnt19

Reg. 0xA02114A8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.561 esmi_ia_cnt19

Reg. 0xA02114AC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.562 esmi_tcmd_cnt19

Reg. 0xA02114B0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.563 esmi_twcmd_cnt19

Reg. 0xA02114B4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.564 esmi_dm_cnt19

Reg. 0xA02114B8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.565 esmi_s0_cnt20

Reg. 0xA02114C0

SEND0 Packet Count Register
SEND0 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.566 esmi_s0_crc20

Reg. 0xA02114C4

SEND0 CRC error Count Register
total SEND0 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s0_crc | rw | na | 0x0 | esmi_s0_crc |

### 1.11.567 esmi_s1_cnt20

Reg. 0xA02114C8

SEND1 Packet Count Register
SEND1 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s0_cnt | rw | na | 0x0 | esmi_s0_cnt |

### 1.11.568 esmi_s1_crc20

Reg. 0xA02114CC

SEND1 CRC error Count Register
total SEND1 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s1_crc | rw | na | 0x0 | esmi_s1_crc |

### 1.11.569 esmi_s2_cnt20

Reg. 0xA02114D0

SEND2 Packet Count Register
SEND2 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s2_cnt | rw | na | 0x0 | esmi_s2_cnt |

### 1.11.570 esmi_s2_crc20

Reg. 0xA02114D4

SEND2 CRC error Count Register
total SEND2 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s2_crc | rw | na | 0x0 | esmi_s2_crc |

### 1.11.571 esmi_s7_cnt20

Reg. 0xA02114D8

SEND7 Packet Count Register
SEND7 total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | s7_cnt | rw | na | 0x0 | esmi_s7_cnt |

### 1.11.572 esmi_s7_crc20

Reg. 0xA02114DC

SEND7 CRC error Count Register
total SEND7 CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | s7_crc | rw | na | 0x0 | esmi_s7_crc |

### 1.11.573 esmi_rd_cnt20

Reg. 0xA02114E0

READ Packet Count Register
READ total packet count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | rd_cnt | rw | na | 0x0 | esmi_rd_cnt |

### 1.11.574 esmi_rd_crc20

Reg. 0xA02114E4

READ CRC error Count Register
total READ CRC error count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3:0 | rd_crc | rw | na | 0x0 | esmi_rd_crc |

### 1.11.575 esmi_da_cnt20

Reg. 0xA02114E8

Direct Address Request Count Register
Direct Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | da_cnt | rw | na | 0x0 | esmi_da_cnt |

### 1.11.576 esmi_ia_cnt20

Reg. 0xA02114EC

InDirect Address Request Count Register
InDirect Address request total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | ia_cnt | rw | na | 0x0 | esmi_ia_cnt |

### 1.11.577 esmi_tcmd_cnt20

Reg. 0xA02114F0

TREF without waveform Request Count Register
TREF without waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | tcmd_cnt | rw | na | 0x0 | esmi_tcmd_cnt |

### 1.11.578 esmi_twcmd_cnt20

Reg. 0xA02114F4

TREF with waveform Request Count Register
TREF with waveform total count

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | twcmd_cnt | rw | na | 0x0 | esmi_twcmd_cnt |

### 1.11.579 esmi_dm_cnt20

Reg. 0xA02114F8

DOMO total write to read Latency Count Register
Counts the total time for DOMO W/R transaction, from start of first write to end of first read

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | dm_cnt | rw | na | 0x0 | esmi_dm_cnt |

### 1.11.580 esmi_tref_int1

Reg. 0xA0211500

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.581 esmi_tref_freq1

Reg. 0xA0211504

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.582 esmi_clk_type1

Reg. 0xA0211508

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

enum:esmi_clk_duty_cycle_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

enum:esmi_clk_freq_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock detected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

### 1.11.583 esmi_tref_int2

Reg. 0xA021150C

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.584 esmi_tref_freq2

Reg. 0xA0211510

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.585 esmi_clk_type2

Reg. 0xA0211514

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cycle.<br>enc1 / 1 / 25% duty cycle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock detected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz<br>enc4 / 4 / 50 MHz<br>enc5 / 5 / 62.5 MHz |

### 1.11.586 esmi_tref_int3

Reg. 0xA0211518

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.587 esmi_tref_freq3

Reg. 0xA021151C

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.588 esmi_clk_type3

Reg. 0xA0211520

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cycle.<br>enc1 / 1 / 25% duty cycle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock detected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz<br>enc4 / 4 / 50 MHz<br>enc5 / 5 / 62.5 MHz |

## 1.11.589 esmi_tref_int4

Reg. 0xA0211524

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.590 esmi_tref_freq4

Reg. 0xA0211528

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.591 esmi_clk_type4

Reg. 0xA021152C

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cycle.<br>enc1 / 1 / 25% duty cycle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock detected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz<br>enc4 / 4 / 50 MHz<br>enc5 / 5 / 62.5 MHz |

## 1.11.592 esmi_tref_int5

Reg. 0xA0211530

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.593 esmi_tref_freq5

Reg. 0xA0211534

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.594 esmi_clk_type5

Reg. 0xA0211538

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

enum:esmi_clk_duty_cycle_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

enum:esmi_clk_freq_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock detected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

## 1.11.595 esmi_tref_int6

Reg. 0xA021153C

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.596 esmi_tref_freq6

Reg. 0xA0211540

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.597 esmi_clk_type6

Reg. 0xA0211544

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cycle.<br>enc1 / 1 / 25% duty cycle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock detected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz<br>enc4 / 4 / 50 MHz<br>enc5 / 5 / 62.5 MHz |

## 1.11.598 esmi_tref_int7

Reg. 0xA0211548

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.599 esmi_tref_freq7

Reg. 0xA021154C

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.600 esmi_clk_type7

Reg. 0xA0211550

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cycle.<br>enc1 / 1 / 25% duty cycle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock detected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz |

| | | |
|---|---|---|
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

### 1.11.601 esmi_tref_int8

Reg. 0xA0211554

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.602 esmi_tref_freq8

Reg. 0xA0211558

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.603 esmi_clk_type8

Reg. 0xA021155C

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

enum:esmi_clk_duty_cycle_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

enum:esmi_clk_freq_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock detected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

### 1.11.604 esmi_tref_int9

Reg. 0xA0211560

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.605 esmi_tref_freq9

Reg. 0xA0211564

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.606 esmi_clk_type9

Reg. 0xA0211568

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cycle.<br>enc1 / 1 / 25% duty cycle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock detected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz<br>enc4 / 4 / 50 MHz<br>enc5 / 5 / 62.5 MHz |

### 1.11.607 esmi_tref_int10

Reg. 0xA021156C

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.608 esmi_tref_freq10

Reg. 0xA0211570

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.609 esmi_clk_type10

Reg. 0xA0211574

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cycle.<br>enc1 / 1 / 25% duty cycle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock detected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz |

| | | |
|---|---|---|
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

### 1.11.610 esmi_tref_int11

Reg. 0xA0211578

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.611 esmi_tref_freq11

Reg. 0xA021157C

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.612 esmi_clk_type11

Reg. 0xA0211580

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

enum:esmi_clk_duty_cycle_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

enum:esmi_clk_freq_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock detected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

### 1.11.613 esmi_tref_int12

Reg. 0xA0211584

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.614 esmi_tref_freq12

Reg. 0xA0211588

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.615 esmi_clk_type12

Reg. 0xA021158C

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock detected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

### 1.11.616 esmi_tref_int13

Reg. 0xA0211590

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

### 1.11.617 esmi_tref_freq13

Reg. 0xA0211594

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

### 1.11.618 esmi_clk_type13

Reg. 0xA0211598

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock de |

| | | |
|---|---|---|
| | | tected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

## 1.11.619 esmi_tref_int14

Reg. 0xA021159C

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.620 esmi_tref_freq14

Reg. 0xA02115A0

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.621 esmi_clk_type14

Reg. 0xA02115A4

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cy cle. |
| enc1 | 1 | 25% duty cy cle. |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock de tected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

## 1.11.622 esmi_tref_int15

Reg. 0xA02115A8

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.623 esmi_tref_freq15

Reg. 0xA02115AC

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.624 esmi_clk_type15

Reg. 0xA02115B0

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock detected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

## 1.11.625 esmi_tref_int16

Reg. 0xA02115B4

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.626 esmi_tref_freq16

Reg. 0xA02115B8

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.627 esmi_clk_type16

Reg. 0xA02115BC

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock de tected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

## 1.11.628 esmi_tref_int17

Reg. 0xA02115C0

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.629 esmi_tref_freq17

Reg. 0xA02115C4

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.630 esmi_clk_type17

Reg. 0xA02115C8

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

enum:esmi_clk_duty_cycle_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cy cle. |
| enc1 | 1 | 25% duty cy cle. |

enum:esmi_clk_freq_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock de tected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

## 1.11.631 esmi_tref_int18

Reg. 0xA02115CC

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.632 esmi_tref_freq18

Reg. 0xA02115D0

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.633 esmi_clk_type18

Reg. 0xA02115D4

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding |

enum:esmi_clk_duty_cycle_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

enum:esmi_clk_freq_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | No clock detected |
| enc1 | 1 | 10.41 MHz |
| enc2 | 2 | 12.5 MHz |
| enc3 | 3 | 31.25 MHz |
| enc4 | 4 | 50 MHz |
| enc5 | 5 | 62.5 MHz |

## 1.11.634 esmi_tref_int19

Reg. 0xA02115D8

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.635 esmi_tref_freq19

Reg. 0xA02115DC

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.636 esmi_clk_type19

Reg. 0xA02115E0

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding |

enum:esmi_clk_duty_cycle_encoding

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | 50% duty cycle. |
| enc1 | 1 | 25% duty cycle. |

| | | | | | |
|---|---|---|---|---|---|
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock de tected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz<br>enc4 / 4 / 50 MHz<br>enc5 / 5 / 62.5 MHz |

## 1.11.637 esmi_tref_int20

Reg. 0xA02115E4

Internal TREF Enable Register
Enables internal TREF

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | tref_int | rw | ro | 0x0 | esmi_tref_int |

## 1.11.638 esmi_tref_freq20

Reg. 0xA02115E8

Internal TREF Period Register
Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | tref_freq | rw | ro | 0x824 | esmi_tref_freq |

## 1.11.639 esmi_clk_type20

Reg. 0xA02115EC

Clock Type Register
clk_duty_cycle: See esmi_clk_duty_cycle_encoding
clk_freq : See esmi_clk_freq_encoding

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 3 | clk_duty_cycle | ro | wo | X | esmi_clk_duty_cycle<br><br>enum:esmi_clk_duty_cycle_encoding<br>Name / Value / Description<br>enc0 / 0 / 50% duty cy cle.<br>enc1 / 1 / 25% duty cy cle. |
| 2:0 | clk_freq | ro | wo | X | esmi_clk_type<br><br>enum:esmi_clk_freq_encoding<br>Name / Value / Description<br>enc0 / 0 / No clock de tected<br>enc1 / 1 / 10.41 MHz<br>enc2 / 2 / 12.5 MHz<br>enc3 / 3 / 31.25 MHz<br>enc4 / 4 / 50 MHz<br>enc5 / 5 / 62.5 MHz |

## 1.11.640 euv_sim1

Reg. 0xA02115F0

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is en- abled. This is a HW only feature. |

### 1.11.641 euv_sim2

Reg. 0xA02115F4

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.642 euv_sim3

Reg. 0xA02115F8

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.643 euv_sim4

Reg. 0xA02115FC

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.644 euv_sim5

Reg. 0xA0211600

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.645 euv_sim6

Reg. 0xA0211604

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.646 euv_sim7

Reg. 0xA0211608

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.647 euv_sim8

Reg. 0xA021160C

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.648 euv_sim9

Reg. 0xA0211610

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.649 euv_sim10

Reg. 0xA0211614

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.650 euv_sim11

Reg. 0xA0211618

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.651 euv_sim12

Reg. 0xA021161C

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.652 euv_sim13

Reg. 0xA0211620

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.653 euv_sim14

Reg. 0xA0211624

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.654 euv_sim15

Reg. 0xA0211628

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.655 euv_sim16

Reg. 0xA021162C

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.656 euv_sim17

Reg. 0xA0211630

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.657 euv_sim18

Reg. 0xA0211634

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.658 euv_sim19

Reg. 0xA0211638

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.659 euv_sim20

Reg. 0xA021163C

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | euv_sim | rw | ro | 0x0 | Sets the simulated energy value when simulation is enabled. This is a HW only feature. |

### 1.11.660 esmi_scratch

Reg. 0xA0211640

Scratchpad Test Register
Scratchpad test register to ensure proper R/W communcation

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratch | rw | na | 0x0 | esmi_scratch |

### 1.11.661 esmi_s7_1ms_cnt

Reg. 0xA0211644

SEND7 1ms packet counter

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:16 | rxd_min | ro | wo | 0x0 | Minimum number of Send7 packets received in a 1ms window |
| 15:8 | rxd_max | ro | wo | 0x0 | Maximum number of Send7 packets received in a 1ms window |
| 7:0 | rxd_last | ro | wo | 0x0 | Number of Send7 packets received in the last 1ms window |

### 1.11.662 esmi_xpam_bw_ovld

Reg. 0xA0211648

xPAM Bandwidth Overload register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 19:0 | bw_ovld | rw | rw | 0x0 | Bandwidth Overload |

### 1.11.663 esmi_xpam_init_err

Reg. 0xA021164C

xPAM Initialization Error register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 19:0 | init_err | rw | rw | 0x0 | Initialization Error |

### 1.11.664 esmi_xlam_cab_disc

Reg. 0xA0211650

xLAM Cable Disconnect register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 19:0 | cab_disc | rw | rw | 0x0 | Cable Disconnect |

### 1.11.665 esmi_adc_clip_cnt1

Reg. 0xA0211680

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.666 esmi_adc_clip_cnt2

Reg. 0xA0211684

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.667 esmi_adc_clip_cnt3

Reg.

0xA0211688

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.668 esmi_adc_clip_cnt4

Reg.

0xA021168C

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.669 esmi_adc_clip_cnt5

Reg.

0xA0211690

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.670 esmi_adc_clip_cnt6

Reg.

0xA0211694

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.671 esmi_adc_clip_cnt7

Reg.

0xA0211698

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.672 esmi_adc_clip_cnt8

Reg.

0xA021169C

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.673 esmi_adc_clip_cnt9

Reg.

0xA02116A0

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.674 esmi_adc_clip_cnt10

Reg.

0xA02116A4

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.675 esmi_adc_clip_cnt11

0xA02116A8

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.676 esmi_adc_clip_cnt12

0xA02116AC

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.677 esmi_adc_clip_cnt13

0xA02116B0

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.678 esmi_adc_clip_cnt14

0xA02116B4

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.679 esmi_adc_clip_cnt15

0xA02116B8

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.680 esmi_adc_clip_cnt16

0xA02116BC

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.681 esmi_adc_clip_cnt17

0xA02116C0

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.682 esmi_adc_clip_cnt18

0xA02116C4

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.683 esmi_adc_clip_cnt19

0xA02116C8

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.684 esmi_adc_clip_cnt20

Reg. 0xA02116CC

xPAM ADC Clip Count Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 7:0 | adc_clip_cnt | rw | na | 0x0 | esmi_adc_clip_cnt |

### 1.11.685 esmi_dat1

Reg. 0xA02116D0

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.686 esmi_dat2

Reg. 0xA02116D4

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

### 1.11.687 esmi_dat3

Reg. 0xA02116D8

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.688 esmi_dat4

Reg. 0xA02116DC

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.689 esmi_dat5

Reg. 0xA02116E0

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up stat |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | e |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.690 esmi_dat6

Reg. 0xA02116E4

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Framing or CRC error |
| enc5 | 5 | SPM cable not connected |
| enc8 | 8 | Normal, valid data |
| encE | 14 | ESM cable not connected |
| encF | 15 | Indicates ESM is in power up state |

| | | | | | |
|---|---|---|---|---|---|
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.691 esmi_dat7

Reg. 0xA02116E8

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Framing or CRC error |
| enc5 | 5 | SPM cable not connected |
| enc8 | 8 | Normal, valid data |
| encE | 14 | ESM cable not connected |
| encF | 15 | Indicates ESM is in power up state |

| | | | | | |
|---|---|---|---|---|---|
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.692 esmi_dat8

Reg. 0xA02116EC

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding |

| Name | Value | Description |
|---|---|---|
| enc0 | 0 | Framing or CRC error |
| enc5 | 5 | SPM cable n |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ot connecte d<br>enc8 8 Normal, val id data<br>encE 14 ESM cable n ot connecte d<br>encF 15 Indicates E SM is in po wer up stat e |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.693 esmi_dat9

Reg. 0xA02116F0

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name Value Description<br>enc0 0 Framing or CRC error<br>enc5 5 SPM cable n ot connecte d<br>enc8 8 Normal, val id data<br>encE 14 ESM cable n ot connecte d<br>encF 15 Indicates E SM is in po wer up stat e |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.694 esmi_dat10

Reg. 0xA02116F4

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name Value Description<br>enc0 0 Framing or CRC error<br>enc5 5 SPM cable n ot connecte d<br>enc8 8 Normal, val id data<br>encE 14 ESM cable n ot connecte d<br>encF 15 Indicates E SM is in po wer up stat e |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.695 esmi_dat11

Reg. 0xA02116F8

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.696 esmi_dat12

Reg. 0xA02116FC

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.697 esmi_dat13

Reg. 0xA0211700

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connecte |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | d |
| | | | | | encF 15 Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.698 esmi_dat14

Reg. 0xA0211704

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.699 esmi_dat15

Reg. 0xA0211708

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.700 esmi_dat16

Reg. 0xA021170C

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.701 esmi_dat17

Reg. 0xA0211710

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.702 esmi_dat18

Reg. 0xA0211714

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.703 esmi_dat19

Reg. 0xA0211718

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.11.704 esmi_dat20

Reg. 0xA021171C

THIS REGISTER IS RESERVED

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:12 | t3_t0 | ro | wo | 0x0 | ESM/BPAM Status<br><br>enum:esmi_dat_t_encoding<br>Name / Value / Description<br>enc0 / 0 / Framing or CRC error<br>enc5 / 5 / SPM cable not connected<br>enc8 / 8 / Normal, valid data<br>encE / 14 / ESM cable not connected<br>encF / 15 / Indicates ESM is in power up state |
| 7:0 | d7_d0 | ro | wo | 0x0 | ESM/BPAM direct register read data |

## 1.12 mcdma_feed_registers_srdl

Block 0xA0240000 - 0xA0240F73

Register map if the ingress(machine constatns) Open Loop algo Inputs

## 1.12.1 mcdma_feed_module_name

Reg. 0xA0240000

Defines the module name

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | module_name | ro | na | 0x77687765 | ASCII code for module name for MCDMA IP in PS = MDMA |

### 1.12.2 mcdma_feed_module_version

Reg. 0xA0240004

Module version

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:16 | rfu | ro | na | 0x521 | Algo IO Date |
| 15:8 | major_revision | ro | na | 0x3 | Major revision - 01 = MCDMA |
| 7:0 | minor_revision | ro | na | 0x1 | Minor revisoin - 01 = TPG packet rate control |

### 1.12.3 mcdma_feed_page_properties

Reg. 0xA0240008

Address page properties

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31 | present | ro | wo | 0x1 | Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not. |
| 30:16 | rfu | ro | na | 0x0 | Reserver for Future Use - RFU |
| 15:8 | page_size | ro | na | 0x1 | Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enetr here. |
| 7:0 | unified_header_rev | ro | na | 0x1 | Unified Header Format common registers revision - 01 = initial unified header |

### 1.12.4 mcdma_feed_scratchregister

Reg. 0xA024000C

Scratchregister register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | scratchregister | rw | na | 0x12345678 | SW can write to it and read from it for test purposes. |

### 1.12.5 mcdma_feed_irq_enable

Reg. 0xA0240010

Interrupt Requests Enable/Mask Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_enable | rw | ro | 0x0 | IRQ0 enable bit. Not in use. |
| 1 | irq1_enable | rw | ro | 0x0 | IRQ1 enable bit. Not in use. |

### 1.12.6 mcdma_feed_irq_pending

Reg. 0xA0240014

Interrupt Pending Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_pending | r/w1c | wo | 0x0 | IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not in use. |
| 1 | irq1_pending | r/w1c | wo | 0x0 | IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not in use. |

### 1.12.7 mcdma_feed_irq_raw

Reg. 0xA0240018

Interrupt Raw Status Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | irq0_raw | ro | wo | 0x0 | IRQ0 raw status bit. Not in use. |
| 1 | irq1_raw | ro | wo | 0x0 | IRQ1 raw status bit. Not in use. |

### 1.12.8 mcdma_feed_irq_force

Reg. 0xA024001C

Interrupt Force Control Register

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 0 | irq0_force | rw | ro | 0x0 | IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not in use. |
| 1 | irq1_force | rw | ro | 0x0 | IRQ1 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not in use. |

### 1.12.9 streamtpg_en_ctrl

Reg. 0xA0240020

Control register - Data streams and Test Packet Generators(TPG) Enable. Data Streams are enabled by the 16LSB. TPG are enabled by 16MSB. Stream 0-15 & TPG 0-15 are mapped to MCDMA Channel 1-16.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | streamtpg_en | rw | ro | 0xFFFF | Bits 15-0 - Data streams 15-0.<br>Bits 31-16 - TPG 15-0.<br>By default all are disabled. Avoid enabling Data streams and TPG on the same channel at the same time! |

### 1.12.10 streamsx16_err_stat

Reg. 0xA0240024

Status register - All x16 Data streams errors. One sticky bit per stream/channel, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream0_err | r/w1c | wo | 0x0 | Stream 0 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 1 | stream1_err | r/w1c | wo | 0x0 | Stream 1 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 2 | stream2_err | r/w1c | wo | 0x0 | Stream 2 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 3 | stream3_err | r/w1c | wo | 0x0 | Stream 3 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 4 | stream4_err | r/w1c | wo | 0x0 | Stream 4 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 5 | stream5_err | r/w1c | wo | 0x0 | Stream 5 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 6 | stream6_err | r/w1c | wo | 0x0 | Stream 6 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 7 | stream7_err | r/w1c | wo | 0x0 | Stream 7 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 8 | stream8_err | r/w1c | wo | 0x0 | Stream 8 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 9 | stream9_err | r/w1c | wo | 0x0 | Stream 9 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 10 | stream10_err | r/w1c | wo | 0x0 | Stream 10 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 11 | stream11_err | r/w1c | wo | 0x0 | Stream 11 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 12 | stream12_err | r/w1c | wo | 0x0 | Stream 12 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 13 | stream13_err | r/w1c | wo | 0x0 | Stream 13 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 14 | stream14_err | r/w1c | wo | 0x0 | Stream 14 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |
| 15 | stream15_err | r/w1c | wo | 0x0 | Stream 15 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear. |

### 1.12.11 tpg0_packet_rate_clks_ctrl

Reg. 0xA0240034

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.12 tpg0_packet_size_clks_ctrl

Reg. 0xA0240038

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.13 stream0_expsize_dis_ctrl

Reg. 0xA024003C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream0_expsize_dis | rw | ro | 0x4D | Bits 15-0 - Data stream expected packet size in 4Byte incr-ments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.14 stream0_exprate_dis_ctrl

Reg. 0xA0240040

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream0_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the ex-pected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- devia-tion in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.15 stream0_err_stat

Reg. 0xA0240044

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal opera-tion. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.16 stream0_err_expsize_cntr_stat

Reg. 0xA0240048

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.17 stream0_err_pfifofull_cntr_stat

Reg. 0xA024004C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.18 stream0_err_bfifofull_cntr_stat

Reg. 0xA0240050

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.19 stream0_err_maxsize_cntr_stat

Reg. 0xA0240054

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.20 stream0_err_minsize_cntr_stat

Reg. 0xA0240058

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.21 stream0_err_notlast_cntr_stat

Reg. 0xA024005C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.22 stream0_err_minipg_cntr_stat

Reg. 0xA0240060

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.23 stream0_err_watchdog_cntr_stat

Reg. 0xA0240064

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.24 stream0_exc_exprate_cntr_stat

Reg. 0xA0240068

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.25 stream0_exc_expratedeviate_cntr_stat

Reg. 0xA024006C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.26 stream0_rate_measured_stat

Reg. 0xA0240070

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.27 tpg1_packet_rate_clks_ctrl

Reg. 0xA0240134

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.28 tpg1_packet_size_clks_ctrl

Reg. 0xA0240138

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.29 stream1_expsize_dis_ctrl

Reg. 0xA024013C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream1_expsize_dis | rw | ro | 0x2C | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.30 stream1_exprate_dis_ctrl

Reg. 0xA0240140

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream1_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.31 stream1_err_stat

Reg. 0xA0240144

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.32 stream1_err_expsize_cntr_stat

Reg. 0xA0240148

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.33 stream1_err_pfifofull_cntr_stat

Reg. 0xA024014C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.34 stream1_err_bfifofull_cntr_stat

Reg. 0xA0240150

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.35 stream1_err_maxsize_cntr_stat

Reg. 0xA0240154

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.36 stream1_err_minsize_cntr_stat

Reg. 0xA0240158

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.37 stream1_err_notlast_cntr_stat

Reg. 0xA024015C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.38 stream1_err_minipg_cntr_stat

Reg. 0xA0240160

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.39 stream1_err_watchdog_cntr_stat

Reg. 0xA0240164

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.40 stream1_exc_exprate_cntr_stat

Reg. 0xA0240168

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.41 stream1_exc_expratedeviate_cntr_stat

Reg. 0xA024016C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.42 stream1_rate_measured_stat

Reg. 0xA0240170

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.43 tpg2_packet_rate_clks_ctrl

Reg. 0xA0240234

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.44 tpg2_packet_size_clks_ctrl

Reg. 0xA0240238

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.45 stream2_expsize_dis_ctrl

Reg. 0xA024023C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream2_expsize_dis | rw | ro | 0x13 | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.46 stream2_exprate_dis_ctrl

Reg. 0xA0240240

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream2_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.47 stream2_err_stat

Reg. 0xA0240244

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfif | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |

| | | | | | |
|---|---|---|---|---|---|
| | ofull | | | | |
| 2 | stream_err_bfif ofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxs ize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_mins ize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notl ast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_mini pg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watc hdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.48 stream2_err_expsize_cntr_stat

Reg. 0xA0240248

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_exps ize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.49 stream2_err_pfifofull_cntr_stat

Reg. 0xA024024C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfif ofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.50 stream2_err_bfifofull_cntr_stat

Reg. 0xA0240250

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfif ofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.51 stream2_err_maxsize_cntr_stat

Reg. 0xA0240254

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxs ize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.52 stream2_err_minsize_cntr_stat

Reg. 0xA0240258

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_mins ize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.53 stream2_err_notlast_cntr_stat

Reg. 0xA024025C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notl ast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.54 stream2_err_minipg_cntr_stat

Reg. 0xA0240260

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.55 stream2_err_watchdog_cntr_stat

Reg. 0xA0240264

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.56 stream2_exc_exprate_cntr_stat

Reg. 0xA0240268

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.57 stream2_exc_expratedeviate_cntr_stat

Reg. 0xA024026C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.58 stream2_rate_measured_stat

Reg. 0xA0240270

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.59 tpg3_packet_rate_clks_ctrl

Reg. 0xA0240334

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.60 tpg3_packet_size_clks_ctrl

Reg. 0xA0240338

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.61 stream3_expsize_dis_ctrl

Reg. 0xA024033C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream3_expsize_dis | rw | ro | 0xD | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.62 stream3_exprate_dis_ctrl

Reg. 0xA0240340

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream3_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.63 stream3_err_stat

Reg. 0xA0240344

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.64 stream3_err_expsize_cntr_stat

Reg. 0xA0240348

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.65 stream3_err_pfifofull_cntr_stat

Reg. 0xA024034C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.66 stream3_err_bfifofull_cntr_stat

Reg. 0xA0240350

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.67 stream3_err_maxsize_cntr_stat

Reg. 0xA0240354

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.68 stream3_err_minsize_cntr_stat

Reg. 0xA0240358

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.69 stream3_err_notlast_cntr_stat

Reg. 0xA024035C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.70 stream3_err_minipg_cntr_stat

Reg. 0xA0240360

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.71 stream3_err_watchdog_cntr_stat

Reg. 0xA0240364

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.72 stream3_exc_exprate_cntr_stat

Reg. 0xA0240368

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.73 stream3_exc_expratedeviate_cntr_stat

Reg. 0xA024036C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.74 stream3_rate_measured_stat

Reg. 0xA0240370

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.75 tpg4_packet_rate_clks_ctrl

Reg. 0xA0240434

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.76 tpg4_packet_size_clks_ctrl

Reg. 0xA0240438

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.77 stream4_expsize_dis_ctrl

Reg. 0xA024043C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream4_expsize_dis | rw | ro | 0xC | Bits 15-0 - Data stream expected packet size in 4Byte incrments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.78 stream4_exprate_dis_ctrl

Reg. 0xA0240440

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream4_exprate | rw | ro | 0x7F0040 | |

| | | | | | |
|---|---|---|---|---|---|
| | _dis | | | | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.79 stream4_err_stat

Reg. 0xA0240444

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.80 stream4_err_expsize_cntr_stat

Reg. 0xA0240448

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.81 stream4_err_pfifofull_cntr_stat

Reg. 0xA024044C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.82 stream4_err_bfifofull_cntr_stat

Reg. 0xA0240450

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.83 stream4_err_maxsize_cntr_stat

Reg. 0xA0240454

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.84 stream4_err_minsize_cntr_stat

Reg. 0xA0240458

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.85 stream4_err_notlast_cntr_stat

Reg. 0xA024045C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.86 stream4_err_minipg_cntr_stat

Reg. 0xA0240460

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.87 stream4_err_watchdog_cntr_stat

Reg. 0xA0240464

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.88 stream4_exc_exprate_cntr_stat

Reg. 0xA0240468

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.89 stream4_exc_expratedeviate_cntr_stat

Reg. 0xA024046C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.90 stream4_rate_measured_stat

Reg. 0xA0240470

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.91 tpg5_packet_rate_clks_ctrl

Reg. 0xA0240534

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.92 tpg5_packet_size_clks_ctrl

Reg. 0xA0240538

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.93 stream5_expsize_dis_ctrl

Reg. 0xA024053C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream5_expsize_dis | rw | ro | 0x7A | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.94 stream5_exprate_dis_ctrl

Reg. 0xA0240540

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream5_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.95 stream5_err_stat

Reg. 0xA0240544

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |

| | | | | | |
|---|---|---|---|---|---|
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.96 stream5_err_expsize_cntr_stat

Reg. 0xA0240548

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.97 stream5_err_pfifofull_cntr_stat

Reg. 0xA024054C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.98 stream5_err_bfifofull_cntr_stat

Reg. 0xA0240550

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.99 stream5_err_maxsize_cntr_stat

Reg. 0xA0240554

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.100 stream5_err_minsize_cntr_stat

Reg. 0xA0240558

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.101 stream5_err_notlast_cntr_stat

Reg. 0xA024055C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.102 stream5_err_minipg_cntr_stat

Reg. 0xA0240560

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.103 stream5_err_watchdog_cntr_stat

Reg. 0xA0240564

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.104 stream5_exc_exprate_cntr_stat

Reg. 0xA0240568

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.105 stream5_exc_expratedeviate_cntr_stat

Reg. 0xA024056C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.106 stream5_rate_measured_stat

Reg. 0xA0240570

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.107 tpg6_packet_rate_clks_ctrl

Reg. 0xA0240634

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.108 tpg6_packet_size_clks_ctrl

Reg. 0xA0240638

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.109 stream6_expsize_dis_ctrl

Reg. 0xA024063C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream6_expsize_dis | rw | ro | 0xBD | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.110 stream6_exprate_dis_ctrl

Reg. 0xA0240640

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream6_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.111 stream6_err_stat

Reg. 0xA0240644

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.112 stream6_err_expsize_cntr_stat

Reg. 0xA0240648

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.113 stream6_err_pfifofull_cntr_stat

Reg. 0xA024064C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfif ofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.114 stream6_err_bfifofull_cntr_stat

Reg. 0xA0240650

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfif ofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.115 stream6_err_maxsize_cntr_stat

Reg. 0xA0240654

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxs ize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.116 stream6_err_minsize_cntr_stat

Reg. 0xA0240658

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_mins ize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.117 stream6_err_notlast_cntr_stat

Reg. 0xA024065C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notl ast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.118 stream6_err_minipg_cntr_stat

Reg. 0xA0240660

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_mini pg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.119 stream6_err_watchdog_cntr_stat

Reg. 0xA0240664

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watc hdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.120 stream6_exc_exprate_cntr_stat

Reg. 0xA0240668

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expr ate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.121 stream6_exc_expratedeviate_cntr_stat

Reg. 0xA024066C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.122 stream6_rate_measured_stat

Reg. 0xA0240670

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.123 tpg7_packet_rate_clks_ctrl

Reg. 0xA0240734

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.124 tpg7_packet_size_clks_ctrl

Reg. 0xA0240738

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.125 stream7_expsize_dis_ctrl

Reg. 0xA024073C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream7_expsize_dis | rw | ro | 0x1D | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.126 stream7_exprate_dis_ctrl

Reg. 0xA0240740

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream7_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.127 stream7_err_stat

Reg. 0xA0240744

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.128 stream7_err_expsize_cntr_stat

Reg. 0xA0240748

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.129 stream7_err_pfifofull_cntr_stat

Reg. 0xA024074C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.130 stream7_err_bfifofull_cntr_stat

Reg. 0xA0240750

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.131 stream7_err_maxsize_cntr_stat

Reg. 0xA0240754

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.132 stream7_err_minsize_cntr_stat

Reg. 0xA0240758

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.133 stream7_err_notlast_cntr_stat

Reg. 0xA024075C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.134 stream7_err_minipg_cntr_stat

Reg. 0xA0240760

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.135 stream7_err_watchdog_cntr_stat

Reg. 0xA0240764

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.136 stream7_exc_exprate_cntr_stat

Reg. 0xA0240768

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.137 stream7_exc_expratedeviate_cntr_stat

Reg. 0xA024076C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.138 stream7_rate_measured_stat

Reg. 0xA0240770

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.139 tpg8_packet_rate_clks_ctrl

Reg. 0xA0240834

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.140 tpg8_packet_size_clks_ctrl

Reg. 0xA0240838

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.141 stream8_expsize_dis_ctrl

Reg. 0xA024083C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream8_expsize_dis | rw | ro | 0x110 | Bits 15-0 - Data stream expected packet size in 4Byte incr-ments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.142 stream8_exprate_dis_ctrl

Reg. 0xA0240840

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream8_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the ex-pected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- devia-tion in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.143 stream8_err_stat

Reg. 0xA0240844

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal opera-tion. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |

| | | | | | |
|---|---|---|---|---|---|
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.144 stream8_err_expsize_cntr_stat

Reg. 0xA0240848

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.145 stream8_err_pfifofull_cntr_stat

Reg. 0xA024084C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.146 stream8_err_bfifofull_cntr_stat

Reg. 0xA0240850

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.147 stream8_err_maxsize_cntr_stat

Reg. 0xA0240854

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.148 stream8_err_minsize_cntr_stat

Reg. 0xA0240858

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.149 stream8_err_notlast_cntr_stat

Reg. 0xA024085C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.150 stream8_err_minipg_cntr_stat

Reg. 0xA0240860

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.151 stream8_err_watchdog_cntr_stat

Reg. 0xA0240864

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.152 stream8_exc_exprate_cntr_stat

Reg. 0xA0240868

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.153 stream8_exc_expratedeviate_cntr_stat

Reg. 0xA024086C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.154 stream8_rate_measured_stat

Reg. 0xA0240870

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.155 tpg9_packet_rate_clks_ctrl

Reg. 0xA0240934

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.156 tpg9_packet_size_clks_ctrl

Reg. 0xA0240938

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.157 stream9_expsize_dis_ctrl

Reg. 0xA024093C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream9_expsize_dis | rw | ro | 0x34 | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.158 stream9_exprate_dis_ctrl

Reg. 0xA0240940

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream9_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.159 stream9_err_stat

Reg. 0xA0240944

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.160 stream9_err_expsize_cntr_stat

Reg. 0xA0240948

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.161 stream9_err_pfifofull_cntr_stat

Reg. 0xA024094C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.162 stream9_err_bfifofull_cntr_stat

Reg. 0xA0240950

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.163 stream9_err_maxsize_cntr_stat

Reg. 0xA0240954

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.164 stream9_err_minsize_cntr_stat

Reg. 0xA0240958

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.165 stream9_err_notlast_cntr_stat

Reg. 0xA024095C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.166 stream9_err_minipg_cntr_stat

Reg. 0xA0240960

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.167 stream9_err_watchdog_cntr_stat

Reg. 0xA0240964

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.168 stream9_exc_exprate_cntr_stat

Reg. 0xA0240968

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.169 stream9_exc_expratedeviate_cntr_stat

Reg. 0xA024096C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprateddeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.170 stream9_rate_measured_stat

Reg. 0xA0240970

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.171 tpg10_packet_rate_clks_ctrl

Reg. 0xA0240A34

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.172 tpg10_packet_size_clks_ctrl

Reg. 0xA0240A38

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.173 stream10_expsize_dis_ctrl

Reg. 0xA0240A3C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream10_expsize_dis | rw | ro | 0x83 | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.174 stream10_exprate_dis_ctrl

Reg. 0xA0240A40

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream10_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.175 stream10_err_stat

Reg. 0xA0240A44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.176 stream10_err_expsize_cntr_stat

Reg. 0xA0240A48

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.177 stream10_err_pfifofull_cntr_stat

Reg. 0xA0240A4C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.178 stream10_err_bfifofull_cntr_stat

Reg. 0xA0240A50

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.179 stream10_err_maxsize_cntr_stat

Reg. 0xA0240A54

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.180 stream10_err_minsize_cntr_stat

Reg. 0xA0240A58

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.181 stream10_err_notlast_cntr_stat

Reg. 0xA0240A5C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.182 stream10_err_minipg_cntr_stat

Reg. 0xA0240A60

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.183 stream10_err_watchdog_cntr_stat

Reg. 0xA0240A64

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.184 stream10_exc_exprate_cntr_stat

Reg. 0xA0240A68

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.185 stream10_exc_expratedeviate_cntr_stat

Reg. 0xA0240A6C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.186 stream10_rate_measured_stat

Reg. 0xA0240A70

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.187 tpg11_packet_rate_clks_ctrl

Reg. 0xA0240B34

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.188 tpg11_packet_size_clks_ctrl

Reg. 0xA0240B38

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.189 stream11_expsize_dis_ctrl

Reg. 0xA0240B3C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream11_expsize_dis | rw | ro | 0x1E | Bits 15-0 - Data stream expected packet size in 4Byte incr-ments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. |

### 1.12.190 stream11_exprate_dis_ctrl

Reg. 0xA0240B40

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream11_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the ex-pected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- devia-tion in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.191 stream11_err_stat

Reg. 0xA0240B44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal opera-tion. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.192 stream11_err_expsize_cntr_stat

Reg. 0xA0240B48

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.193 stream11_err_pfifofull_cntr_stat

Reg. 0xA0240B4C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.194 stream11_err_bfifofull_cntr_stat

Reg. 0xA0240B50

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.195 stream11_err_maxsize_cntr_stat

Reg. 0xA0240B54

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.196 stream11_err_minsize_cntr_stat

Reg. 0xA0240B58

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.197 stream11_err_notlast_cntr_stat

Reg. 0xA0240B5C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.198 stream11_err_minipg_cntr_stat

Reg. 0xA0240B60

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.199 stream11_err_watchdog_cntr_stat

Reg. 0xA0240B64

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.200 stream11_exc_exprate_cntr_stat

Reg. 0xA0240B68

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.201 stream11_exc_expratedeviate_cntr_stat

Reg. 0xA0240B6C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.202 stream11_rate_measured_stat

Reg. 0xA0240B70

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.203 tpg12_packet_rate_clks_ctrl

Reg. 0xA0240C34

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.204 tpg12_packet_size_clks_ctrl

Reg. 0xA0240C38

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.205 stream12_expsize_dis_ctrl

Reg. 0xA0240C3C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 31:0 | stream12_expsize_dis | rw | ro | 0x40 | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.<br>Default is TBDWords=0xTBD (equal to TBDWords when add x2 tags and x padding words)<br>Allowed min packet size = 3(3*4Bytes), allowed max packet size = 512(512*4Bytes). |

### 1.12.206 stream12_exprate_dis_ctrl

Reg. 0xA0240C40

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream12_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.207 stream12_err_stat

Reg. 0xA0240C44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.208 stream12_err_expsize_cntr_stat

Reg. 0xA0240C48

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.209 stream12_err_pfifofull_cntr_stat

Reg. 0xA0240C4C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.210 stream12_err_bfifofull_cntr_stat

Reg. 0xA0240C50

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.211 stream12_err_maxsize_cntr_stat

Reg. 0xA0240C54

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.212 stream12_err_minsize_cntr_stat

Reg. 0xA0240C58

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.213 stream12_err_notlast_cntr_stat

Reg. 0xA0240C5C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.214 stream12_err_minipg_cntr_stat

Reg. 0xA0240C60

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.215 stream12_err_watchdog_cntr_stat

Reg. 0xA0240C64

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.216 stream12_exc_exprate_cntr_stat

Reg. 0xA0240C68

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.217 stream12_exc_expratedeviate_cntr_stat

Reg. 0xA0240C6C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.218 stream12_rate_measured_stat

Reg. 0xA0240C70

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.219 tpg13_packet_rate_clks_ctrl

Reg. 0xA0240D34

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.220 tpg13_packet_size_clks_ctrl

Reg. 0xA0240D38

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.221 stream13_expsize_dis_ctrl

Reg. 0xA0240D3C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream13_expsize_dis | rw | ro | 0x40 | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.<br>Default is TBDWords=0xTBD (equal to TBDWords when add x2 tags and x padding words)<br>Allowed min packet size = 3(3*4Bytes), allowed max packet size = 512(512*4Bytes). |

### 1.12.222 stream13_exprate_dis_ctrl

Reg. 0xA0240D40

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream13_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.223 stream13_err_stat

Reg. 0xA0240D44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.224 stream13_err_expsize_cntr_stat

Reg. 0xA0240D48

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.225 stream13_err_pfifofull_cntr_stat

Reg. 0xA0240D4C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.226 stream13_err_bfifofull_cntr_stat

Reg. 0xA0240D50

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.227 stream13_err_maxsize_cntr_stat

Reg. 0xA0240D54

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.228 stream13_err_minsize_cntr_stat

Reg. 0xA0240D58

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.229 stream13_err_notlast_cntr_stat

Reg. 0xA0240D5C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.230 stream13_err_minipg_cntr_stat

Reg. 0xA0240D60

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.231 stream13_err_watchdog_cntr_stat

Reg. 0xA0240D64

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.232 stream13_exc_exprate_cntr_stat

Reg. 0xA0240D68

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.233 stream13_exc_expratedeviate_cntr_stat

Reg. 0xA0240D6C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.234 stream13_rate_measured_stat

Reg. 0xA0240D70

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.235 tpg14_packet_rate_clks_ctrl

Reg. 0xA0240E34

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.236 tpg14_packet_size_clks_ctrl

Reg. 0xA0240E38

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.237 stream14_expsize_dis_ctrl

Reg. 0xA0240E3C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream14_expsize_dis | rw | ro | 0x40 | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.<br>Default is TBDWords=0xTBD (equal to TBDWords when add x2 tags and x padding words)<br>Allowed min packet size = 3(3*4Bytes), allowed max packet size = 512(512*4Bytes). |

### 1.12.238 stream14_exprate_dis_ctrl

Reg. 0xA0240E40

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream14_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.239 stream14_err_stat

Reg. 0xA0240E44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_mins | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |

| | | | | | |
|---|---|---|---|---|---|
| | ize | | | | |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.240 stream14_err_expsize_cntr_stat

Reg. 0xA0240E48

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.241 stream14_err_pfifofull_cntr_stat

Reg. 0xA0240E4C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.242 stream14_err_bfifofull_cntr_stat

Reg. 0xA0240E50

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.243 stream14_err_maxsize_cntr_stat

Reg. 0xA0240E54

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.244 stream14_err_minsize_cntr_stat

Reg. 0xA0240E58

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.245 stream14_err_notlast_cntr_stat

Reg. 0xA0240E5C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.246 stream14_err_minipg_cntr_stat

Reg. 0xA0240E60

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.247 stream14_err_watchdog_cntr_stat

Reg. 0xA0240E64

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.248 stream14_exc_exprate_cntr_stat

Reg. 0xA0240E68

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.249 stream14_exc_expratedeviate_cntr_stat

Reg. 0xA0240E6C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.250 stream14_rate_measured_stat

Reg. 0xA0240E70

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

### 1.12.251 tpg15_packet_rate_clks_ctrl

Reg. 0xA0240F34

Control register - TPG Stream Packet rate

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | tpg_packet_rate_clks | rw | ro | 0x823 | Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks = 0x823 |

### 1.12.252 tpg15_packet_size_clks_ctrl

Reg. 0xA0240F38

Control register - TPG Stream Packet size

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | tpg_packet_size_clks | rw | ro | 0x40 | Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit. |

### 1.12.253 stream15_expsize_dis_ctrl

Reg. 0xA0240F3C

Control register - Data stream expected packet size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream15_expsize_dis | rw | ro | 0x40 | Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).<br>Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.<br>Default is TBDWords=0xTBD (equal to TBDWords when add x2 tags and x padding words)<br>Allowed min packet size = 3(3*4Bytes), allowed max packet size = 512(512*4Bytes). |

### 1.12.254 stream15_exprate_dis_ctrl

Reg. 0xA0240F40

Control register - Data stream expected packet rate.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 31:0 | stream15_exprate_dis | rw | ro | 0x7F0040 | Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.<br>Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.<br>Bits 27-16 - Set Data stream expected packet rate +/- deviation in 125MHz clocks. Default 0x7f=+/-127 clocks.<br>Bit 31 - set to 1 to disable rate deviation match against the expected packet rate deviation +/-, by default enabled. |

### 1.12.255 stream15_err_stat

Reg. 0xA0240F44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 0 | stream_err_expsize | r/w1c | wo | 0x0 | Expected packet size not matching to configured. Sticky bit. Write '1' to clear. |
| 1 | stream_err_pfifofull | r/w1c | wo | 0x0 | Packet FIFO is full. Sticky bit. Write '1' to clear. |
| 2 | stream_err_bfifofull | r/w1c | wo | 0x0 | Buffer FIFO is full. Sticky bit. Write '1' to clear. |
| 3 | stream_err_maxsize | r/w1c | wo | 0x0 | Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear. |
| 4 | stream_err_minsize | r/w1c | wo | 0x0 | Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear. |
| 5 | stream_err_notlast | r/w1c | wo | 0x0 | No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear. |
| 6 | stream_err_minipg | r/w1c | wo | 0x0 | Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear. |
| 7 | stream_err_watchdog | r/w1c | wo | 0x0 | FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear. |

### 1.12.256 stream15_err_expsize_cntr_stat

Reg. 0xA0240F48

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_expsize_cntr | rw | na | 0x0 | Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.257 stream15_err_pfifofull_cntr_stat

Reg. 0xA0240F4C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_pfifofull_cntr | rw | na | 0x0 | Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.258 stream15_err_bfifofull_cntr_stat

Reg. 0xA0240F50

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_bfifofull_cntr | rw | na | 0x0 | Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.259 stream15_err_maxsize_cntr_stat

Reg. 0xA0240F54

Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_maxsize_cntr | rw | na | 0x0 | Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.260 stream15_err_minsize_cntr_stat

Reg. 0xA0240F58

Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minsize_cntr | rw | na | 0x0 | Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.261 stream15_err_notlast_cntr_stat

Reg. 0xA0240F5C

Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_notlast_cntr | rw | na | 0x0 | Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.262 stream15_err_minipg_cntr_stat

Reg. 0xA0240F60

Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_minipg_cntr | rw | na | 0x0 | Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.263 stream15_err_watchdog_cntr_stat

Reg. 0xA0240F64

Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_err_watchdog_cntr | rw | na | 0x0 | Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.264 stream15_exc_exprate_cntr_stat

Reg. 0xA0240F68

Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_exprate_cntr | rw | na | 0x0 | Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.265 stream15_exc_expratedeviate_cntr_stat

Reg.

0xA0240F6C

Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 15:0 | stream_exc_expratedeviate_cntr | rw | na | 0x0 | Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero. |

### 1.12.266 stream15_rate_measured_stat

Reg.

0xA0240F70

Status register - Data stream packet rate. Measured in clocks.

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 23:0 | stream_rate_measured | rw | wo | 0x0 | Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823 |

## 1.13 ipi_mcdma_axilite_pg288

Block

0xA1000000 - 0xA1001FFF

MCDMA IP

### 1.13.1 ram_8kb_inst

ram_8kb_inst

0xA1000000, 0xA1000004 ... 0xA1001FFF

| offset | | depth | 2048 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

## 1.14 ipi_gpio_cache_control

Block

0xA2000000 - 0xA2000003

GPIO Cache Control

### 1.14.1 gpio_cache_control_inst

Reg.

0xA2000000

GPIO IP used to control the cache and protection flags on MCDMA AXI-MM busses

| bits | name | s/w | h/w | default | description |
|---|---|---|---|---|---|
| 6:0 | gpio_cache_control | ro | na | 0x2B | The 4bit cache flag default value is 0xb. The 3bit prot flag default value is 0x2 |

## 1.15 ipi_mcdma_bd_ram

Block

0xAA000000 - 0xAA007FFF

MCDMA BD RAM for Sim and HW debug

### 1.15.1 ram_32kb_inst

ram_32kb_inst

0xAA000000, 0xAA000004 ... 0xAA007FFF

| offset | | depth | 8192 | width | 32 | default | 0x0 |
|---|---|---|---|---|---|---|---|

| 1.16 ipi_mcdma_debug_ram | Block | 0xAB000000 - 0xAB007FFF |
|---|---|---|
| MCDMA Debug Ram for Sim and HW debug | | |

| 1.16.1 ram_32kb_inst | ram_32kb_inst | | | | | 0xAB000000, 0xAB000004 ... 0xAB007FFF |
|---|---|---|---|---|---|---|
| offset | | depth | 8192 | width | 32 | default | 0x0 |