dg\_dtec\_odf

		Table o		
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	chip : dg_dtec_odf		0x00000000 - 0xFFFFFFFF	58
.1	block : id_registers		0xA0000000 - 0xA000001B	58
.1.1	reg : proj_id	0x54726F6F	0xA000000	58
.1.2	reg : firm_id	0x00000000	0xA0000004	58
.1.3	reg : firm_build	0x00000000	0xA0000008	58
.1.4	reg : fpga_id	0x00000000	0xA00000C	58
.1.5	reg : fpga_build	0x00000000	0xA0000010	58
.1.6	reg:tec_id	0x00000000	0xA0000014	59
.1.7	reg : context_id		0xA0000018	59
.2	block : core_registers_srdl	000000000	0xA0010000 - 0xA0017FFF	59
		000057005		
.2.1	reg : core_module_name		0xA0010000	59
.2.2	reg : core_module_version	0x00000000	0xA0010004	59
.2.3	reg : core_page_properties	0x80000101	0xA0010008	59
.2.4	reg : core_scratchregister	0x12345678	0xA001000C	60
.2.5	reg : core_irq_enable			60
.2.6	reg : core_irq_pending		0xA0010014	60
.2.7	reg : core_irq_raw		0xA0010018	61
.2.8	reg : core_irq_force		0xA001001C	61
.2.9	reg : build_time	0xDEADC0D	E0xA0010040	62
.2.10	reg : build_date	0xDEADC0D	E0xA0010044	62
.2.11	reg : build_githash		E0xA0010048	62
.2.12	reg : uptime		0xA0010048	63
.2.13	reg : freerun_counter_stat		0xA0010060	63
.2.14	reg : resets_ctrl			63
.2.15	reg : refclk_freq50mhz_stat	0x00000000	0xA0010068	63
.2.16	reg : refclk_freqalgo_stat	0x00000000	0xA001006C	64
.2.17	reg : debug_ctrl	0x00000000	0xA0010070	64
.2.18	reg : debug_stat	0x00000000	0xA0010074	64
.2.19	reg : tod_load_low	0x00000000	0xA0010080	64
.2.20	reg : tod_load_high	0x00000000	0xA0010084	64
.2.21	reg : tod_cntr_low	0x00000000	0xA0010088	64
.2.22	reg : tod_cntr_high	0x00000000	0xA001008C	64
.2.23	reg: lts_cntr	0x00000000	0xA0010090	65
.2.24	reg : tod_incr		0xA0010094	65
.2.25	reg : led_control		0xA00100A0	65
.2.26	reg : damp_to_algo_snoop_xfe r_count	0x00000000	0xA00100B0	65
1.2.27	reg : damp_to_algo_snoop_dro p_count	0x00000000	0xA00100B4	65
.2.28	reg : damp_to_algo_snoop_tou t count	0x00000000	0xA00100B8	65
.2.29	reg : esm_to_algo_snoop_xfer	0x0000000	0xA00100BC	65
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.2.30	reg : esm_to_algo_snoop_drop _count	0x00000000	0xA00100C0	65
.2.31	reg : esm_to_algo_snoop_tout	0x00000000	0xA00100C4	66
.2.32	memory : damp_diag_region		0xA0014000, 0xA0014004 0xA0017FFF	66
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.3.2		0x00000000	0xA0020004	66
.3.3	reg : algo_ingress_page_prop	0x80000101	0xA0020008	66
.3.4	reg : algo_ingress_scratchre	0x12345678	0xA002000C	66
.3.5	gister reg : algo_ingress_irq_enabl	0x00000000	0xA0020010	67
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1.3.9	reg : machineconstants_clst_ thr_pkval_low_perc	0x000007AE	0xA0020020	67
1.3.10	reg : machineconstants_clst_ thr_neighbor_perc	0x00000CCD	0xA0020024	67
1.3.11	reg : machineconstants_clst_ thr_dist2antinode_perc	0x0000599A	0xA0020028	67
1.3.12	reg : machineconstants_clst_ km_nearcluster	0x0000599A	0xA002002C	68
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1.3.14	reg : machineconstants_clst_ em_centroiddist	0x0000199A	0xA0020034	68
1.3.15	reg : machineconstants_clst_ em_thr_pkval_pivot_perc	0x0000C000	0xA0020038	68
1.3.16	reg : machineconstants_clst_ em_maxclustersize	0x0000B333	0xA002003C	68
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1.3.22	reg : machineconstants_clst_ fl_thr_pkval_2m_smaller_boun d	0x00000FF3	0xA0020054	69
1.3.23	reg : machineconstants_clst_ fl_thr_pkval_500_2m_bound	0x00002DCC	0xA0020058	69
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1.3.27	reg : machineconstants_clst_ thr_dist2antinode_ddm_perc	0x00007333	0xA0020068	70
1.3.28	reg : machineconstants_clst_ fl_thr_pkval_500_2m_ddm_bou d	0x00002DCC	0xA002006C	70
1.3.29	reg : machineconstants_clst_ thr_pkval_low_tfdcm_perc	0x0000199A	0xA0020070	70
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1.3.34	reg : atomic_group1_en		0xA0020084	71
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1.3.42	reg : ps2pl_cal_dcm_qc_pass	0x00000001	0xA00200A4	72
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1.3.52	reg : machineconstants_idc_x int3sigmaaveragedthershold	0x00006666	0xA00200CC	73
1.3.53	reg : machineconstants_idc_s atratioaveragethreshold_off	0x0147AE14	0xA00200D0	74
1.3.54	reg : machineconstants_idc_s atratiothreshold	0x00000CCD	0xA00200D4	74
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1.3.64	reg : machineconstants_idc_d t	0xFFFFF000	0xA00200FC	75
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1.3.71	reg : machineconstants_idc_a mplitudereduction		0xA0020118	76
1.3.72	reg : machineconstants_idc_a 0max		0xA002011C	76
1.3.73	reg : machineconstants_idc_a 0min		0xA0020120	76
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1.3.82	reg : machineconstants_idc_p eakmissedratethreshold	0x00000CCD	0xA0020144	78
1.3.83	reg : machineconstants_idc_m ultsatratiothreshold	0x00000CCD	0xA0020148	78
1.3.84	reg : machineconstants_idc_s igmacthreshold	0x00000CCD	0xA002014C	78
1.3.85	reg : machineconstants_idc_s igmalthreshold	0x00000148	0xA0020150	78
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1.3.87	reg : machineconstants_idc_a veraginglength	0x000007D0	0xA0020158	78
1.3.88	reg : machineconstants_idc_m aincl_holdoffcounter	0x00000007	0xA002015C	78
1.3.89	reg : machineconstants_idc_s ubclopt_holdoffcounter	0x00000005	0xA0020160	79
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1.3.91	reg : machineconstants_idc_e xposure_earlyexposurethresho		0xA0020168	79
1.3.92	reg : machineconstants_idc_i dcbtriggerconfig	0x00000000	0xA002016C	79
1.3.93		0x0000000B	0xA0020170	79
1.3.94	reg : machineconstants_idc_e xposuremonitoringcountermax	0x0000000A	0xA0020174	79
1.3.95	reg : machineconstants_idc_d cmbpam2dtec_crcerrthr	0x00000006	0xA0020178	80
1.3.96	reg : machineconstants_idc_d dmbpam2dtec_crcerrthr	0x00000006	0xA002017C	80
1.3.97	reg : machineconstants_idc_d cmbpam2dtec_minnumvalidpks hr		0xA0020180	80
1.3.98	reg : machineconstants_idc_d dmbpam2dtec_minnumvalidpks hr		0xA0020184	80
1.3.99	reg : machineconstants_idc_d cm_signallevel_min	0x00006666	0xA0020188	80
1.3.100	reg : machineconstants_idc_d dm_signallevel_min	0x00004CCD	0xA002018C	80
1.3.101	reg: machineconstants_idc_p hi0marginholdoff	0x00124F80	0xA0020190	80
1.3.102	reg : machineconstants_idc_d cmqualitycountermax	0x0000000A	0xA0020194	81
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1.3.198	reg : machineconstants_slt_p hi0_16	0x00000000	0xA0020314	94
1.3.199	reg : machineconstants_slt_p hi0_17	0x00000000	0xA0020318	94
1.3.200	reg : machineconstants_slt_p hi0_18	0x00000000	0xA002031C	95
1.3.201	reg : machineconstants_slt_p hi0_19	0x00000000	0xA0020320	95
1.3.202	reg : machineconstants_slt_p hi1_1	0x00000000	0xA0020324	95
1.3.203	reg : machineconstants_slt_p hi1_2	0x00000000	0xA0020328	95
1.3.204	reg : machineconstants_slt_p hi1_3	0x00000000	0xA002032C	95
1.3.205	reg : machineconstants_slt_p hi1_4	0x00000000	0xA0020330	95
1.3.206	reg : machineconstants_slt_p hi1_5	0x00000000	0xA0020334	95
1.3.207	reg : machineconstants_slt_p hi1_6	0x00000000	0xA0020338	96
1.3.208	reg : machineconstants_slt_p hi1_7	0x00000000	0xA002033C	96
1.3.209	reg : machineconstants_slt_p hi1_8	0x00000000	0xA0020340	96
1.3.210	reg : machineconstants_slt_p hi1_9	0x00000000	0xA0020344	96
1.3.211	reg : machineconstants_slt_p hi1_10	0x00000000	0xA0020348	96

1.3.212	reg : machineconstants_slt_p hi1_11	0x00000000	0xA002034C	96
1.3.213	reg : machineconstants_slt_p hi1_12	0x00000000	0xA0020350	96
1.3.214	reg : machineconstants_slt_p hi1_13	0x00000000	0xA0020354	96
1.3.215	reg : machineconstants_slt_p hi1_14	0x00000000	0xA0020358	97
1.3.216	reg : machineconstants_slt_p hi1_15	0x00000000	0xA002035C	97
1.3.217	reg : machineconstants_slt_p hi1 16	0x00000000	0xA0020360	97
1.3.218	reg : machineconstants_slt_p hi1_17	0x00000000	0xA0020364	97
1.3.219	reg : machineconstants_slt_p hi1_18	0x00000000	0xA0020368	97
1.3.220	reg : machineconstants_slt_p hi1_19	0x00000000	0xA002036C	97
1.3.221	reg : machineconstants_slt_p resubcoal_flag_1	0x00000001	0xA0020370	97
1.3.222	reg : machineconstants_slt_p resubcoal_flag_2	0x00000001	0xA0020374	98
1.3.223	reg : machineconstants_slt_p resubcoal_flag_3	0x00000001	0xA0020378	98
1.3.224	reg : machineconstants_slt_p resubcoal_flag_4	0x00000001	0xA002037C	98
1.3.225	reg : machineconstants_slt_p resubcoal_flag_5	0x00000001	0xA0020380	98
1.3.226	reg : machineconstants_slt_p resubcoal_flag_6	0x00000001	0xA0020384	98
1.3.227	reg : machineconstants_slt_p resubcoal_flag_7	0x00000001	0xA0020388	98
1.3.228	reg : machineconstants_slt_p resubcoal_flag_8	0x00000001	0xA002038C	98
1.3.229	reg : machineconstants_slt_p resubcoal_flag_9	0x00000001	0xA0020390	99
1.3.230	reg : machineconstants_slt_p resubcoal_flag_10	0x00000001	0xA0020394	99
1.3.231	reg : machineconstants_slt_p resubcoal_flag_11	0x00000001	0xA0020398	99
1.3.232	reg : machineconstants_slt_p resubcoal_flag_12	0x00000001	0xA002039C	99
1.3.233	reg : machineconstants_slt_p resubcoal_flag_13	0x00000001	0xA00203A0	99
1.3.234	reg : machineconstants_slt_p resubcoal_flag_14	0x00000001	0xA00203A4	99
1.3.235	reg : machineconstants_slt_p resubcoal flag_15	0x00000001	0xA00203A8	99
1.3.236	reg : machineconstants_slt_p resubcoal_flag_16	0x00000001	0xA00203AC	100
1.3.237	reg : machineconstants_slt_p resubcoal_flag_17	0x00000001	0xA00203B0	100
1.3.238	reg : machineconstants_slt_p resubcoal_flag_18	0x00000001	0xA00203B4	100
1.3.239	reg : machineconstants_slt_p resubcoal_flag_19	0x00000001	0xA00203B8	100
1.3.240	reg : machineconstants_slt_j itter_1	0x00000000	0xA00203BC	100
1.3.241	reg : machineconstants_slt_j itter_2	0x00000000	0xA00203C0	100
1.3.242	reg : machineconstants_slt_j itter_3	0x00000000	0xA00203C4	100
1.3.243	reg : machineconstants_slt_j itter_4	0x00000000	0xA00203C8	101
1.3.244	reg: machineconstants_slt_j itter_5	0x00000000	0xA00203CC	101
1.3.245	reg : machineconstants_slt_j itter_6	0x00000000	0xA00203D0	101

1.3.246	reg : machineconstants_slt_j itter 7	0x00000000	0xA00203D4	101
1.3.247	reg : machineconstants_slt_j itter_8	0x00000000	0xA00203D8	101
1.3.248	reg : machineconstants_slt_j itter_9	0x00000000	0xA00203DC	101
1.3.249	reg : machineconstants_slt_j itter_10	0x00000000	0xA00203E0	101
1.3.250	reg : machineconstants_slt_j itter_11	0x00000000	0xA00203E4	101
1.3.251	reg : machineconstants_slt_j itter_12	0x00000000	0xA00203E8	102
1.3.252	reg : machineconstants_slt_j itter_13	0x00000000	0xA00203EC	102
1.3.253	reg : machineconstants_slt_j itter_14	0x00000000	0xA00203F0	102
1.3.254	reg : machineconstants_slt_j itter_15	0x00000000	0xA00203F4	102
1.3.255	reg : machineconstants_slt_j itter_16	0x00000000	0xA00203F8	102
1.3.256	reg : machineconstants_slt_j itter_17	0x00000000	0xA00203FC	102
1.3.257	reg : machineconstants_slt_j itter_18	0x00000000	0xA0020400	102
1.3.258	reg : machineconstants_slt_j itter_19	0x00000000	0xA0020404	102
1.3.259	reg : machineconstants_slt_m ultpresubrate_1	0x00000000	0xA0020408	103
1.3.260	reg : machineconstants_slt_m ultpresubrate_2	0x00000000	0xA002040C	103
1.3.261	reg: machineconstants_slt_m ultpresubrate_3	0x00000000	0xA0020410	103
1.3.262	reg: machineconstants_slt_m ultpresubrate_4	0x00000000	0xA0020414	103
1.3.263	reg : machineconstants_slt_m ultpresubrate_5	0x00000000	0xA0020418	103
1.3.264	reg : machineconstants_slt_m ultpresubrate_6	0x00000000	0xA002041C	103
1.3.265		0x00000000	0xA0020420	103
1.3.266	reg : machineconstants_slt_m ultpresubrate_8	0x00000000	0xA0020424	104
1.3.267	reg: machineconstants_slt_m ultpresubrate_9	0x00000000	0xA0020428	104
1.3.268	reg : machineconstants_slt_m ultpresubrate_10	0x00000000	0xA002042C	104
1.3.269	reg: machineconstants_slt_m ultpresubrate_11	0x00000000	0xA0020430	104
1.3.270	reg: machineconstants_slt_m ultpresubrate_12	0x00000000	0xA0020434	104
1.3.271	reg: machineconstants_slt_m ultpresubrate_13	0x00000000	0xA0020438	104
1.3.272	reg : machineconstants_slt_m ultpresubrate_14	0x00000000	0xA002043C	105
1.3.273	reg : machineconstants_slt_m ultpresubrate_15	0x00000000	0xA0020440	105
1.3.274	reg : machineconstants_slt_m ultpresubrate_16	0x00000000	0xA0020444	105
1.3.275	reg: machineconstants_slt_m ultpresubrate_17	0x00000000	0xA0020448	105
1.3.276	reg : machineconstants_slt_m ultpresubrate_18	0x00000000	0xA002044C	105
1.3.277	reg : machineconstants_slt_m ultpresubrate_19	0x00000000	0xA0020450	105
1.3.278	reg : machineconstants_slt_p resubrate_1	0x00000000	0xA0020454	105
1.3.279	reg : machineconstants_slt_p resubrate_2	0x00000000	0xA0020458	106

1.3.280	reg : machineconstants_slt_p resubrate_3	0x00000000	0xA002045C	106
1.3.281	reg : machineconstants_slt_p resubrate_4	0x00000000	0xA0020460	106
1.3.282	reg : machineconstants_slt_p resubrate_5	0x00000000	0xA0020464	106
1.3.283	reg : machineconstants_slt_p resubrate_6	0x00000000	0xA0020468	106
1.3.284	reg : machineconstants_slt_p resubrate_7	0x00000000	0xA002046C	106
1.3.285	reg : machineconstants_slt_p resubrate_8	0x00000000	0xA0020470	106
1.3.286	reg : machineconstants_slt_p	0x00000000	0xA0020474	107
1.3.287	resubrate_9 reg: machineconstants_slt_p	0x00000000	0xA0020478	107
1.3.288	reg: machineconstants_slt_p	0x00000000	0xA002047C	107
1.3.289	reg: machineconstants_slt_p	0x00000000	0xA0020480	107
1.3.290	reg: machineconstants_slt_p	0x00000000	0xA0020484	107
1.3.291	resubrate_13 reg : machineconstants_slt_p	0x00000000	0xA0020488	107
1.3.292	resubrate_14 reg : machineconstants_slt_p	0x00000000	0xA002048C	107
1.3.293	resubrate_15 reg : machineconstants_slt_p	0x00000000	0xA0020490	108
1.3.294	resubrate_16 reg : machineconstants_slt_p	0x00000000	0xA0020494	108
1.3.295	resubrate_17 reg : machineconstants_slt_p	0x00000000	0xA0020498	108
1.3.296	resubrate_18 reg: machineconstants_slt_p	0x00000000	0xA002049C	108
1.3.297	resubrate_19 reg : machineconstants_slt_c	0x00000000	0xA00204A0	108
1.3.298	m_1 reg : machineconstants_slt_c	0x00000000	0xA00204A4	108
1.3.299	m_2 reg : machineconstants_slt_c	0x00000000	0xA00204A8	108
1.3.300	m_3 reg : machineconstants_slt_c	0x00000000	0xA00204AC	109
1.3.301	m_4 reg: machineconstants_slt_c	0x00000000	0xA00204B0	109
1.3.302	m_5 reg: machineconstants_sit_c	0x00000000	0xA00204B4	109
1.3.303	m_6 reg: machineconstants_sit_c	0x00000000	0xA00204B8	109
	m_7			
1.3.304	reg: machineconstants_slt_c m_8	0x00000000	0xA00204BC	109
1.3.305	reg : machineconstants_slt_c m_9	0x00000000	0xA00204C0	109
1.3.306	reg : machineconstants_slt_c m_10	0x00000000	0xA00204C4	109
1.3.307	reg : machineconstants_slt_c m_11	0x00000000	0xA00204C8	109
1.3.308	reg : machineconstants_slt_c m_12	0x00000000	0xA00204CC	110
1.3.309	reg : machineconstants_slt_c m_13	0x00000000	0xA00204D0	110
1.3.310	reg : machineconstants_slt_c m_14	0x00000000	0xA00204D4	110
1.3.311	reg : machineconstants_slt_c m_15	0x00000000	0xA00204D8	110
1.3.312	reg : machineconstants_slt_c m_16	0x00000000	0xA00204DC	110
1.3.313	reg : machineconstants_slt_c m_17	0x00000000	0xA00204E0	110

1.3.314	reg : machineconstants_slt_c m_18	0x00000000	0xA00204E4	110
1.3.315	reg : machineconstants_slt_c m_19	0x00000000	0xA00204E8	110
1.3.316	reg : machineconstants_slt_d	0x00000000	0xA00204EC	111
1.3.317	m_1 reg : machineconstants_slt_d	0x00000000	0xA00204F0	111
1.3.318	m_2 reg : machineconstants_slt_d	0x00000000	0xA00204F4	111
1.3.319	m_3 reg : machineconstants_slt_d	0x00000000	0xA00204F8	111
1.3.320	m_4 reg : machineconstants_slt_d	0x00000000	0xA00204FC	111
1.3.321	m_5 reg : machineconstants_slt_d	0x00000000	0xA0020500	111
1.3.322	m_6 reg : machineconstants_slt_d	0x00000000	0xA0020504	111
1.3.323	m_7 reg : machineconstants_slt_d	0x00000000	0xA0020508	112
	m_8			440
1.3.324	reg : machineconstants_slt_d m_9	0x00000000	0xA002050C	112
1.3.325	reg : machineconstants_slt_d m_10	0x00000000	0xA0020510	112
1.3.326	reg : machineconstants_slt_d m_11	0x00000000	0xA0020514	112
1.3.327	reg: machineconstants_slt_d m_12	0x00000000	0xA0020518	112
1.3.328	reg : machineconstants_slt_d m_13	0x00000000	0xA002051C	112
1.3.329	reg : machineconstants_slt_d m_14	0x00000000	0xA0020520	112
1.3.330	reg : machineconstants_slt_d m_15	0x00000000	0xA0020524	112
1.3.331	reg : machineconstants_slt_d m_16	0x00000000	0xA0020528	113
1.3.332	reg : machineconstants_slt_d m_17	0x00000000	0xA002052C	113
1.3.333	reg : machineconstants_slt_d m 18	0x00000000	0xA0020530	113
1.3.334	reg : machineconstants_slt_d m_19	0x00000000	0xA0020534	113
1.3.335	reg : machineconstants_slt_d	0x00000000	0xA0020538	113
1.3.336	cdphi reg: machineconstants_slt_p	0x00000000	0xA002053C	113
1.3.337	hi1margin_1 reg : machineconstants_slt_p	0x00000000	0xA0020540	113
1.3.338	hi1margin_2 reg : machineconstants_slt_p	0x00000000	0xA0020544	114
1.3.339	hi1margin_3 reg : machineconstants_slt_p	0x00000000	0xA0020548	114
1.3.340	hi1margin_4 reg : machineconstants_slt_p	0x00000000	0xA002054C	114
1.3.341	hi1margin_5 reg : machineconstants_slt_p	0x00000000	0xA0020550	114
1.3.342	hi1margin_6 reg : machineconstants_slt_p	0x00000000	0xA0020554	114
1.3.343	hi1margin_7 reg : machineconstants_slt_p	0x00000000	0xA0020558	114
1.3.344	hi1margin_8 reg : machineconstants_slt_p	0x00000000	0xA002055C	114
1.3.345	hi1margin_9 reg : machineconstants_slt_p	0x00000000	0xA0020560	115
	hi1margin_10			
1.3.346	reg : machineconstants_slt_p hi1margin_11	0x00000000	0xA0020564	115
1.3.347	reg : machineconstants_slt_p hi1margin_12	0x00000000	0xA0020568	115

1.3.348	reg : machineconstants_slt_p hi1margin_13	0x00000000	0xA002056C	115
1.3.349	reg : machineconstants_slt_p hi1margin_14	0x00000000	0xA0020570	115
1.3.350	reg : machineconstants_slt_p hi1margin_15	0x00000000	0xA0020574	115
1.3.351	reg : machineconstants_slt_p	0x00000000	0xA0020578	115
1.3.352	hi1margin_16  reg : machineconstants_slt_p	0x00000000	0xA002057C	116
1.3.353	hi1margin_17  reg : machineconstants_slt_p	0x00000000	0xA0020580	116
1.3.354	hi1margin_18 reg : machineconstants_slt_p	0x00000000	0xA0020584	116
1.3.355	hi1margin_19 reg : machineconstants_slt_p	0x00000000	0xA0020588	116
1.3.356	hi0margin reg : machineconstants_slt_s	0x00000000	0xA002058C	116
1.3.357	atrateavg_off reg : machineconstants_slt_s	0x00000000	0xA0020590	116
	atrateavg_on			
1.3.358	reg : machineconstants_slt_x int3sigma_avg	0x00000000	0xA0020594	116
1.3.359	reg : machineconstants_slt_p resubrate_avg	0x00000000	0xA0020598	117
1.3.360	reg : machineconstants_slt_o pt_sol	0x00000002	0xA002059C	117
1.3.361	reg : machineconstants_slt_b k_sol	0x00000002	0xA00205A0	117
1.3.362	reg : machineconstants_damp_damp2piezo_gain	0x00000A3D	0xA00205A4	117
1.3.363	reg : machineconstants_damp_ waveform_debug_setup_aoch1		0xA00205A8	117
1.3.364		0x00000000	0xA00205AC	117
1.3.365	reg : machineconstants_damp_ waveform_debug_setup_aoch3	0x00000000	0xA00205B0	117
1.3.366	reg : machineconstants_damp_ waveform_debug_setup_aoch4	0x00000000	0xA00205B4	118
1.3.367	reg : machineconstants_damp_ deltan		0xA00205B8	118
1.3.368	reg : machineconstants_damp_ ditherbits	0x00000000	0xA00205BC	118
1.3.369	reg : machineconstants_cal_b do_basefreqmin	0x2A4C2000	0xA00205C0	118
1.3.370	reg : machineconstants_cal_b do_basefreqnumber	0x00000003	0xA00205C4	118
1.3.371	reg : machineconstants_cal_b do_basefreqres	0x03D86000	0xA00205C8	118
1.3.372	reg : machineconstants_cal_s	0x00001000	0xA00205CC	119
1.3.373	qrampltf reg: machineconstants_cal_m	0x03C8C000	0xA00205D0	119
1.3.374	ainfreqvec_min reg : machineconstants_cal_m	0x00000015	0xA00205D4	119
1.3.375	ainfreqvec_number reg : machineconstants_cal_m	0x00019000	0xA00205D8	119
1.3.376	ainfreqvec_res reg : machineconstants_cal_s	0x00001C00	0xA00205DC	119
1.3.377	ubfreqmultvec_min reg : machineconstants_cal_s	0x00000004	0xA00205E0	119
1.3.378	ubfreqmultvec_number reg : machineconstants_cal_s	0x00000400	0xA00205E4	119
1.3.379	ubfreqmultvec_res reg : machineconstants_cal_s	0x00000066	0xA00205E8	120
1.3.380	ineampltfmin reg: machineconstants_cal_s	0x00000066	0xA00205EC	120
	ineampltfres			
1.3.381	reg : machineconstants_cal_s ineampltfnumber	0x00000014	0xA00205F0	120

1.3.382	reg : machineconstants_cal_m ainfreqdiag_min	0x030D4000	0xA00205F4	120
1.3.383	reg : machineconstants_cal_m ainfreqdiag_res	0x00019000	0xA00205F8	120
1.3.384	reg : machineconstants_cal_m ainfreqdiag_number	0x000000C9	0xA00205FC	120
1.3.385	reg: machineconstants_cal_b do_holdoff	0x0000000A	0xA0020600	120
1.3.386	reg : machineconstants_cal_t fm_holdoff	0x0000000A	0xA0020604	121
1.3.387	reg : machineconstants_cal_d dmmainpeakvalthr	0x00002000	0xA0020608	121
1.3.388	reg : machineconstants_cal_d dmsnrthr	0x00000500	0xA002060C	121
1.3.389	reg : machineconstants_cal_d dmwidththr	0x000004CD	0xA0020610	121
1.3.390	reg : machineconstants_cal_d dmqc_holdoff	0x00000005	0xA0020614	121
1.3.391	reg: machineconstants_cal_d cmgc_holdoff	0x00000005	0xA0020618	121
1.3.392	reg : machineconstants_cal_d cmmainpeakvalthr	0x00002000	0xA002061C	121
1.3.393	reg : machineconstants_cal_d cmsnrthr	0x00000500	0xA0020620	122
1.3.394	reg : machineconstants_cal_d cmwidththr	0x000004CD	0xA0020624	122
1.3.395	reg : machineconstants_cal_d cmcheckiter	0x00000004	0xA0020628	122
1.3.396	reg : machineconstants_cal_d dmcheckiter	0x00000004	0xA002062C	122
1.3.397	reg : machineconstants_cal_t argetcl	0x0000012C	0xA0020630	122
1.3.398	reg : machineconstants_cal_t argetsubcl_initial	0x0000001E	0xA0020634	122
1.3.399	reg : machineconstants_cal_t argetsubcl_res	0x00000014	0xA0020638	122
1.3.400	reg : machineconstants_cal_t argetsubcl_num	0x00000002	0xA002063C	123
1.3.401	reg : machineconstants_cal_t argetscl_optimized	0x00000022	0xA0020640	123
1.3.402	reg : machineconstants_cal_t ferrthr	0x00008000	0xA0020644	123
1.3.403	reg : machineconstants_cal_t otalvoltage	0x00010400	0xA0020648	123
1.3.404	reg : machineconstants_cal_c ost_weight_p0	0x00010000	0xA002064C	123
1.3.405	reg : machineconstants_cal_c ost_weight_p1	0x00010000	0xA0020650	123
1.3.406	reg : machineconstants_cal_c ost_weight_p2	0x00010000	0xA0020654	123
1.3.407	reg: machineconstants_cal_c ost_weight_p3	0x00010000	0xA0020658	124
1.3.408	reg : machineconstants_cal_c ost_weight_p4	0x00010000	0xA002065C	124
1.3.409	reg : machineconstants_cal_c ost_weight_p5	0x00010000	0xA0020660	124
1.3.410	reg : machineconstants_cal_c ostfunctiondswthr	0x0000CCC	0xA0020664	124
1.3.411	reg : machineconstants_cal_c ostfunctionhwthr	0x0000CCC	0xA0020668	124
1.3.412	reg : machineconstants_cal_f reqdiagnosticnumber	0x00000003	0xA002066C	124
1.3.413	reg : machineconstants_cal_f reqdiagnosticres	0x00002710	0xA0020670	124
1.3.414	reg : machineconstants_cal_m aindropletdiameter	0x001B4CCD	0xA0020674	125
1.3.415	reg : machineconstants_cal_m aindropletvelocity	0x00820000	0xA0020678	125

1.3.416	reg : machineconstants_cal_s atellitediametermindcm	0x00040000	0xA002067C	125
1.3.417	reg : machineconstants_cal_s atellitediameterminddm	0x00060000	0xA0020680	125
1.3.418	reg : machineconstants_cal_d cmlocation	0x00000046	0xA0020684	125
1.3.419	reg : machineconstants_cal_e rrorratiothreshold	0x00008000	0xA0020688	125
1.3.420	reg : machineconstants_cal_b do dc res	0x0000000A	0xA002068C	125
1.3.421	reg : machineconstants_cal_d ragcte	0x00000001	0xA0020690	126
1.3.422	reg : machineconstants_cal_n	0x00000015	0xA0020694	126
1.3.423	um_candidate_soln reg : machineconstants_cal_s	0x00000007	0xA0020698	126
1.3.424	reg: machineconstants_cal_s	0x00000001	0xA002069C	126
1.3.425	reg : machineconstants_cal_s	0x00000014	0xA00206A0	126
1.3.426	pcfg_6 reg : machineconstants_cal_m	0x00000000	0xA00206A4	126
1.3.427	ainfreqopt_type reg : machineconstants_cal_s	0x00000001	0xA00206A8	126
1.3.428	pcfg_8 reg: machineconstants_cal_p	0x0000199A	0xA00206AC	127
1.3.429	kuniformitymax reg : machineconstants_cal_s	0x00000001	0xA00206B0	127
1.3.430	pcfg_10 reg : machineconstants_cal_s	0x0000001E	0xA00206B4	127
1.3.431	pcfg_11 reg : machineconstants_cal_s	0x00000000	0xA00206B8	127
1.3.432	pcfg_12 reg : machineconstants_cal_j	0x00000001	0xA00206BC	127
1.3.433	mpbnddelay reg: machineconstants_cal_s	0x00000003	0xA00206C0	127
1.3.434	pcfg_14 reg : machineconstants_cal_s	0x00000000	0xA00206C4	127
1.3.435	pcfg_15 reg : machineconstants_cal_s	0x00000000	0xA00206C8	127
1.4	pcfg_16 block : algo_egr_registers_s		0xA0030000 - 0xA003D07F	128
	rdl			
1.4.1	reg : algo_egress_module_nam e	0x6F616C67	0xA0030000	128
1.4.2	reg : algo_egress_module_ver sion	0x00000000	0xA0030004	128
1.4.3	reg : algo_egress_page_prope rties	0x80001001	0xA0030008	128
1.4.4	reg : algo_egress_scratchreg ister	0x12345678	0xA003000C	128
1.4.5	reg : algo_egress_irq_enable	0x00000000	0xA0030010	128
1.4.6	reg : algo_egress_irq_pendin g	0x00000000	0xA0030014	128
1.4.7	reg : algo_egress_irq_raw	0x00000000	0xA0030018	129
1.4.8	reg : algo_egress_irq_force	0x00000000	0xA003001C	129
1.4.9	reg : region_1_start_tag	0x00000000	0xA0031000	129
1.4.10	reg : region_1_dtec_tod_lsbs	0x00000000	0xA0031004	129
1.4.11	reg : region_1_dtec_tod_msbs	0x00000000	0xA0031008	129
1.4.12	reg : region_1_dtec_lts	0x00000000	0xA003100C	129
1.4.13	reg : dtec_algo_rev_revision _major	0x00000000	0xA0031010	129
1.4.14	reg : dtec_algo_rev_revision _minor	0x00000000	0xA0031014	130
1.4.15	reg : dtec_algo_rev_revision _patch	0x00000000	0xA0031018	130
1.4.16	reg : spares_spare_uint_1	0x00000000	0xA003101C	130
1.4.17	reg : spares_spare_uint_2	0x00000000	0xA0031020	130

1 1 10		10.00000000	10. 10001001	1400
1.4.18	reg : spares_spare_uint_3	0x00000000	0xA0031024	130
1.4.19	reg : spares_spare_uint_4	0x00000000		130
1.4.20	reg : spares_spare_uint_5	0x00000000		130
1.4.21	reg : spares_spare_uint_6	0x00000000		130
1.4.22	reg : spares_spare_uint_7	0x00000000		131
1.4.23	reg : spares_spare_uint_8	0x00000000		131
1.4.24	reg : spares_spare_uint_9	0x00000000	0xA003103C	131
1.4.25	reg : spares_spare_uint_10	0x00000000	0xA0031040	131
1.4.26	reg : spares_spare_uint_11	0x00000000	0xA0031044	131
1.4.27	reg : spares_spare_uint_12	0x00000000	0xA0031048	131
1.4.28	reg : spares_spare_uint_13	0x00000000	0xA003104C	131
1.4.29	reg : spares_spare_uint_14	0x00000000	0xA0031050	131
1.4.30	reg : spares_spare_uint_15	0x00000000	0xA0031054	132
1.4.31	reg : spares_spare_uint_16	0x00000000	0xA0031058	132
1.4.32	reg : spares_spare_int_1	0x00000000	0xA003105C	132
1.4.33	reg : spares_spare_int_2	0x00000000	0xA0031060	132
1.4.34	reg : spares_spare_int_3	0x00000000		132
1.4.35	reg : spares_spare_int_4	0x00000000		132
1.4.36	reg : spares_spare_int_5	0x00000000		132
1.4.37	reg : spares_spare_int_6	0x00000000		133
1.4.38	reg : spares_spare_int_7	0x00000000		133
1.4.39	reg : spares_spare_int_8	0x00000000		133
1.4.40	reg : spares_spare_int_9		0xA0031076 0xA003107C	133
1.4.41	reg : spares_spare_int_10	0x00000000		133
1.4.42	reg : spares_spare_int_10	0x00000000		133
1.4.42	reg : spares_spare_int_12		0xA0031088	133
1.4.44	reg : spares_spare_int_13	0x00000000		133
1.4.45		0x00000000		134
	reg : spares_spare_int_14			134
1.4.46 1.4.47	reg : spares_spare_int_15	0x00000000		134
	reg : spares_spare_int_16	0x00000000		
1.4.48	reg : spares_spare_ufi_1	0x00000000		134
1.4.49	reg : spares_spare_ufi_2	0x00000000		134
1.4.50	reg : spares_spare_ufi_3	0x00000000		134
1.4.51	reg : spares_spare_ufi_4	0x00000000		134
1.4.52	reg : spares_spare_ufi_5	0x00000000		134
1.4.53	reg : spares_spare_ufi_6	0x00000000		135
1.4.54	reg : spares_spare_ufi_7	0x00000000		135
1.4.55	reg : spares_spare_ufi_8	0x00000000		135
1.4.56	reg : spares_spare_ufi_9	0x00000000		135
1.4.57	reg : spares_spare_ufi_10		0xA00310C0	135
1.4.58	reg : spares_spare_ufi_11	0x00000000		135
1.4.59	reg : spares_spare_ufi_12	0x00000000		135
1.4.60	reg : spares_spare_ufi_13	0x00000000		136
1.4.61	reg : spares_spare_ufi_14	0x00000000		136
1.4.62	reg : spares_spare_ufi_15	0x00000000		136
1.4.63	reg : spares_spare_ufi_16	0x00000000		136
1.4.64	reg : spares_spare_sfi_1	0x00000000		136
1.4.65	reg : spares_spare_sfi_2		0xA00310E0	136
1.4.66	reg : spares_spare_sfi_3	0x00000000		136
1.4.67	reg : spares_spare_sfi_4	0x00000000		136
1.4.68	reg : spares_spare_sfi_5	0x00000000		137
1.4.69	reg : spares_spare_sfi_6	0x00000000	0xA00310F0	137
1.4.70	reg : spares_spare_sfi_7	0x00000000	0xA00310F4	137
1.4.71	reg : spares_spare_sfi_8	0x00000000	0xA00310F8	137
1.4.72	reg : spares_spare_sfi_9	0x00000000	0xA00310FC	137
1.4.73	reg : spares_spare_sfi_10	0x00000000	0xA0031100	137
1.4.74	reg : spares_spare_sfi_11	0x00000000	0xA0031104	137
1.4.75	reg : spares_spare_sfi_12	0x00000000	0xA0031108	137
1.4.76	reg : spares_spare_sfi_13	0x00000000	0xA003110C	138
				138
1.4.77	reg : spares_spare_sfi_14	0x00000000	0240031110	
	reg : spares_spare_sfi_14 reg : spares_spare_sfi_15	0x00000000 0x00000000		138
1.4.77	reg : spares_spare_sfi_15		0xA0031114	
1.4.77 1.4.78 1.4.79	reg : spares_spare_sfi_15 reg : spares_spare_sfi_16	0x00000000	0xA0031114 0xA0031118	138
1.4.77 1.4.78 1.4.79 1.4.80	reg: spares_spare_sfi_15 reg: spares_spare_sfi_16 reg: region_1_end_tag	0x00000000 0x00000000 0x00000000	0xA0031114 0xA0031118 0xA003111C	138 138 138
1.4.77 1.4.78 1.4.79	reg : spares_spare_sfi_15 reg : spares_spare_sfi_16	0x00000000 0x00000000 0x00000000 0x000000	0xA0031114 0xA0031118 0xA003111C	138 138

1.4.84	reg : region_4_dtec_lts	0x00000000		139
1.4.85	reg : dcm_fb_metrics_fb_lm	0x00000000		139
1.4.86	reg : dcm_fb_metrics_fb_tm	0x00000000		139
1.4.87	reg : dcm_fb_metrics_fb_cm	0x00000000	0xA0034018	139
1.4.88	reg : dcm_fb_metrics_fb_dm	0x00000000	0xA003401C	139
1.4.89	reg : dcm_fb_metrics_sigmal	0x00000000	0xA0034020	139
1.4.90	reg : dcm_fb_metrics_sigmat	0x00000000	0xA0034024	139
1.4.91	reg : dcm_fb_metrics_sigmac	0x00000000	0xA0034028	140
1.4.92	reg : dcm fb metrics sigmad	0x00000000	0xA003402C	140
1.4.93	reg : dcm_fb_metrics_maindro	0x00000000	0xA0034030	140
	pletnumber			
1.4.94	reg : dcm_fb_metrics_presubn umber	0x00000000	0xA0034034	140
1.4.95	reg : dcm_fb_metrics_multpre subnumber	0x00000000	0xA0034038	140
1.4.96	reg : dcm_fb_metrics_leftpea kmissednumber	0x00000000	0xA003403C	140
1.4.97	reg : dcm_fb_metrics_rightpe akmissednumber	0x00000000	0xA0034040	140
1.4.98	reg : dcm_fb_metrics_timesta	0x00000000	0xA0034044	141
1.4.99	mp_tod_lsb reg : dcm_fb_metrics_timesta		0xA0034048	141
	mp_tod_msb	0x00000000		
1.4.100	reg : dcm_fb_metrics_timesta mp_lts	0x00000000	0xA003404C	141
1.4.101	reg : region_4_end_tag	0x00000000		141
1.4.102	reg : region_5_start_tag	0x00000000		141
1.4.103	reg : region_5_dtec_tod_lsbs	0x00000000	0xA0035004	141
1.4.104	reg : region_5_dtec_tod_msbs	0x00000000	0xA0035008	141
1.4.105	reg : region_5_dtec_lts	0x00000000	0xA003500C	141
1.4.106	reg : ddm_fb_metrics_maindro pletnumber	0x00000000	0xA0035010	142
1.4.107	reg : ddm_fb_metrics_satelli terate	0x00000000	0xA0035014	142
1.4.108	reg : ddm_fb_metrics_xint3si gma	0x00000000	0xA0035018	142
1.4.109	reg : ddm_fb_metrics_xintmea	0x00000000	0xA003501C	142
1.4.110	reg : ddm_fb_metrics_mainpea k	0x00000000	0xA0035020	142
1.4.111	reg : ddm_fb_metrics_pf_expo suredc	0x00000000	0xA0035024	142
1.4.112	reg : ddm_fb_metrics_signalq uality	0x00000000	0xA0035028	142
1.4.113	reg : ddm_fb_metrics_timesta mp_tod_lsb	0x00000000	0xA003502C	143
1.4.114	reg : ddm_fb_metrics_timesta mp_tod_msb	0x00000000	0xA0035030	143
1.4.115	reg : ddm_fb_metrics_timesta mp_lts	0x00000000	0xA0035034	143
1.4.116	reg : region_5_end_tag	0x00000000	0xA0035038	143
1.4.117	reg : region_6_start_tag	0x00000000	0xA0036000	143
1.4.118	reg : region_6_dtec_tod_lsbs	0x00000000	0xA0036004	143
1.4.119	reg : region_6_dtec_tod_msbs	0x00000000		143
1.4.120	reg : region_6_dtec_lts	0x00000000	0xA003600C	143
1.4.121	reg:	0x00000000	0xA0036010	144
	damp_waveformparamspkg _damp_signals_1			
1.4.122	reg:	0x00000000	0xA0036014	144
	damp_waveformparamspkg _damp_signals_2			
1.4.123	reg:	0x00000000	0xA0036018	144
20	damp_waveformparamspkg _damp_signals_3			
1.4.124	reg:	0x00000000	0xA003601C	144
	damp_waveformparamspkg _damp_signals_4			

4 4 405		0.0000000	0.4000000	
1.4.125	reg: damp_waveformparamspkg _damp_signals_5	0x00000000	0xA0036020	144
1.4.126	reg: damp_waveformparamspkg _damp_signals_6	0x00000000	0xA0036024	144
1.4.127	reg : damp_waveformparamspkg	0x00000000	0xA0036028	144
1.4.128	_damp_signals_7 reg: damp_waveformparamspkg	0x00000000	0xA003602C	145
1.4.129	_damp_signals_8 reg: damp_waveformparamspkg	0x00000000	0xA0036030	145
1.4.130	_damp_signals_9 reg: damp_waveformparamspkg	0x00000000	0xA0036034	145
1.4.131	_damp_signals_10 reg: damp_waveformparamspkg	0x00000000	0xA0036038	145
1.4.132	_damp_signals_11 reg: damp_waveformparamspkg	0x00000000	0xA003603C	145
1.4.133	_damp_signals_12 reg: damp_waveformparamspkg	0x00000000	0xA0036040	145
1.4.134	_damp_signals_13 reg: damp_waveformparamspkg	0x00000000	0xA0036044	146
1.4.135	_damp_signals_14 reg: damp_waveformparamspkg	0x00000000	0xA0036048	146
1.4.136	_damp_signals_15 reg: damp_waveformparamspkg	0x00000000	0xA003604C	146
1.4.137	_damp_signals_16 reg: damp_waveformparamspkg	0x00000000	0xA0036050	146
1.4.138	_damp_signals_17 reg: damp_waveformparamspkg	0x00000000	0xA0036054	146
1.4.139	damp_signals_18  reg: damp_waveformparamspkg	0x00000000	0xA0036058	146
1.4.140	_damp_signals_19 reg:	0x00000000	0xA003605C	146
1.4.141	damp_waveformparamspkg _damp_signals_20 reg:	0x00000000	0xA0036060	147
	damp_waveformparamspkg _damp_signals_21			
1.4.142	reg : damp_waveformparamspkg _damp_signals_22	0x00000000	0xA0036064	147
1.4.143	reg : damp_waveformparamspkg _damp_signals_23	0x00000000	0xA0036068	147
1.4.144	reg: damp_waveformparamspkg _damp_signals_24	0x00000000	0xA003606C	147
1.4.145	reg: damp_waveformparamspkg _damp_signals_25	0x00000000	0xA0036070	147
1.4.146	reg : damp_waveformparamspkg _damp_signals_26	0x00000000	0xA0036074	147
1.4.147	reg : damp_waveformparamspkg _damp_signals_27	0x00000000	0xA0036078	147

1.4.148	reg: damp_waveformparamspkg _damp_signals_28	0x00000000	0xA003607C	148
1.4.149	reg : damp_waveformparamspkg _damp_signals_29	0x00000000	0xA0036080	148
1.4.150	reg : damp_waveformparamspkg _damp_signals_30	0x00000000	0xA0036084	148
1.4.151	reg: damp_waveformparamspkg _damp_signals_31	0x00000000	0xA0036088	148
1.4.152	reg : damp_waveformparamspkg _damp_signals_32	0x00000000	0xA003608C	148
1.4.153	reg : damp_waveformparamspkg _damp_signals_33	0x00000000	0xA0036090	148
1.4.154	reg : damp_waveformparamspkg _damp_signals_34	0x00000000	0xA0036094	148
1.4.155	reg: damp_waveformparamspkg _damp_signals_35	0x00000000	0xA0036098	149
1.4.156	reg : damp_waveformparamspkg _damp_signals_36	0x00000000	0xA003609C	149
1.4.157	reg : damp_waveformparamspkg _damp_signals_37	0x00000000	0xA00360A0	149
1.4.158	reg : damp_waveformparamspkg _damp_signals_38	0x00000000	0xA00360A4	149
1.4.159	reg : damp_waveformparamspkg _damp_signals_39	0x00000000	0xA00360A8	149
1.4.160	reg : damp_waveformparamspkg _damp_signals_40	0x00000000	0xA00360AC	149
1.4.161	reg: damp_waveformparamspkg _damp_signals_41	0x00000000	0xA00360B0	149
1.4.162	reg: damp_waveformparamspkg _damp_signals_42	0x00000000	0xA00360B4	150
1.4.163	reg: damp_waveformparamspkg _damp_signals_43	0x00000000	0xA00360B8	150
1.4.164	reg: damp_waveformparamspkg _damp_signals_44	0x00000000	0xA00360BC	150
1.4.165	reg : damp_waveformparamspkg _damp_signals_45	0x00000000	0xA00360C0	150
1.4.166	reg: damp_waveformparamspkg _damp_signals_46	0x00000000	0xA00360C4	150
1.4.167	reg : damp_waveformparamspkg _damp_signals_47	0x00000000	0xA00360C8	150
1.4.168	reg: damp_waveformparamspkg _damp_signals_48	0x00000000	0xA00360CC	150
1.4.169	reg : damp_waveformparamspkg _damp_signals_49	0x00000000	0xA00360D0	151
1.4.170	reg: damp_waveformparamspkg _damp_signals_50	0x00000000	0xA00360D4	151

		0.0000000	la 4000000	1.5.
1.4.171	reg : damp_waveformparamspkg _damp_signals_51	0x00000000	0xA00360D8	151
1.4.172	reg : damp_waveformparamspkg _damp_signals_52	0x00000000	0xA00360DC	151
1.4.173	reg : damp_waveformparamspkg _damp_signals_53	0x00000000	0xA00360E0	151
1.4.174	reg : damp_waveformparamspkg _damp_signals_54	0x00000000	0xA00360E4	151
1.4.175	reg : damp_waveformparamspkg _damp_signals_55	0x00000000	0xA00360E8	151
1.4.176	reg : damp_waveformparamspkg _damp_signals_56	0x00000000	0xA00360EC	152
1.4.177	reg: damp_waveformparamspkg	0x00000000	0xA00360F0	152
1.4.178	damp_signals_57  reg : damp_waveformparamspkg _damp_signals_58	0x00000000	0xA00360F4	152
1.4.179	reg : damp_waveformparamspkg _damp_signals_59	0x00000000	0xA00360F8	152
1.4.180	reg : damp_waveformparamspkg _damp_signals_60	0x00000000	0xA00360FC	152
1.4.181	reg : damp_waveformparamspkg _damp_signals_61	0x00000000	0xA0036100	152
1.4.182	reg : damp_waveformparamspkg _damp_signals_62	0x00000000	0xA0036104	153
1.4.183	reg : damp_waveformparamspkg _damp_signals_63	0x00000000	0xA0036108	153
1.4.184	reg : damp_waveformparamspkg _damp_signals_64	0x00000000	0xA003610C	153
1.4.185	reg : damp_waveformparamspkg damp_signals_65	0x00000000	0xA0036110	153
1.4.186	reg : damp_waveformparamspkg _damp_signals_66	0x00000000	0xA0036114	153
1.4.187	reg : damp_waveformparamspkg _damp_signals_67	0x00000000	0xA0036118	153
1.4.188	reg : damp_waveformparamspkg _damp_signals_68	0x00000000	0xA003611C	153
1.4.189	reg : damp_waveformparamspkg _damp_signals_69	0x00000000	0xA0036120	154
1.4.190	reg : damp_waveformparamspkg _damp_signals_70	0x00000000	0xA0036124	154
1.4.191	reg : damp_waveformparamspkg _damp_signals_71	0x00000000	0xA0036128	154
1.4.192	reg : damp_waveformparamspkg _damp_signals_72	0x00000000	0xA003612C	154
1.4.193	reg : damp_waveformparamspkg _damp_signals_73	0x00000000	0xA0036130	154

1.4.194	reg:	0x00000000	0xA0036134	154
1.4.104	damp_waveformparamspkg _damp_signals_74	0.00000000	OA 10000104	10-4
1.4.195	reg : damp_waveformparamspkg _damp_signals_75	0x00000000	0xA0036138	154
1.4.196	reg : damp_waveformparamspkg _damp_signals_76	0x00000000	0xA003613C	155
1.4.197	reg : damp_waveformparamspkg _damp_signals_77	0x00000000	0xA0036140	155
1.4.198	reg : damp_waveformparamspkg _damp_signals_78	0x00000000	0xA0036144	155
1.4.199	reg : damp_waveformparamspkg _damp_signals_79	0x00000000	0xA0036148	155
1.4.200	reg: damp_waveformparamspkg	0x00000000	0xA003614C	155
1.4.201	_damp_signals_80 reg : damp_waveformparamspkg	0x00000000	0xA0036150	155
1.4.202	_damp_signals_81  reg : damp_waveformparamspkg	0x00000000	0xA0036154	155
1.4.203	_damp_signals_82 reg : damp_waveformparamspkg	0x00000000	0xA0036158	156
1.4.204	_damp_signals_83 reg : damp_waveformparamspkg	0x00000000	0xA003615C	156
1.4.205	_damp_signals_84 reg : damp_waveformparamspkg	0x00000000	0xA0036160	156
1.4.206	_damp_signals_85 reg : damp_waveformparamspkg	0x00000000	0xA0036164	156
1.4.207	_damp_signals_86 reg : damp_waveformparamspkg	0x00000000	0xA0036168	156
1.4.208	damp_signals_87  reg : damp_waveformparamspkg _damp_signals_88	0x00000000	0xA003616C	156
1.4.209	reg : damp_waveformparamspkg _damp_signals_89	0x00000000	0xA0036170	156
1.4.210	reg : damp_waveformparamspkg _damp_signals_90	0x00000000	0xA0036174	157
1.4.211	reg : damp_waveformparamspkg _damp_signals_91	0x00000000	0xA0036178	157
1.4.212	reg : damp_waveformparamspkg _damp_signals_92	0x00000000	0xA003617C	157
1.4.213	reg : damp_waveformparamspkg _damp_signals_93	0x00000000	0xA0036180	157
1.4.214	reg : damp_waveformparamspkg _damp_signals_94	0x00000000	0xA0036184	157
1.4.215	reg : damp_waveformparamspkg _damp_signals_95	0x00000000	0xA0036188	157
1.4.216	reg : damp_waveformparamspkg _damp_signals_96	0x00000000	0xA003618C	157

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1.4.217	reg : damp_waveformparamspkg _damp_signals_97	0x00000000	0xA0036190	158
1.4.218	reg : damp_waveformparamspkg _damp_signals_98	0x00000000	0xA0036194	158
1.4.219	reg : damp_waveformparamspkg _damp_signals_99	0x00000000	0xA0036198	158
1.4.220	reg: damp_waveformparamspkg _damp_signals_100	0x00000000	0xA003619C	158
1.4.221	reg : damp_waveformparamspkg _damp_signals_101	0x00000000	0xA00361A0	158
1.4.222	reg : damp_waveformparamspkg _damp_signals_102	0x00000000	0xA00361A4	158
1.4.223	reg: damp_waveformparamspkg	0x00000000	0xA00361A8	158
1.4.224	_damp_signals_103 reg : damp_waveformparamspkg	0x00000000	0xA00361AC	159
1.4.225	_damp_signals_104 reg : damp_waveformparamspkg	0x00000000	0xA00361B0	159
1.4.226	damp_signals_105 reg: damp_waveformparamspkg _damp_signals_106	0x00000000	0xA00361B4	159
1.4.227	reg : damp_waveformparamspkg	0x00000000	0xA00361B8	159
1.4.228	damp_signals_107 reg: damp_waveformparamspkg _damp_signals_108	0x00000000	0xA00361BC	159
1.4.229	reg : damp_waveformparamspkg _damp_signals_109	0x00000000	0xA00361C0	159
1.4.230	reg : damp_waveformparamspkg _damp_signals_110	0x00000000	0xA00361C4	160
1.4.231	reg : damp_waveformparamspkg _damp_signals_111	0x00000000	0xA00361C8	160
1.4.232	reg : damp_waveformparamspkg _damp_signals_112	0x00000000	0xA00361CC	160
1.4.233	reg : damp_waveformparamspkg _damp_signals_113	0x00000000	0xA00361D0	160
1.4.234	reg : damp_waveformparamspkg _damp_signals_114	0x00000000	0xA00361D4	160
1.4.235	reg : damp_waveformparamspkg _damp_signals_115	0x00000000	0xA00361D8	160
1.4.236	reg : damp_waveformparamspkg _damp_signals_116	0x00000000	0xA00361DC	160
1.4.237	reg : damp_waveformparamspkg _damp_signals_117	0x00000000	0xA00361E0	161
1.4.238	reg : damp_waveformparamspkg _damp_signals_118	0x00000000	0xA00361E4	161
1.4.239	reg : damp_waveformparamspkg _damp_signals_119	0x00000000	0xA00361E8	161

1.4.240	reg : damp_waveformparamspkg	0x00000000	0xA00361EC	161
4 4 0 4 4	_damp_signals_120	000000000	040000450	404
1.4.241	reg : damp_waveformparamspkg _damp_signals_121	0x00000000	0xA00361F0	161
1.4.242	reg : damp_waveformparamspkg _damp_signals_122	0x00000000	0xA00361F4	161
1.4.243	reg : damp_waveformparamspkg	0x00000000	0xA00361F8	161
1.4.244	_damp_signals_123 reg: damp_waveformparamspkg	0x00000000	0xA00361FC	162
	_damp_signals_124			
1.4.245	reg : damp_waveformparamspkg _damp_signals_125	0x00000000	0xA0036200	162
1.4.246	reg : damp_waveformparamspkg _damp_signals_126	0x00000000	0xA0036204	162
1.4.247	reg : damp_waveformparamspkg _damp_signals_127	0x00000000	0xA0036208	162
1.4.248	reg : damp_waveformparamspkg _damp_signals_128	0x00000000	0xA003620C	162
1.4.249	reg : region_6_end_tag	0x00000000	0xA0036210	162
1.4.250	reg : region_7_start_tag	0x00000000		162
1.4.251	reg : region_7_dtec_tod_lsbs	0x00000000		163
1.4.252	reg : region_7_dtec_tod_msbs	0x00000000		163
1.4.253	reg : region_7_dtec_lts	0x00000000	0xA003700C	163
1.4.254	reg : solutiontable_out_solu	0x00000000	0xA0037000	163
	tiontype			
1.4.255	reg : solutiontable_out_hype rparameters_1	0x00000000	0xA0037014	163
1.4.256	reg : solutiontable_out_hype rparameters_2	0x00000000	0xA0037018	163
1.4.257	reg : solutiontable_out_hype rparameters_3	0x00000000	0xA003701C	164
1.4.258	reg : solutiontable_out_hype rparameters_4	0x00000000	0xA0037020	164
1.4.259	reg : solutiontable_out_sine amps_1	0x00000000	0xA0037024	164
1.4.260	reg : solutiontable_out_sine amps_2	0x00000000	0xA0037028	164
1.4.261	reg : solutiontable_out_phi0	0x00000000	0xA003702C	164
1.4.262	reg : solutiontable_out_phi0	0x00000000	0xA0037030	164
1.4.263	reg : solutiontable_out_phi0	0x00000000	0xA0037034	165
1.4.264	reg : solutiontable_out_phi0 4	0x00000000	0xA0037038	165
1.4.265	reg : solutiontable_out_phi0 _5	0x00000000	0xA003703C	165
1.4.266	reg : solutiontable_out_phi0	0x00000000	0xA0037040	165
1.4.267	reg : solutiontable_out_phi0 _7	0x00000000	0xA0037044	165
1.4.268	reg : solutiontable_out_phi0 _8	0x00000000	0xA0037048	165
1.4.269	reg : solutiontable_out_phi0	0x00000000	0xA003704C	165
1.4.270	reg : solutiontable_out_phi0	0x00000000	0xA0037050	166
1.4.271	reg : solutiontable_out_phi0 _11	0x00000000	0xA0037054	166

1.4.272	reg : solutiontable_out_phi0 _12	0x00000000	0xA0037058	166
1.4.273	reg : solutiontable_out_phi0 _13	0x00000000	0xA003705C	166
1.4.274	reg : solutiontable_out_phi0	0x00000000	0xA0037060	166
1.4.275	reg : solutiontable_out_phi0	0x00000000	0xA0037064	166
1.4.276	reg : solutiontable_out_phi0	0x00000000	0xA0037068	166
1.4.277	16 reg : solutiontable_out_phi0	0x00000000	0xA003706C	166
1.4.278	17 reg : solutiontable_out_phi0	0x00000000	0xA0037070	167
1.4.279	18 reg : solutiontable_out_phi0	0x00000000	0xA0037074	167
1.4.280	19 reg : solutiontable_out_phi1	0x00000000	0xA0037078	167
1.4.281	reg : solutiontable_out_phi1	0x00000000	0xA003707C	167
1.4.282	2 reg : solutiontable_out_phi1	0x00000000	0xA0037080	167
1.4.283		0x00000000	0xA0037084	167
1.4.284		0x00000000	0xA0037088	167
1.4.285	5 reg : solutiontable_out_phi1	0x00000000	0xA003708C	168
1.4.286	6 reg : solutiontable_out_phi1	0x00000000	0xA0037090	168
1.4.287		0x00000000	0xA0037094	168
1.4.288	_8 reg : solutiontable_out_phi1	0x00000000	0xA0037098	168
1.4.289	_9 reg : solutiontable_out_phi1	0x00000000	0xA003709C	168
1.4.290	_10 reg : solutiontable_out_phi1	0x00000000	0xA00370A0	168
1.4.291	11 reg : solutiontable_out_phi1	0x00000000	0xA00370A4	169
1.4.292	12 reg : solutiontable_out_phi1	0x00000000	0xA00370A8	169
1.4.293	13 reg : solutiontable_out_phi1	0x00000000	0xA00370AC	169
1.4.294	_14 reg : solutiontable_out_phi1	0x00000000	0xA00370B0	169
1.4.295	_15 reg : solutiontable_out_phi1	0x00000000	0xA00370B4	169
1.4.296	_16 reg : solutiontable_out_phi1	0x0000000	0xA00370B8	169
1.4.297	_17 reg : solutiontable_out_phi1	0x00000000	0xA00370BC	170
1.4.298	_18 reg : solutiontable_out_phi1	0x00000000	0xA00370C0	170
	_19			
1.4.299	reg : solutiontable_out_pres ubcoal_flag_1	0x00000000	0xA00370C4	170
1.4.300	reg : solutiontable_out_pres ubcoal_flag_2	0x00000000	0xA00370C8	170
1.4.301	reg : solutiontable_out_pres ubcoal_flag_3	0x00000000	0xA00370CC	170
1.4.302	reg : solutiontable_out_pres ubcoal_flag_4	0x00000000	0xA00370D0	170
1.4.303	reg : solutiontable_out_pres ubcoal_flag_5	0x00000000	0xA00370D4	171
1.4.304	reg : solutiontable_out_pres ubcoal_flag_6	0x00000000	0xA00370D8	171
1.4.305	reg : solutiontable_out_pres ubcoal_flag_7	0x00000000	0xA00370DC	171

1.4.306	reg : solutiontable_out_pres ubcoal_flag_8	0x00000000	0xA00370E0	171
1.4.307	reg : solutiontable_out_pres ubcoal_flag_9	0x00000000	0xA00370E4	171
1.4.308	reg : solutiontable_out_pres ubcoal_flag_10	0x00000000	0xA00370E8	171
1.4.309	reg : solutiontable_out_pres	0x00000000	0xA00370EC	172
1.4.310	ubcoal_flag_11 reg : solutiontable_out_pres	0x00000000	0xA00370F0	172
1.4.311	ubcoal_flag_12 reg : solutiontable_out_pres	0x00000000	0xA00370F4	172
1.4.312	ubcoal_flag_13 reg : solutiontable_out_pres	0x00000000	0xA00370F8	172
1.4.313	ubcoal_flag_14 reg : solutiontable_out_pres	0x00000000	0xA00370FC	172
1.4.314	ubcoal_flag_15 reg : solutiontable_out_pres	0x00000000	0xA0037100	172
1.4.315	ubcoal_flag_16 reg : solutiontable_out_pres	0x00000000	0xA0037104	173
	ubcoal_flag_17			
1.4.316	reg : solutiontable_out_pres ubcoal_flag_18	0x00000000	0xA0037108	173
1.4.317	reg : solutiontable_out_pres ubcoal_flag_19	0x00000000	0xA003710C	173
1.4.318	reg : solutiontable_out_jitt er_1	0x00000000	0xA0037110	173
1.4.319	reg : solutiontable_out_jitt er_2	0x00000000	0xA0037114	173
1.4.320	reg : solutiontable_out_jitt er_3	0x00000000	0xA0037118	174
1.4.321	reg : solutiontable_out_jitt er_4	0x00000000	0xA003711C	174
1.4.322	reg : solutiontable_out_jitt er_5	0x00000000	0xA0037120	174
1.4.323	reg : solutiontable_out_jitt er_6	0x00000000	0xA0037124	174
1.4.324	reg : solutiontable_out_jitt er_7	0x00000000	0xA0037128	175
1.4.325	reg : solutiontable_out_jitt er 8	0x00000000	0xA003712C	175
1.4.326	reg : solutiontable_out_jitt er_9	0x00000000	0xA0037130	175
1.4.327	reg : solutiontable_out_jitt er_10	0x00000000	0xA0037134	175
1.4.328	reg : solutiontable_out_jitt er_11	0x00000000	0xA0037138	176
1.4.329	reg : solutiontable_out_jitt er_12	0x00000000	0xA003713C	176
1.4.330	reg : solutiontable_out_jitt	0x00000000	0xA0037140	176
1.4.331	er_13 reg : solutiontable_out_jitt	0x00000000	0xA0037144	176
1.4.332	er_14 reg : solutiontable_out_jitt	0x00000000	0xA0037148	177
1.4.333	er_15 reg : solutiontable_out_jitt	0x00000000	0xA003714C	177
1.4.334	er_16 reg : solutiontable_out_jitt	0x00000000	0xA0037150	177
1.4.335	er_17 reg : solutiontable_out_jitt	0x00000000	0xA0037154	177
1.4.336	er_18 reg : solutiontable_out_jitt	0x00000000	0xA0037158	178
1.4.337	er_19 reg : solutiontable_out_mult	0x00000000	0xA003715C	178
1.4.338	presubrate_1 reg : solutiontable_out_mult	0x00000000	0xA0037160	178
	presubrate_2 reg : solutiontable_out_mult			178
1.4.339	presubrate_3	0x00000000	0xA0037164	170

1.4.340	reg : solutiontable_out_mult presubrate_4	0x00000000	0xA0037168	178
1.4.341	reg : solutiontable_out_mult presubrate_5	0x00000000	0xA003716C	178
1.4.342	reg : solutiontable_out_mult presubrate_6	0x00000000	0xA0037170	179
1.4.343	reg : solutiontable_out_mult	0x00000000	0xA0037174	179
1.4.344	presubrate_7 reg : solutiontable_out_mult	0x00000000	0xA0037178	179
1.4.345	presubrate_8 reg : solutiontable_out_mult	0x00000000	0xA003717C	179
1.4.346	presubrate_9 reg : solutiontable_out_mult	0x00000000	0xA0037180	179
1.4.347	presubrate_10 reg : solutiontable_out_mult	0x00000000	0xA0037184	179
1.4.348	presubrate_11 reg : solutiontable_out_mult	0x00000000	0xA0037188	179
1.4.349	presubrate_12 reg : solutiontable_out_mult	0x00000000	0xA003718C	180
	presubrate_13			
1.4.350	reg : solutiontable_out_mult presubrate_14	0x00000000	0xA0037190	180
1.4.351	reg : solutiontable_out_mult presubrate_15	0x00000000	0xA0037194	180
1.4.352	reg : solutiontable_out_mult presubrate_16	0x00000000	0xA0037198	180
1.4.353	reg : solutiontable_out_mult presubrate_17	0x00000000	0xA003719C	180
1.4.354	reg : solutiontable_out_mult presubrate_18	0x00000000	0xA00371A0	180
1.4.355	reg : solutiontable_out_mult presubrate_19	0x00000000	0xA00371A4	180
1.4.356	reg : solutiontable_out_pres ubrate_1	0x00000000	0xA00371A8	181
1.4.357	reg : solutiontable_out_pres ubrate_2	0x00000000	0xA00371AC	181
1.4.358	reg : solutiontable_out_pres ubrate_3	0x00000000	0xA00371B0	181
1.4.359	reg : solutiontable_out_pres ubrate 4	0x00000000	0xA00371B4	181
1.4.360	reg : solutiontable_out_pres ubrate_5	0x00000000	0xA00371B8	181
1.4.361	reg : solutiontable_out_pres ubrate_6	0x00000000	0xA00371BC	181
1.4.362	reg : solutiontable_out_pres ubrate_7	0x00000000	0xA00371C0	181
1.4.363	reg : solutiontable_out_pres ubrate_8	0x00000000	0xA00371C4	181
1.4.364	reg : solutiontable_out_pres	0x00000000	0xA00371C8	182
1.4.365	ubrate_9 reg : solutiontable_out_pres	0x00000000	0xA00371CC	182
1.4.366	ubrate_10 reg : solutiontable_out_pres	0x00000000	0xA00371D0	182
1.4.367	ubrate_11 reg : solutiontable_out_pres	0x00000000	0xA00371D4	182
1.4.368	ubrate_12 reg : solutiontable_out_pres	0x00000000	0xA00371D8	182
1.4.369	ubrate_13 reg : solutiontable_out_pres	0x00000000	0xA00371DC	182
1.4.370	ubrate_14 reg : solutiontable_out_pres	0x00000000	0xA00371E0	182
1.4.371	ubrate_15 reg : solutiontable_out_pres	0x00000000	0xA00371E4	183
1.4.372	ubrate_16 reg : solutiontable_out_pres	0x00000000	0xA00371E8	183
1.4.373	ubrate_17 reg : solutiontable_out_pres	0x0000000	0xA00371EC	183
1.4.3/3	ubrate_18	0.000000000	OAAOOS/ TEO	100

1.4.374	reg : solutiontable_out_pres	0x00000000	0xA00371F0	183
1.4.375	ubrate_19	0x00000000	0×4,00274.54	102
1.4.375	reg : solutiontable_out_cm_1	0x00000000	0xA00371F4 0xA00371F8	183 183
1.4.376	reg : solutiontable_out_cm_2 reg : solutiontable_out_cm_3	0x00000000	0xA00371F8	183
1.4.377	reg : solutiontable_out_cm_4	0x00000000	0xA00371FC	184
1.4.376	reg : solutiontable_out_cm_5	0x00000000	0xA0037200 0xA0037204	184
1.4.380	reg : solutiontable_out_cm_6	0x00000000	0xA0037204 0xA0037208	184
1.4.381	reg : solutiontable_out_cm_o	0x00000000	0xA0037200	184
1.4.382	reg : solutiontable_out_cm_/	0x00000000	0xA0037200	184
1.4.383	reg : solutiontable_out_cm_9	0x00000000	0xA0037210	184
1.4.384	reg : solutiontable_out_cm_1	0x00000000	0xA0037214	184
	0			
1.4.385	reg : solutiontable_out_cm_1 1	0x00000000	0xA003721C	184
1.4.386	reg : solutiontable_out_cm_1 2	0x00000000	0xA0037220	185
1.4.387	reg : solutiontable_out_cm_1 3	0x00000000	0xA0037224	185
1.4.388	reg : solutiontable_out_cm_1 4	0x00000000	0xA0037228	185
1.4.389	reg : solutiontable_out_cm_1 5	0x00000000	0xA003722C	185
1.4.390	reg : solutiontable_out_cm_1 6	0x00000000	0xA0037230	185
1.4.391	reg : solutiontable_out_cm_1 7	0x00000000	0xA0037234	185
1.4.392	reg : solutiontable_out_cm_1 8	0x00000000	0xA0037238	185
1.4.393	reg : solutiontable_out_cm_1 9	0x00000000	0xA003723C	186
1.4.394	reg : solutiontable_out_dm_1	0x00000000	0xA0037240	186
1.4.395	reg : solutiontable_out_dm_2	0x00000000	0xA0037244	186
1.4.396	reg : solutiontable_out_dm_3	0x00000000	0xA0037248	186
1.4.397	reg : solutiontable_out_dm_4	0x00000000	0xA003724C	186
1.4.398	reg : solutiontable_out_dm_5	0x00000000	0xA0037250	186
1.4.399	reg : solutiontable_out_dm_6	0x00000000	0xA0037254	186
1.4.400	reg : solutiontable_out_dm_7	0x00000000	0xA0037258	186
1.4.401 1.4.402	reg : solutiontable_out_dm_8 reg : solutiontable_out_dm_9	0x00000000	0xA003725C	187
		0x00000000 0x00000000	0xA0037260	187
1.4.403	reg : solutiontable_out_dm_1 0		0xA0037264	187
1.4.404	reg : solutiontable_out_dm_1 1	0x00000000	0xA0037268	187
1.4.405	reg : solutiontable_out_dm_1 2	0x00000000	0xA003726C	187
1.4.406	reg : solutiontable_out_dm_1 3	0x00000000	0xA0037270	187
1.4.407	reg : solutiontable_out_dm_1 4	0x00000000	0xA0037274	187
1.4.408	reg : solutiontable_out_dm_1 5	0x00000000	0xA0037278	187
1.4.409	reg : solutiontable_out_dm_1 6	0x00000000	0xA003727C	188
1.4.410	reg : solutiontable_out_dm_1 7	0x00000000	0xA0037280	188
1.4.411	reg : solutiontable_out_dm_1 8	0x00000000	0xA0037284	188
1.4.412	reg : solutiontable_out_dm_1 9	0x00000000	0xA0037288	188
1.4.413	reg : solutiontable_out_dcdp hi	0x00000000	0xA003728C	188
1.4.414	reg : solutiontable_out_phi1 margin_1	0x00000000	0xA0037290	188
1.4.415	reg : solutiontable_out_phi1 margin_2	0x00000000	0xA0037294	188
1.4.416	reg : solutiontable_out_phi1 margin_3	0x00000000	0xA0037298	189

1.4.417	reg : solutiontable_out_phi1 margin_4	0x00000000	0xA003729C	189
1.4.418	reg : solutiontable_out_phi1 margin_5	0x00000000	0xA00372A0	189
1.4.419	reg : solutiontable_out_phi1 margin_6	0x00000000	0xA00372A4	189
1.4.420	reg : solutiontable_out_phi1 margin_7	0x00000000	0xA00372A8	189
1.4.421	reg : solutiontable_out_phi1 margin_8	0x00000000	0xA00372AC	189
1.4.422	reg : solutiontable_out_phi1 margin_9	0x00000000	0xA00372B0	190
1.4.423	reg : solutiontable_out_phi1 margin_10	0x00000000	0xA00372B4	190
1.4.424	reg : solutiontable_out_phi1 margin_11	0x00000000	0xA00372B8	190
1.4.425	reg : solutiontable_out_phi1 margin_12	0x00000000	0xA00372BC	190
1.4.426	reg : solutiontable_out_phi1 margin_13	0x00000000	0xA00372C0	190
1.4.427	reg : solutiontable_out_phi1 margin_14	0x00000000	0xA00372C4	190
1.4.428	reg : solutiontable_out_phi1 margin_15	0x00000000	0xA00372C8	190
1.4.429	reg : solutiontable_out_phi1 margin_16	0x00000000	0xA00372CC	191
1.4.430	reg : solutiontable_out_phi1 margin_17	0x00000000	0xA00372D0	191
1.4.431	reg : solutiontable_out_phi1 margin_18	0x00000000	0xA00372D4	191
1.4.432	reg : solutiontable_out_phi1 margin_19	0x00000000	0xA00372D8	191
1.4.433	reg : solutiontable_out_phi0 margin	0x00000000	0xA00372DC	191
1.4.434	reg : solutiontable_out_satr ateavg_off	0x00000000	0xA00372E0	191
1.4.435	reg : solutiontable_out_satr ateavg_on	0x00000000	0xA00372E4	192
1.4.436	reg : solutiontable_out_xint 3sigma_avg	0x00000000	0xA00372E8	192
1.4.437	reg : solutiontable_out_pres ubrate_avg	0x00000000	0xA00372EC	192
1.4.438	reg : solutiontable_out_opt_ solution	0x00000000	0xA00372F0	192
1.4.439	reg : solutiontable_out_bk_s olution	0x00000000	0xA00372F4	192
1.4.440	reg : region_7_end_tag	0x00000000	0xA00372F8	192
1.4.441	reg : region_8_start_tag	0x00000000		192
1.4.442	reg : region 8 dtec tod Isbs		0xA0038004	193
1.4.443	reg : region_8_dtec_tod_msbs	0x00000000		193
1.4.444	reg : region_8_dtec_lts	0x00000000		193
1.4.445	reg : region_o_dtec_its	0x00000000		193
1.4.446	reg : state		0xA0038014	193
1.4.447	reg:test_probes_probe1	0x00000000		193
1.4.448	reg : test_probes_probe2	0x00000000		193
1.4.449	reg : test_probes_probe3	0x00000000	0xA0038020	193
1.4.450	reg : internal_clst_done_lat ched	0x00000000	0xA0038024	194
1.4.451	reg : diag_exposure_preriset ime	0x00000000	0xA0038028	194
1.4.452	reg : diag_exposure_exposure flag	0x00000000	0xA003802C	194
	_1149		0xA0038030	194
1.4.453	reg : diag_exposure_falltime _flag	0x00000000	UXAUU36U3U	154
1.4.453 1.4.454	reg : diag_exposure_falltime	0x00000000 0x00000000	0xA0038034	194
	reg : diag_exposure_falltime _flag reg : diag_exposure_risetime	0x00000000		

1.4.457	reg : xer_out_xer_bank2	0x00000000	0xA0038040	195
1.4.458	reg : events_out_events_bank	0x00000000	0xA0038044	195
1.4.459	reg : events_out_events_bank	0x00000000	0xA0038048	195
1.4.460	reg : warnings_out_warnings_ bank1	0x00000000	0xA003804C	195
1.4.461	reg : warnings_out_warnings_ bank2	0x00000000	0xA0038050	195
1.4.462	reg : region_8_end_tag	0x00000000	0xA0038054	195
1.4.463	reg : region_9_start_tag	0x00000000	0xA0039000	195
1.4.464	reg : region_9_dtec_tod_lsbs	0x00000000	0xA0039004	195
1.4.465	reg : region_9_dtec_tod_msbs	0x00000000	0xA0039008	196
1.4.466	reg : region_9_dtec_lts	0x00000000	0xA003900C	196
1.4.467	reg : dcm_diag_missing_dropl ets	0x00000000	0xA0039010	196
1.4.468	reg : dcm_diag_pklabels_roi1 _1	0x00000000	0xA0039014	196
1.4.469	reg : dcm_diag_pklabels_roi1 _2	0x00000000	0xA0039018	196
1.4.470	reg : dcm_diag_pklabels_roi1 _3	0x00000000	0xA003901C	196
1.4.471	reg : dcm_diag_pklabels_roi1 _4	0x00000000	0xA0039020	196
1.4.472	reg : dcm_diag_pklabels_roi1 _5	0x00000000	0xA0039024	196
1.4.473	reg : dcm_diag_pklabels_roi1 _6	0x00000000	0xA0039028	197
1.4.474	reg : dcm_diag_pklabels_roi1 _7	0x00000000	0xA003902C	197
1.4.475	reg : dcm_diag_pklabels_roi1 _8	0x00000000	0xA0039030	197
1.4.476	reg : dcm_diag_pklabels_roi1 _9	0x00000000	0xA0039034	197
1.4.477	reg : dcm_diag_pklabels_roi1 _10	0x00000000	0xA0039038	197
1.4.478	reg : dcm_diag_pklabels_roi1 _11	0x00000000	0xA003903C	197
1.4.479	reg : dcm_diag_pklabels_roi1 _12	0x00000000	0xA0039040	197
1.4.480	reg : dcm_diag_pklabels_roi1 _13	0x00000000	0xA0039044	198
1.4.481	reg : dcm_diag_pklabels_roi1 _14	0x00000000	0xA0039048	198
1.4.482	reg : dcm_diag_pklabels_roi1 _15	0x00000000	0xA003904C	198
1.4.483	reg : dcm_diag_pklabels_roi1 _16	0x00000000	0xA0039050	198
1.4.484	reg : dcm_diag_pklabels_roi1 _17	0x00000000	0xA0039054	198
1.4.485	reg : dcm_diag_pklabels_roi1 _18	0x00000000	0xA0039058	198
1.4.486	reg : dcm_diag_pklabels_roi1 _19	0x00000000	0xA003905C	198
1.4.487	reg : dcm_diag_pklabels_roi1 _20	0x00000000	0xA0039060	198
1.4.488	reg : dcm_diag_pklabels_roi1 _21	0x00000000	0xA0039064	199
1.4.489	reg : dcm_diag_pklabels_roi1 _22	0x00000000	0xA0039068	199
1.4.490	reg : dcm_diag_pklabels_roi1 _23	0x00000000	0xA003906C	199
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1.4.493	reg : dcm_diag_pkposglobal_r oi1_2	0x00000000	0xA0039078	199

1.4.494	reg : dcm_diag_pkposglobal_r oi1_3	0x00000000	0xA003907C	199
1.4.495	reg : dcm_diag_pkposglobal_r oi1_4	0x00000000	0xA0039080	199
1.4.496	reg : dcm_diag_pkposglobal_r oi1_5	0x00000000	0xA0039084	200
1.4.497	reg : dcm_diag_pkposglobal_r	0x00000000	0xA0039088	200
1.4.498	oi1_6 reg : dcm_diag_pkposglobal_r oi1_7	0x00000000	0xA003908C	200
1.4.499	reg : dcm_diag_pkposglobal_r oi1 8	0x00000000	0xA0039090	200
1.4.500	reg : dcm_diag_pkposglobal_r oi1_9	0x00000000	0xA0039094	200
1.4.501	reg : dcm_diag_pkposglobal_r oi1_10	0x00000000	0xA0039098	200
1.4.502	reg : dcm_diag_pkposglobal_r oi1_11	0x00000000	0xA003909C	200
1.4.503	reg : dcm_diag_pkposglobal_r oi1_12	0x00000000	0xA00390A0	201
1.4.504	reg : dcm_diag_pkposglobal_r oi1_13	0x00000000	0xA00390A4	201
1.4.505	reg : dcm_diag_pkposglobal_r oi1_14	0x00000000	0xA00390A8	201
1.4.506	reg : dcm_diag_pkposglobal_r oi1_15	0x00000000	0xA00390AC	201
1.4.507	reg : dcm_diag_pkposglobal_r oi1_16	0x00000000	0xA00390B0	201
1.4.508	reg : dcm_diag_pkposglobal_r oi1_17	0x00000000	0xA00390B4	201
1.4.509	reg : dcm_diag_pkposglobal_r oi1_18	0x00000000	0xA00390B8	201
1.4.510	reg : dcm_diag_pkposglobal_r oi1_19	0x00000000	0xA00390BC	201
1.4.511	reg : dcm_diag_pkposglobal_r oi1_20	0x00000000	0xA00390C0	202
1.4.512	reg : dcm_diag_pkposglobal_r	0x00000000	0xA00390C4	202
1.4.513	reg : dcm_diag_pkposglobal_r oi1_22	0x00000000	0xA00390C8	202
1.4.514	reg : dcm_diag_pkposglobal_r oi1_23	0x00000000	0xA00390CC	202
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1.4.518	reg : region_10_dtec_tod_lsb	0x00000000	0xA003A004	202
1.4.519	reg : region_10_dtec_tod_msb	0x00000000	0xA003A008	203
1.4.520	reg : region_10_dtec_lts	0x00000000	0xA003A00C	203
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1.4.533	reg : clustering_dcm_diag_ji tter_dcm_presubcl	0x00000000	0xA003A040	205
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1.4.544	reg : clustering_ddm_diag_pk width_median_updated_label3	0x00000000	0xA003A06C	207
1.4.545	reg : clustering_ddm_diag_pk width_std_updated_label3	0x00000000	0xA003A070	207
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1.4.553	reg : region_12_dtec_tod_msb s	0x00000000	0xA003C008	208
1.4.554	reg : region_12_dtec_lts	0x00000000	0xA003C00C	208
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1.4.556	reg:idcb_triggers_idcb_tri gger_ch2	0x00000000	0xA003C014	208
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1.4.558	reg:idcb_triggers_idcb_tri gger_ch9	0x00000000	0xA003C01C	209
1.4.559	reg:idcb_triggers_idcb_tri gger_ch10	0x00000000	0xA003C020	209
1.4.560	reg:idcb_triggers_idcb_tri gger_ch12	0x00000000	0xA003C024	209
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1.4.565	reg : region_13_dtec_lts	0x00000000	0xA003D00C	209
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1.4.570	reg : cal_lf_costfunciterati	0x00000000	0xA003D020	210
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1.7.38	reg: PKT_COUNT_RX_TOTAL	0x00000000	0xA0090100	235
1.7.39	reg: BYTE_COUNT_RX_TOTAL	0x00000000	0xA0090104	235
1.7.40	reg: PKT_COUNT_RX_FCS_ERRO	0x00000000	0xA0090108	235
1.7.41	reg: BYTE_COUNT_RXTX_LPBK_EROR	0x00000000	0xA009010C	235
1.7.42	reg: PKT_COUNT_TX_TOTAL	0x00000000	0xA0090120	236
1.7.43	reg: BYTE_COUNT_TX_TOTAL		0xA0090124	236
1.7.44	reg : PKT_COUNT_TX_BUS_ERRO		0xA0090128	236
1.7.45	reg: PKT_COUNT_TX_DATA_ERR		0xA009012C	236
1.7.46	reg: PKT_COUNT_TX_TOO_SHOR _ERROR	0x00000000	0xA0090130	236
1.7.47			0xA0090134	236
1.7.48	reg: CPU_INSERT_BUFFER_CNT	0x00000000	0xA0090140	236
1.7.49	reg: CPU_CAPTURE_BUFFER_CN		0xA0090144	237
1.7.50	reg: CPU_CAPTURE_BUFFER_CN 1		0xA0090148	237
1.7.51	reg : LINK DOWN COUNT	0x00000000	0xA0090150	237
1.7.52			0xA0090180	237
1.7.53	reg: PACKET_GEN_CHECKER_ST TUS0		0xA0090184	237
1.7.54		0x00000000	0xA0090188	237
1.7.55	reg: PACKET_GEN_CHECKER_ST TUS1		0xA009018C	237
1.7.56	reg: PACKET_GEN_CHECKER_ST TUS2		0xA0090190	237
1.7.57	reg: PACKET_GEN_CHECKER_ST TUS3		0xA0090194	238
1.7.58	reg: PACKET_GEN_CHECKER_ST TUS4		0xA0090198	238
	·		·	

1.7.59	reg:	0x00000000	0xA009019C	238
	PACKET_GEN_CHECKER_ST			
1.7.60	memory: CPU_INSERT_BUFFER		0xA0091000, 0xA0091004 0xA00917FF	238
1.7.60.1	reg : CPU_INSERT_BUFFER	0x00000000		
1.7.61	memory: CPU_CAPTURE_BUFFER		0xA0091800, 0xA0091804 0xA0091FFF	238
1.7.61.1	reg: CPU_CAPTURE_BUFFER	0x00000000		
1.7.62	memory: RX_STATS_ENGINE		0xA0094000, 0xA0094004 0xA00947FF	238
1.7.62.1	reg : RX_STATS_ENGINE	0x00000000	0xA0094000, 0x0000000000	
1.7.63	memory: TX_STATS_ENGINE		0xA0096000, 0xA0096004 0xA00967FF	238
1.7.63.1	reg : TX_STATS_ENGINE	0x00000000	0xA0096000, 0x0000000000	
1.8	block : tselclient_appl_regi sters_srdl		0xA00A0000 - 0xA00A00EB	239
1.8.1	reg : tselclient_module_name	0x74636C69	0xA00A0000	239
1.8.2	reg : tselclient_module_vers	0x00000000	0xA00A0004	239
1.8.3	reg : tselclient_page_proper ties	0x80000101	0xA00A0008	239
1.8.4	reg : tselclient_scratchregi ster	0x12345678	0xA00A000C	239
1.8.5	reg : tselclient_irq_enable	0x00000000	0xA00A0010	239
1.8.6	reg : tselclient_irq_pending	0x00000000		240
1.8.7	reg : tselclient_irq_raw	0x00000000		240
1.8.8	reg : tselclient_irq_force	0x00000000		240
1.8.9	reg : rt_data_handler_stat	0x00000000		240
1.8.10	reg : tx_fsm_dg_kpi_ctrl	0x00000001	0xA00A0064	241
1.8.11	section : pkt1		0xA00A0068 - 0xA00A008F	241
1.8.11.1	reg : tag1	0x00000000		241
1.8.11.2	reg : timestamp_data	0x00000000		241
1.8.11.3	reg : sync_stat_data	0x00000000	0xA00A0070	242
1.8.11.4	reg : shot_id_data	0x00000000	0xA00A0074	242
1.8.11.5	reg : burst_id_data	0x00000000	0xA00A0078	242
1.8.11.6	reg : msec_id_data	0x00000000	0xA00A007C	242
1.8.11.7	reg : lc_diag_data	0x00000007	0xA00A0080	242
1.8.11.8	reg : pp2mp_tfire_totaldelaydata		0xA00A0084	243
1.8.11.9	reg : euv_value_data		0xA00A0088	243
1.8.11.10	reg : tag2	0x00000000		243
1.8.12	reg: ddm_bpam_send7_crc_err _cnt	0x00000000	0xA00A0090	243
1.8.13	reg : ddm_data_lost_cnt	0x00000000		243
1.8.14	reg : ddm_data_bytes_err_cnt	0x00000000		243
1.8.15	reg : rx_fsm_pkt_lgth_field_ err_cnt	0x00000000	0xA00A009C	243
1.8.16	reg : rx_fsm_pload_err_cnt	0x00000000		243
1.8.17	reg: unknown_pkt_rx_cnt	0x00000000	0xA00A00A4	244
1.8.18	reg:pkt1_sync_hdr_err_cnt	0x00000000	0xA00A00A8	244
1.8.19	reg : pkt1_etecflags_hdr_err _cnt	0x00000000	0xA00A00AC	244
1.8.20	reg : pkt1_zeropad_hdr_err_c nt	0x00000000	0xA00A00B0	244
1.8.21	reg : rx_fsm_eot_err_cnt	0x00000000	0xA00A00B4	244
1.8.22	reg : pkt1_seq_err_cnt	0x00000000	0xA00A00B8	244
1.8.23	reg : pkt2_seq_err_cnt	0x00000000	0xA00A00BC	244
1.8.24	reg : rx_fsm_eop_err_cnt	0x00000000	0xA00A00C0	244
1.8.25	reg:rx_fsm_wdog_err_cnt	0x00000000	0xA00A00C4	244
1.8.26	reg : pkt2_axis_fsm_wdog_err _cnt	0x00000000	0xA00A00C8	245
1.8.27	reg : reserved_byte_err_cnt	0x00000000	0xA00A00CC	245
1.8.28	reg : pkt2_zeropad_hdr_err_c nt	0x00000000	0xA00A00D0	245
	- <del></del>		· · · · · · · · · · · · · · · · · · ·	

1.8.29	reg : tx_fsm_wdog_err_cnt	0x00000000	0xA00A00D4	245
1.8.30	reg : pkt1_rx_cnt	0x00000000	0xA00A00D8	245
1.8.31	reg : pkt2_rx_cnt	0x00000000		245
1.8.32	reg : good_pkt1_rx_cnt	0x00000000		245
1.8.33	reg : good_pkt1_rx_cnt	0x00000000		245
1.8.34		0x00000000	0xA00A00E4 0xA00A00E8	246
	reg : good_pkt2_lost_cnt	000000000	0xA00A1000 - 0xA00A110F	246
1.9	block : tselbridge_appl_regi sters_srdl			
1.9.1	reg : tselbridge_module_name			246
1.9.2	reg : tselbridge_module_vers ion	0x00000000	0xA00A1004	246
1.9.3	reg:tselbridge_page_properties	0x80000101	0xA00A1008	246
1.9.4	reg : tselbridge_scratchregi ster	0x12345678	0xA00A100C	246
1.9.5	reg : tselbridge_irq_enable	0x00000000	0xA00A1010	246
1.9.6	reg : tselbridge_irq_pending	0x00000000	0xA00A1014	247
1.9.7	reg : tselbridge_irq_raw		0xA00A1018	247
1.9.8	reg : tselbridge_irq_force			247
1.9.9	reg : rt_data_handler_algo_r	0x00000000	0xA00A1060	247
	x_stat			
1.9.10	reg : rt_data_handler_boot_r x_stat	0x00000000	0xA00A1064	247
1.9.11	reg : rt_data_handler_diag_r x_stat	0x00000000	0xA00A1068	248
1.9.12	reg : rt_data_handler_wfm_re g_rx_stat	0x00000000	0xA00A106C	249
1.9.13	reg : rt_data_handler_vol_wf m_samp_rx_stat	0x00000000	0xA00A1070	249
1.9.14	reg : rt_data_handler_amp_wf m_samp_rx_stat	0x00000000	0xA00A1074	250
1.9.15	reg : rt_data_handler_tx_sta t	0x00000000	0xA00A1078	251
1.9.16	reg : ps_por_b	0x00000000	0xA00A107C	251
1.9.17	reg : ps_srst_b	0x00000000	0xA00A1080	251
1.9.18	reg : enb_wfm_cap		0xA00A1084	251
1.9.19	reg : direct_boot_offset_set	0x00000000		252
1.9.20	reg : cntrl_pkt_rate_ctrl		0xA00A108C	252
1.9.21	reg : algo_data_good_frame_c			252
1.9.22	nt reg : algo_data_bad_frame_cn		0xA00A1094	252
	t			
1.9.23	reg : goodalgo_tsel_pkt_lost _cnt	0x00000000	0xA00A1098	252
1.9.24	reg : boot_data_good_frame_c nt		0xA00A109C	252
1.9.25	reg : boot_data_bad_frame_cn t		0xA00A10A0	252
1.9.26	reg : boot_tsel_pkt_lost_cnt	0x00000000	0xA00A10A4	252
1.9.27	reg : diag_data_good_frame_c nt	0x00000000	0xA00A10A8	253
1.9.28	reg : diag_data_bad_frame_cn t	0x00000000	0xA00A10AC	253
1.9.29	reg : diag_tsel_pkt_lost_cnt	0x00000000	0xA00A10B0	253
1.9.30	reg : wfm_reg_data_good_fram e_cnt		0xA00A10B4	253
1.9.31	reg : wfm_reg_data_bad_frame	0x00000000	0xA00A10B8	253
1.9.32	reg : wfm_reg_tsel_pkt_lost_ cnt	0x00000000	0xA00A10BC	253
1.9.33	reg: vol_wfm_samp_data_good _frame_cnt	0x00000000	0xA00A10C0	253
1.9.34	reg: vol_wfm_samp_data_bad_ frame_cnt	0x00000000	0xA00A10C4	253
1.9.35	reg : vol_wfm_samp_tsel_pkt_ lost_cnt	0x00000000	0xA00A10C8	254

1.9.36	reg:	0x00000000	0xA00A10CC	254
	amp_wfm_samp_data_good			
	_frame_cnt			
1.9.37	reg:	0x00000000	0xA00A10D0	254
	amp_wfm_samp_data_bad_			
	frame_cnt			
1.9.38	reg:	0×00000000	0xA00A10D4	254
1.3.30	amp_wfm_samp_tsel_pkt_	020000000	0220021004	204
4.0.00	lost_cnt	0.0000000	0.40044000	05.4
1.9.39	reg:	000000000	0xA00A10D8	254
	wfm_samp_data_bad_fram			
	e_cnt			
1.9.40	reg : unknown_pkt_cnt	0x00000000	0xA00A10DC	254
1.9.41	reg : boot_data_sop_err_cnt	0x00000000	0xA00A10E0	254
1.9.42	reg : boot_data_eop_err_cnt	0x00000000	0xA00A10E4	254
1.9.43		0x00000000	0xA00A10E8	255
	rder_cnt			
1.9.44	reg : diag_data_sop_err_cnt	0x00000000	0xA00A10EC	255
1.9.45	reg : diag_data_sop_err_cnt	0x00000000	0xA00A10F0	255
		0x00000000	0xA00A10F0	
1.9.46	0 0	UXUUUUUUU	UXAUUA TUF4	255
101=	rder_cnt	0.00000	2.40044050	0.55
1.9.47	reg:	0x00000000	0xA00A10F8	255
	amp_wfm_samp_sop_err_c			
	nt			
1.9.48	reg:	0x00000000	0xA00A10FC	255
	amp_wfm_samp_eop_err_c			
	nt			
1.9.49	reg:	0x00000000	0xA00A1100	255
	amp_wfm_samp_seg_out_o	CACCCCCCC	0,0,100,11,100	
	f_order_cnt			
1.9.50	reg : vol_wfm_samp_sop_err_c	0,00000000	0xA00A1104	255
1.9.50	reg. voi_wiiii_samp_sop_eii_c	000000000	0XA00A1104	255
	4			
1051	nt	0.0000000	0.40044400	0=0
1.9.51	reg : vol_wfm_samp_eop_err_c	0x00000000	0xA00A1108	256
	reg : vol_wfm_samp_eop_err_c			
	reg : vol_wfm_samp_eop_err_c nt reg :	0x00000000 0x00000000		256 256
	reg : vol_wfm_samp_eop_err_c nt reg : vol_wfm_samp_seg_out_o			
1.9.51	reg:vol_wfm_samp_eop_err_c nt reg: vol_wfm_samp_seg_out_o f_order_cnt		0xA00A110C	
	reg : vol_wfm_samp_eop_err_c nt reg : vol_wfm_samp_seg_out_o			
1.9.52	reg: vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block: ipi_scratchpad		0xA00A110C	256
1.9.52 1.10 1.10.1	reg: vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block: ipi_scratchpad memory: ram_256kb_inst	0x00000000	0xA00A110C 0xA00C0000 - 0xA00FFFF 0xA00C0000, 0xA00C0004 0xA00FFFF	256 256
1.9.52 1.10 1.10.1 1.10.1.1	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst	0x00000000	0xA00A110C 0xA00C0000 - 0xA00FFFFF 0xA00C0000, 0xA00C0004 0xA00FFFFF 0xA00C0000, 0x0000000000	256 256 256
1.9.52 1.10 1.10.1	reg: vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block: ipi_scratchpad memory: ram_256kb_inst reg: ram_256kb_inst block:	0x00000000	0xA00A110C 0xA00C0000 - 0xA00FFFF 0xA00C0000, 0xA00C0004 0xA00FFFF	256 256
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers	0x00000000	0xA00A110C 0xA00C0000 - 0xA00FFFFF 0xA00C0000, 0xA00C0004 0xA00FFFFF 0xA00C0000, 0x0000000000 0xA0210000 - 0xA021171F	256 256 256 256
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1	0x00000000 0x00000000 0x00000001	0xA00A110C 0xA00C0000 - 0xA00FFFF 0xA00C0000, 0xA00C0004 0xA00FFFF 0xA00C0000, 0x0000000000 0xA0210000 - 0xA021171F 0xA0210000	256 256 256 256 256
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.1 1.11.2	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1	0x00000000 0x00000000 0x00000001 0x00000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004	256 256 256 256 256 256 258
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.1 1.11.2 1.11.3	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1 reg:esmi_32dat1	0x00000000 0x00000000 0x00000001 0x00000000 0x00000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008	256 256 256 256 256 256 258 258
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.1 1.11.2 1.11.3 1.11.4	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1 reg:esmi_32dat1 reg:esmi_tdly1	0x00000000 0x00000000 0x00000001 0x00000000 0x00000000 0x000000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA021000C	256 256 256 256 256 258 258 259
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1 reg:esmi_32dat1 reg:esmi_tdly1 reg:esmi_fncmd1	0x00000000 0x00000000 0x00000000 0x00000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA021000C  0xA0210014	256 256 256 256 256 258 258 258 259 259
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1 reg:esmi_32dat1 reg:esmi_tdly1	0x00000000 0x00000000 0x00000000 0x00000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA021000C  0xA0210014	256 256 256 256 256 258 258 258 259 259
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6	reg:vol_wfm_samp_eop_err_cont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1 reg:esmi_32dat1 reg:esmi_tdly1 reg:esmi_fncmd1	0x00000000 0x00000000 0x00000000 0x00000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA021000C  0xA0210014	256 256 256 256 256 258 258 258 259 259
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7	reg:vol_wfm_samp_eop_err_cont  reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1 reg:esmi_32dat1 reg:esmi_dly1 reg:esmi_flocmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_jacmd1 reg:esmi_jacmd1	0x00000000  0x00000000  0x00000001  0x00000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018	256 256 256 256 256 258 258 258 259 259 259 260
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_cmd1 reg:esmi_32dat1 reg:esmi_dly1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_jacmd1	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFFF 0xA00C0000, 0xA00C0004 0xA00FFFF 0xA00C0000, 0x0000000000 0xA0210000 - 0xA021171F  0xA0210000 0xA0210004 0xA0210008 0xA021000C 0xA0210014 0xA0210018 0xA021001C 0xA0210030	256 256 256 256 256 258 258 259 259 259 260 260
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_ctl1 reg:esmi_32dat1 reg:esmi_flocmd1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_flocmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_cmd2	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034	256 256 256 256 256 258 258 258 259 259 259 260 260 261
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9 1.11.10	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_ctl1 reg:esmi_32dat1 reg:esmi_fncmd1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_cd2 reg:esmi_32dat2	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034  0xA0210038	256 256 256 256 256 258 258 259 259 260 260 261 262
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9 1.11.10	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_ctl1 reg:esmi_32dat1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_cd2 reg:esmi_32dat2 reg:esmi_tdly2	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038	256 256 256 256 256 258 258 259 259 260 260 261 262 263
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9 1.11.10 1.11.11	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_ctl1 reg:esmi_32dat1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_dly2 reg:esmi_tdly2 reg:esmi_fncmd2	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA021003C  0xA0210044	256 256 256 256 256 258 258 258 259 260 260 261 262 263 263
1.9.52 1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9 1.11.10 1.11.11	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_ctl1 reg:esmi_32dat1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_d2dat2 reg:esmi_flcmd2 reg:esmi_flcmd2 reg:esmi_fncmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210044  0xA0210048	256 256 256 256 256 258 258 259 259 260 260 261 262 263 263
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_dly1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_cd2 reg:esmi_dly2 reg:esmi_flocmd2 reg:esmi_flocmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_extdat2	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA0210018  0xA0210030  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210038  0xA0210040  0xA0210040  0xA0210040	256 256 256 256 256 258 258 259 259 260 260 261 262 263 263 263
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_dly1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_dly2 reg:esmi_flocmd2 reg:esmi_flocmd2 reg:esmi_flocmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_flocmd2 reg:esmi_iacmd2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_ctl3	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA0210018  0xA0210030  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210048  0xA0210048  0xA0210048  0xA021004C  0xA0210060	256 256 256 256 256 258 258 259 259 260 260 261 262 263 263 263 264
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_dly1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_dly2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_cmd3	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210060  0xA0210060	256 256 256 256 256 258 258 258 259 259 260 260 261 262 263 263 263 264 265
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_dly1 reg:esmi_iacmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_dly2 reg:esmi_flocmd2 reg:esmi_flocmd2 reg:esmi_flocmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_flocmd2 reg:esmi_iacmd2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_extdat2 reg:esmi_ctl3	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210060  0xA0210060	256 256 256 256 256 258 258 259 259 260 260 261 262 263 263 263 264
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.15 1.11.16 1.11.17	reg: vol_wfm_samp_eop_err_ont  reg: vol_wfm_samp_seg_out_o f_order_cnt block: ipi_scratchpad memory: ram_256kb_inst  reg: ram_256kb_inst  block: esm_common_registers  reg: esmi_ctl1  reg: esmi_s2dat1  reg: esmi_flcmd1  reg: esmi_flcmd1  reg: esmi_iacmd1  reg: esmi_extdat1  reg: esmi_extdat1  reg: esmi_ctl2  reg: esmi_ctl2  reg: esmi_ctl2  reg: esmi_s2dat2  reg: esmi_flcmd2  reg: esmi_flcmd2  reg: esmi_flcmd2  reg: esmi_flcmd2  reg: esmi_flcmd2  reg: esmi_extdat2  reg: esmi_extdat2  reg: esmi_extdat2  reg: esmi_extdat2  reg: esmi_extdat2  reg: esmi_cmd3  reg: esmi_cmd3  reg: esmi_32dat3	0x00000000  0x00000000  0x00000000  0x000000	0xA00A110C  0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210004  0xA0210008  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210040  0xA0210060  0xA0210060	256 256 256 256 256 258 258 259 259 260 260 261 262 263 263 263 263 264 265 266
1.9.52  1.10 1.10.1 1.10.1 1.11.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.9 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18	reg: vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block: ipi_scratchpad memory: ram_256kb_inst reg: ram_256kb_inst block: esm_common_registers reg: esmi_ctl1 reg: esmi_ctl1 reg: esmi_flocmd1 reg: esmi_flocmd1 reg: esmi_flocmd1 reg: esmi_extdat1 reg: esmi_extdat1 reg: esmi_ctl2 reg: esmi_ctl2 reg: esmi_ctl2 reg: esmi_s2dat2 reg: esmi_s2dat3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_s2dat3 reg: esmi_tdly3	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFFF 0xA00C0000, 0xA00C0004 0xA00FFFFF 0xA00C0000, 0x00000000000 0xA0210000 - 0xA021171F  0xA0210000 0xA0210004 0xA0210008 0xA0210014 0xA0210018 0xA021001C 0xA0210030 0xA0210034 0xA0210038 0xA0210038 0xA0210038 0xA0210040 0xA0210038 0xA0210060 0xA0210048 0xA0210048 0xA0210048 0xA0210066 0xA0210068 0xA0210066	256 256 256 256 256 258 258 259 259 260 260 261 262 263 263 263 263 264 265 266
1.9.52  1.10 1.10.1 1.10.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18 1.11.19	reg: vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block: ipi_scratchpad memory: ram_256kb_inst reg: ram_256kb_inst block: esm_common_registers reg: esmi_ctl1 reg: esmi_s2dat1 reg: esmi_flocmd1 reg: esmi_flocmd1 reg: esmi_extdat1 reg: esmi_extdat1 reg: esmi_ctl2 reg: esmi_ctl2 reg: esmi_ctl2 reg: esmi_s2dat2 reg: esmi_flocmd2 reg: esmi_flocmd2 reg: esmi_flocmd2 reg: esmi_extdat2 reg: esmi_extdat2 reg: esmi_extdat2 reg: esmi_extdat3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_ctl3 reg: esmi_flocmd3 reg: esmi_flocmd3 reg: esmi_flocmd3 reg: esmi_flocmd3 reg: esmi_flocmd3	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFFF  0xA00C0000, 0xA00C0004 0xA00FFFFF  0xA00C0000, 0x00000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210044  0xA0210048  0xA02100404  0xA0210048  0xA0210048  0xA021004C  0xA021004C  0xA0210066  0xA0210066  0xA0210066  0xA021006C  0xA0210074	256 256 256 256 256 258 258 259 259 260 261 262 263 263 263 263 264 265 266 266 267
1.9.52  1.10 1.10.1 1.10.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18 1.11.19 1.11.10	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_fncmd1 reg:esmi_fncmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_d2 reg:esmi_d2 reg:esmi_d2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_ctl3 reg:esmi_ctl3 reg:esmi_ctl3 reg:esmi_ctl3 reg:esmi_cmd3 reg:esmi_cmd3 reg:esmi_fncmd3 reg:esmi_fncmd3 reg:esmi_fncmd3 reg:esmi_fncmd3 reg:esmi_iacmd3 reg:esmi_iacmd3 reg:esmi_iacmd3 reg:esmi_fncmd3 reg:esmi_fncmd3 reg:esmi_iacmd3 reg:esmi_iacmd3	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFFF  0xA00C0000, 0xA00C0004 0xA00FFFFF  0xA00C0000, 0x00000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210044  0xA0210044  0xA0210060  0xA0210048  0xA0210048  0xA0210048  0xA0210048  0xA0210060  0xA0210060  0xA0210060  0xA0210060  0xA0210060  0xA0210074  0xA0210078	256 256 256 256 256 258 258 259 259 260 261 262 263 263 263 263 263 264 265 266 266 267 267
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18 1.11.19 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18 1.11.19 1.11.20 1.11.21	reg: vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block: ipi_scratchpad memory: ram_256kb_inst reg: ram_256kb_inst block: esm_common_registers reg: esmi_ctl1 reg: esmi_dtly1 reg: esmi_fncmd1 reg: esmi_fncmd1 reg: esmi_extdat1 reg: esmi_extdat1 reg: esmi_ctl2 reg: esmi_ctl2 reg: esmi_dtly2 reg: esmi_dtly2 reg: esmi_fncmd2 reg: esmi_fncmd2 reg: esmi_extdat2 reg: esmi_extdat2 reg: esmi_ctl3	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFFF  0xA00C0000, 0xA00C0004 0xA00FFFFF  0xA00C0000, 0x00000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA0210044  0xA0210044  0xA0210060  0xA0210046  0xA0210048  0xA021004C  0xA0210060  0xA0210060  0xA0210060  0xA0210060  0xA0210060  0xA0210074  0xA0210078  0xA0210078	256 256 256 256 256 258 258 259 259 260 261 262 263 263 263 263 263 264 265 266 266 267 267
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18 1.11.19 1.11.18 1.11.19 1.11.10 1.11.11 1.11.20 1.11.20 1.11.21 1.11.22	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_s2dat2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_ctl3 reg:esmi_ctl4	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA021004  0xA0210038  0xA0210060  0xA0210044  0xA0210044  0xA0210048  0xA021004C  0xA0210046  0xA0210060  0xA0210068  0xA021006C  0xA0210074  0xA0210078  0xA021007C  0xA0210090	256 256 256 256 256 258 258 259 259 260 261 262 263 263 263 263 263 264 265 266 266 267 267
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18 1.11.19 1.11.10 1.11.11 1.11.20 1.11.20 1.11.21 1.11.22 1.11.23	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_jacmd2 reg:esmi_jacmd2 reg:esmi_jacmd2 reg:esmi_jacmd2 reg:esmi_jacmd2 reg:esmi_jacmd2 reg:esmi_jacmd2 reg:esmi_jacmd2 reg:esmi_jacmd3 reg:esmi_ctl3 reg:esmi_ctl4 reg:esmi_ctl4 reg:esmi_ctl4 reg:esmi_ctl4 reg:esmi_cmd4	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA0210008  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210006  0xA0210038  0xA0210038  0xA0210038  0xA0210038  0xA0210044  0xA0210060  0xA0210044  0xA0210068  0xA0210066  0xA0210068  0xA0210076  0xA0210078  0xA0210090  0xA0210090	256 256 256 256 256 258 258 259 259 260 261 262 263 263 263 263 263 264 265 266 267 267 267 269
1.9.52  1.10 1.10.1 1.10.1.1 1.11.1 1.11.2 1.11.3 1.11.4 1.11.5 1.11.6 1.11.7 1.11.8 1.11.10 1.11.11 1.11.12 1.11.13 1.11.14 1.11.15 1.11.16 1.11.17 1.11.18 1.11.19 1.11.18 1.11.19 1.11.10 1.11.11 1.11.20 1.11.20 1.11.21 1.11.22	reg:vol_wfm_samp_eop_err_ont reg: vol_wfm_samp_seg_out_o f_order_cnt block:ipi_scratchpad memory:ram_256kb_inst reg:ram_256kb_inst block: esm_common_registers reg:esmi_ctl1 reg:esmi_s2dat1 reg:esmi_fncmd1 reg:esmi_iacmd1 reg:esmi_extdat1 reg:esmi_extdat1 reg:esmi_ctl2 reg:esmi_ctl2 reg:esmi_s2dat2 reg:esmi_fncmd2 reg:esmi_fncmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_iacmd2 reg:esmi_ctl3 reg:esmi_ctl4	0x00000000  0x00000000  0x00000000  0x000000	0xA00C0000 - 0xA00FFFF  0xA00C0000, 0xA00C0004 0xA00FFFF  0xA00C0000, 0x0000000000  0xA0210000 - 0xA021171F  0xA0210000  0xA0210004  0xA021000C  0xA0210014  0xA0210018  0xA021001C  0xA0210030  0xA0210034  0xA0210038  0xA0210038  0xA021004  0xA0210038  0xA0210060  0xA0210044  0xA0210044  0xA0210048  0xA021004C  0xA0210046  0xA0210060  0xA0210068  0xA021006C  0xA0210074  0xA0210078  0xA021007C  0xA0210090	256 256 256 256 256 258 258 259 259 260 261 262 263 263 263 263 263 264 265 266 266 267 267

1 11 00		0.0000000  0.0000000	074
1.11.26	reg : esmi_fncmd4	0x0000000 0xA02100A4	271
1.11.27	reg : esmi_iacmd4	0x0000000 0xA02100A8	271 271
1.11.28	reg : esmi_extdat4	0x00000000 0xA02100AC	271
1.11.29 1.11.30	reg : esmi_ctl5	0x00000001 0xA02100C0 0x00000000 0xA02100C4	271
1.11.30	reg : esmi_cmd5 reg : esmi_32dat5	0x00000000 0xA02100C4 0x00000000 0xA02100C8	273
1.11.32	reg : esmi_tdly5	0x00000000 0xA02100C6 0x00000021 0xA02100CC	274
1.11.32	reg : esmi_fncmd5	0x00000021 0xA02100CC 0x00000000 0xA02100D4	274
1.11.34	reg : esmi_iacmd5	0x00000000 0xA02100D4 0x00000000 0xA02100D8	275
1.11.35	reg : esmi_lactrid5	0x00000000 0xA02100D8	275
1.11.36	reg : esmi_ctl6	0x00000001 0xA02100F0	275
1.11.37	reg : esmi_cmd6	0x00000000 0xA02100F4	276
1.11.38	reg : esmi_32dat6	0x0000000 0xA0210014	277
1.11.39	reg : esmi_tdly6	0x00000001 0xA02100FC	278
1.11.40	reg : esmi_fncmd6	0x00000000 0xA0210104	278
1.11.41	reg : esmi_iacmd6	0x00000000 0xA0210108	278
1.11.42	reg : esmi_extdat6	0x00000000 0xA021010C	279
1.11.43	reg : esmi_ctl7	0x00000001 0xA0210120	279
1.11.44	reg : esmi_cmd7	0x0000000 0xA0210124	280
1.11.45	reg : esmi_32dat7	0x00000000 0xA0210128	281
1.11.46	reg : esmi_tdly7	0x00000021 0xA021012C	282
1.11.47	reg : esmi_fncmd7	0x0000000 0xA0210134	282
1.11.48	reg : esmi_iacmd7	0x00000000 0xA0210138	282
1.11.49	reg : esmi_extdat7	0x00000000 0xA021013C	282
1.11.50	reg : esmi_ctl8	0x00000001 0xA0210150	283
1.11.51	reg : esmi_cmd8	0x00000000 0xA0210154	284
1.11.52	reg : esmi_32dat8	0x00000000 0xA0210158	284
1.11.53	reg : esmi_tdly8	0x00000021 0xA021015C	285
1.11.54	reg : esmi_fncmd8	0x00000000 0xA0210164	286
1.11.55	reg : esmi_iacmd8	0x00000000 0xA0210168	286
1.11.56	reg : esmi_extdat8	0x00000000 0xA021016C	286
1.11.57	reg : esmi_ctl9	0x00000001 0xA0210180	286
1.11.58	reg : esmi_cmd9	0x00000000 0xA0210184	288
1.11.59	reg : esmi_32dat9	0x00000000 0xA0210188	288
1.11.60	reg : esmi_tdly9	0x00000021 0xA021018C	289
1.11.61	reg : esmi_fncmd9	0x00000000 0xA0210194	289
1.11.62	reg : esmi_iacmd9	0x00000000 0xA0210198	290
1.11.63	reg : esmi_extdat9	0x00000000 0xA021019C	290
1.11.64	reg : esmi_ctl10	0x00000001 0xA02101B0	290
1.11.65	reg : esmi_cmd10	0x00000000 0xA02101B4	292
1.11.66	reg : esmi_32dat10	0x00000000 0xA02101B8	292
1.11.67	reg : esmi_tdly10	0x00000021 0xA02101BC	293
1.11.68	reg : esmi_fncmd10	0x00000000 0xA02101C4	293
1.11.69	reg : esmi_iacmd10	0x00000000 0xA02101C8	293
1.11.70	reg : esmi_extdat10	0x00000000 0xA02101CC	294
1.11.71	reg : esmi_ctl11	0x00000001 0xA02101E0	294
1.11.72	reg : esmi_cmd11	0x00000000 0xA02101E4	295
1.11.73	reg : esmi_32dat11	0x00000000 0xA02101E8 0x00000021 0xA02101EC	296
1.11.74	reg : esmi_tdly11		297
1.11.75	reg : esmi_fncmd11	0x00000000 0xA02101F4 0x00000000 0xA02101F8	297 297
1.11.76 1.11.77	reg : esmi_iacmd11 reg : esmi_extdat11	0x00000000 0xA02101F8 0x00000000 0xA02101FC	297
1.11.77	reg : esmi_extdat11	0x00000000 0xA02101FC 0x00000001 0xA0210210	297
1.11.78	reg : esmi_cmd12	0x00000000 0xA0210210	299
1.11.79	reg : esmi_32dat12	0x00000000 0xA0210214 0x00000000 0xA0210218	299
1.11.81	reg : esmi_tdly12	0x00000000 0xA0210218 0x00000021 0xA021021C	300
1.11.82	reg : esmi_fncmd12	0x00000001 0xA021021C	301
1.11.83	reg : esmi_iacmd12	0x00000000 0xA0210224	301
1.11.84	reg : esmi_extdat12	0x00000000 0xA0210220	301
1.11.85	reg : esmi_ctl13	0x00000001 0xA0210220	301
1.11.86	reg : esmi_cmd13	0x00000001 0xA0210240	303
1.11.87	reg : esmi_32dat13	0x00000000 0xA0210244	303
1.11.88	reg : esmi_tdly13	0x00000001 0xA021024C	304
1.11.89	reg : esmi_fncmd13	0x00000000 0xA0210254	304
1.11.90	reg : esmi_iacmd13	0x00000000 0xA0210258	305
1.11.91	reg : esmi_extdat13	0x00000000 0xA021025C	305

4.44.00		000000004	04.004.0070	005
1.11.92	reg : esmi_ctl14	0x00000001	0xA0210270	305
1.11.93	reg : esmi_cmd14	0x00000000	0xA0210274	307
1.11.94	reg : esmi_32dat14	0x00000000	0xA0210278	307
1.11.95	reg : esmi_tdly14	0x00000021	0xA021027C	308
1.11.96	reg : esmi_fncmd14	0x00000000		308
1.11.97	reg : esmi_iacmd14	0x00000000		308
1.11.98	reg : esmi_extdat14	0x00000000		309
1.11.99	reg : esmi_ctl15	0x00000001		309
1.11.100	reg : esmi_cmd15	0x00000000		310
1.11.101	reg : esmi_32dat15	0x00000000		311
1.11.102	reg : esmi_tdly15	0x00000021		312
1.11.103	reg : esmi_fncmd15	0x00000000		312
1.11.104	reg : esmi_iacmd15	0x00000000		312
1.11.105	reg : esmi_extdat15		0xA02102BC	312
1.11.106	reg : esmi_ctl16	0x00000001		313
1.11.107	reg : esmi_cmd16	0x00000000		314
1.11.108	reg : esmi_32dat16	0x00000000		315
1.11.109	reg : esmi_tdly16	0x00000021	0xA02102DC	315
1.11.110	reg : esmi_fncmd16	0x00000000		316
1.11.111	reg : esmi_iacmd16	0x00000000		316
1.11.112	reg : esmi_extdat16	0x00000000		316
1.11.113	reg : esmi_ctl17	0x00000001	0xA0210300	316
1.11.114	reg : esmi_cmd17	0x00000000		318
1.11.115	reg : esmi_32dat17	0x00000000		318
1.11.116	reg : esmi_tdly17	0x00000021		319
1.11.117	reg : esmi_fncmd17	0x00000000		320
1.11.118	reg : esmi_iacmd17	0x00000000		320
1.11.119	reg : esmi_extdat17	0x00000000	0xA021031C	320
1.11.120	reg : esmi_ctl18	0x00000001	0xA0210330	320
1.11.121	reg : esmi_cmd18	0x00000000		322
1.11.122	reg : esmi_32dat18	0x00000000		322
1.11.123	reg : esmi_tdly18	0x00000021	0xA021033C	323
1.11.124	reg : esmi_fncmd18	0x00000000		323
1.11.125	reg : esmi_iacmd18	0x00000000	0xA0210348	324
1.11.126	reg : esmi_extdat18	0x00000000	0xA021034C	324
1.11.127	reg : esmi_ctl19	0x00000001	0xA0210360	324
1.11.128	reg : esmi_cmd19	0x00000000	0xA0210364	325
1.11.129	reg : esmi_32dat19	0x00000000	0xA0210368	326
1.11.130	reg : esmi_tdly19	0x00000021	0xA021036C	327
1.11.131	reg : esmi_fncmd19	0x00000000	0xA0210374	327
1.11.132	reg : esmi_iacmd19	0x00000000	0xA0210378	327
1.11.133	reg : esmi_extdat19	0x00000000	0xA021037C	328
1.11.134	reg : esmi_ctl20	0x00000001	0xA0210390	328
1.11.135	reg : esmi_cmd20	0x00000000	0xA0210394	329
1.11.136	reg : esmi_32dat20	0x00000000		330
1.11.137	reg : esmi_tdly20	0x00000021	0xA021039C	331
1.11.138	reg : esmi_fncmd20	0x00000000		331
1.11.139	reg : esmi_iacmd20		0xA02103A8	331
1.11.140	reg : esmi_extdat20	0x00000000		331
1.11.141	reg : esmi_crc	0x00000000		332
1.11.142	reg : esmi_crc_sel	0x00000000		332
1.11.143	reg : esmi_crc_cnt		0xA0210708	332
1.11.144	reg : esmi_cab	0x00000000		332
1.11.145	reg : spm_cab	0x00000000		332
1.11.146	reg : t9_esmi	0x00000000		332
1.11.147	reg : nrgy_a1	0x00000000		332
1.11.148	reg : pkamp_a1_pktime_a1	0x00000000		333
1.11.149	reg : nrgy_b1	0x00000000		334
1.11.150	reg : pkamp_b1_pktime_b1	0x00000000		335
1.11.151	reg : nrgy_c1	0x00000000		335
1.11.152	reg : pkamp_c1_pktime_c1	0x00000000		336
1.11.153	reg : nrgy_a2	0x00000000		337
1.11.154	reg : pkamp_a2_pktime_a2	0x00000000		338
1.11.155	reg : nrgy_b2	0x00000000		339
1.11.156	reg : pkamp_b2_pktime_b2		0xA0210824	339
1.11.157	reg : nrgy_c2	0x00000000		340
	109 . 1119y_02	3703000000	0/4 t0Z 100Z0	J-10

1 11 150			0. 1001000	0.44
1.11.158			0xA021082C	341
1.11.159	reg : nrgy_a3	0x00000000		342
1.11.160	reg:pkamp_a3_pktime_a3	0x00000000		342
1.11.161	reg : nrgy_b3		0xA0210838	343
1.11.162	reg : pkamp_b3_pktime_b3		0xA021083C	344
1.11.163	reg : nrgy_c3		0xA0210840	345
1.11.164	reg : pkamp_c3_pktime_c3	0x00000000	0xA0210844	345
1.11.165	reg : nrgy_a4	0x00000000	0xA0210848	346
1.11.166	reg : pkamp_a4_pktime_a4	0x00000000	0xA021084C	347
1.11.167	reg:nrgy_b4	0x00000000	0xA0210850	348
1.11.168	reg : pkamp_b4_pktime_b4	0x00000000	0xA0210854	348
1.11.169	reg: nrgy_c4	0x00000000	0xA0210858	349
1.11.170	reg : pkamp_c4_pktime_c4	0x00000000	0xA021085C	350
1.11.171	reg : nrgy_a5	0x00000000	0xA0210860	351
1.11.172	reg : pkamp_a5_pktime_a5	0x00000000	0xA0210864	351
1.11.173	reg : nrgy_b5		0xA0210868	352
1.11.174	reg : pkamp_b5_pktime_b5		0xA021086C	353
1.11.175	reg : nrgy_c5		0xA0210870	354
1.11.176	reg : pkamp_c5_pktime_c5	0x00000000		355
1.11.177	reg : nrgy_a6		0xA0210878	355
1.11.178	reg : pkamp_a6_pktime_a6		0xA021087C	356
1.11.179	reg : nrgy_b6		0xA0210880	357
1.11.180	reg : pkamp_b6_pktime_b6		0xA0210884	358
1.11.181	reg: nrgy_c6		0xA0210888	358
1.11.182	reg : pkamp_c6_pktime_c6		0xA021088C	359
1.11.183	reg : nrgy_a7		0xA0210890	360
1.11.184	reg : pkamp_a7_pktime_a7		0xA0210894	361
1.11.185	reg : nrgy_b7		0xA0210898	361
1.11.186	reg : pkamp_b7_pktime_b7	0x00000000		362
1.11.187	reg : nrgy_c7	0x00000000		363
1.11.188	reg : pkamp_c7_pktime_c7		0xA02108A4	364
1.11.189	reg : nrgy_a8	0x00000000		365
1.11.190	reg : pkamp_a8_pktime_a8	0x00000000		365
1.11.191	reg : nrgy_b8		0xA02108B0	366
1.11.192	reg : pkamp_b8_pktime_b8		0xA02108B4	367
1.11.193	reg: nrgy_c8	0x00000000		368
1.11.194	reg : pkamp_c8_pktime_c8	0x00000000		368
1.11.195	reg : nrgy_a9	0x00000000	0xA02108C0	369
1.11.196	reg : pkamp_a9_pktime_a9	0x00000000	0xA02108C4	370
1.11.197	reg : nrgy_b9	0x00000000	0xA02108C8	371
1.11.198	reg : pkamp_b9_pktime_b9	0x00000000	0xA02108CC	371
1.11.199	reg : nrgy_c9	0x00000000	0xA02108D0	372
1.11.200	reg : pkamp_c9_pktime_c9	0x00000000	0xA02108D4	373
1.11.201	reg:nrgy_a10	0x00000000	0xA02108D8	374
1.11.202		0x00000000		374
1.11.203	reg : nrgy_b10	0x00000000	0xA02108E0	375
1.11.204	reg : pkamp_b10_pktime_b10	0x00000000	0xA02108E4	376
1.11.205	reg : nrgy_c10	0x00000000	0xA02108E8	377
1.11.206		0x00000000	0xA02108EC	377
1.11.207	reg : nrgy_a11	0x00000000	0xA02108F0	378
1.11.208		0x00000000		379
1.11.209	reg : nrgy_b11		0xA02108F8	380
1.11.210	3.	0x00000000		381
1.11.211	reg : nrgy_c11	0x00000000		381
1.11.212			0xA0210904	382
1.11.213	reg : nrgy_a12		0xA0210908	383
1.11.214		0x00000000		384
1.11.215	reg : nrgy_b12	0x00000000	0xA0210910	384
1.11.216		0x00000000	0xA0210914	385
1.11.217	reg : nrgy_c12	0x00000000		386
1.11.218		0x00000000	0xA021091C	387
1.11.219	reg : nrgy_a13	0x00000000		387
1.11.220		0x00000000	0xA0210924	388
1.11.221	reg : nrgy_b13	0x00000000	0xA0210928	389
1.11.222			0xA021092C	390
1.11.223	reg : nrgy_c13	0x00000000	0xA0210930	391

1 11 001	10 11: 10	0.0000000	0. 10010001	004
1.11.224	reg : pkamp_c13_pktime_c13			391
1.11.225	reg : nrgy_a14		0xA0210938	392
1.11.226	reg:pkamp_a14_pktime_a14			393
1.11.227	reg : nrgy_b14		0xA0210940	394
1.11.228	reg:pkamp_b14_pktime_b14			394
1.11.229	reg : nrgy_c14		0xA0210948	395
1.11.230	reg:pkamp_c14_pktime_c14		0xA021094C	396
1.11.231	reg : nrgy_a15		0xA0210950	397
1.11.232	reg : pkamp_a15_pktime_a15			397
1.11.233	reg : nrgy_b15		0xA0210958	398
1.11.234	reg : pkamp_b15_pktime_b15			399
1.11.235	reg : nrgy_c15		0xA0210960	400
1.11.236	reg:pkamp_c15_pktime_c15			400
1.11.237	reg : nrgy_a16	0x00000000	0xA0210968	401
1.11.238	reg:pkamp_a16_pktime_a16			402
1.11.239	reg : nrgy_b16		0xA0210970	403
1.11.240	reg:pkamp_b16_pktime_b16		0xA0210974	403
1.11.241	reg : nrgy_c16		0xA0210978	404
1.11.242	reg : pkamp_c16_pktime_c16		0xA021097C	405
1.11.243	reg : nrgy_a17		0xA0210980	406
1.11.244	reg:pkamp_a17_pktime_a17			407
1.11.245	reg : nrgy_b17		0xA0210988	407
1.11.246	reg : pkamp_b17_pktime_b17			408
1.11.247	reg : nrgy_c17		0xA0210990	409
1.11.248	reg : pkamp_c17_pktime_c17		0xA0210994	410
1.11.249	reg : nrgy_a18		0xA0210998	410
1.11.250	reg : pkamp_a18_pktime_a18			411
1.11.251	reg : nrgy_b18		0xA02109A0	412
1.11.252	reg : pkamp_b18_pktime_b18			413
1.11.253	reg : nrgy_c18	0x00000000	0xA02109A8	413
1.11.254	reg : pkamp_c18_pktime_c18			414
1.11.255	reg : nrgy_a19		0xA02109B0	415
1.11.256	reg: pkamp_a19_pktime_a19		0xA02109B4	416
1.11.257	reg : nrgy_b19		0xA02109B8	417
1.11.258	reg: pkamp_b19_pktime_b19	0x00000000	0xA02109BC	417
1.11.259	reg : nrgy_c19	0x00000000	0xA02109C0	418
1.11.260	reg : pkamp_c19_pktime_c19	0x00000000	0xA02109C4	419
1.11.261	reg : nrgy_a20		0xA02109C8	420
1.11.262	reg: pkamp_a20_pktime_a20	0x00000000	0xA02109CC	420
1.11.263	reg : nrgy_b20		0xA02109D0	421
1.11.264	reg : pkamp_b20_pktime_b20	0x00000000	0xA02109D4	422
1.11.265	reg : nrgy_c20	0x00000000	0xA02109D8	423
1.11.266	reg : pkamp_c20_pktime_c20	0x00000000	0xA02109DC	423
1.11.267	reg : ffa_lk	0x00000000	0xA0210FCC	424
1.11.268	reg : ffa_s1_x	0x00000000		425
1.11.269	reg : ffa_s1_y	0x00000000		425
1.11.270	reg : ffa_s1_sum	0x00000000		425
1.11.271	reg : ffa_s2_x		0xA0210FDC	425
1.11.272	reg : ffa_s2_y	0x00000000		425
1.11.273	reg : ffa_s2_sum	0x00000000	0xA0210FE4	425
1.11.274	reg : quadcell_read_sel	0x00000000		426
1.11.275	reg : debug_wave	0x00000000	0xA0210FEC	426
1.11.276	reg : wave_pkt_cnt	0x00000000	0xA0210FF0	426
1.11.277	reg : map4_hop	0x00000000	0xA0210FF4	426
1.11.278	reg : map4_latch_time	0x00000000	0xA0210FF8	426
1.11.279	reg : map4_keep_time		0xA0210FFC	426
1.11.280	reg : esmi_s0_cnt1	0x00000000		427
1.11.281	reg : esmi_s0_crc1	0x00000000		427
1.11.282	reg : esmi_s1_cnt1	0x00000000		427
1.11.283	reg : esmi_s1_crc1	0x00000000		427
1.11.284	reg : esmi_s2_cnt1	0x00000000		427
1.11.285	reg : esmi_s2_crc1	0x00000000		427
1.11.286	reg : esmi_s7_cnt1	0x00000000		427
1.11.287	reg : esmi_s7_crc1	0x00000000		428
1.11.288	reg : esmi_rd_cnt1		0xA0211020	428
1.11.289	reg : esmi_rd_crc1	0x00000000		428

11.29	1 11 000		0.00000000  0.00044000	1400
1.11.292   reg. esmit tond cnt1	1.11.290	reg : esmi_da_cnt1	0x0000000 0xA0211028	428
1.11.293				
1.11.294				
1.11.295   reg   cerm   s0   cert				
1.11.266				
1.11.297   reg.; cemi_st_cnc2   0x00000000   0x0211046   429   1.11.299   cemi_st_cnc2   0x00000000   0x0211050   429   1.11.299   cemi_st_cnc2   0x00000000   0x0211050   429   1.11.300   reg.; cemi_st_cnc2   0x00000000   0x0211054   429   1.11.301   reg.; cemi_st_cnc2   0x00000000   0x0211056   429   1.11.302   reg.; cemi_st_cnc2   0x00000000   0x0211056   429   1.11.302   reg.; cemi_st_cnc2   0x00000000   0x0211056   429   1.11.301   reg.; cemi_st_cnc2   0x00000000   0x0211056   430   1.11.304   reg.; cemi_st_cnc2   0x00000000   0x0211066   430   1.11.304   reg.; cemi_st_cnc2   0x00000000   0x0211066   430   1.11.306   reg.; cemi_st_cnc2   0x00000000   0x0211068   430   1.11.306   reg.; cemi_st_cnc2   0x00000000   0x0211066   430   1.11.306   reg.; cemi_st_cnc2   0x00000000   0x0211066   430   1.11.306   reg.; cemi_st_cnc2   0x00000000   0x0211070   430   1.11.308   reg.; cemi_st_cnc2   0x00000000   0x0211074   430   1.11.309   reg.; cemi_st_cnc2   0x00000000   0x0211074   430   1.11.310   reg.; cemi_st_cnc2   0x00000000   0x0211080   431   1.11.311   reg.; cemi_st_cnc3   0x00000000   0x0211080   431   1.11.312   reg.; cemi_st_cnc3   0x00000000   0x0211080   431   1.11.314   reg.; cemi_st_cnc3   0x00000000   0x0211080   431   1.11.314   reg.; cemi_st_cnc3   0x00000000   0x0211080   431   1.11.317   reg.; cemi_st_cnc3   0x00000000   0x0211090   431   1.11.317   reg.; cemi_st_cnc3   0x00000000   0x0211090   431   1.11.318   reg.; cemi_st_cnc3   0x00000000   0x0211090   431   1.11.319   reg.; cemi_st_cnc3   0x00000000   0x0211090   432   1.11.321   reg.; cemi_st_cnc4   0x00000000   0x0211090   432   1.11.331   reg.; cemi_st_cnc4   0x00000000   0x0211000   432   1.11.331   reg.; cemi_st_cnc4   0x00000000   0x0211000   433   1.11.331   reg.; cemi_st_cnc4   0x000000				
111.128				
1.11.399				
1.11.300				
1.11.3.01   reg.:csmi s7 crd2				
111.302   reg :esmi_s7_crc2				
111.303				
111.304   reg : esmi_rd_crc2				
111.305   reg   semi_la_cnt2   0x0000000   0xA021106C   430				
1.11.306   reg   semi_lacint2				
1.11.308	1.11.306		0x00000000 0xA021106C	430
111.309   reg : esmi_s0_cnd2	1.11.307	reg : esmi_tcmd_cnt2	0x00000000 0xA0211070	430
1.11.310	1.11.308	reg : esmi_twcmd_cnt2	0x00000000 0xA0211074	430
1.11.311			0x00000000 0xA0211078	
1.11.3.12         leg: esmi_st_crd3         0x00000000         0xA021108C         431           1.11.3.13         leg: esmi_st_crd3         0x00000000         0xA021109C         431           1.11.3.15         leg: esmi_st_crd3         0x000000000         0xA0211094         431           1.11.3.16         leg: esmi_st_crd3         0x000000000         0xA0211094         431           1.11.3.17         leg: esmi_st_crd3         0x000000000         0xA021109C         432           1.11.3.17         leg: esmi_rd_crd3         0x000000000         0xA02110AO         432           1.11.3.19         leg: esmi_rd_crd3         0x00000000         0xA02110AA         432           1.11.3.20         leg: esmi_rd_crd3         0x00000000         0xA02110AA         432           1.11.3.21         leg: esmi_rd_crd3         0x00000000         0xA02110AA         432           1.11.3.22         leg: esmi_rd_crd3         0x00000000         0xA02110BA         432           1.11.3.22         leg: esmi_rd_crd13         0x00000000         0xA02110BA         432           1.11.3.25         leg: esmi_rd_crd4         0x00000000         0xA02110BA         432           1.11.3.26         leg: esmi_rd_orrd4         0x000000000         0xA02110CA         43				
1.11.3131         leg: esmi_s1_crc3         0x00000000         0xA021109C         431           1.11.314         leg: esmi_s2_crc3         0x00000000         0xA0211090         431           1.11.315         reg: esmi_s2_crc3         0x00000000         0xA0211098         431           1.11.316         reg: esmi_s7_crc3         0x00000000         0xA0211098         432           1.11.318         reg: esmi_d_crc13         0x00000000         0xA02110A0         432           1.11.319         reg: esmi_d_crc3         0x00000000         0xA02110A0         432           1.11.321         reg: esmi_d_crc13         0x00000000         0xA02110A4         432           1.11.322         reg: esmi_d_crc13         0x00000000         0xA02110AC         432           1.11.322         reg: esmi_t_d_crc13         0x00000000         0xA02110B0         432           1.11.322         reg: esmi_t_d_m_crt3         0x00000000         0xA02110B4         432           1.11.324         reg: esmi_s0_crt4         0x00000000         0xA02110B8         432           1.11.325         reg: esmi_s1_crt4         0x00000000         0xA02110CC         433           1.11.327         reg: esmi_s1_crt4         0x00000000         0xA02110CC         433 <td></td> <td></td> <td></td> <td></td>				
1.11.3.14         reg : esml_s2_crt3         0x00000000         0xA0211090         431           1.11.3.15         reg : esml_s7_crt3         0x00000000         0xA0211094         431           1.11.3.16         reg : esml_s7_crt3         0x00000000         0xA021109C         432           1.11.3.17         reg : esml_rd_crt3         0x00000000         0xA02110AO         432           1.11.3.19         reg : esml_rd_crt3         0x00000000         0xA02110AA         432           1.11.3.20         reg : esml_rd_crt3         0x00000000         0xA02110AB         432           1.11.3.21         reg : esml_ia_crt3         0x00000000         0xA02110AB         432           1.11.3.22         reg : esml_tcmd_crt3         0x00000000         0xA02110BO         432           1.11.3.22         reg : esml_tcmd_crt3         0x00000000         0xA02110BA         432           1.11.3.25         reg : esml_s0_crt4         0x00000000         0xA02110BA         432           1.11.3.26         reg : esml_s0_crt4         0x00000000         0xA02110CA         433           1.11.3.27         reg : esml_s1_crt4         0x00000000         0xA02110CA         433           1.11.3.28         reg : esml_s2_crt4         0x00000000         0xA02110CA				
1.11.315         reg : esml. s2_crc3         0x00000000         0xA0211098         431           1.11.316         reg : esml. s7_crc3         0x0000000         0xA0211098         432           1.11.317         reg : esml. rd_crc3         0x00000000         0xA02110A0         432           1.11.319         reg : esml. rd_crc3         0x00000000         0xA02110A4         432           1.11.321         reg : esml. da_crc13         0x00000000         0xA02110A4         432           1.11.322         reg : esml. da_crc13         0x00000000         0xA02110AC         432           1.11.322         reg : esml. twcmd_crc13         0x00000000         0xA02110B0         432           1.11.323         reg : esml. twcmd_crc13         0x00000000         0xA02110B0         432           1.11.324         reg : esml.s0_crc4         0x00000000         0xA02110B8         432           1.11.325         reg : esml.s0_crc4         0x00000000         0xA02110C4         433           1.11.327         reg : esml.s1_crc4         0x00000000         0xA02110C4         433           1.11.329         reg : esml.s2_crc4         0x00000000         0xA02110C6         433           1.11.330         reg : esml.s2_crc4         0x00000000         0xA02110C6				
1.11.316   reg : esmi_s7_crt3   0x00000000				
1.11.317         reg : esmi_s7_crc3         0x00000000         0xA021109C         432           1.11.318         reg : esmi_rd_crc3         0x00000000         0xA02110A0         432           1.11.319         reg : esmi_da_cnt3         0x00000000         0xA02110A8         432           1.11.321         reg : esmi_da_cnt3         0x00000000         0xA02110AC         432           1.11.322         reg : esmi_twcmd_cnt3         0x00000000         0xA02110B0         432           1.11.323         reg : esmi_twcmd_cnt3         0x00000000         0xA02110B4         432           1.11.324         reg : esmi_sb_cnt4         0x00000000         0xA02110B4         432           1.11.325         reg : esmi_sb_cnt4         0x00000000         0xA02110C0         433           1.11.326         reg : esmi_sb_cnt4         0x00000000         0xA02110C0         433           1.11.327         reg : esmi_sb_cnt4         0x00000000         0xA02110CC         433           1.11.329         reg : esmi_sb_cnt4         0x00000000         0xA02110CC         433           1.11.330         reg : esmi_sb_cnt4         0x00000000         0xA02110D0         433           1.11.331         reg : esmi_sb_cnt4         0x00000000         0xA02110D0         433				
1.11.318				
1.11.319				
1.11.320				
1.11.321   reg : esmi_ta_cnt3				
1.11.322         reg : esmi_twcmd_cnt3         0x00000000         0xA02110B4         432           1.11.323         reg : esmi_tdm_cnt3         0x00000000         0xA02110B8         432           1.11.324         reg : esmi_dm_cnt3         0x00000000         0xA02110C0         433           1.11.325         reg : esmi_s0_cnt4         0x00000000         0xA02110C0         433           1.11.327         reg : esmi_s1_cnt4         0x00000000         0xA02110C8         433           1.11.327         reg : esmi_s1_crc4         0x00000000         0xA02110CC         433           1.11.329         reg : esmi_s2_cnt4         0x00000000         0xA02110D0         433           1.11.331         reg : esmi_s2_crc4         0x00000000         0xA02110D0         433           1.11.332         reg : esmi_s2_crc4         0x00000000         0xA02110D8         433           1.11.332         reg : esmi_s7_crc4         0x00000000         0xA02110D8         433           1.11.333         reg : esmi_s7_crc4         0x00000000         0xA02110DC         433           1.11.333         reg : esmi_s6_cnt4         0x00000000         0xA02110DC         434           1.11.335         reg : esmi_d6_cnt4         0x00000000         0xA02110E4         434 </td <td></td> <td></td> <td></td> <td></td>				
1.11.323				
1.11.324         reg:esmi_s0_cnt4         0x00000000         0xA02110E8         432           1.11.325         reg:esmi_s0_crc4         0x00000000         0xA02110C0         433           1.11.326         reg:esmi_s1_cnt4         0x00000000         0xA02110C8         433           1.11.327         reg:esmi_s1_crc4         0x00000000         0xA02110CC         433           1.11.328         reg:esmi_s2_cnt4         0x00000000         0xA02110D0         433           1.11.329         reg:esmi_s2_crc4         0x00000000         0xA02110D0         433           1.11.330         reg:esmi_s7_cnt4         0x00000000         0xA02110DA         433           1.11.331         reg:esmi_s7_crc4         0x00000000         0xA02110DB         433           1.11.332         reg:esmi_rd_cnt4         0x00000000         0xA02110DC         433           1.11.333         reg:esmi_rd_cnt4         0x00000000         0xA02110E0         434           1.11.335         reg:esmi_rd_cnt4         0x00000000         0xA02110E4         434           1.11.336         reg:esmi_id_cnt4         0x00000000         0xA02110E0         434           1.11.337         reg:esmi_twcmd_cnt4         0x00000000         0xA02110E0         434				
1.11.325   reg : esmi_s0_crd4				
1.11.326         reg:esmi_s0_crc4         0x00000000         0xA02110C4         433           1.11.327         reg:esmi_s1_cnt4         0x00000000         0xA02110CC         433           1.11.328         reg:esmi_s1_crc4         0x00000000         0xA02110D0         433           1.11.329         reg:esmi_s2_crc4         0x00000000         0xA02110D4         433           1.11.330         reg:esmi_s7_cnt4         0x00000000         0xA02110DB         433           1.11.331         reg:esmi_s7_crc4         0x00000000         0xA02110DC         433           1.11.332         reg:esmi_rd_cnt4         0x00000000         0xA02110DC         433           1.11.333         reg:esmi_rd_cnt4         0x00000000         0xA02110E0         434           1.11.334         reg:esmi_rd_crc4         0x00000000         0xA02110E4         434           1.11.335         reg:esmi_acnt4         0x00000000         0xA02110E8         434           1.11.336         reg:esmi_acnt4         0x00000000         0xA02110E0         434           1.11.337         reg:esmi_dcnt4         0x00000000         0xA02110F0         434           1.11.339         reg:esmi_dcnt4         0x00000000         0xA02110F4         434           1.1				
1.11.327         reg:esmi_s1_cnt4         0x00000000         0xA02110C8         433           1.11.328         reg:esmi_s1_crc4         0x00000000         0xA02110D0         433           1.11.329         reg:esmi_s2_cnt4         0x00000000         0xA02110D0         433           1.11.330         reg:esmi_s2_crc4         0x00000000         0xA02110D8         433           1.11.331         reg:esmi_s7_cnt4         0x00000000         0xA02110DC         433           1.11.332         reg:esmi_s7_crc4         0x00000000         0xA02110DC         433           1.11.333         reg:esmi_rd_cnt4         0x00000000         0xA02110E0         434           1.11.335         reg:esmi_da_cnt4         0x00000000         0xA02110E0         434           1.11.336         reg:esmi_da_cnt4         0x00000000         0xA02110EC         434           1.11.337         reg:esmi_tomd_cnt4         0x00000000         0xA02110FC         434           1.11.339         reg:esmi_dm_cnt4         0x00000000         0xA02110F0         434           1.11.340         reg:esmi_s0_cnt5         0x00000000         0xA02110F8         434           1.11.341         reg:esmi_s1_crc5         0x00000000         0xA021110A         435				
1.11.328   reg : esmi_s1_crc4				
1.11.329         reg:esmi_s2_cnt4         0x00000000         0xA02110D0         433           1.11.330         reg:esmi_s2_crc4         0x00000000         0xA02110D4         433           1.11.331         reg:esmi_s7_cnt4         0x00000000         0xA02110DC         433           1.11.332         reg:esmi_s7_crc4         0x00000000         0xA02110DC         433           1.11.333         reg:esmi_rd_cnt4         0x00000000         0xA02110E0         434           1.11.334         reg:esmi_rd_crc4         0x00000000         0xA02110E4         434           1.11.335         reg:esmi_da_cnt4         0x00000000         0xA02110E8         434           1.11.336         reg:esmi_la_cnt4         0x00000000         0xA02110EC         434           1.11.337         reg:esmi_tomd_cnt4         0x00000000         0xA02110F0         434           1.11.339         reg:esmi_tomd_cnt4         0x00000000         0xA02110F4         434           1.11.340         reg:esmi_s0_cnt5         0x00000000         0xA021110A         435           1.11.341         reg:esmi_s1_cnt5         0x00000000         0xA021110A         435           1.11.342         reg:esmi_s1_cnt5         0x00000000         0xA0211110C         435	1.11.328		0x00000000 0xA02110CC	433
1.11.331       reg:esmi_s7_crc4       0x00000000       0xA02110DB       433         1.11.332       reg:esmi_s7_crc4       0x00000000       0xA02110DC       433         1.11.333       reg:esmi_rd_crc4       0x000000000       0xA02110E0       434         1.11.334       reg:esmi_rd_crc4       0x00000000       0xA02110E4       434         1.11.335       reg:esmi_da_cnt4       0x00000000       0xA02110EC       434         1.11.337       reg:esmi_tcmd_cnt4       0x00000000       0xA02110F0       434         1.11.338       reg:esmi_tmcd_cnt4       0x00000000       0xA02110F0       434         1.11.339       reg:esmi_dm_cnt4       0x00000000       0xA02110F4       434         1.11.340       reg:esmi_s0_cnt5       0x00000000       0xA0211100       435         1.11.341       reg:esmi_s0_crc5       0x00000000       0xA0211104       435         1.11.342       reg:esmi_s1_cnt5       0x00000000       0xA0211100       435         1.11.344       reg:esmi_s2_crc5       0x00000000       0xA0211110       435         1.11.345       reg:esmi_s2_crc5       0x00000000       0xA0211110       435         1.11.346       reg:esmi_s2_crc5       0x00000000       0xA0211110       435<	1.11.329		0x00000000 0xA02110D0	433
1.11.332         reg:esmi_s7_crc4         0x00000000         0xA02110DC         433           1.11.333         reg:esmi_rd_cnt4         0x00000000         0xA02110E0         434           1.11.334         reg:esmi_rd_crc4         0x00000000         0xA02110E4         434           1.11.335         reg:esmi_da_cnt4         0x00000000         0xA02110EC         434           1.11.336         reg:esmi_da_cnt4         0x00000000         0xA02110FC         434           1.11.337         reg:esmi_tcmd_cnt4         0x00000000         0xA02110FO         434           1.11.338         reg:esmi_twcmd_cnt4         0x00000000         0xA02110FA         434           1.11.339         reg:esmi_dm_cnt4         0x00000000         0xA02110FA         434           1.11.340         reg:esmi_s0_cnt5         0x00000000         0xA021110FA         435           1.11.341         reg:esmi_s0_crc5         0x00000000         0xA021110FA         435           1.11.342         reg:esmi_s1_cnt5         0x00000000         0xA021110FA         435           1.11.344         reg:esmi_s2_cnt5         0x00000000         0xA021110C         435           1.11.345         reg:esmi_s2_cnt5         0x00000000         0xA021111A         435	1.11.330	reg : esmi_s2_crc4	0x00000000 0xA02110D4	433
1.11.333         reg : esmi_rd_crc4         0x00000000         0xA02110E0         434           1.11.334         reg : esmi_dc_crc4         0x00000000         0xA02110E4         434           1.11.335         reg : esmi_da_cnt4         0x00000000         0xA02110E8         434           1.11.336         reg : esmi_ia_cnt4         0x00000000         0xA02110F0         434           1.11.337         reg : esmi_tcmd_cnt4         0x00000000         0xA02110F0         434           1.11.338         reg : esmi_dm_cnt4         0x00000000         0xA02110F4         434           1.11.339         reg : esmi_dm_cnt4         0x00000000         0xA02110F8         434           1.11.340         reg : esmi_s0_cnt5         0x00000000         0xA0211100         435           1.11.341         reg : esmi_s1_cnt5         0x00000000         0xA0211104         435           1.11.342         reg : esmi_s1_cnt5         0x00000000         0xA021110C         435           1.11.344         reg : esmi_s2_cnt5         0x00000000         0xA0211110         435           1.11.345         reg : esmi_s2_crc5         0x00000000         0xA0211114         435           1.11.346         reg : esmi_s2_crc5         0x00000000         0xA0211114         435 <td>1.11.331</td> <td>reg : esmi_s7_cnt4</td> <td>0x00000000 0xA02110D8</td> <td>433</td>	1.11.331	reg : esmi_s7_cnt4	0x00000000 0xA02110D8	433
1.11.334         reg:esmi_rd_crc4         0x00000000         0xA02110E4         434           1.11.335         reg:esmi_da_cnt4         0x00000000         0xA02110E8         434           1.11.336         reg:esmi_ia_cnt4         0x00000000         0xA02110EC         434           1.11.337         reg:esmi_tomd_cnt4         0x00000000         0xA02110F0         434           1.11.338         reg:esmi_twcmd_cnt4         0x00000000         0xA02110F4         434           1.11.339         reg:esmi_dm_cnt4         0x00000000         0xA02110F8         434           1.11.340         reg:esmi_s0_cnt5         0x00000000         0xA0211100         435           1.11.341         reg:esmi_s0_crc5         0x00000000         0xA0211104         435           1.11.342         reg:esmi_s1_cnt5         0x00000000         0xA021110C         435           1.11.344         reg:esmi_s2_cnt5         0x00000000         0xA0211110         435           1.11.345         reg:esmi_s2_crc5         0x00000000         0xA0211110         435           1.11.346         reg:esmi_s7_cnt5         0x00000000         0xA0211114         435           1.11.347         reg:esmi_s7_cnt5         0x00000000         0xA0211112         436		reg : esmi_s7_crc4	0x00000000 0xA02110DC	433
1.11.335       reg:esmi_da_cnt4       0x00000000       0xA02110E8       434         1.11.336       reg:esmi_ia_cnt4       0x00000000       0xA02110EC       434         1.11.337       reg:esmi_tcmd_cnt4       0x00000000       0xA02110F0       434         1.11.338       reg:esmi_twcmd_cnt4       0x00000000       0xA02110F4       434         1.11.339       reg:esmi_dm_cnt4       0x00000000       0xA02110F8       434         1.11.340       reg:esmi_s0_cnt5       0x00000000       0xA0211100       435         1.11.341       reg:esmi_s0_crc5       0x00000000       0xA0211100       435         1.11.342       reg:esmi_s1_cnt5       0x00000000       0xA0211108       435         1.11.343       reg:esmi_s1_crc5       0x00000000       0xA021110C       435         1.11.344       reg:esmi_s2_cnt5       0x00000000       0xA0211110       435         1.11.345       reg:esmi_s7_cnt5       0x00000000       0xA0211110       435         1.11.347       reg:esmi_s7_cnt5       0x00000000       0xA0211110       435         1.11.348       reg:esmi_rd_cnt5       0x00000000       0xA02111120       436         1.11.349       reg:esmi_dc_cnt5       0x00000000       0xA0211120       436				
1.11.336       reg:esmi_ia_cnt4       0x00000000       0xA02110EC       434         1.11.337       reg:esmi_tcmd_cnt4       0x00000000       0xA02110F0       434         1.11.338       reg:esmi_twcmd_cnt4       0x00000000       0xA02110F4       434         1.11.339       reg:esmi_dm_cnt4       0x00000000       0xA02110F8       434         1.11.340       reg:esmi_s0_cnt5       0x00000000       0xA0211100       435         1.11.341       reg:esmi_s0_crc5       0x00000000       0xA0211104       435         1.11.342       reg:esmi_s1_cnt5       0x00000000       0xA0211108       435         1.11.343       reg:esmi_s1_crc5       0x00000000       0xA021110C       435         1.11.344       reg:esmi_s2_crc5       0x00000000       0xA0211110       435         1.11.345       reg:esmi_s7_cnt5       0x00000000       0xA0211114       435         1.11.347       reg:esmi_s7_crc5       0x00000000       0xA0211110C       435         1.11.348       reg:esmi_s7_crc5       0x00000000       0xA0211110C       435         1.11.349       reg:esmi_rd_cnt5       0x00000000       0xA02111120       436         1.11.350       reg:esmi_ia_cnt5       0x00000000       0xA021112C       4				
1.11.337         reg : esmi_tcmd_cnt4         0x00000000         0xA02110F0         434           1.11.338         reg : esmi_twcmd_cnt4         0x00000000         0xA02110F4         434           1.11.339         reg : esmi_dm_cnt4         0x00000000         0xA02110F8         434           1.11.340         reg : esmi_s0_cnt5         0x00000000         0xA0211100         435           1.11.341         reg : esmi_s0_crc5         0x00000000         0xA0211104         435           1.11.342         reg : esmi_s1_cnt5         0x00000000         0xA0211108         435           1.11.343         reg : esmi_s1_crc5         0x00000000         0xA021110C         435           1.11.344         reg : esmi_s2_cnt5         0x00000000         0xA0211110         435           1.11.345         reg : esmi_s7_cnt5         0x00000000         0xA0211114         435           1.11.347         reg : esmi_s7_cnt5         0x00000000         0xA0211110         435           1.11.348         reg : esmi_rd_cnt5         0x00000000         0xA0211110         436           1.11.349         reg : esmi_rd_cnt5         0x00000000         0xA0211120         436           1.11.351         reg : esmi_da_cnt5         0x00000000         0xA0211124         436<				
1.11.338         reg : esmi_twcmd_cnt4         0x00000000         0xA02110F4         434           1.11.339         reg : esmi_dm_cnt4         0x00000000         0xA02110F8         434           1.11.340         reg : esmi_s0_crt5         0x00000000         0xA0211100         435           1.11.341         reg : esmi_s0_crt5         0x00000000         0xA0211104         435           1.11.342         reg : esmi_s1_crt5         0x00000000         0xA0211108         435           1.11.343         reg : esmi_s1_crt5         0x00000000         0xA021110C         435           1.11.344         reg : esmi_s2_crt5         0x00000000         0xA0211110         435           1.11.345         reg : esmi_s2_crt5         0x00000000         0xA0211114         435           1.11.346         reg : esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg : esmi_s7_crt5         0x00000000         0xA02111120         436           1.11.348         reg : esmi_rd_crt5         0x00000000         0xA0211124         436           1.11.350         reg : esmi_da_crt5         0x00000000         0xA0211128         436           1.11.351         reg : esmi_tcmd_crt5         0x00000000         0xA0211130         436				
1.11.339         reg:esmi_dm_cnt4         0x00000000         0xA02110F8         434           1.11.340         reg:esmi_s0_crt5         0x00000000         0xA0211100         435           1.11.341         reg:esmi_s0_crt5         0x00000000         0xA0211104         435           1.11.342         reg:esmi_s1_crt5         0x00000000         0xA0211108         435           1.11.343         reg:esmi_s1_crt5         0x00000000         0xA021110C         435           1.11.344         reg:esmi_s2_crt5         0x00000000         0xA0211110         435           1.11.345         reg:esmi_s2_crt5         0x00000000         0xA0211114         435           1.11.346         reg:esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg:esmi_s7_crt5         0x00000000         0xA021111C         435           1.11.348         reg:esmi_rd_crt5         0x00000000         0xA0211120         436           1.11.349         reg:esmi_rd_crt5         0x00000000         0xA0211124         436           1.11.351         reg:esmi_la_crt5         0x00000000         0xA0211120         436           1.11.352         reg:esmi_tcmd_crt5         0x00000000         0xA0211130         436				
1.11.340         reg:esmi_s0_crc5         0x00000000         0xA0211100         435           1.11.341         reg:esmi_s0_crc5         0x00000000         0xA0211104         435           1.11.342         reg:esmi_s1_crt5         0x00000000         0xA0211108         435           1.11.343         reg:esmi_s1_crc5         0x00000000         0xA0211110C         435           1.11.344         reg:esmi_s2_crt5         0x00000000         0xA0211110         435           1.11.345         reg:esmi_s2_crc5         0x00000000         0xA0211114         435           1.11.346         reg:esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg:esmi_s7_crc5         0x00000000         0xA021111C         435           1.11.348         reg:esmi_rd_crt5         0x00000000         0xA0211120         436           1.11.349         reg:esmi_rd_crc5         0x00000000         0xA0211124         436           1.11.350         reg:esmi_da_crt5         0x00000000         0xA0211120         436           1.11.352         reg:esmi_tcmd_crt5         0x00000000         0xA0211130         436           1.11.354         reg:esmi_dm_crt5         0x00000000         0xA0211138         436				
1.11.341         reg:esmi_s0_crc5         0x00000000         0xA0211104         435           1.11.342         reg:esmi_s1_crc5         0x00000000         0xA0211108         435           1.11.343         reg:esmi_s1_crc5         0x00000000         0xA0211110C         435           1.11.344         reg:esmi_s2_crc5         0x00000000         0xA0211110         435           1.11.345         reg:esmi_s2_crc5         0x00000000         0xA0211114         435           1.11.346         reg:esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg:esmi_s7_crc5         0x00000000         0xA021111C         435           1.11.348         reg:esmi_rd_crt5         0x00000000         0xA0211120         436           1.11.349         reg:esmi_rd_crt5         0x00000000         0xA0211124         436           1.11.350         reg:esmi_da_crt5         0x00000000         0xA021112C         436           1.11.351         reg:esmi_tcmd_crt5         0x00000000         0xA0211130         436           1.11.353         reg:esmi_tcmd_crt5         0x00000000         0xA0211134         436           1.11.354         reg:esmi_dm_crt5         0x00000000         0xA0211138         436				
1.11.342         reg:esmi_s1_crc5         0x00000000         0xA0211108         435           1.11.343         reg:esmi_s1_crc5         0x00000000         0xA021110C         435           1.11.344         reg:esmi_s2_crt5         0x00000000         0xA0211110         435           1.11.345         reg:esmi_s2_crc5         0x00000000         0xA0211114         435           1.11.346         reg:esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg:esmi_s7_crc5         0x00000000         0xA021111C         435           1.11.348         reg:esmi_rd_crt5         0x00000000         0xA0211120         436           1.11.349         reg:esmi_rd_crt5         0x00000000         0xA0211124         436           1.11.350         reg:esmi_da_crt5         0x00000000         0xA0211128         436           1.11.351         reg:esmi_ia_crt5         0x00000000         0xA021112C         436           1.11.352         reg:esmi_tcmd_crt5         0x00000000         0xA0211130         436           1.11.354         reg:esmi_dm_crt5         0x00000000         0xA0211138         436				
1.11.343         reg: esmi_s1_crc5         0x00000000         0xA021110C         435           1.11.344         reg: esmi_s2_crt5         0x00000000         0xA0211110         435           1.11.345         reg: esmi_s2_crc5         0x00000000         0xA0211114         435           1.11.346         reg: esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg: esmi_s7_crc5         0x00000000         0xA021111C         435           1.11.348         reg: esmi_rd_crt5         0x00000000         0xA0211120         436           1.11.349         reg: esmi_rd_crc5         0x00000000         0xA0211124         436           1.11.350         reg: esmi_da_crt5         0x00000000         0xA0211128         436           1.11.351         reg: esmi_ia_crt5         0x00000000         0xA021112C         436           1.11.352         reg: esmi_tcmd_crt5         0x00000000         0xA0211130         436           1.11.353         reg: esmi_twcmd_crt5         0x00000000         0xA0211134         436           1.11.354         reg: esmi_dm_crt5         0x00000000         0xA0211138         436				
1.11.344         reg: esmi_s2_crt5         0x00000000         0xA0211110         435           1.11.345         reg: esmi_s2_crc5         0x00000000         0xA0211114         435           1.11.346         reg: esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg: esmi_s7_crc5         0x00000000         0xA021111C         435           1.11.348         reg: esmi_rd_crt5         0x00000000         0xA0211120         436           1.11.349         reg: esmi_rd_crc5         0x00000000         0xA0211124         436           1.11.350         reg: esmi_da_crt5         0x00000000         0xA0211128         436           1.11.351         reg: esmi_ia_crt5         0x00000000         0xA021112C         436           1.11.352         reg: esmi_tcmd_crt5         0x00000000         0xA0211130         436           1.11.353         reg: esmi_twcmd_crt5         0x00000000         0xA0211134         436           1.11.354         reg: esmi_dm_crt5         0x00000000         0xA0211138         436				
1.11.345         reg: esmi_s2_crc5         0x00000000         0xA0211114         435           1.11.346         reg: esmi_s7_crt5         0x00000000         0xA0211118         435           1.11.347         reg: esmi_s7_crc5         0x00000000         0xA021111C         435           1.11.348         reg: esmi_rd_crt5         0x00000000         0xA0211120         436           1.11.349         reg: esmi_rd_crc5         0x00000000         0xA0211124         436           1.11.350         reg: esmi_da_cnt5         0x00000000         0xA0211128         436           1.11.351         reg: esmi_ia_cnt5         0x00000000         0xA021112C         436           1.11.352         reg: esmi_tcmd_cnt5         0x00000000         0xA0211130         436           1.11.353         reg: esmi_twcmd_cnt5         0x00000000         0xA0211134         436           1.11.354         reg: esmi_dm_cnt5         0x00000000         0xA0211138         436				
1.11.346       reg: esmi_s7_cnt5       0x00000000       0xA0211118       435         1.11.347       reg: esmi_s7_crc5       0x00000000       0xA021111C       435         1.11.348       reg: esmi_rd_cnt5       0x00000000       0xA0211120       436         1.11.349       reg: esmi_rd_crc5       0x00000000       0xA0211124       436         1.11.350       reg: esmi_da_cnt5       0x00000000       0xA0211128       436         1.11.351       reg: esmi_ia_cnt5       0x00000000       0xA021112C       436         1.11.352       reg: esmi_tcmd_cnt5       0x00000000       0xA0211130       436         1.11.353       reg: esmi_twcmd_cnt5       0x00000000       0xA0211134       436         1.11.354       reg: esmi_dm_cnt5       0x00000000       0xA0211138       436				
1.11.347       reg: esmi_s7_crc5       0x00000000       0xA021111C       435         1.11.348       reg: esmi_rd_crt5       0x00000000       0xA0211120       436         1.11.349       reg: esmi_rd_crc5       0x00000000       0xA0211124       436         1.11.350       reg: esmi_da_cnt5       0x00000000       0xA0211128       436         1.11.351       reg: esmi_ia_cnt5       0x00000000       0xA021112C       436         1.11.352       reg: esmi_tcmd_cnt5       0x00000000       0xA0211130       436         1.11.353       reg: esmi_twcmd_cnt5       0x00000000       0xA0211134       436         1.11.354       reg: esmi_dm_cnt5       0x00000000       0xA0211138       436				
1.11.348         reg : esmi_rd_cnt5         0x00000000         0xA0211120         436           1.11.349         reg : esmi_rd_crc5         0x00000000         0xA0211124         436           1.11.350         reg : esmi_da_cnt5         0x00000000         0xA0211128         436           1.11.351         reg : esmi_ia_cnt5         0x00000000         0xA021112C         436           1.11.352         reg : esmi_tcmd_cnt5         0x00000000         0xA0211130         436           1.11.353         reg : esmi_twcmd_cnt5         0x00000000         0xA0211134         436           1.11.354         reg : esmi_dm_cnt5         0x00000000         0xA0211138         436				
1.11.349       reg: esmi_rd_crc5       0x00000000       0xA0211124       436         1.11.350       reg: esmi_da_cnt5       0x00000000       0xA0211128       436         1.11.351       reg: esmi_ia_cnt5       0x00000000       0xA021112C       436         1.11.352       reg: esmi_tcmd_cnt5       0x00000000       0xA0211130       436         1.11.353       reg: esmi_twcmd_cnt5       0x00000000       0xA0211134       436         1.11.354       reg: esmi_dm_cnt5       0x00000000       0xA0211138       436				
1.11.350       reg : esmi_da_cnt5       0x00000000       0xA0211128       436         1.11.351       reg : esmi_ia_cnt5       0x00000000       0xA021112C       436         1.11.352       reg : esmi_tcmd_cnt5       0x00000000       0xA0211130       436         1.11.353       reg : esmi_twcmd_cnt5       0x00000000       0xA0211134       436         1.11.354       reg : esmi_dm_cnt5       0x00000000       0xA0211138       436				
1.11.352     reg : esmi_tcmd_cnt5     0x00000000     0xA0211130     436       1.11.353     reg : esmi_twcmd_cnt5     0x00000000     0xA0211134     436       1.11.354     reg : esmi_dm_cnt5     0x00000000     0xA0211138     436				
1.11.353     reg: esmi_twcmd_cnt5     0x00000000     0xA0211134     436       1.11.354     reg: esmi_dm_cnt5     0x00000000     0xA0211138     436				
1.11.354 reg : esmi_dm_cnt5 0x00000000 0xA0211138 436	1.11.352	reg : esmi_tcmd_cnt5	0x00000000 0xA0211130	
1.11.355   reg : esmi_s0_cnt6   0x00000000   0xA0211140   436				
	1.11.355	reg : esmi_s0_cnt6	0x00000000  0xA0211140	436

				1.5-
1.11.356	reg : esmi_s0_crc6		0xA0211144	437
1.11.357	reg : esmi_s1_cnt6		0xA0211148	437
1.11.358	reg : esmi_s1_crc6		0xA021114C	437
1.11.359	reg : esmi_s2_cnt6		0xA0211150	437
1.11.360	reg : esmi_s2_crc6	0x00000000		437
1.11.361	reg : esmi_s7_cnt6	0x00000000		437
1.11.362	reg : esmi_s7_crc6		0xA021115C	437
1.11.363	reg : esmi_rd_cnt6	0x00000000		438
1.11.364	reg : esmi_rd_crc6	0x00000000	0xA0211164	438
1.11.365	reg : esmi_da_cnt6	0x00000000	0xA0211168	438
1.11.366	reg : esmi_ia_cnt6	0x00000000	0xA021116C	438
1.11.367	reg : esmi_tcmd_cnt6	0x00000000	0xA0211170	438
1.11.368	reg : esmi_twcmd_cnt6	0x00000000	0xA0211174	438
1.11.369	reg : esmi_dm_cnt6	0x00000000	0xA0211178	438
1.11.370	reg : esmi_s0_cnt7	0x00000000	0xA0211180	438
1.11.371	reg : esmi_s0_crc7	0x00000000	0xA0211184	439
1.11.372	reg : esmi_s1_cnt7	0x00000000	0xA0211188	439
1.11.373	reg : esmi_s1_crc7	0x00000000	0xA021118C	439
1.11.374	reg : esmi_s2_cnt7			439
1.11.375	reg : esmi_s2_crc7			439
1.11.376	reg : esmi_s7_cnt7	0x00000000		439
1.11.377	reg : esmi_s7_crc7		0xA021119C	439
1.11.378	reg : esmi_rd_cnt7	0x00000000		439
1.11.379	reg : esmi_rd_crc7	0x00000000		440
1.11.380	reg : esmi_da_cnt7	0x00000000		440
1.11.381	reg : esmi_ia_cnt7		0xA02111AC	440
1.11.382	reg : esmi_tcmd_cnt7			440
1.11.383	reg : esmi_twcmd_cnt7		0xA02111B4	440
1.11.384	reg : esmi_dm_cnt7		0xA02111B8	440
1.11.385	reg : esmi_s0_cnt8			440
1.11.386	reg : esmi_s0_crc8		0xA02111C4	441
1.11.387	reg : esmi_s1_cnt8		0xA02111C8	441
1.11.388	reg : esmi_s1_crc8	0x00000000	0xA02111CC	441
1.11.389	reg : esmi_s2_cnt8	0x00000000	0xA02111D0	441
1.11.390	reg : esmi_s2_crc8	0x00000000	0xA02111D4	441
1.11.391	reg : esmi_s7_cnt8	0x00000000	0xA02111D8	441
1.11.392	reg : esmi_s7_crc8	0x00000000	0xA02111DC	441
1.11.393	reg : esmi_rd_cnt8	0x00000000	0xA02111E0	441
1.11.394	reg : esmi_rd_crc8	0x00000000	0xA02111E4	442
1.11.395	reg : esmi_da_cnt8	0x00000000	0xA02111E8	442
1.11.396	reg : esmi_ia_cnt8	0x00000000	0xA02111EC	442
1.11.397	reg : esmi_tcmd_cnt8	0x00000000	0xA02111F0	442
1.11.398	reg : esmi_twcmd_cnt8	0x00000000	0xA02111F4	442
1.11.399	reg : esmi_dm_cnt8		0xA02111F8	442
1.11.400	reg : esmi_s0_cnt9		0xA0211200	442
1.11.401	reg : esmi_s0_crc9		0xA0211204	442
1.11.402	reg : esmi_s1_cnt9		0xA0211208	443
1.11.403	reg : esmi_s1_crc9		0xA021120C	443
1.11.404	reg : esmi_s2_cnt9	0x00000000		443
1.11.405	reg : esmi_s2_crc9			443
1.11.406	reg : esmi_s7_cnt9	0x00000000		443
1.11.407	reg : esmi_s7_crc9	0x00000000		443
1.11.408	reg : esmi_rd_cnt9		0xA0211220	443
1.11.409	reg : esmi_rd_crc9			444
1.11.410	reg : esmi_da_cnt9		0xA0211228	444
1.11.411	reg : esmi_ia_cnt9		0xA021122C	444
1.11.412	reg : esmi_tcmd_cnt9			444
1.11.413	reg : esmi_twcmd_cnt9		0xA0211234	444
1.11.414	reg : esmi_dm_cnt9		0xA0211238	444
1.11.415	reg : esmi_s0_cnt10		0xA0211240	444
1.11.416	reg : esmi_s0_crc10		0xA0211244	444
1.11.417	reg : esmi_s1_cnt10		0xA0211248	445
1.11.418	reg : esmi_s1_crc10		0xA021124C	445
1.11.419	reg : esmi_s2_cnt10		0xA0211250	445
1.11.420	reg : esmi_s2_crc10	0x00000000		445
1.11.421	reg : esmi_s7_cnt10	0x00000000	0xA0211258	445

		T	1
1.11.422	reg : esmi_s7_crc10	0x00000000 0xA021125C	445
1.11.423	reg : esmi_rd_cnt10	0x00000000 0xA0211260	445
1.11.424	reg : esmi_rd_crc10	0x00000000 0xA0211264	445
1.11.425	reg : esmi_da_cnt10	0x00000000 0xA0211268	446
1.11.426	reg : esmi_ia_cnt10	0x00000000 0xA021126C	446
1.11.427	reg : esmi_tcmd_cnt10	0x00000000 0xA0211270	446
1.11.428	reg : esmi_twcmd_cnt10	0x00000000 0xA0211274	446
1.11.429	reg : esmi_dm_cnt10	0x00000000 0xA0211278	446
1.11.430	reg : esmi_s0_cnt11	0x00000000 0xA0211280	446
1.11.431	reg : esmi_s0_crc11	0x00000000 0xA0211284	446
1.11.432	reg : esmi_s1_cnt11	0x00000000 0xA0211288	447
1.11.433	reg : esmi_s1_crc11	0x00000000 0xA021128C	447
1.11.434	reg : esmi_s2_cnt11	0x00000000 0xA0211290	447
1.11.435	reg : esmi_s2_crc11	0x00000000 0xA0211294	447
1.11.436	reg : esmi_s7_cnt11	0x00000000 0xA0211298	447
1.11.437	reg : esmi_s7_crc11	0x00000000 0xA021129C	447
1.11.438	reg : esmi_rd_cnt11	0x00000000 0xA02112A0	447
1.11.439	reg : esmi_rd_crc11	0x00000000 0xA02112A4	447
1.11.440	reg : esmi_da_cnt11	0x00000000 0xA02112A8	448
1.11.441	reg : esmi_ia_cnt11	0x00000000 0xA02112AC	448
1.11.442	reg : esmi_tcmd_cnt11	0x00000000 0xA02112B0	448
1.11.443	reg : esmi_twcmd_cnt11	0x00000000 0xA02112B4	448
1.11.444	reg : esmi_dm_cnt11	0x00000000 0xA02112B8	448
1.11.445	reg : esmi_s0_cnt12	0x00000000 0xA02112C0	448
1.11.446	reg : esmi_s0_crc12	0x00000000 0xA02112C4	448
1.11.447	reg : esmi_s1_cnt12	0x00000000 0xA02112C8	448
1.11.448	reg : esmi_s1_crc12	0x00000000 0xA02112CC	449
1.11.449	reg : esmi_s2_cnt12	0x00000000 0xA02112D0	449
1.11.450	reg : esmi_s2_crc12	0x00000000 0xA02112D4	449
1.11.451	reg : esmi_s7_cnt12	0x00000000 0xA02112D8	449
1.11.452	reg : esmi_s7_crc12	0x00000000 0xA02112DC	449
1.11.453	reg : esmi_rd_cnt12	0x00000000 0xA02112E0	449
1.11.454	reg : esmi_rd_crc12	0x00000000 0xA02112E4	449
1.11.455	reg : esmi_da_cnt12	0x00000000 0xA02112E8	450
1.11.456	reg : esmi_ia_cnt12	0x00000000 0xA02112EC	450
1.11.457	reg : esmi_tcmd_cnt12	0x00000000 0xA02112F0	450
1.11.458	reg : esmi_twcmd_cnt12	0x00000000 0xA02112F4	450
1.11.459	reg : esmi_dm_cnt12	0x00000000 0xA02112F8	450
1.11.460	reg : esmi_s0_cnt13	0x00000000 0xA0211300	450
1.11.461	reg : esmi_s0_crc13	0x00000000 0xA0211304	450
1.11.462	reg : esmi_s1_cnt13	0x00000000 0xA0211308	450
1.11.463	reg : esmi_s1_crc13	0x00000000 0xA021130C	451
1.11.464	reg : esmi_s2_cnt13	0x00000000 0xA0211310	451
1.11.465	reg : esmi_s2_crc13	0x00000000 0xA0211314	451
1.11.466	reg : esmi_s7_cnt13	0x00000000 0xA0211318	451
1.11.467	reg : esmi_s7_crc13	0x00000000 0xA021131C	451
1.11.468	reg : esmi_rd_cnt13	0x0000000 0xA0211320	451
1.11.469	reg : esmi_rd_crc13	0x0000000 0xA0211324	451
1.11.470	reg : esmi_da_cnt13	0x00000000 0xA0211328	451
1.11.471	reg : esmi_ia_cnt13	0x00000000 0xA021132C	452
1.11.472	reg : esmi_tcmd_cnt13	0x0000000 0xA0211330	452
1.11.473	reg : esmi_twcmd_cnt13	0x00000000 0xA0211334	452
1.11.474	reg : esmi_dm_cnt13	0x00000000 0xA0211338	452 452
1.11.475 1.11.476	reg : esmi_s0_cnt14 reg : esmi_s0_crc14	0x00000000 0xA0211340 0x00000000 0xA0211344	452 452
1.11.476	reg : esmi_s0_crc14 reg : esmi_s1_cnt14	0x00000000 0xA0211344 0x00000000 0xA0211348	452 452
1.11.477	reg : esmi_s1_crc14	0x00000000 0xA0211346 0x00000000 0xA021134C	452
1.11.478	reg : esmi_s1_crc14	0x00000000 0xA021134C 0x00000000 0xA0211350	453
1.11.479	reg : esmi_s2_crc14	0x00000000 0xA0211350 0x00000000 0xA0211354	453
1.11.481	reg : esmi_s2_crc14	0x00000000 0xA0211354 0x00000000 0xA0211358	453
1.11.482	reg : esmi_s7_crc14	0x00000000 0xA0211356 0x00000000 0xA021135C	453
1.11.483	reg : esmi_rd_cnt14	0x00000000 0xA021135C	453
1.11.484	reg : esmi_rd_crc14	0x00000000 0xA0211360 0x00000000 0xA0211364	453
1.11.485	reg : esmi_da_cnt14	0x00000000 0xA0211364 0x00000000 0xA0211368	453
1.11.486	reg : esmi_ia_cnt14	0x00000000 0xA0211366 0x00000000 0xA021136C	454
1.11.487	reg : esmi_tcmd_cnt14	0x00000000 0xA0211300	454
7.11.707	10g. oom_toma_ont14	CACCOCCCC CATOL TOTO	70-7

11.14.89					1
11.1490	1.11.488	reg : esmi_twcmd_cnt14	0x00000000	0xA0211374	454
11.1.492					
1.1.1.493					
1.11.495					
1.11.496					
111.499 reg : semi rd cnt15					
1.11.488 reg semi_rd_crof5					
1.11.499					
1.11.500 reg : semi_la_cnt15					
111.501   reg : esmi tcmd cnt15					
1.11.502					
111.503					
111.504					
1.11.505   eg.; esmi_s0_crc16   0x00000000   0xA02113C4   456   1.11.506   reg.; esmi_s1_crc16   0x00000000   0xA02113C4   456   1.11.508   reg.; esmi_s1_crc16   0x00000000   0xA02113C8   456   1.11.508   reg.; esmi_s1_crc16   0x00000000   0xA02113CC   456   1.11.508   reg.; esmi_s1_crc16   0x00000000   0xA02113CC   456   1.11.509   reg.; esmi_s2_crc16   0x00000000   0xA02113DA   457   1.11.510   reg.; esmi_s7_crc16   0x00000000   0xA02113DA   457   1.11.511   reg.; esmi_s7_crc16   0x00000000   0xA02113DA   457   1.11.511   reg.; esmi_s7_crc16   0x00000000   0xA02113DA   457   1.11.512   reg.; esmi_s7_crc16   0x00000000   0xA02113DA   457   1.11.513   reg.; esmi_d_crc16   0x00000000   0xA02113ED   457   1.11.515   reg.; esmi_d_crc16   0x00000000   0xA02113EA   457   1.11.515   reg.; esmi_d_crc16   0x00000000   0xA02113EA   457   1.11.516   reg.; esmi_d_crc16   0x00000000   0xA02113EA   457   1.11.517   reg.; esmi_d_crc16   0x00000000   0xA02113EC   457   1.11.518   reg.; esmi_d_crc16   0x00000000   0xA02113EA   458   1.11.519   reg.; esmi_d_crc16   0x00000000   0xA02113FA   458   1.11.519   reg.; esmi_d_crc16   0x00000000   0xA02113FA   458   1.11.520   reg.; esmi_s0_crc17   0x00000000   0xA02113FA   458   1.11.521   reg.; esmi_s0_crc17   0x00000000   0xA021140A   458   1.11.522   reg.; esmi_s0_crc17   0x00000000   0xA021140A   458   1.11.524   reg.; esmi_s0_crc17   0x00000000   0xA021140A   458   1.11.524   reg.; esmi_s0_crc17   0x00000000   0xA021140A   459   1.11.525   reg.; esmi_s0_crc17   0x00000000   0xA021140A   459   1.11.526   reg.; esmi_s0_crc17   0x00000000   0xA021140A   459   1.11.526   reg.; esmi_s0_crc17   0x00000000   0xA021140A   459   1.11.526   reg.; esmi_s0_crc17   0x00000000   0xA021140A   459   1.11.527   reg.; esmi_s0_crc17   0x00000000   0xA021140A   459   1.11.528   reg.; esmi_s0_crc17   0x00000000   0xA021140A   459   1.11.529   reg.; esmi_s0_crc18   0x00000000   0xA021140A   460   1.11.539   reg.; esmi_s0_crc18   0x00000000   0xA021144A   460   1.11.539   reg.; esmi_s0_crc18   0x000					
1.11.5.06         reg: esmi_s0_crc16         0x00000000         0xA02113CA         456           1.11.5.07         reg: esmi_s1_crc16         0x00000000         0xA02113CC         456           1.11.5.09         reg: esmi_s1_crc16         0x00000000         0xA02113D0         457           1.11.5.10         reg: esmi_s2_crc16         0x00000000         0xA02113D0         457           1.11.5.11         reg: esmi_s7_crc16         0x00000000         0xA02113DC         457           1.11.5.12         reg: esmi_s7_crc16         0x00000000         0xA02113DC         457           1.11.5.13         reg: esmi_d_crc16         0x00000000         0xA02113E0         457           1.11.5.14         reg: esmi_d_crc16         0x00000000         0xA02113E4         457           1.11.5.15         reg: esmi_d_a_crc16         0x00000000         0xA02113E0         457           1.11.5.15         reg: esmi_d_a_crc16         0x00000000         0xA02113E0         457           1.11.5.17         reg: esmi_d_a_crc16         0x00000000         0xA02113E0         457           1.11.5.17         reg: esmi_d_a_crt16         0x00000000         0xA02113E0         457           1.11.5.18         reg: esmi_d_a_crt16         0x00000000         0xA02113E0					
1.11.507   reg : esmi_s1_crc16					
1.11.508					
1.11.509   reg : esmi_s2_cnt16					
1.11.510         reg:esmi.s2_crc16         0x00000000         0xA02113DA         457           1.11.511         reg:esmi.s7_crc16         0x00000000         0xA02113DB         457           1.11.512         reg:esmi.s7_crc16         0x00000000         0xA02113EO         457           1.11.513         reg:esmi.rd_crc16         0x00000000         0xA02113EO         457           1.11.515         reg:esmi.da_cnt16         0x00000000         0xA02113EC         457           1.11.516         reg:esmi.da_cnt16         0x00000000         0xA02113EC         457           1.11.517         reg:esmi.da_cnt16         0x00000000         0xA02113EC         457           1.11.518         reg:esmi.da_cnt16         0x00000000         0xA02113F0         458           1.11.529         reg:esmi.dm_cnt16         0x00000000         0xA02113F8         458           1.11.520         reg:esmi.sd_cnt17         0x00000000         0xA0211404         458           1.11.521         reg:esmi.sd_crc17         0x00000000         0xA0211404         458           1.11.522         reg:esmi.sd_cnt17         0x00000000         0xA0211404         458           1.11.524         reg:esmi.sd_cnt17         0x00000000         0xA0211400         458					
1.11.511         reg:esmi_s7_crt16         0x00000000         0xA02113DB         457           1.11.512         reg:esmi_s7_crt16         0x00000000         0xA02113E0         457           1.11.513         reg:esmi_rd_crt16         0x00000000         0xA02113E4         457           1.11.515         reg:esmi_da_cnt16         0x00000000         0xA02113EA         457           1.11.516         reg:esmi_la_cnt16         0x00000000         0xA02113EC         457           1.11.517         reg:esmi_tcmd_cnt16         0x00000000         0xA02113F0         458           1.11.518         reg:esmi_tcmd_cnt16         0x00000000         0xA02113F0         458           1.11.519         reg:esmi_dm_cnt16         0x00000000         0xA02113F4         458           1.11.520         reg:esmi_dm_cnt16         0x00000000         0xA02113F4         458           1.11.520         reg:esmi_s0_cnt17         0x00000000         0xA0211400         458           1.11.521         reg:esmi_s0_cnt17         0x00000000         0xA0211404         458           1.11.522         reg:esmi_s1_cnt17         0x00000000         0xA0211400         458           1.11.523         reg:esmi_s1_cnt17         0x00000000         0xA0211400         458					
1.11.512         reg:esmi_s7_ccr16         0x00000000         0xA02113EO         457           1.11.513         reg:esmi_rd_crt16         0x00000000         0xA02113E0         457           1.11.516         reg:esmi_rd_crt16         0x00000000         0xA02113E8         457           1.11.516         reg:esmi_la_crt16         0x00000000         0xA02113E0         457           1.11.517         reg:esmi_lcmd_crt16         0x00000000         0xA02113F0         458           1.11.518         reg:esmi_lcmd_crt16         0x00000000         0xA02113F4         458           1.11.519         reg:esmi_d_m_crt16         0x00000000         0xA02113F4         458           1.11.521         reg:esmi_s0_crt17         0x00000000         0xA0211400         458           1.11.521         reg:esmi_s0_crt17         0x00000000         0xA0211404         458           1.11.522         reg:esmi_s1_crt17         0x00000000         0xA0211404         458           1.11.522         reg:esmi_s2_crt17         0x00000000         0xA0211400         458           1.11.524         reg:esmi_s2_crt17         0x00000000         0xA0211410         459           1.11.525         reg:esmi_s7_crt17         0x000000000         0xA0211410         459 <td></td> <td></td> <td></td> <td></td> <td></td>					
1.11.513         reg : esmi_rd_crt16         0x00000000         0xA02113E0         457           1.11.514         reg : esmi_rd_crt16         0x00000000         0xA02113E4         457           1.11.516         reg : esmi_da_cnt16         0x00000000         0xA02113EC         457           1.11.517         reg : esmi_tomd_cnt16         0x00000000         0xA02113F0         458           1.11.517         reg : esmi_twomd_cnt16         0x00000000         0xA02113F4         458           1.11.519         reg : esmi_dm_cnt16         0x00000000         0xA02113F4         458           1.11.520         reg : esmi_s0_cnt17         0x00000000         0xA0211400         458           1.11.520         reg : esmi_s0_cnt17         0x00000000         0xA0211404         458           1.11.521         reg : esmi_s1_cnt17         0x00000000         0xA0211404         458           1.11.522         reg : esmi_s1_crt17         0x00000000         0xA0211404         458           1.11.523         reg : esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.524         reg : esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.526         reg : esmi_s7_cnt17         0x00000000         0xA0211410					
1.11.514         reg : esmi_rd_crc16         0x00000000         0xA02113E4         457           1.11.515         reg : esmi_da_cnt16         0x00000000         0xA02113E8         457           1.11.516         reg : esmi_la_cnt16         0x00000000         0xA02113F0         458           1.11.517         reg : esmi_tcmd_cnt16         0x00000000         0xA02113F0         458           1.11.518         reg : esmi_tdm_cnt16         0x00000000         0xA02113F8         458           1.11.520         reg : esmi_sd_cnt17         0x00000000         0xA0211400         458           1.11.521         reg : esmi_sd_cnt17         0x00000000         0xA0211404         458           1.11.522         reg : esmi_sd_cnt17         0x00000000         0xA0211408         458           1.11.523         reg : esmi_sd_cnt17         0x00000000         0xA0211408         458           1.11.524         reg : esmi_sd_cnt17         0x00000000         0xA0211410         459           1.11.525         reg : esmi_sd_cnt17         0x00000000         0xA0211410         459           1.11.526         reg : esmi_sd_cnt17         0x00000000         0xA0211414         459           1.11.527         reg : esmi_sf_cnt17         0x00000000         0xA0211420					
1.11.515         reg : esmi_da_cnt16         0x00000000         0xA02113E8         457           1.11.516         reg : esmi_tcmd_cnt16         0x00000000         0xA02113FO         458           1.11.518         reg : esmi_tcmd_cnt16         0x00000000         0xA02113F4         458           1.11.519         reg : esmi_dm_cnt16         0x00000000         0xA02113F4         458           1.11.520         reg : esmi_s0_cnt17         0x00000000         0xA0211400         458           1.11.521         reg : esmi_s0_cnt17         0x00000000         0xA0211404         458           1.11.522         reg : esmi_s1_cnt17         0x00000000         0xA0211404         458           1.11.523         reg : esmi_s2_cnt17         0x00000000         0xA021140C         458           1.11.524         reg : esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.525         reg : esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.526         reg : esmi_s2_cnt17         0x00000000         0xA0211414         459           1.11.527         reg : esmi_s2_cnt17         0x00000000         0xA0211414         459           1.11.528         reg : esmi_s2_cnt17         0x00000000         0xA0211420					
1.11.516	1.11.514	reg : esmi_rd_crc16	0x00000000	0xA02113E4	
1.11.517         reg : esmi_twcmd_cnt16         0x00000000         0xA02113F0         458           1.11.518         reg : esmi_twcmd_cnt16         0x00000000         0xA02113F8         458           1.11.520         reg : esmi_dm_cnt17         0x00000000         0xA0211400         458           1.11.521         reg : esmi_s0_cnt17         0x00000000         0xA0211404         458           1.11.521         reg : esmi_s1_cnt17         0x00000000         0xA0211404         458           1.11.522         reg : esmi_s1_crt17         0x00000000         0xA021140C         458           1.11.524         reg : esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.525         reg : esmi_s2_crt17         0x00000000         0xA0211410         459           1.11.526         reg : esmi_s2_crt17         0x00000000         0xA0211418         459           1.11.527         reg : esmi_s7_crt17         0x00000000         0xA0211418         459           1.11.528         reg : esmi_rd_crt17         0x00000000         0xA0211420         459           1.11.529         reg : esmi_rd_crt17         0x00000000         0xA0211424         459           1.11.520         reg : esmi_rd_crt17         0x00000000         0xA0211424	1.11.515	reg : esmi_da_cnt16	0x00000000	0xA02113E8	457
1.11.518	1.11.516	reg : esmi_ia_cnt16	0x00000000	0xA02113EC	
1.11.519         reg:esmi_dm_cnt16         0x0000000         0xA02113F8         458           1.11.520         reg:esmi_s0_crc17         0x0000000         0xA0211400         458           1.11.521         reg:esmi_s0_crc17         0x0000000         0xA0211404         458           1.11.522         reg:esmi_s1_crc17         0x00000000         0xA0211408         458           1.11.523         reg:esmi_s1_crc17         0x00000000         0xA0211410         458           1.11.524         reg:esmi_s2_crc17         0x00000000         0xA0211410         459           1.11.525         reg:esmi_s2_crc17         0x00000000         0xA0211414         459           1.11.526         reg:esmi_s7_crc17         0x00000000         0xA0211418         459           1.11.527         reg:esmi_rd_crc17         0x00000000         0xA0211420         459           1.11.528         reg:esmi_rd_crc17         0x00000000         0xA0211420         459           1.11.529         reg:esmi_da_crt17         0x00000000         0xA0211424         459           1.11.531         reg:esmi_da_crt17         0x00000000         0xA0211420         459           1.11.532         reg:esmi_da_crt17         0x00000000         0xA0211430         460 <t< td=""><td>1.11.517</td><td>reg : esmi_tcmd_cnt16</td><td>0x00000000</td><td>0xA02113F0</td><td>458</td></t<>	1.11.517	reg : esmi_tcmd_cnt16	0x00000000	0xA02113F0	458
1.11.520         reg:esmi_s0_cnt17         0x00000000         0xA0211400         458           1.11.521         reg:esmi_s0_crc17         0x00000000         0xA0211404         458           1.11.522         reg:esmi_s1_cnt17         0x00000000         0xA021140C         458           1.11.523         reg:esmi_s1_crc17         0x00000000         0xA0211410         458           1.11.524         reg:esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.525         reg:esmi_s2_crc17         0x00000000         0xA0211414         459           1.11.526         reg:esmi_s7_cnt17         0x00000000         0xA0211418         459           1.11.527         reg:esmi_s7_crc17         0x00000000         0xA0211420         459           1.11.528         reg:esmi_d_cnt17         0x00000000         0xA0211420         459           1.11.529         reg:esmi_da_cnt17         0x00000000         0xA0211424         459           1.11.531         reg:esmi_da_cnt17         0x00000000         0xA0211426         459           1.11.532         reg:esmi_da_cnt17         0x00000000         0xA0211430         460           1.11.533         reg:esmi_da_cnt17         0x00000000         0xA0211444         460	1.11.518	reg : esmi_twcmd_cnt16	0x00000000	0xA02113F4	458
1.11.521         reg:esmi_s0_crc17         0x00000000         0xA0211404         458           1.11.522         reg:esmi_s1_cnt17         0x00000000         0xA021140C         458           1.11.523         reg:esmi_s1_crc17         0x00000000         0xA0211410         458           1.11.524         reg:esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.525         reg:esmi_s2_crc17         0x00000000         0xA0211418         459           1.11.526         reg:esmi_s7_cnt17         0x00000000         0xA0211418         459           1.11.527         reg:esmi_s7_crc17         0x00000000         0xA0211420         459           1.11.529         reg:esmi_rd_crc17         0x00000000         0xA0211424         459           1.11.530         reg:esmi_da_cnt17         0x00000000         0xA0211428         459           1.11.531         reg:esmi_ala_cnt17         0x00000000         0xA0211420         459           1.11.533         reg:esmi_dm_cnt17         0x00000000         0xA0211420         459           1.11.534         reg:esmi_dm_cnt17         0x00000000         0xA0211430         460           1.11.534         reg:esmi_so_cnt18         0x00000000         0xA0211440         460	1.11.519	reg : esmi_dm_cnt16	0x00000000	0xA02113F8	458
1.11.522         reg:esmi_s1_crc17         0x00000000         0xA0211408         458           1.11.523         reg:esmi_s1_crc17         0x00000000         0xA021140C         458           1.11.524         reg:esmi_s2_crc17         0x00000000         0xA0211410         459           1.11.525         reg:esmi_s2_crc17         0x00000000         0xA0211414         459           1.11.526         reg:esmi_s7_crc17         0x00000000         0xA0211410         459           1.11.527         reg:esmi_s7_crc17         0x00000000         0xA0211420         459           1.11.528         reg:esmi_rd_crc17         0x00000000         0xA0211420         459           1.11.529         reg:esmi_d_crc17         0x00000000         0xA0211424         459           1.11.531         reg:esmi_d_a_cnt17         0x00000000         0xA0211426         459           1.11.532         reg:esmi_d_cnt17         0x00000000         0xA0211430         460           1.11.533         reg:esmi_d_cnt17         0x00000000         0xA0211434         460           1.11.534         reg:esmi_d_cnt18         0x0000000         0xA0211440         460           1.11.535         reg:esmi_s0_crt18         0x0000000         0xA0211440         460	1.11.520	reg : esmi_s0_cnt17	0x00000000	0xA0211400	458
1.11.523         reg:esmi_s1_crc17         0x00000000         0xA021140C         458           1.11.524         reg:esmi_s2_crc17         0x00000000         0xA0211410         459           1.11.525         reg:esmi_s2_crc17         0x00000000         0xA0211414         459           1.11.526         reg:esmi_s7_crc17         0x00000000         0xA0211418         459           1.11.527         reg:esmi_s7_crc17         0x00000000         0xA0211410         459           1.11.528         reg:esmi_rd_crc17         0x00000000         0xA0211420         459           1.11.529         reg:esmi_rd_crc17         0x00000000         0xA0211424         459           1.11.530         reg:esmi_da_cnt17         0x00000000         0xA0211426         459           1.11.531         reg:esmi_tac_nt17         0x00000000         0xA021142C         459           1.11.532         reg:esmi_temd_cnt17         0x00000000         0xA0211430         460           1.11.533         reg:esmi_dm_cnt17         0x00000000         0xA0211434         460           1.11.534         reg:esmi_dm_cnt17         0x00000000         0xA0211440         460           1.11.537         reg:esmi_s0_crt18         0x00000000         0xA0211440         460	1.11.521	reg : esmi_s0_crc17	0x00000000	0xA0211404	458
1.11.524         reg : esmi_s2_cnt17         0x00000000         0xA0211410         459           1.11.525         reg : esmi_s2_crc17         0x00000000         0xA0211414         459           1.11.526         reg : esmi_s7_cnt17         0x00000000         0xA0211418         459           1.11.527         reg : esmi_s7_crc17         0x00000000         0xA0211420         459           1.11.528         reg : esmi_rd_cnt17         0x00000000         0xA0211420         459           1.11.530         reg : esmi_da_cnt17         0x00000000         0xA0211428         459           1.11.531         reg : esmi_la_cnt17         0x00000000         0xA021142C         459           1.11.531         reg : esmi_la_cnt17         0x00000000         0xA021142C         459           1.11.531         reg : esmi_la_cnt17         0x00000000         0xA0211430         460           1.11.532         reg : esmi_dm_cnt17         0x00000000         0xA0211434         460           1.11.533         reg : esmi_dm_cnt17         0x00000000         0xA0211440         460           1.11.535         reg : esmi_s0_crt18         0x00000000         0xA0211444         460           1.11.536         reg : esmi_s1_crt18         0x00000000         0xA0211444	1.11.522	reg : esmi_s1_cnt17	0x00000000	0xA0211408	458
1.11.525         reg : esmi_s2_crc17         0x00000000         0xA0211414         459           1.11.526         reg : esmi_s7_crc17         0x00000000         0xA0211418         459           1.11.527         reg : esmi_s7_crc17         0x00000000         0xA021141C         459           1.11.528         reg : esmi_rd_crc17         0x00000000         0xA0211420         459           1.11.529         reg : esmi_da_crc17         0x00000000         0xA0211424         459           1.11.530         reg : esmi_da_crc17         0x00000000         0xA021142C         459           1.11.531         reg : esmi_lcmd_crc17         0x00000000         0xA021142C         459           1.11.532         reg : esmi_tcmd_crc17         0x00000000         0xA0211430         460           1.11.533         reg : esmi_dm_crc117         0x00000000         0xA0211434         460           1.11.534         reg : esmi_dm_crc117         0x00000000         0xA0211438         460           1.11.535         reg : esmi_s0_crc18         0x00000000         0xA0211444         460           1.11.536         reg : esmi_s0_crc18         0x00000000         0xA0211444         460           1.11.537         reg : esmi_s1_crc18         0x00000000         0xA0211446	1.11.523	reg : esmi_s1_crc17	0x00000000	0xA021140C	458
1.11.526         reg : esmi_s7_cnt17         0x0000000         0xA0211418         459           1.11.527         reg : esmi_s7_crc17         0x0000000         0xA021141C         459           1.11.528         reg : esmi_rd_cnt17         0x00000000         0xA0211420         459           1.11.529         reg : esmi_rd_crc17         0x00000000         0xA0211424         459           1.11.530         reg : esmi_da_cnt17         0x00000000         0xA021142C         459           1.11.531         reg : esmi_tcmd_cnt17         0x00000000         0xA021142C         459           1.11.532         reg : esmi_tcmd_cnt17         0x00000000         0xA0211430         460           1.11.533         reg : esmi_dm_cnt17         0x00000000         0xA0211434         460           1.11.534         reg : esmi_dm_cnt17         0x00000000         0xA0211438         460           1.11.535         reg : esmi_sol_crt18         0x00000000         0xA0211440         460           1.11.536         reg : esmi_sol_crt18         0x00000000         0xA0211444         460           1.11.537         reg : esmi_sol_crt18         0x00000000         0xA0211448         460           1.11.539         reg : esmi_sol_crt18         0x00000000         0xA0211440	1.11.524	reg : esmi_s2_cnt17	0x00000000	0xA0211410	459
1.11.527         reg : esmi_s7_crc17         0x0000000         0xA021141C         459           1.11.528         reg : esmi_rd_cnt17         0x0000000         0xA0211420         459           1.11.529         reg : esmi_dc_crc17         0x00000000         0xA0211424         459           1.11.530         reg : esmi_da_cnt17         0x00000000         0xA0211428         459           1.11.531         reg : esmi_dc_cnt17         0x00000000         0xA021142C         459           1.11.532         reg : esmi_tcmd_cnt17         0x00000000         0xA0211430         460           1.11.533         reg : esmi_tmc_cnt17         0x00000000         0xA0211434         460           1.11.534         reg : esmi_dm_cnt17         0x00000000         0xA0211438         460           1.11.535         reg : esmi_s0_cnt18         0x00000000         0xA0211440         460           1.11.536         reg : esmi_s1_cnt18         0x00000000         0xA0211444         460           1.11.537         reg : esmi_s1_crt18         0x00000000         0xA0211448         460           1.11.539         reg : esmi_s2_cnt18         0x00000000         0xA0211450         460           1.11.540         reg : esmi_s2_cnt18         0x00000000         0xA0211454	1.11.525	reg : esmi_s2_crc17	0x00000000	0xA0211414	459
1.11.528         reg:esmi_rd_crc17         0x00000000         0xA0211420         459           1.11.529         reg:esmi_rd_crc17         0x00000000         0xA0211424         459           1.11.530         reg:esmi_da_cnt17         0x00000000         0xA0211428         459           1.11.531         reg:esmi_ia_cnt17         0x00000000         0xA021142C         459           1.11.532         reg:esmi_tcmd_cnt17         0x00000000         0xA0211430         460           1.11.533         reg:esmi_tmcmd_cnt17         0x00000000         0xA0211434         460           1.11.534         reg:esmi_dm_cnt17         0x00000000         0xA0211434         460           1.11.535         reg:esmi_s0_cnt18         0x00000000         0xA0211440         460           1.11.536         reg:esmi_s0_crt18         0x00000000         0xA0211444         460           1.11.537         reg:esmi_s1_crt18         0x00000000         0xA0211448         460           1.11.538         reg:esmi_s2_crt18         0x00000000         0xA0211440         460           1.11.539         reg:esmi_s2_crt18         0x00000000         0xA0211450         461           1.11.540         reg:esmi_s2_crt18         0x00000000         0xA0211454         461 <td>1.11.526</td> <td>reg : esmi_s7_cnt17</td> <td>0x00000000</td> <td>0xA0211418</td> <td>459</td>	1.11.526	reg : esmi_s7_cnt17	0x00000000	0xA0211418	459
1.11.528         reg:esmi_rd_crc17         0x00000000         0xA0211420         459           1.11.529         reg:esmi_rd_crc17         0x00000000         0xA0211424         459           1.11.530         reg:esmi_da_cnt17         0x00000000         0xA0211428         459           1.11.531         reg:esmi_ia_cnt17         0x00000000         0xA021142C         459           1.11.532         reg:esmi_tcmd_cnt17         0x00000000         0xA0211430         460           1.11.533         reg:esmi_tmcmd_cnt17         0x00000000         0xA0211434         460           1.11.534         reg:esmi_dm_cnt17         0x00000000         0xA0211434         460           1.11.535         reg:esmi_s0_cnt18         0x00000000         0xA0211440         460           1.11.536         reg:esmi_s0_crt18         0x00000000         0xA0211444         460           1.11.537         reg:esmi_s1_crt18         0x00000000         0xA0211448         460           1.11.538         reg:esmi_s2_crt18         0x00000000         0xA0211440         460           1.11.539         reg:esmi_s2_crt18         0x00000000         0xA0211450         461           1.11.540         reg:esmi_s2_crt18         0x00000000         0xA0211454         461 <td>1.11.527</td> <td>reg : esmi_s7_crc17</td> <td>0x00000000</td> <td>0xA021141C</td> <td>459</td>	1.11.527	reg : esmi_s7_crc17	0x00000000	0xA021141C	459
1.11.530       reg:esmi_da_cnt17       0x00000000       0xA0211428       459         1.11.531       reg:esmi_la_cnt17       0x00000000       0xA021142C       459         1.11.532       reg:esmi_tcmd_cnt17       0x00000000       0xA0211430       460         1.11.533       reg:esmi_twcmd_cnt17       0x00000000       0xA0211434       460         1.11.534       reg:esmi_dm_cnt17       0x00000000       0xA0211438       460         1.11.535       reg:esmi_s0_cnt18       0x00000000       0xA0211440       460         1.11.536       reg:esmi_s0_crc18       0x00000000       0xA0211444       460         1.11.537       reg:esmi_s1_cnt18       0x00000000       0xA0211444       460         1.11.538       reg:esmi_s1_crc18       0x00000000       0xA021144C       460         1.11.539       reg:esmi_s2_cnt18       0x00000000       0xA0211450       460         1.11.540       reg:esmi_s7_cnt18       0x00000000       0xA0211454       461         1.11.542       reg:esmi_s7_crt18       0x00000000       0xA0211456       461         1.11.543       reg:esmi_d-crt18       0x00000000       0xA0211460       461         1.11.544       reg:esmi_d-crt18       0x00000000       0xA0211466	1.11.528		0x00000000	0xA0211420	459
1.11.531         reg : esmi_ia_cnt17         0x00000000         0xA021142C         459           1.11.532         reg : esmi_tcmd_cnt17         0x00000000         0xA0211430         460           1.11.533         reg : esmi_twcmd_cnt17         0x00000000         0xA0211434         460           1.11.534         reg : esmi_dm_cnt17         0x00000000         0xA0211438         460           1.11.535         reg : esmi_s0_cnt18         0x00000000         0xA0211440         460           1.11.536         reg : esmi_s0_crc18         0x00000000         0xA0211444         460           1.11.537         reg : esmi_s1_cnt18         0x00000000         0xA0211448         460           1.11.538         reg : esmi_s1_crc18         0x00000000         0xA021144C         460           1.11.539         reg : esmi_s2_crt18         0x00000000         0xA0211450         460           1.11.540         reg : esmi_s7_cnt18         0x00000000         0xA0211454         461           1.11.541         reg : esmi_s7_crt18         0x00000000         0xA021145C         461           1.11.543         reg : esmi_rd_cnt18         0x00000000         0xA0211460         461           1.11.544         reg : esmi_rd_crt18         0x00000000         0xA021146C	1.11.529	reg : esmi_rd_crc17	0x00000000	0xA0211424	459
1.11.532       reg : esmi_tcmd_cnt17       0x00000000       0xA0211430       460         1.11.533       reg : esmi_twcmd_cnt17       0x00000000       0xA0211434       460         1.11.534       reg : esmi_dm_cnt17       0x00000000       0xA0211438       460         1.11.535       reg : esmi_s0_cnt18       0x00000000       0xA0211440       460         1.11.536       reg : esmi_s0_crc18       0x00000000       0xA0211444       460         1.11.537       reg : esmi_s1_cnt18       0x00000000       0xA0211448       460         1.11.538       reg : esmi_s1_crc18       0x00000000       0xA021144C       460         1.11.539       reg : esmi_s2_cnt18       0x00000000       0xA0211450       460         1.11.540       reg : esmi_s2_crc18       0x00000000       0xA0211454       461         1.11.541       reg : esmi_s7_cnt18       0x00000000       0xA0211450       461         1.11.542       reg : esmi_s7_crc18       0x00000000       0xA0211450       461         1.11.543       reg : esmi_d_cnt18       0x00000000       0xA0211460       461         1.11.544       reg : esmi_d_a_cnt18       0x00000000       0xA0211464       461         1.11.5456       reg : esmi_d_a_cnt18       0x00000000 </td <td>1.11.530</td> <td>reg : esmi_da_cnt17</td> <td>0x00000000</td> <td>0xA0211428</td> <td>459</td>	1.11.530	reg : esmi_da_cnt17	0x00000000	0xA0211428	459
1.11.532       reg : esmi_tcmd_cnt17       0x00000000       0xA0211430       460         1.11.533       reg : esmi_twcmd_cnt17       0x00000000       0xA0211434       460         1.11.534       reg : esmi_dm_cnt17       0x00000000       0xA0211438       460         1.11.535       reg : esmi_s0_cnt18       0x00000000       0xA0211440       460         1.11.536       reg : esmi_s0_crc18       0x00000000       0xA0211444       460         1.11.537       reg : esmi_s1_cnt18       0x00000000       0xA0211448       460         1.11.538       reg : esmi_s1_crc18       0x00000000       0xA021144C       460         1.11.539       reg : esmi_s2_cnt18       0x00000000       0xA0211450       460         1.11.540       reg : esmi_s2_crc18       0x00000000       0xA0211454       461         1.11.541       reg : esmi_s7_cnt18       0x00000000       0xA0211450       461         1.11.542       reg : esmi_s7_crc18       0x00000000       0xA0211450       461         1.11.543       reg : esmi_d_cnt18       0x00000000       0xA0211460       461         1.11.544       reg : esmi_d_a_cnt18       0x00000000       0xA0211464       461         1.11.5456       reg : esmi_d_a_cnt18       0x00000000 </td <td></td> <td></td> <td></td> <td></td> <td></td>					
1.11.533       reg : esmi_twcmd_cnt17       0x00000000       0xA0211434       460         1.11.534       reg : esmi_dm_cnt17       0x00000000       0xA0211438       460         1.11.535       reg : esmi_s0_cnt18       0x00000000       0xA0211440       460         1.11.536       reg : esmi_s0_crc18       0x00000000       0xA0211444       460         1.11.537       reg : esmi_s1_cnt18       0x00000000       0xA021144C       460         1.11.538       reg : esmi_s1_crc18       0x00000000       0xA021144C       460         1.11.539       reg : esmi_s2_cnt18       0x00000000       0xA0211450       460         1.11.540       reg : esmi_s2_crc18       0x00000000       0xA0211454       461         1.11.541       reg : esmi_s7_cnt18       0x00000000       0xA0211458       461         1.11.542       reg : esmi_s7_crc18       0x00000000       0xA021145C       461         1.11.543       reg : esmi_rd_cnt18       0x00000000       0xA0211460       461         1.11.544       reg : esmi_da_cnt18       0x00000000       0xA0211460       461         1.11.545       reg : esmi_da_cnt18       0x00000000       0xA021146C       461         1.11.546       reg : esmi_tcmd_cnt18       0x00000000 <td></td> <td></td> <td></td> <td></td> <td></td>					
1.11.534         reg:esmi_dm_cnt17         0x00000000         0xA0211438         460           1.11.535         reg:esmi_s0_cnt18         0x00000000         0xA0211440         460           1.11.536         reg:esmi_s0_crc18         0x00000000         0xA0211444         460           1.11.537         reg:esmi_s1_cnt18         0x00000000         0xA0211448         460           1.11.538         reg:esmi_s1_crc18         0x00000000         0xA021144C         460           1.11.539         reg:esmi_s2_cnt18         0x00000000         0xA0211450         460           1.11.540         reg:esmi_s2_crc18         0x00000000         0xA0211454         461           1.11.541         reg:esmi_s7_cnt18         0x00000000         0xA0211458         461           1.11.542         reg:esmi_s7_crc18         0x00000000         0xA021145C         461           1.11.543         reg:esmi_rd_cnt18         0x00000000         0xA0211460         461           1.11.544         reg:esmi_da_cnt18         0x00000000         0xA0211464         461           1.11.545         reg:esmi_ja_cnt18         0x00000000         0xA021146C         461           1.11.547         reg:esmi_tcmd_cnt18         0x00000000         0xA0211470         462					
1.11.535         reg:esmi_s0_crc18         0x00000000         0xA0211440         460           1.11.536         reg:esmi_s0_crc18         0x00000000         0xA0211444         460           1.11.537         reg:esmi_s1_crt18         0x00000000         0xA0211448         460           1.11.538         reg:esmi_s1_crc18         0x00000000         0xA021144C         460           1.11.539         reg:esmi_s2_crt18         0x00000000         0xA0211450         460           1.11.540         reg:esmi_s2_crc18         0x00000000         0xA0211454         461           1.11.541         reg:esmi_s7_crt18         0x00000000         0xA0211458         461           1.11.542         reg:esmi_s7_crc18         0x00000000         0xA021145C         461           1.11.543         reg:esmi_rd_crt18         0x00000000         0xA0211460         461           1.11.544         reg:esmi_rd_crt18         0x00000000         0xA0211468         461           1.11.545         reg:esmi_da_crt18         0x00000000         0xA021146C         461           1.11.546         reg:esmi_tcmd_crt18         0x00000000         0xA0211470         462           1.11.548         reg:esmi_dm_crt18         0x00000000         0xA0211478         462					
1.11.536         reg:esmi_s0_crc18         0x00000000         0xA0211444         460           1.11.537         reg:esmi_s1_cnt18         0x00000000         0xA0211448         460           1.11.538         reg:esmi_s1_crc18         0x00000000         0xA021144C         460           1.11.539         reg:esmi_s2_cnt18         0x00000000         0xA0211450         461           1.11.540         reg:esmi_s2_crc18         0x00000000         0xA0211454         461           1.11.541         reg:esmi_s7_cnt18         0x00000000         0xA0211458         461           1.11.542         reg:esmi_s7_crc18         0x00000000         0xA021145C         461           1.11.543         reg:esmi_rd_cnt18         0x00000000         0xA0211460         461           1.11.544         reg:esmi_rd_crc18         0x00000000         0xA0211464         461           1.11.545         reg:esmi_da_cnt18         0x00000000         0xA0211468         461           1.11.546         reg:esmi_ia_cnt18         0x00000000         0xA0211470         462           1.11.548         reg:esmi_twcmd_cnt18         0x00000000         0xA0211474         462           1.11.549         reg:esmi_dm_cnt18         0x00000000         0xA0211470         462			0x00000000		
1.11.537       reg: esmi_s1_cnt18       0x00000000       0xA0211448       460         1.11.538       reg: esmi_s1_crc18       0x00000000       0xA021144C       460         1.11.539       reg: esmi_s2_cnt18       0x00000000       0xA0211450       460         1.11.540       reg: esmi_s2_crc18       0x00000000       0xA0211454       461         1.11.541       reg: esmi_s7_cnt18       0x00000000       0xA0211458       461         1.11.542       reg: esmi_s7_crc18       0x00000000       0xA021145C       461         1.11.543       reg: esmi_rd_cnt18       0x00000000       0xA0211460       461         1.11.544       reg: esmi_d_cnt18       0x00000000       0xA0211464       461         1.11.545       reg: esmi_da_cnt18       0x00000000       0xA021146C       461         1.11.547       reg: esmi_tcmd_cnt18       0x00000000       0xA0211470       462         1.11.548       reg: esmi_twcmd_cnt18       0x00000000       0xA0211478       462         1.11.549       reg: esmi_d_cnt18       0x00000000       0xA0211478       462         1.11.550       reg: esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.538         reg: esmi_s1_crc18         0x00000000         0xA021144C         460           1.11.539         reg: esmi_s2_cnt18         0x00000000         0xA0211450         460           1.11.540         reg: esmi_s2_crc18         0x00000000         0xA0211454         461           1.11.541         reg: esmi_s7_cnt18         0x00000000         0xA0211458         461           1.11.542         reg: esmi_s7_crc18         0x00000000         0xA021145C         461           1.11.543         reg: esmi_rd_cnt18         0x00000000         0xA0211460         461           1.11.544         reg: esmi_rd_crc18         0x00000000         0xA0211464         461           1.11.545         reg: esmi_da_cnt18         0x00000000         0xA0211468         461           1.11.546         reg: esmi_ia_cnt18         0x00000000         0xA0211470         462           1.11.548         reg: esmi_twcmd_cnt18         0x00000000         0xA0211474         462           1.11.549         reg: esmi_dm_cnt18         0x00000000         0xA0211478         462           1.11.550         reg: esmi_s0_cnt19         0x00000000         0xA0211480         462					
1.11.539         reg: esmi_s2_cnt18         0x00000000         0xA0211450         460           1.11.540         reg: esmi_s2_crc18         0x00000000         0xA0211454         461           1.11.541         reg: esmi_s7_cnt18         0x00000000         0xA0211458         461           1.11.542         reg: esmi_s7_crc18         0x00000000         0xA021145C         461           1.11.543         reg: esmi_rd_cnt18         0x00000000         0xA0211460         461           1.11.544         reg: esmi_rd_crc18         0x00000000         0xA0211464         461           1.11.545         reg: esmi_da_cnt18         0x00000000         0xA0211468         461           1.11.546         reg: esmi_ia_cnt18         0x00000000         0xA0211470         462           1.11.548         reg: esmi_twcmd_cnt18         0x00000000         0xA0211474         462           1.11.549         reg: esmi_dm_cnt18         0x00000000         0xA0211478         462           1.11.550         reg: esmi_s0_cnt19         0x00000000         0xA0211480         462					
1.11.540         reg: esmi_s2_crc18         0x00000000         0xA0211454         461           1.11.541         reg: esmi_s7_cnt18         0x00000000         0xA0211458         461           1.11.542         reg: esmi_s7_crc18         0x00000000         0xA021145C         461           1.11.543         reg: esmi_rd_cnt18         0x00000000         0xA0211460         461           1.11.544         reg: esmi_rd_crc18         0x00000000         0xA0211464         461           1.11.545         reg: esmi_da_cnt18         0x00000000         0xA0211468         461           1.11.546         reg: esmi_ia_cnt18         0x00000000         0xA0211470         462           1.11.547         reg: esmi_tcmd_cnt18         0x00000000         0xA0211474         462           1.11.548         reg: esmi_twcmd_cnt18         0x00000000         0xA0211474         462           1.11.549         reg: esmi_dm_cnt18         0x00000000         0xA0211478         462           1.11.550         reg: esmi_s0_cnt19         0x00000000         0xA0211480         462					
1.11.541       reg:esmi_s7_cnt18       0x00000000       0xA0211458       461         1.11.542       reg:esmi_s7_crc18       0x00000000       0xA021145C       461         1.11.543       reg:esmi_rd_cnt18       0x00000000       0xA0211460       461         1.11.544       reg:esmi_rd_crc18       0x00000000       0xA0211464       461         1.11.545       reg:esmi_da_cnt18       0x00000000       0xA0211468       461         1.11.546       reg:esmi_ia_cnt18       0x00000000       0xA021146C       461         1.11.547       reg:esmi_tcmd_cnt18       0x00000000       0xA0211470       462         1.11.548       reg:esmi_twcmd_cnt18       0x00000000       0xA0211474       462         1.11.549       reg:esmi_dm_cnt18       0x00000000       0xA0211478       462         1.11.550       reg:esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.542       reg: esmi_s7_crc18       0x00000000       0xA021145C       461         1.11.543       reg: esmi_rd_cnt18       0x00000000       0xA0211460       461         1.11.544       reg: esmi_rd_crc18       0x00000000       0xA0211464       461         1.11.545       reg: esmi_da_cnt18       0x00000000       0xA0211468       461         1.11.546       reg: esmi_ia_cnt18       0x00000000       0xA021146C       461         1.11.547       reg: esmi_tcmd_cnt18       0x00000000       0xA0211470       462         1.11.548       reg: esmi_twcmd_cnt18       0x00000000       0xA0211474       462         1.11.549       reg: esmi_dm_cnt18       0x00000000       0xA0211478       462         1.11.550       reg: esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.543         reg : esmi_rd_cnt18         0x00000000         0xA0211460         461           1.11.544         reg : esmi_rd_crc18         0x00000000         0xA0211464         461           1.11.545         reg : esmi_da_cnt18         0x00000000         0xA0211468         461           1.11.546         reg : esmi_ia_cnt18         0x00000000         0xA021146C         461           1.11.547         reg : esmi_tcmd_cnt18         0x00000000         0xA0211470         462           1.11.548         reg : esmi_twcmd_cnt18         0x00000000         0xA0211474         462           1.11.549         reg : esmi_dm_cnt18         0x00000000         0xA0211478         462           1.11.550         reg : esmi_s0_cnt19         0x00000000         0xA0211480         462					
1.11.544       reg: esmi_rd_crc18       0x00000000       0xA0211464       461         1.11.545       reg: esmi_da_cnt18       0x00000000       0xA0211468       461         1.11.546       reg: esmi_ia_cnt18       0x00000000       0xA021146C       461         1.11.547       reg: esmi_tcmd_cnt18       0x00000000       0xA0211470       462         1.11.548       reg: esmi_twcmd_cnt18       0x00000000       0xA0211474       462         1.11.549       reg: esmi_dm_cnt18       0x00000000       0xA0211478       462         1.11.550       reg: esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.545       reg : esmi_da_cnt18       0x00000000       0xA0211468       461         1.11.546       reg : esmi_ia_cnt18       0x00000000       0xA021146C       461         1.11.547       reg : esmi_tcmd_cnt18       0x00000000       0xA0211470       462         1.11.548       reg : esmi_twcmd_cnt18       0x00000000       0xA0211474       462         1.11.549       reg : esmi_dm_cnt18       0x00000000       0xA0211478       462         1.11.550       reg : esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.546       reg : esmi_ia_cnt18       0x00000000       0xA021146C       461         1.11.547       reg : esmi_tcmd_cnt18       0x00000000       0xA0211470       462         1.11.548       reg : esmi_twcmd_cnt18       0x00000000       0xA0211474       462         1.11.549       reg : esmi_dm_cnt18       0x00000000       0xA0211478       462         1.11.550       reg : esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.547     reg : esmi_tcmd_cnt18     0x00000000     0xA0211470     462       1.11.548     reg : esmi_twcmd_cnt18     0x00000000     0xA0211474     462       1.11.549     reg : esmi_dm_cnt18     0x00000000     0xA0211478     462       1.11.550     reg : esmi_s0_cnt19     0x00000000     0xA0211480     462					
1.11.548       reg : esmi_twcmd_cnt18       0x00000000       0xA0211474       462         1.11.549       reg : esmi_dm_cnt18       0x00000000       0xA0211478       462         1.11.550       reg : esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.549       reg : esmi_dm_cnt18       0x00000000       0xA0211478       462         1.11.550       reg : esmi_s0_cnt19       0x00000000       0xA0211480       462					
1.11.550 reg: esmi_s0_cnt19 0x00000000 0xA0211480 462					
<b>U</b> = = =					
11.11.001   ICU . COIII OU DIVIZ   UXUUUUUUU UXAUZ 11404   467	1.11.551	reg : esmi_s0_crc19	0x00000000		462
1.11.552 reg: esmi_s1_cnt19					
1.11.553 reg : esmi_s1_crc19 0x0000000 0xA021148C 462					

1.11.554	reg : esmi_s2_cnt19	0x00000000	0xA0211490	462
1.11.555	reg : esmi_s2_crc19	0x00000000	0xA0211494	463
1.11.556	reg : esmi_s7_cnt19	0x00000000	0xA0211498	463
1.11.557	reg : esmi_s7_crc19	0x00000000		463
1.11.558	reg : esmi rd cnt19	0x00000000		463
1.11.559	reg : esmi_rd_crc19	0x00000000		463
1.11.560	reg : esmi_da_cnt19	0x00000000		463
1.11.561	reg : esmi_ia_cnt19	0x00000000		463
1.11.562	reg : esmi_tcmd_cnt19	0x00000000		463
1.11.563	reg : esmi_twcmd_cnt19	0x00000000		464
1.11.564	reg : esmi_dm_cnt19	0x00000000		464
1.11.565	reg : esmi_s0_cnt20	0x00000000	0xA02114C0	464
1.11.566	reg : esmi_s0_crc20	0x00000000		464
1.11.567	reg : esmi_s1_cnt20	0x00000000	0xA02114C8	464
1.11.568	reg : esmi_s1_crc20	0x00000000	0xA02114CC	464
1.11.569	reg : esmi_s2_cnt20	0x00000000	0xA02114D0	464
1.11.570	reg : esmi_s2_crc20	0x00000000	0xA02114D4	465
1.11.571	reg : esmi_s7_cnt20	0x00000000		465
1.11.572	reg : esmi_s7_crc20	0x00000000		465
1.11.573	reg : esmi_rd_cnt20		0xA02114E0	465
1.11.574	reg : esmi_rd_crc20	0x00000000		465
1.11.575	reg : esmi_da_cnt20	0x00000000		465
1.11.576	reg : esmi_ia_cnt20	0x00000000	0xA02114EC	465
1.11.577	reg : esmi_tcmd_cnt20	0x00000000		465
1.11.578	reg : esmi_twcmd_cnt20	0x00000000		466
1.11.579	reg : esmi_dm_cnt20	0x00000000		466
1.11.580	reg : esmi_tref_int1	0x00000000		466
1.11.581	reg : esmi_tref_freq1	0x00000824	0xA0211504	466
1.11.582	reg : esmi_clk_type1	0x00000000	0xA0211508	466
1.11.583	reg : esmi_tref_int2	0x00000000		467
1.11.584	reg : esmi_tref_freq2	0x00000824		467
1.11.585	reg : esmi_clk_type2	0x00000000		467
1.11.586	reg : esmi_tref_int3	0x00000000		467
1.11.587	reg : esmi_tref_freq3	0x000000000000000000000000000000000000		467
1.11.588	reg : esmi_clk_type3	0x000000024		467
1.11.589	reg : esmi_tref_int4	0x00000000		468
1.11.590	reg : esmi_tref_freq4	0x00000824		468
1.11.591	reg : esmi_clk_type4	0x00000000		468
1.11.592	reg : esmi_tref_int5		0xA0211530	469
1.11.593	reg : esmi_tref_freq5	0x00000824	0xA0211534	469
1.11.594	reg : esmi_clk_type5	0x00000000	0xA0211538	469
1.11.595	reg : esmi_tref_int6	0x00000000	0xA021153C	469
1.11.596	reg : esmi_tref_freq6	0x00000824	0xA0211540	469
1.11.597	reg : esmi_clk_type6	0x00000000	0xA0211544	469
1.11.598	reg : esmi_tref_int7	0x00000000		470
1.11.599	reg : esmi_tref_freq7		0xA021154C	470
1.11.600	reg : esmi_clk_type7	0x00000000		470
1.11.601	reg : esmi_tref_int8	0x00000000		471
1.11.602	reg : esmi_tref_freq8	0x00000000		471
	-			471
1.11.603	reg : esmi_clk_type8	0x00000000		
1.11.604	reg : esmi_tref_int9	0x00000000		471
1.11.605	reg : esmi_tref_freq9	0x00000824		471
1.11.606	reg : esmi_clk_type9	0x00000000		472
1.11.607	reg : esmi_tref_int10		0xA021156C	472
1.11.608	reg : esmi_tref_freq10	0x00000824	0xA0211570	472
1.11.609	reg : esmi_clk_type10	0x00000000	0xA0211574	472
1.11.610	reg : esmi_tref_int11	0x00000000	0xA0211578	473
1.11.611	reg : esmi_tref_freq11	0x00000824		473
1.11.612	reg : esmi_clk_type11		0xA0211580	473
1.11.613	reg : esmi_tref_int12		0xA0211584	473
1.11.614	reg : esmi_tref_freq12	0x000000824		473
1.11.615	reg : esmi_clk_type12	0x000000024		474
	reg : esmi_tref_int13	0x00000000		474
1.11.616				
1.11.617	reg : esmi_tref_freq13	0x00000824		474
1.11.618	reg : esmi_clk_type13	0x00000000		474
1.11.619	reg : esmi_tref_int14	0x00000000	0xA021159C	475

1.11.620	reg : esmi_tref_freq14	0x00000824	0xA02115A0	475
1.11.621	reg : esmi_clk_type14	0x00000000	0xA02115A4	475
1.11.622	reg : esmi_tref_int15	0x00000000	0xA02115A8	475
1.11.623	reg : esmi_tref_freq15	0x00000824		475
1.11.624	reg : esmi_clk_type15	0x00000000		476
1.11.625	reg : esmi_tref_int16	0x00000000		476
1.11.626	reg : esmi_tref_freq16	0x00000824		476
1.11.627	reg : esmi_clk_type16	0x00000000		476
1.11.628	reg : esmi_tref_int17	0x00000000	0xA02115C0	477
1.11.629	reg : esmi_tref_freq17	0x00000824	0xA02115C4	477
1.11.630	reg : esmi_clk_type17	0x00000000	0xA02115C8	477
1.11.631	reg : esmi_tref_int18	0x00000000	0xA02115CC	477
1.11.632	reg : esmi_tref_freq18	0x00000824	0xA02115D0	477
1.11.633	reg : esmi_clk_type18	0x00000000	0xA02115D4	478
1.11.634	reg : esmi_tref_int19	0x00000000	0xA02115D8	478
1.11.635	reg : esmi_tref_freq19	0x00000824	0xA02115DC	478
1.11.636	reg : esmi_clk_type19	0x00000000	0xA02115E0	478
1.11.637	reg : esmi_tref_int20	0x00000000	0xA02115E4	479
1.11.638	reg : esmi_tref_freq20	0x00000824	0xA02115E8	479
1.11.639	reg : esmi_clk_type20	0x00000000	0xA02115EC	479
1.11.640	reg : euv_sim1	0x00000000		479
1.11.641	reg : euv_sim2	0x00000000		480
1.11.642	reg : euv_sim3		0xA02115F8	480
1.11.643	reg : euv_sim4	0x00000000		480
1.11.644	reg : euv_sim5	0x00000000		480
1.11.645	reg : euv_sim6	0x00000000	0xA0211604	480
1.11.646	reg : euv_sim7	0x00000000		480
1.11.647	reg : euv_sim8	0x00000000		480
1.11.648	reg : euv_sim9	0x00000000	0xA0211610	480
1.11.649	reg : euv_sim10	0x00000000	0xA0211614	480
1.11.650	reg : euv_sim11	0x00000000	0xA0211618	481
1.11.651	reg : euv_sim12	0x00000000	0xA021161C	481
1.11.652	reg : euv_sim13	0x00000000	0xA0211620	481
1.11.653	reg : euv_sim14	0x00000000	0xA0211624	481
1.11.654	reg : euv_sim15	0x00000000	0xA0211628	481
1.11.655	reg : euv_sim16	0x00000000	0xA021162C	481
1.11.656	reg : euv_sim17	0x00000000	0xA0211630	481
1.11.657	reg : euv_sim18	0x00000000	0xA0211634	481
1.11.658	reg : euv_sim19	0x00000000		481
1.11.659	reg : euv_sim20		0xA021163C	482
1.11.660	reg : esmi_scratch		0xA0211640	482
1.11.661	reg : esmi_s7_1ms_cnt		0xA0211644	482
1.11.662	reg : esmi_xpam_bw_ovld	0x00000000		482
1.11.663	reg : esmi_xpam_init_err	0x00000000		482
1.11.664	reg : esmi_xlam_cab_disc	0x00000000		482
1.11.665	reg : esmi_adc_clip_cnt1	0x00000000		482
1.11.666	reg : esmi_adc_clip_cnt2	0x00000000		482
1.11.667	reg : esmi_adc_clip_cnt3		0xA0211688	483
1.11.668	reg : esmi_adc_clip_cnt4		0xA021168C	483
1.11.669	reg : esmi_adc_clip_cnt5	0x00000000		483
1.11.670	reg : esmi_adc_clip_cnt6		0xA0211694	483
1.11.671	reg : esmi_adc_clip_cnt7		0xA0211698	483
1.11.672	reg : esmi_adc_clip_cnt8	0x00000000		483
1.11.673	reg : esmi_adc_clip_cnt9	0x00000000		483
1.11.674	reg : esmi_adc_clip_cnt10	0x00000000		483
1.11.675	reg : esmi_adc_clip_cnt11		0xA02116A8	484
1.11.676	reg : esmi_adc_clip_cnt12	0x00000000		484
1.11.677	reg : esmi_adc_clip_cnt13	0x00000000		484
1.11.678	reg : esmi_adc_clip_cnt14	0x00000000		484
1.11.679	reg : esmi_adc_clip_cnt15	0x00000000		484
1.11.680	reg : esmi_adc_clip_cnt16	0x00000000		484
1.11.681	reg : esmi_adc_clip_cnt17	0x00000000		484 484
1.11.682 1.11.683	reg : esmi_adc_clip_cnt18 reg : esmi_adc_clip_cnt19	0x00000000 0x00000000		484
1.11.683	reg : esmi_adc_clip_cnt19 reg : esmi_adc_clip_cnt20		0xA02116C8 0xA02116CC	485
1.11.685	reg : esmi_dat1	0x00000000		485
1.11.000	rog . com_uatr	3700000000	0/// 10// 11/00/0	700

1 11 000		10. 00000000	0.40044004	105
1.11.686	reg : esmi_dat2	0x00000000	0xA02116D4	485
1.11.687	reg : esmi_dat3	0x00000000	0xA02116D8	485
1.11.688	reg : esmi_dat4	0x00000000		486
1.11.689	reg : esmi_dat5	0x00000000		486
1.11.690	reg : esmi_dat6	0x00000000		487
1.11.691	reg : esmi_dat7	0x00000000		487
1.11.692	reg : esmi_dat8	0x00000000	0xA02116EC	487
1.11.693	reg : esmi_dat9	0x00000000	0xA02116F0	488
1.11.694	reg : esmi_dat10	0x00000000	0xA02116F4	488
1.11.695	reg : esmi_dat11	0x00000000	0xA02116F8	488
1.11.696	reg : esmi_dat12	0x00000000	0xA02116FC	489
1.11.697	reg : esmi_dat13	0x00000000		489
1.11.698	reg : esmi_dat14		0xA0211704	490
1.11.699	reg : esmi_dat15		0xA0211708	490
1.11.700	reg : esmi_dat16	0x00000000		490
1.11.701	reg : esmi_dat17	0x00000000	0xA0211710	491
1.11.702	reg : esmi_dat17	0x00000000		491
1.11.702	reg : esmi_dat19	0x00000000	0xA0211718	492
1.11.703	reg : esmi_dat20	0x00000000	0xA0211716 0xA021171C	492
1.11.704	block : mcdma_feed_registers	000000000	0xA0240000 - 0xA0240F73	492
1.12			0XA0240000 - 0XA0240F73	492
1 12 1	_srdl	0x77607705	0×40240000	492
1.12.1	reg:	0x77687765	0xA0240000	492
1.10.0	mcdma_feed_module_name	0.05040004	0.40040004	400
1.12.2	reg:	0x05210301	0xA0240004	493
	mcdma_feed_module_vers			
	ion			100
1.12.3	reg:	0x80000101	0xA0240008	493
	mcdma_feed_page_proper			
	ties			
1.12.4	reg : mcdma_feed_scratchregi	0x12345678	0xA024000C	493
	ster			
1.12.5	reg : mcdma_feed_irq_enable	0x00000000		493
1.12.6	reg:	0x00000000	0xA0240014	493
	mcdma_feed_irq_pending			
1.12.7	reg : mcdma_feed_irq_raw	0x00000000	0xA0240018	493
1.12.8	reg : mcdma_feed_irq_force	0x00000000		493
1.12.9	reg : streamtpg_en_ctrl		0xA0240020	494
1.12.10	reg : streamsx16_err_stat	0x00000000	0xA0240024	494
1.12.11	reg : tpg0_packet_rate_clks_	0x00000823	0xA0240034	494
	ctrl			
1.12.12	reg: tpg0_packet_size_clks_	0x00000040	0xA0240038	495
	ctrl			
1.12.13	reg: stream0_expsize_dis_ct	0x0000004D	0xA024003C	495
	rl			
1.12.14	reg : stream0_exprate_dis_ct	0x007F0040	0xA0240040	495
	rl			
1.12.15	reg : stream0_err_stat	0x00000000	0xA0240044	495
1.12.16	reg : stream0_err_expsize_cn	0x00000000	0xA0240048	495
	tr_stat			
1.12.17	reg : stream0_err_pfifofull_	0x00000000	0xA024004C	496
	cntr_stat			
1.12.18	reg:stream0_err_bfifofull_	0x00000000	0xA0240050	496
	cntr_stat			
1.12.19	reg : stream0_err_maxsize_cn	0x00000000	0xA0240054	496
	tr_stat			
1.12.20	reg : stream0_err_minsize_cn	0x00000000	0xA0240058	496
	tr_stat			
1.12.21	reg : stream0_err_notlast_cn	0x00000000	0xA024005C	496
	tr_stat		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
1.12.22	reg : stream0_err_minipg_cnt	0x00000000	0xA0240060	496
	r_stat	CACCOCCOCC	J. 1.32 10000	100
1.12.23	reg : stream0_err_watchdog_c	0x00000000	0xA0240064	496
	ntr_stat	CACCOCCOCC	0.0.102 1000 1	100
1.12.24	reg : stream0_exc_exprate_cn	0x0000000	0xA0240068	497
	10g . oliodino_oxo_oxpiate_cii	CAUGUUUU	0.0 10 TO	107
	tr stat			
	tr_stat	0x00000000	0xA024006C	497
1.12.25	tr_stat reg : stream0_exc_expratedev iate_cntr_stat	0x00000000	0xA024006C	497

1.12.26	reg : stream0_rate_measured_ stat	0x00000000	0xA0240070	497
1.12.27	reg : tpg1_packet_rate_clks_ ctrl	0x00000823	0xA0240134	497
1.12.28	reg : tpg1_packet_size_clks_ ctrl	0x00000040	0xA0240138	497
1.12.29	reg : stream1_expsize_dis_ct	0x0000002C	0xA024013C	497
1.12.30	reg : stream1_exprate_dis_ct	0x007F0040	0xA0240140	498
1.12.31	reg : stream1_err_stat	0x00000000	0xA0240144	498
1.12.32	reg : stream1_err_expsize_cn tr_stat	0x00000000	0xA0240148	498
1.12.33	reg : stream1_err_pfifofull_ cntr_stat	0x00000000	0xA024014C	498
1.12.34	reg : stream1_err_bfifofull_ cntr_stat	0x00000000	0xA0240150	498
1.12.35		0x00000000	0xA0240154	498
1.12.36	reg: stream1_err_minsize_cn tr_stat	0x00000000	0xA0240158	499
1.12.37	reg : stream1_err_notlast_cn tr_stat	0x00000000	0xA024015C	499
1.12.38	reg : stream1_err_minipg_cnt r_stat	0x00000000	0xA0240160	499
1.12.39	reg : stream1_err_watchdog_c ntr_stat	0x00000000	0xA0240164	499
1.12.40	reg : stream1_exc_exprate_cn tr_stat	0x00000000	0xA0240168	499
1.12.41	reg : stream1_exc_expratedev iate_cntr_stat	0x00000000	0xA024016C	499
1.12.42	reg : stream1_rate_measured_ stat	0x00000000	0xA0240170	500
1.12.43	reg : tpg2_packet_rate_clks_ ctrl	0x00000823	0xA0240234	500
1.12.44	reg : tpg2_packet_size_clks_ ctrl	0x00000040	0xA0240238	500
1.12.45		0x00000013	0xA024023C	500
1.12.46	reg : stream2_exprate_dis_ct	0x007F0040	0xA0240240	500
1.12.47	reg : stream2_err_stat	0x00000000	0xA0240244	500
1.12.48	reg : stream2_err_expsize_cn tr_stat	0x00000000	0xA0240248	501
1.12.49	reg : stream2_err_pfifofull_ cntr_stat	0x00000000	0xA024024C	501
1.12.50	reg : stream2_err_bfifofull_ cntr_stat	0x00000000	0xA0240250	501
1.12.51	reg : stream2_err_maxsize_cn tr_stat	0x00000000	0xA0240254	501
1.12.52	reg : stream2_err_minsize_cn tr_stat	0x00000000	0xA0240258	501
1.12.53	reg : stream2_err_notlast_cn tr_stat	0x00000000	0xA024025C	501
1.12.54	reg : stream2_err_minipg_cnt r_stat	0x00000000	0xA0240260	502
1.12.55	reg : stream2_err_watchdog_c ntr_stat	0x00000000	0xA0240264	502
1.12.56	reg : stream2_exc_exprate_cn tr_stat	0x00000000	0xA0240268	502
1.12.57	reg : stream2_exc_expratedev iate_cntr_stat	0x00000000	0xA024026C	502
1.12.58	reg : stream2_rate_measured_ stat	0x00000000	0xA0240270	502
1.12.59	reg : tpg3_packet_rate_clks_ ctrl	0x00000823	0xA0240334	502
1.12.60	reg : tpg3_packet_size_clks_ ctrl	0x00000040	0xA0240338	502

1.12.61	reg : stream3_expsize_dis_ct	0x000000D	0xA024033C	503
1.12.62	rl reg : stream3_exprate_dis_ct rl	0x007F0040	0xA0240340	503
1.12.63	reg : stream3_err_stat	0x00000000	0xA0240344	503
1.12.64	reg : stream3_err_expsize_cn	0x00000000	0xA0240348	503
1.12.65	tr_stat reg : stream3_err_pfifofull_	0x00000000	0xA024034C	504
1.12.66	cntr_stat reg : stream3_err_bfifofull_	0x00000000	0xA0240350	504
1.12.67	cntr_stat	0x00000000		
	reg : stream3_err_maxsize_cn tr_stat		0xA0240354	504
1.12.68	reg : stream3_err_minsize_cn tr_stat	0x00000000	0xA0240358	504
1.12.69	reg : stream3_err_notlast_cn tr_stat	0x00000000	0xA024035C	504
1.12.70	reg : stream3_err_minipg_cnt r_stat	0x00000000	0xA0240360	504
1.12.71		0x00000000	0xA0240364	504
1.12.72	reg : stream3_exc_exprate_cn tr_stat	0x00000000	0xA0240368	504
1.12.73	reg : stream3_exc_expratedev	0x00000000	0xA024036C	505
1.12.74	iate_cntr_stat reg : stream3_rate_measured_	0x00000000	0xA0240370	505
1.12.75	stat reg : tpg4_packet_rate_clks_	0x00000823	0xA0240434	505
1.12.76	ctrl reg:tpg4_packet_size_clks_	0x00000040	0xA0240438	505
1.12.77	ctrl reg : stream4_expsize_dis_ct	0x0000000C	0xA024043C	505
	rl			
1.12.78	reg : stream4_exprate_dis_ct	0x007F0040	0xA0240440	505
1.12.79	reg : stream4_err_stat	0x00000000	0xA0240444	506
1.12.80	reg : stream4_err_expsize_cn tr_stat	0x00000000	0xA0240448	506
1.12.81	reg : stream4_err_pfifofull_ cntr_stat	0x00000000	0xA024044C	506
1.12.82	reg : stream4_err_bfifofull_ cntr_stat	0x00000000	0xA0240450	506
1.12.83	reg : stream4_err_maxsize_cn tr stat	0x00000000	0xA0240454	506
1.12.84	reg : stream4_err_minsize_cn tr_stat	0x00000000	0xA0240458	507
1.12.85	reg : stream4_err_notlast_cn tr_stat	0x00000000	0xA024045C	507
1.12.86	reg : stream4_err_minipg_cnt	0x00000000	0xA0240460	507
1.12.87		0x00000000	0xA0240464	507
1.12.88	ntr_stat reg : stream4_exc_exprate_cn	0x00000000	0xA0240468	507
1.12.89	tr_stat reg : stream4_exc_expratedev	0x00000000	0xA024046C	507
1.12.90	iate_cntr_stat reg : stream4_rate_measured_	0x00000000	0xA0240470	507
1.12.91	stat reg : tpg5_packet_rate_clks_	0x00000823	0xA0240534	508
1.12.92	ctrl reg : tpg5_packet_size_clks_	0x00000040	0xA0240538	508
	ctrl			
1.12.93	reg : stream5_expsize_dis_ct	0x0000007A	0xA024053C	508
1.12.94	reg : stream5_exprate_dis_ct	0x007F0040	0xA0240540	508
1.12.95	reg : stream5_err_stat	0x00000000	0xA0240544	508
1.12.96	reg : stream5_err_expsize_cn	0x00000000	0xA0240548	509

	tr_stat			
1.12.97	reg : stream5_err_pfifofull_ cntr_stat	0x00000000	0xA024054C	509
1.12.98	reg : stream5_err_bfifofull_ cntr_stat	0x00000000	0xA0240550	509
1.12.99	reg : stream5_err_maxsize_cn tr_stat	0x00000000	0xA0240554	509
1.12.100	reg : stream5_err_minsize_cn tr_stat	0x00000000	0xA0240558	509
1.12.101	reg : stream5_err_notlast_cn tr_stat	0x00000000	0xA024055C	509
1.12.102	reg : stream5_err_minipg_cnt r_stat	0x00000000	0xA0240560	509
1.12.103	reg : stream5_err_watchdog_c ntr_stat	0x00000000	0xA0240564	510
1.12.104	reg : stream5_exc_exprate_cn tr_stat	0x00000000	0xA0240568	510
1.12.105	reg : stream5_exc_expratedev iate_cntr_stat	0x00000000	0xA024056C	510
1.12.106	reg : stream5_rate_measured_ stat	0x00000000	0xA0240570	510
1.12.107	reg : tpg6_packet_rate_clks_ ctrl	0x00000823	0xA0240634	510
1.12.108	reg : tpg6_packet_size_clks_ ctrl	0x00000040	0xA0240638	510
1.12.109	reg : stream6_expsize_dis_ct	0x000000BD	0xA024063C	511
1.12.110	reg : stream6_exprate_dis_ct	0x007F0040	0xA0240640	511
1.12.111	reg : stream6_err_stat	0x00000000	0xA0240644	511
1.12.112	reg : stream6_err_expsize_cn tr_stat	0x00000000	0xA0240648	511
1.12.113	reg : stream6_err_pfifofull_ cntr_stat	0x00000000	0xA024064C	511
1.12.114	reg : stream6_err_bfifofull_ cntr_stat	0x00000000	0xA0240650	512
1.12.115		0x00000000	0xA0240654	512
1.12.116	reg : stream6_err_minsize_cn tr_stat	0x00000000	0xA0240658	512
1.12.117	reg : stream6_err_notlast_cn tr stat	0x00000000	0xA024065C	512
1.12.118	reg : stream6_err_minipg_cnt r stat	0x00000000	0xA0240660	512
1.12.119		0x00000000	0xA0240664	512
1.12.120	reg : stream6_exc_exprate_cn tr_stat	0x00000000	0xA0240668	512
1.12.121	reg : stream6_exc_expratedev iate_cntr_stat	0x00000000	0xA024066C	513
1.12.122	reg : stream6_rate_measured_ stat	0x00000000	0xA0240670	513
1.12.123	reg : tpg7_packet_rate_clks_ ctrl	0x00000823	0xA0240734	513
1.12.124	reg : tpg7_packet_size_clks_ ctrl	0x00000040	0xA0240738	513
1.12.125	reg : stream7_expsize_dis_ct	0x0000001D	0xA024073C	513
1.12.126	reg : stream7_exprate_dis_ct	0x007F0040	0xA0240740	513
1.12.127	reg : stream7_err_stat	0x00000000	0xA0240744	514
1.12.128	reg : stream7_err_expsize_cn tr_stat	0x00000000	0xA0240748	514
1.12.129	reg : stream7_err_pfifofull_ cntr_stat	0x00000000	0xA024074C	514
1.12.130	reg : stream7_err_bfifofull_ cntr_stat	0x00000000	0xA0240750	514
1.12.131	reg : stream7_err_maxsize_cn	0x00000000	0xA0240754	514

	tr_stat		I	
1.12.132	reg : stream7_err_minsize_cn tr_stat	0x00000000	0xA0240758	514
1.12.133	reg : stream7_err_notlast_cn tr_stat	0x00000000	0xA024075C	515
1.12.134	reg : stream7_err_minipg_cnt r_stat	0x00000000	0xA0240760	515
1.12.135	reg : stream7_err_watchdog_c ntr_stat	0x00000000	0xA0240764	515
1.12.136	reg : stream7_exc_exprate_cn tr_stat	0x00000000	0xA0240768	515
1.12.137	reg : stream7_exc_expratedev iate_cntr_stat	0x00000000	0xA024076C	515
1.12.138	reg : stream7_rate_measured_ stat	0x00000000	0xA0240770	515
1.12.139	reg : tpg8_packet_rate_clks_ ctrl	0x00000823	0xA0240834	516
1.12.140	reg : tpg8_packet_size_clks_ ctrl	0x00000040	0xA0240838	516
1.12.141	reg : stream8_expsize_dis_ct rl	0x00000110	0xA024083C	516
1.12.142	reg : stream8_exprate_dis_ct	0x007F0040	0xA0240840	516
1.12.143	reg : stream8_err_stat	0x00000000	0xA0240844	516
1.12.144	reg : stream8_err_expsize_cn tr_stat	0x00000000	0xA0240848	517
1.12.145	reg : stream8_err_pfifofull_ cntr_stat	0x00000000	0xA024084C	517
1.12.146	reg : stream8_err_bfifofull_ cntr_stat	0x00000000	0xA0240850	517
1.12.147	reg : stream8_err_maxsize_cn tr_stat	0x00000000	0xA0240854	517
1.12.148	reg : stream8_err_minsize_cn tr_stat	0x00000000	0xA0240858	517
1.12.149	reg : stream8_err_notlast_cn tr_stat	0x00000000	0xA024085C	517
1.12.150	reg : stream8_err_minipg_cnt r_stat	0x00000000	0xA0240860	517
1.12.151	reg : stream8_err_watchdog_c ntr_stat		0xA0240864	518
1.12.152	reg : stream8_exc_exprate_cn tr_stat		0xA0240868	518
1.12.153	reg : stream8_exc_expratedev iate_cntr_stat		0xA024086C	518
1.12.154	reg : stream8_rate_measured_ stat	0x00000000	0xA0240870	518
1.12.155	reg : tpg9_packet_rate_clks_ ctrl	0x00000823	0xA0240934	518
1.12.156	reg : tpg9_packet_size_clks_ ctrl	0x00000040	0xA0240938	518
1.12.157	reg : stream9_expsize_dis_ct rl	0x00000034	0xA024093C	519
1.12.158	reg : stream9_exprate_dis_ct rl	0x007F0040	0xA0240940	519
1.12.159	reg : stream9_err_stat	0x00000000	0xA0240944	519
1.12.160	reg : stream9_err_expsize_cn tr_stat	0x00000000	0xA0240948	519
1.12.161	reg : stream9_err_pfifofull_ cntr_stat	0x00000000	0xA024094C	519
1.12.162	reg : stream9_err_bfifofull_ cntr_stat	0x00000000	0xA0240950	520
1.12.163	reg : stream9_err_maxsize_cn tr_stat	0x00000000	0xA0240954	520
1.12.164	reg : stream9_err_minsize_cn tr_stat	0x00000000	0xA0240958	520
1.12.165	reg : stream9_err_notlast_cn tr_stat	0x00000000	0xA024095C	520
1.12.166	reg: stream9_err_minipg_cnt	0x00000000	0xA0240960	520

	r_stat			
1.12.167	reg : stream9_err_watchdog_c ntr_stat	0x00000000	0xA0240964	520
1.12.168	reg : stream9_exc_exprate_cn tr_stat	0x00000000	0xA0240968	520
1.12.169	reg : stream9_exc_expratedev iate_cntr_stat	0x00000000	0xA024096C	520
1.12.170	reg : stream9_rate_measured_ stat	0x00000000	0xA0240970	521
1.12.171	reg : tpg10_packet_rate_clks	0x00000823	0xA0240A34	521
1.12.172	reg : tpg10_packet_size_clks	0x00000040	0xA0240A38	521
1.12.173	reg : stream10_expsize_dis_c	0x00000083	0xA0240A3C	521
1.12.174	reg : stream10_exprate_dis_c trl	0x007F0040	0xA0240A40	521
1.12.175	reg : stream10_err_stat	0x00000000	0xA0240A44	522
1.12.176	reg : stream10_err_expsize_c ntr_stat	0x00000000	0xA0240A48	522
1.12.177	reg : stream10_err_pfifofull _cntr_stat	0x00000000	0xA0240A4C	522
1.12.178	reg : stream10_err_bfifofull _cntr_stat	0x00000000	0xA0240A50	522
1.12.179	reg : stream10_err_maxsize_c ntr_stat	0x00000000	0xA0240A54	522
1.12.180	reg : stream10_err_minsize_c ntr_stat	0x00000000	0xA0240A58	522
1.12.181	reg : stream10_err_notlast_c ntr_stat	0x00000000	0xA0240A5C	523
1.12.182	reg : stream10_err_minipg_cn tr_stat	0x00000000	0xA0240A60	523
1.12.183	reg : stream10_err_watchdog_ cntr_stat	0x00000000	0xA0240A64	523
1.12.184	reg : stream10_exc_exprate_c ntr_stat	0x00000000	0xA0240A68	523
1.12.185	reg : stream10_exc_expratede viate_cntr_stat	0x00000000	0xA0240A6C	523
1.12.186	reg : stream10_rate_measured _stat	0x00000000	0xA0240A70	523
1.12.187	reg : tpg11_packet_rate_clks _ctrl	0x00000823	0xA0240B34	523
1.12.188	reg : tpg11_packet_size_clks _ctrl	0x00000040	0xA0240B38	524
1.12.189	reg : stream11_expsize_dis_c trl	0x0000001E	0xA0240B3C	524
1.12.190	reg : stream11_exprate_dis_c trl	0x007F0040	0xA0240B40	524
1.12.191	reg : stream11_err_stat	0x00000000	0xA0240B44	524
1.12.192	reg : stream11_err_expsize_c ntr_stat	0x00000000	0xA0240B48	525
1.12.193	reg : stream11_err_pfifofull _cntr_stat	0x00000000	0xA0240B4C	525
1.12.194	reg : stream11_err_bfifofull _cntr_stat	0x00000000	0xA0240B50	525
1.12.195	reg:stream11_err_maxsize_c ntr_stat	0x00000000	0xA0240B54	525
1.12.196	reg : stream11_err_minsize_c ntr_stat	0x00000000	0xA0240B58	525
1.12.197	reg : stream11_err_notlast_c ntr_stat	0x00000000	0xA0240B5C	525
1.12.198	reg : stream11_err_minipg_cn tr_stat	0x00000000	0xA0240B60	525
1.12.199	reg : stream11_err_watchdog_ cntr_stat	0x00000000	0xA0240B64	525
1.12.200	reg : stream11_exc_exprate_c ntr_stat		0xA0240B68	526
1.12.201	reg : stream11_exc_expratede	0x00000000	0xA0240B6C	526

	viate_cntr_stat		I	
1.12.202	reg : stream11_rate_measured	0x00000000	0xA0240B70	526
1.12.203	reg : tpg12_packet_rate_clks	0x00000823	0xA0240C34	526
1.12.204	reg : tpg12_packet_size_clks	0x00000040	0xA0240C38	526
1.12.205	reg : stream12_expsize_dis_c	0x00000040	0xA0240C3C	526
1.12.206	reg : stream12_exprate_dis_c	0x007F0040	0xA0240C40	527
1.12.207	reg : stream12_err_stat	0x00000000	0xA0240C44	527
1.12.208	reg : stream12_err_expsize_c ntr_stat	0x00000000	0xA0240C48	527
1.12.209	reg : stream12_err_pfifofull _cntr_stat	0x00000000	0xA0240C4C	527
1.12.210	reg : stream12_err_bfifofull _cntr_stat	0x00000000	0xA0240C50	528
1.12.211	reg : stream12_err_maxsize_c ntr_stat	0x00000000	0xA0240C54	528
1.12.212	reg : stream12_err_minsize_c ntr_stat	0x00000000	0xA0240C58	528
1.12.213	reg : stream12_err_notlast_c ntr_stat	0x00000000	0xA0240C5C	528
1.12.214	reg : stream12_err_minipg_cn tr_stat	0x00000000	0xA0240C60	528
1.12.215	reg : stream12_err_watchdog_ cntr_stat	0x00000000	0xA0240C64	528
1.12.216	reg : stream12_exc_exprate_c ntr_stat	0x00000000	0xA0240C68	528
1.12.217	reg : stream12_exc_expratede viate_cntr_stat	0x00000000	0xA0240C6C	528
1.12.218	reg : stream12_rate_measured _stat	0x00000000	0xA0240C70	529
1.12.219	reg : tpg13_packet_rate_clks _ctrl	0x00000823	0xA0240D34	529
1.12.220	reg : tpg13_packet_size_clks _ctrl	0x00000040	0xA0240D38	529
1.12.221	reg : stream13_expsize_dis_c trl	0x00000040	0xA0240D3C	529
1.12.222	reg : stream13_exprate_dis_c trl	0x007F0040	0xA0240D40	529
1.12.223	reg : stream13_err_stat	0x00000000	0xA0240D44	530
1.12.224	reg : stream13_err_expsize_c ntr_stat	0x00000000	0xA0240D48	530
1.12.225	reg : stream13_err_pfifofull _cntr_stat	0x00000000	0xA0240D4C	530
1.12.226	reg : stream13_err_bfifofull _cntr_stat	0x00000000	0xA0240D50	530
1.12.227	reg : stream13_err_maxsize_c ntr_stat	0x00000000	0xA0240D54	530
1.12.228	reg : stream13_err_minsize_c ntr_stat	0x00000000	0xA0240D58	530
1.12.229	reg : stream13_err_notlast_c ntr_stat	0x00000000	0xA0240D5C	531
1.12.230	reg : stream13_err_minipg_cn tr_stat	0x00000000	0xA0240D60	531
1.12.231	reg : stream13_err_watchdog_ cntr_stat	0x00000000	0xA0240D64	531
1.12.232	reg : stream13_exc_exprate_c ntr_stat		0xA0240D68	531
1.12.233	reg : stream13_exc_expratede viate_cntr_stat		0xA0240D6C	531
1.12.234	reg : stream13_rate_measured _stat		0xA0240D70	531
1.12.235	reg : tpg14_packet_rate_clks _ctrl	0x00000823	0xA0240E34	532
1.12.236	reg : tpg14_packet_size_clks	0x00000040	0xA0240E38	532

	_ctrl			
1.12.237	reg : stream14_expsize_dis_c trl	0x00000040	0xA0240E3C	532
1.12.238	reg : stream14_exprate_dis_c trl	0x007F0040	0xA0240E40	532
1.12.239	reg : stream14_err_stat	0x00000000	0xA0240E44	532
1.12.240	reg : stream14_err_expsize_c ntr_stat	0x00000000	0xA0240E48	533
1.12.241	reg : stream14_err_pfifofull _cntr_stat	0x00000000	0xA0240E4C	533
1.12.242	reg : stream14_err_bfifofull	0x00000000	0xA0240E50	533
1.12.243	reg : stream14_err_maxsize_c ntr_stat	0x00000000	0xA0240E54	533
1.12.244	reg : stream14_err_minsize_c ntr_stat	0x00000000	0xA0240E58	533
1.12.245	reg : stream14_err_notlast_c ntr_stat	0x00000000	0xA0240E5C	533
1.12.246	reg:stream14_err_minipg_cn tr_stat	0x00000000	0xA0240E60	533
1.12.247	reg : stream14_err_watchdog_ cntr_stat	0x00000000	0xA0240E64	534
1.12.248	reg : stream14_exc_exprate_c ntr_stat	0x00000000	0xA0240E68	534
1.12.249	reg : stream14_exc_expratede viate_cntr_stat	0x00000000	0xA0240E6C	534
1.12.250	reg : stream14_rate_measured	0x00000000	0xA0240E70	534
1.12.251	reg : tpg15_packet_rate_clks _ctrl	0x00000823	0xA0240F34	534
1.12.252	reg : tpg15_packet_size_clks _ctrl	0x00000040	0xA0240F38	534
1.12.253	reg : stream15_expsize_dis_c trl	0x00000040	0xA0240F3C	535
1.12.254	reg : stream15_exprate_dis_c trl	0x007F0040	0xA0240F40	535
1.12.255	reg : stream15_err_stat	0x00000000	0xA0240F44	535
1.12.256	reg : stream15_err_expsize_c ntr_stat	0x00000000	0xA0240F48	535
1.12.257	reg : stream15_err_pfifofull _cntr_stat	0x00000000	0xA0240F4C	535
1.12.258	reg : stream15_err_bfifofull _cntr_stat	0x00000000	0xA0240F50	536
1.12.259	reg : stream15_err_maxsize_c ntr_stat	0x00000000	0xA0240F54	536
1.12.260	reg : stream15_err_minsize_c ntr_stat	0x00000000	0xA0240F58	536
1.12.261	reg : stream15_err_notlast_c ntr_stat	0x00000000	0xA0240F5C	536
1.12.262	reg : stream15_err_minipg_cn tr_stat	0x00000000	0xA0240F60	536
1.12.263	reg : stream15_err_watchdog_ cntr_stat	0x00000000	0xA0240F64	536
1.12.264	reg : stream15_exc_exprate_c ntr_stat	0x00000000	0xA0240F68	536
1.12.265	reg : stream15_exc_expratede viate_cntr_stat	0x00000000	0xA0240F6C	537
1.12.266	reg : stream15_rate_measured _stat	0x00000000	0xA0240F70	537
1.13	block : ipi_mcdma_axilite_pg 288		0xA1000000 - 0xA1001FFF	537
1.13.1	memory : ram_8kb_inst		0xA1000000, 0xA1000004 0xA1001FFF	537
1.13.1.1	reg : ram_8kb_inst	0x00000000	0xA1000000, 0x0000000000	
1.14	block : ipi_gpio_cache_contr ol		0xA2000000 - 0xA2000003	537
1.14.1	reg : gpio_cache_control_ins t	0x0000002B	0xA2000000	537
1.15	block : ipi_mcdma_bd_ram		0xAA000000 - 0xAA007FFF	537

1.15.1	memory : ram_32kb_inst		0xAA000000, 0xAA000004 0xAA007FFF	537
1.15.1.1	reg : ram_32kb_inst	0x00000000	0xAA000000, 0x0000000000	
1.16	block : ipi_mcdma_debug_ram		0xAB000000 - 0xAB007FFF	538
1.16.1	memory : ram_32kb_inst		0xAB000000, 0xAB000004 0xAB007FFF	538
1.16.1.1	reg : ram_32kb_inst	0x00000000	0xAB000000, 0x0000000000	

1 dg_dtec_odf	Chip	0x00000000 - 0xFFFFFFFF
Complete Register map HSI document for DTEC PL.		

0xA0000000 -

0xA000001B

Block

1.1.1	1.1.1 proj_id 0xA0000000							
This register defines the Project ID value								
bits name s/w h/w default description								
31:0	project_id	ro	na	0x54726F6E	ASCII value for TR	ON		

1.1.2	firm_id	Reg.	0xA0000004								
This	This register defines the Firmware ID										
bits	bits name s/w h/w default description										
31:0 firmware_id ro wo X Firmware ID for xTEC											

1.1.3	firm_build	Reg.	0xA0000008							
This register defines the Firmware build ID										
bits	name	s/w	h/w	default		description	n			
31:0	firmware_build_ id	ro	WO	X	This register is currently undefined in D000741068. Will be set after FPGA is built.					

1.1.4	fpga_id	0xA000000C								
	This regiser define the FPGA firmware image identifier. For example: F70.02.00 for a cTEC image for NXE 3800 phase 2 first release									
bits	name	s/w	h/w	default	description					
31:24	fpga_type	ro	wo	X	Major product identifier. This field only identifies the major product and is treated and displayed as an ASCII character. cTEC is 0x46 or ASCII F					
23:16	configuration	ro	WO	X	Major generation identification. This hex field is displayed as a decimal value by SW. NXE3800 is hex 0x46 or decimal 70.					
15:8	major_revision	ro	WO	X	New features or capabilities definition. This hex field is displayed as a decimal value by SW. For phase 0 this value will be 00 in decimal. For phase 1 this value will be 01 in decimal. etc.					
7:0	minor_revision	ro	WO	X	Minor revision definition. This field indicates bug fixes have been applied. For any new features/capabilities increment this field.					

1.1.5 fp	ga_build	Reg.	0xA0000010						
This regi	This register defines the FPGA_BUILD in ASCII								
bits	name	s/w h/w	default		descri	ption			

1.1 id\_registers

1.1.6	tec_id	0xA0000014						
This register defines the TEC_ID to identify major product identifier and variations								
bits	name	description						
31:24	major_product_i d	ro	WO	Х	Major product identifier. This field only identifies the major product and is treated and displayed as an ASCII character. 0x43 for cTEC. 0x45 for eTEC			
23:16	variation	ro	na	0x0	Variation field currently undefined. Shall be set to 0x00			
15:8	sub_variation	ro	na	0x0	Sub variation field currently undefined. Shall be set to 0x00			
7:0	spare	ro	na	0x0	Spare field currently undefined. Shall be set to 0x00			

1.1.7	context_id	Reg.	0xA0000018							
This r	This register represents the CONTEXT ID value for port X76 of the cTEC									
bits	name	s/w	h/w	default		description	n			
3:0	3:0 CID ro wo X 4-bit field for the context ID that is connected. 4'b1110 = eTEC, 4'b1101 = cTEC, 4'b1011 = dTEC									

1.2 core_registers_srdl	Block □ T	0xA0010000 - 0xA0017FFF
Register map used to access and control global FPGA functionality		

1.2.1	core_module_name	Reg.	0xA0010000							
Defin	Defines the module name									
bits	bits name s/w h/w default description									
31:0	module_name	ro	ASCII code for mo	odule name - top	module(core) = core					

1.2.2	core_module_ve	ersion	Reg.	0xA0010004					
Modu	lle version								
bits name s/w h/w default description									
31:16	rfu	ro	na	0x0	Reserver for Future Use - RFU				
15:8	major_revision	ro	wo	0x0	Major Revisoin of module - N nition have been added.	lew features or capabilities defi-			
7:0	minor_revision	ro	Minor Revision of module. The have been applied. For any ment, this field will reset to ze	new features/capabilities incre-					

1.2.3	core_page_propert	Reg.	0xA0010008						
Address page properties									
bits	name		description						
31	present	ro	WO	0x1	Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not.				
30:16	rfu	ro	na	0x0	Reserver for Futu	re Use - RFU			
15:8	page_size	ro	na	0x1	Address page siz value to 4k and e		BkB, etc. Divide the real		
7:0	unified_header_ rev	ro	na	0x1	Unified Header Fo	ormat common re	gisters revision.		

1.2.4	core_scratchregist	Reg.	0xA001000C								
Scrate	Scratchregister register										
bits	bits name s/w h/w default description										
31:0	scratchregister	SW can write to it	and read from it t	for test purposes.							

1.2.5	core_irq_enable				0xA0010010
Inter	rupt Requests Enable/l	Mask Contr	ol Reg	gister	
bits	name	s/w	h/w	default	description
0	irq0_enable	rw	ro	0x0	IRQ0 enable bit. Used by MCDMA CH1 S2MM IRQ. Not in use in DTEC.
1	irq1_enable	rw	ro	0x0	IRQ1 enable bit. Used by MCDMA CH2 S2MM IRQ. Not in use in DTEC.
2	irq2_enable	rw	ro	0x0	IRQ2 enable bit. Used by MCDMA CH3 S2MM IRQ. Not in use in DTEC.
3	irq3_enable	rw	ro	0x0	IRQ3 enable bit. Used by MCDMA CH4 S2MM IRQ. Not in use in DTEC.
4	irq4_enable	rw	ro	0x0	IRQ4 enable bit. Used by MCDMA CH5 S2MM IRQ. Not in use in DTEC.
5	irq5_enable	rw	ro	0x0	IRQ5 enable bit. Used by MCDMA CH6 S2MM IRQ. Not in use in DTEC.
6	irq6_enable	rw	ro	0x0	IRQ6 enable bit. Used by MCDMA CH7 S2MM IRQ. Not in use in DTEC.
7	irq7_enable	rw	ro	0x0	IRQ7 enable bit. Used by MCDMA CH8 S2MM IRQ. Not in use in DTEC.
8	irq8_enable	rw	ro	0x0	IRQ8 enable bit. Used by MCDMA CH8 S2MM IRQ. Not in use in DTEC.
9	irq9_enable	rw	ro	0x0	IRQ9 enable bit. Used by MCDMA CH9 S2MM IRQ. Not in use in DTEC.
10	irq10_enable	rw	ro	0x0	IRQ10 enable bit. Used by MCDMA CH10 S2MM IRQ. Not in use in DTEC.
11	irq11_enable	rw	ro	0x0	IRQ11 enable bit. Used by MCDMA CH11 S2MM IRQ. Not in use in DTEC.
12	irq12_enable	rw	ro	0x0	IRQ12 enable bit. Used by MCDMA CH12 S2MM IRQ. Not in use in DTEC.
13	irq13_enable	rw	ro	0x0	IRQ13 enable bit. Used by MCDMA CH13 S2MM IRQ. Not in use in DTEC.
14	irq14_enable	rw	ro	0x0	IRQ14 enable bit. Used by MCDMA CH14 S2MM IRQ. Not in use in DTEC.
15	irq15_enable	rw	ro	0x0	IRQ15 enable bit. Used by MCDMA CH15 S2MM IRQ. Not in use in DTEC.

1.2.6	core_irq_pending			Reg.	0xA0010014						
Interr	Interrupt Pending Status Register										
bits	name	s/w		description							
0	irq0_pending	r/w1c	WO	0x0		ve edge. Used by	Write '1' to clear. Asserts MCDMA CH1 S2MM				
1	irq1_pending	r/w1c	WO	0x0		ve edge. Used by	Write '1' to clear. Asserts MCDMA CH2 S2MM				
2	irq2_pending	r/w1c	WO	0x0		ve edge. Used by	Write '1' to clear. Asserts MCDMA CH3 S2MM				
3	irq3_pending	r/w1c	WO	0x0		ve edge. Used by	Write '1' to clear. Asserts MCDMA CH4 S2MM				
4	irq4_pending	r/w1c	WO	0x0		ve edge. Used by	Write '1' to clear. Asserts MCDMA CH5 S2MM				

5	irq5_pending	r/w1c	WO	0x0	IRQ5 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH6 S2MM IRQ. Not in use in DTEC.
6	irq6_pending	r/w1c	WO	0x0	IRQ6 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH7 S2MM IRQ. Not in use in DTEC.
7	irq7_pending	r/w1c	WO	0x0	IRQ7 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH8 S2MM IRQ. Not in use in DTEC.
8	irq8_pending	r/w1c	WO	0x0	IRQ8 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH9 S2MM IRQ. Not in use in DTEC.
9	irq9_pending	r/w1c	WO	0x0	IRQ9 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH10 S2MM IRQ. Not in use in DTEC.
10	irq10_pending	r/w1c	WO	0x0	IRQ10 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH11 S2MM IRQ. Not in use in DTEC.
11	irq11_pending	r/w1c	WO	0x0	IRQ11 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH12 S2MM IRQ. Not in use in DTEC.
12	irq12_pending	r/w1c	WO	0x0	IRQ12 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH13 S2MM IRQ. Not in use in DTEC.
13	irq13_pending	r/w1c	WO	0x0	IRQ13 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH14 S2MM IRQ. Not in use in DTEC.
14	irq14_pending	r/w1c	WO	0x0	IRQ14 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH15 S2MM IRQ. Not in use in DTEC.
15	irq15_pending	r/w1c	WO	0x0	IRQ15 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Used by MCDMA CH16 S2MM IRQ. Not in use in DTEC.

1.2.7	core_irq_raw	1	Reg.	0xA0010018						
Interrupt Raw Status Register										
bits	name		descriptio	n						
0	irq0_raw	ro	wo	0x0	IRQ0 raw status b	it. Used by MCD	MA CH1 S2MM IRQ.			
1	irq1_raw	ro	WO	0x0	IRQ1 raw status b	it.Used by MCDI	MA CH1 S2MM IRQ.			
2	irq2_raw	ro	wo	0x0			MA CH3 S2MM IRQ.			
3	irq3_raw	ro	wo	0x0	IRQ3 raw status b	it.Used by MCDI	MA CH4 S2MM IRQ.			
4	irq4_raw	ro	WO	0x0	IRQ4 raw status b	it. Used by MCD	MA CH5 S2MM IRQ.			
5	irq5_raw	ro	wo	0x0	IRQ5 raw status b	it.Used by MCDI	MA CH6 S2MM IRQ.			
6	irq6_raw	ro	wo	0x0	IRQ6 raw status b	it. Used by MCD	MA CH6 S2MM IRQ.			
7	irq7_raw	ro	wo	0x0	IRQ7 raw status b	it.Used by MCDI	MA CH8 S2MM IRQ.			
8	irq8_raw	ro	WO	0x0	IRQ8 raw status b	it. Used by MCD	MA CH9 S2MM IRQ.			
9	irq9_raw	ro	WO	0x0	IRQ9 raw status b	it.Used by MCDI	MA CH10 S2MM IRQ.			
10	irq10_raw	ro	WO	0x0		,	DMA CH11 S2MM IRQ.			
11	irq11_raw	ro	wo	0x0	IRQ11 raw status	bit.Used by MCE	DMA CH12 S2MM IRQ.			
12	irq12_raw	ro	WO	0x0	IRQ12 raw status	bit. Used by MC	DMA CH13 S2MM IRQ.			
13	irq13_raw	ro	WO	0x0	IRQ13 raw status	bit.Used by MCE	MA CH14 S2MM IRQ.			
14	irq14_raw	ro	WO	0x0	IRQ14 raw status	bit. Used by MC	DMA CH15 S2MM IRQ.			
15	irq15_raw	ro	WO	0x0	IRQ15 raw status	bit.Used by MCE	MA CH16 S2MM IRQ.			

1.2.8	core_irq_force	Reg.	0xA001001C						
Interrupt Force Control Register									
bits	name	s/w	h/w	default		description	า		
0 irq0_force rw ro 0x0 IRQ0 force bit. SW to write '1' to emulate an '0' to clear. Used by MCDMA CH1 S2MM IR on DTEC.									

1	irq1_force	rw	ro	0x0	IRQ1 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH2 S2MM IRQ. Not in use on DTEC.
2	irq2_force	rw	ro	0x0	IRQ2 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH3 S2MM IRQ. Not in use on DTEC.
3	irq3_force	rw	ro	0x0	IRQ3 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH4 S2MM IRQ. Not in use on DTEC.
4	irq4_force	rw	ro	0x0	IRQ force bit. SW to write '1' to emulate an interrupt. Write '5' to clear. Used by MCDMA CH5 S2MM IRQ. Not in use on DTEC.
5	irq5_force	rw	ro	0x0	IRQ5 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH6 S2MM IRQ. Not in use on DTEC.
6	irq6_force	rw	ro	0x0	IRQ6 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH7 S2MM IRQ. Not in use on DTEC.
7	irq7_force	rw	ro	0x0	IRQ7 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH8 S2MM IRQ. Not in use on DTEC.
8	irq8_force	rw	ro	0x0	IRQ8 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH9 S2MM IRQ. Not in use on DTEC.
9	irq9_force	rw	ro	0x0	IRQ9 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH10 S2MM IRQ. Not in use on DTEC.
10	irq10_force	rw	ro	0x0	IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH11 S2MM IRQ. Not in use on DTEC.
11	irq11_force	rw	ro	0x0	IRQ11 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH12 S2MM IRQ. Not in use on DTEC.
12	irq12_force	rw	ro	0x0	IRQ12 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH13 S2MM IRQ. Not in use on DTEC.
13	irq13_force	rw	ro	0x0	IRQ13 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH14 S2MM IRQ. Not in use on DTEC.
14	irq14_force	rw	ro	0x0	IRQ14 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH15 S2MM IRQ. Not in use on DTEC.
15	irq15_force	rw	ro	0x0	IRQ15 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Used by MCDMA CH16 S2MM IRQ. Not in use on DTEC.

1.2.9	build_time	Reg.	0xA0010040						
FPGA Build Time									
bits	name	s/w	h/w	default	description				
31:0	build_time	ro	na	0xDEADC0DEFPGA Build time hh-mm-ss using 24h format. All numbers are decimal but stored without conversion to hex. Automa cally generated during compilation.					

1.2.1	0 build_date	Reg.	0xA0010044						
FPGA Build Date									
bits	name	s/w	h/w	default		description			
31:0	build_date	ro	na			version to hex. A	mbers are decimal but automatically generated		

1.2.11 build_githash	Reg.	0xA0010048

FPGA	FPGA Build GIT Hash										
bits	name	s/w	h/w	default	description						
31:0	build_githash	ro	na		FPGA Build GIT hash, the first 8 Bytes of the commit hash. All numbers are in hex. Automatically generated during comilation.						

1.2.1	2 uptime	Reg.	0xA0010054								
Uptim	Uptime										
bits	bits name s/w h/w default description										
31:0	uptime	ed in seconds									

1.2.1	3 freerun_counter_s	Reg.	0xA0010060								
Free	Free running counter status										
bits	name	s/w	h/w	default		description	า				
31:0 freerun_counter rw na 0x0 Current free running counter at 125MHz. Can be used for software profiling.											

1.2.1	4 resets_ctrl				0xA0010064
Majo	r DTEC modules resets,	controlle	d by S	SW	
bits	name	s/w	h/w	default	description
31:0	resets	ΓW	ro	0x0	Major DTEC modules resets controlled by SW, check DTEC EDS D001264457 for details.  Reset signal - 1 = reset / 0 = no reset  Bit Reset Signal name Signal Clock Domain Module Name Short Description  0 core_reset ps_clk125 Core DTEC Core module, deisgn top level equivalent  1 algo_reset ps_clk125 Algo Matalb algorithm and interfaces status and control  2 clkalgo_reset ps_clkalgo Algo Matlab algorithm slow clock logic  3 tselclient_reset ps_clk125 TSEL Client TSEL Client facing ETEC status and control  4 tselbridge_reset ps_clk125 TSEL Bridge TSEL Bridge facing DAMP status and control  5 clk50_reset ps_clk50 TSEL GDB TSEL GDB reconfiguration clock domain  6 eth1ge_reset ps_clk125 1G Ethernet 1GE interface towards LC  7 mcdma_reset ps_clk125 MCDMA IP Xilinx MCDMA IP  8 mcdmafeed_reset ps_clk125 MCDMA Feed MCDMA streams shaping logic  9 bpam2dcm_reset ps_clk125 BPAM2 DCM BPAM 2  (DCM) interface status and control  10 bpam3mmdc_reset ps_clk125 BPAM3 MMDC BPAM 3  (MMDC) interface status and control  11 todlts_reset ps_clk125 TOD LTS TOD and LTS maintaing  12 dampregs_reset ps_clk125 DAMP Registers data received from DAMP  13-31 <reserved>  Writing to this register '1' will apply reset, writing '0' will remove the reset.  Reading the register will indicate the reset status, it might be updated a few clocks later after it is manipulted by SW.</reserved>

50MH	50MHz Clock pulses, measured for 1s.									
bits	name	s/w	h/w	default	description					
31:0	refclk_freq50mh z	ro	WO	0x0	Frequency of 50MHz clock in Hz. Represents the number of clocks captured for 1 second. Has to be converted from Hex to decimal.					

1.2.1	6 refclk_freqalgo_st		Reg.	0xA001006C						
Algo Clock pulses, measured for 1s.										
bits	name	s/w	h/w	default	description					
31:0	refclk_freqalgo	ro	WO	0x0	Frequency of Algo clock in Hz. Represents the number of clocks captured for 1 second. Has to be converted from H to decimal.					

1.2.1	7 debug_ctrl	Reg.	0xA0010070							
Debug Control										
bits	name	s/w	h/w	default		description	١			
31:0	debug	rw	ro	0x0	Current debug bu tionality	s driven value - fo	or temporary debug func-			

1.2.18	8 debug_stat	Reg.	0xA0010074							
Debug Status										
bits	name	s/w	h/w	default		description	า			
31:0	debug	ro	wo	0x0	current debug bus status - NOTE: software should de- bounce the read value					

1.2.1	9 tod_lo	ad_low	Reg.	0xA0010080							
TOD	TOD Load Low										
bits		name	s/w	h/w	default	description					
31:0	tod_load_	low	rw	ro	0x0	Lower 32 bits writ	ten to TOD by PS				

1.2.2	0 tod_load_high	Reg.	0xA0010084								
TOD	TOD Load High										
bits	name	s/w	h/w	default	description						
31:0	tod_load_high	rw	ro	0x0	Upper 32 bits writ	ten to TOD by PS					

1.2.2	1 tod_cntr_low		Reg.	0xA0010088						
TOD	TOD Counter Low									
bits	name	s/w	h/w	default	description					
31:0	tod_cntr_low	ro	wo	0x0	Lower 32 bits of TOD counter read by PS. Caution: these lower 32 bits rollover every second. No mechanism is currently implemented to make this read coherent with tod_cntr_high.					

1.2.2	2 tod_cntr_high	Reg.	0xA001008C								
TOD	TOD Counter High										
bits	name	s/w	h/w	default	description						
31:0	tod_cntr_high	ro	wo	0x0	Upper 32 bits of TOD counter read by PS						

1.2.2	3 lts_cr	ntr		Reg.	0xA0010090							
LTS (	LTS Counter											
bits		name	s/w	h/w	default	description						
31:0	lts_cntr		ro	WO	0x0	LTS counter read	by PS					

1.2.2	4 tod_in	cr		Reg.	0xA0010094				
TOD Increment									
bits		name	s/w	h/w	default	description			
31:0	tod_incr		rw	ro	0x225C01	Number of LSBs to increment the TOD counter each clock period. Resolution is 2^-48 sec/LSB. 32'h00225C17 ~= 8ns per clock.			

1.2.2	5 led_control			Reg.	0xA00100A0					
LED Control										
bits	name	s/w	h/w	default		description	١			
7:6	status_led	rw	ro	0x2	Status LED: 0x0 ange	= OFF, 0x1 = Red	, 0x2 = Green, 0x3 = Or-			
5:4	state_led	rw	ro	0x2	State LED: 0x0 = ange	OFF, $0x1 = Red$ ,	0x2 = Green, 0x3 = Or-			
3:2	fault_led	rw	ro	0x2	Fault LED: 0x0 = ange	OFF, $0x1 = Red$ ,	0x2 = Green, 0x3 = Or-			
1:0	master_led	rw	ro	0x2	Master LED: 0x0 ange	= OFF, 0x1 = Red	d, 0x2 = Green, 0x3 = Or-			

1.2.2	6 damp_to_algo_sn	Reg.	0xA00100B0								
Counts the number of AXIS Snooper Output Packets.											
bits	name	s/w	h/w	default		description	١				
31:0	counter	ro	wo	0x0	Counter						

1.2.2	7 damp_to_algo_sn	Reg.	0xA00100B4							
Counts the number of AXIS Snooper Dropped Packets.										
bits	name	s/w	h/w	default		description	n			
31:0	counter	ro	wo	0x0	Counter					

1.2.28	8 damp_to_algo_sn	Reg.	0xA00100B8								
Counts the number of AXIS Snooper Timeouts Packets.											
bits	name	s/w	h/w	default	t description						
31:0	counter	ro	wo	0x0	Counter						

1.2.2	9 esm_to_algo_sno	Reg.	0xA00100BC								
Counts the number of AXIS Snooper Output Packets.											
bits	name	s/w	h/w	default	description						
31:0	counter	ro	wo	0x0	Counter						

1.2.30 esm_to_algo_snoop_drop_count	Reg.	0xA00100C0
1.2.30 csiii_to_aigo_siloop_diop_codiit		07.11.00.100.00

Coun	Counts the number of AXIS Snooper Dropped Packets.										
bits	name	s/w	h/w	default	description						
31:0	counter	ro	wo	0x0	Counter						

1.2.3	1 esm_to_algo_sno	Reg.	0xA00100C4								
Counts the number of AXIS Snooper Timeouts Packets.											
bits	bits name s/w h/w default description										
31:0	counter	ro	wo	0x0	Counter						

1.2.32 dam	gion	damp_diag_region							0xA0014000, 0xA0014004 0xA0017FFF	
offset		dep	th	4096	width	32	def	ault	0x0	
This buffer is	for CPU to be	able to r	ead D	AMP Diagr	nostic Data	a from the	TSEL Brid	ge		

1.3 algo_ing_registers_srdl	Block □⊤□	0xA0020000 - 0xA00206CB
Register map of the ingress algo registers		

1.3.1	algo_ingress_mode	Reg.	0xA0020000								
Defin	Defines the module name										
bits	name	s/w	h/w	default		description	n				
31:0	module_name	ro	ASCII code for me	odule name - top	module(core) = core						

1.3.2	algo_ingress_mod	dule_ve	Reg.	0xA0020004						
Module version										
bits	name	s/w	h/w	default	efault description					
31:16	rfu	ro	na	0x0	Reserved for Futu	ire Use - RFU				
15:8	major_revision	ro	na	0x0	Major Revision					
7:0	minor_revision	ro	na	0x0	Minor Revision					

1.3.3	algo_ingress_page	_prop		Reg.	0xA0020008					
Address page properties										
bits	name		description	1						
31	present	ro	wo	0x1	Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is available/implemented or not.					
30:16	rfu	ro	na	0x0	Reserver for Futu	re Use - RFU				
15:8	page_size	ro	na	0x1	Address page siz value to 4k and e		BkB, etc. Divide the real			
7:0	unified_header_ rev	ro	na	0x1	Unified Header Fo	ormat common re	gisters revision.			

1.3.4	algo_ingress_scr	atchreg		Reg.	0xA002000C					
Scratchregister register										
bits	bits name s/w h/w default description									
31:0	scratchregister	rw	na	0x12345678	SW can write to it and read from it for test purposes.					

1.3.5	algo_ingress_irq_e	nable		Reg.	0xA0020010					
Interrupt Requests Enable/Mask Control Register										
bits	name	s/w	h/w	default		description	า			
0	irq0_enable	rw	ro	0x0	IRQ0 enable bit. N	lot implemented I	here/DTEC			
1	irq1_enable	rw	ro	0x0	IRQ1 enable bit. N	lot implemented I	here/DTEC			

1.3.6	algo_ingress_irq_p	Reg.	0xA0020014							
Interr	Interrupt Pending Status Register									
bits	name	s/w	h/w	default	description					
0	irq0_pending	r/w1c	WO	0x0	IRQ0 pending status bit, sticky bit. interrupt on positive edge. Not imp					
1	irq1_pending	r/w1c	WO	0x0	IRQ1 pending status bit, sticky bit. interrupt on positive edge. Not imp					

1.3.7	algo_ingress_irq_ra	Reg.	0xA0020018							
Interrupt Raw Status Register										
bits	name	s/w	h/w	default	description					
0	irq0_raw	ro	wo	0x0	IRQ0 raw status b	it. Not implement	ed here/DTEC			
1	irq1_raw	ro	wo	0x0	IRQ1 raw status b	it. Not implement	ed here/DTEC			

1.3.8	algo_ingress_irq_fo	Reg.	0xA002001C							
Interr	Interrupt Force Control Register									
bits	name	s/w	h/w	default	description					
0	irq0_force	rw	ro	0x0	IRQ0 force bit. SW to write '1' to '0' to clear. Not implemented her	•				
1	irq1_force	rw	ro	0x0	IRQ1 force bit. SW to write '1' to '0' to clear. Not implemented her	•				

1.3.9	machineconstants_	_clst_	perc	Reg.	0xA0020020					
For small peak removal after main droplets clustering. This is the 2nd time of applying such threshold, refer to table 2.2 for 1st time;										
bits	name	s/w	h/w	default		description	on			
31:0	machineconstant s_clst_thr_pkva I_low_perc	rw	ro	0x7AE	· ·		droplets clustering. This reshold, refer to table 2.2			

1.3.1	0 machineconstants	Reg.	0xA0020024							
For main droplets peak clustering, window size around new pivots; if the module is performing TF measurement, this parameter need to be modified, refer to section 5 (Calibration CPD)										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_clst_thr_neig hbor_perc	rw	ro	0xCCD	pivots; if the modu	ule is performing	window size around new TF measurement, this pa- to section 5 (Calibration			

1.3.11 machineconstants_clst_thr_dist2antinode_per	Reg.	0xA0020028
С		

Defin	Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing										
bits	name	s/w	h/w	default	description						
-	machineconstant s_clst_thr_dist 2antinode_perc	rw	ro	0x599A	Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing						

1.3.1	2 machineconstants	_clst	r	Reg.	0xA002002C						
pkVal ratio for merging close-by clusters for K-mean algorithm											
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_clst_km_nearc luster	rw	ro	0x599A	pkVal ratio for me rithm	rging close-by clu	usters for K-mean algo-				

1.3.1	3 machineconstants	Reg.	0xA0020030							
Weight factor for the peak position term in the GMM probability distribution used in EM;										
bits	name	s/w	h/w	default		description				
31:0	machineconstant s_clst_em_wt_pk pos	rw	ro	0xC000	Weight factor for the bility distribution u	•	term in the GMM proba-			

1.3.1	4 machineconstants	st	Reg.	0xA0020034						
Centroid distance for merging clusters;										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_clst_em_centr oiddist	rw	ro	0x199A	Centroid distance for merging clusters;					

1.3.1 rc	1.3.15 machineconstants_clst_em_thr_pkval_pivot_pe oxA0020038										
Term	Terminate condition for main droplets clustering.										
31:0	name s/w h/w default description machineconstant rw ro 0xC000 Terminate condition for main droplets clustering. s_clst_em_thr_p kval_pivot_perc										

1.3.1	1.3.16 machineconstants_clst_em_maxclustersize 0xA002003C										
Cluster size threshold for merging clusters;											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_clst_em_maxcl ustersize	rw	ro	0xB333	Cluster size threshold for merging clusters;						

1.3.1	7 machineconstants	Reg.	0xA0020040							
Threshold (% of DS) for relabel close by intermediate droplet clusters										
bits	name	s/w	h/w	default		description	٦			
31:0	31:0 machineconstant rw ro 0x9000 Threshold (% of DS) for relabel close by intermediate droplet clusters									

1.3.18 machineconstants_clst_em_ds2m	Reg.	0xA0020044

Threshold (% of DS) for relabel close by intermediate droplet clusters									
bits	bits name s/w h/w default description								
31:0	machineconstant	rw	ro	0x4829	Threshold (% of DS) for relabel close by intermediate				
	s_clst_em_ds2m droplet clusters								

1.3.19 machineconstants_clst_em_minclustersize 0xA0020048										
Cluster size threshold for merging clusters;										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_clst_em_mincl ustersize	rw	ro	0x3333	Cluster size thres	er size threshold for merging clusters;				

	0 machineconstants kpos	lustercen	Reg.	0xA002004C								
Dista	Distance to centroid for merging clusters											
bits	name	s/w	h/w	default		description	า					
31:0	machineconstant s_clst_em_maxdi st2clustercente r_pkpos	rw	ro	0xCCD	Distance to centroid for merging clusters							

1.3.2	1 machineconstants	Reg.	0xA0020050							
Criteria for merging clusters based on pkPos										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_clst_em_delta _pkpos	rw	ro	0x28F	Criteria for mergir	riteria for merging clusters based on pkPos				

	1.3.22 machineconstants_clst_fl_thr_pkval_2m_small er_bound 0xA0020054										
Threshold for relabeling outliers as presubdroplets											
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_clst_fl_thr_p kval_2m_smaller bound	rw	ro	0xFF3	Threshold for relabeling outliers as presubdroplets						

1.3.23 machineconstants_clst_fl_thr_pkval_500_2m_b ound											
Threshold for relabeling outliers as subdroplets											
bits	name	s/w	h/w	default		description	1				
31:0	machineconstant s_clst_fl_thr_p kval_500_2m_bou nd	rw	ro	0x2DCC	Threshold for relabeling outliers as subdroplets						

1.3.2	4 machineconstants		Reg.	0xA002005C						
Sampling frequency from DCM BPAM										
bits	name	s/w	h/w	default		description	n			
31:0 machineconstant rw ro 0x7735940 Sampling frequency from DCM BPAM s_clst_bpam_fsa										

mp |

#### 1.3.25 machineconstants\_clst\_thr\_pkval\_low\_ddm\_per

Reg.

0xA0020060

For small peak removal after main droplets clustering. This is the 2nd time of applying such threshold, refer to table 2.2 for 1st time;

bits	name	s/w	h/w	default	description
-	machineconstant s_clst_thr_pkva l_low_ddm_perc	rw	ro	0x7AE	For small peak removal after main droplets clustering. This is the 2nd time of applying such threshold, refer to table 2.2 for 1st time;

#### 1.3.26 machineconstants\_clst\_thr\_neighbor\_ddm\_perc

Reg.

0xA0020064

For main droplets peak clustering, window size around new pivots; if the module is performing TF measurement, this parameter need to be modified, refer to section 5 (Calibration CPD)

bits	name	s/w	h/w	default	description
31:0	machineconstant s_clst_thr_neig hbor_ddm_perc	rw	ro	0x2E14	For main droplets peak clustering, window size around new pivots; if the module is performing TF measurement, this parameter need to be modified, refer to section 5 (Calibration CPD)

#### 1.3.27 machineconstants\_clst\_thr\_dist2antinode\_ddm \_perc

Reg.

0xA0020068

Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing

	some region of minimum of the process of the second of the										
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_clst_thr_dist 2antinode_ddm_p erc	rw	ro	0x7333	Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing						

## 1.3.28 machineconstants\_clst\_fl\_thr\_pkval\_500\_2m\_d dm\_bound



0xA002006C

Threshold for labeling ddm peaks as subdroplets

	•		-		
bits	name	s/w	h/w	default	description
31:0	machineconstant s_clst_fl_thr_p kval_500_2m_ddm _bound	rw	ro	0x2DCC	Threshold for labeling ddm peaks as subdroplets

# 1.3.29 machineconstants\_clst\_thr\_pkval\_low\_tfdcm\_p erc



0xA0020070

For small peak removal after main droplets clustering in TF mode for DCM

	•		•	J	
bits	name	s/w	h/w	default	description
31:0	machineconstant s_clst_thr_pkva l_low_tfdcm_per c	rw	ro	0x199A	For small peak removal after main droplets clustering in TF mode for DCM

## 1.3.30 machineconstants\_clst\_thr\_dist2antinode\_tfd cm\_perc

Reg.

0xA0020074

Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing, DCM, TF mode

bits name s/w h/w default description

31:0	machineconstant s_clst_thr_dist 2antinode tfdcm	rw	ro	0x8000	Define region of interest (ROI), as function of distance to antinode, normalized by main droplet spacing, DCM, TF mode
	_perc				

1.3.3	1 machineconstants	Reg.	0xA0020078							
Threshold for D to calculate mult-satellite ratio										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_clst_multsatr ate_dthr	rw	ro	0x0	Threshold for D to	atellite ratio				

1.3.3	2 machineconstants	max	Reg.	0xA002007C						
Maximum allowed pkValue before detecting pkSaturation										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_clst_dcm_pkva lue_max	rw	ro	0x20000	Maximum allowed	owed pkValue before detecting pkSaturation				

1.3.3	3 machineconstants	Reg.	0xA0020080							
Maximum allowed pkValue before detecting pkSaturation										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_clst_ddm_pkva lue_max	rw	ro	0x20000	Maximum allowed	ed pkValue before detecting pkSaturation				

1.3.3	4 atomic_group1_er	Reg.	0xA0020084								
Atom	Atomic Group1 Enable SW writes 0x0000_0001 to transfer atomic group data to algo										
bits	name	s/w	h/w	default		description	n				
31:0	31:0 atomic_group1_e rw rw 0x0 Atomic Group1 Enable SW writes 0x0000_0001 to tr atomic group data to algo						0x0000_0001 to transfer				

1.3.3	5 req_func	Reg.	0xA0020088							
MSC requested function										
bits	name	s/w	h/w	default		description	ı			
31:0	req_func	MSC requested fu	ınction							

1.3.3	6 idcb_manual	Reg.	0xA002008C								
Manu	Manual trigger signal for IDCB channels										
bits	bits name s/w h/w default description										
31:0	idcb_manual	Manual trigger sig	lanual trigger signal for IDCB channels								

1.3.3	7 events_in_events_	Reg.	0xA0020090							
Acknowledgement signal from PS to clear events in bank1										
bits	name	s/w	h/w	default	description	n				
	events_in_event s_bank1_ack	rw	ro	0x0	Acknowledgement signal from PS	to clear events in bank1				

1.3.3	8 events_in_events_	Reg.	0xA0020094							
Acknowledgement signal from PS to clear events in bank2										
bits	name	s/w	h/w	default	description					
31:0	events_in_event s_bank2_ack	rw	ro	0x0	Acknowledgemen	t signal from PS t	to clear events in bank2			

1.3.3	9 disable_intermiter	Reg.	0xA0020098						
Disables subclupdates that may interfere with other CPDS									
bits	name	s/w	h/w	default	description				
31:0	disable_intermi tent_tuning	rw	ro	0x0	Disables subclupe	dates that may int	erfere with other CPDS		

1.3.4	0 ps2pl_cal_bdo_f2	Reg.	0xA002009C							
Base droplet optimization Optimal f2										
bits	name	s/w	h/w	default		description	٦			
31:0	ps2pl_cal_bdo_f 2_opt	rw	ro	0x0	Base droplet optir	mization Optimal f	2			

1.3.4	1 ps2pl_cal_bdo_dc	Reg.	0xA00200A0							
Base Droplet Optimization Optimum Duty Cycle										
bits	name	s/w	h/w	default	description					
31:0	ps2pl_cal_bdo_d c_opt	rw	ro	0x0	Base Droplet Opti	mization Optimur	n Duty Cycle			

1.3.4	2 ps2pl_cal_dcm_q	Reg.	0xA00200A4							
DCM Quality Check. 1-Pass, 0-Fail										
bits	name	s/w	h/w	default	description					
31:0	ps2pl_cal_dcm_q c_pass	rw	ro	0x1	DCM Quality Che	ck. 1-Pass, 0-Fail				

1.3.4	3 ps2pl_cal_ps_gen	Reg.	0xA00200A8							
PS General Error Register										
bits	name	s/w	h/w	default		description	ı			
31:0	ps2pl_cal_ps_ge neral_error_reg	rw	ro	0x0	PS General Error	Register				

1.3.4	4 ps2pl_cal_advcmo	Reg.	0xA00200AC							
Advanced command										
bits	name	s/w	h/w	default		descriptio	n			
31:0	ps2pl_cal_advcm d	rw	ro	0x0	Advanced comma	and				

1.3.45	ps2pl_cal_spare1	Reg.	0xA00200B0						
PS2PL spare signal									
bits	name	s/w	h/w	default		description			

1:0	ps2pl_cal_spare 1	rw	ro	0x0	PS2PL spare sig	nal	
.3.4	6 ps2pl_cal_spare2					Reg.	0xA00200B4
PS2I	PL spare signal						
bits	name	s/w	h/w	default			cription
1:0	ps2pl_cal_spare 2	rw	ro	0x0	PS2PL spare sig	nal	
.3.4	7 ps2pl_cal_spare3					Reg.	0xA00200B8
PS2I	PL spare signal						
bits	name	s/w	h/w	default			cription
1:0	ps2pl_cal_spare 3	rw	ro	0x0	PS2PL spare sig	nal	
.3.4	8 machineconstants	s_idc	_dphi	1		Reg.	0xA00200BC
inline	e Tuning parameter: dphi1						
bits	name	s/w	h/w	default			cription
1:0	machineconstant s_idc_dphi1	rw	ro	0x666	Inline Tuning par	ameter: dph	i1 
.3.4	9 machineconstants	s_idc	_dphi	0		Reg.	0xA00200C0
Inline	e Tuning parameter: dphi0						
bits	name	s/w	h/w	default		desc	cription
1:0	machineconstant s_idc_dphi0	rw	ro	0x666	Inline Tuning par	ameter: dph	iO
.3.5	0 machineconstants	s_idc	_pres	ubthersho	ld	Reg.	0xA00200C4
Inline	e Tuning parameter: preSu	ubThers	shold				
bits	name	s/w	h/w	default			cription
1:0	machineconstant s_idc_presubthe rshold	rw	ro	0xCCD	Inline Tuning par	ameter: pres	SubThershold
	1 machineconstants	s_idc	_pres	ubaverage	thershold	Reg.	0xA00200C8
.3.5			ageThe	ershold			
	e Tuning parameter: preSu	ubAvera	J				
Inline bits	name	s/w	h/w	default			cription
Inline bits	name machineconstant s_idc_presubave		-	default 0x147AE14	Inline Tuning par		cription SubAverageThershold
bits 1:0	name machineconstant s_idc_presubave ragethershold  2 machineconstants	s/w rw	h/w ro	0x147AE14			
bits 1:0	name machineconstant s_idc_presubave ragethershold  2 machineconstants	s/w rw	h/w ro	0x147AE14  Bsigmaaver		ameter: pre\$	SubAverageThershold
bits 51:0	name machineconstant s_idc_presubave ragethershold  2 machineconstants d	s/w rw	h/w ro	0x147AE14  Bsigmaaver	agedther	ameter: pres	SubAverageThershold

old			

	1.3.53 machineconstants_idc_satratioaveragethresho 0xA00200D0										
Inline Tuning parameter: satRatioAverageThreshold off droplet  bits name s/w h/w default description											
31:0	machineconstant s_idc_satratioa veragethreshold off	rw	ro	0x147AE14	description Inline Tuning parameter: satRatioAverageThreshold off droplet						

1.3.5	4 machineconstants	Reg.	0xA00200D4							
Inline Tuning parameter: satRatioThreshold										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_satratiot hreshold	rw	ro	0xCCD	Inline Tuning parameter: satRatioThreshold					

1.3.5	1.3.55 machineconstants_idc_monitoringcountermax 0xA00200D8											
Inline Tuning parameter: monitoringCounterMax												
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_idc_monitorin gcountermax	rw	ro	0x927C0	Inline Tuning para	ameter: monitorin	gCounterMax					

1.3.5	1.3.56 machineconstants_idc_monitorinitialcounter 0xA00200DC											
Inline Tuning parameter: monitorInitialCounter												
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_idc_monitorin itialcounter	rw	ro	0xA	Inline Tuning para	ameter: monitorIn	itialCounter					

1.3.5	7 machineconstants	Reg.	0xA00200E0									
Inline	Inline Tuning parameter: KL											
bits	name	s/w	h/w	default		description	า					
31:0 machineconstant rw ro 0x4000 Inline Tuning parameter: KL s_idc_kl												

1.3.5	8 machineconstant	Reg.	0xA00200E4									
Inline	Inline Tuning parameter: KT											
bits	name	s/w	h/w	default		descriptio	n					
31:0 machineconstant rw ro 0x4000 Inline Tuning parameter: KT s_idc_kt												

1.3.5	9 machineconstants	Reg.	0xA00200E8								
Inline	Inline Tuning parameter: KC										
bits	bits name s/w h/w default description										
31:0	machineconstant	rw	meter: KC								

s ido ko			
0_100_100			

1.3.6	0 machineconstants	Reg.	0xA00200EC								
Inline	Inline Tuning parameter: KD										
bits	name	s/w	h/w	default		description	n				
31:0 machineconstant rw ro 0xFFFC000 Inline Tuning parameter: KD s_idc_kd						meter: KD					

1.3.6	1 machineconstants	Reg.	0xA00200F0									
Inline	Inline Tuning parameter: LT											
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x4000 Inline Tuning parameter: LT s_idc_lt												

1.3.6	2 machineconstant	Reg.	0xA00200F4							
Inline Tuning parameter: TT										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_tt	rw	ro	0x2000	Inline Tuning para	ameter: TT				

1.3.6	3 machineconstants	Reg.	0xA00200F8							
Inline Tuning parameter: cT										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_idc_ct	rw	ro	0x4000	Inline Tuning parameter: cT					

1.3.6	4 machineconstants	Reg.	0xA00200FC							
Inline Tuning parameter: Target for DC/DPHI										
bits	name	s/w	h/w	default		description	ı			
31:0	machineconstant s_idc_dt	rw	ro	0xFFFFF000	Inline Tuning para	meter: Target for	DC/DPHI			

1.3.6	5 machineconstants	Reg.	0xA0020100							
Inline Tuning parameter: Desired DC/DPHI										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_idc_td	rw	ro	0xFFFFE666	Inline Tuning para	meter: Desired D	C/DPHI			

1.3.6	6 machineconstants	Reg.	0xA0020104							
Inline Tuning parameter: d Threshold										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_idc_d_thr	rw	ro	0x0	Inline Tuning para	ameter: d Thresho	old			

1.3.67 machineconstants_idc_maincliteration	Reg.	0xA0020108
Inline Tuning parameter: MainCLIteration		

bits	name	s/w	h/w	default	description
-	machineconstant s_idc_mainclite ration	rw	ro	0x64	Inline Tuning parameter: MainCLIteration

1.3.6	1.3.68 machineconstants_idc_tuningintervalstimemax 0xA002010C										
Inline Tuning parameter: tuningIntervalsTimeMax											
bits	name	s/w	h/w	default	description						
	machineconstant s_idc_tuningint ervalstimemax	rw	ro	0xA	Inline Tuning para	arameter: tuningIntervalsTimeMax					

1.3.6	1.3.69 machineconstants_idc_phasecorrectionphi0 0xA0020110										
Inline Tuning parameter: phaseCorrectionPhi0											
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_idc_phasecorr ectionphi0	rw	ro	0x19A	Inline Tuning para	e Tuning parameter: phaseCorrectionPhi0					

1.3.70 machineconstants_idc_phasecorrectionphi1 0xA0020114										
Inline Tuning parameter: phaseCorrectionPhi1										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_idc_phasecorr ectionphi1	rw	ro	0x19A	Inline Tuning parameter: phaseCorrectionPhi1					

1.3.7	1 machineconstants	ction	Reg.	0xA0020118						
Inline Tuning parameter: amplitudeReduction										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_idc_amplitude reduction	rw	ro	0x39A	Inline Tuning para	uning parameter: amplitudeReduction				

1.3.7	2 machineconstants	Reg.	0xA002011C							
Inline Tuning parameter: A0Max										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_idc_a0max	rw	ro	0x5000	Inline Tuning parameter: A0Max					

1.3.7	3 machineconstants	Reg.	0xA0020120							
Inline Tuning parameter: A0Min										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_a0min	rw	ro	0x66	Inline Tuning para	ameter: A0Min				

1.3.74	machineconstants	Reg.	0xA0020124							
Inline 7	Inline Tuning parameter: A1Max									
bits	name	description	n							

31:0	machineconstant	rw	ro	0x5000	Inline Tuning parameter: A1Max
	s idc a1max				

1.3.7	5 machineconstants	Reg.	0xA0020128							
Inline Tuning parameter: A1Min										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_a1min	rw	ro	0x66	Inline Tuning para	ameter: A1Min				

1.3.7	6 machineconstants	Reg.	0xA002012C							
Inline Tuning parameter: voltageMax										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_voltagema x	rw	ro	0x10400	Inline Tuning para	meter: voltageMa	ax			

1.3.7	7 machineconstants	Reg.	0xA0020130							
Inline Tuning parameter: LMargin										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_lmargin	rw	ro	0x28F	Inline Tuning para	ameter: LMargin				

1.3.7	8 machineconstants	Reg.	0xA0020134							
Inline Tuning parameter: TMargin										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_tmargin	rw	ro	0x28F	Inline Tuning para	ameter: TMargin				

1.3.7	9 machineconstan	Reg.	0xA0020138								
Inline Tuning parameter: CMargin											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_idc_cmargin	rw	ro	0x28F	Inline Tuning parameter: CMargin						

1.3.8	0 machineconstants	Reg.	0xA002013C							
Inline Tuning parameter: Margin for DCDPHI										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_idc_dmargin	rw	ro	0x28F	Inline Tuning parameter: Margin for DCDPHI					

1.3.8	1 machineconstants	Reg.	0xA0020140								
Inline Tuning parameter: subCLCounterMax											
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_idc_subclcoun termax	rw	ro	0xA	Inline Tuning parameter: subCLCounterMax						

1.3.8 d	1.3.82 machineconstants_idc_peakmissedratethreshol 0xA0020144										
Inline Tuning parameter: peakMissedRateThreshold											
bits	name	s/w	h/w	default		descriptior	า				
31:0	machineconstant s_idc_peakmisse dratethreshold	rw	ro	0xCCD	Inline Tuning para	ameter: peakMiss	edRateThreshold				

1.3.8	1.3.83 machineconstants_idc_multsatratiothreshold 0xA0020148										
Inline	Inline Tuning parameter: multSatRatioThreshold										
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_idc_multsatra tiothreshold	rw	ro	0xCCD	Inline Tuning parameter: multSatRatioThreshold						

1.3.8	4 machineconstants	Reg.	0xA002014C								
Inline Tuning parameter: sigmaCThreshold											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_idc_sigmacthr eshold	rw	ro	0xCCD	Inline Tuning para	ne Tuning parameter: sigmaCThreshold					

1.3.8	5 machineconstants	Reg.	0xA0020150								
Inline Tuning parameter: sigmaLThreshold											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_idc_sigmalthr eshold	rw	ro	0x148	1						

1.3.86 machineconstants_idc_falltimedetectionmax 0xA0020154											
Inline Tuning parameter: exposureMonitorIterationMax											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_idc_falltimed etectionmax	rw	ro	0x3E8	Inline Tuning parameter: exposureMonitorIterationMax						

1.3.8	7 machineconstants	Reg.	0xA0020158								
Inline Tuning parameter: Averaging Length											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_idc_averaging length	rw	ro	0x7D0	Inline Tuning parameter: Averaging Length						

1.3.8	1.3.88 machineconstants_idc_maincl_holdoffcounter 0xA002015C											
Inline Tuning parameter: MainCL update holdoff												
bits	bits name s/w h/w default description											
31:0	machineconstant s_idc_maincl_ho ldoffcounter	rw	ro	0x7	Inline Tuning para	ameter: Mair	nCL update holdoff					

1.3.8 r	1.3.89 machineconstants_idc_subclopt_holdoffcounte										
Inline	Inline Tuning parameter: SubCL Update Opt Holdoff										
bits	name	s/w	h/w	default	description	n					
31:0	31:0 machineconstant rw ro 0x5 Inline Tuning parameter: SubCL Update Opt Holdoff s_idc_subclopt_holdoffcounter										

1.3.9	1.3.90 machineconstants_idc_subclbk_holdoffcounter 0xA0020164											
Inline Tuning parameter: SubCL Bk Update Holdoff												
bits	name	s/w	h/w	default	t description							
31:0	machineconstant s_idc_subclbk_h oldoffcounter	rw	ro	0x7	Inline Tuning para	ameter: SubCL Bl	CUpdate Holdoff					

	1.3.91 machineconstants_idc_exposure_earlyexposure 0xA0020168 threshold											
Expo	Exposure parameter: Early Exposure Threshold  bits name s/w h/w default description											
31:0	machineconstant s_idc_exposure_ earlyexposureth reshold	rw	ro	0x0	Exposure parame	•						

1.3.9	2 machineconstants	Reg.	0xA002016C								
Configuration word for IDCB Triggers											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_idc_idcbtrigg erconfig	rw	ro	0x0	Configuration word for IDCB Triggers						

1.3.9 amp	1.3.93 machineconstants_idc_monitoringcountersafed amp 0xA0020170											
Numb	Number of iterations to wait in monitoring before updating SafeDAMP											
DIIS	name	s/w	h/w	default		description						
31:0	machineconstant s_idc_monitorin gcountersafedam p	rw	ro	0xB	Number of iterations to wait in monitoring before updating SafeDAMP							

1.3.9 term	4 machineconstant ax	s_idc_	toringcoun	Reg.	0xA0020174							
Numl	Number of iterations to wait for exposure signal to go high											
	name	s/w	h/w	default		description						
31:0	machineconstant s_idc_exposurem onitoringcounte rmax	rw	ro	0xA	Number of iteration	ons to wait for exp	osure signal to go high					

1.3.9	1.3.95 machineconstants_idc_dcmbpam2dtec_crcerrthr 0xA0020178											
Threshold for CRC errors coming from DCM BPAM												
bits	name	s/w	h/w	default	lt description							
31:0	machineconstant s_idc_dcmbpam2d tec_crcerrthr	rw	ro	0x6	Threshold for CR0	C errors coming f	rom DCM BPAM					

1.3.9	1.3.96 machineconstants_idc_ddmbpam2dtec_crcerrthr 0xA002017C										
Threshold for CRC errors coming from DDM BPAM											
bits	name	s/w h/w default description									
31:0	machineconstant s_idc_ddmbpam2d tec_crcerrthr	rw	ro	0x6	Threshold for CR	C errors coming f	rom DDM BPAM				

	1.3.97 machineconstants_idc_dcmbpam2dtec_minnumval dpks_thr 0xA0020180											
Thres	Threshold for minimum number of valid PDS packets coming from DCM BPAM											
bits	name	s/w	h/w	default	description	1						
31:0	machineconstant s_idc_dcmbpam2d tec_minnumvalid pks_thr	rw	ro	0x32	Threshold for minimum number of valid PDS packets coming from DCM BPAM							

	1.3.98 machineconstants_idc_ddmbpam2dtec_minnumval constants_idc_ddmbpam2dtec_minnumval constants_idc_ddmbpam2dtec_minnumv											
	Threshold for minimum number of valid PDS packets coming from DDM BPAM											
bits	name	s/w	h/w	default		description	า					
31:0	machineconstant s_idc_ddmbpam2d tec_minnumvalid pks_thr	rw	ro	0x32	Threshold for minimum number of valid PDS packets coming from DDM BPAM							

1.3.99 machineconstants_idc_dcm_signallevel_min 0xA0020188										
Threshold for lower value for median of main peaks for DCM										
bits	bits name s/w h/w default description									
	machineconstant s_idc_dcm_signa llevel_min	rw	ro	0x6666	Threshold for lower value for median of main peaks for DCM					

1.3.1	1.3.100 machineconstants_idc_ddm_signallevel_min 0xA002018C										
Thres	Threshold for lower value for median of main peaks for DDM										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_idc_ddm_signa llevel_min	rw	ro	0x4CCD	Threshold for lower value for median of main peaks for DDM						

1.3.1	01 machineconstan	Reg.	0xA0020190						
Holdoff before triggering the next offaxismain check									
bits	name	s/w	h/w	default		description	١		
31:0	machineconstant	rw	Holdoff before trig	gering the next of	ffaxismain check				

s_idc_phi0margi			
nholdoff			

1.3.1	02 machineconstant	untermax	Reg.	0xA0020194								
Numb	Number of consecutive DCM Quality fails allowed in monitoring											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_idc_dcmqualit ycountermax	rw	ro	0xA	Number of consecutive DCM Quality fails allowed in more toring							

1.3.1	03 machineconstant	Reg.	0xA0020198									
Numb	Number of consecutive DDM Quality fails allowed in monitoring											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_idc_ddmqualit ycountermax	rw	ro	0xA	Number of consecutive DDM Quality fails allowed in monitoring							

1.3.1	1.3.104 machineconstants_idc_healthsignals_config 0xA002019C										
Enables/Disables HW communication and health checks											
bits	name	s/w h/w default description									
31:0	machineconstant s_idc_healthsig nals_config	rw	ro	0xFF	Enables/Disables HW communication and health checks						

1.3.105 machineconstants_idc_oavsub_phi1marginres 0xA00201A0										
Off Axis Sub: idc_oavsub_phi1marginres										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_oavsub_ph i1marginres	rw	ro	0xCD	Off Axis Sub: idc_oavsub_phi1marginres					

1.3.106 machineconstants_idc_oavsub_phi1marginnum 0xA00201A4											
Off Axis Sub: idc_oavsub_phi1marginnum											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_idc_oavsub_ph i1marginnum	rw	ro	0x5	Off Axis Sub: idc_oavsub_phi1marginnum						

1.3.107 machineconstants_idc_oavsub_ddmlatency 0xA00201A8											
Off Axis Sub: idc_oavsub_ddmlatency											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_idc_oavsub_dd mlatency	rw	ro	0x3	Off Axis Sub: idc_oavsub_ddmlatency						

1.3.108 machineconstants_idc_oavmain_phi0marginres 0xA00201AC											
Off Axis N	Off Axis Main: idc_oavmain_phi0marginres										
bits name s/w h/w default description											

31:0	machineconstant	rw	ro	0xCD	Off Axis Main: idc_oavmain_phi0marginres
	s_idc_oavmain_p				
	hi0marginres				

1.3.1	1.3.109 machineconstants_idc_oavmain_phi0marginnum											
Off Axis Main: idc_oavmain_phi0marginnum												
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_idc_oavmain_p hi0marginnum	rw	ro	0x5	Off Axis Main: idc	f Axis Main: idc_oavmain_phi0marginnum						

1.3.1	10 machineconstan		Reg.	0xA00201B4								
Off ax	Off axis velocity state configuration word. Enables or disable new off axis states											
bits	name	s/w h/w default description										
31:0	machineconstant s_idc_oav_confi g	rw	ro	0x0	Off axis velocity state configuration word. Enables or disal new off axis states							

	1.3.111 machineconstants_idc_coveragesourcereprate 0xA00201B8perc											
	Percentage coverage of source rep rate band with nozzle operating band (at TF = idc_TF_coverage_operatingband_thr)											
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x199A Percentage coverage of source rep rate band with nozzle operating band (at TF = idc_TF_coverage_operatingband_thr)												

	1.3.112 machineconstants_idc_tf_coverage_operating 0xA00201BC band_thr											
Thres	Threshold for coverage of source rep rate band with nozzle operating band											
bits	name	s/w	h/w	default		description	1					
31:0	machineconstant s_idc_tf_covera ge_operatingban d_thr	rw	ro	0x199A	Threshold for coverage of source rep rate band with nozzle operating band							

1.3.1	1.3.113 machineconstants_idc_workingsubclfreqs 0xA00201C0											
Number of working sub-coalescence frequencies after initial calibration (voltage > idc_workingsubclvoltage_thr)												
bits	name	s/w	h/w	default		description						
31:0	machineconstant s_idc_workingsu bclfreqs	rw	ro	0x1	Number of workin calibration (voltag		ce frequencies after initial ubclvoltage_thr)					

1.3.1 hr	1.3.114 machineconstants_idc_workingsubclvoltage_t hr										
Threshold for voltage of working sub-cl frequencies after initial calibration											
bits	name	s/w	h/w	default	descr	iption					
31:0	machineconstant s_idc_workingsu bclvoltage_thr	rw	ro	0x1	Threshold for voltage of working sub-cl frequencies after initial calibration						

	1.3.115 machineconstants_idc_satratioaveragethresh oxA00201C8											
Inline	Inline Tuning parameter: satRatioAverageThreshold on droplet											
bits	bits name s/w h/w default description											
31:0	machineconstant s_idc_satratioa veragethreshold _on	rw	ro	0x999999A	Inline Tuning parameter: satRatioAverageThreshold on droplet							

1.3.1	16 machineconstant	Reg.	0xA00201CC									
Time	Time in ms that DDM can be down before rising an error											
bits	name	s/w	h/w	default		descriptio	n					
31:0	machineconstant s_idc_ddmdownti me	rw	ro	0x927C0	Time in ms that DDM can be down before rising an erro							

1.3.1	17 machineconstant	Reg.	0xA00201D0							
Treshold for DCM BL value before reporting an error										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_idc_dcm_bl_th r	rw	ro	0x10000	Treshold for DCM BL value before reporting an error					

1.3.1	18 machineconstant		Reg.	0xA00201D4					
Tresh	Treshold for DDM BL value before reporting an error								
bits	name	s/w h/w default				description			
31:0	machineconstant s_idc_ddm_bl_th r	rw	ro	0x10000	Treshold for DDM	I BL value before	reporting an error		

1.3.1 hr	.3.119 machineconstants_idc_dcm_missingdroplets_t									
Tresh	Treshold for DCM number of missed main droplets value before reporting an error bits name s/w h/w default description									
31:0	machineconstant s_idc_dcm_missi ngdroplets_thr	rw	ro	0xA	Treshold for DCM number of misse before reporting an error					

1.3.1 hr	.3.120 machineconstants_idc_ddm_missingdroplets_t										
Tresh	Treshold for DDM number of missed main droplets value before reporting an error										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_idc_ddm_missi ngdroplets_thr	rw	ro	0xA	Treshold for DDN before reporting a		ed main droplets value				

1.3.121 machineconstants_idc_exposureoff_holdoffco	Reg.	0xA00201E0
unter		

Amou	Amount of time the satrate will be ignored before starting the satrateaverage for off droplet									
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_idc_exposureo ff_holdoffcount er	rw	ro	0x1	Amount of time the satrate will be ignored before starting the satrateaverage for off droplet					

1.3.1 nter	22 machineconstan	ts_ido	noldoffcou	Reg.	0xA00201E4				
Amou	Amount of time before risetime that satrate would be ignored to calculate satrate off droplet  bits name s/w h/w default description								
31:0	machineconstant s_idc_exposureo n_holdoffcounte r	rw	ro	0x1	Amount of time be nored to calculate	fore risetime that	satrate would be ig-		

1.3.1	.3.123 machineconstants_idc_dcm_pksaturation_thr 0xA00201E8									
PkSa	PkSaturation Rate threshold used to measure dcm quality									
bits	name	s/w h/w default description								
31:0	machineconstant s_idc_dcm_pksat uration_thr	rw	ro	0x10000	PkSaturation Rat	e threshold used	to measure dcm quality			

1.3.1	.3.124 machineconstants_idc_ddm_pksaturation_thr 0xA00201EC									
PkSa	PkSaturation Rate threshold used to measure ddm quality									
bits	name	s/w h/w default description								
31:0	machineconstant s_idc_ddm_pksat uration_thr	rw	ro	0x10000	PkSaturation Rate	e threshold used	to measure ddm quality			

1.3.1	25 machineconstant	Reg.	0xA00201F0							
idc_e	idc_enable_ddm_violations									
bits	name	s/w		description						
31:0	machineconstant s_idc_spcfg_03	rw	ro	0x3	idc_enable_ddm_	violations				

1.3.1	26 machineconstant	Reg.	0xA00201F4							
clst_e	clst_enable_dcm_signallevel									
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_idc_spcfg_04	rw	ro	0x1	clst_enable_dcm_	_signallevel				

1.3.1	27 machineconstan	Reg.	0xA00201F8							
idc_o	idc_offaxissub_holdoff									
bits	name	s/w	h/w	default		description				
31:0	machineconstant s_idc_spcfg_05	rw	ro	0x8	idc_offaxissub_hc	oldoff				

## 1.3.128 machineconstants\_idc\_spcfg\_06 0xA00201FC

idc_re	idc_recovery_holdoff								
bits	name	s/w	h/w	default	description				
31:0	machineconstant s_idc_spcfg_06	rw	ro	0xEA60	idc_recovery_holdoff				

1.3.1	29 machineconstant	Reg.	0xA0020200									
idc_o	idc_offaxismain_holdoff											
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x8 idc_offaxismain_holdoff s_idc_spcfg_07												

1.3.1	30 machineconstant	Reg.	0xA0020204								
idc_ti	idc_timebetweenrecoveries_thr										
bits	name	s/w	h/w	default		description	٦				
31:0 machineconstant rw ro 0x493E0 idc_timebetweenrecoveries_thr s_idc_spcfg_08											

1.3.1	31 machineconsta	Reg.	0xA0020208								
idc_allowedrecoveries_thr											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_idc_spcfg_09	rw	ro	0x3	idc_allowedrecov	eries_thr					

1.3.1	32 machineconstan	Reg.	0xA002020C								
idc_monitoringdcrejection_time											
bits	name	s/w	h/w	default		description	n				
31:0 machineconstant rw ro 0xEA60 idc_monitoringdcrejection_time s_idc_spcfg_10											

1.3.1	33 machineconstant	Reg.	0xA0020210								
idc_exposurerecoverytransition_countermax											
bits	name	s/w	h/w	default		description	1				
31:0 machineconstant rw ro 0xA idc_exposurerecoverytransition_countermax s_idc_spcfg_11											

1.3.1	34 machineconstan	Reg.	0xA0020214								
idc_timebetweenrecoveries_etecnok_thr											
bits	name	s/w	h/w	default		description	า				
31:0 machineconstant rw ro 0xA1220 idc_timebetweenrecoveries_etecnok_thr s_idc_spcfg_12											

1.3.1	35 machineconstan	Reg.	0xA0020218									
idc_w	idc_workingdcperc											
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x0 idc_workingdcperc s_idc_spcfg_13												

		nts_id					
idc_e	expmon_qualitycounterm	ax					
bits	name	s/w	h/w	default			scription
31:0	machineconstant s_idc_spcfg_14	rw	ro	0xA	idc_expmon_qua	litycounter	rmax
1.3.1	37 machineconsta	nts_id	_spo	cfg_15		Reg.	0xA0020220
idc_c	ountfromlastsubclupmax						
bits 31:0	name machineconstant s_idc_spcfg_15	s/w rw	h/w ro	default 0x927C0	idc_countfromlas		scription ax
1.3.1	38 machineconsta	nts_ido	c_spo	cfg_16		Reg.	0xA0020224
Spar	e Signal						
bits	name	s/w	h/w	default		de	scription
31:0	machineconstant s_idc_spcfg_16	rw	ro	0x0	Spare Signal		
1 2 1	20 maahinaaanata	nto ida	2 0 0 0	of a 17		Reg.	0xA0020228
	39 machineconsta	าเร_เนเ	;_sp	sig_i <i>t</i>			02020220
bits	e Signal name	s/w	h/w	default		do	scription
31:0	machineconstant s_idc_spcfg_17	rw	ro	0x0	Spare Signal	ue	scription
1.3.1	40 machineconsta	nts_ido	c_spo	cfg_18		Reg.	0xA002022C
	e Signal						
bits	name	s/w	h/w	default	0	de	scription
31:0	machineconstant s_idc_spcfg_18	rw	ro	0x0	Spare Signal		
1.3.1	41 machineconsta	nts_id	c_spo	cfg_19		Reg.	0xA0020230
Spar	e Signal						
bits	name	s/w	h/w	default		de	scription
31:0	machineconstant s_idc_spcfg_19	rw	ro	0x0	Spare Signal		
1.3.1	42 machineconsta	nts_id	c_sp	cfg_20		Reg.	0xA0020234
mvp_	ignoreexpgate						
	name	s/w	h/w	default		de	scription
bits 31:0	machineconstant			0x0	mvp_ignoreexpga		

ype

0xA0020238

Reg.

1.3.143 machineconstants\_cmd\_manualtuningwaveformt

Sets the waveform type during manual mode

bits	name	s/w	h/w	default	description
	machineconstant s_cmd_manualtun ingwaveformtype	rw	ro	0x0	Sets the waveform type during manual mode

1.3.1	44 machineconstan	Reg.	0xA002023C									
2sine	2sine-square Waveform duty cycle											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_cmd_tssw_duty cycle	rw	ro	0xA	2sine-square Wa	veform duty cycle						

1.3.1	45 machineconstant	Reg.	0xA0020240							
2sine-square Waveform RiseTime										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_cmd_tssw_rise time	rw	ro	0x0	2sine-square Wav	eform RiseTime				

1.3.1	1.3.146 machineconstants_cmd_tssw_sineamplitude0 0xA0020244											
2sine-square Waveform SineAmpliude0												
bits	name	s/w	h/w	default	description							
31:0	machineconstant s_cmd_tssw_sine amplitude0	rw	ro	0x1400	2sine-square Wav	veform SineAmpli	ude0					

1.3.1	1.3.147 machineconstants_cmd_tssw_sineamplitude1 0xA0020248											
2sine	2sine-square Waveform SineAmpliude1											
bits	bits name s/w h/w default description											
31:0	machineconstant s_cmd_tssw_sine amplitude1	rw	ro	0x1400	2sine-square Waveform SineAmpliude1							

1.3.148 machineconstants_cmd_tssw_sinefrequency 0xA002024C											
2sine-square Waveform SineFrequency											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cmd_tssw_sine frequency	rw	ro	0x3A98000	2sine-square Waveform SineFrequency						

1.3.1 tiplie	49 machineconstant r	Reg.	0xA0020250									
2sine	2sine-square Waveform SineFrequencyMultiplier											
bits	name	s/w	h/w	default		description	า					
31:0	machineconstant s_cmd_tssw_sine frequencymultip lier	rw	ro	0x2800	2sine-square Waveform SineFrequencyMultiplier							

1.3.1	50 machineconstant	Reg.	0xA0020254									
2sine	2sine-square Waveform SinePhase0											
bits	bits name s/w h/w default description											
31:0	machineconstant s_cmd_tssw_sine phase0	rw	ro	0x0	2sine-square Wa	e-square Waveform SinePhase0						

1.3.151 machineconstants_cmd_tssw_sinephase1 0xA0020258												
2sine	2sine-square Waveform SinePhase1											
bits	name	s/w	h/w	default		description	ı					
31:0	machineconstant s_cmd_tssw_sine phase1	rw	ro	0x0	2sine-square Waveform SinePhase1							

1.3.1	1.3.152 machineconstants_cmd_tssw_squareamplitude 0xA002025C											
2sine-square Waveform SquareAmplitude												
bits	bits name s/w h/w default description											
31:0	machineconstant s_cmd_tssw_squa reamplitude	rw	ro	0x800	2sine-square Waveform SquareAmplitude							

1.3.1 ultipl	53 machineconstan ier	Reg.	0xA0020260									
	2sine-square Waveform SquareFrequencyMultiplier											
bits	name	s/w	h/w	default		description	า					
31:0	machineconstant s_cmd_tssw_squa refrequencymult iplier	rw	ro	0x1000	2sine-square Waveform SquareFrequencyMultiplier							

1.3.1	54 machineconstan	Reg.	0xA0020264									
Startı	Startup Waveform duty cycle											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_cmd_stup_duty cycle	rw	ro	0xA	Startup Waveforn	n duty cycle						

1.3.1	55 machineconstant	Reg.	0xA0020268									
Startu	Startup Waveform RiseTime											
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x0 Startup Waveform RiseTime s_cmd_stup_rise time												

1.3.1	1.3.156 machineconstants_cmd_stup_sineamplitude0 0xA002026C											
Startı	Startup Waveform SineAmpliude0											
bits	bits name s/w h/w default description											
31:0 machineconstant rw ro 0x400 Startup Waveform SineAmpliude0  s_cmd_stup_sine amplitude0												

1.3.1	.3.157 machineconstants_cmd_stup_sineamplitude1 0xA0020270											
Startu	Startup Waveform SineAmpliude1											
bits	bits name s/w h/w default description											
31:0	machineconstant s_cmd_stup_sine amplitude1	rw	ro	0x400	Startup Waveform	SineAmpliude1						

1.3.1	58 machineconstant	Reg.	0xA0020274									
Startu	Startup Waveform SineFrequency											
bits	bits name s/w h/w default description											
31:0	machineconstant s_cmd_stup_sine frequency	rw	ro	0x3C8C000	Startup Waveform SineFrequency							

1.3.1 tiplie	59 machineconstant r	quencymul	Reg.	0xA0020278							
Startup Waveform SineFrequencyMultiplier											
bits	name	s/w	h/w	default		descriptior	า				
31:0	machineconstant s_cmd_stup_sine frequencymultip lier	rw	ro	0x2800	Startup Waveform SineFrequencyMultiplier						

1.3.1	60 machineconstan	Reg.	0xA002027C							
Startup Waveform SinePhase0										
bits	name	s/w	h/w	default		description				
31:0	machineconstant s_cmd_stup_sine phase0	rw	ro	0x0	Startup Waveform SinePhase0					

1.3.1	61 machineconstar	Reg.	0xA0020280							
Startup Waveform SinePhase1										
bits	name	s/w	h/w	default		descriptio	n			
31:0	machineconstant s_cmd_stup_sine phase1	rw	ro	0x0	Startup Waveform SinePhase1					

1.3.1	62 machineconstan	ts_cn	eamplitude	Reg.	0xA0020284							
Startı	Startup Waveform SquareAmplitude											
bits	name	s/w	h/w	default		description	1					
31:0	machineconstant s_cmd_stup_squa reamplitude	rw	ro	0x1000	Startup Waveform SquareAmplitude							

1.3.163 ma ultiplier	chineconsta	frequencym Reg.	0xA0020288								
Startup Wave	Startup Waveform SquareFrequencyMultiplier										
bits	name s/w h/w default description										

31:0	machineconstant	rw	ro	0x1000	Startup Waveform SquareFrequencyMultiplier
	s_cmd_stup_squa				
	refrequencymult				
	iplier				

1.3.1	64 machineconstan	е	Reg.	0xA002028C						
Hybrid waveform DutyCycle										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_cmd_hw_dutycy cle	rw	ro	0xA	Hybrid waveform DutyCycle					

1.3.1	65 machineconstant	Reg.	0xA0020290							
Hybrid waveform RiseTime										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_cmd_hw_riseti me	rw	ro	0x2AF31DC	Hybrid waveform RiseTime					

1.3.1	66 machineconstan	Reg.	0xA0020294							
Hybrid waveform SineAmplitude										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_cmd_hw_sineam plitude	rw	ro	0x1400	Hybrid waveform SineAmplitude					

1.3.1	67 machineconstan	ts_cm	uency	Reg.	0xA0020298					
Hybrid waveform SineFrequency										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_cmd_hw_sinefr equency	rw	ro	0x3A98000	Hybrid waveform SineFrequency					

1.3.1	68 machineconstar	Reg.	0xA002029C							
Hybrid waveform SquareAmplitude										
bits	name	s/w	h/w	h/w default description						
31:0	machineconstant s_cmd_hw_square amplitude	rw	ro	0x800	Hybrid waveform SquareAmplitude					

1.3.1 tiplie	69 machineconstan r	requencymul	Reg.	0xA00202A0									
Hybri	Hybrid waveform SquareFrequencyMultiplier												
bits	name	s/w	h/w	default		description	1						
31:0	machineconstant s_cmd_hw_square frequencymultip lier	rw	ro	0x1000	Hybrid waveform SquareFrequencyMultiplier								

1.3.1	1.3.170 machineconstants_cmd_hw_squarephase 0xA00202A4												
Hybrid waveform SquarePhase													
bits	bits name s/w h/w default description												
31:0 machineconstant rw ro 0x0 Hybrid waveform SquarePhase s_cmd_hw_square phase													

1.3.1	1.3.171 machineconstants_cmd_sw_dutycycle 0xA00202A8											
Squa	Square DutyCycle											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_cmd_sw_dutycy cle	rw	ro	0xA	Square DutyCycle	e						

1.3.1	72 machineconstant	Reg.	0xA00202AC								
Squa	Square RiseTime										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cmd_sw_riseti me	rw	ro	0x44B830	Square RiseTime						

1.3.1	1.3.173 machineconstants_cmd_sw_squareamplitude 0xA00202B0												
Squa	Square SquareAmplitude												
bits	bits name s/w h/w default description												
31:0	machineconstant s_cmd_sw_square amplitude	rw	ro	0x1400	Square SquareAmplitude								

1.3.174 machineconstants_cmd_sw_squarefrequency 0xA00202B4												
Square SquareFrequency												
bits	bits name s/w h/w default description											
31:0	machineconstant s_cmd_sw_square frequency	rw	ro	0x3A98000	Square SquareFrequency							

1.3.1	1.3.175 machineconstants_cmd_waveform_enable 0xA00202B8											
Wave	Waveform enable external cmd											
bits	name	s/w	h/w	default		description	า					
31:0	•											

1.3.1	76 machineconstant	Reg.	0xA00202BC								
Solut	Solution Table type: 0:2sineSquare, 1:HWO										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_solutiont ype	rw	Solution Table typ	e: 0:2sineSquare	, 1:HWO						

1.3.1	1.3.177 machineconstants_slt_hyperparameters_1											
Solution Table f0, N0, N1, As												
bits	name	s/w	h/w	default		descriptio	n					
31:0	31:0 machineconstant rw ro 0x3A98000 Solution Table f0, N0, N1, As s_slt_hyperpara meters_1											

1.3.1	1.3.178 machineconstants_slt_hyperparameters_2 0xA00202C4											
Solut	Solution Table f0, N0, N1, As											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_slt_hyperpara meters_2	rw	ro	0x2800	Solution Table f0, N0, N1, As							

1.3.1	1.3.179 machineconstants_slt_hyperparameters_3 0xA00202C8											
Solut	Solution Table f0, N0, N1, As											
bits	name	s/w	h/w	default		description	n					
31:0												

1.3.1	1.3.180 machineconstants_slt_hyperparameters_4 0xA00202CC											
Solution Table f0, N0, N1, As												
bits	s name s/w h/w default description											
31:0	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7											

1.3.1	81 machineconstant	Reg.	0xA00202D0							
Solution Table A0, A1										
bits	name	s/w	h/w	default		descriptio	n			
31:0	machineconstant s_slt_sineamps_ 1	rw	ro	0x1400	Solution Table A0	), A1				

1.3.1	82 machineconstan	Reg.	0xA00202D4								
Solution Table A0, A1											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_slt_sineamps_ 2	rw	ro	0x1400	Solution Table A0	, A1					

1.3.1	83 machineconstant		Reg.	0xA00202D8								
Solut	Solution table, phi0. DC 5											
bits	name	s/w	h/w	default		description	١					
31:0	machineconstant s_slt_phi0_1	rw	ro	0x0	Solution table, phi0. DC 5							

	84 machineconsta	nts_sit	_pni	J_ <b>Z</b>		Reg.	0xA00202DC
Solu	tion table, phi0. DC 10						
bits	name	s/w	h/w	default		des	cription
31:0	machineconstant	rw	ro	0x0	Solution table, ph		
	s_slt_phi0_2						
.3.1	85 machineconsta	nts_slt	_phi(	0_3		Reg.	0xA00202E0
Solu	tion table, phi0. DC 15						
bits	name	s/w	h/w	default		des	cription
31:0	machineconstant s_slt_phi0_3	rw	ro	0x0	Solution table, ph		
1.3.1	86 machineconsta	nts_slt	_phi	0_4		Reg.	0xA00202E4
Solu	tion table, phi0. DC 20						
bits	name	s/w	h/w	default		des	cription
1:0	machineconstant s_slt_phi0_4	rw	ro	0x0	Solution table, ph	i0. DC 20	
	87 machineconstation table, phi0. DC 25	nts_slt	_phi(	0_5		Reg.	0xA00202E8
	87 machineconsta	nts_slt	_phi(	<b>D_5</b>			0xA00202E8
Solu	87 machineconstation table, phi0. DC 25		•		Solution table, ph	des	0xA00202E8
Solu bits	87 machineconsta tion table, phi0. DC 25 name machineconstant	s/w	h/w	default	Solution table, ph	des	
Solu bits 31:0	87 machineconsta tion table, phi0. DC 25 name machineconstant	s/w rw	h/w ro	default 0x0	Solution table, ph	des	
Solu bits 31:0	87 machineconsta tion table, phi0. DC 25 name machineconstant s_slt_phi0_5	s/w rw	h/w ro	default 0x0	Solution table, ph	des	scription
Solu bits 31:0 1.3.1 Solu bits	87 machineconsta tion table, phi0. DC 25 name machineconstant s_slt_phi0_5  88 machineconsta tion table, phi0. DC 30 name	s/w rw	h/w ro	default 0x0		des ii0. DC 25	scription
Solu bits 31:0	87 machineconsta tion table, phi0. DC 25 name machineconstant s_slt_phi0_5  88 machineconsta tion table, phi0. DC 30	s/w rw	h/w ro	default 0x0	Solution table, ph	des ii0. DC 25	ocription  0xA00202EC
Solu bits 31:0 1.3.1 Solu bits	87 machineconsta tion table, phi0. DC 25 name machineconstant s_slt_phi0_5  88 machineconsta tion table, phi0. DC 30 name machineconstant	s/w rw	h/w ro	default 0x0		des ii0. DC 25	ocription 0xA00202EC
Solubits 31:0	87 machineconsta tion table, phi0. DC 25 name machineconstant s_slt_phi0_5  88 machineconsta tion table, phi0. DC 30 name machineconstant	s/w rw nts_slt	h/w ro _phi(	default 0x0  O_6  default 0x0		des ii0. DC 25	ocription 0xA00202EC
Solubits 31:0	87 machineconsta tion table, phi0. DC 25 name machineconstant s_slt_phi0_5  88 machineconsta tion table, phi0. DC 30 name machineconstant s_slt_phi0_6	s/w rw nts_slt	h/w ro _phi(	default 0x0  O_6  default 0x0		des ii0. DC 25	0xA00202EC
Solu bits 31:0  1.3.1  Solu bits 31:0	87 machineconsta tion table, phi0. DC 25 name machineconstant s_slt_phi0_5  88 machineconsta tion table, phi0. DC 30 name machineconstant s_slt_phi0_6  89 machineconsta	s/w rw nts_slt	h/w ro _phi(	default 0x0  O_6  default 0x0		desiio. DC 25  Reg. desiio. DC 30	0xA00202EC

h/w default

ro 0x0

s/w

rw

0xA00202F4

Reg.

Solution table, phi0. DC 40

description

1.3.190 machineconstants\_slt\_phi0\_8

Solution table, phi0. DC 40

31:0 machineconstant

s\_slt\_phi0\_8

name

bits

31:0	machineconstant	rw	ro	0x0	Solution table, phi0. DC 45	
	s_slt_phi0_9					
.3.1	92 machineconsta	ınts_slt	_phi	0_10	Reg.	0xA00202FC
Solu	tion table, phi0. DC 50					
bits 31:0	name machineconstant s_slt_phi0_10	s/w rw	h/w ro	default 0x0	desc Solution table, phi0. DC 50	cription
1.3.1	93 machineconsta	ınts slt	phi	n 11	Reg.	0xA0020300
	tion table, phi0. DC 55		_p	<u></u>		
bits	• •	s/w	h/w	default	desc	ription
31:0	machineconstant s_slt_phi0_11	rw	ro	0x0	Solution table, phi0. DC 55	,
1.3.1	94 machineconsta	nts_slt	_phi	0_12	Reg.	0xA0020304
Solu	tion table, phi0. DC 60					
bits		s/w	h/w	default		ription
31:0	machineconstant s_slt_phi0_12	rw	ro	0x0	Solution table, phi0. DC 60	
	tion table, phi0. DC 65	s/w	h/w	default	desc	0xA0020308 cription
31:0	machineconstant s_slt_phi0_13	rw	ro	0x0	Solution table, phi0. DC 65	
1.3.1	96 machineconsta	nts_slt	_phi	0_14	Reg.	0xA002030C
Solu	tion table, phi0. DC 70					
bits 31:0	name machineconstant s_slt_phi0_14	s/w rw	h/w ro	default 0x0	deso Solution table, phi0. DC 70	cription
1.3.1	97 machineconsta	ints slt	phi	0 15	Reg.	0xA0020310
	tion table, phi0. DC 75		_Piii			
bits	·	s/w	h/w	default	desc	ription
- WILD	machineconstant s_slt_phi0_15	rW	ro	0x0	Solution table, phi0. DC 75	, , , , , , , , , , , , , , , , , , ,
31:0						
31:0		inte elt	nhi	0 16	Reg.	0xA0020314
31:0 1.3.1	98 machineconsta	ınts_slt	_phi	0_16	Reg.	0xA0020314
31:0 1.3.1	98 machineconstation table, phi0. DC 80	ints_slt	_phi	0_16  default		0xA0020314

1.3.199 machineconstants\_slt\_phi0\_17

0xA0020318

Solut	Solution table, phi0. DC 85										
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_slt_phi0_17	rw	ro	0x0	Solution table, phi0. DC 85						

1.3.2	00 machineconstant	Reg.	0xA002031C									
Solution table, phi0. DC 90												
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x0 Solution table, phi0. DC 90 s_slt_phi0_18												

1.3.2	01 machineconstant	Reg.	0xA0020320									
Solut	Solution table, phi0. DC 95											
bits	name	s/w	h/w	default		description	า					
31:0 machineconstant rw ro 0x0 Solution table, phi0. DC 95 s_slt_phi0_19												

1.3.2	02 machineconstant	s_slt		Reg.	0xA0020324							
Solut	Solution Table, phi1 DC 5											
bits	name	s/w	h/w	default		description	ı					
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 5 s_slt_phi1_1												

1.3.2	03 machineconstant		Reg.	0xA0020328							
Solution Table, phi1 DC 10											
bits	name	s/w	h/w	default		description	n				
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 10 s_slt_phi1_2											

1.3.2	04 machineconstant	Reg.	0xA002032C										
Solut	Solution Table, phi1 DC 15												
bits	name	s/w	h/w	default		description	١						
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 15 s_slt_phi1_3													

1.3.2	05 machineconstai	Reg.	0xA0020330									
Solution Table, phi1 DC 20												
bits	name	s/w	h/w	default		description	า					
31:0	machineconstant s_slt_phi1_4	rw	ro	0x0	Solution Table, phi1 DC 20							

1.3.2	06 machineconstan	Reg.	0xA0020334									
Solution Table, phi1 DC 25												
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 25 s_slt_phi1_5												

Solut	ion Table, phi1 DC 30					
bits	name	s/w	h/w	default	desc	ription
31:0	machineconstant s_slt_phi1_6	rw	ro	0x0	Solution Table, phi1 DC 30	

1.3.208 machineconstants_slt_phi1_7 0xA002033C											
Solution Table, phi1 DC 35											
bits	name	s/w	h/w	default		description	n				
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 35 s_slt_phi1_7											

1.3.2	09 machineconstant	Reg.	0xA0020340								
Solution Table, phi1 DC 40											
bits	name	s/w	h/w	default		description	ı				
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 40 s_slt_phi1_8											

1.3.2	10 machineconstan	Reg.	0xA0020344								
Solution Table, phi1 DC 45											
bits	name	s/w	h/w	default		description	n				
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 45 s_slt_phi1_9											

1.3.2	11 machineconstant	Reg.	0xA0020348									
Solut	Solution Table, phi1 DC 50											
bits	name	s/w	h/w	default		description	ı					
31:0	2.22											

1.3.2	12 machineconstant	Reg.	0xA002034C									
Solut	Solution Table, phi1 DC 55											
bits	name	s/w	h/w	default		description	ı					
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 55 s_slt_phi1_11												

1.3.2	13 machineconstant	Reg.	0xA0020350								
Solution Table, phi1 DC 60											
bits	name	s/w	h/w	default		description	n				
31:0 machineconstant rw ro 0x0 Solution Table, phi1 DC 60 s_slt_phi1_12											

1.3.21	4 machineconstant	Reg.	0xA0020354						
Solution Table, phi1 DC 65									
bits name s/w h/w default description									

31:0	machineconstant	rw	ro	0x0	Solution Table, pl	hi1 DC 65	
	s_slt_phi1_13						
3 2	15 machineconstar	nte elt	nhi′	1 14		Reg.	0xA0020358
		113_311	_piii	'-'7			07.0.1002000
	ion Table, phi1 DC 70		. ,				
bits 31:0	name machineconstant	s/w rw	h/w ro	default 0x0	Solution Table, pl		cription
51.0	s_slt_phi1_14	1 00	10	OAO	Coldion Table, pi	111 00 70	
1.3.2	16 machineconstar	nts_slt	_phi′	1_15		Reg.	0xA002035C
Solut	ion Table, phi1 DC 75						
bits	name	s/w	h/w	default			cription
31:0	machineconstant	rw	ro	0x0	Solution Table, pl	ni1 DC 75	
	s_slt_phi1_15						
1.3.2	17 machineconstar	nts_slt	_phi′	1_16		Reg.	0xA0020360
Solut	ion Table, phi1 DC 80						
bits	name	s/w	h/w	default		des	cription
31:0	machineconstant s_slt_phi1_16	rw	ro	0x0	Solution Table, pl		
	18 machineconstar ion Table, phi1 DC 85	nts_slt	_phi′	1_17		Reg.	0xA0020364
bits	name	s/w	h/w	default			cription
31:0	machineconstant s_slt_phi1_17	rw	ro	0x0	Solution Table, pl	ni1 DC 85	
1.3.2	19 machineconstar	nts_slt	_phi′	1_18		Reg.	0xA0020368
Solut	ion Table, phi1 DC 90						
bits	name	s/w	h/w	default			cription
31:0	machineconstant s_slt_phi1_18	rw	ro	0x0	Solution Table, pl	hi1 DC 90	
1.3.2	20 machineconstar	nts_slt	_phi′	1_19		Reg.	0xA002036C
Solut	ion Table, phi1 DC 95						
bits	name	s/w	h/w	default			cription
31:0	machineconstant s_slt_phi1_19	rw	ro	0x0	Solution Table, pl	hi1 DC 95	
1.3.2	21 machineconstar	nts_slt	_pre	subcoal_fl	ag_1	Reg.	0xA0020370
Solut	ion Table, pre-subcoal fla	ag DC 5					
bits	name	s/w	h/w	default	Solution Table, p		cription
31:0	machineconstant	rw	ro	0x1			

s\_slt\_presubcoa l\_flag\_1

1.3.2	1.3.222 machineconstants_slt_presubcoal_flag_2 0xA0020374											
Solution Table, pre-subcoal flag DC 10												
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_slt_presubcoa l_flag_2	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 10					

1.3.223 machineconstants_slt_presubcoal_flag_3 0xA0020378											
Solut	Solution Table, pre-subcoal flag DC 15										
bits	name	s/w	h/w	default		description	٦				
31:0	machineconstant s_slt_presubcoa l_flag_3	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 15				

1.3.224 machineconstants_slt_presubcoal_flag_4 0xA002037C										
Solution Table, pre-subcoal flag DC 20										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_presubcoa l_flag_4	rw	ro	0x1	Solution Table, pre-subcoal flag DC 20					

1.3.225 machineconstants_slt_presubcoal_flag_5 0xA0020380										
Solut	Solution Table, pre-subcoal flag DC 25									
bits	name	s/w	h/w	default		descriptio	n			
31:0	machineconstant s_slt_presubcoa l_flag_5	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 25			

1.3.2	26 machineconstan	Reg.	0xA0020384						
Solution Table, pre-subcoal flag DC 30									
bits	name	s/w	h/w	default		description	n		
31:0	machineconstant s_slt_presubcoa l_flag_6	rw	ro	0x1	Solution Table, p	re-subcoal flag D0	C 30		

1.3.227 machineconstants_slt_presubcoal_flag_7 0xA0020388										
Solution Table, pre-subcoal flag DC 35										
bits	name	s/w	h/w	default		descriptio	n			
	machineconstant s_slt_presubcoa l_flag_7	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 35			

1.3.2	28 machineconstan	Reg.	0xA002038C						
Solution Table, pre-subcoal flag DC 40									
bits	name	s/w	h/w	default		descriptio	n		
31:0	machineconstant s_slt_presubcoa l_flag_8	rw	ro	0x1	Solution Table, p	e-subcoal flag D0	C 40		

1.3.2	1.3.229 machineconstants_slt_presubcoal_flag_9 0xA0020390										
Solution Table, pre-subcoal flag DC 45											
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_presubcoa l_flag_9	rw	ro	0x1	Solution Table, p	e-subcoal flag D0	C 45				

1.3.230 machineconstants_slt_presubcoal_flag_10 0xA0020394										
Solution Table, pre-subcoal flag DC 50										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_slt_presubcoa l_flag_10	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 50			

1.3.231 machineconstants_slt_presubcoal_flag_11 0xA0020398										
Solut	Solution Table, pre-subcoal flag DC 55									
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_presubcoa l_flag_11	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 55			

1.3.232 machineconstants_slt_presubcoal_flag_12 0xA002039C										
Solut	Solution Table, pre-subcoal flag DC 60									
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_slt_presubcoa l_flag_12	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 60			

1.3.233 machineconstants_slt_presubcoal_flag_13 0xA00203A0										
Solution Table, pre-subcoal flag DC 65										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_presubcoa l_flag_13	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 65			

1.3.2	1.3.234 machineconstants_slt_presubcoal_flag_14 0xA00203A4										
Solut	Solution Table, pre-subcoal flag DC 70										
bits	s name s/w h/w default description										
31:0	machineconstant s_slt_presubcoa l_flag_14	rw	ro	0x1	Solution Table, pr	e-subcoal flag D0	C 70				

1.3.235 machineconstants_slt_presubcoal_flag_15 0xA00203A8									
Solut	Solution Table, pre-subcoal flag DC 75								
bits	name	s/w	h/w	default		description	า		
31:0	machineconstant s_slt_presubcoa	rw	ro	0x1	Solution Table, pr	e-subcoal flag DC	C 75		

I flag 15		

1.3.2	1.3.236 machineconstants_slt_presubcoal_flag_16 0xA00203AC										
Solution Table, pre-subcoal flag DC 80											
bits	name	s/w h/w default description									
31:0	machineconstant s_slt_presubcoa l_flag_16	rw	ro	0x1	Solution Table, pre-subcoal flag DC 80						

1.3.2	1.3.237 machineconstants_slt_presubcoal_flag_17 0xA00203B0										
Solution Table, pre-subcoal flag DC 85											
bits	bits name s/w h/w default description										
31:0	machineconstant s_slt_presubcoa l_flag_17	rw	ro	0x1	Solution Table, pr	e-subcoal flag DC	C 85				

1.3.2	.3.238 machineconstants_slt_presubcoal_flag_18 0xA00203B4										
Solution Table, pre-subcoal flag DC 90											
bits	its name s/w h/w default description										
31:0	machineconstant s_slt_presubcoa l_flag_18	rw	ro	0x1	Solution Table, pre-subcoal flag DC 90						

1.3.2	1.3.239 machineconstants_slt_presubcoal_flag_19 0xA00203B8										
Solution Table, pre-subcoal flag DC 95											
bits	bits name s/w h/w default description										
31:0	machineconstant s_slt_presubcoa l_flag_19	rw	ro	0x1	Solution Table, p	e-subcoal flag D0	C 95				

1.3.2	40 machineconstant	Reg.	0xA00203BC								
Solution Table, Jitter Metric DC 5											
bits name s/w h/w default description											
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 5 s_slt_jitter_1											

1.3.2	1.3.241 machineconstants_slt_jitter_2 0xA00203C0										
Solut	Solution Table, Jitter Metric DC 10										
bits	bits name s/w h/w default description										
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 10 s_slt_jitter_2											

1.3.2	0xA00203C4									
Solution Table, Jitter Metric DC 15										
bits name s/w h/w default description										
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 15 s_slt_jitter_3										

Solution Table, Jitter Metric DC 20  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 20  s slt iitter 4	1.3.2	43 machineconstan	Reg.	0xA00203C8								
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 20	Solution Table, Jitter Metric DC 20											
	bits name s/w h/w default description											
	31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 20 s_slt_jitter_4											

1.3.2	0xA00203CC										
Solut	Solution Table, Jitter Metric DC 25										
bits name s/w h/w default description											
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 25 s_slt_jitter_5											

1.3.2	45 machineconstant	Reg.	0xA00203D0								
Soluti	Solution Table, Jitter Metric DC 30										
bits name s/w h/w default description											
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 30 s_slt_jitter_6											

1.3.2	46 machineconstant	Reg.	0xA00203D4							
Solution Table, Jitter Metric DC 35										
bits	bits name s/w h/w default description									
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 35 s_slt_jitter_7										

1.3.2	47 machineconstant		Reg.	0xA00203D8							
Soluti	Solution Table, Jitter Metric DC 40										
bits	name	description	n								
31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 40 s_slt_jitter_8											

1.3.2	48 machineconstan	Reg.	0xA00203DC							
Solution Table, Jitter Metric DC 45										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_jitter_9	rw	ro	0x0	Solution Table, Ji	tter Metric DC 45				

1.3.2	49 machineconstant	Reg.	0xA00203E0							
Solution Table, Jitter Metric DC 50										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_slt_jitter_10	rw	ro	0x0	Solution Table, Ji	tter Metric DC 50				

1.3.25	0 machineconstant	Reg.	0xA00203E4						
Solution Table, Jitter Metric DC 55									
bits	name	s/w h/w	default	description					

Solution Table, Jitter Metric DC 60  bits name s/w h/w default s, stt_jitter_12								
Solution Table, Jitter Metric DC 60 bits name s/w h/w default s_stt_jitter_12  1.3.252 machineconstants_slt_jitter_13  3.252 machineconstants_slt_jitter_13  3.253 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 65  bits name s/w h/w default description ox0  1.3.253 machineconstants_slt_jitter_14  3.254 machineconstants_slt_jitter_14  3.255 machineconstants_slt_jitter_15  3.256 machineconstants_slt_jitter_15  3.257 machineconstants_slt_jitter_15  3.258 machineconstants_slt_jitter_15  3.259 machineconstants_slt_jitter_15  3.250 machineconstants_slt_jitter_15  3.250 machineconstants_slt_jitter_15  3.251 machineconstants_slt_jitter_16  3.255 machineconstants_slt_jitter_16  3.256 machineconstants_slt_jitter_17  3.257 machineconstants_slt_jitter_17  3.258 machineconstants_slt_jitter_17  3.259 machineconstants_slt_jitter_17  3.250 machineconstants_slt_jitter_17  3.250 machineconstants_slt_jitter_17  3.250 machineconstants_slt_jitter_17  3.250 machineconstants_slt_jitter_17  3.251 machineconstants_slt_jitter_17  3.252 machineconstants_slt_jitter_17  3.253 machineconstants_slt_jitter_17  3.254 machineconstants_slt_jitter_17  3.255 machineconstants_slt_jitter_17  3.256 machineconstants_slt_jitter_17  3.257 machineconstants_slt_jitter_18  3.257 machineconstants_slt_jitter_18		Metric DC 55	olution Table, Jitter N	0x0	ro	rw		31:0
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Solution Table, Jitter Metric DC 65  bits name s/w h/w default description  11:0 machineconstant s_slt_jitter_14  13:253 machineconstants_slt_jitter_14  14:252  Solution Table, Jitter Metric DC 70  bits name s/w h/w default description  15:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 70  bits name s/w h/w default description  15:0 s_slt_jitter_14  16:0 xAC  Solution Table, Jitter Metric DC 75  bits name s/w h/w default description  16:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 75  bits name s/w h/w default description  16:0 xAC  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  16:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  17:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  18:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  18:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 80  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  18:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  18:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  18:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  18:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 85								
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Solution Table, Jitter Metric DC 70  Solution Table, Jitter Metric DC 75  bits name s/w h/w default nachineconstants_slt_jitter_16  Solution Table, Jitter Metric DC 75  bits name s/w h/w default s_slt_jitter_15  Solution Table, Jitter Metric DC 75  Solution Table, Jitter Metric DC 75  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description 11:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description 11:0 machineconstant rw ro 0x0  Solution Table, Jitter Metric DC 80  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 20:00  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 20:00  Solution Table, Jitter Metric DC 85		description		default	h/w			
.3.254 machineconstants_slt_jitter_15  Solution Table, Jitter Metric DC 75  bits name s/w h/w default description  11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 75  .3.255 machineconstants_slt_jitter_16  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  .3.256 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  .3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  11:0 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  .3.257 machineconstants_slt_jitter_18		•	olution Table, Jitter N				machineconstant	
Solution Table, Jitter Metric DC 75  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 75 s_slt_jitter_15  1.3.255 machineconstants_slt_jitter_16  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  1.3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description							·_ <b>_</b> _···	
Solution Table, Jitter Metric DC 75  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 75 s_slt_jitter_15  1.3.255 machineconstants_slt_jitter_16  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  1.3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description								
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3.255 machineconstants_slt_jitter_16  Solution Table, Jitter Metric DC 75  Solution Table, Jitter Metric DC 80  bits name s/w h/w default description  1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  3.256 machineconstant s_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description  1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  3.257 machineconstants_slt_jitter_18						75	on Table, Jitter Metric DC	Solut
Solution Table, Jitter Metric DC 80  bits name s/w h/w default description 31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  1.3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 31:0 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  1.3.257 machineconstants_slt_jitter_18				default	h/w	s/w		bits
bits name s/w h/w default description 11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  3.257 machineconstants_slt_jitter_18		Metric DC 75	olution Table, Jitter N	0x0	ro	rw		31:0
Solution Table, Jitter Metric DC 80  bits name s/w h/w default description 31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  1.3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 31:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  1.3.257 machineconstant s_slt_jitter_18								
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1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 80  3.256 machineconstants_slt_jitter_17						80	on Table, Jitter Metric DC	Solut
Solution Table, Jitter Metric DC 85  bits name s/w h/w default description rw ro 0x0 Solution Table, Jitter Metric DC 85  1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  3.257 machineconstants_slt_jitter_18		description		default	h/w	s/w	name	bits
.3.256 machineconstants_slt_jitter_17  Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  s_slt_jitter_17  .3.257 machineconstants_slt_jitter_18		Metric DC 80	olution Table, Jitter N	0x0	ro	rw		1:0
Solution Table, Jitter Metric DC 85  bits name s/w h/w default description 1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  s_slt_jitter_17  3.257 machineconstants_slt_jitter_18							<u></u>	
bits name s/w h/w default description 1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85  3.257 machineconstants_slt_jitter_18	A00203FC	0	Reg.	_17	_jitte	ts_slt_	i6 machineconstant	.3.2
1:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 85 s_slt_jitter_17  3.257 machineconstants_slt_jitter_18						85	on Table, Jitter Metric DC	Solut
s_slt_jitter_17  3.257 machineconstants_slt_jitter_18  0xA0		•						
Total Triddining of the Julian Line Control		Metric DC 85	olution Table, Jitter N	0x0	ro	rw		1:0
Total Triddiminosoficianto_ont_jittoi_ro								
Solution Table, Jitter Metric DC 90	A0020400	0	Reg.	_18	_jitte	ts_slt_	7 machineconstant	.3.2
						90	on Table, Jitter Metric DC	Solut
bits name s/w h/w default description		description		default	h/w	s/w	name	bits
11:0 machineconstant rw ro 0x0 Solution Table, Jitter Metric DC 90 s_slt_jitter_18		•	lution Table, Jitter N	0x0	ro	rw		31:0

1.3.258 machineconstants\_slt\_jitter\_19

0xA0020404

Solut	ion Table, Jitter Metric DC	95			
bits	name	s/w	h/w	default	description
31:0	machineconstant s_slt_jitter_19	rw	ro	0x0	Solution Table, Jitter Metric DC 95

1.3.2	59 machineconstant	Reg.	0xA0020408								
Soluti	Solution Table, multPresubRate DC 5										
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_slt_multpresu brate_1	rw	ro	0x0	Solution Table, m	ultPresubRate D0	C 5				

1.3.260 machineconstants_slt_multpresubrate_2 0xA002040C									
Solution Table, multPresubRate DC 10									
bits	name	s/w	h/w	default	description				
31:0	machineconstant s_slt_multpresu brate_2	rw	ro	0x0	Solution Table, m	ultPresubRate D0	C 10		

1.3.2	61 machineconstan	Reg.	0xA0020410							
Solution Table, multPresubRate DC 15										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_slt_multpresu brate_3	rw	ro	0x0	Solution Table, m	ultPresubRate D	C 15			

1.3.2	62 machineconstant	Reg.	0xA0020414							
Solution Table, multPresubRate DC 20										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_slt_multpresu brate_4	rw	ro	0x0	Solution Table, m	ultPresubRate D0	C 20			

1.3.2	63 machineconstant	Reg.	0xA0020418						
Solution Table, multPresubRate DC 25									
bits	name	s/w	h/w	default	description				
31:0	machineconstant s_slt_multpresu brate_5	rw	ro	0x0	Solution Table, m	ultPresubRate D0	C 25		

1.3.2	64 machineconstant	Reg.	0xA002041C						
Solution Table, multPresubRate DC 30									
bits	name	s/w	h/w	default	description				
31:0	machineconstant s_slt_multpresu brate_6	rw	ro	0x0	Solution Table, m	ultPresubRate D0	C 30		

1.3.265 machineconstants_slt_multpresubrate_7	Reg.	0xA0020420
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Soluti	Solution Table, multPresubRate DC 35										
bits	bits name s/w h/w default description										
	machineconstant s_slt_multpresu brate_7	rw	ro	0x0	Solution Table, multPresubRate DC 35						

1.3.2	66 machineconstant	Reg.	0xA0020424							
Solution Table, multPresubRate DC 40										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_multpresu brate_8	rw	ro	0x0	Solution Table, multPresubRate DC 40					

1.3.267 machineconstants_slt_multpresubrate_9 0xA0020428										
Solution Table, multPresubRate DC 45										
bits	ts name s/w h/w default description									
31:0	machineconstant s_slt_multpresu brate_9	rw	ro	0x0	Solution Table, multPresubRate DC 45					

1.3.2	68 machineconstant	Reg.	0xA002042C							
Solution Table, multPresubRate DC 50										
bits	its name s/w h/w default description									
31:0	machineconstant s_slt_multpresu brate_10	rw	ro	0x0	Solution Table, multPresubRate DC 50					

1.3.269 machineconstants_slt_multpresubrate_11 0xA0020430											
Solut	Solution Table, multPresubRate DC 55										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_multpresu brate_11	rw	ro	0x0	Solution Table, multPresubRate DC 55						

1.3.2	1.3.270 machineconstants_slt_multpresubrate_12 0xA0020434										
Solut	Solution Table, multPresubRate DC 60										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_multpresu brate_12	rw	ro	0x0	Solution Table, multPresubRate DC 60						

1.3.271 machineconstants_slt_multpresubrate_13 0xA0020438											
Solut	Solution Table, multPresubRate DC 65										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_multpresu brate_13	rw	ro	0x0	Solution Table, multPresubRate DC 65						

1.3.2	1.3.272 machineconstants_slt_multpresubrate_14 0xA002043C											
Soluti	Solution Table, multPresubRate DC 70											
bits	name	name s/w h/w default description										
31:0	machineconstant s_slt_multpresu brate_14	rw	ro	0x0	Solution Table, multPresubRate DC 70							

1.3.2	1.3.273 machineconstants_slt_multpresubrate_15 0xA0020440										
Solut	Solution Table, multPresubRate DC 75										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_multpresu brate_15	rw	ro	0x0	Solution Table, multPresubRate DC 75						

1.3.274 machineconstants_slt_multpresubrate_16 0xA0020444										
Solution Table, multPresubRate DC 80										
bits	s name s/w h/w default description									
31:0	machineconstant s_slt_multpresu brate_16	rw	ro	0x0	Solution Table, multPresubRate DC 80					

1.3.275 machineconstants_slt_multpresubrate_17 0xA0020448											
Solution Table, multPresubRate DC 85											
bits	bits name s/w h/w default description										
31:0	machineconstant s_slt_multpresu brate_17	rw	ro	0x0	Solution Table, multPresubRate DC 85						

1.3.2	76 machineconstan	Reg.	0xA002044C									
Solut	Solution Table, multPresubRate DC 90											
bits	bits name s/w h/w default description											
31:0	machineconstant s_slt_multpresu brate_18	rw	ro	0x0	Solution Table, multPresubRate DC 90							

1.3.277 machineconstants_slt_multpresubrate_19 0xA0020450										
Solution Table, multPresubRate DC 95										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_slt_multpresu brate_19	rw	ro	0x0	Solution Table, multPresubRate DC 95					

1.3.2	78 machineconstant		Reg.	0xA0020454							
Solut	Solution Table,PreSubRate DC 5										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_presubrat e_1	rw	ro	0x0	Solution Table,PreSubRate DC 5						

1.3.2	79 machineconstan	ts_slt	_pres	subrate_2		Reg.	0xA0020458			
Solution Table,PreSubRate DC 10										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_slt_presubrat e_2	rw	ro	0x0	Solution Table,PreSubRate DC 10					

1.3.2	80 machineconstan	Reg.	0xA002045C							
Solution Table,PreSubRate DC 15										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_presubrat e_3	rw	ro	0x0	Solution Table,PreSubRate DC 15					

1.3.281 machineconstants_slt_presubrate_4 0xA00									
Solution Table,PreSubRate DC 20									
bits	bits name s/w h/w default description								
31:0	machineconstant s_slt_presubrat e_4	rw	ro	0x0	Solution Table,PreSubRate DC 20				

1.3.2	82 machineconstan	Reg.	0xA0020464							
Solution Table,PreSubRate DC 25										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_slt_presubrat e_5	rw	ro	0x0	Solution Table,PreSubRate DC 25					

1.3.2	83 machineconstant	Reg.	0xA0020468							
Solution Table,PreSubRate DC 30										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_presubrat e_6	rw	ro	0x0	Solution Table,PreSubRate DC 30					

1.3.2	84 machineconstant		Reg.	0xA002046C							
Solut	Solution Table, PreSubRate DC 35										
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_slt_presubrat e_7	rw	ro	0x0	Solution Table,PreSubRate DC 35						

1.3.2	1.3.285 machineconstants_slt_presubrate_8 0xA0020470									
Solution Table,PreSubRate DC 40										
bits	name	s/w	h/w	default		description	٦			
31:0	machineconstant s_slt_presubrat	rw	ro	0x0	Solution Table, PreSubRate DC 40					

e 8		

1.3.2	86 machineconstan	ts_slt		Reg.	0xA0020474						
Solut	Solution Table, PreSubRate DC 45										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_slt_presubrat e_9	rw	ro	0x0	Solution Table,Pr	eSubRate DC 45					

1.3.2	87 machineconstant	Reg.	0xA0020478							
Solution Table,PreSubRate DC 50										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_slt_presubrat e_10	rw	ro	0x0	Solution Table,PreSubRate DC 50					

1.3.2	88 machineconstan	Reg.	0xA002047C										
Soluti	Solution Table,PreSubRate DC 55												
bits	name s/w h/w default description												
31:0	machineconstant s_slt_presubrat e_11	rw	eSubRate DC 55										

1.3.2	1.3.289 machineconstants_slt_presubrate_12 0xA0020480											
Solut	Solution Table,PreSubRate DC 60											
bits	bits name s/w h/w default description											
31:0	machineconstant s_slt_presubrat e_12	rw	ro	0x0	Solution Table,Pr	eSubRate DC 60						

1.3.2	I.3.290 machineconstants_slt_presubrate_13 0xA0020484											
Solution Table,PreSubRate DC 65												
bits	bits name s/w h/w default description											
31:0	machineconstant s_slt_presubrat e_13	rw	ro	0x0	Solution Table,Pr	eSubRate DC 65	5					

1.3.2	91 machineconstant	Reg.	0xA0020488								
Solution Table,PreSubRate DC 70											
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_presubrat e_14	rw	ro	0x0	Solution Table,Pre	eSubRate DC 70					

1.3.29	92 machineconstant	Reg.	0xA002048C									
Soluti	Solution Table, PreSubRate DC 75											
bits	bits name s/w h/w default description											
31:0 machineconstant rw ro 0x0 Solution Table, PreSubRate DC 75												

s_slt_presubrat			
e_15			

1.3.2	0xA0020490											
Solut	Solution Table,PreSubRate DC 80											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_slt_presubrat e_16	rw	ro	0x0	Solution Table,Pr	eSubRate DC 80						

1.3.2	94 machineconstant	Reg.	0xA0020494									
Solut	Solution Table,PreSubRate DC 85											
bits	name	s/w	h/w	default		description	า					
31:0	machineconstant s_slt_presubrat e_17	rw	ro	0x0	Solution Table,Pre	eSubRate DC 85						

1.3.2	0xA0020498											
Solut	Solution Table,PreSubRate DC 90											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_slt_presubrat e_18	rw	ro	0x0	Solution Table,Pro	eSubRate DC 90						

1.3.296 machineconstants_slt_presubrate_19 0xA002049C											
Solution Table,PreSubRate DC 95											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_slt_presubrat e_19	rw	ro	0x0	Solution Table,Pr	eSubRate DC 95					

1.3.2	97 machineconstant	Reg.	0xA00204A0									
Solut	Solution Table, CM DC 5											
bits	name	s/w	h/w	default		description	١					
31:0 machineconstant rw ro 0x0 Solution Table, CM DC 5 s_slt_cm_1												

1.3.2	98 machineconstant	Reg.	0xA00204A4									
Solut	Solution Table, CM DC 10											
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x0 Solution Table, CM DC 10 s_slt_cm_2												

1.3.299 machineconstants_slt_cm_3						Reg.	0xA00204A8
Solution Table, CM DC 15							
bits	name	s/w	h/w	default	description		
31:0	machineconstant s_slt_cm_3	rw	ro	0x0	Solution Table, Cl	ole, CM DC 15	

O - I	800 machineconstar					
	tion Table, CM DC 20	- /	<b>b</b> /	ماملور بالا	dana	uinti a u
bits 1:0	name machineconstant	s/w rw	h/w ro	default 0x0	Solution Table, CM DC 20	cription
	s_slt_cm_4	1 **	10	OXO	Coldion Table, CW 20 20	
3.3	801 machineconstar	nts sit	cm	5	Reg.	0xA00204B0
		110_010	_0111_			
bits	tion Table, CM DC 25	s/w	h/w	default	dosc	cription
1:0	machineconstant	rw	ro	0x0	Solution Table, CM DC 25	приоп
71.0	s_slt_cm_5	1 **	10	UNU .	Columbia Fable, CIVI DO 20	
.3.3	802 machineconstar	nts sit	cm	6	Reg	0xA00204B4
	tion Table, CM DC 30					
		0/11	h/w	dofoult	ام	cription
bits 1:0	name machineconstant	s/w rw	h/w ro	default 0x0	Solution Table, CM DC 30	cription
1.0	s_slt_cm_6	1 44	10	3,0	Coldion Table, ON DO 50	
2 2	803 machineconstar	nte els	cm	7	Reg.	0xA00204B8
		113_511	0111_	_1	***************************************	0A/ 100204B0
	tion Table, CM DC 35	,				
bits	name	s/w	h/w	default		cription
1:0	machineconstant s_slt_cm_7	rw	ro	0x0	Solution Table, CM DC 35	
2.0	004 machinesenetes	-414	0.100	0	Ren	0×400204PC
	804 machineconstar	าเร_Sit	_cm_	_0	Reg.	0xA00204BC
Solu	tion Table, CM DC 40					
	name	s/w	h/w	default		cription
bits	machineconstant	rw	ro	0x0	Solution Table, CM DC 40	
bits 1:0	s_slt_cm_8					
	s_slt_cm_8					
1:0		ate old	om	0	Rea	0× $0$ 00204 $0$ 0
1:0	05 machineconstar	nts_slt	_cm_	_9	Reg.	0xA00204C0
1:0   .3.3   Solu	<b>305 machineconstar</b> tion Table, CM DC 45					
1:0   .3.3   Solu	tion Table, CM DC 45	s/w	h/w	default	desc	0xA00204C0
1:0   .3.3   Solu	<b>305 machineconstar</b> tion Table, CM DC 45					
1:0   .3.3   Solu	tion Table, CM DC 45 name machineconstant	s/w	h/w	default	desc	
3.3.3 Solu bits 31:0	tion Table, CM DC 45 name machineconstant s_slt_cm_9	s/w rw	h/w ro	default 0x0	deso Solution Table, CM DC 45	cription
3.3.3 Solu bits 11:0	tion Table, CM DC 45 name machineconstant s_slt_cm_9	s/w rw	h/w ro	default 0x0	desc	
31:0 3.3.3 Solu bits 51:0 Solu	ition Table, CM DC 45 name machineconstant s_slt_cm_9  806 machineconstant tion Table, CM DC 50	s/w rw	h/w ro	default 0x0	Solution Table, CM DC 45	oxA00204C4
3.3.3 Solu bits 11:0	ition Table, CM DC 45 name machineconstant s_slt_cm_9  806 machineconstant tion Table, CM DC 50	s/w rw	h/w ro	default 0x0	Solution Table, CM DC 45	cription

1.3.307 machineconstants\_slt\_cm\_11

s/w h/w

Solution Table, CM DC 55

name

default

0xA00204C8

Reg.

description

31:0	machineconstant	rw	ro	0x0	Solution Table, Cl	M DC 55	
	s_slt_cm_11				2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	_ 2 30	
.3.2	308 machineconstar	nts slt	cm	12		Reg.	0xA00204CC
	tion Table, CM DC 60	010		_ • _			
bits		s/w	h/w	default		das	cription
31:0	machineconstant	rw	ro	0x0	Solution Table, Cl		onpuon
	s_slt_cm_12						
1.0				10			0.40004P0
	809 machineconstar	nts_sIt	_cm	_13		Reg.	0xA00204D0
	tion Table, CM DC 65	,	. ,				
bits 31:0	name machineconstant	s/w rw	h/w ro	default 0x0	Solution Table, Cl		cription
J1.U	s_slt_cm_13	1 VV	10	0.00	Joidholl Table, Ol	VI DO 03	
1.3.3	310 machineconstar	nts_slt	_cm	_14		Reg.	0xA00204D4
Solu	tion Table, CM DC 70						
bits		s/w	h/w	default	Coluston Table Of		cription
31:0	machineconstant s_slt_cm_14	rw	ro	0x0	Solution Table, Cl	VI DC 70	
Solu bits 31:0	name machineconstant s_slt_cm_15	s/w rw	h/w ro	default 0x0	Solution Table, Cl		cription
	0_01(_0111_10						
1.3.3	312 machineconstar	nts_slt	_cm	_16		Reg.	0xA00204DC
	tion Table, CM DC 80						
bits		s/w	h/w	default	Coluston Teles Of		cription
31:0	machineconstant s_slt_cm_16	rw	ro	0x0	Solution Table, Cl	IVI DC 80	
1.3.3	313 machineconstar	nts_slt	_cm	_17		Reg.	0xA00204E0
Solu	tion Table, CM DC 85						
bits		s/w	h/w	default			cription
31:0	machineconstant s_slt_cm_17	rw	ro	0x0	Solution Table, Cl	M DC 85	
1.3.3	314 machineconstar	nts_slt	_cm	_18		Reg.	0xA00204E4
	tion Table, CM DC 90						
bits		s/w	h/w	default	Coluston Teles Of		cription
31:0	machineconstant s_slt_cm_18	rw	ro	0x0	Solution Table, Cl	M DC 90	

1.3.315 machineconstants\_slt\_cm\_19

0xA00204E8

Solut	ion Table, CM DC 95				
bits	name	s/w	h/w	default	description
31:0	machineconstant s_slt_cm_19	rw	ro	0x0	Solution Table, CM DC 95

1.3.3	1.3.316 machineconstants_slt_dm_1 0xA00204EC										
Soluti	Solution Table, DM DC 5										
bits	name	s/w	h/w	default		description	n				
-											

1.3.3	0xA00204F0										
Soluti	Solution Table, DM DC 10										
bits	name	s/w	h/w	default		description	า				
31:0											

1.3.3	18 machineconsta	nts_slt	Reg.	0xA00204F4							
Solut	Solution Table, DM DC 15										
bits	name	s/w	h/w	default		description	า				
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1										

1.3.3	I.3.319 machineconstants_slt_dm_4 0xA00204F8										
Solut	Solution Table, DM DC 20										
bits	name	s/w	h/w	default		description	n				
31:0											

1.3.3	1.3.320 machineconstants_slt_dm_5 0xA00204FC											
Solut	Solution Table, DM DC 25											
bits	name	s/w	h/w	default		description	١					
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											

1.3.3	1.3.321 machineconstants_slt_dm_6 0xA0020500											
Solut	Solution Table, DM DC 30											
bits	name	s/w	h/w	default		description	ı					
31:0	7 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -											

1.3.3	1.3.322 machineconstants_slt_dm_7 0xA0020504										
Solut	Solution Table, DM DC 35										
bits	name	s/w	h/w	default		description	1				
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1										

	323 machineconstar	nts_slt	_dm_	_8		Reg.	0xA0020508
Solu	tion Table, DM DC 40						
bits	name	s/w	h/w	default		desc	cription
31:0	machineconstant	rw	ro	0x0	Solution Table, D	M DC 40	
	s_slt_dm_8						
.3.3	324 machineconstar	nts slt	dm	9		Reg.	0xA002050C
	tion Table, DM DC 45						
bits		s/w	h/w	default		door	printion
31:0	name machineconstant	rw	ro	0x0	Solution Table, D		cription
71.0	s_slt_dm_9	1 00	10	OXO	Colditor Table, D	W DO 43	
2 2	325 machineconstar	nte els	dm	10		Reg.	0xA0020510
		แอ_5เเ	_uiii_	_10			0A/10020010
	tion Table, DM DC 50						
bits		s/w	h/w	default			cription
31:0	machineconstant s_slt_dm_10	rw	ro	0x0	Solution Table, D	M DC 50	
	5_5IL_UIII_10						
.3.3	326 machineconstar	nts slt	dm	11		Reg.	0xA0020514
	tion Table, DM DC 55						
Joilu		- 1	b/w	default		4	cription
hits	name	S/\W					
bits		s/w rw	h/w ro		Solution Table, D		лірион
bits 31:0	name machineconstant s_slt_dm_11	rw	ro	0x0	Solution Table, D		лрион
	machineconstant				Solution Table, D		лрион
31:0	machineconstant s_slt_dm_11	rw	ro	0x0	Solution Table, D	M DC 55	
31:0	machineconstant	rw	ro	0x0	Solution Table, D		0xA0020518
31:0	machineconstant s_slt_dm_11	rw	ro	0x0	Solution Table, D	M DC 55	
31:0	machineconstant s_slt_dm_11	rw	ro	0x0	Solution Table, D	M DC 55	0xA0020518
31:0 1.3.3 Solu bits	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60	rw	ro _dm_	0x0 _12	Solution Table, D	M DC 55	
31:0 1.3.3 Solu	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60 name	rw nts_slt	ro dm_	0x0  12  default		M DC 55	0xA0020518
31:0 1.3.3 Solu bits	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60 name machineconstant	rw nts_slt	ro dm_	0x0  12  default		M DC 55	0xA0020518
31:0 Solubits 31:0	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60 name machineconstant	rw  nts_slt	no dm_dm_	0x0  12  default 0x0		M DC 55	0xA0020518
31:0 Solu bits 31:0	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60 name machineconstant s_slt_dm_12  328 machineconstar	rw  nts_slt	no dm_dm_	0x0  12  default 0x0		M DC 55  Reg.  desc M DC 60	0xA0020518 cription
1.3.3 Solu bits 31:0	machineconstant s_slt_dm_11  327 machineconstar  tion Table, DM DC 60  name machineconstant s_slt_dm_12  328 machineconstar  tion Table, DM DC 65	rw  s/w rw  nts_slt	h/w ro	0x0		M DC 55  Reg.  desc M DC 60	0xA0020518 cription 0xA002051C
1.3.3 Solu bits 31:0 Solu bits	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60 name machineconstant s_slt_dm_12  328 machineconstar	rw  nts_slt	no dm_dm_	0x0  12  default 0x0	Solution Table, D	M DC 55  Reg.  desc M DC 60	0xA0020518 cription
1.3.3 Solu bits 31:0 Solu bits	machineconstant s_slt_dm_11  327 machineconstar tion Table, DM DC 60 name machineconstant s_slt_dm_12  328 machineconstar tion Table, DM DC 65 name	s/w rw	h/w ro	0x0  12  default 0x0  13		M DC 55  Reg.  desc M DC 60	0xA0020518 cription 0xA002051C
1.3.3 Solu bits 31:0 Solu bits	machineconstant s_slt_dm_11  327 machineconstar  tion Table, DM DC 60  name machineconstant s_slt_dm_12  328 machineconstar  tion Table, DM DC 65  name machineconstant	s/w rw	h/w ro	0x0  12  default 0x0  13	Solution Table, D	M DC 55  Reg.  desc M DC 60	0xA0020518 cription 0xA002051C
31:0 Solu bits 31:0 Solu bits	machineconstant s_slt_dm_11  327 machineconstar  tion Table, DM DC 60  name machineconstant s_slt_dm_12  328 machineconstar  tion Table, DM DC 65  name machineconstant s_slt_dm_13	s/w rw	h/w ro	0x0  12  default 0x0  13  default 0x0	Solution Table, D	desc M DC 60	0xA0020518  OxA002051C  cription
3.3.3 Solu bits 51:0 Solu bits 51:0	machineconstant s_slt_dm_11  327 machineconstar tion Table, DM DC 60	s/w rw	h/w ro	0x0  12  default 0x0  13  default 0x0	Solution Table, D	M DC 55  Reg.  desc M DC 60	0xA0020518 cription 0xA002051C
Solu bits Solu bits S1:0	machineconstant s_slt_dm_11  327 machineconstar  tion Table, DM DC 60  name machineconstant s_slt_dm_12  328 machineconstar  tion Table, DM DC 65  name machineconstant s_slt_dm_13	s/w rw	h/w ro	0x0  12  default 0x0  13  default 0x0	Solution Table, D	desc M DC 60	0xA0020518  0xA002051C  cription  0xA0020520
Solu bits 31:0	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60	s/w rw	h/w ro	0x0  12  default 0x0  13  default 0x0	Solution Table, D	desc M DC 60	0xA0020518  OxA002051C  cription
1.3.3 Solu bits 31:0 Solu bits 31:0	machineconstant s_slt_dm_11  327 machineconstar tion Table, DM DC 60	s/w rw	h/w ro	0x0  12  default 0x0  13  default 0x0	Solution Table, D	desc M DC 60	0xA0020518  0xA002051C  cription  0xA0020520
Solu bits 1:0	machineconstant s_slt_dm_11  327 machineconstart tion Table, DM DC 60	s/w rw	h/w ro  h/w ro  h/w	0x0  12  default 0x0  13  default 0x0	Solution Table, D	desc M DC 60	0xA0020518  0xA002051C  cription  0xA0020520
1:0  .3.3  Solu bits 1:0  .3.3  Solu bits 1:0	machineconstant s_slt_dm_11  327 machineconstar tion Table, DM DC 60	s/w rw	h/w ro  h/w ro  h/w	0x0  12  default 0x0  13  default 0x0	Solution Table, D	desc M DC 60	0xA0020518  0xA002051C  cription  0xA0020520
1:0  .3.3 Solu bits 1:0  .3.3 Solu bits 1:0	machineconstant s_slt_dm_11  327 machineconstar tion Table, DM DC 60	s/w rw	h/w ro  h/w ro	0x0  12  default 0x0  13  default 0x0  14  default 0x0	Solution Table, D	desc M DC 60	0xA0020518  OxA002051C  OxA0020520

Solution Table, DM DC 75

name

s/w h/w

description

31:0	machineconstant	rw	ro	0x0	Solution Table, DM DC 75	
	s_slt_dm_15					
.3.3	31 machineconsta	nts_slt	_dm_	_16	Reg.	0xA0020528
Solut	ion Table, DM DC 80					
bits	name	s/w	h/w	default	descrip	tion
31:0	machineconstant s_slt_dm_16	rw	ro	0x0	Solution Table, DM DC 80	
.3.3	32 machineconsta	nts_slt	_dm_	_17	Reg.	0xA002052C
Solut	ion Table, DM DC 85					
bits	name	s/w	h/w	default	descrip	tion
31:0	machineconstant s_slt_dm_17	rw	ro	0x0	Solution Table, DM DC 85	
1.3.3	33 machineconsta	nts_slt	_dm_	_18	Reg.	0xA0020530
Solut	ion Table, DM DC 90					
bits	name	s/w	h/w	default	descrip	tion
31:0	machineconstant s_slt_dm_18	rw	ro	0x0	Solution Table, DM DC 90	
4.0.0	04 11	4 14		10	Dan	0.40000524
1.3.3	34 machineconsta	nts_sit	_dm_	_19	Reg.	0xA0020534
Solut	ion Table, DM DC 95					
bits	name	s/w	h/w	default	descrip	tion
31:0	machineconstant s_slt_dm_19	rw	ro	0x0	Solution Table, DM DC 95	
1.3.3	35 machineconsta	nts slt	dcd	phi	Reg.	0xA0020538
	ion Table, DM DCDPhi			•		
bits	name	s/w	h/w	default	descrip	tion
31:0	machineconstant	rw	ro	0x0	Solution Table, DM DCDPhi	uon
	s_slt_dcdphi				,	
120	26 maakinassusts	of -14	n la la	I morain 4	Ran	0xA002053C
	36 machineconstalion table, phi1Margin DC		_pnı'	ımargın_1	Reg.	UXAUUZUOSC
bits	name	s/w	h/w	default	descrip	tion
31:0	machineconstant	rw	ro	0x0	Solution table, phi1Margin DC 5	
	s_slt_phi1margi n_1				71	
1.3.3	37 machineconsta	nts_slt	_phi′	Imargin_2	Reg.	0xA0020540
Solut	ion table, phi1Margin DC	: 10				
bits	name	s/w	h/w	default	descrip	
31:0	machineconstant	rw	ro	0x0	Solution table, phi1Margin DC 1	0

s\_slt\_phi1margi n\_2

1.3.3	1.3.338 machineconstants_slt_phi1margin_3 0xA0020544											
Solution table, phi1Margin DC 15												
bits	bits name s/w h/w default description											
31:0	machineconstant s_slt_phi1margi n_3	rw	ro	0x0	Solution table, phi1Margin DC 15							

1.3.3	39 machineconstant	0xA0020548									
Solut	Solution table, phi1Margin DC 20										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_slt_phi1margi n_4	rw	ro	0x0	Solution table, phi1Margin DC 20						

1.3.340 machineconstants_slt_phi1margin_5 0xA002054C											
Solut	Solution table, phi1Margin DC 25										
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_slt_phi1margi n_5	rw	ro	0x0	Solution table, ph	i1Margin DC 25					

1.3.3	41 machineconstan	Reg.	0xA0020550							
Solution table, phi1Margin DC 30										
bits	name	s/w	h/w	default		descriptio	n			
31:0	machineconstant s_slt_phi1margi n_6	rw	ro	0x0	Solution table, phi1Margin DC 30					

1.3.3	42 machineconstant	Reg.	0xA0020554							
Solution table, phi1Margin DC 35										
bits name s/w h/w default description										
31:0	machineconstant s_slt_phi1margi n_7	rw	ro							

1.3.3	43 machineconstant	Reg.	0xA0020558								
Solut	Solution table, phi1Margin DC 40										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_slt_phi1margi n_8	rw	ro	0x0	Solution table, phi1Margin DC 40						

1.3.344 machineconstants_slt_phi1margin_9 0xA002055C											
Solut	Solution table, phi1Margin DC 45										
bits	name	s/w	h/w	default		description	า				
31:0											

1.3.3	1.3.345 machineconstants_slt_phi1margin_10 0xA0020560											
Solut	Solution table, phi1Margin DC 50											
bits	bits name s/w h/w default description											
31:0	machineconstant s_slt_phi1margi n_10	rw	ro	0x0	Solution table, ph	i1Margin DC 50						

1.3.346 machineconstants_slt_phi1margin_11 0xA0020564										
Solution table, phi1Margin DC 55										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_slt_phi1margi n_11	rw	ro	0x0	Solution table, phi1Margin DC 55					

1.3.3	47 machineconstant	Reg.	0xA0020568							
Solution table, phi1Margin DC 60										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_phi1margi n_12	rw	ro							

1.3.3	48 machineconstant	Reg.	0xA002056C								
Solution table, phi1Margin DC 65											
bits	its name s/w h/w default description										
-	machineconstant s_slt_phi1margi n_13	rw	i1Margin DC 65								

1.3.349 machineconstants_slt_phi1margin_14 0xA0020570											
Solut	Solution table, phi1Margin DC 70										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_slt_phi1margi n_14	rw	ro	0x0	Solution table, phi1Margin DC 70						

1.3.3	50 machineconstan	Reg.	0xA0020574							
Solution table, phi1Margin DC 75										
bits	name	s/w	h/w	default		description				
31:0	machineconstant s_slt_phi1margi n_15	rw	ro	0x0	Solution table, ph	i1Margin DC 75				

1.3.3	1.3.351 machineconstants_slt_phi1margin_16 0xA0020578								
Solution table, phi1Margin DC 80									
bits	name	s/w	h/w	default		description	า		
31:0	machineconstant s_slt_phi1margi	rw	ro	0x0	Solution table, phi1Margin DC 80				

n 16		

1.3.3	52 machineconstan	Reg.	0xA002057C						
Solution table, phi1Margin DC 85									
bits	name	s/w	h/w	default		description	n		
31:0	machineconstant s_slt_phi1margi n_17	rw	ro	0x0	Solution table, ph	i1Margin DC 85			

1.3.3	53 machineconstant	Reg.	0xA0020580						
Solution table, phi1Margin DC 90									
bits	name	s/w	h/w	default		description	า		
31:0	machineconstant s_slt_phi1margi n_18	rw	ro	0x0	Solution table, ph	1Margin DC 90			

1.3.3	54 machineconstan	Reg.	0xA0020584						
Solution table, phi1Margin DC 95									
bits	name	s/w	h/w	default		descriptio	n		
31:0	machineconstant s_slt_phi1margi n_19	rw	ro	0x0	Solution table, phi1Margin DC 95				

1.3.3	55 machineconstant	Reg.	0xA0020588						
Solution Table, phi0Margin DC 5									
bits	name	s/w	h/w	default		descriptio	n		
31:0	machineconstant s_slt_phi0margi n	rw	ro	0x0	Solution Table, p	hi0Margin DC 5			

1.3.3	1.3.356 machineconstants_slt_satrateavg_off 0xA002058C									
Satrate average, DDM, off droplet										
bits	bits name s/w h/w default description									
31:0	machineconstant s_slt_satrateav g_off	rw	ro	0x0	Satrate average, DDM, off droplet					

1.3.3	57 machineconstant		Reg.	0xA0020590					
Satrate average, DDM, on droplet									
bits	name	s/w	h/w	default		description	า		
31:0	machineconstant s_slt_satrateav g_on	rw	ro	0x0	Satrate average,	DDM, on droplet			

1.3.3	58 machineconstant	Reg.	0xA0020594							
Solution table xint3sigma_avg										
bits	bits name s/w h/w default description									
31:0	machineconstant	rw	ro	0x0	Solution table xint3sigma_avg					

s_slt_xint3sigm			
a_avg			

1.3.3	59 machineconstant	g	Reg.	0xA0020598						
presubrateavg, monitor state, for OPT DC										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_presubrat e_avg	rw	ro	0x0	presubrateavg, m	onitor state, for O	PT DC			

1.3.3	60 machineconstan	Reg.	0xA002059C							
Index of the Optimal solution in the solution table										
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_slt_opt_sol	rw	ro	0x2	Index of the Optimal solution in the solution table					

1.3.3	61 machineconstan	Reg.	0xA00205A0							
Index of the next Backup solution in the solution table										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_slt_bk_sol	rw	ro	0x2	Index of the next Backup solution in the solution table					

1.3.3	1.3.362 machineconstants_damp_damp2piezo_gain 0xA00205A4											
DAMP Gain adjustment												
bits	name	s/w	h/w	default	description							
31:0	machineconstant s_damp_damp2pie zo_gain	rw	ro	0xA3D	DAMP Gain adjustment							

1.3.30 _aoc	63 machineconstan h1	Reg.	0xA00205A8								
•	planned for MVP only. They setup debug mode for the analog outputs for the DAMP										
bits	name	s/w	h/w	default		descriptior	1				
-	machineconstant s_damp_waveform _debug_setup_ao ch1	rw	ro	0x0	planned for MVP ( log outputs for the		debug mode for the ana-				

	1.3.364 machineconstants_damp_waveform_debug_setup 0xA00205AC _aoch2											
plann	planned for MVP only. They setup debug mode for the analog outputs for the DAMP  bits name s/w h/w default description											
31:0	machineconstant s_damp_waveform _debug_setup_ao ch2	rw			planned for MVP only. They setup debug mode for the analog outputs for the DAMP							

1.3.365 machineconstants_damp_waveform_debug_setup	Reg.	0xA00205B0
_aoch3		

plann	planned for MVP only. They setup debug mode for the analog outputs for the DAMP										
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_damp_waveform _debug_setup_ao ch3	rw	ro	0x0	planned for MVP only. They setup debug mode for the analog outputs for the DAMP						

	1.3.366 machineconstants_damp_waveform_debug_setup 0xA00205B4										
planned for MVP only. They setup debug mode for the analog outputs for the DAMP  bits name s/w h/w default description											
31:0	machineconstant s_damp_waveform _debug_setup_ao ch4	rw	ro	0x0	planned for MVP only log outputs for the DA	only. They setup debug mode for the ana-					

1.3.3	67 machineconstant	Reg.	0xA00205B8							
DAMP deltaN is samples										
bits	name	s/w	h/w	default		description	١			
31:0	machineconstant s_damp_deltan	rw	ro	0x0	DAMP deltaN is samples					

1.3.3	68 machineconstant	Reg.	0xA00205BC							
DAMP ditherbits is samples										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_damp_ditherbi ts	rw	ro	0x0	DAMP ditherbits is samples					

1.3.3	69 machineconstant	min	Reg.	0xA00205C0						
Base Frequency Min for Base Droplet Optimization										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_cal_bdo_basef reqmin	rw	ro	0x2A4C2000	Base Frequency I	Min for Base Droplet Optimization				

1.3.3	1.3.370 machineconstants_cal_bdo_basefreqnumber 0xA00205C4										
Base Frequency Number for Base Droplet Optimization											
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_cal_bdo_basef reqnumber	rw	ro	0x3	Base Frequency I	Number for Base Droplet Optimization					

1.3.3	71 machineconstant	res	Reg.	0xA00205C8							
Base Frequency Resolution for Base Droplet Optimization											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_cal_bdo_basef reqres	rw	ro	0x3D86000	Base Frequency Resolution for Base Droplet Optimization						

1.3.3	72 machineconstant	Reg.	0xA00205CC								
Squa	Square Amplitude for TFM										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_sqrampltf	Square Amplitude	e for TFM								

1.3.373 machineconstants_cal_mainfreqvec_min 0xA00205D0											
Calibration parameter: cal_mainfreqvec_min											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_cal_mainfreqv ec_min	rw	ro	0x3C8C000	Calibration parameter: cal_mainfreqvec_min						

1.3.3	1.3.374 machineconstants_cal_mainfreqvec_number 0xA00205D4											
Calibration parameter: cal_mainfreqvec_number												
bits	bits name s/w h/w default description											
31:0	machineconstant s_cal_mainfreqv ec_number	rw	ro	0x15	Calibration parameter: cal_mainfreqvec_number							

1.3.3	75 machineconstan	Reg.	0xA00205D8								
Calibration parameter: cal_mainfreqvec_res											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_cal_mainfreqv ec_res	rw	ro	0x19000	Calibration parameter: cal_mainfreqvec_res						

1.3.3	1.3.376 machineconstants_cal_subfreqmultvec_min 0xA00205DC											
Calibration parameter: cal_subfreqmultvec_min												
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_cal_subfreqmu ltvec_min	rw	ro	0x1C00	Calibration parameter: cal_subfreqmultvec_min							

1.3.3	1.3.377 machineconstants_cal_subfreqmultvec_number 0xA00205E0											
Calibration parameter: cal_subfreqmultvec_number												
bits	bits name s/w h/w default description											
31:0	machineconstant s_cal_subfreqmu ltvec_number	rw	ro	0x4	Calibration parameter: cal_subfreqmultvec_number							

1.3.378 machineconstants_cal_subfreqmultvec_res 0xA00205E4											
Calibration parameter: cal_subfreqmultvec_res											
bits	bits name s/w h/w default description										
31:0	machineconstant s_cal_subfreqmu ltvec_res	rw	ro	0x400	Calibration parameter: cal_subfreqmultvec_res						

1.3.3	1.3.379 machineconstants_cal_sineampltfmin 0xA00205E8											
Calib	Calibration parameter: cal_sineampltfmin											
bits	bits name s/w h/w default description											
31:0	machineconstant s_cal_sineamplt fmin	rw	ro	0x66	Calibration parameter: cal_sineampltfmin							

1.3.3	80 machineconstant	Reg.	0xA00205EC								
Calib	Calibration parameter: cal_sineampltfres										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_sineamplt fres	rw	ro	0x66	Calibration parameter: cal_sineampltfres						

1.3.3	81 machineconstant	Reg.	0xA00205F0							
Calibration parameter: cal_sineampltfnumber										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_cal_sineamplt fnumber	rw	ro	0x14	Calibration parameter: cal_sineampltfnumber					

1.3.3	0xA00205F4										
Calibration parameter: cal_mainfreqdiag_min											
bits	oits name s/w h/w default description										
31:0	machineconstant s_cal_mainfreqd iag_min	rw	ro	0x30D4000	Calibration parameter: cal_mainfreqdiag_min						

1.3.3	83 machineconstant	Reg.	0xA00205F8								
Calib	Calibration parameter: cal_mainfreqdiag_res										
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_cal_mainfreqd iag_res	rw	ro	0x19000	Calibration parameter: cal_mainfreqdiag_res						

1.3.3	84 machineconstan	number	Reg.	0xA00205FC							
Calib	Calibration parameter: cal_mainfreqdiag_number										
bits	name	s/w	h/w	default	description						
31:0	machineconstant s_cal_mainfreqd iag_number	rw	ro	0xC9	Calibration parameter: cal_mainfreqdiag_number						

1.3.3	1.3.385 machineconstants_cal_bdo_holdoff 0xA0020600									
Calib	Calibration parameter: cal_bdo_holdoff									
bits	name	s/w	h/w	default		description	٦			
31:0	machineconstant s_cal_bdo_holdo	rw	ro	0xA	Calibration parameter: cal_bdo_holdoff					

ff |

1.3.3	86 machineconstant	Reg.	0xA0020604							
Calib	Calibration parameter: cal_tfm_holdoff									
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_cal_tfm_holdo ff	rw	ro	0xA	Calibration parameter: cal_tfm_holdoff					

1.3.3	87 machineconstant	Reg.	0xA0020608							
Calibration parameter: cal_ddmmainpeakvalthr										
bits	name	s/w	h/w	default	description					
31:0	machineconstant s_cal_ddmmainpe akvalthr	rw	ro	0x2000	Calibration parameter: cal_ddmmainpeakvalthr					

1.3.3	88 machineconstan	Reg.	0xA002060C								
Calib	Calibration parameter: cal_ddmsnrthr										
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_cal_ddmsnrthr	rw	ro	0x500	Calibration parameter: cal_ddmsnrthr						

1.3.3	89 machineconstant	Reg.	0xA0020610								
Calibi	Calibration parameter: cal_ddmwidththr										
bits	name	s/w	h/w	default	de	scription					
31:0	machineconstant s_cal_ddmwidtht hr	rw	ro	0x4CD	Calibration parameter: cal_ddmwidththr						

1.3.3	90 machineconstan	Reg.	0xA0020614								
Calib	Calibration parameter: cal_ddmqc_holdoff										
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_ddmqc_hol doff	rw	ro	0x5	Calibration param	_holdoff					

1.3.3	91 machineconstant	Reg.	0xA0020618							
Calib	Calibration parameter: cal_dcmqc_holdoff									
bits	name	s/w	h/w	default		description	า			
31:0	machineconstant s_cal_dcmqc_hol doff	rw	ro	0x5	Calibration param	eter: cal_dcmqc_	holdoff			

1.3.3	1.3.392 machineconstants_cal_dcmmainpeakvalthr 0xA002061C											
Calib	Calibration parameter: cal_dcmmainpeakvalthr											
bits	name	s/w	h/w	default		descriptio	n					
31:0	machineconstant s_cal_dcmmainpe	rw	ro	0x2000	Calibration parameter: cal_dcmmainpeakvalthr							

مرافا مربيا			
akvalthr			

1.3.3	93 machineconstar	Reg.	0xA0020620								
Calib	Calibration parameter: cal_dcmsnrthr										
bits	name	s/w	h/w	default		description	n				
31:0 machineconstant rw ro 0x500 Calibration parameter: cal_dcmsnrthr s_cal_dcmsnrthr											

1.3.394 machineconstants_cal_dcmwidththr 0xA0020624										
Calibration parameter: cal_dcmwidththr										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_cal_dcmwidtht hr	rw	ro	0x4CD	Calibration param	eter: cal_dcmwid	iththr			

1.3.3	95 machineconstant	ts_ca	l_dcn	ncheckiter		Reg.	0xA0020628		
Calibration parameter: cal_dcmcheckiter									
bits	name	s/w	h/w	default		description	n		
31:0	machineconstant s_cal_dcmchecki ter	rw	ro	0x4	Calibration parame	eter: cal_dcmche	eckiter		

1.3.3	.3.396 machineconstants_cal_ddmcheckiter 0xA002062C									
Calibration parameter: cal_ddmcheckiter										
bits	name	s/w	h/w	default		description	n			
31:0	machineconstant s_cal_ddmchecki ter	rw	ro	0x4	Calibration param	eter: cal_ddmche	eckiter			

1.3.3	97 machineconstan	Reg.	0xA0020630					
To support KPI phase 3. Target Coalescence								
bits	name	s/w	h/w	default		description	n	
31:0	machineconstant s_cal_targetcl	rw	ro	0x12C	To support KPI pl	nase 3. Target Co	palescence	

1.3.3	1.3.398 machineconstants_cal_targetsubcl_initial 0xA0020634										
Calibration parameter: cal_targetsubcl_initial											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_targetsub cl_initial	rw	ro	0x1E	Calibration param	eter: cal_targetsu	ubcl_initial				

1.3.3	99 machineconstan	ts_ca	l_targ	getsubcl_re	es	Reg.	0xA0020638
Calib	ration parameter: cal_targ	etsubcl	_res				
bits	name	s/w	h/w	default		descriptio	n
31:0	machineconstant s_cal_targetsub cl_res	rw	ro	0x14	Calibration param	neter: cal_targetsu	ubcl_res

1.3.4	00 machineconstan	ts_ca	l_targ	getsubcl_ni	um	Reg.	0xA002063C	
Calib	ration parameter: cal_targ	etsubcl	_num					
bits	name	s/w	h/w	default		description	า	
31:0	machineconstant s_cal_targetsub cl_num	rw	ro	0x2	Calibration parameter: cal_targetsubcl_num			

1.3.4	3.401 machineconstants_cal_targetscl_optimized 0xA0020640										
To support KPI phase 3. Target Sub-Coalescence Optimized											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_targetscl _optimized	rw	ro	0x22	To support KPI ph mized	ase 3. Target Su	b-Coalescence Opti-				

1.3.4	02 machineconstant	Reg.	0xA0020644						
Calibration parameter: cal_tferrthr									
bits	name	s/w	h/w	default		description	n		
31:0	machineconstant s_cal_tferrthr	rw	ro	0x8000	Calibration param	eter: cal_tferrthr			

1.3.4	03 machineconstan	ts_ca	l_tota	alvoltage		Reg.	0xA0020648		
Calibration parameter: cal_totalvoltage									
bits	name	s/w	h/w	default		descriptio	n		
31:0	machineconstant s_cal_totalvolt age	rw	ro	0x10400	Calibration param	neter: cal_totalvoli	tage		

1.3.4	3.404 machineconstants_cal_cost_weight_p0 0xA002064C										
Calibration parameter: cal_cost_weight_p0											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_cost_weig ht_p0	rw	ro	0x10000	Calibration param	eter: cal_cost_we	eight_p0				

1.3.405 machineconstants_cal_cost_weight_p1 0xA0020650											
Calibration parameter: cal_cost_weight_p1											
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_cal_cost_weig	rw	ro	0x10000	Calibration param	eter: cal_cost_we	eight_p1				

1.3.406 machineconstants_cal_cost_weight_p2 0xA0020654											
Calibration parameter: cal_cost_weight_p2											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_cal_cost_weig ht_p2	rw	ro	0x10000	Calibration param	on parameter: cal_cost_weight_p2					

1.3.4	07 machineconstant	Reg.	0xA0020658									
Calib	Calibration parameter: cal_cost_weight_p3											
bits	bits name s/w h/w default description											
31:0	machineconstant s_cal_cost_weig ht_p3	rw	ro	0x10000	Calibration parameter: cal_cost_weight_p3							

1.3.408 machineconstants_cal_cost_weight_p4 0xA002065C											
Calibration parameter: cal_cost_weight_p4											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_cost_weig ht_p4	rw	ro	0x10000	Calibration param	tion parameter: cal_cost_weight_p4					

1.3.409 machineconstants_cal_cost_weight_p5 0xA0020660											
Calibration parameter: cal_cost_weight_p5											
bits	name	s/w	h/w	default		description	า				
31:0	machineconstant s_cal_cost_weig ht_p5	rw	ro	0x10000	Calibration parameter: cal_cost_weight_p5						

1.3.4	1.3.410 machineconstants_cal_costfunctiondswthr 0xA0020664											
Calibration parameter: cal_costfunctiondswthr												
bits	name	name s/w h/w default description										
31:0	machineconstant s_cal_costfunct iondswthr	rw	ro	0xCCCD	Calibration param	meter: cal_costfunctiondswthr						

1.3.411 machineconstants_cal_costfunctionhwthr 0xA0020668											
Calibration parameter: cal_costfunctionhwthr											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_costfunct ionhwthr	rw	ro	0xCCCD	Calibration param	eter: cal_costfun	ctionhwthr				

1.3.4	1.3.412 machineconstants_cal_freqdiagnosticnumber 0xA002066C											
Calib	Calibration parameter: cal_freqdiagnosticnumber											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_cal_freqdiagn osticnumber	rw	ro	0x3	Calibration param	alibration parameter: cal_freqdiagnosticnumber						

1.3.4	1.3.413 machineconstants_cal_freqdiagnosticres 0xA0020670											
Calibration parameter: cal_freqdiagnosticres												
bits	name	s/w	h/w	default		descriptio	n					
31:0	machineconstant s_cal_freqdiagn	rw	ro									

osticres			

1.3.4	1.3.414 machineconstants_cal_maindropletdiameter 0xA0020674											
Diam	Diameter for main droplets in um											
bits	name	s/w	h/w	default		description	n					
31:0	machineconstant s_cal_maindropl etdiameter	rw	ro	0x1B4CCD	Diameter for main	droplets in um						

1.3.415 machineconstants_cal_maindropletvelocity 0xA0020678											
Main droplet velocity											
bits	name	s/w	h/w	default		description	n				
31:0	machineconstant s_cal_maindropl etvelocity	rw	ro	0x820000	Main droplet velo	city					

1.3.4 cm	1.3.416 machineconstants_cal_satellitediametermind cm 0xA002067C											
Calib	Calibration parameter: cal_satellitediametermindcm											
bits	name	s/w	h/w	default		description	า					
31:0	· ·											

1.3.4 dm	1.3.417 machineconstants_cal_satellitediametermind 0xA0020680											
Calib	Calibration parameter: cal_satellitediameterminddm											
bits	name	s/w	h/w	default		description	า					
31:0	machineconstant s_cal_satellite diameterminddm	onstant rw ro 0x60000 Calibration parameter: cal_satellitediameterminddm										

1.3.4	18 machineconstant	Reg.	0xA0020684						
DCM location									
bits	name	s/w	h/w	default		description	n		
31:0	machineconstant s_cal_dcmlocati on	rw	ro	0x46	DCM location				

1.3.4	19 machineconsta	Reg.	0xA0020688								
TF Error ratio threshold											
bits	name	s/w	h/w	default		descr	ription				
31:0	machineconstant s_cal_errorrati othreshold	rw	ro	0x8000	TF Error ratio thre	shold					

1.3.420 machineconstants_cal_bdo_dc_res 0xA002068C										
Duty Cycle resolution while performing BDO scan										
bits	bits name s/w h/w default description									

31:0	machineconstant s_cal_bdo_dc_re s	rw	ro	0xA	Duty Cycle res	solution while p	performing BDO scan
1.3.4	21 machineconstar	nts_ca	l_dra	gcte		Reg.	0xA0020690
Drag	coefficient						
bits	name	s/w	h/w	default		des	cription
31:0	machineconstant s_cal_dragcte	rw	ro	0x1	Drag coefficie	nt	
1.3.4	22 machineconstar	nts_cal	l_nuı	m_candida	te_soln	Reg.	0xA0020694
Numl	ber of candidate solutions	S					
bits 31:0	name machineconstant s_cal_num_candi date_soln	s/w rw	h/w ro	default 0x15	Number of car	des ndidate solution	cription ns
	23 machineconstar	nts_cal	l_spo	cfg_4		Reg.	0xA0020698
bits	name	s/w	h/w	default		das	cription
31:0	machineconstant s_cal_spcfg_4	rW	ro	0x7	cal_dcm_qual		Cilption
1.3.4	24 machineconstar	nts_ca	l_spo	ofg_5		Reg.	0xA002069C
cal_ta	argetsubcl_num_MX						
bits	name	s/w	h/w	default			cription
31:0	machineconstant s_cal_spcfg_5	rw	ro	0x1	cal_targetsub	cl_num_MX	
	25 machineconstar	nts_ca	l_spo	cfg_6		Reg.	0xA00206A0
	argetsubcl_res_MX						
bits	name	s/w	h/w	default	ool torgeteral		cription
31:0	machineconstant s_cal_spcfg_6	rw	ro	0x14	cal_targetsub	ci_res_IVIX	
1 3 /	26 machineconstai	nts cal	l ma	infregont (	tyne	Reg.	0xA00206A4
Main		ype: 0-M		–	•		on failure; 1-Only main freq
bits	name	s/w	h/w	default		des	cription
31:0	machineconstant s_cal_mainfreqo pt_type	rw	ro	0x0		y optimization	type: 0-Main freqiency opti- ation on failure; 1-Only main

1.3.4	27 machineconsta	Reg.	0xA00206A8								
cal_n	cal_mainfreqopt_type_MX										
bits	name	s/w	h/w	default		description	١				
31:0 machineconstant rw ro 0x1 cal_mainfreqopt_type_MX s_cal_spcfg_8											

1.3.428 machineconstants_cal_pkuniformitymax 0xA00206AC											
Maximum peakuniformity											
bits	name	s/w	h/w	default		descriptio	n				
31:0	machineconstant s_cal_pkuniform itymax	rw	ro	0x199A	Maximum peakuniformity						

1.3.4	29 machineconstant	Reg.	0xA00206B0								
cal_n	cal_num_candidate_soln_MX										
bits	name	s/w	h/w	default		description	٦				
31:0 machineconstant rw ro 0x1 cal_num_candidate_soln_MX s_cal_spcfg_10											

1.3.4	30 machineconstant	Reg.	0xA00206B4									
cal_ta	cal_targetsubcl_initial_MX											
bits	name	s/w	h/w	default		description	n					
31:0 machineconstant rw ro 0x1E cal_targetsubcl_initial_MX s_cal_spcfg_11												

1.3.4	31 machineconstan	Reg.	0xA00206B8							
Calibration parameter: cal_spcfg_12										
bits	name	s/w	h/w	default		description	n			
31:0 machineconstant rw ro 0x0 Calibration parameter: cal_spcfg_12										

1.3.4	32 machineconstant	Reg.	0xA00206BC							
Jump boundary delay										
bits	bits name s/w h/w default description									
31:0	machineconstant s_cal_jmpbnddel ay	rw	ro	0x1	Jump boundary d	elay				

1.3.4	1.3.433 machineconstants_cal_spcfg_14 0xA00206C0											
cal_monitoringqualcheckcountermax												
bits	name	s/w	h/w	default		description	n					
31:0												

1.3.4	34 machineconstant	Reg.	0xA00206C4								
Calib	Calibration parameter: cal_spcfg_15										
bits	name	s/w	h/w	default		description	า				
31:0 machineconstant rw ro 0x0 Calibration parameter: cal_spcfg_15 s_cal_spcfg_15											

1.3.435 machineconstants_cal_spcfg_16	Reg.	0xA00206C8
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Calibration parameter: cal_spcfg_16									
bits	name	s/w	h/w	default	description				
31:0	machineconstant s_cal_spcfg_16	rw	ro	0x0	Calibration parameter: cal_spcfg_16				

## 1.4 algo\_egr\_registers\_srdl OxA0030000 - OxA003D07F Register map of the egress algo registers

1.4.1	algo_egress_modu	Reg.	0xA0030000								
Defin	Defines the module name										
bits	bits name s/w h/w default description										
31:0	module_name	ASCII code for mo	odule name - top	module(core) = core							

1.4.2	algo_egress_mo	Reg.	0xA0030004							
Module version										
bits	name	s/w	h/w	default		desc	cription			
31:16	rfu	ro	na	0x0	Reserved for Futi	ure Use - RF	-U			
15:8	major_revision	ro	na	0x0	Major Revision					
7:0 minor_revision ro na 0x0 Minor Revision										

1.4.3	algo_egress_pag	ge_prop		Reg.	0xA0030008						
Address page properties											
bits name s/w h/w default description											
31	present	ro	WO	0x1	Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not.						
30:16	rfu	ro	na	0x0	Reserver for Futu	re Use - RFU					
15:8	page_size	ro	na	0x10	Address page siz value to 4k and e		BkB, etc. Divide the real				
7:0	unified_header_ rev	ro	na	0x1	Unified Header Fo	ormat common re	gisters revision.				

1.4.4	algo_egress_scrato	Reg.	0xA003000C								
Scrat	Scratchregister register										
bits	bits name s/w h/w default description										
31:0	scratchregister	SW can write to it	and read from it f	for test purposes.							

1.4.5	algo_egress_irq_er	Reg.	0xA0030010							
Interrupt Requests Enable/Mask Control Register										
bits	name	s/w	h/w	default		description	٦			
0	irq0_enable	rw	ro	0x0	IRQ0 enable bit. Not implemented here/DTEC					
1	irq1_enable	rw	IRQ1 enable bit.	Not implemented I	here/DTEC					

1.4.6 alg	go_egress_irq_ <sub> </sub>	Reg.	0xA0030014							
Interrupt	Interrupt Pending Status Register									
bits	name	des	scription							

0	irq0_pending	r/w1c	WO	0x0	IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC
1	irq1_pending	r/w1c	wo	0x0	IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts
					interrupt on positive edge. Not implemented here/DTEC

1.4.7	algo_egress_irq_ra	Reg.	0xA0030018							
Interrupt Raw Status Register										
bits	name	s/w	h/w	default		description	า			
0	irq0_raw	ro	wo	0x0	IRQ0 raw status b	it. Not implement	ed here/DTEC			
1	irq1_raw	ro	wo	0x0	IRQ1 raw status b	it. Not implement	ed here/DTEC			

1.4.8	algo_egress_irq_fo	Reg.	0xA003001C						
Interrupt Force Control Register									
bits	name	s/w	h/w	default	description				
0	irq0_force	rw	ro	0x0	IRQ0 force bit. SV '0' to clear. Not im		nulate an interrupt. Write DTEC		
1	irq1_force	rw	ro	0x0	IRQ1 force bit. SV '0' to clear. Not im		nulate an interrupt. Write DTEC		

1.4.9	region_1_start_tag	Reg.	0xA0031000										
regio	region_1_start_tag												
bits	name	s/w	h/w	default		description	١						
31:0	region_1_start_ tag	ro	wo	X	region_1_start_ta	g							

1.4.1	0 region_1_dtec_too	0xA0031004											
regio	region_1_dtec_tod_lsbs												
bits	name	s/w	h/w		default		descript	ion					
31:0 region_1_dtec_t ro wo X region_1_dtec_tod_lsbs od_lsbs													

1.4.1	1 region_1_dtec_too	Reg.	0xA0031008									
region_1_dtec_tod_msbs												
bits	name	s/w	h/w	default		description	า					
31:0	31:0 region_1_dtec_t ro wo X region_1_dtec_tod_msbs											

1.4.1	2 region_1_dtec_lts	Reg.	0xA003100C										
regio	region_1_dtec_lts												
bits	name	s/w	h/w	default		description	٦						
31:0	31:0 region_1_dtec_l ro wo X region_1_dtec_lts												

1.4.1	3 dtec_algo_rev_rev	Reg.	0xA0031010										
Majo	Major version												
bits	name	s/w	h/w	default		description	١						
31:0	31:0 dtec_algo_rev_r ro wo X Major version evision_major												

1.4.1	4 dtec_algo_rev_rev	vision	_min	or		Re		0xA0031014
Mino	r version							
bits	name	s/w	h/w		default		descriptio	n
31:0	dtec_algo_rev_r evision_minor	ro	wo	X		Minor version		
1.4.1	5 dtec_algo_rev_rev	vision	_pat	ch		Re	g.	0xA0031018
Patch	n version							
bits	name	s/w	h/w		default		descriptio	n
31:0	dtec_algo_rev_r evision_patch	ro	wo	X		Patch version		
	6 spares_spare_uin	it_1				Re	g.	0xA003101C
•	e unsigned integer	,						
bits 31:0	name	s/w	h/w wo	X	default	Spare unsigned integ	descriptio	n
) I.U	spares_spare_ui nt_1	ro	WO	^		Spare unsigned inte	y <del>o</del> i	
	7 spares_spare_uin	t_2				Re	g.	0xA0031020
-	e unsigned integer							
bits	name	s/w	h/w	V	default	0	descriptio	n
31:0	spares_spare_ui nt_2	ro	WO	X		Spare unsigned integ	ger	
4.4.4	0	4.0				•		0×40004004
1.4.1	8 spares_spare_uin	t_3				Re	.g.	0xA0031024
Spar	e unsigned integer							
	name	s/w			default		descriptio	n
31:0	spares_spare_ui nt_3	ro	WO	X		Spare unsigned inte	ger	
1.4.1	9 spares_spare_uin	t_4				Re	g.	0xA0031028
Spar	e unsigned integer							
bits	name	s/w	h/w		default		descriptio	n
31:0	spares_spare_ui nt_4	ro	WO	Χ		Spare unsigned integ	ger	
	IN_T							
1.4.2	0 spares_spare_uin	t_5				Re	·g.	0xA003102C
	e unsigned integer							
bits	name	s/w	h/w		default		descriptio	n
31:0	spares_spare_ui nt_5	ro	WO	X		Spare unsigned inte		
1.4.2	1 spares_spare_uin	t_6				Re	g.	0xA0031030
Spar	e unsigned integer							

name

s/w h/w

description

31:0	spares_spare_ui nt_6	ro	WO	X		Spare unsigned in	teger	
	_							
1.4.2	2 spares_spare_uint	t_ <b>7</b>				i	Reg.	0xA0031034
Spar	e unsigned integer							
bits	name	s/w	h/w		default		(	description
31:0	spares_spare_ui nt_7	ro	WO	X		Spare unsigned in		
1.4.2	3 spares_spare_uin	t_8				ı	Reg.	0xA0031038
Spar	e unsigned integer							
bits	name	s/w	h/w		default		(	description
31:0	spares_spare_ui nt_8	ro	wo	X		Spare unsigned in		
1.4.2	4 spares_spare_uin	t_9				ī	Reg.	0xA003103C
	e unsigned integer							
bits	name	s/w	h/w		default		,	description
31:0	spares_spare_ui	ro	WO	Χ	uciauli	Spare unsigned in		GOOGIPHOH
5 0	nt_9		****			Sparo andigned in	901	
1.4.2	5 spares_spare_uin	t_10				i	Reg.	0xA0031040
Spar	e unsigned integer							
bits	name	s/w	h/w		default		(	description
31:0	spares_spare_ui	ro	wo	Χ		Spare unsigned in		·
	nt_10							
1.4.2	6 spares_spare_uin	t_11				ı	Reg.	0xA0031044
Spar	e unsigned integer							
bits	name	s/w	h/w		default			description
31:0	spares_spare_ui nt_11	ro	WO	X		Spare unsigned in	teger	
1.4.2	7 spares_spare_uint	12					Reg.	0xA0031048
	e unsigned integer							
bits	name	s/w	h/w		default		,	description
31:0	spares_spare_ui	ro	WO	Χ	u <del>c</del> iauit	Spare unsigned in		uesonption
J	nt_12		0			2 can a ranging in	901	
1.4.2	8 spares_spare_uin	t_13				ı	Reg.	0xA003104C
Spar	e unsigned integer							
bits	name	s/w	h/w		default		(	description
31:0	spares_spare_ui nt_13	ro	WO	X		Spare unsigned in		
1.4.2	9 spares_spare_uint	t_14					Reg.	0xA0031050

Spare	Spare unsigned integer												
bits	name	s/w	h/w	default	description								
31:0	spares_spare_ui nt_14	ro	wo	X	Spare unsigned integer								

1.4.3	0 spares_spare_uin	Reg.	0xA0031054								
Spare unsigned integer											
bits	name	s/w	h/w	default		description	1				
31:0 spares_spare_ui ro wo X Spare unsigned integer nt_15											

1.4.3	1 spares_spare_uin	Reg.	0xA0031058									
Spare	Spare unsigned integer											
bits	name	s/w	h/w	default		description	ı					
31:0 spares_spare_ui ro wo X Spare unsigned integer nt_16												

1.4.3	2 spares_spare_int_	Reg.	0xA003105C									
Spare	Spare signed integer											
bits	name	s/w	h/w	default		description	n					
31:0	31:0 spares_spare_in ro wo X Spare signed integer t_1											

1.4.3	3 spares_spare_in	Reg.	0xA0031060								
Spare signed integer											
bits	name	s/w	h/w	default		description	า				
31:0 spares_spare_in ro wo X Spare signed integer t_2											

1.4.3	4 spares_spare_int_	Reg.	0xA0031064									
Spare signed integer												
bits	name	s/w	h/w	default		description						
31:0	spares_spare_in t_3	ro	wo	X	Spare signed inte	ger						

1.4.3	5 spares_spare_int	Reg.	0xA0031068								
Spare signed integer											
bits	name	s/w	h/w	default		description	1				
31:0	spares_spare_in t_4	ro	WO	X	Spare signed inte	ger					

1.4.3	6 spares_spare_ir	Reg.	0xA003106C									
Spare signed integer												
bits	name	s/w	h/w	default		description	n					
31:0	spares_spare_in t_5	ro	wo	Х	Spare signed inte	ger						

	spares_spare_in	t_6				Reg.	0xA0031070
Spare	signed integer						
bits	name	s/w	h/w		default		description
	spares_spare_in :_6	ro	WO	X		Spare signed integer	
1.4.38	spares_spare_in	t_7				Reg.	0xA0031074
Spare	signed integer						
bits	name	s/w	h/w		default		description
	spares_spare_in :_7	ro	WO	X		Spare signed integer	
1.4.39	spares_spare_in	t_8				Reg.	0xA0031078
	signed integer						
bits	name	s/w	h/w		default		description
31:0	spares_spare_in :_8	ro	WO	X		Spare signed integer	
1.4.40	spares_spare_in	t 9				Reg.	0xA003107C
	signed integer					lucione de la constante de la	
bits	name	s/w	h/w		default		description
31:0	spares_spare_in i_9	ro	WO	X	aciaaii	Spare signed integer	accomplion
	spares_spare_in	t_10				Reg.	0xA0031080
	signed integer						
31:0	name spares_spare_in i_10	s/w ro	h/w wo	X	default	Spare signed integer	description
1.4.42	spares_spare_in	t_11				Reg.	0xA0031084
Spare	signed integer						
bits	name	s/w	h/w		default		description
	spares_spare_in :_11	ro	WO	X		Spare signed integer	
1.4.43	spares_spare_in	t_12				Reg.	0xA0031088
Spare	signed integer						
bits	name	s/w	h/w		default		description
	spares_spare_in i_12	ro	WO	X		Spare signed integer	
1.4.44	spares spare in	t 13				Reg.	0xA003108C
	spares_spare_in	t_13				Reg.	0xA003108C
	spares_spare_in	t_13	h/w		default		0xA003108C

Spare signed integer	31:0	spares_spare_in t_13	ro	WO	Χ		Spare signed integer	
Spare signed integer bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_in ro wo X Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w default Spare unsigned fixed point bits name s/w h/w Spare unsigned fixed point								
bits name s/w h/w default description  1.4.46 spares_spare_in to wo X Spare signed integer  1.4.46 spares_spare_int 15	1.4.4	5 spares_spare_int <sub>_</sub>	_14				Reg.	0xA0031090
31.0 spares_spare_in to wo X Spare signed integer  1.4.46 spares_spare_int_15  Spare signed integer  bits	Spar	e signed integer						
1.4.46 spares_spare_int_15  Spare signed integer bits	bits	name	s/w	h/w		default		description
Spare signed integer bits name s/w h/w default Spare signed integer  1.4.47 spares_spare_in t_15  1.4.47 spares_spare_in t_16  Spare signed integer bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_in t_16  1.4.48 spares_spare_in t_16  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf i_1  1.4.49 spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf i_2  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point Spares_spare_uf ro wo X	31:0		ro	WO	X		Spare signed integer	
Spare signed integer bits name s/w h/w default Spare signed integer  1.4.47 spares_spare_in t_15  1.4.47 spares_spare_in t_16  Spare signed integer bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_in t_16  1.4.48 spares_spare_in t_16  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf i_1  1.4.49 spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf i_2  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default spares_spare_uf ro wo X  Spare unsigned fixed point Spares_spare_uf ro wo X								
bits name s/w h/w default Spare signed integer  1.4.47 spares_spare_int_16  Spare signed integer  bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_int_16  Spare signed integer  bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_ufi_1  Spare unsigned fixed point bits name s/w h/w default spares_spare_ufi_1  1.4.49 spares_spare_ufi_1  Spare unsigned fixed point bits name s/w h/w default spares_spare_ufi_1  1.4.49 spares_spare_ufi_2  Spare unsigned fixed point bits name s/w h/w default spares_spare_ufi_1  1.4.50 spares_spare_ufi_3  Spare unsigned fixed point bits name s/w h/w default spares_spare_ufi_1  1.4.50 spares_spare_ufi_3  Spare unsigned fixed point bits name s/w h/w default spares_spare_ufi_1  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default spares_spare_ufi_2  Spare unsigned fixed point  bits name s/w h/w default spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default spares_spare_ufi_4  Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default spares_spare_ufi_4  Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  DXA00310A8  Spare unsigned fixed point	1.4.4	6 spares_spare_int_	_15				Reg.	0xA0031094
31.0 spares_spare_in t_16  1.4.47 spares_spare_int_16  Spare signed integer  bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_ufi	Spar	e signed integer						
1.4.47 spares_spare_int_16						default		description
Spare signed integer  bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_ufi_1	31:0		ro	WO	X		Spare signed integer	
bits name s/w h/w default Spare signed integer  1.4.48 spares_spare_ufi_1	1.4.4	7 spares_spare_int	_16				Reg.	0xA0031098
31:0 spares_spare_in t_16  1.4.48 spares_spare_ufi_1  Dispare unsigned fixed point bits name s/w h/w default spares_spare_uf i_2  1.4.49 spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default description  31:0 spares_spare_uf ro wo X  Spare unsigned fixed point bits name s/w h/w default description  31:0 spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w default description  1.4.51 spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w default description  Spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w default description  Spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w Spare unsigned fixed point  Spares_spare_uf ro wo X  Spare unsigned fixed point  bits name s/w h/w Spare unsigned fixed point  Spares_spare_uf ro wo X  Spare unsigned fixed point	Spar	e signed integer						
31:0 spares_spare_in t_16	bits	name	s/w	h/w		default		description
Spare unsigned fixed point bits	31:0		ro	WO	X		Spare signed integer	
1.4.49 spares_spare_ufi_2  Spare unsigned fixed point  bits	bits	name spares_spare_uf			X	default	Spare unsigned fixed po	
Spare unsigned fixed point  bits name s/w h/w default description 31:0 spares_spare_uf ro wo X Spare unsigned fixed point  1.4.50 spares_spare_ufi_3  Spare unsigned fixed point  bits name s/w h/w default description 31:0 spares_spare_uf ro wo X Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point		<u>i_</u> 1						
bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  1.4.50 spares_spare_ufi_3  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point	1.4.4	9 spares_spare_ufi	_2				Reg.	0xA00310A0
31:0 spares_spare_uf	Spar	e unsigned fixed point						
1.4.50 spares_spare_ufi_3  Spare unsigned fixed point  bits name s/w h/w default description 31:0 spares_spare_uf ro wo X  Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description  Spare unsigned fixed point  bits name s/w h/w default description 31:0 spares_spare_uf ro wo X  Spare unsigned fixed point  Spare unsigned fixed point  Spare unsigned fixed point  Spare unsigned fixed point						default		
Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  i_4	31:0		ro	WO	X		Spare unsigned fixed po	int
Spare unsigned fixed point  bits name s/w h/w default description 31:0 spares_spare_uf ro wo X Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  i_4  Spare unsigned fixed point	1.4.5	0 spares spare ufi	3				Reg	0xA00310A4
bits name s/w h/w default description 31:0 spares_spare_uf ro wo X Spare unsigned fixed point  1.4.51 spares_spare_ufi_4  Spare unsigned fixed point  bits name s/w h/w default description 31:0 spares_spare_uf ro wo X Spare unsigned fixed point  i_4  Spare unsigned fixed point  Spare unsigned fixed point  Spare unsigned fixed point								
spares_spare_uf	-		s/w	h/w		default		description
Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  i_4		spares_spare_uf			X		Spare unsigned fixed po	
Spare unsigned fixed point  bits name s/w h/w default description  31:0 spares_spare_uf ro wo X Spare unsigned fixed point  i_4								
bits name s/w h/w default description 31:0 spares_spare_uf			_4				Reg.	UXA00310A8
31:0 spares_spare_uf ro wo X Spare unsigned fixed point i_4		· ·	s/w	h/w		default		description
		spares_spare_uf			X	doladit	Spare unsigned fixed po	
1.4.52 spares_spare_ufi_5 0xA00310AC								
	1.4.5	2 spares_spare_ufi	_5				Reg.	0xA00310AC

Spare	Spare unsigned fixed point											
bits	name	s/w	h/w	default	description							
31:0	spares_spare_uf i_5	ro	wo	X	Spare unsigned fixed point							

1.4.5	3 spares_spare_ufi_	Reg.	0xA00310B0								
Spare unsigned fixed point											
bits	name	s/w	h/w	default		description	n				
31:0	spares_spare_uf i_6	ro	WO	X	Spare unsigned fi	xed point					

1.4.5	4 spares_spare_ufi_	Reg.	0xA00310B4									
Spare	Spare unsigned fixed point											
bits	name	s/w	h/w		default		description	١				
31:0	spares_spare_uf i_7	ro	WO	X		Spare unsigned fi	xed point					

1.4.5	5 spares_spare_ufi	Reg.	0xA00310B8								
Spare unsigned fixed point											
bits	name	s/w	h/w	default		description	n				
31:0	spares_spare_uf i_8	ro	WO	X	Spare unsigned fi	xed point					

1.4.5	6 spares_spare_ufi_	Reg.	0xA00310BC								
Spare unsigned fixed point											
bits	name	s/w	h/w	default		description	า				
31:0	spares_spare_uf i_9	ro	wo	X	Spare unsigned fi	xed point					

1.4.5	7 spares_spare_ufi_	Reg.	0xA00310C0									
Spare unsigned fixed point												
bits	name	s/w	h/w	default		description	٦					
31:0	spares_spare_uf i_10	ro	WO	Х	Spare unsigned fi	xed point						

1.4.5	8 spares_spare_ufi_	Reg.	0xA00310C4								
Spare unsigned fixed point											
bits	name	s/w	h/w	default		description	า				
31:0 spares_spare_uf ro wo X Spare unsigned fixed point i_11											

1.4.5	9 spares_spare_uf	i_12				Reg.	0xA00310C8
Spare	e unsigned fixed point						
bits	name	s/w	h/w	default		description	n
31:0	spares_spare_uf i_12	ro	wo	X	Spare unsigned fi	xed point	

¬nar	o uppigned fixed						
-	e unsigned fixed point	,	/		1.6.16		•
bits 1:0	name spares_spare_uf	s/w ro	h/w wo	X	default	Spare unsigned fixed point	cription
	i_13					Spare analytica fixed point	
1.4.6	61 spares_spare_ufi	_14				Reg.	0xA00310D0
Spar	e unsigned fixed point						
bits	name	s/w	h/w		default	desc	cription
31:0	spares_spare_uf i_14	ro	WO	X		Spare unsigned fixed point	
1.4.6	2 spares_spare_ufi	_15				Reg.	0xA00310D4
Spar	e unsigned fixed point						
bits	name	s/w	h/w		default		cription
31:0	spares_spare_uf i_15	ro	WO	X		Spare unsigned fixed point	
1 1 6	3 spares_spare_ufi	16				Reg.	0xA00310D8
	e unsigned fixed point	_10				******	5.2.10001000
bits	name	s/w	h/w		default	dos	cription
31:0	spares_spare_uf i_16	ro	WO	X	ueraun	Spare unsigned fixed point	сприоп
1 4 6	A anama anama afi	4				Ren	0xA00310DC
	64 spares_spare_sfire signed fixed point	_'				Reg.	02/10001000
bits	name	s/w	h/w		default	desc	cription
31:0	spares_spare_sf i_1	ro	WO	X	dolddit	Spare signed fixed point	onpuon
1 / 6	55 spares_spare_sfi	2				Reg.	0xA00310E0
							5.2.10001020
-	e signed fixed point	c/:··	h/		default	.l	orintian
bits 31:0	name spares_spare_sf i_2	s/w ro	h/w wo	X	uelault	Spare signed fixed point	cription
1 4 0	Congress of the congress of th	2				Ren	0xA00310E4
	66 spares_spare_sfi	_3				Reg.	UAAUU3 10E4
	e signed fixed point	- L	I- 1		al a f = ! f		a win 4: a m
bits	name spares_spare_sf	s/w ro	h/w wo	X	default	Spare signed fixed point	cription
31:0	i_3		0				
31:0							
31:0 1.4.6	67 spares_spare_sfi	_4				Reg.	0xA00310E8

name

s/w

h/w

description

31:0	spares_spare_sf i_4	ro	wo	X		Spare signed fixe	ed point	
1.4.6	8 spares_spare_sfi	_5					Reg.	0xA00310EC
Spar	e signed fixed point							
bits	name	s/w	h/w		default		des	cription
31:0	spares_spare_sf i_5	ro	WO	X		Spare signed fixe	ed point	
1.4.6	9 spares_spare_sfi	_6					Reg.	0xA00310F0
Spar	e signed fixed point							
bits	name	s/w	h/w		default			cription
31:0	spares_spare_sf i_6	ro	WO	X		Spare signed fixe	ed point	
1.4.7	0 spares_spare_sfi	_7					Reg.	0xA00310F4
Spar	e signed fixed point							
bits	name	s/w	h/w		default			cription
31:0	spares_spare_sf i_7	ro	WO	X		Spare signed fixe	ed point	
147	1 spares_spare_sfi	8					Reg.	0xA00310F8
	e signed fixed point							
bits	name	s/w	h/w		default		des	cription
31:0	spares_spare_sf i_8	ro	WO	X		Spare signed fixe	ed point	
1.4.7	2 spares_spare_sfi	_9					Reg.	0xA00310FC
Spar	e signed fixed point							
bits	name	s/w	h/w		default		des	cription
31:0	spares_spare_sf i_9	ro	WO	X		Spare signed fixe		
	2	40					Reg	0v40031100
	3 spares_spare_sfi	_10					Reg.	0xA0031100
	e signed fixed point	,	, ,					
bits 31:0	name spares_spare_sf	s/w ro	h/w wo	Χ	default	Spare signed fixe		cription
71.0	i_10	10	WO			Opare signed lixe	ou point	
1.4.7	4 spares_spare_sfi	_11					Reg.	0xA0031104
Spar	e signed fixed point							
bits	name	s/w	h/w		default			cription
31:0	spares_spare_sf i_11	ro	wo	X		Spare signed fixe	ed point	
1 4 7	5 spares_spare_sfi	12					Reg.	0xA0031108

Spare	e signed fixed point				
bits	name	s/w	h/w	default	description
31:0	spares_spare_sf i_12	ro	wo	X	Spare signed fixed point

1.4.7	6 spares_spare_sfi_	_13				Reg.	0xA003110C
Spare	e signed fixed point						
bits	name	s/w	h/w	default		description	n
31:0	spares_spare_sf i_13	ro	wo	X	Spare signed fixe	d point	

1.4.7	7 spares_spare_sfi_	14				Reg.	0xA0031110
Spare	e signed fixed point						
bits	name	s/w	h/w	default		description	n
31:0	spares_spare_sf i_14	ro	WO	X	Spare signed fixe	d point	

1.4.7	8 spares_spare_sfi	_15				Reg.	0xA0031114
Spare	e signed fixed point						
bits	name	s/w	h/w	default		descriptio	n
31:0	spares_spare_sf i_15	ro	WO	X	Spare signed fixe	d point	

1.4.7	9 spares_spare_sfi_	16				Reg.	0xA0031118
Spare	e signed fixed point						
bits	name	s/w	h/w	default		description	n
31:0	spares_spare_sf i_16	ro	WO	X	Spare signed fixe	d point	

1.4.80	0 region_1_end_tag					Reg.	0xA003111C
region	n_1_end_tag						
bits	name	s/w	h/w	default		description	n
31:0	region_1_end_ta g	ro	wo	X	region_1_end_tag	)	

1.4.8	1 region_4_start_tag	J				Reg.	0xA0034000
regio	n_4_start_tag						
bits	name	s/w	h/w	default		description	١
31:0	region_4_start_ tag	ro	wo	X	region_4_start_ta	g	

1.4.8	2 region_4_dtec_too	d_lsbs	S			Reg.	0xA0034004
region	n_4_dtec_tod_lsbs						
bits	name	s/w	h/w	default		description	n
31:0	region_4_dtec_t od_lsbs	ro	WO	X	region_4_dtec_to	d_lsbs	

regio								
hits	on_4_dtec_tod_msbs							
		s/w	h/w		default			scription
31:0	region_4_dtec_t od_msbs	ro	WO	X		region_4_dtec_to	d_msbs	
1.4.8	34 region_4_dtec_lt	ts					Reg.	0xA003400C
regio	on_4_dtec_lts							
bits		s/w	h/w		default			cription
31:0	region_4_dtec_l ts	ro	wo	X		region_4_dtec_lts	3	
1.4.8	35 dcm_fb_metrics	_fb_lm					Reg.	0xA0034010
Medi	ian of L							
bits		s/w	h/w		default		des	scription
31:0	dcm_fb_metrics_ fb_lm	ro	WO	X		Median of L		
	fb_lm							
1 / 5	86 dcm_fb_metrics	fh tm					Reg.	0xA0034014
		_וט_נווו						0,3 1000 10 17
	ian of T							
bits		s/w	h/w	V	default	Median of T	des	scription
31:0	dcm_fb_metrics_ fb_tm	ro	WO	X		iviedian of 1		
1.4.8	37 dcm_fb_metrics	_fb_cm					Reg.	0xA0034018
Med	ian of C							
bits	name	s/w			default		des	scription
		s/w ro	h/w wo		default	Median of C	des	scription
bits	name dcm_fb_metrics_				default		des	scription
bits 31:0	name dcm_fb_metrics_	ro	WO		default		des	0xA003401C
bits 31:0	name dcm_fb_metrics_ fb_cm	ro	WO		default			
bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D	ro	WO		default		Reg.	
bits 31:0 1.4.8 Medi	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_	ro _fb_dm	wo	X			Reg.	0xA003401C
bits 31:0 1.4.8 Medi	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name	ro _fb_dm	wo	X		Median of C	Reg.	0xA003401C
bits 31:0 1.4.8 Medi bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_ fb_dm	_fb_dm	h/w wo	X		Median of C	Reg.	0xA003401C scription
bits 31:0 1.4.8 Medi bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_ fb_dm  89 dcm_fb_metrics_	_fb_dm	h/w wo	X		Median of C	Reg.	0xA003401C
bits 31:0 1.4.8 Medi bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_ fb_dm  89 dcm_fb_metrics_ of L	ro  _fb_dm s/w ro	h/w wo	X	default	Median of C	des	0xA003401C scription 0xA0034020
bits 31:0 1.4.8 Medi bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_ fb_dm  89 dcm_fb_metrics_ of L  name	ro  _fb_dm  s/w ro  _sigma	h/w wo	X		Median of C  Median of D	des	0xA003401C scription
bits 31:0 1.4.8 Medi bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_ fb_dm  89 dcm_fb_metrics_ of L	ro  _fb_dm s/w ro	h/w wo	X	default	Median of C	des	0xA003401C scription 0xA0034020
bits 31:0 1.4.8 Medi bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_ fb_dm  89 dcm_fb_metrics_ of L  name dcm_fb_metrics_	ro  _fb_dm  s/w ro  _sigma	h/w wo	X	default	Median of C  Median of D	des	0xA003401C scription 0xA0034020
bits 31:0  1.4.8  Medi bits 31:0  1.4.8  Std c bits 31:0	name dcm_fb_metrics_ fb_cm  88 dcm_fb_metrics_ ian of D  name dcm_fb_metrics_ fb_dm  89 dcm_fb_metrics_ of L  name dcm_fb_metrics_	s/w ro	h/w wo	X	default	Median of C  Median of D	des	0xA003401C scription 0xA0034020

name

s/w h/w

description

31:0	dcm_fb_metrics_ sigmat	ro	wo	X		std of T		
1.4.9	1 dcm_fb_metrics_s	sigma	IC				Reg.	0xA0034028
std o	f C							
bits	name	s/w	h/w		default		des	cription
31:0	dcm_fb_metrics_ sigmac	ro	WO	X		std of C		
1 4 9	2 dcm_fb_metrics_s	siama	nd				Reg.	0xA003402C
std o		Sigina	IG					0,4 1000 1020
		0/11	b/w		dofoult		doo	orintian
bits 31:0	name dcm_fb_metrics_ sigmad	s/w ro	h/w wo	X	default	std of D	des	cription
1.4.9	3 dcm_fb_metrics_	maind	Irople	etn	umber		Reg.	0xA0034030
# ma	in-droplets							
bits	name	s/w	h/w		default		des	cription
31:0	dcm_fb_metrics_ maindropletnumb er	ro	wo	X		# main-droplets		
1.4.9	4 dcm_fb_metrics_	presu	bnun	nbe	er		Reg.	0xA0034034
# pre	-sub-coalesced droplets							
bits	name	s/w	h/w		default			cription
31:0	dcm_fb_metrics_ presubnumber	ro	wo	X		# pre-sub-coales	ced droplets	S
1.4.9	5 dcm_fb_metrics_	multp	resul	bηι	ımber		Reg.	0xA0034038
# dro	plets with more than 1 pre	e-sub-co	oalesc	ed c	Iroplets			
bits	name	s/w	h/w		default		des	cription
31:0	dcm_fb_metrics_ multpresubnumbe r	ro	wo	X		# droplets with m	ore than 1 p	ore-sub-coalesced droplets
1.4.9	6 dcm_fb_metrics_l	leftpe	akmi	SSE	dnumbe	er	Reg.	0xA003403C
# no	intermediate droplets befo	ore antii	node/ a	# ma	ain droplet	S		
bits	name	s/w	h/w		default			cription
31:0	dcm_fb_metrics_ leftpeakmissedn umber	ro	wo	X		# no intermediate	e droplets b	efore antinode/ # main droplets
		_						
1.4.9	7 dcm_fb_metrics_i	rightp	eakn	niss	sednum	ber	Reg.	0xA0034040
# no	intermediate droplets afte	r antino	de/# ı	mair	n droplets			
bits	name	s/w	h/w		default			cription
31:0	dcm_fb_metrics_ rightpeakmissed number	ro	wo	X		# no intermediate	e droplets at	fter antinode/ # main droplets

1.4.9	1.4.98 dcm_fb_metrics_timestamp_tod_lsb 0xA0034044												
Time	Time of Day register. it increments at 8ns resolution for the first PDS packet												
bits	name	s/w	h/w		default		description	٦					
31:0	dcm_fb_metrics_ timestamp_tod_l sb	ro	WO	X		Time of Day regis first PDS packet	me of Day register. it increments at 8ns resolution for the						

1.4.9	9 dcm_fb_metrics_t	Reg.	0xA0034048									
Time of Day register. it increments at 8ns resolution for the first PDS packet												
bits	name	s/w	h/w		default		description	n				
31:0	dcm_fb_metrics_ timestamp_tod_m sb	ro	wo	X		Time of Day regis first PDS packet	gister. it increments at 8ns resolution for th					

1.4.1	00 dcm_fb_metrics_	Reg.	0xA003404C									
Local	Local Time Stamp. Synchronized with 32bit eTEC timestamp.for the first PDS packet											
bits	name	s/w	h/w	default		description	٦					
31:0 dcm_fb_metrics_ ro wo X Local Time Stamp. Synchronized with 32bit eTEC timestamp_lts timestamp.for the first PDS packet												

1.4.10	01 region_4_end_tag	Reg.	0xA0034050								
region_4_end_tag											
bits	name	s/w	h/w	default		description					
31:0	region_4_end_ta g	ro	WO	Х	region_4_end_tag	)					

1.4.1	02 region_5_start_ta	Reg.	0xA0035000										
regio	region_5_start_tag												
bits	name	s/w	h/w	default		description	١						
31:0	region_5_start_ tag	ro	WO	Х	region_5_start_ta	g							

1.4.1	03 region_5_dtec_to	Reg.	0xA0035004								
region_5_dtec_tod_lsbs											
bits	name	s/w	h/w	default		description	n				
31:0	region_5_dtec_t od_lsbs	ro	WO	X	region_5_dtec_tod_lsbs						

1.4.1	04 region_5_dtec_to	Reg.	0xA0035008										
regio	region_5_dtec_tod_msbs												
bits	name	s/w	h/w	default		description	า						
31:0 region_5_dtec_t ro wo X region_5_dtec_tod_msbs													

1.4.105 region_5_dtec_lts	Reg.	0xA003500C
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region	region_5_dtec_lts											
bits	name	s/w	h/w	default	description							
31:0	region_5_dtec_l ts	ro	WO	X	region_5_dtec_lts							

1.4.1	06 ddm_fb_metrics_	Reg.	0xA0035010									
# main-droplets												
bits	name	s/w	h/w		default		description					
31:0	ddm_fb_metrics_ maindropletnumb er	ro	wo	X		# main-droplets						

1.4.1	07 ddm_fb_metrics_	Reg.	0xA0035014									
# pre-sub-coalesced droplets												
bits	name	s/w	h/w	default		description	า					
31:0	ddm_fb_metrics_ satelliterate	ced droplets										

1.4.1	08 ddm_fb_metrics	Reg.	0xA0035018									
3-sigi	3-sigma of crossing intervals											
bits	name	s/w	h/w	default		descriptio	n					
31:0 ddm_fb_metrics_ ro wo X 3-sigma of crossing intervals xint3sigma												

1.4.1	09 ddm_fb_metrics_	Reg.	0xA003501C									
3-sigr	3-sigma of crossing intervals											
bits	name	s/w	h/w	default		description	٦					
31:0	ddm_fb_metrics_ xintmean	ng intervals										

1.4.1	10 ddm_fb_metrics_	Reg.	0xA0035020									
3-sigr	3-sigma of crossing intervals											
bits	name	s/w	h/w	defau	lt	descriptio	n					
31:0 ddm_fb_metrics_ ro wo X 3-sigma of crossing intervals mainpeak												

1.4.1	1.4.111 ddm_fb_metrics_pf_exposuredc 0xA0035024											
3-sigi	3-sigma of crossing intervals											
bits	name	s/w	h/w	default		description	า					
31:0	31:0 ddm_fb_metrics_ ro wo X 3-sigma of crossing intervals pf_exposuredc											

1.4.1	12 ddm_fb_metrics_	Reg.	0xA0035028									
Signa	Signal quality calculated using width, value, and noise											
bits	name	s/w	h/w	default		description	า					
31:0 ddm_fb_metrics_ ro wo X Signal quality calculated using width, value, ar signal quality												

1.4.1	1.4.113 ddm_fb_metrics_timestamp_tod_lsb 0xA003502C											
Time	Time of Day register. it increments at 8ns resolution											
bits	bits name s/w h/w default description											
31:0	ddm_fb_metrics_ timestamp_tod_l sb	ro	WO	X		Time of Day register. it increments at 8ns resolution						

1.4.1	1.4.114 ddm_fb_metrics_timestamp_tod_msb 0xA0035030										
Time of Day register. it increments at 8ns resolution											
bits	name	s/w	h/w		default		description	n			
31:0	ddm_fb_metrics_ timestamp_tod_m sb							at 8ns resolution			

1.4.1	15 ddm_fb_metrics_	Reg.	0xA0035034								
Local	Local Time Stamp. Synchronized with 32bit eTEC timestamp.										
bits	name	s/w	h/w	default		description	า				
31:0 ddm_fb_metrics_ ro wo X Local Time Stamp. Synchronized with 32bit eTEC times-timestamp_lts tamp.											

1.4.11	16 region_5_end_tag	Reg.	0xA0035038									
region	region_5_end_tag											
bits	name	s/w	h/w	default		description	า					
31:0 region_5_end_ta ro wo X region_5_end_tag												

1.4.1	17 region_6_start_ta	Reg.	0xA0036000									
regio	region_6_start_tag											
bits	name	s/w	h/w	default		description	ı					
31:0 region_6_start_ ro wo X region_6_start_tag tag												

1.4.1	18 region_6_dtec_to	Reg.	0xA0036004									
regio	region_6_dtec_tod_lsbs											
bits	name	s/w	h/w	default		description	n					
31:0 region_6_dtec_t ro wo X region_6_dtec_tod_lsbs												

1.4.1	19 region_6_dtec_to	Reg.	0xA0036008									
regio	region_6_dtec_tod_msbs											
bits	name	s/w	h/w	default		description	٦					
31:0 region_6_dtec_t ro wo X region_6_dtec_tod_msbs												

1.4.120 region_6_dtec_lts	Reg.	0xA003600C
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regio	n_6_dtec_lts				
bits	name	s/w	h/w	default	description
31:0	region_6_dtec_l ts	ro	wo	X	region_6_dtec_lts

1.4.1	21 damp_waveform	Reg.	0xA0036010							
512 bytes from dTEC 2 DAMP										
bits	name	s/w	h/w		default	description				
31:0	damp_waveformpa ramspkg_damp_si gnals_1	ro	WO	X		512 bytes from d	TEC 2 DAMP			

1.4.1	0xA0036014											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description					
31:0	damp_waveformpa ramspkg_damp_si gnals_2	ro	wo	X		512 bytes from d	ΓEC 2 DAMP					

1.4.1	0xA0036018											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description					
31:0	damp_waveformpa ramspkg_damp_si gnals_3	ro	wo	X		512 bytes from d	TEC 2 DAMP					

1.4.1	24 damp_waveform	Reg.	0xA003601C								
512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w	default		description					
31:0	damp_waveformpa ramspkg_damp_si gnals_4	ro	wo	X	512 bytes from d	ΓEC 2 DAMP					

1.4.1	25 damp_waveform	Reg.	0xA0036020									
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description					
31:0	damp_waveformpa ramspkg_damp_si gnals_5	ro	wo	X		512 bytes from d	TEC 2 DAMP					

1.4.1	26 damp_waveform	Reg.	0xA0036024									
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description					
31:0	damp_waveformpa ramspkg_damp_si gnals_6	ro	WO	X		512 bytes from d	ΓEC 2 DAMP					

1.4.127 damp_waveformparamspkg_damp_signals_7 0xA0036028	
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512 b	512 bytes from dTEC 2 DAMP											
bits	bits name s/w h/w default description											
	damp_waveformpa ramspkg_damp_si gnals_7	ro	WO	X	512 bytes from dTEC 2 DAMP							

1.4.1	28 damp_waveform	paran	ignals_8	Reg.	0xA003602C								
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_8	ro	512 bytes from d	ΓEC 2 DAMP									

1.4.1	29 damp_waveform	gnals_9	Reg.	0xA0036030									
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_9													

1.4.1	30 damp_waveform	paran	ignals_10	Reg.	0xA0036034								
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_10	ro	wo	X		512 bytes from d	TEC 2 DAMP						

1.4.1	1.4.131 damp_waveformparamspkg_damp_signals_11 0xA0036038													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_11														

1.4.1	32 damp_waveform	gnals_12	Reg.	0xA003603C									
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	1					
31:0	damp_waveformpa ramspkg_damp_si gnals_12	ro	wo	X		512 bytes from d	TEC 2 DAMP						

1.4.1	1.4.133 damp_waveformparamspkg_damp_signals_13 0xA0036040												
512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	า					
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_13													

1.4.1	1.4.134 damp_waveformparamspkg_damp_signals_14 0xA0036044													
512 bytes from dTEC 2 DAMP														
bits	bits name s/w h/w default description													
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_14														

1.4.1	1.4.135 damp_waveformparamspkg_damp_signals_15 0xA0036048												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.136 damp_waveformparamspkg_damp_signals_16 0xA0036													
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	111 111												

1.4.1	37 damp_waveforn	Reg.	0xA0036050										
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_17													

1.4.1	38 damp_waveform	paran	gnals_18	Reg.	0xA0036054								
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_18	ro	WO	X	512 bytes from d	ΓEC 2 DAMP							

1.4.1	I.4.139 damp_waveformparamspkg_damp_signals_19 0xA0036058													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													

1.4.1	1.4.140 damp_waveformparamspkg_damp_signals_20 0xA003605C													
512 b	512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	า						
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1													

1.4.1	4.141 damp_waveformparamspkg_damp_signals_21 0xA0036060													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_21														

1.4.1	.4.142 damp_waveformparamspkg_damp_signals_22 0xA0036064													
512 b	512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	n						
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_22														

1.4.1	.4.143 damp_waveformparamspkg_damp_signals_23 0xA0036068													
512 b	512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	n						
31:0														

1.4.1	.4.144 damp_waveformparamspkg_damp_signals_24 0xA003606C													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_24														

1.4.1	.4.145 damp_waveformparamspkg_damp_signals_25 0xA0036070												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	n					
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.1	46 damp_waveform	ignals_26	Reg.	0xA0036074										
512 b	512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	n						
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_26														

1.4.1	1.4.147 damp_waveformparamspkg_damp_signals_27 0xA0036078												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w	default		description	٦						
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

gnals_27			

1.4.1	.4.148 damp_waveformparamspkg_damp_signals_28 0xA003607C												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	n					
31:0	damp_waveformpa ramspkg_damp_si gnals_28	ro	WO	X		512 bytes from dTEC 2 DAMP							

1.4.1	1.4.149 damp_waveformparamspkg_damp_signals_29 0xA0036080													
512 b	512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	ı						
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_29														

1.4.1	50 damp_waveform	paran	nspk	g_d	lamp_s	ignals_30	Reg.	0xA0036084						
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
	damp_waveformpa ramspkg_damp_si gnals_30	ro	wo	X		512 bytes from d	TEC 2 DAMP							

1.4.1	51 damp_wavefori	mparan	nspk	g_d	amp_s	ignals_31	Reg.	0xA0036088						
512 b	512 bytes from dTEC 2 DAMP													
bits name s/w h/w default description														
31:0														

1.4.1	4.152 damp_waveformparamspkg_damp_signals_32 0xA003608C														
512 b	512 bytes from dTEC 2 DAMP														
bits	bits name s/w h/w default description														
31:0	damp_waveformpa ramspkg_damp_si gnals_32	ro	WO	X	512 bytes from dTEC 2 DAMP										

1.4.1	53 damp_waveform	paran	Reg.	0xA0036090									
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_33													

1.4.1	1.4.154 damp_waveformparamspkg_damp_signals_34 0xA0036094													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0	31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP													

ramspkg_damp_si		
gnals_34		

1.4.1	55 damp_waveform	paran	nspko	g_d	lamp_si	gnals_35	Reg.	0xA0036098					
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_35													

1.4.1	4.156 damp_waveformparamspkg_damp_signals_36 0xA003609C														
512 b	512 bytes from dTEC 2 DAMP														
bits	bits name s/w h/w default description														
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_36															

1.4.1	57 damp_waveform	paran	nspkg	g_d	lamp_si	gnals_37	Reg.	0xA00360A0					
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.1	58 damp_waveform	paran	nspk	g_c	damp_s	ignals_38	Reg.	0xA00360A4						
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0	damp_waveformpa ramspkg_damp_si gnals_38	ro	wo	X		512 bytes from dTEC 2 DAMP								

1.4.1	59 damp_waveform	paran	nspk	g_c	damp_si	gnals_39	Reg.	0xA00360A8					
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
	damp_waveformpa ramspkg_damp_si gnals_39	ro	WO	X		512 bytes from d	TEC 2 DAMP						

1.4.1	.4.160 damp_waveformparamspkg_damp_signals_40 0xA00360AC														
512 b	512 bytes from dTEC 2 DAMP														
bits	bits name s/w h/w default description														
31:0	damp_waveformpa ramspkg_damp_si gnals_40	ro	WO	X	512 bytes from dTEC 2 DAMP										

1.4.161 d	lamp_wavefo	ormparamspkg_	nals_41	Reg.	0xA00360B0						
512 bytes	512 bytes from dTEC 2 DAMP										
bits name s/w h/w default description											

31:0	damp_waveformpa	ro	WO	X	512 bytes from dTEC 2 DAMP
	ramspkg_damp_si				
	gnals_41				

1.4.1	1.4.162 damp_waveformparamspkg_damp_signals_42 0xA00360B4												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_42	ro	WO	X		512 bytes from d	TEC 2 DAMP						

1.4.1	1.4.163 damp_waveformparamspkg_damp_signals_43 0xA00360B8												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.164 damp_waveformparamspkg_damp_signals_44 0xA00360BC													
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0													

1.4.165 damp_waveformparamspkg_damp_signals_45 0xA00360C0												
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	٦				
31:0												

1.4.1	66 damp_waveform	Reg.	0xA00360C4										
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_46	ro	wo	X		512 bytes from d	TEC 2 DAMP						

1.4.1	67 damp_waveform <sub>l</sub>	0xA00360C8											
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0													

1.4.168 damp_waveformparamspkg_damp_signals_48	Reg.	0xA00360CC
512 bytes from dTEC 2 DAMP		

bits	name	s/w	h/w	default	description
31:0	damp_waveformpa ramspkg_damp_si gnals_48	ro	WO	X	512 bytes from dTEC 2 DAMP

1.4.169 damp_waveformparamspkg_damp_signals_49 0xA00360D0														
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0														

1.4.170 damp_waveformparamspkg_damp_signals_50 0xA00360D4												
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0												

1.4.1	1.4.171 damp_waveformparamspkg_damp_signals_51 0xA00360D8												
512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	n					

1.4.1	72 damp_waveform	Reg.	0xA00360DC										
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_52	ro	WO	X		512 bytes from d	ΓEC 2 DAMP						

1.4.1	73 damp_waveform	nparan	gnals_53	Reg.	0xA00360E0								
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_53													

1.4.1	1.4.174 damp_waveformparamspkg_damp_signals_54 0xA00360E4												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0													

1.4.175 damp_waveformparamspkg_damp_signals_55	Reg.	0xA00360E8	
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512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w	default	description						
31:0	damp_waveformpa ramspkg_damp_si gnals_55	ro	wo	X	512 bytes from dTEC 2 DAMP						

1.4.1	76 damp_waveform	paran	ignals_56	Reg.	0xA00360EC							
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	n				
31:0	damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_56											

1.4.1	1.4.177 damp_waveformparamspkg_damp_signals_57 0xA00360F0													
512 bytes from dTEC 2 DAMP														
bits	name	s/w	h/w		default		description	n						

1.4.1	1.4.178 damp_waveformparamspkg_damp_signals_58 0xA00360F4												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_58	ro	wo	X		512 bytes from d	TEC 2 DAMP						

1.4.1	1.4.179 damp_waveformparamspkg_damp_signals_59 0xA00360F8												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.1	1.4.180 damp_waveformparamspkg_damp_signals_60 0xA00360FC												
512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	า					
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_60													

1.4.18	1.4.181 damp_waveformparamspkg_damp_signals_61 0xA0036100											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	า				
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											

1.4.1	1.4.182 damp_waveformparamspkg_damp_signals_62 0xA0036104											
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0												

1.4.1	1.4.183 damp_waveformparamspkg_damp_signals_63 0xA0036108											
512 b	512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w		default		description	n				
31:0												

1.4.1	1.4.184 damp_waveformparamspkg_damp_signals_64 0xA003610C												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_64	ro	WO	X		512 bytes from d	TEC 2 DAMP						

1.4.1	1.4.185 damp_waveformparamspkg_damp_signals_65 0xA0036110												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_65	ro	WO	X		512 bytes from dTEC 2 DAMP							

1.4.1	1.4.186 damp_waveformparamspkg_damp_signals_66 0xA0036114												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_66	ro	WO	X	512 bytes from d	TEC 2 DAMP							

1.4.18	1.4.187 damp_waveformparamspkg_damp_signals_67 0xA0036118											
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											

1.4.1	1.4.188 damp_waveformparamspkg_damp_signals_68 0xA003611C												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	٦					
31:0	damp_waveformpa ramspkg_damp_si gnals_68	ro	wo	X		512 bytes from d	TEC 2 DAMP						

1.4.1	1.4.189 damp_waveformparamspkg_damp_signals_69 0xA0036120												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_69													

1.4.1	1.4.190 damp_waveformparamspkg_damp_signals_70 0xA0036124												
512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	n					
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_70													

1.4.19	1.4.191 damp_waveformparamspkg_damp_signals_71 0xA0036128											
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											

1.4.19	1.4.192 damp_waveformparamspkg_damp_signals_72 0xA003612C												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.1	1.4.193 damp_waveformparamspkg_damp_signals_73 0xA0036130												
512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		description	n					
31:0	damp_waveformpa ramspkg_damp_si gnals_73	ro	wo	X		512 bytes from d	ΓEC 2 DAMP						

1.4.1	94 damp_waveform	paran	ignals_74	Reg.	0xA0036134								
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	n					
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_74													

1.4.1	1.4.195 damp_waveformparamspkg_damp_signals_75 0xA0036138											
512 b	512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w	default		description	n					
31:0	31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si											

gnals 75			

1.4.1	1.4.196 damp_waveformparamspkg_damp_signals_76 0xA003613C												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w	de	efault		description	n					
31:0													

1.4.19	97 damp_waveform	paran	nspk	g_c	damp_si	gnals_77	Reg.	0xA0036140				
512 b	512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w		default		description	n				
31:0												

1.4.19	I.4.198 damp_waveformparamspkg_damp_signals_78 0xA0036144												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0													

1.4.1	1.4.199 damp_waveformparamspkg_damp_signals_79 0xA0036148												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		descriptio	n					
31:0	damp_waveformpa ramspkg_damp_si gnals_79	ro	WO	X		512 bytes from d	TEC 2 DAMP						

1.4.2	.4.200 damp_waveformparamspkg_damp_signals_80 0xA003614C												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												

1.4.20	1.4.201 damp_waveformparamspkg_damp_signals_81 0xA0036150												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	า					

1.4.2	1.4.202 damp_waveformparamspkg_damp_signals_82 0xA0036154												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP													

ramspkg_damp_si			
gnals_82			

1.4.2	1.4.203 damp_waveformparamspkg_damp_signals_83 0xA0036158											
512 b	512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w		default		description	n				
31:0	7.7											

1.4.2	.4.204 damp_waveformparamspkg_damp_signals_84 0xA003615C													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0														

1.4.2	.4.205 damp_waveformparamspkg_damp_signals_85 0xA0036160												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0													

1.4.2	06 damp_waveform	paran	nspk	g_c	damp_s	ignals_86	Reg.	0xA0036164					
512 b	512 bytes from dTEC 2 DAMP												
bits	ts name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_86	ro	wo	X		512 bytes from dTEC 2 DAMP							

1.4.2	07 damp_waveform	paran	nspk	g_c	damp_si	ignals_87	Reg.	0xA0036168					
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
	7 T T T T T T T T T T T T T T T T T T T												

1.4.2	1.4.208 damp_waveformparamspkg_damp_signals_88 0xA003616C													
512 b	512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w	default		description	n							
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_88														

1.4.209 d	1.4.209 damp_waveformparamspkg_damp_signals_89 0xA0036170											
512 bytes	512 bytes from dTEC 2 DAMP											
bits name s/w h/w default description												

31:0	damp_waveformpa	ro	WO	X	512 bytes from dTEC 2 DAMP
	ramspkg_damp_si				
	gnals_89				

1.4.2	10 damp_waveform	paran	nspk	<b>g_</b> c	damp_s	ignals_90	Reg.	0xA0036174					
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0													

1.4.2	.4.211 damp_waveformparamspkg_damp_signals_91 0xA0036178													
512 b	512 bytes from dTEC 2 DAMP													
bits	name	s/w	h/w		default		descriptio	n						
31:0														

1.4.2	12 damp_waveform	paran	nspk	g_c	damp_si	gnals_92	Reg.	0xA003617C				
512 b	512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w		default		description	n				

1.4.2	.4.213 damp_waveformparamspkg_damp_signals_93 0xA0036180												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	١					
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.2	.4.214 damp_waveformparamspkg_damp_signals_94 0xA0036184												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		descriptio	n					
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.2	15 damp_waveform <sub> </sub>	Reg.	0xA0036188							
512 bytes from dTEC 2 DAMP										
bits	name	s/w	h/w		default		description	n		
31:0	damp_waveformpa ramspkg_damp_si gnals_95	ro	WO	Х		512 bytes from d	TEC 2 DAMP			

1.4.216 damp_waveformparamspkg_damp_signals_96	Reg.	0xA003618C
512 bytes from dTEC 2 DAMP		

bits	name	s/w	h/w	default	description
31:0	damp_waveformpa ramspkg_damp_si gnals_96	ro	WO	X	512 bytes from dTEC 2 DAMP

1.4.2	1.4.217 damp_waveformparamspkg_damp_signals_97 0xA0036190											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w	de	efault		description	n				
31:0	damp_waveformpa ramspkg_damp_si gnals_97	ro	wo	X		512 bytes from d	TEC 2 DAMP					

1.4.2	1.4.218 damp_waveformparamspkg_damp_signals_98 0xA0036194											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	n				
31:0	damp_waveformpa ramspkg_damp_si gnals_98	ro	WO	X		512 bytes from d	ΓEC 2 DAMP					

1.4.2	1.4.219 damp_waveformparamspkg_damp_signals_99 0xA0036198											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		descriptio	n				
	damp_waveformpa ramspkg_damp_si gnals_99	ro	WO	X		512 bytes from d	TEC 2 DAMP					

1.4.2	1.4.220 damp_waveformparamspkg_damp_signals_100 0xA003619C											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	n				
31:0	damp_waveformpa ramspkg_damp_si gnals_100	ro	WO	X		512 bytes from d	TEC 2 DAMP					

1.4.2	1.4.221 damp_waveformparamspkg_damp_signals_101											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w	default		description						
31:0	damp_waveformpa ramspkg_damp_si gnals_101	ro	WO	X	512 bytes from d	TEC 2 DAMP						

1.4.2	22 damp_waveform <sub>l</sub>	gnals_102	Reg.	0xA00361A4						
512 bytes from dTEC 2 DAMP										
bits	name	s/w	h/w		default		description	า		
31:0	damp_waveformpa ramspkg_damp_si gnals_102	ro	wo	X		512 bytes from d	TEC 2 DAMP			

1.4.223 damp_waveformparamspkg_damp_si	nals_103 Reg.	0xA00361A8
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512 b	512 bytes from dTEC 2 DAMP										
bits	name	s/w	h/w	default	description						
31:0	damp_waveformpa ramspkg_damp_si gnals_103	ro	WO	X	512 bytes from dTEC 2 DAMP						

1.4.2	24 damp_waveform	paran	ignals_104	Reg.	0xA00361AC						
512 bytes from dTEC 2 DAMP											
bits	name	s/w	h/w		default		description				
31:0	damp_waveformpa ramspkg_damp_si gnals_104	ro	wo	X		512 bytes from d	ΓEC 2 DAMP				

1.4.2	25 damp_waveform	paran	nspk	g_d	amp_si	gnals_105	Reg.	0xA00361B0				
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0	damp_waveformpa ramspkg_damp_si gnals_105	ro	wo	X		512 bytes from d	TEC 2 DAMP					

1.4.2	26 damp_waveform	paran	nspk	g_d	amp_s	ignals_106	Reg.	0xA00361B4				
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0	damp_waveformpa ramspkg_damp_si gnals_106	ro	WO	X		512 bytes from d	TEC 2 DAMP					

1.4.2	27 damp_waveform	paran	nspk	g_damp_si	gnals_107	Reg.	0xA00361B8					
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0	damp_waveformpa ramspkg_damp_si gnals_107	ro	WO	X	512 bytes from d	TEC 2 DAMP						

1.4.2	28 damp_waveform	paran	nspk	ignals_108	Reg.	0xA00361BC					
512 bytes from dTEC 2 DAMP											
bits	bits name s/w h/w default description										
31:0	damp_waveformpa ramspkg_damp_si gnals_108	ro	WO	X		512 bytes from d	TEC 2 DAMP				

1.4.2	1.4.229 damp_waveformparamspkg_damp_signals_109 0xA00361C0											
512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	า				
31:0	damp_waveformpa ramspkg_damp_si gnals_109	ro	wo	X		512 bytes from d	TEC 2 DAMP					

1.4.2	1.4.230 damp_waveformparamspkg_damp_signals_110												
512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_110	ro	wo	X		512 bytes from d	TEC 2 DAM	Р					

1.4.2	I.4.231 damp_waveformparamspkg_damp_signals_111 0xA00361C8												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	n					
31:0	damp_waveformpa ramspkg_damp_si gnals_111	ro	wo	X		512 bytes from d	TEC 2 DAMP						

1.4.2	32 damp_waveform	paran	nspk	g_c	lamp_s	ignals_112	Reg.	0xA00361CC				
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0	damp_waveformpa ramspkg_damp_si gnals_112	ro	WO	X		512 bytes from d	TEC 2 DAMP					

1.4.2	0xA00361D0											
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0	damp_waveformpa ramspkg_damp_si gnals_113	ro	WO	X		512 bytes from d	EC 2 DAMP					

1.4.2	34 damp_waveform	paran	nspk	g_damp_si	gnals_114	Reg.	0xA00361D4				
512 bytes from dTEC 2 DAMP											
bits	bits name s/w h/w default description										
31:0	damp_waveformpa ramspkg_damp_si gnals_114	ro	WO	X	512 bytes from d	TEC 2 DAM	<b>JP</b>				

1.4.23	1.4.235 damp_waveformparamspkg_damp_signals_115 0xA00361D8												
512 b	512 bytes from dTEC 2 DAMP												
bits	name	s/w	h/w		default		description	า					
	damp_waveformpa ramspkg_damp_si gnals_115	ro	wo	X		512 bytes from d	TEC 2 DAMP						

1.4.2	1.4.236 damp_waveformparamspkg_damp_signals_116											
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_116												

1.4.2	.4.237 damp_waveformparamspkg_damp_signals_117 0xA00361E0													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_117														

1.4.2	1.4.238 damp_waveformparamspkg_damp_signals_118 0xA00361E4													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_118														

1.4.2	I.4.239 damp_waveformparamspkg_damp_signals_119 0xA00361E8												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.2	.4.240 damp_waveformparamspkg_damp_signals_120 0xA00361EC												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0													

1.4.2	1.4.241 damp_waveformparamspkg_damp_signals_121 0xA00361F0												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_121													

1.4.2	.4.242 damp_waveformparamspkg_damp_signals_122 0xA00361F4													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_122														

1.4.2	43 damp_waveform	paran	nspk	g_damp_si	gnals_123	Reg.	0xA00361F8						
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si													

gnals 123		

1.4.2	44 damp_waveform	paran	nspk	g_c	damp_s	ignals_124	Reg.	0xA00361FC					
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0	damp_waveformpa ramspkg_damp_si gnals_124	ro	WO	X	512 bytes from dTEC 2 DAMP								

1.4.2	1.4.245 damp_waveformparamspkg_damp_signals_125 0xA0036200												
512 b	512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description												
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_125													

1.4.2	.4.246 damp_waveformparamspkg_damp_signals_126 0xA0036204													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
	damp_waveformpa ramspkg_damp_si gnals_126	ro	wo	X		512 bytes from d	TEC 2 DAMP							

1.4.2	I.4.247 damp_waveformparamspkg_damp_signals_127 0xA0036208													
512 b	512 bytes from dTEC 2 DAMP													
bits	bits name s/w h/w default description													
31:0	damp_waveformpa ramspkg_damp_si gnals_127	ro	WO	X		512 bytes from d	TEC 2 DAMP							

1.4.2	48 damp_waveform	nparan	nspk	g_damp_si	gnals_128	Reg.	0xA003620C					
512 bytes from dTEC 2 DAMP												
bits	bits name s/w h/w default description											
31:0 damp_waveformpa ro wo X 512 bytes from dTEC 2 DAMP ramspkg_damp_si gnals_128												

1.4.2	49 region_6_end_ta	Reg.	0xA0036210									
regio	region_6_end_tag											
bits	name	s/w	h/w	default		description	١					
31:0	region_6_end_ta g	region_6_end_tag	)									

1.4.2	50 region_7_start_ta	Reg.	0xA0037000				
regio	n_7_start_tag						
bits	name	s/w	h/w	default		description	า
31:0	region_7_start_ tag	ro	region_7_start_ta	g			

1.4.2	51 region_7_dtec_to	Reg.	0xA0037004									
regio	region_7_dtec_tod_lsbs											
bits	name	s/w	h/w	default		description	n					
31:0	31:0 region_7_dtec_t ro wo X region_7_dtec_tod_lsbs od_lsbs											

1.4.2	52 region_7_dtec_to	Reg.	0xA0037008									
regio	region_7_dtec_tod_msbs											
bits	name	s/w	h/w	default		description	n					
31:0	region_7_dtec_t od_msbs	d_msbs										

1.4.2	53 region_7_dtec_lts	Reg.	0xA003700C				
regio	n_7_dtec_lts						
bits	name	s/w	h/w	default		description	n
31:0	region_7_dtec_l ts	i					

1.4.2	54 solutiontable_ou		Reg.	0xA0037010								
	0: 2 sine square waveform 1: HWO											
bits	name	s/w	h/w	default		description	n					
31:0	31:0 solutiontable_o ro wo X 0: 2 sine square waveform 1: HWO											

1.4.2	55 solutiontable_oเ	ıt_hyp	perpa	ran	neters_	1	Reg.	0xA0037014			
Vecto 1. f0 2. N0 3. N1 4. As											
bits	name	s/w	h/w		default		description	n			
31:0											

1.4.2	56 solutiontable_ou	ıt_hyp	perpa	ram	eters_2		Reg.	0xA0037018			
Vector 1. f0 2. N0 3. N1 4. As											
bits	name	s/w	h/w		default		description	n			
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1										

1.4.2	57 solutiontable_ou	ıt_hyp	erpa	rameters_	3	Reg.	0xA003701C			
Vecto 1. f0 2. N0 3. N1 4. As										
bits	name	s/w	h/w	default		description	n			
31:0 solutiontable_o ro wo X Vector of HyperParameters: ut_hyperparamet ers_3										

1.4.2	.4.258 solutiontable_out_hyperparameters_4 0xA0037020												
Vecto 1. f0 2. N0 3. N1 4. As													
bits	name	s/w	h/w	default		descriptio	n						
31:0													

1.4.2	59 solutiontable_ou	Reg.	0xA0037024									
1. A0	Sine Amplitudes: 1. A0 2. A1											
bits	name	s/w	h/w	default		descriptio	n					
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											

1.4.2	60 solutiontable_ou	t_sin	eamp	s_2		Reg.	0xA0037028
Sine . 1. A0 2. A1	Amplitudes:						
bits	name	s/w	h/w	default		description	n
31:0	solutiontable_o ut_sineamps_2	ro	wo	Х	Sine Amplitudes: 1. A0 2. A1		

1.4.2	61 solutiontable_	out_phi	0_1		Reg.	0xA003702C
Solut	ion table phi0 column					
bits	name	s/w	h/w	default	des	cription
31:0	solutiontable_o ut_phi0_1	ro	wo	X	Solution table phi0 column	

1.4.262 solutiontable_out_phi0_2	Reg.	0xA0037030

Soluti	ion table phi0 column				
bits	name	s/w	h/w	default	description
31:0	solutiontable_o	ro	wo	X	Solution table phi0 column
	ut_phi0_2				

1.4.2	63 solutiontable_ou	t_phi	0_3				Reg.	0xA0037034
Solut	on table phi0 column							
bits	name	s/w	h/w		default		description	٦
31:0	solutiontable_o ut_phi0_3	ro	wo	Χ		Solution table phi	0 column	

1.4.2	64 solutiontable_ou	t_phi	0_4				Reg.	0xA0037038
Solut	ion table phi0 column							
bits	name	s/w	h/w		default		description	n
31:0	solutiontable_o ut_phi0_4	ro	wo	X		Solution table phi	0 column	

1.4.2	65 solutiontable_ou	t_phi	0_5			Reg.	0xA003703C
Solut	ion table phi0 column						
bits	name	s/w	h/w	default		description	า
31:0	solutiontable_o ut_phi0_5	ro	wo	X	Solution table phi	0 column	

1.4.2	66 solutiontable_ou	t_phi	0_6			Reg.	0xA0037040
Solut	ion table phi0 column						
bits	name	s/w	h/w	default		description	n
31:0	solutiontable_o ut_phi0_6	ro	wo	X	Solution table phi	0 column	

1.4.2	67 solutiontable_ou	t_phi	0_7			Reg.	0xA0037044
Solut	ion table phi0 column						
bits	name	s/w	h/w	default		description	١
31:0	solutiontable_o ut_phi0_7	ro	WO	Х	Solution table phi	0 column	

1.4.2	68 solutiontable_ou	t_phi	8_0			Reg.	0xA0037048
Solut	ion table phi0 column						
bits	name	s/w	h/w	default		description	١
31:0	solutiontable_o ut_phi0_8	ro	WO	X	Solution table phi	0 column	

1.4.2	69 solutiontable_	out_phi	0_9			Reg.	0xA003704C
Solut	ion table phi0 column						
bits	name	s/w	h/w	default		description	n
31:0	solutiontable_o ut_phi0_9	ro	wo	X	Solution table phi	0 column	

	tion table phi0 column						
bits	name	s/w	h/w		default	desc	ription
31:0	solutiontable_o ut_phi0_10	ro	wo	X		Solution table phi0 column	
1.4.2	?71 solutiontable_o	ut_phi	0_11			Reg.	0xA0037054
Solu	tion table phi0 column						
bits	name	s/w	h/w		default		ription
31:0	solutiontable_o ut_phi0_11	ro	WO	X		Solution table phi0 column	
1.4.2	?72 solutiontable_o	ut_phi	0_12			Reg.	0xA0037058
	tion table phi0 column						
bits	name	s/w	h/w	V	default		ription
31:0	solutiontable_o ut_phi0_12	ro	WO	X		Solution table phi0 column	
	tion table phi0 column	ut_phi	0_13			Reg.	0xA003705C
bits	name	s/w	h/w		default	desc	ription
31:0	solutiontable_o ut_phi0_13	ro	wo	Χ		Solution table phi0 column	
1.4.2	274 solutiontable_o	ut_phi	0_14			Reg.	0xA0037060
Solu	tion table phi0 column						
	name	s/w	h/w		default	desc	ription
bits	solutiontable_o	ro	wo	X		Solution table phi0 column	
bits 31:0	ut_phi0_14						
	ut_phi0_14						
31:0	ut_phi0_14 275 solutiontable_ou	ut_phi	0_15			Reg.	0xA0037064
31:0 <b>1.4.2</b> Solu		ut_phi					
31:0  1.4.2  Solutibits	275 solutiontable_oution table phi0 column name	s/w	h/w	V	default	desc	0xA0037064 ription
31:0 <b>1.4.2</b> Solu	275 solutiontable_oution table phi0 column	-		X	default		
31:0  1.4.2  Solutibits	275 solutiontable_oution table phi0 column name solutiontable_o	s/w	h/w	X	default	desc	
31:0 1.4.2 Solu bits 31:0	275 solutiontable_oution table phi0 column name solutiontable_o	s/w ro	h/w wo	X	default	desc	
31:0 1.4.2 Solur bits 31:0	tion table phi0 column name solutiontable_o ut_phi0_15	s/w ro	h/w wo	X	default	desc Solution table phi0 column	ription
31:0 1.4.2 Solur bits 31:0	tion table phi0 column name solutiontable_o ut_phi0_15	s/w ro	h/w wo	X	default	desc Solution table phi0 column	ription

bits

Solution table phi0 column

name

s/w h/w

description

default

31:0	solutiontable_o	ro	wo	X	Solution table phi0 column
	ut_phi0_17				

1.4.2	78 solutiontable_ou	t_phi		Reg.	0xA0037070							
Solution table phi0 column												
bits	name	s/w	h/w	default		description	n					
31:0	solutiontable_o ut_phi0_18	ro	wo	X	Solution table phi	le phi0 column						

1.4.2	79 solutiontable_ou	Reg.	0xA0037074									
Solution table phi0 column												
bits	name	s/w	h/w	default		description	า					
31:0	solutiontable_o ut_phi0_19	ro	wo	X	Solution table phi0 column							

1.4.2	80 solutiontable_ou	t_phi	i	Reg.	0xA0037078						
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	(	default		description	on			
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1										

1.4.2	1.4.281 solutiontable_out_phi1_2 0xA003707C												
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.													
					description								
bits	name	s/w	h/w	default		description	n						

1.4.2	82 solutiontable_ou	t_phi		Reg.	0xA0037080							
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
					•							
bits	name	s/w	h/w	default		descriptio	n					

1.4.2	83 solutiontable_o	ut_phi	1_4		Reg	3.	0xA0037084						
	Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	default		description	า						
31:0	solutiontable_o ut_phi1_4	ro	WO	X	Solution table phi1 contact Each row represents steps of 0.05.								

1.4.284 solutiontable_out_phi1_5	Reg.	0xA0037088
Solution table phi1 column.		

Each	Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default	description						
31:0	solutiontable_o ut_phi1_5	ro	WO	X	Solution table phi1 column.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.						

1.4.2	1.4.285 solutiontable_out_phi1_6 0xA003708C												
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.													
bits	name	s/w	h/w	default	description								
31:0	solutiontable_o	ro	wo	X	Solution table phi1 column.								
	ut phi1 6				Each row represents a different DC, from 0.05 to 0.95, in								
	at_piiii_o				Edon fow represents a amerent Be, from 6:00 to 6:00, in								

1.4.2	86 solutiontable_ou		Reg.	0xA0037090								
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w		default		descripti	on				
31:0	solutiontable_o	ro	wo	Χ		Solution table phi	Solution table phi1 column.					
	ut_phi1_7					Each row represe steps of 0.05.	row represents a different DC, from 0.05 to 0.95, in					

1.4.2	87 solutiontable_	out_phi	Reg.		0xA0037094						
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w		default		desc	cription	n		
31:0											

1.4.288 solutiontable_out_phi1_9 0xA0037098											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	default	des	cription					
31:0	solutiontable_o ut_phi1_9	ro	wo	X	Solution table phi1 column. Each row represents a differ steps of 0.05.	ent DC, from 0.05 to 0.95, in					

1.4.2	1.4.289 solutiontable_out_phi1_10 0xA003709C											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	default	C	description						
31:0 solutiontable_o												

1.4.290 solutiontable_out_phi1_11 0xA00370A0											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
	bits name s/w h/w default description										
	name	s/w	h/w	default	desc	ription					

ut_phi1_11	Each row represents a different DC, from 0.05 to 0.95, in
	steps of 0.05.

1.4.2	1.4.291 solutiontable_out_phi1_12 0xA00370A4											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	default		description						
31:0	solutiontable_o	ro	wo	X	Solution table phi1 colum	n.						
	solutiontable_o ro wo X Solution table phi1 column.  ut_phi1_12 ro wo X Solution table phi1 column.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											

1.4.2	1.4.292 solutiontable_out_phi1_13 0xA00370A8											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	default	descrip	otion						
21.0	bits name s/w h/w default description  31:0 solutiontable_o ro wo X Solution table phi1 column.  ut_phi1_13											

1.4.2	1.4.293 solutiontable_out_phi1_14 0xA00370AC											
Solution table phi1 column.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	default	description							
31:0	solutiontable_o	ro	wo	X	Solution table phi1 column.							

1.4.2	1.4.294 solutiontable_out_phi1_15 0xA00370B0											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits name s/w h/w default description												
bits	bits name s/w h/w default description 31:0 solutiontable_o ro wo X Solution table phi1 column.  ut_phi1_15 Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											

1.4.2	1.4.295 solutiontable_out_phi1_16 0xA00370B4												
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.													
bits	name	s/w	h/w	default	description								
31:0	solutiontable_o	ro	wo										
	31:0 solutiontable_o ro wo X Solution table phi1 column. ut_phi1_16 Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												

1.4.2	1.4.296 solutiontable_out_phi1_17 0xA00370B8											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	defa	t	descrip	otion					
31:0												

#### 0xA00370BC 1.4.297 solutiontable\_out\_phi1\_18 Reg. Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. default bits name s/w h/w description 31:0 solutiontable\_o Solution table phi1 column. ro wo X ut\_phi1\_18 Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

1.4.2	1.4.298 solutiontable_out_phi1_19 0xA00370C0											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w		default		desc	cription	1			
31:0												

1.4.29	1.4.299 solutiontable_out_presubcoal_flag_1 0xA00370C4										
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	default		description	n				
31:0	solutiontable_o ut_presubcoal_f lag_1	ro	WO	X	dicates a bad brea	akout, so bad DC	r bFlag) column. If 0, in- C, from 0.05 to 0.95, in				

1.4.3	1.4.300 solutiontable_out_presubcoal_flag_2 0xA00370C8										
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	default	description						
31:0											

1.4.3	01 solutiontable_ou	Reg.	0xA00370CC							
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default		descriptio	n			
31:0	The state of the s									

1.4.3	.4.302 solutiontable_out_presubcoal_flag_4 0xA00370D0											
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	default		description	n					
31:0	solutiontable_o ut_presubcoal_f lag_4	ro	wo	X	dicates a bad brea	akout, so bad DC	r bFlag) column. If 0, in- c, from 0.05 to 0.95, in					

#### 1.4.303 solutiontable\_out\_presubcoal\_flag\_5 0xA00370D4 Reg. Solution table PreSubCoal\_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. bits name s/w h/w default description Solution table PreSubCoal\_Flag (or bFlag) column. If 0, in-31:0 solutiontable\_o wo X ro ut\_presubcoal\_f dicates a bad breakout, so bad DC. lag\_5 Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

1.4.3	04 solutiontable_ou	Reg.	0xA00370D8							
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default		description	n			
31:0	solutiontable_o ut_presubcoal_f lag_6	ro	WO	X	dicates a bad brea	akout, so bad DC	r bFlag) column. If 0, in- c, from 0.05 to 0.95, in			

1.4.3	05 solutiontable_ou	Reg.	0xA00370DC							
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default		descriptio	n			
31:0	solutiontable_o ut_presubcoal_f lag_7	ro	WO	X	dicates a bad brea	akout, so bad DC	or bFlag) column. If 0, in- c. C, from 0.05 to 0.95, in			

1.4.3	06 solutiontable_ou	Reg.	0xA00370E0								
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	default		description	n				
31:0	solutiontable_o ut_presubcoal_f lag_8	ro	WO	X	dicates a bad brea	akout, so bad DC	or bFlag) column. If 0, in- c. C, from 0.05 to 0.95, in				

1.4.3	1.4.307 solutiontable_out_presubcoal_flag_9 0xA00370E4										
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	default		description	n				
31:0	solutiontable_o ut_presubcoal_f lag_9	ro	wo	X	dicates a bad brea	akout, so bad DC	r bFlag) column. If 0, in- C, from 0.05 to 0.95, in				

1.4.3	1.4.308 solutiontable_out_presubcoal_flag_10 0xA00370E8										
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
Each	row represents a differ	ent DC, fr	om 0.0	05 to 0.95, in s	steps of 0.05.						
Each bits	row represents a differ	ent DC, fr	om 0.0 h/w	05 to 0.95, in single	steps of 0.05.	desc	cription				

lag_10	Each row represents a different DC, from 0.05 to 0.95, in
	steps of 0.05.

1.4.3	09 solutiontable_ou	Reg.	0xA00370EC								
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	d	lefault		description	n			
31:0											

1.4.3	1.4.310 solutiontable_out_presubcoal_flag_12 0xA00370F0										
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w		default		description	n			
31:0											

1.4.3	1.4.311 solutiontable_out_presubcoal_flag_13 0xA00370F4									
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default		description	n			
31:0										

1.4.3	12 solutiontable_ou	Reg.	0xA00370F8							
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w		default		description	n		
31:0	solutiontable_o ut_presubcoal_f lag_14	ro	WO	X		dicates a bad brea	akout, so bad DC	r bFlag) column. If 0, in- C, from 0.05 to 0.95, in		

1.4.3	13 solutiontable_o	ut_pre	5 0xA00370FC							
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default	description					
31:0	solutiontable_o	ro	wo	X	Solution table PreSubCoal_Flag (or bFlag) column. If 0, in-					

1.4.314 solutiontable_out_presubcoal_flag_16 0xA0037100										
			lumn. If 0, indicates a to 0.95, in steps of 0	bad breakout, so bad 0.05.	d DC.					

31:0	solutiontable_o	ro	WO	Χ	Solution table PreSubCoal_Flag (or bFlag) column. If 0, in-
	ut_presubcoal_f				dicates a bad breakout, so bad DC.
	lag_16				Each row represents a different DC, from 0.05 to 0.95, in
					steps of 0.05.

1.4.3	15 solutiontable_ou	Reg.	0xA0037104							
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	de	efault		description	n		
31:0	solutiontable_o ut_presubcoal_f lag_17	ro	WO	X		dicates a bad brea	akout, so bad DC	r bFlag) column. If 0, in- C, from 0.05 to 0.95, in		

1.4.3	16 solutiontable_ou	Reg.	0xA0037108							
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w		default		description	n		
31:0	solutiontable_o ut_presubcoal_f lag_18	ro	WO	X		dicates a bad brea	akout, so bad DC	r bFlag) column. If 0, in- c, from 0.05 to 0.95, in		

1.4.3	17 solutiontable_ou	t_pre	9	Reg.	0xA003710C					
Solution table PreSubCoal_Flag (or bFlag) column. If 0, indicates a bad breakout, so bad DC. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default		description	า			
31:0	solutiontable_o ut_presubcoal_f lag_19	ro	WO	X	dicates a bad bre	akout, so bad DC	r bFlag) column. If 0, in- c, from 0.05 to 0.95, in			

1.4.3	18 solutiontable_ou	t_jitte	er_1			Reg.	0xA0037110		
Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.									
bits	name	s/w	h/w	default		descriptio	n		
31:0	solutiontable_o ut_jitter_1	ro	WO	X	ral jitter. This metric is use coalescence. Min	ring subCL upda d to rank solution imum sigmaC is t	te which quantifies natu- is with complete pre-sub- the best. C, from 0.05 to 0.95, in		

1.4.3	19 solutiontable_ou	t_jitte		Reg.	0xA0037114				
Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.									
				•			ine best.		
				•		descriptio			

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

## 1.4.320 solutiontable\_out\_jitter\_3

Reg.

0xA0037118

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_3	ro	WO	X	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.  Each row represents a different DC, from 0.05 to 0.95, in
					steps of 0.05.

### 1.4.321 solutiontable\_out\_jitter\_4

Reg.

0xA003711C

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_4	ro	wo	X	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.322 solutiontable\_out\_jitter\_5

Reg.

0xA0037120

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w		default	description
31:0	solutiontable_o ut_jitter_5	ro	WO	X		Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-sub-
						coalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.323 solutiontable\_out\_jitter\_6



0xA0037124

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

bits	name	s/w	h/w		default	description
31:0	solutiontable_o ut_jitter_6	ro	WO	X		Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.324 solutiontable\_out\_jitter\_7

Reg.

0xA0037128

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_7	ro	WO	X	Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

## 1.4.325 solutiontable\_out\_jitter\_8

Reg.

0xA003712C

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_8	ro	WO	X	Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

### 1.4.326 solutiontable\_out\_jitter\_9

Reg.

0xA0037130

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.327 solutiontable\_out\_jitter\_10



0xA0037134

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

bits name s/w h/w default	description
ut_jitter_10	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.328 solutiontable\_out\_jitter\_11

Reg.

0xA0037138

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_11	ro	WO	X	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

# 1.4.329 solutiontable\_out\_jitter\_12

Reg.

0xA003713C

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w		default	description
31:0	solutiontable_o ut_jitter_12	ro	WO	X		Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.330 solutiontable\_out\_jitter\_13



0xA0037140

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_13	ro	WO	X	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.
					Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

### 1.4.331 solutiontable\_out\_jitter\_14



0xA0037144

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_14	ro	WO	X	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.332 solutiontable\_out\_jitter\_15

Reg.

0xA0037148

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_15	ro	WO	X	Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.333 solutiontable\_out\_jitter\_16

Reg.

0xA003714C

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_16	ro	wo	X	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natu-
					ral jitter. This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

### 1.4.334 solutiontable\_out\_jitter\_17



0xA0037150

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

bits	name	s/w	h/w	default	description
	solutiontable_o ut_jitter_17	ro		X	Solution table sigmaC column.  Std of C signal during subCL update which quantifies natural jitter.  This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.  Each row represents a different DC, from 0.05 to 0.95, in
					steps of 0.05.

#### 1.4.335 solutiontable\_out\_jitter\_18



0xA0037154

Solution table sigmaC column.

Std of C signal during subCL update which quantifies natural jitter.

This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best.

bits	name	s/w	h/w	default	description
31:0	solutiontable_o ut_jitter_18	ro	WO	X	Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.

#### 1.4.336 solutiontable\_out\_jitter\_19 0xA0037158 Reg. Solution table sigmaC column. Std of C signal during subCL update which quantifies natural jitter. This metric is used to rank solutions with complete pre-sub-coalescence. Minimum sigmaC is the best. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05. bits name s/w h/w default description 31:0 solutiontable\_o ro wo X Solution table sigmaC column. Std of C signal during subCL update which quantifies natuut\_jitter\_19 This metric is used to rank solutions with complete pre-subcoalescence. Minimum sigmaC is the best.

Each row represents a different DC, from 0.05 to 0.95, in

1.4.3	1.4.337 solutiontable_out_multpresubrate_1 0xA003715C												
ILT M	ILT Multpresubrate												
bits name s/w h/w default description													
31:0	solutiontable_o ut_multpresubra te_1	ro	wo	X		ILT Multpresubrate							

steps of 0.05.

1.4.3	1.4.338 solutiontable_out_multpresubrate_2 0xA0037160												
ILT Multpresubrate													
bits	name	s/w	h/w		default		description	n					
31:0	solutiontable_o ut_multpresubra te_2	ro	wo	X		ILT Multpresubra	e						

1.4.3	39 solutiontable_ou	Reg.	0xA0037164										
ILT M	ILT Multpresubrate												
bits	name	s/w	h/w		default		description	n					
31:0	solutiontable_o ut_multpresubra te_3	ro	WO	X		ILT Multpresubrat	е						

1.4.3	40 solutiontable_ou	Reg.	0xA0037168									
ILT M	ILT Multpresubrate											
bits	name	s/w	h/w		default		description	n				
31:0	solutiontable_o ut_multpresubra te_4	ro	wo	X		ILT Multpresubrat	е					

1.4.3	1.4.341 solutiontable_out_multpresubrate_5 0xA003716C												
ILT Multpresubrate													
bits	name	s/w	h/w		default		descriptio	n					
31:0	solutiontable_o ut_multpresubra te_5	ro	wo	X		ILT Multpresubra	e						

1.4.3	1.4.342 solutiontable_out_multpresubrate_6 0xA0037170												
ILT Multpresubrate													
bits	bits name s/w h/w default description												
31:0 solutiontable_o ro wo X ILT Multpresubrate ut_multpresubra te_6													

1.4.3	1.4.343 solutiontable_out_multpresubrate_7 0xA0037174												
ILT M	ILT Multpresubrate												
bits	name	s/w	h/w		default		description	n					
31:0	solutiontable_o ut_multpresubra te_7	ro	WO	X		ILT Multpresubrat	е						

1.4.3	44 solutiontable_ou	Reg.	0xA0037178								
ILT Multpresubrate											
bits	name	s/w	h/w		default		description	n			
31:0	solutiontable_o ut_multpresubra te_8	ro	WO	X		ILT Multpresubra	te				

1.4.3	1.4.345 solutiontable_out_multpresubrate_9 0xA003717C												
ILT Multpresubrate													
bits	name	s/w	h/w		default		description	n					
31:0	solutiontable_o ut_multpresubra te_9	ro	wo	X		ILT Multpresubrate							

1.4.3	46 solutiontable_ou	Reg.	0xA0037180										
ILT M	ILT Multpresubrate												
bits	bits name s/w h/w default description												
31:0	solutiontable_o ut_multpresubra te_10	ro wo X ILT Multpresubrate											

1.4.3	47 solutiontable_ou	Reg.	0xA0037184									
ILT Multpresubrate												
bits	name	s/w	h/w		default		description	า				
31:0	solutiontable_o ut_multpresubra te_11	ro	wo	X		ILT Multpresubrat	е					

1.4.3	48 solutiontable_ou	Reg.	0xA0037188							
ILT Multpresubrate										
bits	name	s/w	h/w		default	description				
31:0	solutiontable_o ut_multpresubra te_12	ro	wo	X		ILT Multpresubrat	е			

1.4.3	49 solutiontable_ou	Reg.	0xA003718C							
ILT Multpresubrate										
bits	name	s/w	h/w	default	description					
31:0	solutiontable_o ut_multpresubra te_13	ro	wo	X	ILT Multpresubrat	е				

1.4.3	50 solutiontable_ou	Reg.	0xA0037190							
ILT Multpresubrate										
bits	name	s/w	h/w		default	description				
31:0	solutiontable_o ut_multpresubra te_14	ro	wo	X		ILT Multpresubra	e			

1.4.3	51 solutiontable_ou	Reg.	0xA0037194							
ILT Multpresubrate										
bits	name	s/w	h/w	default	description					
31:0	solutiontable_o ut_multpresubra te_15	ro	wo	X	ILT Multpresubrat	е				

1.4.3	52 solutiontable_ou	Reg.	0xA0037198								
ILT Multpresubrate											
bits	name	s/w	h/w	default		description					
31:0	solutiontable_o ut_multpresubra te_16	ro	WO	X	ILT Multpresubrat	е					

1.4.3	53 solutiontable_ou	Reg.		0xA003719C						
ILT Multpresubrate										
bits	name	s/w	h/w		default	description				
31:0	solutiontable_o ut_multpresubra te_17	ro	wo	X		ILT Multpresubrat	е			

1.4.3	54 solutiontable_ou	Reg.	0xA00371A0							
ILT Multpresubrate										
bits	name	s/w	h/w		default	description				
31:0	solutiontable_o ut_multpresubra te_18	ro	wo	X		ILT Multpresubrat	e			

1.4.3	1.4.355 solutiontable_out_multpresubrate_19 0xA00371A4											
ILT Multpresubrate												
bits	name	s/w	h/w	default		description						
31:0	solutiontable_o ut_multpresubra	ro	wo	X	ILT Multpresubrat	е						

	te_19							
1.4.3	56 solutiontable_ou	t_pre	subr	ate	_1		Reg.	0xA00371A8
	PreSubRate							
bits	name	s/w	h/w		default		desc	cription
31:0	solutiontable_o ut_presubrate_1	ro	WO	X		ILT PreSubRate		·
1.4.3	57 solutiontable_ou	t_pre	subr	ate	_2		Reg.	0xA00371AC
	PreSubRate							
bits	name	s/w	h/w	X	default	ILT PreSubRate	desc	cription
31:0	solutiontable_o ut_presubrate_2	ro	WO	^		ILT Presubrate		
1.4.3	58 solutiontable_ou	t_pre	subr	ate	_3		Reg.	0xA00371B0
	PreSubRate	_			-			
bits	name	s/w	h/w		default		desc	cription
31:0	solutiontable_o ut_presubrate_3	ro	wo	Χ		ILT PreSubRate		
	59 solutiontable_ou	t_pre	subr	ate	_4		Reg.	0xA00371B4
bits	name	s/w	h/w		default		desc	cription
31:0	solutiontable_o ut_presubrate_4	ro	WO	X		ILT PreSubRate		
1.4.3	60 solutiontable_ou	t_pre	subr	ate	_5		Reg.	0xA00371B8
ILT F	PreSubRate							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_presubrate_5	ro	WO	X		ILT PreSubRate		
1.4.3	61 solutiontable_ou	t_pre	subr	ate	_6		Reg.	0xA00371BC
ILT F	PreSubRate							
bits	name	s/w	h/w		default		desc	cription
31:0	solutiontable_o ut_presubrate_6	ro	wo	X		ILT PreSubRate		
1.4.3	62 solutiontable_ou	t_pre	subr	ate	_7		Reg.	0xA00371C0
ILT F	PreSubRate							
bits	name	s/w	h/w		default		desc	cription
31:0	solutiontable_o ut_presubrate_7	ro	WO	X		ILT PreSubRate		

ILT PreSubRate

1.4.363 solutiontable\_out\_presubrate\_8

Reg.

0xA00371C4

bits	name	s/w	h/w	default	description ILT PreSubRate	
31:0	solutiontable_o ut_presubrate_8	ro	wo	X	ILT Plesuprate	

1.4.3	64 solutiontable_ou	t_pre	subra	ate_9		Reg.	0xA00371C8
ILT P	reSubRate						
bits	name	s/w	h/w	default		description	1
31:0	solutiontable_o ut_presubrate_9	ro	wo	X	ILT PreSubRate		

1.4.3	65 solutiontable_ou	t_pre	subra	ate_	_10		Reg.	0xA00371CC
ILT P	reSubRate							
bits	name	s/w	h/w		default		descriptio	n
31:0	solutiontable_o ut_presubrate_1 0	ro	wo	X		ILT PreSubRate		

1.4.3	66 solutiontable_ou	t_pre	subra	ate_	_11		Reg.	0xA00371D0
ILT P	reSubRate							
bits	name	s/w	h/w		default		description	n
31:0	solutiontable_o ut_presubrate_1 1	ro	WO	X		ILT PreSubRate		

1.4.3	67 solutiontable_ou	t_pre	subra	ate_12		Reg.	0xA00371D4
ILT P	reSubRate						
bits	name	s/w	h/w	default		description	n
31:0	solutiontable_o ut_presubrate_1 2	ro	WO	X	ILT PreSubRate		

1.4.3	68 solutiontable_ou	t_pre	subra	ate <sub>.</sub>	_13		Reg.	0xA00371D8
ILT P	reSubRate							
bits	name	s/w	h/w		default		description	n
31:0	solutiontable_o ut_presubrate_1 3	ro	wo	X		ILT PreSubRate		

1.4.3	69 solutiontable_ou	t_pre	subra	ate	_14		Reg.	0xA00371DC
ILT P	reSubRate							
bits	name	s/w	h/w		default		description	n
31:0	solutiontable_o ut_presubrate_1 4	ro	WO	X		ILT PreSubRate		

1.4.37	0 solutiontable_ou	ıt_pre	subra	ite_15	Reg.	0xA00371E0
ILT Pre	eSubRate					
bits	name	s/w	h/w	default	descript	ion

31:0	solutiontable_o ut_presubrate_1 5	ro	WO	X		ILT PreSubRate		
1.4.3	71 solutiontable_c	out_pre	subra	ate	_16		Reg.	0xA00371E4
ILT F	PreSubRate							
bits	name	s/w	h/w		default			description
31:0	solutiontable_o ut_presubrate_1 6	ro	WO	X		ILT PreSubRate		
1.4.3	72 solutiontable_c	out pre	subra	ate	17		Reg.	0xA00371E8
	PreSubRate				<del>_</del>			
bits	name	s/w	h/w		default			description
31:0	solutiontable_o ut_presubrate_1 7	ro	WO	X		ILT PreSubRate		
1.4.3	73 solutiontable_c	out_pre	subra	ate	_18		Reg.	0xA00371EC
ILT F	PreSubRate							
bits	name	s/w	h/w		default			description
31:0	solutiontable_o ut_presubrate_1 8	ro	WO	X		ILT PreSubRate		
1 / 2	74 solutiontable_c	uit pro	cubr	nto	10		Reg.	0xA00371F0
	PreSubRate	ut_pre	Subi	ate	_13			0,0,10,001,11,0
bits		c/w	h/w		default			description
31:0	solutiontable_o ut_presubrate_1	ro	WO	X	deladit	ILT PreSubRate		чезоприон
1.4.3	75 solutiontable_c	out_cm	_1				Reg.	0xA00371F4
ILT C	CM							
bits	name	s/w	h/w		default			description
31:0	solutiontable_o ut_cm_1	ro	wo	X		ILT CM		
1.4.3	76 solutiontable_c	out_cm	_2				Reg.	0xA00371F8
ILT C	CM							
bits	name	s/w	h/w		default			description
31:0	solutiontable_o ut_cm_2	ro	WO	X		ILT CM		
1.4.3	77 solutiontable_c	out_cm_	_3				Reg.	0xA00371FC
ILT C	CM							
bits	name	s/w	h/w		default			description
31:0	solutiontable_o	ro	wo	Χ		ILT CM		

	ut_cm_3							
12	79 colutiontable ou	ıt om	1				Reg.	0xA0037200
	78 solutiontable_οι 	it_Ciii	_4					0xA0031200
ILT C		o hu	h/w		default		doo	orintian
1:0	name solutiontable_o ut_cm_4	s/w ro	WO	X	derauit	ILT CM	des	cription
.4.3	79 solutiontable_ou	ıt_cm	_5				Reg.	0xA0037204
ILT C	CM							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_cm_5	ro	WO	X		ILT CM		
43	80 solutiontable_ou	ıt cm	6				Reg.	0xA0037208
ILT C								
bits	name	s/w	h/w		default		dos	scription
1:0	solutiontable_o ut_cm_6	ro	WO	X	deladit	ILT CM	ues	СПриоп
.4.3	81 solutiontable_oเ	ıt_cm	_7				Reg.	0xA003720C
ILT C	CM							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_cm_7	ro	WO	X		ILT CM		
1 4 2		.4	0				Reg	0xA0037210
	82 solutiontable_ou	it_cm_	_0				Reg.	0XA0037210
ILT C		,	. ,					
bits 1:0	name solutiontable_o ut_cm_8	s/w ro	h/w wo	X	default	ILT CM	des	cription
.4.3	83 solutiontable_oเ	ıt_cm_	_9				Reg.	0xA0037214
ILT C	CM							
bits	name	s/w	h/w	V	default	U.T. O.M.	des	cription
1:0	solutiontable_o ut_cm_9	ro	WO	X		ILT CM		
12	94 colutiontable ou	ıt om	10				Reg.	0xA0037218
	84 solutiontable_ou	it_CIII	_10				Reg.	OM 10001 2 10
ILT C			1. /		-l-( ''			and the co
bits 1:0	name solutiontable_o ut_cm_10	s/w ro	h/w wo	X	default	ILT CM	des	cription
.4.3	85 solutiontable_oเ	ıt_cm	_11				Reg.	0xA003721C
ILT C	CM							

bits								
	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_cm_11	ro	wo	X		ILT CM		
1.4.3	86 solutiontable_d	out_cm	12				Reg.	0xA0037220
ILT (								
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_cm_12	ro	WO	X		ILT CM		
1.4.3	87 solutiontable_d	out_cm_	_13				Reg.	0xA0037224
ILT (	CM							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_cm_13	ro	wo	X		ILT CM		
1 1 2	88 solutiontable_d	aut am	11				Reg.	0xA0037228
		Jui_ciii	_14				********	0X/1000/220
ILT (								
bits 31:0	name solutiontable_o ut_cm_14	s/w ro	h/w wo	X	default	ILT CM	des	cription
1.4.3	89 solutiontable_d	out_cm_	_15				Reg.	0xA003722C
ILT (	CM							
ILT C	CM name	s/w	h/w		default		des	cription
		s/w ro		X	default	ILT CM	des	cription
bits	name solutiontable_o			X	default	ILT CM	des	cription
bits 31:0	name solutiontable_o	ro	wo	X	default	ILT CM	des	oxA0037230
bits 31:0	name solutiontable_o ut_cm_15	ro	wo	X	default	ILT CM		
bits 31:0	name solutiontable_o ut_cm_15	ro	wo	X	default	ILT CM	Reg.	
bits 31:0 <b>1.4.3</b> ILT (	name solutiontable_o ut_cm_15  90 solutiontable_c	ro  out_cm_	wo	X		ILT CM	Reg.	0xA0037230
bits 31:0 <b>1.4.3</b> ILT ( bits 31:0	name solutiontable_o ut_cm_15  690 solutiontable_o CM name solutiontable_o ut_cm_16	ro  out_cm_ s/w ro					Reg.	0xA0037230
bits 31:0 1.4.3 ILT ( bits 31:0	name solutiontable_o ut_cm_15  90 solutiontable_c CM  name solutiontable_o ut_cm_16	ro  out_cm_ s/w ro					Reg.	0xA0037230 cription
bits 31:0 1.4.3 ILT ( bits 31:0	name solutiontable_o ut_cm_15  90 solutiontable_c CM  name solutiontable_o ut_cm_16	ro  out_cm_ s/w ro					Reg.	0xA0037230 cription

ILT CM bits

31:0 solutiontable\_o

ut\_cm\_18

1.4.392 solutiontable\_out\_cm\_18

name

s/w h/w

wo X

ro

ILT CM

default

0xA0037238

Reg.

description

1.4.393 solut	iontable_ou	ıt_cm	_19				Reg.	0xA003723C
ILT CM								
	name	s/w	h/w	,	default	U <b>T</b> 014	desc	cription
solutionta ut_cm_19		ro	WO	X		ILT CM		
4 204 colut	lantable au	معالم 4	4				Reg.	0xA0037240
1.4.394 soluti	iontable_ou	it_am	_1				Reg.	0XA0037240
ILT DM bits	name	s/w	h/w		default		desc	cription
solutionta ut_dm_1		ro		X	deladit	ILT DM	4030	лрион
I.4.395 soluti	iontable ou	ıt dm	2				Reg.	0xA0037244
	iontable_ou	it_um						0X/ (000/ 244
ILT DM bits	name	s/w	h/w		default		door	cription
31:0 solutionta ut_dm_2	name ble_o	ro	WO	X	ueldull	ILT DM	ueso	ыγион
I.4.396 soluti	iontable ou	ıt dm	3				Reg.	0xA0037248
ILT DM								
	name	s/w	h/w		default		desc	cription
1:0 solutionta ut_dm_3		ro		X	doradit	ILT DM	4000	лен
I.4.397 soluti	iontable ou	ıt dm	4				Reg.	0xA003724C
ILT DM			_ •					
	name	s/w	h/w		default		desc	cription
31:0 solutionta ut_dm_4		ro	WO	X	doladit	ILT DM	4000	nipilo.
I.4.398 solut	iontable ou	ıt dm	5				Reg.	0xA0037250
ILT DM	iontable_oa	it_diii	_5				-	0,0 10001 200
	name	s/w	h/w		default		desc	cription
31:0 solutionta ut_dm_5		ro	WO	X	deladit	ILT DM	4030	лрион
I.4.399 solut	iontable ou	ıt dm	6				Reg.	0xA0037254
ILT DM								
bits	name	s/w	h/w		default		desc	cription
1:0 solutionta ut_dm_6	ble_o	ro	WO	X		ILT DM		
I.4.400 solut	iontable_ou	ıt_dm	_7				Reg.	0xA0037258
ILT DM								
	name	s/w	h/w		default		desc	cription
s1:0 solutionta		ro	WO	X		ILT DM		
ut_dm_7								

1.4.4	01 solutiontable_c	out_dm	_8				Reg.	0xA003725C
ILT D	DM							
bits	name	s/w	h/w		default		des	cription
1:0	solutiontable_o ut_dm_8	ro	WO	X		ILT DM		
	ut_um_o							
.4.4	02 solutiontable_d	out_dm	_9				Reg.	0xA0037260
LT C	DM							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o	ro	wo	Χ		ILT DM		•
	ut_dm_9							
.4.4	03 solutiontable_c	out_dm	_10				Reg.	0xA0037264
ILT D	DM							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_dm_10	ro	WO	X		ILT DM		
1.4.4	04 solutiontable_c	out_dm	_11				Reg.	0xA0037268
ILT C	DM							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_dm_11	ro	WO	X		ILT DM		
1.4.4 ILT C	05 solutiontable_c	out_dm	_12				Reg.	0xA003726C
bits		s/w	h/w		default		des	cription
31:0	solutiontable_o ut_dm_12	ro	wo		doradit	ILT DM	400	onpuon
1.4.4	06 solutiontable_c	out_dm	_13				Reg.	0xA0037270
ILT D	DM							
bits	name	s/w	h/w		default		des	cription
31:0	solutiontable_o ut_dm_13	ro	WO	Х		ILT DM		
1.4.4	07 solutiontable_d	out_dm	_14				Reg.	0xA0037274
ILT D								
bits		s/w	h/w		default		des	cription
31:0	solutiontable_o ut_dm_14	ro	WO	X		ILT DM		
1.4.4	08 solutiontable_c	out_dm	_15				Reg.	0xA0037278
ILT D	DM		h/w		default			cription

31:0								
, i .U	solutiontable_o ut_dm_15	ro	WO	X		ILT DM		
.4.4	09 solutiontable_o	ut_dm	_16				Reg.	0xA003727C
ILT [	DM							
bits	name	s/w	h/w	V	default	II T DM	des	scription
1:0	solutiontable_o ut_dm_16	ro	wo	X		ILT DM		
44	10 solutiontable_o	out dm	17				Reg.	0xA0037280
ILT D		at_am						
		o hu	h/w		default		dos	parintian
bits 31:0	name solutiontable_o	s/w ro	WO	Χ	derauit	ILT DM	ues	scription
71.0	ut_dm_17	10	WO			IET DIWI		
.4.4	11 solutiontable_o	ut_dm	_18				Reg.	0xA0037284
ILT D	DM							
bits	name	s/w	h/w		default		des	scription
31:0	solutiontable_o ut_dm_18	ro	WO	X		ILT DM		•
ILT D bits 31:0	DM name solutiontable_o	s/w ro	h/w wo	X	default	ILT DM	des	scription
	ut dm 10					ILI DIVI		
	ut_dm_19					ILI DIVI		
1.4.4	13 solutiontable_o	out_dcd				ILT DIVI	Reg.	0xA003728C
1 <b>.4.4</b> ILT [	13 solutiontable_o		lphi		dofoult	ILT DIVI		
I.4.4 ILT [ bits	13 solutiontable_o	s/w ro	lphi h/w	X	default	ILT DCDPhi		0xA003728C scription
I.4.4 ILT [ bits	213 solutiontable_o DCDPhi name solutiontable_o	s/w	lphi h/w	X	default			
.4.4 ILT [ bits :1:0	213 solutiontable_o DCDPhi name solutiontable_o	s/w ro	h/w wo					
I.4.4 ILT E bits 31:0	name solutiontable_o ut_dcdphi	s/w ro	h/w wo	gir	n_1	ILT DCDPhi	des	scription
I.4.4 ILT E bits 31:0	name solutiontable_o ut_dcdphi  14 solutiontable_o tion table phi1 column.	s/w ro	h/w wo	gir	n_1	ILT DCDPhi	Reg.	scription
I.4.4 ILT E bits 31:0	name solutiontable_o ut_dcdphi  14 solutiontable_o tion table phi1 column. row represents a differen	s/w ro	h/w wo	gir	1_1 o 0.95, in s	ILT DCDPhi steps of 0.05. Solution table p	des Reg. des hi1 column.	oxA0037290
I.4.4 ILT E bits 31:0 Solut Each bits 31:0	name solutiontable_o ut_dcdphi  14 solutiontable_o tion table phi1 column. row represents a difference name solutiontable_o ut_phi1margin_1	s/w ro ent DC, fr	h/w wo 1mar om 0.0 h/w wo	gir 05 to X	n_1 o 0.95, in s default	ILT DCDPhi steps of 0.05. Solution table p Each row repre	des des hi1 column. sents a differ	0xA0037290 Scription rent DC, from 0.05 to 0.95, in
J.4.4 ILT E bits 11:0 Solur Each bits 11:0	name solutiontable_o ut_dcdphi  14 solutiontable_o tion table phi1 column. row represents a difference name solutiontable_o ut_phi1margin_1	s/w ro ent DC, fr s/w ro	h/w wo 1mar om 0.0 h/w wo	opir O5 to X	1_1 o 0.95, in s default	ILT DCDPhi steps of 0.05.  Solution table p Each row represteps of 0.05.	des Reg. des hi1 column.	0xA0037290 Scription
J.4.4 ILT E bits 11:0 Solur Each bits 11:0	name solutiontable_o ut_dcdphi  14 solutiontable_o tion table phi1 column. row represents a difference name solutiontable_o ut_phi1margin_1	s/w ro ent DC, fr s/w ro	h/w wo 1mar om 0.0 h/w wo	opir O5 to X	1_1 o 0.95, in s default	ILT DCDPhi steps of 0.05.  Solution table p Each row represteps of 0.05.	des des	0xA0037290  Scription  rent DC, from 0.05 to 0.95, in  0xA0037294
I.4.4 ILT E bits 31:0 I.4.4 Solur Each bits 31:0	name solutiontable_o ut_dcdphi  14 solutiontable_o tion table phi1 column. row represents a difference name solutiontable_o ut_phi1margin_1	s/w ro ent DC, fr s/w ro	h/w wo 1mar om 0.0 h/w wo	opir O5 to X	1_1 o 0.95, in s default	ILT DCDPhi steps of 0.05.  Solution table p Each row represteps of 0.05.	des	0xA0037290 Scription rent DC, from 0.05 to 0.95, in

1.4.4	16 solutiontable_	out_phi	1mar	gin_3		Reg.	0xA0037298
	ion table phi1 column. row represents a diffe	rent DC, fr	om 0.0	05 to 0.95, in	steps of 0.05.		
bits	name	s/w	h/w	default		description	n
							•
31:0	solutiontable_o	ro	wo	X	Solution table phi	1 column.	

1.4.4	17 solutiontable_ou	t_phi	1mar	gin	_4		Reg.	0xA003729C
	ion table phi1 column. row represents a differen	t DC, fr	om 0.0	)5 tc	0.95, in	steps of 0.05.		
bits	name	s/w	h/w		default		descriptio	n
31:0	solutiontable_o ut_phi1margin_4	ro	WO	X		Solution table phi Each row represe steps of 0.05.		C, from 0.05 to 0.95, in

1.4.4	18 solutiontable_ou	t_phi	1mar	gin_5	Reg.	0xA00372A0
	ion table phi1 column. row represents a different	DC, fr	om 0.0	5 to 0.95, in s	teps of 0.05.	ion
31:0	solutiontable_o ut_phi1margin_5	ro		X	Solution table phi1 column. Each row represents a different I steps of 0.05.	

1.4.4	19 solutiontable_d	out_phi	1mar	gin	_6	Re	eg.	0xA00372A4
	ion table phi1 column. row represents a differ	ent DC, fr	om 0.0	)5 to	0.95, in	steps of 0.05.		
bits	name	s/w	h/w		default		description	n
31:0	solutiontable_o ut_phi1margin_6	ro	wo	X		Solution table phi1 of Each row represents steps of 0.05.		C, from 0.05 to 0.95, in

1.4.4	20 solutiontable_d	out_phi	1mar	gin	_7	Reg	g.	0xA00372A8
	ion table phi1 column. row represents a differ	ent DC, fr	om 0.0	)5 to	0.95, in	steps of 0.05.		
bits	name	s/w	h/w		default		description	n
31:0	solutiontable_o ut_phi1margin_7	ro	WO	X		Solution table phi1 contact Each row represents steps of 0.05.		C, from 0.05 to 0.95, in

1.4.4	21 solutiontable_	out_phi	1mar	gin_8		Reg.	0xA00372AC
	ion table phi1 column. row represents a differ	rent DC, fr	om 0.0	05 to 0.95, in	steps of 0.05.	descrii	ntion
31:0	solutiontable_o ut_phi1margin_8	ro	WO	X	Solution table phi Each row represe steps of 0.05.	1 column.	t DC, from 0.05 to 0.95, in

1.4.4	22 solutiontable_ou	ut_phi	1mar	gin_9	Reg.	0xA00372B0
	ion table phi1 column. row represents a differer	nt DC, fr	om 0.0	05 to 0.95, in s	steps of 0.05.	
bits	name	s/w	h/w	default	des	cription
31:0	solutiontable_o	ro	wo	X	Solution table phi1 column.	
	ut_phi1margin_9				Each row represents a differ steps of 0.05.	ent DC, from 0.05 to 0.95, in

1.4.4	23 solutiontable_o	ut_phi	1mar	gin_10	Reg.	0xA00372B4
	ion table phi1 column. row represents a differen	nt DC, fr	om 0.0		steps of 0.05.	
bits	name	s/w	h/w	default	d	lescription
31:0	solutiontable_o ut_phi1margin_1	ro	wo	X	Solution table phi1 column Each row represents a diff steps of 0.05.	n. ferent DC, from 0.05 to 0.95, in

1.4.4	24 solutiontable_οι	ıt_phi	1mar	gin_11		Reg.	0xA00372B8
Each	ion table phi1 column. row represents a differen				steps of 0.05.		
bits	name	s/w	h/w	default		descriptio	n
31:0	solutiontable_o ut_phi1margin_1	ro	wo	X	Solution table phi1 Each row represer		from 0.05 to 0.95 in

1.4.4	25 solutiontable_ou	Re	g.	0xA00372BC							
	Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default		descriptio	n				
31:0											

1.4.4	1.4.426 solutiontable_out_phi1margin_13 0xA00372C0											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
		,			0.000							
bits	name	s/w	h/w	default	окоро от отоо.	descriptio	n					

1.4.4	1.4.427 solutiontable_out_phi1margin_14 0xA00372C4											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.												
bits	name	s/w	h/w	default		description	n					
~ 4 ^	31:0 solutiontable_o ro wo X Solution table phi1 column.  ut_phi1margin_1 4 Solution table phi2 column.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											

1.4.428 solutiontable_out_phi1margin_15	Reg.	0xA00372C8
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.		

bits	name	s/w	h/w	default	description
31:0	solutiontable_o	ro	wo	X	Solution table phi1 column.
	ut_phi1margin_1				Each row represents a different DC, from 0.05 to 0.95, in
	5				steps of 0.05.

1.4.4	1.4.429 solutiontable_out_phi1margin_16 0xA00372CC												
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.													
bits	name	s/w	h/w	default		description	n						
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1												

1.4.4	30 solutiontable_ou	0xA00372D0									
Solution table phi1 column.  Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits name s/w h/w default description 31:0 solutiontable_o ro wo X Solution table phi1 column. ut_phi1margin_1 Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											

1.4.4	31 solutiontable_d	out_phi		Reg.	0xA00372D4					
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.										
bits	name	s/w	h/w	default		descriptio	n			
31:0										

1.4.432 solutiontable_out_phi1margin_19 0xA00372D8											
Solution table phi1 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
	bits name s/w h/w default description										
bits	name	s/w	h/w	default		descriptio	n				

1.4.4	33 solutiontable_ou	Reg.	0xA00372DC								
Solution table phi0 column. Each row represents a different DC, from 0.05 to 0.95, in steps of 0.05.											
bits	name	s/w	h/w	default		descriptio	n				
31:0											

1.4.4	34 solutiontable_ou	Reg.	0xA00372E0								
Solut	Solution table satrateavg_off										
bits	name	s/w	h/w		default		description	า			
31:0											

1.4.4	35 solutiontable_ou	Reg.	0xA00372E4							
Solution table satrateavg_on										
bits	name	s/w	h/w		default		description			
31:0	solutiontable_o ut_satrateavg_o n	ro	wo	X		Solution table sat	rateavg_on			

1.4.4	1.4.436 solutiontable_out_xint3sigma_avg 0xA00372E8											
Solution table xint3sigma_avg												
bits	name	s/w	h/w		default		description	า				
31:0	solutiontable_o ut_xint3sigma_a vg	ro	wo	X		Solution table xin	t3sigma_avg					

1.4.4	1.4.437 solutiontable_out_presubrate_avg 0xA00372EC											
Solution table presubrate_avg												
bits	name	s/w	h/w		default		description	n				
31:0	solutiontable_o ut_presubrate_a vg	ro	WO	X		Solution table pre	subrate_avg					

1.4.4	38 solutiontable_oเ		Reg.	0xA00372F0							
Optimum Solution											
bits	name	s/w	h/w	default		description	n				
31:0 solutiontable_o ro wo X Optimum Solution ut_opt_solution											

1.4.4	39 solutiontable_ou		Reg.	0xA00372F4								
Back	Backuo Solution Index											
bits	name	s/w	h/w	default		description	า					
31:0												

1.4.4	40 region_7_end_tag	Reg.	0xA00372F8								
regio	region_7_end_tag										
bits	name	s/w	h/w	default		description	١				
31:0 region_7_end_ta ro wo X region_7_end_tag											

1.4.4	41 region_8_start_ta	Reg.	0xA0038000								
region_8_start_tag											
bits	name	s/w	h/w	default		description	n				
31:0 region_8_start_ ro wo X region_8_start_tag											

	42 region_8_dtec_	_tod_lsl	bs		Reg.	0xA0038004
regio	n_8_dtec_tod_lsbs					
bits	name	s/w	h/w	default	des	cription
31:0	region_8_dtec_t od_lsbs	ro	wo	Х	region_8_dtec_tod_lsbs	
1 1 1		tod m	cho		Reg.	0×40038008
	43 region_8_dtec_	_tod_m	sbs		Reg.	0xA0038008
		_tod_ms	sbs	default	_	0xA0038008

1.4.4	44 region_8_dtec_lt	Reg.	0xA003800C									
regio	region_8_dtec_lts											
bits	name	s/w	h/w	default		description	า					
31:0 region_8_dtec_I ro wo X region_8_dtec_lts ts												

1.4.4	45 req_func_out	Reg.	0xA0038010								
Read	Readback of diagnostics signature for main CL algo block										
bits	name	s/w	h/w	default		description	٦				
31:0	req_func_out	ro	wo	Χ	Readback of diagn	ostics signature	for main CL algo block				

1.4.4	46 state	Reg.	0xA0038014								
Read	back of diagnostics signat	ure for	monito	r algo block							
bits	name	s/w	h/w	default	descript	ion					
31:0 state ro wo X Readback of diagnostics signature for monitor algo block											

1.4.4	47 test_probes_prol	Reg.	0xA0038018								
Generic Test Probe 1											
bits	name	s/w	h/w	default		description	n				
31:0 test_probes_pro ro wo X Generic Test Probe 1											

1.4.4	48 test_probes_prob		Reg	0xA003801C							
Gene	Generic Test Probe 2										
bits	name	s/w	h/w	default		description	n				
31:0 test_probes_pro ro wo X Generic Test Probe 2 be2											

1.4.4	1.4.449 test_probes_probe3 0xA0038020											
Generic Test Probe 3												
bits	name	s/w	h/w	default	des	scription						
bits name s/w h/w default description  31:0 test_probes_pro ro wo X Generic Test Probe 3 be3												

1.4.4	50 internal_clst_dor	ne_lat	ched		Re	eg.	0xA0038024					
Deter	Determines if CLST algo has converged for any given milisecond											
bits	name	s/w	h/w	default		description	า					
31:0												

1.4.4	1.4.451 diag_exposure_prerisetime 0xA0038028											
Rise time within 20ms (ETEC to DTEC)												
bits	name	s/w	h/w	default		description	ı					
31:0 diag_exposure_p ro wo X Rise time within 20ms (ETEC to DTEC) rerisetime												

1.4.4	52 diag_exposure_e	Reg.	0xA003802C								
new o	Exposure gate signal into the dTEC algo to be 2 bit wide, with MSB being a write flag indicating new data written (1 = new data written) and LSB is the 1 bit Exposure Gate Signal.  Expand the buffer and dTEC algo for the exposure gate to receive up to 70 values in 1ms timeframe.										
bits	name	s/w	h/w	default		description	n				
31:0	diag_exposure_e xposure_flag	ro	WO	X	with MSB being a new data written) nal.	write flag indicati and LSB is the 1	C algo to be 2 bit wide, ing new data written (1 = bit Exposure Gate Sig- for the exposure gate to be frame.				

1.4.4	53 diag_exposure_	_falltim	e_fla	g		Reg.	0xA0038030						
Fall-ti	Fall-time detected for exposure signals.												
bits	name	s/w	h/w	default		description	n						
31:0													

1.4.4	1.4.454 diag_exposure_risetime_flag 0xA0038034											
Rise-	Rise-time detected for exposure signals.											
bits	name	s/w	h/w	default		description	٦					
31:0 diag_exposure_r ro wo X Rise-time detected for exposure signals.												

1.4.4	1.4.455 diag_state_diag											
Read	back of diagnostics signa	ture for	curren	nt st	tate							
bits	name	s/w	h/w		default	d	escription	٦				
31:0 diag_state_diag ro wo X Readback of diagnostics signature for current state												

1.4.4	56 xer_out_xer_ban	Reg.		0xA003803C								
XER	XER Bank 1											
bits	name	s/w	h/w		default		de	escriptio	n			
31:0 xer_out_xer_ban ro wo X XER Bank 1												

	bank2							
bits	name	s/w	h/w		default		d	escription
31:0	xer_out_xer_ban k2	ro	wo	X	doladit	XER bank2	u	occupaci.
.4.4	58 events_out_eve	nts_ba	ank1				Reg.	0xA0038044
Ever	nts Bank1							
bits	name	s/w	h/w		default		d	escription
31:0	events_out_even ts_bank1	ro	WO	X		Events Bank1		
	59 events_out_eve	nts_ba	ank2				Reg.	0xA0038048
Ever	nts Bank2							
bits	name	s/w	h/w		default	_	d	escription
31:0	events_out_even ts_bank2	ro	WO	X		Events Bank2		
	100			1	-4		Reg	0xA003804C
	60 warnings_out_v	varnin	gs_b	anı	KI		Reg.	UXA003604C
Warr	nings Bank1							
bits	name	s/w	h/w		default		d	escription
bits 31:0	name warnings_out_wa rnings_bank1	s/w ro	h/w wo	X	default	Warnings Bank1	d	escription
31:0	warnings_out_wa rnings_bank1	ro	WO			Warnings Bank1		
31:0	warnings_out_wa	ro	WO			Warnings Bank1	Reg.	escription  0xA0038050
31:0 1.4.4	warnings_out_wa rnings_bank1	ro	WO			Warnings Bank1		
31:0 1.4.4	warnings_out_wa rnings_bank1	ro	WO			Warnings Bank1	Reg.	
31:0 1.4.4 Warr	warnings_out_wa rnings_bank1  61 warnings_out_v nings Bank2	ro	wo gs_b		k2	Warnings Bank1 Warnings Bank2	Reg.	0xA0038050
31:0 1.4.4 Warr bits 31:0	warnings_out_wa rnings_bank1  661 warnings_out_v  nings Bank2  name warnings_out_wa rnings_bank2	varning s/w ro	wo gs_b	anl	k2		Reg.	0xA0038050 escription
31:0 1.4.4 Warr bits 31:0	warnings_out_wa rnings_bank1  661 warnings_out_va nings Bank2  name warnings_out_wa rnings_bank2	varning s/w ro	wo gs_b	anl	k2		Reg.	0xA0038050
31:0 1.4.4 Warr bits 31:0	warnings_out_wa rnings_bank1  661 warnings_out_v  nings Bank2  name warnings_out_wa rnings_bank2	varning s/w ro	wo gs_b	anl	k2		Reg.	0xA0038050 escription
11.4.4 Warr bits 31:0	warnings_out_warnings_bank1  661 warnings_out_wanings Bank2  name warnings_out_warnings_bank2  662 region_8_end_tempon_8_end_tempon_8_end_tag  name	varning s/w ro	wo gs_b h/w wo	x	k2	Warnings Bank2	Reg.	0xA0038050 escription
11.4.4 Warr bits 31:0	warnings_out_warnings_bank1  61 warnings_out_wanings Bank2  name warnings_out_warnings_bank2  62 region_8_end_temp_on_8_end_temp_on_8_end_tag	ro varning s/w ro	wo gs_b h/w wo	anl	k2 default		Reg.	0xA0038050 escription 0xA0038054
11.4.4 Warr bits 31:0	warnings_out_wa rnings_bank1  661 warnings_out_va nings Bank2  name warnings_out_wa rnings_bank2  662 region_8_end_t  n_8_end_tag  name region_8_end_ta	s/w ro	wo gs_b h/w wo	x	k2 default	Warnings Bank2	Reg.	0xA0038050 escription 0xA0038054
bits 31:0	warnings_out_wa rnings_bank1  661 warnings_out_va nings Bank2  name warnings_out_wa rnings_bank2  662 region_8_end_t  n_8_end_tag  name region_8_end_ta	s/w ro	wo gs_b h/w wo	x	k2 default	Warnings Bank2	Reg.	0xA0038050 escription 0xA0038054
11.4.4 Warr bits 31:0	warnings_out_warnings_bank1  661 warnings_out_warnings Bank2  name warnings_out_warnings_bank2  662 region_8_end_tempon_8_end_tempon_8_end_tag  name region_8_end_tag  g	s/w ro	wo gs_b h/w wo	x	k2 default	Warnings Bank2	Reg.	0xA0038050 escription 0xA0038054 escription
31:0 Warr bits 31:0 bits 31:0	warnings_out_warnings_bank1  661 warnings_out_warnings Bank2  name warnings_out_warnings_bank2  662 region_8_end_tempon_8_end_tempon_8_end_tag  name region_8_end_tag  g  663 region_9_start_	s/w ro	wo gs_b h/w wo	x	k2 default	Warnings Bank2	Reg.	0xA0038050 escription 0xA0038054 escription

bits

region\_9\_dtec\_tod\_lsbs

name

s/w

h/w

description

default

31:0	region_9_dtec_t od_lsbs	ro	WO	X		region_9_dtec_to	d_lsbs	
1.4.4	65 region_9_dtec_to	od_m	sbs				Reg.	0xA0039008
regio	n_9_dtec_tod_msbs							
bits	name	s/w	h/w	.,	default			cription
31:0	region_9_dtec_t od_msbs	ro	WO	X		region_9_dtec_to	a_msbs	
1.4.4	66 region_9_dtec_lt	S					Reg.	0xA003900C
	n_9_dtec_lts							
bits	name	s/w	h/w		default		des	cription
31:0	region_9_dtec_l ts	ro	WO	X	doladit	region_9_dtec_lts		onpuon
1.4.4	67 dcm_diag_missii	ng_dr	ople	ts			Reg.	0xA0039010
	ng main droplets in 1ms							
bits	name	s/w	h/w	V	default	Migging grant in al		cription
31:0	dcm_diag_missin g_droplets	ro	WO	X		Missing main drop	olets in 1ms	<b>S</b>
1.4.4	68 dcm_diag_pklab	els_ro	oi1_1				Reg.	0xA0039014
Labe	ls for first ROI							
bits	name	s/w	h/w		default		des	cription
31:0	dcm_diag_pklabe ls_roi1_1	ro	wo	Χ		Labels for first RC	)I	
	15_1011_1							
1.4.4	69 dcm_diag_pklabo	els_ro	oi1_2				Reg.	0xA0039018
Labe	ls for first ROI							
bits	name	s/w	h/w		default		des	cription
31:0	dcm_diag_pklabe ls_roi1_2	ro	wo	X		Labels for first RC	)I	
	15_1011_2							
		_						0.40000040
1.4.4	70 dcm_diag_pklab	els_ro	oi1_3				Reg.	0xA003901C
Labe	ls for first ROI							
bits	name	s/w	h/w	V	default	I obole for first DC		cription
31:0	dcm_diag_pklabe ls_roi1_3	ro	WO	X		Labels for first RC	)I	
1.4.4	71 dcm_diag_pklabe	els_ro	oi1_4				Reg.	0xA0039020
Labe	ls for first ROI							
bits	name	s/w	h/w		default			cription
31:0	dcm_diag_pklabe ls_roi1_4	ro	wo	X		Labels for first RC	)l	

1.4.472 dcm\_diag\_pklabels\_roi1\_5

0xA0039024

Label	Labels for first ROI												
bits	name	s/w	h/w	default	description								
31:0	dcm_diag_pklabe	ro	wo	X	Labels for first ROI								
	ls_roi1_5												

1.4.4	1.4.473 dcm_diag_pklabels_roi1_6 0xA0039028											
Labels for first ROI												
bits	name	s/w	h/w	default		description	n					
31:0 dcm_diag_pklabe ro wo X Labels for first ROI ls_roi1_6												

1.4.4	74 dcm_diag_pklabe	Reg.	0xA003902C								
Labels for first ROI											
bits	name	s/w	h/w	defaul		description	ı				
31:0 dcm_diag_pklabe ro wo X Labels for first ROI ls_roi1_7											

1.4.4	75 dcm_diag_pklab	Reg.	0xA0039030								
Labels for first ROI											
bits	name	s/w	h/w	default		description	า				
31:0 dcm_diag_pklabe ro wo X Labels for first ROI ls_roi1_8											

1.4.4	76 dcm_diag_pklab	Reg.	0xA0039034								
Labels for first ROI											
bits	name	s/w	h/w	default		description	n				
31:0 dcm_diag_pklabe ro wo X Labels for first ROI ls_roi1_9											

1.4.4	77 dcm_diag_pklabe	Reg.	0xA0039038									
Labels for first ROI												
bits	name	s/w	h/w	default		description	n					
31:0 dcm_diag_pklabe ro wo X Labels for first ROI ls_roi1_10												

1.4.4	78 dcm_diag_pklab	Reg.	0xA003903C									
Labels for first ROI												
bits	name	s/w	h/w	default		description	า					
31:0 dcm_diag_pklabe ro wo X Labels for first ROI ls_roi1_11												

1.4.4	79 dcm_diag_pklab	Reg.	0xA0039040								
Labels for first ROI											
bits	name	s/w	h/w	default		description	n				
31:0 dcm_diag_pklabe ro wo X Labels for first ROI ls_roi1_12											

Labe	ls for first ROI							
bits	name	s/w	h/w		default		description	n
31:0	dcm_diag_pklabe ls_roi1_13	ro	WO	X		Labels for first ROI		
								2 4 2 2 2 2 4 2
	81 dcm_diag_pklab	els_ro	0i1_1	4		Reg		0xA0039048
Labe	ls for first ROI							
bits 31:0	name dcm_diag_pklabe ls_roi1_14	s/w ro	h/w wo	X	default	Labels for first ROI	descriptio	n
			14 4	_		Date		0.40020040
	82 dcm_diag_pklab	eis_ro	011_1	5		Reg		0xA003904C
	ls for first ROI							
bits 31:0	name dcm_diag_pklabe	s/w	h/w	Χ	default	Labels for first ROI	description	n
,1.0	ls_roi1_15	ro	WO	^		Labels for first KOI		
1.4.4	83 dcm_diag_pklab	els_r	oi1_1	6		Reg	-	0xA0039050
Labe	els for first ROI							
bits	name	s/w	h/w		default		description	n
31:0	dcm_diag_pklabe	ro	wo	Χ		Labels for first ROI		
	ls_roi1_16							
	84 dcm_diag_pklab	oels_ro	oi1_1	7		Reg		0xA0039054
Labe	84 dcm_diag_pklab			7		Reg		
Labe bits	84 dcm_diag_pklab els for first ROI name	s/w	h/w		default		descriptio	
Labe	84 dcm_diag_pklab		h/w	7 X	default	Labels for first ROI		
Labe bits	84 dcm_diag_pklak els for first ROI name dcm_diag_pklabe	s/w	h/w		default			
Labe bits 31:0	84 dcm_diag_pklak els for first ROI name dcm_diag_pklabe	s/w ro	h/w wo	X	default		descriptio	
Labe bits 31:0	els for first ROI name dcm_diag_pklabe ls_roi1_17	s/w ro	h/w wo	X	default	Labels for first ROI	descriptio	n
Labe bits 31:0	els for first ROI name dcm_diag_pklabe ls_roi1_17  els dcm_diag_pklabe ls_roi1_17	s/w ro	h/w wo	X	default	Labels for first ROI	descriptio	oxA0039058
Labe bits 31:0	e84 dcm_diag_pklakels for first ROI  name dcm_diag_pklabe ls_roi1_17  e85 dcm_diag_pklakels for first ROI  name dcm_diag_pklabe	s/w ro	h/w wo	X		Labels for first ROI	descriptio	oxA0039058
Labe bits 31:0	els for first ROI name dcm_diag_pklabe ls_roi1_17  els dcm_diag_pklabe ls_roi1_17	s/w ro	h/w wo	X		Labels for first ROI	descriptio	oxA0039058
Labe bits 31:0 1.4.4 Labe bits 31:0	els for first ROI name dcm_diag_pklabe ls_roi1_17  els dcm_diag_pklabe ls_roi1_18	s/w ro	h/w wo	X X		Labels for first ROI  Reg Labels for first ROI	descriptio	oxA0039058
Labee bits 31:0	name dcm_diag_pklak ls for first ROI  name dcm_diag_pklabe ls_roi1_17  85 dcm_diag_pklak ls for first ROI  name dcm_diag_pklabe ls_roi1_18	s/w ro	h/w wo	X X		Labels for first ROI	descriptio	oxA0039058
Labee bits 31:0  1.4.4 Labee bits 31:0	els for first ROI name dcm_diag_pklabe ls_roi1_17  els dcm_diag_pklabe ls_roi1_18  els for first ROI name dcm_diag_pklabe ls_roi1_18  els for first ROI sels for first ROI sels for first ROI	s/w ro	h/w wo bi1_12 h/w wo	X X	default	Labels for first ROI  Reg Labels for first ROI	descriptio	0xA0039058 n
Labee bits 31:0  1.4.4  Labee bits 31:0	els for first ROI  name dcm_diag_pklabe ls_roi1_17  els dcm_diag_pklabe ls_roi1_18  els for first ROI  name dcm_diag_pklabe ls_roi1_18  els for first ROI  name name name name name name ls_roi1_18	s/w ro  pels_ro  s/w ro  s/w	h/w wo bi1_1:	X X		Labels for first ROI  Labels for first ROI	descriptio	0xA0039058 n
Labee bits 31:0  1.4.4 Labee bits 31:0	els for first ROI name dcm_diag_pklabe ls_roi1_17  els dcm_diag_pklabe ls_roi1_18  els for first ROI name dcm_diag_pklabe ls_roi1_18  els for first ROI sels for first ROI sels for first ROI	s/w ro	h/w wo bi1_1:	X X	default	Labels for first ROI  Reg Labels for first ROI	descriptio	0xA0039058
Labee bits 31:0  1.4.4  Labee bits 31:0	els for first ROI  name dcm_diag_pklabe ls_roi1_17  els dcm_diag_pklabe ls_roi1_18  els for first ROI  name dcm_diag_pklabe ls_roi1_18  els for first ROI  name dcm_diag_pklabe ls_roi1_18	s/w ro  pels_ro  s/w ro  s/w	h/w wo bi1_1:	X X	default	Labels for first ROI  Labels for first ROI	descriptio	0xA0039058 n

bits

name

s/w h/w

description

default

31:0	dcm_diag_pklabe ls_roi1_20	ro	wo	X		Labels for first RO	OI	
1.4.4	88 dcm_diag_pklab	els_rc	oi1_2	1			Reg.	0xA0039064
Labe	ls for first ROI							
bits	name	s/w	h/w		default			cription
31:0	dcm_diag_pklabe ls_roi1_21	ro	WO	X		Labels for first R0	ال	
4 4 4	00 dam dian uldah	ala va	:4 0	2			Reg	0×40030069
	89 dcm_diag_pklabe	eis_rc	011_2	2			Reg.	0xA0039068
	ls for first ROI	,	. ,					
bits 31:0	name dcm_diag_pklabe ls_roi1_22	s/w ro	h/w wo	Χ	default	Labels for first RO		cription
	15_1011_22							
1.4.4	90 dcm_diag_pklab	els_rc	oi1_2	3			Reg.	0xA003906C
Labe	ls for first ROI							
bits	name	s/w	h/w		default		des	cription
31:0	dcm_diag_pklabe ls_roi1_23	ro	wo	X		Labels for first R0	Ol	
1.4.4	91 dcm_diag_pklabo	els_rc	oi1_2	4			Reg.	0xA0039070
Labe	ls for first ROI							
bits	name	s/w	h/w		default			cription
31:0	dcm_diag_pklabe ls_roi1_24	ro	WO	X		Labels for first R0	OI	
1.4.4	92 dcm_diag_pkpos	globa	al_roi	1_	1		Reg.	0xA0039074
Glob	al pk positions for first ROI							
bits	name	s/w	h/w		default			cription
31:0	dcm_diag_pkposg lobal_roi1_1	ro	WO	X		Global pk position	ns for first F	ROI
1.4.4	93 dcm_diag_pkpos	globa	al_roi	1_	2		Reg.	0xA0039078
	al pk positions for first ROI							
bits	name	s/w	h/w	X	default	Clobal alvassidis		cription
31:0	dcm_diag_pkposg lobal_roi1_2	ro	WO	^		Global pk position	ns for first r	KOI
1.4.4	94 dcm_diag_pkpos	globa	al_roi	1_	3		Reg.	0xA003907C
Glob	al pk positions for first ROI							
bits	name	s/w	h/w	V	default	Clobal alvasairis		cription
31:0	dcm_diag_pkposg lobal_roi1_3	ro	WO	X		Global pk position	is for tirst h	(UI

1.4.495 dcm\_diag\_pkposglobal\_roi1\_4

0xA0039080

Globa	Global pk positions for first ROI										
bits	name	s/w	h/w	default	description						
31:0	dcm_diag_pkposg lobal_roi1_4	ro	wo	X	Global pk positions for first ROI						

1.4.4	96 dcm_diag_pkpos	Reg.	0xA0039084									
Global pk positions for first ROI												
bits	name	s/w	h/w	default		description	n					
31:0 dcm_diag_pkposg ro wo X Global pk positions for first ROI lobal_roi1_5												

1.4.4	1.4.497 dcm_diag_pkposglobal_roi1_6 0xA0039088												
Global pk positions for first ROI													
bits	name	s/w	h/w	default		description	า						
31:0	1												

1.4.4	98 dcm_diag_pkpos	Reg.	0xA003908C								
Global pk positions for first ROI											
bits	name	s/w	h/w	default		description	n				
31:0 dcm_diag_pkposg ro wo X Global pk positions for first ROI lobal_roi1_7											

1.4.4	99 dcm_diag_pkpos	Reg.	0xA0039090								
Global pk positions for first ROI											
bits	name	s/w	h/w	default		description	n				
31:0 dcm_diag_pkposg ro wo X Global pk positions for first ROI lobal_roi1_8											

1.4.5	00 dcm_diag_pkpos	Reg.	0xA0039094										
Globa	Global pk positions for first ROI												
bits	name	s/w	h/w	default		description	1						
31:0													

1.4.5	01 dcm_diag_pkpo	Reg.	0xA0039098									
Global pk positions for first ROI												
bits	name	s/w	h/w	default		description	า					
31:0 dcm_diag_pkposg ro wo X Global pk positions for first ROI lobal_roi1_10												

1.4.5	02 dcm_diag_pkpos	Reg.	0xA003909C										
Global pk positions for first ROI													
bits	name	s/w	h/w	default		description	n						
31:0	· · · · · · · · · · · · · · · · · · ·												

	al pk positions for first RO	l					
bits 31:0	name dcm_diag_pkposg	s/w ro	h/w wo	X	default	des Global pk positions for first	scription ROI
71.0	lobal_roi1_12	10	WO			Global prepositions for mot	
1.4.5	04 dcm_diag_pkpos	sglob	al_ro	i1_	13	Reg.	0xA00390A4
Glob	al pk positions for first RO	I					
bits	name	s/w	h/w		default		scription
31:0	dcm_diag_pkposg lobal_roi1_13	ro	WO	X		Global pk positions for first	ROI
1.4.5	05 dcm_diag_pkpos	sglob	al_ro	i1_	14	Reg.	0xA00390A8
Glob	al pk positions for first RO	I					
bits	name	s/w	h/w		default		scription
31:0	dcm_diag_pkposg lobal_roi1_14	ro	WO	X		Global pk positions for first	ROI
1 4 5	06 dcm_diag_pkpos	saloh	al ro	i1	15	Reg.	0xA00390AC
	• • • • • • • • • • • • • • • • • • • •		ai_i	''-	.10	-	0,11,10,000,110
	al pk positions for first RO						
bits	name	s/w	h/w		default	des	scription
	dem diag pkposg	ro	WO	X		Global pk positions for first	•
31:0	dcm_diag_pkposg lobal_roi1_15	ro	wo	X		Global pk positions for first	•
		ro	WO	Х		Global pk positions for first	•
31:0					16	Global pk positions for first	•
31:0 1.4.5	lobal_roi1_15	sglob			16		ROİ
31:0 1.4.5	lobal_roi1_15	sglob			16 default	Reg.	ROİ
31:0 1.4.5 Glob	lobal_roi1_15  07 dcm_diag_pkpos al pk positions for first RO	sglob	al_ro			Reg.	0xA00390B0
31:0 1.4.5 Glob bits	lobal_roi1_15  07 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg	sgloba	al_ro	i1_		Reg.	0xA00390B0
31:0 1.4.5 Glob bits 31:0	lobal_roi1_15  07 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16	sgloba I s/w ro	h/w wo	i1_ X	default	de: Global pk positions for first	0xA00390B0
31:0 1.4.5 Glob bits 31:0	lobal_roi1_15  07 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16  08 dcm_diag_pkpos	sgloba s/w ro	h/w wo	i1_ X	default	Reg.	0xA00390B0 scription ROI
31:0 1.4.5 Glob bits 31:0	lobal_roi1_15  07 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16  08 dcm_diag_pkpos al pk positions for first RO	sgloba I s/w ro	h/w wo	i1_ X	default	de: Global pk positions for first	0xA00390B0 scription ROI  0xA00390B4
31:0 1.4.5 Glob bits 31:0	lobal_roi1_15  07 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16  08 dcm_diag_pkpos	sgloba s/w ro	h/w wo	i1_ X	default	de: Global pk positions for first	0xA00390B0 scription ROI  0xA00390B4 scription
11.4.5 Glob bits 31:0	lobal_roi1_15  O7 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16  O8 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg	sglobal s/w ro	h/w wo	i1_ x	default	de:  Global pk positions for first	0xA00390B0 scription ROI  0xA00390B4 scription
11.4.5 Glob bits 31:0 Glob bits 31:0	lobal_roi1_15  O7 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16  O8 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg	sgloba I s/w ro	h/w wo	i1_ x	default	de:  Global pk positions for first	0xA00390B0 scription ROI  0xA00390B4 scription
11.4.5 Glob bits 31:0 11.4.5 Glob bits 31:0	lobal_roi1_15  107 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16  108 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_17	sglobal s/w ro	h/w wo	i1_ x	default	de: Global pk positions for first  de: Global pk positions for first	0xA00390B0 scription ROI  0xA00390B4 scription ROI
11.4.5 Glob bits 31:0 11.4.5 Glob bits 31:0	lobal_roi1_15  107 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_16  108 dcm_diag_pkpos al pk positions for first RO name dcm_diag_pkposg lobal_roi1_17	sglobal s/w ro	h/w wo	i1_ x	default	de: Global pk positions for first  de: Global pk positions for first	0xA00390B0 scription ROI  0xA00390B4 scription ROI

bits

1.4.510 dcm\_diag\_pkposglobal\_roi1\_19

s/w h/w

Global pk positions for first ROI

name

default

0xA00390BC

Reg.

description

31:0	dcm_diag_pkposg lobal_roi1_19	ro	wo	X		Global pk position	ns for first RO	
4.4.5	44 1 11 1				20		Pag	04.0020000
1.4.5	11 dcm_diag_pkpos	sgloba	al_ro	11_	20		Reg.	0xA00390C0
	al pk positions for first ROI							
bits 31:0	name dcm_diag_pkposg	s/w ro	h/w wo	X	default	Global pk position	descri	•
31.0	lobal_roi1_20	10	WO	^		Global pk position	15 101 11151 110	1
1.4.5	12 dcm_diag_pkpos	sgloba	al_ro	i1_	21		Reg.	0xA00390C4
Globa	al pk positions for first ROI	l						
bits	name	s/w	h/w		default		descri	
31:0	dcm_diag_pkposg lobal_roi1_21	ro	WO	X		Global pk position	ns for first RO	
1.4.5	13 dcm_diag_pkpos	globa	al_ro	i1_	22		Reg.	0xA00390C8
Globa	al pk positions for first ROI	<u> </u>						
bits	name	s/w	h/w		default		descri	ption
31:0	dcm_diag_pkposg lobal_roi1_22	ro	WO	X		Global pk position		
1 1 5	14 dam diag nknas	alab	al ro	1	22		Reg.	0xA00390CC
	14 dcm_diag_pkpos		al_lO	''-	.23			0x40003000
	al pk positions for first ROI							
bits 31:0	name dcm_diag_pkposg	s/w ro	h/w wo	Х	default	Global pk position	descri	•
31.0	lobal_roi1_23	10	WO			Global pk position	13 101 11131 110	
1 4 5	15 dcm_diag_pkpos	aloha	al ro	1	24		Reg.	0xA00390D0
	• • • • • • • • • • • • • • • • • • • •		ai_i	''-	,2-7			0,0 10000000
	al pk positions for first ROI		. ,					
bits 31:0	name dcm_diag_pkposg	s/w ro	h/w wo	X	default	Global pk position	descri	
01.0	lobal_roi1_24	10	***			Clobal ph pooliio	10 101 11101 110	
1.4.5	16 region_9_end_ta	g					Reg.	0xA00390D4
regio	n_9_end_tag							
bits	name	s/w	h/w		default		descri	ption
31:0	region_9_end_ta g	ro	WO	X		region_9_end_tag	g	
1.4.5	17 region_10_start_	tag					Reg.	0xA003A000
regio	n_10_start_tag							
bits	name	s/w	h/w		default		descri	ption
31:0	region_10_start	ro	wo	X		region_10_start_t	tag	
	_tag							

1.4.518 region\_10\_dtec\_tod\_lsbs

0xA003A004

region	region_10_dtec_tod_lsbs										
bits	name	s/w	h/w	default	description						
31:0	region_10_dtec_ tod_lsbs	ro	WO	Х	region_10_dtec_tod_lsbs						

1.4.5	19 region_10_dtec_t	Reg.	0xA003A008									
region	region_10_dtec_tod_msbs											
bits	name	s/w	h/w	default		description	n					
31:0	31:0 region_10_dtec_ ro wo X region_10_dtec_tod_msbs											

1.4.5	20 region_10_dtec_l	Reg.	0xA003A00C								
regio	region_10_dtec_lts										
bits	name	s/w	h/w	default		description	1				
31:0	region_10_dtec_ lts	ro	WO	X	region_10_dtec_lt	S					

1.4.5 abel2	1.4.521 clustering_dcm_diag_pkval_median_updated_l 0xA003A010 abel2												
Media	Median of PkVal for label2												
bits	name	s/w	h/w	def	ault		description	า					
31:0	clustering_dcm_ diag_pkval_medi an_updated_labe l2	ro											

1.4.5 12	1.4.522 clustering_dcm_diag_pkval_std_updated_labe 0xA003A014												
std of	std of PkVal for label2												
bits	name	s/w	h/w	default		description	า						
31:0 clustering_dcm_ ro wo X std of PkVal for label2 diag_pkval_std_ updated_label2													

1.4.52 abel3	23 clustering_dcm_o	Reg.	0xA003A018										
Media	Median of PkVal for label3												
bits	name	s/w	h/w	default		description	า						
31:0	clustering_dcm_ diag_pkval_medi an_updated_labe l3	ro	WO	X	Median of PkVal for label3								

1.4.5 I3	1.4.524 clustering_dcm_diag_pkval_std_updated_labe 0xA003A01C											
std of	std of PkVal for label3											
bits	name	s/w	h/w	default		description	า					
31:0	clustering_dcm_ diag_pkval_std_ updated_label3	ro	WO	Х	std of PkVal for label3							

	1.4.525 clustering_dcm_diag_pkwidth_median_updated 0xA003A020 _label2											
Media	Median of pkWidth for label2											
bits	name	s/w	h/w		default		description	า				
31:0	clustering_dcm_ diag_pkwidth_me dian_updated_la bel2	ro	WO	X		Median of pkWidt	h for label2					

1.4.5 bel2	1.4.526 clustering_dcm_diag_pkwidth_std_updated_la 0xA003A024 bel2												
std of	std of pkWidth for label2												
bits	name	s/w	h/w		default		description	1					
31:0	clustering_dcm_ diag_pkwidth_st d_updated_label 2	ro	WO	X		std of pkWidth for label2							

	1.4.527 clustering_dcm_diag_pkwidth_median_updated 0xA003A028 _label3											
Media	Median of pkWidth for label3											
bits	name	s/w	h/w		default		description	า				
31:0	clustering_dcm_ diag_pkwidth_me dian_updated_la bel3	ro	WO	X		Median of pkWidt	h for label3					

1.4.528 clustering_dcm_diag_pkwidth_std_updated_la													
std of	std of pkWidth for label3												
bits	name	s/w	h/w	C	default		description	า					
31:0	clustering_dcm_ diag_pkwidth_st d_updated_label 3	ro	WO	X		std of pkWidth for	label3						

1.4.5	29 clustering_dcm_	diag_	mall	Reg.	0xA003A030							
the ra	the rate for small (breakup) droplets shall be used as one of the criteria for square uptime acceptance / rejection											
bits	name	s/w	h/w		default		description	า				
31:0	clustering_dcm_ diag_satrate_dc m_small	ro	WO	X			he rate for small (breakup) droplets shall be used as one he criteria for square uptime acceptance / rejection					

1.4.5 d	1.4.530 clustering_dcm_diag_noise_level_updated_st												
Upda	Updated noise level (at output of clustering algo)												
bits	name	s/w	h/w	default		description	า						
31:0 clustering_dcm_ ro wo X Updated noise level (at output of clustering algo) diag_noise_leve l_updated_std													

1.4.5	31 clustering_dcm_	1	Reg.		0xA003A038						
Sigma of XInt											
bits	name	s/w	h/w		default		des	criptio	n		
31:0	clustering_dcm_ diag_jitter_dcm main	ro	WO	X		Sigma of XInt					

1.4.5	32 clustering_dcm_	diag_	cl_a	Reg.	0xA003A03C						
std of A											
bits	name	s/w	h/w		default		description	n			
31:0	clustering_dcm_ diag_jitter_dcm _subcl_a	ro	wo	X		std of A					

1.4.533 clustering_dcm_diag_jitter_dcm_presubcl												
std of	std of C											
bits	name	s/w	h/w	default	description							
31:0	clustering_dcm_ diag_jitter_dcm _presubcl	ro	WO	X	std of C							

1.4.5	34 clustering_dcm_	diag_		Reg.	0xA003A044						
Peak saturation rate for main droplets. Saturation is defined as if peak amplitude of main droplet exceed THR.  bits name s/w h/w default description											
bits	name	description	ı								
31:0	clustering_dcm_ diag_pksaturate rate	ro	WO	X	Peak saturation ra as if peak amplitu		ets. Saturation is defined to exceed THR.				

1.4.5	35 clustering_dcm_	Reg.	0xA003A048									
Peak	Peak oscillation level for main droplets, i.e. std of the peak amplitude for main droplets.											
bits	name	s/w	h/w		default		description	า				
31:0	clustering_dcm_ diag_pkoscileve I	ro	wo	X			description ak oscillation level for main droplets, i.e. std of the p plitude for main droplets.					

1.4.5	36 clustering_dcm_	Reg.	0xA003A04C									
Signa	Signal level for main / subCL / preSubCL droplets											
bits	name	s/w	h/w		default		description	n				
31:0	clustering_dcm_ diag_siglevel_p resubcl	ro	Signal level for ma	ain / subCL / preS	SubCL droplets							

1.4.5	37 clustering_dcm_	Reg.	0xA003A050								
Base	Baseline mean										
bits	name	s/w	h/w	default		descriptio	n				
31:0	clustering_dcm_ diag_bl_mean										

1.4.53 abel1	38 clustering_dcm_	Reg.	0xA003A054								
Media	Median of PkVal for label1										
bits	name	s/w	h/w	default		description	1				
31:0	clustering_dcm_ diag_pkval_medi an_updated_labe I1	ro	WO	X	Median of PkVal f	or label1					

	.4.539 clustering_dcm_diag_pkwidth_median_updated   Reg.   0xA003A058   label1											
Media	Median of pkWidth for label1											
bits	name	s/w	h/w		default		description	า				
31:0	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7											

	.4.540 clustering_dcm_diag_pkwidth_median_updated label0 0xA003A05C									
	Median of pkWidth for label0									
bits	name	s/w	h/w		default		descriptior	า		
31:0	clustering_dcm_ diag_pkwidth_me dian_updated_la bel0	ro	wo	Х		Median of pkWidtl	n for label0			

1.4.5	41 clustering_ddm_	Reg.	0xA003A060								
Base	Baseline mean										
bits	name	s/w	h/w	default		description	า				
31:0	clustering_ddm_ diag_bl_mean	Baseline mean									

1.4.5 <sup>a</sup>	42 clustering_ddm_ 3	Reg.	0xA003A064									
	Median of PkVal for label3											
bits	name	s/w	h/w	default		description	)					
	clustering_ddm_ diag_pkval_medi an_updated_labe l3	ro	WO	X	Median of PkVal f	or label3						

1.4.5 13	1.4.543 clustering_ddm_diag_pkval_std_updated_labe 0xA003A068										
std of	std of PkVal for label3										
bits	name	s/w	h/w	default		description	า				
31:0 clustering_ddm_ ro wo X std of PkVal for label3 diag_pkval_std_ updated_label3											

	1.4.544 clustering_ddm_diag_pkwidth_median_updated 0xA003A06C										
Media	Median of pkWidth for label3										
bits	name	s/w	h/w	default		description	1				
31:0	clustering_ddm_ diag_pkwidth_me dian_updated_la bel3	ro	WO	X	Median of pkWidtl	n for label3					

1.4.5 bel3	1.4.545 clustering_ddm_diag_pkwidth_std_updated_la 0xA003A070 oxA003A070											
std of	std of pkWidth for label3											
bits	name	s/w	h/w		default		description	٦				
31:0	clustering_ddm_ diag_pkwidth_st d_updated_label 3	ro	WO	X		std of pkWidth for	label3					

1.4.5	46 clustering_ddm	0xA003A074				
	ther with cross interval s ent setting to inline tuning	lite rate should be used to provide primary focus metrics for cate				
bits	name	s/w	h/w		default	description
31:0	clustering_ddm_	ro	wo	Х		Together with cross interval standard derivation, the satellite

1.4.5 d	.4.547 clustering_ddm_diag_noise_level_updated_st 0xA003A078										
Upda	Updated noise level (at output of clustering algo)										
bits	name	s/w	h/w	default	descr	iption					
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1										

1.4.5	1.4.548 clustering_ddm_diag_pksaturaterate 0xA003A07C												
Peak saturation rate for main droplets. Saturation is defined as if peak amplitude of main droplet exceed THR.													
bits	name	s/w	h/w		default		description	า					
31:0	clustering_ddm_ diag_pksaturate rate	Peak saturation ra as if peak amplitue		ets. Saturation is defined t exceed THR.									

1.4.549 clustering_ddm_diag_pkoscilevel 0xA003A080											
Peak oscillation level for main droplets, i.e. std of the peak amplitude for main droplets.											
bits	name	s/w	h/w	default	descriptio	n					
31:0 clustering_ddm_ ro wo X Peak oscillation level for main droplets, i.e. std of the diag_pkoscileve amplitude for main droplets.											

1.4.5	50 region_10_end	Reg.	0xA003A084									
region_10_end_tag												
bits	name	s/w	h/w		default		description	on				
31:0 region_10_end_t ro wo X region_10_end_tag												

1.4.5	51 region_12_start_	Reg.	0xA003C000								
region_12_start_tag											
bits	name	s/w	h/w	default		description	ı				
31:0 region_12_start ro wo X region_12_start_tag											

1.4.5	52 region_12_dtec_	Reg.	0xA003C004								
region_12_dtec_tod_lsbs											
bits	name	s/w	h/w	default		description	n				
31:0 region_12_dtec_ ro wo X region_12_dtec_tod_lsbs tod_lsbs											

1.4.5	53 region_12_dtec_	Reg.	0xA003C008								
region_12_dtec_tod_msbs											
bits	name	s/w	h/w	default		description	n				
31:0 region_12_dtec_ ro wo X region_12_dtec_tod_msbs											

1.4.5	54 region_12_dtec_l	Reg.	0xA003C00C								
region_12_dtec_lts											
bits	name	s/w	h/w	default		description	า				
31:0	region_12_dtec_ lts	region_12_dtec_li	ts								

1.4.5	55 idcb_triggers_idd		Reg.	0xA003C010								
IDCB trigger for ch1												
bits	name	s/w	h/w	default		description	٦					
31:0	31:0 idcb_triggers_i ro wo X IDCB trigger for ch1 dcb_trigger_ch1											

1.4.556 idcb_triggers_idcb_trigger_ch2 0xA003C014												
IDCB trigger for ch2												
bits	name	s/w	h/w	default		description	١					
31:0	· ·											

1.4.5	1.4.557 idcb_triggers_idcb_trigger_ch7 0xA003C018											
IDCB trigger for ch7												
bits	name	s/w	h/w	default		description	n					
31:0 idcb_triggers_i ro wo X IDCB trigger for ch7 dcb_trigger_ch7												

1.4.5	1.4.558 idcb_triggers_idcb_trigger_ch9 0xA003C01C											
IDCB trigger for ch9												
bits	name	s/w	h/w	default		description	١					
31:0	31:0 idcb_triggers_i ro wo X IDCB trigger for ch9 dcb_trigger_ch9											

1.4.5	59 idcb_triggers_idd	Reg.	0xA003C020									
IDCB trigger for ch10												
bits	name	s/w	h/w		default		descriptio	n				
31:0	idcb_triggers_i dcb_trigger_ch1 0	ro	WO	X		IDCB trigger for ch10						

1.4.5	60 idcb_triggers_idd		Reg.	0xA003C024						
IDCB trigger for ch12										
bits	name		description							
31:0	idcb_triggers_i dcb_trigger_ch1 2	ro	wo	X	IDCB trigger for ch12					

1.4.5	61 region_12_end_t	Reg.	0xA003C028							
region_12_end_tag										
bits	name	s/w	h/w	default		descriptio	n			
31:0	region_12_end_t ag	ro	WO	X	region_12_end_ta	ag				

1.4.5	62 region_13_start_	Reg.	0xA003D000							
region_13_start_tag										
bits	name	s/w	h/w	default		description	n			
31:0	region_13_start _tag	ro	WO	Х	region_13_start_t	ag				

1.4.5	63 region_13_dtec_t	Reg.	0xA003D004							
region_13_dtec_tod_lsbs										
bits	name	s/w	h/w	default		description	n			
31:0 region_13_dtec_ ro wo X region_13_dtec_tod_lsbs tod_lsbs										

1.4.5	64 region_13_dtec_t	Reg.	0xA003D008							
region_13_dtec_tod_msbs										
bits	name	s/w	h/w	default		description	٦			
31:0	31:0 region_13_dtec_ ro wo X region_13_dtec_tod_msbs tod_msbs									

1.4.565 region_13_dtec_lts	Reg.	0xA003D00C
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region_13_dtec_lts										
bits	name	s/w	h/w	default	description					
31:0	region_13_dtec_ lts	ro	WO	X	region_13_dtec_lts					

1.4.5	66 state_duplicate4	Reg.	0xA003D010							
Readback of diagnostics signature for monitor algo block										
bits	name	s/w	h/w	default		description	n			
31:0	state_duplicate 4reg13	ro	WO	X	Readback of diagnostics signature for monitor algo block					

1.4.5	67 cal_lf_basedrops	Reg.	0xA003D014							
Setting being tested during Base Droplet Optimization										
bits	name	s/w	h/w	default		description	٦			
31:0	cal_lf_basedrop setting	ro	WO	X	Setting being tested during Base Droplet Optimization					

1.4.5	68 cal_lf_basedropi	Reg.	0xA003D018							
Iteration of current Setting being tested during Base Droplet Optimization										
bits	name	s/w	h/w	default		description	า			
31:0	cal_lf_basedrop iteration	ro	WO	X	Iteration of current Optimization	ent Setting being tested during Base Drople				

1.4.5	69 cal_lf_costfunco	Reg.	0xA003D01C							
Setting being tested during Cost Function Optimization										
bits	name	s/w	h/w	default		description	n			
31:0	cal_lf_costfunc optsetting	ro	wo	X	Setting being test	ed during Cost Fu	unction Optimization			

1.4.5	70 cal_lf_costfuncit	Reg.	0xA003D020								
Iteration of current Setting being tested during Cost Function optimization											
bits	name	s/w	h/w	default		description	ı				
31:0	cal_lf_costfunc iteration	ro	wo	X	Iteration of current Setting being tested during Cost Function optimization						

1.4.5	71 cal_lf_stateupdat	Reg.	0xA003D024								
Flag that indicates when a calibration state is done											
bits	name	s/w	h/w	default		description	า				
31:0	cal_lf_stateupd ate	ro	wo	X	Flag that indicates when a calibration state is done						

1.4.5	72 cal_lf_spare5	Reg.	0xA003D028							
Calibration Spare Signal										
bits	bits name s/w h/w default description									
31:0	cal_lf_spare5	ro	wo	Χ		Calibration Spare	Signal			

1.4.573 cal_lf_spare6						Reg.	0xA003D02C
Calibration Spare Signal							
bits name	s/w	h/w		default		descripti	on
31:0 cal_lf_spare6	ro	WO	Χ		Calibration Spare	Signal	
1.4.574 cal_lf_spare7						Reg.	0xA003D030
Calibration Spare Signal							
bits name	s/w	h/w		default		descripti	on
31:0 cal_lf_spare7	ro	WO	X		Calibration Spare	Signal	
1.4.575 cal_lf_spare8						Reg.	0xA003D034
Calibration Spare Signal							
bits name	s/w	h/w		default		descripti	on
31:0 cal_lf_spare8	ro	WO	Χ		Calibration Spare	Signal	
1.4.576 cal_lf_spare9						Reg.	0xA003D038
Calibration Spare Signal							
bits name	s/w	h/w		default		descripti	on
31:0 cal_lf_spare9	ro	WO	X		Calibration Spare	Signal	
1.4.577 cal_hf_du						Reg.	0xA003D03C
Sine fit signal DU							
bits name	s/w	h/w		default		descripti	on
31:0 cal_hf_du	ro	wo	X		Sine fit signal DU		
1.4.578 cal_hf_alpha1						Reg.	0xA003D040
Sine Fit metrics alpha1							
bits name	s/w	h/w		default		descripti	on
31:0 cal_hf_alpha1	ro	WO	Χ		Sine Fit metrics a	lpha1	
1.4.579 cal_hf_alpha2						Reg.	0xA003D044
Sine fit metrics alpha2							
bits name	s/w	h/w		default		descripti	on
31:0 cal_hf_alpha2	ro	wo	Χ		Sine fit metrics al	oha2	
1.4.580 cal_hf_alpha0						Reg.	0xA003D048
Sine Fit signal alpha0							
bits name	s/w	h/w		default		descripti	on
31:0 cal_hf_alpha0	ro	WO	Χ		Sine Fit signal alp	ha0	
1.4.581 cal_hf_beta						Reg.	0xA003D04C
sine fit signal beta							
bits name	s/w	h/w		default		descripti	on
31:0 cal_hf_beta	ro	wo	X		sine fit signal beta	1	

	582 cal_hf_clockcor	rectio	ntact	or			Reg.	0xA003D050
Sine	Fit Algo clockCorrectionFa	actor						
bits	name	s/w	h/w		default		desc	ription
31:0	cal_hf_clockcor rectionfactor	ro	WO	X		SineFit Algo clock	CorrectionF	Factor
.4.5	i83 cal_hf_spare1						Reg.	0xA003D054
Calik	oration Spare Signal							
bits	name	s/w	h/w		default		desc	cription
31:0	cal_hf_spare1	ro	WO	X		Calibration Spare		
1.4.5	684 cal_hf_spare2						Reg.	0xA003D058
Calik	oration Spare Signal							
bits	name	s/w	h/w		default			ription
31:0	cal_hf_spare2	ro	WO	X		Calibration Spare	Signal	
1.4.5	i85 cal_hf_spare3						Reg.	0xA003D05C
Calib	oration Spare Signal							
bits	name	s/w	h/w		default		desc	ription
31:0	cal_hf_spare3	ro	WO	Χ		Calibration Spare	Signal	
1.4.5	i86 cal_hf_spare4						Reg.	0xA003D060
Calib	oration Spare Signal							
bits	name	s/w	h/w		default		desc	ription
31:0	cal_hf_spare4	ro	WO	X		Calibration Spare	Signal	
	i87 clustering_dcm <sub>_</sub> 3_duplicate4reg13	_diag_	pkva	l_r	nedian_	updated_I	Reg.	0xA003D064
Med	ian of PkVal for label3							
bits		s/w	h/w		default			cription
31:0	clustering_dcm_ diag_pkval_medi an_updated_labe l3_duplicate4re g13	ro	WO	X		Median of PkVal fo	or label3	
	i88 clustering_dcm_ el3_duplicate4reg13	_	pkwi	ath	n_media	n_updated	Reg.	0xA003D068
	ian of pkWidth for label3							
Med		0/11	h/w		default		desc	cription
	name clustering_dcm_	s/w ro	wo	Χ		Median of pkWidth		

1.4.589 clustering_dcm_diag_noise_level_updated_st d_duplicate4reg13													
Upda	Updated noise level (at output of clustering algo)												
bits	name	s/w	h/w	default		description	1						
31:0	clustering_dcm_ diag_noise_leve l_updated_std_d uplicate4reg13	ro	WO	X	Jpdated noise level (at output of clustering algo)								

abel3	1.4.590 clustering_ddm_diag_pkval_median_updated_l abel3_duplicate4reg13  Median of PkVal for label3											
bits 31:0	bits name s/w h/w default description 31:0 clustering_ddm_ ro wo X Median of PkVal for label3											
	diag_pkval_medi an_updated_labe l3_duplicate4re g13											

1.4.59 _labe	0xA003D074										
Median of pkWidth for label3											
bits	name	s/w	h/w	default		description	١				
31:0	clustering_ddm_ diag_pkwidth_me dian_updated_la bel3_duplicate4 reg13	ro	WO	X	Median of pkWidth for label3						

	92 clustering_ddm_ plicate4reg13	0xA003D078											
	Updated noise level (at output of clustering algo)												
bits	name	s/w	h/w	default		description	า						
31:0	clustering_ddm_ diag_noise_leve l_updated_std_d uplicate4reg13	ro	WO	X	Updated noise level (at output of clustering algo)								

1.4.5	93 region_13_end_t	Reg.	0xA003D07C							
region_13_end_tag										
bits	name	s/w	h/w	default		description	n			
31:0	region_13_end_t ag	ro	WO	X	region_13_end_ta	ag				

1.5 algo_csr_registers_srdl	Block  □ T	0xA0050000 - 0xA0050173
Register map of the Algo Control and Status registers		

1.5.1	algo_csr_module_ı	Reg.	0xA0050000							
Defines the module name										
bits name s/w h/w default description										

1.5.2	algo_csr_module_v	Reg.	0xA0050004								
Module version											
bits	name	s/w	h/w	default		description					
31:16	rfu	ro	na	0x521	Algo IO Date						
15:8	major_revision	Memory Map num	Map number - Decimal - Thousands/Hundreds								
7:0	minor_revision	ro	na	0x20	Memoru Mao nun	nber - Decimal - T	Tens/Ones				

1.5.3	algo_csr_page_pro	opertie	0xA0050008							
Addre	Address page properties									
bits	name	description								
31	present	ro	WO	0x1	Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not.					
30:16	rfu	ro	na	0x0	Reserver for Future Use - RFU					
15:8	page_size	ro	na	0x1	Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enetr here.					
7:0	unified_header_ rev	ro	na	0x1	Unified Header Format common registers revision.					

1.5.4	algo_csr_scratchre	Reg.	0xA005000C									
Scrat	Scratchregister register											
bits	bits name s/w h/w default description											
31:0	scratchregister	e to it and read from it for test purposes.										

1.5.5	algo_csr_irq_enabl	Reg.	0xA0050010							
Interrupt Requests Enable/Mask Control Register										
bits	name	s/w	h/w	default		description				
0	irq0_enable	rw	ro	0x0	IRQ0 enable bit. Not implemented here/DTEC					
1	irq1_enable	rw	ro	0x0	IRQ1 enable bit.	Not implemented I	here/DTEC			

1.5.6	algo_csr_irq_pend		Reg.	0xA0050014					
Interrupt Pending Status Register									
bits	name	s/w	h/w	default	description				
0	irq0_pending	r/w1c	wo	0x0	IRQ0 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC				
1	irq1_pending	r/w1c	wo	IRQ1 pending status bit, sticky bit. Write '1' to clear. Asserts interrupt on positive edge. Not implemented here/DTEC					

1.5.7	algo_csr_irq_raw	Reg.	0xA0050018								
Interr	Interrupt Raw Status Register										
bits	name	s/w	h/w	default		description	n				
0	irq0_raw	ro	wo	0x0	IRQ0 raw status b	it. Not implement	ed here/DTEC				
1	irq1_raw	ro	wo	0x0	IRQ1 raw status b	oit. Not implement	ted here/DTEC				

1.5.8 algo_csr_irq_force	Reg.	0xA005001C
Interrupt Force Control Register		

bits	name	s/w	h/w	default	description
0	irq0_force	rw	ro	0x0	IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC
1	irq1_force	rw	ro	0x0	IRQ1 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not implemented here/DTEC

1.5.9	dcm_status_reg			Reg.	0xA0050020					
Algo	Algo Buffer Status Register									
bits	name		description							
31:0	status_reg	ro	WO	0x0	[31:4]: unused [3]: CRC Error [2]: FIFO Not Ready [1]: FSM Watchdog [0]: Packet Length Error					

1.5.1	0 ddm_status_reg		Reg.	0xA0050024						
Algo	Algo Buffer Status Register									
bits	bits name s/w h/w default description									
31:0	status_reg	ro	wo	0x0	[31:4]: unused [3]: CRC Error [2]: FIFO Not Ready [1]: FSM Watchdog [0]: Packet Length Error					

1.5.1	1 ch3_xfer_count	Reg.	0xA0050100								
Coun	Count of how many sets of DMA data have been loaded into the FIFO										
bits	name	s/w	h/w	default	description						
31:0	counter	ro	wo	0x0	Count						

1.5.12	2 ch3_drop_count	Reg.	0xA0050104							
Count of how many sets of DMA data have been dropped due to non-empty FIFO										
bits	name	s/w	h/w	default		description				
31:0	counter	ro	wo	0x0	Count					

1.5.1	3 ch4_xfer_count	Reg.	0xA0050108						
Count of how many sets of DMA data have been loaded into the FIFO									
bits	name	s/w h	n/w	default	description				
31:0	counter	ro \	wo	0x0	Count				

1.5.1	4 ch4_drop_count	Reg.	0xA005010C							
Count of how many sets of DMA data have been dropped due to non-empty FIFO										
bits	name	s/w	h/w	default		description				
31:0	counter	ro	wo	0x0	Count					

1.5.1	5 ch5_xfer_count	Reg.	0xA0050110							
Count of how many sets of DMA data have been loaded into the FIFO										
bits	name	s/w	h/w	default	description					
31:0	counter	ro	wo	0x0	Count					

		drop_count	A -1-4-	L L		-l t	Reg.	
	it of now	many sets of DM				due to non-em		andre til and
bits 31:0	counter	name	s/w ro	h/w wo	default 0x0	Count	des	cription
71.0	countor		10	***	OXO	Oddin		
1.5.1	7 ch6_	xfer_count					Reg.	0xA0050118
Coun	t of how	many sets of DM	A data	have b	oeen loaded ir	nto the FIFO		
bits		name	s/w	h/w	default		des	cription
31:0	counter		ro	WO	0x0	Count		
1.5.1	8 ch6_	drop_count					Reg.	0xA005011C
Coun	t of how	many sets of DM	A data	have b	peen dropped	due to non-em	pty FIFO	
bits		name	s/w	h/w	default			cription
31:0	counter		ro	wo	0x0	Count		
1.5.1	9 ch7_	xfer_count					Reg.	0xA0050120
	t of how	many sets of DM				nto the FIFO		
bits 31:0	counter	name	s/w ro	h/w wo	default 0x0	Count	des	cription
1 5 2	0 ah7	drop coupt					Reg.	0×40050124
Coun		drop_count many sets of DM				due to non-em	-	0xA0050124
Coun	t of how	• -	s/w	h/w	default		pty FIFO	0xA0050124
Coun		many sets of DM				due to non-em	pty FIFO	
Coun bits 31:0	t of how counter	many sets of DM	s/w	h/w	default		pty FIFO	
Cound bits 31:0	counter	many sets of DM.	s/w ro	h/w wo	default 0x0	Count	pty FIFO des	cription
bits 31:0  1.5.2  Cound bits	counter  1 ch8_ at of how	many sets of DM. name  xfer_count	s/w ro A data s/w	h/w wo have t	default 0x0  Deen loaded in default	Count  nto the FIFO	pty FIFO des	cription
bits 31:0  1.5.2  Cound bits	counter	many sets of DM.  name   xfer_count  many sets of DM.	s/w ro	h/w wo	default 0x0	Count	pty FIFO des	cription  0xA0050128
Counbits 31:0  1.5.2  Counbits 31:0	counter  1 ch8_2  at of how  counter	many sets of DM.  name   xfer_count  many sets of DM.	s/w ro A data s/w	h/w wo have t	default 0x0  Deen loaded in default	Count  nto the FIFO	pty FIFO des	cription  0xA0050128
Cound bits 31:0 Cound bits 31:0	counter  1 ch8_x at of how counter	many sets of DM. name  xfer_count many sets of DM. name	s/w ro A data s/w ro	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0	Count  nto the FIFO  Count	epty FIFO des	cription  0xA0050128  cription
Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0	counter  1 ch8_; at of how counter  2 ch8_at of how	many sets of DM. name  xfer_count many sets of DM. name	s/w ro A data s/w ro	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0  Deen dropped default	Count  To the FIFO  Count  due to non-em	pty FIFO des	cription  0xA0050128  cription
Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0	counter  1 ch8_x at of how counter	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM.	s/w ro  A data s/w ro	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0	Count  nto the FIFO  Count	pty FIFO des	oxA0050128 cription 0xA005012C
Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0	counter  1 ch8_; at of how counter  2 ch8_at of how	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM.	s/w ro  A data s/w ro  A data	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0  Deen dropped default	Count  To the FIFO  Count  due to non-em	pty FIFO des	oxA0050128 cription 0xA005012C
Cound bits 31:0  1.5.2  Cound bits 31:0  Cound bits 31:0	counter  1 ch8_ at of how counter  2 ch8_ at of how counter	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM.	s/w ro  A data s/w ro  A data	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0  Deen dropped default	Count  To the FIFO  Count  due to non-em	pty FIFO des	oxA0050128 cription 0xA005012C
Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0	counter  1 ch8_2 at of how counter  2 ch8_at of how counter  3 ch9_2	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM. name	s/w ro  A data s/w ro  A data s/w ro	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0  Deen dropped default 0x0	Count  Count  Count  Count	ppty FIFO  des  Reg.  ppty FIFO  des	oxA0050128  cription  0xA005012C  cription
Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0	counter  1 ch8_ at of how counter  2 ch8_ at of how counter  3 ch9_ at of how	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM. name	s/w ro  A data s/w ro  A data s/w ro	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0  Deen dropped default 0x0  Deen loaded in default	Count  Count  Count  Count  Count	des Reg.	oxA0050128  cription  0xA005012C  cription
Cound bits 31:0 Cound bits 31:0 Cound bits 31:0 Cound bits 31:0 Cound bits 31:0 Cound bits 31:0 Cound bits 31:0	counter  1 ch8_2 at of how counter  2 ch8_at of how counter  3 ch9_2	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM. name  xfer_count many sets of DM. name	A data s/w ro  A data s/w ro	h/w wo have t h/w wo	default 0x0  Deen loaded in default 0x0  Deen dropped default 0x0	Count  Count  Count  Count	des Reg.	cription  0xA0050128  cription  0xA005012C  cription  0xA0050130
Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0	counter  1 ch8_ at of how counter  2 ch8_ at of how counter  3 ch9_ at of how	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM. name  xfer_count many sets of DM. name	A data s/w ro  A data s/w ro  A data s/w	h/w wo have the h/w wo have the	default 0x0  Deen loaded in default 0x0  Deen dropped default 0x0  Deen loaded in default	Count  Count  Count  Count  Count	des Reg.	cription  0xA0050128  cription  0xA005012C  cription  0xA0050130
Cound bits 31:0  1.5.2  Cound bits 31:0  1.5.2  Cound bits 31:0  Cound bits 31:0	counter  1 ch8_ at of how counter  2 ch8_ at of how counter  3 ch9_ at of how counter	many sets of DM. name  xfer_count many sets of DM. name  drop_count many sets of DM. name  xfer_count many sets of DM. name	A data s/w ro  A data s/w ro  A data s/w	h/w wo have the h/w wo have the	default 0x0  Deen loaded in default 0x0  Deen dropped default 0x0  Deen loaded in default	Count  Count  Count  Count  Count	des Reg.	cription  0xA0050128  cription  0xA005012C  cription  0xA0050130

31:0	rx_err_c	nt	rw	na	0x0	+1 => the fsr packet	n that recives th	e data, detected an crc erro
bits		name	s/w	h/w	default		des	cription
regist	er used t	o return the coun	t of nu	mber c	of crc error pa	ckets received		
1.5.3	2 dcm_	pkts_crc_err	_cnt				Reg.	0xA005015C
	17_UIL		10	VVO	JAU	gives tile cot	ancovery IIIISEC	,
bits ':0	rx_cnt	name	s/w ro	h/w wo	default 0x0	gives the cou	des int every 1msec	cription
	er usea t	o return the coun			•	msec ume trar		orintion
		pkts_inframe		mha= -	of packate in 4	mana tima tu-		0AA0000130
152	1 dem	nkte inframe	onf				Reg.	0xA0050158
31:0	counter		ro	wo	0x0	Count		
bits		name	s/w	h/w	default		des	cription
Coun	t of how r	many sets of DM	A data	have b	een dropped	due to non-em	pty FIFO	
1.5.3	0 algo_	to_damp_dro	op_cc	unt			Reg.	0xA0050154
31:0	counter		ro	wo	0x0	Count		
bits		name	s/w	h/w	default	-	des	cription
Coun	t of how r	many sets of DM/	A data	have b	een loaded ir	nto the FIFO		
1.5.2	9 algo_	to_damp_xfe	er_co	unt			Reg.	0xA0050150
•	, , , , , , , , , , , , , , , , , , , ,				<del>-</del>	····		
bits 31:0	counter	name	s/w ro	h/w wo	default 0x0	Count	ues	cription
	t Of HOW I	•				ade to non-en		orintion
		many sets of DM	Δ data	have b	neen dronned	due to non om		
1.5.2	8 ch12	_drop_count					Reg.	0xA0050144
31:0	counter		ro	wo	0x0	Count		
bits		name	s/w	h/w	default		des	cription
Coun	t of how r	many sets of DM/	A data	have b	een loaded ir	nto the FIFO		
1.5.2	7 ch12_	_xfer_count					Reg.	0xA0050140
31:0	counter		ro	WO	0x0	Count		
bits	001124==	name	s/w	h/w	default	Count	des	cription
Coun	t of how r	many sets of DM/	A data	have b		due to non-em		
		_drop_count					Reg.	0xA005013C
4.5.0	0 -1:40	almana a sa					Dog	0v40050430
31:0	counter		ro	WO	0x0	Count		
bits	001124==	name	s/w	h/w	default	Count	des	cription
	t of how r	many sets of DM/				nto the FIFO		
		_xfer_count					Reg.	0xA0050138
							1000	0.40050455
			10	VVO	UNU	Count		
31:0	counter		ro	wo	0x0	Count		

packet

1.5.3	3 dcm_pkts_lgth_er	Reg.	0xA0050160							
register used to return the count of number of packets received with packet length error										
bits	name	s/w	h/w	default		description	n			
31:0	rx_err_cnt	rw	na	0x0	+1 => the fsm that recives the data, detected a packet with unexpected length					

1.5.3	1.5.34 ddm_pkts_inframe_cnt 0xA0050164										
register used to return the count of number of packets in 1msec time frame											
bits	name	s/w	h/w	default	ault description						
7:0	rx_cnt	ro	wo	0x0	gives the count ev	ery 1msec					

1.5.3	1.5.35 ddm_pkts_crc_err_cnt 0xA0050168										
register used to return the count of number of crc error packets received											
bits	name	s/w	h/w	default		description	٦				
31:0	111										

1.5.3	I.5.36 ddm_pkts_lgth_err_cnt 0xA005016C										
register used to return the count of number of packets received with packet length error											
bits	name	s/w	h/w	default		description	n				
31:0	rx_err_cnt	rw	na	0x0	+1 => the fsm tha unexpected length	m that recives the data, detected a packet with length					

1.5.3	7 pulse_1ms_phase	Reg.	0xA0050170								
Phase	Phase delay the 1ms algo pulse (used for 1ms clock enable, cluster_start, channel 12 dma capture, etc).										
bits	name	s/w	h/w	default	description						
31:0	count	rw	ro	0x100	delay the 1ms alg The algo team info	nber of clocks (in 125 MHz core clock domain) to phas y the 1ms algo pulse. algo team informed that the max time that the algo s should be ~240 clock cycles.					

1.6 tsel_if_bridge_srdl	Block ■⊤	0xA0080000 - 0xA00867FF
Registers used to configure / control tsel interface		

### 

1.6.2	MODULE_VERSI	ION		Reg.	0xA0080004				
Module info register 1 - used to return module version.  Note: this register might change from build to build and might be used for future backwards compatibility									
Note	this register might cha	ange from I	build to	build and mi	ight be used for futur	e backwards o	compatibility		
Note bits	this register might change	ange from I	build to h/w	build and mi	ight be used for futur	re backwards o descript	•		

7:0 minor ro wo 0x0 Module version minor
--

1.6.3	HEADER_INFO	Reg.	8000800Ax0						
Module info register 2 - used to return module memory page size									
bits	bits name s/w h/w default						description		
15:0	block_size	ro	na	0x4	Addressable address space in 4k pages (1 = 4096 bytes / 2 = 8192)				
31:16	unified_header_ ver	/ersion of unified module memory header - used for any fuure changes to the header							

1.6.4	0xA008000C									
Module info register 3 - scratchpad register used for testing module read / write access.										
bits	name	s/w	h/w	default		description	ı			
31:0 scratchpad rw na 0x0 scratchpad register - can be read and written by software a any time										

1.6.5	IRQ_ENABLE		Reg.	0xA0080010				
_	ster used to enable individation will not change.	dual IRC	s. If de	efined bit is se	et and interrupt occi	urs, interrupt pin	will toggle, otherwise	
bits	name	s/w	h/w	default	description			
	cpu_insert_buff er_fifo_full	rw	na	0x0	IRQ enable - cpu insert buffer full.			
	cpu_insert_buff er_fifo_empty	rw	na	0x0	IRQ enable - cpu	insert buffer emp	ty.	
2	cpu_capture_buf fer_pkt_avail	rw	na	0x0	IRQ enable - cpu	capture buffer pk	t available.	
3	cpu_capture_buf fer_overflow	rw	na	0x0	IRQ enable - cpu capture buffer overflow.			
4	link_up	rw	na	0x0	IRQ enable - link	up.		
5	link_down	rw	na	0x0	IRQ enable - link	down.		

1.6.6	IRQ_PENDING	Reg.	0xA0080014							
Register used to return currently pending IRQs.										
bits name s/w h/w default description										
0	cpu_insert_buff er_fifo_full	r/w1c	wo	0x0	IRQ pending - cpu insert buffer full indication. TBD - do we want this level sensitive?					
1	cpu_insert_buff er_fifo_empty	r/w1c	wo	0x0	IRQ pending - cpu we want this level		pty indication. TBD - do			
2	cpu_capture_buf fer_pkt_avail	r/w1c	wo	0x0	IRQ pending - cpu	u capture buffer p	kt available.			
3	cpu_capture_buf fer_overflow	r/w1c	wo	0x0	IRQ pending - cpu full)	u capture buffer o	verflow (capture buffer			
4	link_up	r/w1c	wo	0x0	IRQ pending - link	c up				
5	link_down	r/w1c	wo	0x0	IRQ pending - link	k down				

1.6.7	IRQ_RAW	0xA0080018						
Register used to return current value of IRQ input signals								
bits	name	description						
0	cpu_insert_buff er_fifo_full	ro	wo	0x0	current value of - cpu insert buffer full indication.			
1	cpu_insert_buff er_fifo_empty	ro	wo	0x0	current value of - cpu insert buffer empty indication.			
2	cpu_capture_buf fer_pkt_avail	ro	wo	0x0	current value of - cpu capture buffer pkt available.			

3	cpu_capture_buf fer_overflow	ro	wo	0x0	current value of - cpu_capture_buffer_overflow.
4	link_up	ro	wo	0x0	current value of - link status (0 = down / 1 = up).
5	link down	ro	wo	0x0	current value of - link status ( $0 = down / 1 = up$ ).

## 1.6.8 IRQ\_FORCE 0xA008001C

Register used to force interrupts via software - this register is to be used for debugging interrupts only. Important, if the user goes and

manually forces an interrupt via any fields in this register (by setting a field to 1), the IRQ routine needs to clear the forced field otherwise the interrupt

will never clear and we will be stuck in an interrupt loop. Additionally, forcing an interrupt that is not enabled, will not result in interrupt pin being toggled.

bits	name	s/w	h/w	default	description
0	cpu_insert_buff er_fifo_full_fo rce	rw	na	0x0	register used to force IRQ-cpu_insert_buffer_fifo_full_force.
1	cpu_insert_buff er_fifo_empty_f orce	rw	na	0x0	register used to force IRQ-cpu_insert_buffer_fifo_empty.
2	cpu_capture_buf fer_pkt_avail_f orce	rw	na	0x0	register used to force IRQ-cpu_capture_buffer_pkt_avail.
3	cpu_capture_buf fer_overflow_fo rce	rw	na	0x0	register used to force IRQ-cpu_capture_buffer_overflow.
4	link_up_force	rw	na	0x0	register used to force IRQ-link_up
5	link_down_force	rw	na	0x0	register used to force IRQ-link_down

1.6.9	BUILD_INFO	R	eg.	0xA0080040					
regist	register used to return TSEL GDB info								
bits	name	s/w		description					
7:0	build_type	ro	TSEL build type: 0 = served	= tsel client / 1 =	tsel bridge / others - re-				
15:8	tsel_index	TSEL index - used t bridge instance num		ory map to tsel client /					

1.6.1	0 BUILD_INFO1	Reg.	0xA0080044						
register used to return TSEL Unified build info									
bits	name	s/w	h/w	default		description			
15:0	rx_stats_engine _size	ro	WO	0x0	number of entries used in rx stats engine. Only use rx_stats_engine if this field > 0				
31:16	tx_stats_engine _size	ro	WO	0x0	number of entries tx_stats_engine if		ngine. Only use		

1.6.1	1 BUILD_INFO2	0xA0080048							
register used to return TSEL Unified build info									
bits	name	description							
7:0	cpu_buf_addr_wi dth	ro	WO	0x0	address size of each CPU buffer; CPU buffer word size is 2^cpu_buf_addr_width				
15:8	cpu_buf_depth	ro	wo	0x0	number of buffers in CPU packet FIFO				
16 stats_bin_type ro wo 0x0 source used for stats binning, RX/TX_STATS_E payload type, 1 - header type									

regist	register used to control tsel gdb									
bits	name	s/w	h/w	default	description					
0	reset_force	rw	ro	0x0	field used to allow software ability to reset tsel GDB. 1=gdb reset / 0= gdb not reset					
4	tsel_client_mac _address_valid	rw	ro	0x0	field used to allow software ability to change mac address, client only. TBD - this might have to be set before core is being reset					
5	tsel_client_eth _type_valid	rw	ro	0x0	field used to allow software ability to change ethernet type.  TBD - this might have to be set before core is being reset					

1.6.1	1.6.13 TSEL_CLIENT_TX_MAC_INSERT_MSB 0xA0080064								
regist	register used to control tsel gdb mac address insertion on the way out, client only								
bits	name	s/w	h/w	default		description	า		
15:0	15:0 msb rw ro 0x1234 register used to assign mac address when external prom is not being used - bits [47:32]								

1.6.14	1.6.14 TSEL_CLIENT_TX_MAC_INSERT_LSB 0xA0080068									
regist	register used to control tsel gdb mac address insertion on the way out, client only									
bits	name	s/w	h/w	default		description	า			
31:0 lsb rw ro 0x56789ABC register used to assign mac address when external prom in not being used - bits [31:0]										

1.6.1	5 TSEL_CLIENT_TX	Reg.	0xA008006C								
regist	register used to control tsel gdb ethernet type on the way out										
bits	bits name s/w h/w default description										
15:0	insert	rw	ro	0x8000	register used to a	ssign ethernet typ	oe .				

1.6.1	6 TSEL_CLIENT_RX	Reg.	0xA0080070								
_	register used to return last packet src mac address (MSB).  Reading this register latches value in tsel_client_rx_mac_insert_lsb and tsel_client_rx_eth_type										
bits name s/w h/w default description											
15:0	msb	ro	wo	0x0	src mac address -	bits [47:32]					

1.6.1	7 TSEL_CLIENT_RX	Reg.	0xA0080074							
register used to return last packet src mac address (LSB)										
bits	bits name s/w h/w default description									
31:0	Isb	ro	wo	0x0	src mac address -	bits [31:0]				

1.6.18	1.6.18 TSEL_CLIENT_RX_SRC_ETH_TYPE 0xA0080078									
register used to return last packet ethernet type - this register is for Client TSEL GDB only										
bits	bits name s/w h/w default description									
15:0	received	ro	wo	0x0	register used to a	ssign ethernet typ	e			

1.6.1	9 CPU_INSERT_BUI	Reg.	0xA0080080									
regist	register used to control insert buffer											
bits	name	s/w	h/w	default		description	٦					
0	fifo_push	rw	ro	0x0	write 1 to perform	insert buffer push	ı					

1.6.2	0 CPU_CAPTURE_B	Reg.	0xA0080084									
cpu c	cpu capture buffer control register.											
bits name s/w h/w default description												
1	fifo_pop	rw	ro	0x0	write 1 to perform	capture buffer fife	рор					

1.6.2	1 CPU_CAPTURE_E	Reg.	0xA0080088						
сри с	apture buffer control regis	ter 2.							
bits	name	s/w	h/w	default		descripti	on		
0	en	rw	ro	0x0	packet capture er	nable. 1 = enabl	ed / 0 = disabled.		
1	capture_src_ctr I	rw	ro	0x0	packet capture src enable. 1 = capture data from TX path / = capture data from RX path.				
5:4	capture_mode	rw	ro	0x0	packet capture mode.  00: capture first packets received  01: capture first packets with pkt_type match  10: capture first pacekts with pkt_typt and header_type match  11: reserved.				
23:8	capture_pkt_typ e	rw	ro	0x0	packet capture type (used in mode 01 and 10)				
31:24	capture_header_ type	rw	ro	0x0	packet capture he	eader type (used	d in mode 10)		

1.6.2	2 TSEL_GDB_STA	TUS			0xA00800A0				
regis	ter used to return tsel G	DB status	S.						
bits	name	s/w	h/w	default	description				
0	tsel_link_statu s	ro	wo	0x0	tsel gdb link status (active high)				
1	diag_enable	ro	wo	0x0	diag_enable> signal from GDB.				
2	wdog_failure	ro	wo	0x0	sfp tsel_wdog_failure> driven by GDB				
8	tsel_led_red	ro	WO	0x0	led red - on and yellow=off and green=off => Power-on, or TSEL GDB detects errors that shall lead to board replacement				
9	tsel_led_yellow	ro	wo	0x0	led yellow - on and red=off and green=off => TSEL GDB detect issues on the link (link loss, remote fault)				
10	tsel_led_green	ro	WO	0x0	led green - on and yellow=off and red=off => TSEL GDB is initialized, link is up and communication with partner is working fine				
12	sfp_present_n	ro	wo	0x0	sfp present_n> active low				
13	sfp_tx_fault	ro	wo	0x0	sfp sfp_tx_fault> signal from SFP transceiver.				
14	sfp_rx_los	ro	wo	0x0	sfp rx los> signal from SFP transceiver.				
15	sfp_tx_disable	ro	wo	0x0	sfp sfp_tx_disable> signal from SFP transceiver.				
16	led_tsel_if_red	ro	WO	0x0	tsel instance specific led red - on and yellow=off and green=off => Power-on, or TSEL client detects errors that shall lead to board replacement				
17	led_tsel_if_yel low	ro	WO	0x0	tsel instance specific led yellow - on and red=off and green=off => TSEL client detect issues on the link (link loss remote fault)				
18	led_tsel_if_gre en	ro	WO	0x0	tsel instance specific led green - on and yellow=off and red=off => TSEL client is initialized, link is up and communication with host is working fine				

1.6.23 TS	EL_DEBUG	_CTRL		Reg.	0xA00800A4							
register us	register used to change default data flow											
bits	name	s/w	description									

0	tx_pkt_loopback	rw	ro	0x0	register used to route tsel TX path to RX. This is a debug feature that allows for stand alone testing where CPU packet inserter can be used drive RX data path.  0=default tx path. 1=tx_packets are looped back to rx
1	rx_pkt_loopback	rw	ro	0x0	register used to route tsel RX path to TX. This is a debug feature that allows for testing TSEL GDB packet loopback. 0=default tx path. 1=rx_packets are looped back to tx

1.6.2	4 TSEL_DEBUG_CT	Reg.	0xA00800A8								
register used to change internal parameters											
bits	name	s/w	h/w	default		description	n				
15:0	interpacket_gap	rw	ro	0x20	change min spacing between packets. DO NOT TOUCH UNLESS YOU KNOW WHAT YOU ARE DOING!						

1.6.2	5 DEBUG	Reg.	0xA00800AC									
reser	reserved											
bits name s/w h/w default description												
31:0	ctrl	rw	ro	0x0	connects to generate	al-purpose modu	le output port					

1.6.2	6 DEBUG_LINK_UP	Reg.	0xA00800B0								
register used to overwrite link status - allows to fake out a connection that tsel is connected to a partner.											
bits	name	s/w	h/w	default		description	า				
0	data	rw	ro	0x0	debug feature only - do not use unless you know what you are doing!						

1.6.2	7 TSEL_CLK_FREQ	Reg.	0xA00800B4							
freque	frequency of recovered clock, TSEL GTH									
bits name s/w h/w default description						١				
31:0	val	ro	wo	0x0	frequency reading	(Hz)				

1.6.2	8 TSEL_DEBUG_IF_	Reg.	0xA00800B8							
regist	register used to suppress interface activity, debug feature									
bits	name	s/w	h/w		description					
0	disable_if_gmii _tx	rw	ro	0x0	set to disable outp	out TX GMII I/F to	GDB, silently discards			
1	disable_if_gmii _rx	rw	ro	0x0	set to disable inpu packet at RX inpu		m GDB, silently discards			
2	disable_if_axis _rx	rw	ro	0x0	set to disable outpat RX output	out RX AXI-S I/F,	silently discards packet			
23:8	disable_if_axis _tx	rw	ro	0x0	set to disable sele (bit[8]=>src0, bit[9					

1.6.29	9 RX_STATS_ENGIN	Reg.	0xA00800C0						
register used to control stats engine.									
bits	bits name s/w h/w default						١		
0	table_clear	rw	write 1 to perform	stats engine table	e clear				

1.6.30 RX_STATS_ENGINE_STATUS	Reg.	0xA00800C4

regist	register used to return stats engine state									
bits	name	s/w	h/w	default	description					
0	busy	ro	wo	0x0	table_not_ready - when 1, stats table is busy (being cleared). Do not read stats engine until zero					
1	oor	ro	wo	0x0	out of range entry detected - when 1 it indicates stats engine was too small to capture statistics for input / outout packet type. reset by clearing stats table					
31:16	oor_pkt_type	ro	wo	0x0	out of range entry detected - last packet type that was out of range. reset by clearing stats table					

1.6.3	1 TX_STATS_ENGIN	Reg.	0xA00800C8							
regist	register used to control stats engine.									
bits name s/w h/w default description						า				
0	table_clear	rw	ro	0x0	write 1 to perform stats engine table clear		e clear			

1.6.3	2 TX_STATS_ENGIN	Reg.	0xA00800CC						
register used to return stats engine state									
bits	name	cription							
0	busy	ro	WO	0x0	cleared). Do not r	ead stats er			
1	oor	ro	wo	0x0	gine was too sma	III to capture t by clearing			
31:16	oor_pkt_type	ro	WO	0x0	out of range entry range. reset by cl		last packet type that was out of table		

1.6.3	3 PACKET_GEN_CT	Reg.	0xA00800E0						
register used to control packet generator rate control.									
bits name s/w h/w default description						า			
31:0	rate_ctrl	rw	ro	0x0	rate control to spa	ice packets. Rate	= 2**33 / value		

1.6.3	4 PACKET_GEN_CT	Reg.	0xA00800E4				
bits	name	s/w	h/w	description			
15:0	packet_type	rw	ro	0x0	packet generator	packet type used	in generating traffic.
23:16	header_type	rw	ro	0x0	header type used	for packet genera	ation.

1.6.3	5 PACKET_GEN_C	TRL2		0xA00800E8					
register used to control packet generator.									
bits	name	s/w	description						
0	enable	rw	ro	0x0	enable. $0 = off / 1 = on$				
1	mode	rw	ro	0x0	packet generator mode. 0 = fixed size (as defined in bits 31:15) / 1 = incremental 46 to 1500, incrementing by 1 on every packet				
15:8	seed	rw	ro	0x0	seed used for packet generator. Do not touch unless you know what you are doing				
31:16	packet_length	rw	ro	0x0	packet length used in mode 0 packet generator. Must be in range of 46 to 1500				

1.6.36 P	ACKET_GEN	Reg.	0xA00800EC		
1		/ 1/	1 6 16		
bits	name	s/w h/w	default	description	on

15:0	packet_type	rw	ro	0x0	packet generator checker packet type used in checking traf-
					fic.
23:16	header_type	rw	ro	0x0	header type used for packet checking.

1.6.3	7 PACKET_GEN_CH		Reg.	0xA00800F0						
register used to control generator checker.										
bits	name	s/w	h/w	default		description				
0	enable	rw	ro	0x0	enable. $0 = off / 1$	= on				
15:8	seed	rw	ro	0x0	seed used for packnow what you ar		not touch unless you			

1.6.3	8 PKT_COUNT_RX_	Reg.	0xA0080100							
generic free running counter										
bits	name	s/w	h/w	default		description	n			
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specifi functionality. Write 0 to clear					

1.6.3	9 BYTE_COUNT_RX	(_ <b>TO</b> 1		Reg.	0xA0080104				
generic free running counter									
bits	name	s/w	h/w	default		description	n		
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear				

1.6.4	D PKT_COUNT_RX_	FCS_	Reg.	0xA0080108						
generic free running counter										
bits	name	s/w	h/w	default	description					
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear					

1.6.4	BYTE_COUNT_RX	Reg.	0xA008010C						
generic free running counter									
bits	name	s/w	h/w	default	description				
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear				

1.6.42	2 PKT_COUNT_TX_	Reg.	0xA0080120						
generic free running counter									
bits	name	s/w	h/w	default		description			
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear				

1.6.43 BYTE_COUNT_TX_TOTAL	Reg.	0xA0080124
generic free running counter		

bits	name	s/w	h/w	default	description
31:0	count	rw	na		generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear

1.6.44	4 PKT_COUNT_TX_	Reg.	0xA0080128						
generic free running counter									
bits	name	s/w	h/w	default	description				
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear				

1.6.4	5 PKT_COUNT_TX_	Reg.	0xA008012C						
generic free running counter									
bits	name	s/w	h/w	default	description				
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specif functionality. Write 0 to clear				

1.6.4	6 PKT_COUNT_TX_	?	Reg.	0xA0080130						
generic free running counter										
bits	name	s/w	h/w	default	description					
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear					

1.6.4	7 PKT_COUNT_TX_	TOO_		Reg.	0xA0080134					
generic free running counter										
bits	name	s/w	h/w	default	description					
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear					

1.6.48	1.6.48 CPU_INSERT_BUFFER_CNT 0xA0080140												
regist	er used to return insert bu	ffer co	unters										
bits name s/w h/w default description													
31:0 success rw na 0x0 successful packet insertion counter													

1.6.4	1.6.49 CPU_CAPTURE_BUFFER_CNT 0xA0080144												
regist	register used to return capture buffer counters												
bits	name	s/w	h/w	default		description	n						
31:0 success rw na 0x0 successful packet capture counter													

1.6.5	0 CPU_CAPTURE_B	UFFE		Reg.	0xA0080148					
bits name s/w h/w default description										
31:0	overflow	rw	na	0x0	number of packets not captured due to CPU capture bubeing full.					

1.6.51	LINK_DOWN_CO	Reg.	0xA0080150									
generic free running counter												
bits	name	s/w	h/w	default	desc	cription						
31:0	count	rw	na		acket counter used for various fer to register name for specific							

1.6.5	1.6.52 PACKET_GEN_STATUS0 0xA0080180												
regist	register used to return packet generator info.												
bits	name	s/w	h/w	default		description	า						
31:0 pkt_count ro wo 0x0 number of packets inserted by the packet generator													

1.6.5	1.6.53 PACKET_GEN_CHECKER_STATUS0 0xA0080184												
regist	ter used to return packet c	hecker	info.										
bits	bits name s/w h/w default description												
31:0 pkt_count ro wo 0x0 number of packets checked													

1.6.5	1.6.54 PACKET_GEN_STATUS1 0xA0080188											
regist	register used to return packet generator info.											
bits	name	s/w	h/w	default		description	١					
31:0 bytes_count ro wo 0x0 number of bytes inserted by the packet generator												

1.6.55 PACKET_GEN_CHECKER_STATUS1 0xA008018C												
regist	register used to return packet checker info.											
bits	name	s/w	h/w	default		description	า					
31:0 bytes_count ro wo 0x0 number of bytes checked by the packet generator												

1.6.5	I.6.56 PACKET_GEN_CHECKER_STATUS2 0xA0080190												
regist	register used to return packet checker info.												
bits	name	s/w	h/w	default		description	1						
31:0 pkt_errors ro wo 0x0 number of packets with errors													

1.6.5	1.6.57 PACKET_GEN_CHECKER_STATUS3 0xA0080194												
regist	er used to return packet c	hecker	info.										
bits name s/w h/w default description													
31:0 byte_errors ro wo 0x0 number of bytes with errors													

1.6.5	1.6.58 PACKET_GEN_CHECKER_STATUS4 0xA0080198												
regist	er used to return packet c	hecker	info.										
bits	bits name s/w h/w default description												
31:0	length_errors	ro	wo	0x0	number of packets	s with length error	rs						

# 1.6.59 PACKET\_GEN\_CHECKER\_STATUS5 register used to return packet checker info. bits name s/w h/w default description 31:0 sequence\_errors ro wo 0x0 number of packets with sequence errors

1.6.60 CPU_INSE	RT_BUFFE		CPU_	_INSERT_	BUFFER					0xA0081000, 0xA0081004 0xA00817FF
offset		de	pth	512	widt	h 32	defa	ault	0x0	

This buffer is for CPU to be able to insert packets into TSEL GDB. This memory is implemented as a 4 packet FIFO that allows CPU to insert packets between 1 and 2044 bytes. Important: it is CPU responsibility to ensure inserted packet is in the correct format (i.e. ethernet packet) The following steps are to be performed in order for CPU to insert a packets: 1) check that insert packet FIFO is not full FIFO by reading IRQ\_RAW->cpu\_insert\_buffer\_fifo\_full = 0 (not full). 2) write insertion length in bytes (between 1-2044) to insert buffer entry [0] 3) write insertion data (between 1-2044 bytes) to insert buffer entries [1:511] 4) issue FIFO push by writting 1 to CPU\_INSERT\_BUFFER\_CTRL->fifo\_push. Packet will be inserted as soon as bus access is granted.

1.6.61 CPU_CAPT	TURE_BUFF		CPU_	CAPTURE_	BUFFER					0xA0081800, 0xA0081804 0xA0081FFF
offset		de	oth	512	width	32	def	ault	0x0	

This buffer is for CPU to be able to capture packets from TSEL GDB. The capture buffer is implemented as a 4 packet FIFO that allows CPU capture packets between 1 and 2044 bytes in length. The following steps are to be performed in order for CPU to capture packets: 1) set capture filter (TBD - not implemented yet) and enable capture engine CPU\_INSERT\_BUFFER\_CTRL->en = 1 2) wait for packet by reading IRQ\_RAW-cpu\_capture\_buffer\_pkt\_avail = 1 (or set up interrupt) 3) read capture buffer entry [0]. This entry holds the length of the captured packet in range of 1-2044 bytes 4) read captured data (between 1-2044 bytes form step 3) from capture buffer entries [1:511] 5) issue capture buffer FIFO pop by writting 1 to CPU\_INSERT\_BUFFER\_CTRL->cpu\_capture\_buffer\_ctrl.

1.6.62 RX_ST	ATS_ENGINE	RX_STATS_EN	NGINE					0xA0084000, 0xA0084004 0xA00847FF
offset	der	oth 512	width	32	defa	ult	0x0	

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

1.6.63 TX_	STATS_ENG	SINE TX_S	TATS_EN	GINE				0xA0086000, 0xA0086004 0xA00867FF
offset		depth	512	width	32	default	0x0	

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

1.7 tsel_if_client_srdl	Block	0xA0090000 - 0xA00967FF
Registers used to configure / control tsel interface		

1.7.1 MODULE_NAME	Reg.	0xA0090000

Module info register 0 - used to return module name. This register can be used for automated module discovery and to ensure

we are on the expected page in memory

bits	name	s/w	h/w	default	description
31:0	data	ro	na	0x52363335	ASCII Module name (TSEI Wrapper) - TSEW

#### 0xA0090004 1.7.2 MODULE\_VERSION Reg. Module info register 1 - used to return module version. Note: this register might change from build to build and might be used for future backwards compatibility default bits name s/w h/w description 31:8 major wo 0x0 Module version major ro 7:0 minor 0x0 Module version minor ro wo

1.7.3	HEADER_INFO	Reg.	0xA0090008									
Modu	Module info register 2 - used to return module memory page size											
bits	name	s/w	h/w	default		description						
15:0	block_size	ro	na	0x4	Addressable addr = 8192)	dress space in 4k pages (1 = 4096 bytes / 2						
31:16	unified_header_ ver	ro	Version of unified module memory header - used for any fuure changes to the header									

1.7.4	SCRATCHPAD		Reg.	0xA009000C								
Modu	Module info register 3 - scratchpad register used for testing module read / write access.											
bits	name	s/w	h/w	default		description	ı					
31:0	scratchpad	rw	na	0x0	scratchpad registe any time	er - can be read a	nd written by software at					

1.7.5	IRQ_ENABLE					Reg.	0xA0090010				
Register used to enable individual IRQs. If defined bit is set and interrupt occurs, interrupt pin will toggle, otherwise IRQ pin will not change.											
bits	name	s/w	h/w	default		description	٦				
0	cpu_insert_buff er_fifo_full	rw	na	0x0	IRQ enable - cpu	insert buffer full.					
1	cpu_insert_buff er_fifo_empty	rw	na	0x0	IRQ enable - cpu	insert buffer emp	ty.				
2	cpu_capture_buf fer_pkt_avail	rw	na	0x0	IRQ enable - cpu	capture buffer pk	t available.				
3	cpu_capture_buf fer_overflow	rw	na	0x0	IRQ enable - cpu	capture buffer ov	erflow.				
4	link_up	rw	na	0x0	IRQ enable - link	up.					
5	link_down	rw	na	0x0	IRQ enable - link	down.					

1.7.6	IRQ_PENDING			Reg.	0xA0090014							
Regis	Register used to return currently pending IRQs.											
bits	name		description									
0	cpu_insert_buff er_fifo_full	r/w1c	wo	0x0	IRQ pending - cpu insert buffer full indication. TBD - do we want this level sensitive?							
1	cpu_insert_buff er_fifo_empty	r/w1c	wo	0x0	IRQ pending - cpu we want this level		er empty indication. TBD - do					
2	cpu_capture_buf fer_pkt_avail	r/w1c	wo	0x0	IRQ pending - cpu	ı capture bu	uffer pkt available.					
3	cpu_capture_buf fer_overflow	r/w1c	wo	0x0	IRQ pending - cpu capture buffer overflow (capture full)							

4	link_up	r/w1c	wo	0x0	IRQ pending - link up
5	link_down	r/w1c	wo	0x0	IRQ pending - link down

1.7.7	IRQ_RAW				Reg.	0xA0090018					
Register used to return current value of IRQ input signals											
bits	name	s/w	h/w	default		description	n				
0	cpu_insert_buff er_fifo_full	ro	WO	0x0	current value of -	cpu insert buffer	full indication.				
1	cpu_insert_buff er_fifo_empty	ro	WO	0x0	current value of -	cpu insert buffer	empty indication.				
2	cpu_capture_buf fer_pkt_avail	ro	WO	0x0	current value of -	cpu capture buffe	er pkt available.				
3	cpu_capture_buf fer_overflow	ro	wo	0x0	current value of -	cpu_capture_buf	fer_overflow.				
4	link_up	ro	wo	0x0	current value of -	link status (0 = do	own / 1 = up).				
5	link_down	ro	wo	0x0	current value of -	link status (0 = do	own / 1 = up).				

## 1.7.8 IRQ\_FORCE 0xA009001C

Register used to force interrupts via software - this register is to be used for debugging interrupts only. Important, if the user goes and

manually forces an interrupt via any fields in this register (by setting a field to 1), the IRQ routine needs to clear the forced field otherwise the interrupt

will never clear and we will be stuck in an interrupt loop. Additionally, forcing an interrupt that is not enabled, will not result in interrupt pin being toggled.

bits	name	s/w	h/w	default	description
0	cpu_insert_buff er_fifo_full_fo rce	rw	na	0x0	register used to force IRQ-cpu_insert_buffer_fifo_full_force.
1	cpu_insert_buff er_fifo_empty_f orce	rw	na	0x0	register used to force IRQ-cpu_insert_buffer_fifo_empty.
2	cpu_capture_buf fer_pkt_avail_f orce	rw	na	0x0	register used to force IRQ-cpu_capture_buffer_pkt_avail.
3	cpu_capture_buf fer_overflow_fo rce	rw	na	0x0	register used to force IRQ-cpu_capture_buffer_overflow.
4	link_up_force	rw	na	0x0	register used to force IRQ-link_up
5	link_down_force	rw	na	0x0	register used to force IRQ-link_down

1.7.9	BUILD_INFO	Re	eg.	0xA0090040					
register used to return TSEL GDB info									
bits	name	s/w		description					
7:0	build_type	ro	WO	0x0	TSEL build type: 0 = tsel client / 1 = tsel bridge / others - reserved				
15:8	tsel_index	TSEL index - used to bridge instance num	ndex - used to confirm memory map to tsel client / instance number						

1.7.1	0 BUILD_INFO1	Reg.	0xA0090044							
register used to return TSEL Unified build info										
bits	bits name s/w h/w default description									
15:0	rx_stats_engine _size	ro	WO	0x0	number of entries used in rx stats engine. Only use rx_stats_engine if this field > 0					
31:16 tx_stats_engine ro wo 0x0 number of entries used in tx stats engine. Only use tx_stats_engine if this field > 0										

1.7.1	1 BUILD_INFO2		0xA0090048							
register used to return TSEL Unified build info										
bits name s/w h/w default description										
7:0	cpu_buf_addr_wi dth	ro	wo	0x0	address size of each CPU buffer; CPU buffer word size is 2^cpu_buf_addr_width					
15:8	cpu_buf_depth	ro	wo	0x0	number of buffers in CPU packet FIFO					
16	stats_bin_type	ro	wo	0x0	source used for stats binning, RX/TX_STATS_ENGINE; 0 - payload type, 1 - header type					

1.7.1	2 TSEL_CTRL	0xA0090060								
register used to control tsel gdb										
bits	name	s/w	description							
0	reset_force	rw	ro	0x0	field used to allow software ability to reset tsel GDB. 1=gd reset / 0= gdb not reset					
4	tsel_client_mac _address_valid	rw	ro	0x0	field used to allow software ability to change mac address, client only. TBD - this might have to be set before core is being reset					
5	tsel_client_eth _type_valid	rw	ro	0x0	field used to allow software ability to change ethernet type. TBD - this might have to be set before core is being reset					

1.7.13	3 TSEL_CLIENT_TX	Reg.	0xA0090064							
register used to control tsel gdb mac address insertion on the way out, client only										
bits	name	s/w	h/w	default		description	٦			
15:0	msb	rw	ro	0x1234	register used to assign mac address when external prom is not being used - bits [47:32]					

1.7.14	4 TSEL_CLIENT_TX		Reg.	0xA0090068							
register used to control tsel gdb mac address insertion on the way out, client only											
bits	name	s/w	h/w	default		description	n				
31:0	lsb	rw	ro		register used to assign mac address when external prom is not being used - bits [31:0]						

1.7.1	5 TSEL_CLIENT_TX	Reg.	0xA009006C							
register used to control tsel gdb ethernet type on the way out										
bits	name	s/w	h/w	default	description					
15:0	insert	rw	ro	0x8000	register used to assign ethernet type					

1.7.10	6 TSEL_CLIENT_RX	Reg.	0xA0090070								
	register used to return last packet src mac address (MSB).  Reading this register latches value in tsel_client_rx_mac_insert_lsb and tsel_client_rx_eth_type										
bits	name	s/w	h/w	default		description					
15:0	msb	ro	wo	0x0	src mac address -	bits [47:32]					

1.7.17	1.7.17 TSEL_CLIENT_RX_SRC_MAC_LSB 0xA0090074									
register used to return last packet src mac address (LSB)										
bits	bits name s/w h/w default description									
31:0	Isb	ro	wo	0x0	src mac address - bits [31:0]					

1.7.1	8 TSEL_CLIENT_RX	Reg.	0xA0090078									
regist	register used to return last packet ethernet type - this register is for Client TSEL GDB only											
bits	name	s/w	h/w	default		description						
15:0	received	ro	wo	0x0	register used to as	ssign ethernet typ	е					

1.7.19	9 CPU_INSERT_BUI	Reg.	0xA0090080								
regist	register used to control insert buffer										
bits	name	s/w	h/w	default	description						
0	fifo_push	rw	ro	0x0	write 1 to perform	insert buffer push	า				

1.7.2	0 CPU_CAPTURE_B	Reg.	0xA0090084							
cpu capture buffer control register.										
bits	name	s/w	h/w	default		description	١			
1	fifo_pop	rw	ro	0x0	write 1 to perform capture buffer fifo pop					

1.7.2	1 CPU_CAPTURE_E	BUFFE		Reg.	0xA0090088						
сри с	cpu capture buffer control register 2.										
bits	name	s/w	h/w	default	description						
0	en	rw	ro	0x0	packet capture er	nable. 1 = enab	oled / 0 = disabled.				
1	capture_src_ctr I	rw	ro	0x0	packet capture src enable. 1 = capture data from TX path = capture data from RX path.						
5:4	capture_mode	rw	ro	0x0	packet capture m 00: capture first p 01: capture first p 10: capture first p match 11: reserved.	ackets receive ackets with pk					
23:8	capture_pkt_typ e	rw	ro	0x0	packet capture ty	pe (used in mo	ode 01 and 10)				
31:24	capture_header_ type	rw	ro	0x0	packet capture he	eader type (use	ed in mode 10)				

1.7.2	2 TSEL_GDB_STA	TUS		0xA00900A0				
regis	ter used to return tsel GI	OB status	S.					
bits	name	s/w	h/w	description				
0	tsel_link_statu s	ro	wo	0x0	tsel gdb link status (active high)			
1	diag_enable	ro	wo	0x0	diag_enable> signal from GDB.			
2	wdog_failure	ro	wo	0x0	sfp tsel_wdog_failure> driven by GDB			
8	tsel_led_red	ro	WO	0x0	led red - on and yellow=off and green=off => Power-on, or TSEL GDB detects errors that shall lead to board replacement			
9	tsel_led_yellow	ro	wo	0x0	led yellow - on and red=off and green=off => TSEL GDB detect issues on the link (link loss, remote fault)			
10	tsel_led_green	ro	WO	0x0	led green - on and yellow=off and red=off => TSEL GDB is initialized, link is up and communication with partner is working fine			
12	sfp_present_n	ro	wo	0x0	sfp present_n> active low			
13	sfp_tx_fault	ro	wo	0x0	sfp sfp_tx_fault> signal from SFP transceiver.			
14	sfp_rx_los	ro	wo	0x0	sfp rx los> signal from SFP transceiver.			
15	sfp_tx_disable	ro	wo	0x0	sfp sfp_tx_disable> signal from SFP transceiver.			

16	led_tsel_if_red	ro	wo	0x0	tsel instance specific led red - on and yellow=off and green=off => Power-on, or TSEL client detects errors that shall lead to board replacement
17	led_tsel_if_yel low	ro	wo	0x0	tsel instance specific led yellow - on and red=off and green=off => TSEL client detect issues on the link (link loss, remote fault)
18	led_tsel_if_gre en	ro	wo	0x0	tsel instance specific led green - on and yellow=off and red=off => TSEL client is initialized, link is up and communication with host is working fine

1.7.2	3 TSEL_DEBUG_CT	Reg	0xA00900A4							
register used to change default data flow										
bits	name		description							
0	tx_pkt_loopback	rw	ro	0x0	feature that allower et inserter can be	oute tsel TX path to RX. This is a debug s for stand alone testing where CPU packused drive RX data path.  1=tx_packets are looped back to rx				
1	rx_pkt_loopback	rw ro 0x0 register used to route tsel RX path to TX. Thi feature that allows for testing TSEL GDB pac 0=default tx path. 1=rx_packets are looped b								

1.7.2	4 TSEL_DEBUG_CT	Reg.	0xA00900A8							
register used to change internal parameters										
bits	name	s/w	h/w	default		description	n			
15:0	15:0 interpacket_gap rw ro 0x20 change min spacing between packets. DO NOT TOUCH UNLESS YOU KNOW WHAT YOU ARE DOING!									

1.7.2	5 DEBUG	Reg.	0xA00900AC									
reser	reserved											
bits	name	s/w	h/w	default		description	1					
31:0	ctrl	rw	ro	0x0	connects to gener	al-purpose modu	le output port					

1.7.2	6 DEBUG_LINK_UP	Reg.	0xA00900B0							
register used to overwrite link status - allows to fake out a connection that tsel is connected to a partner.										
bits	name	s/w	h/w	default		description	า			
0	0 data rw ro 0x0 debug feature only - do not use unless you know what you are doing!									

1.7.2	7 TSEL_CLK_FREQ	Reg.		0xA00900B4							
freque	frequency of recovered clock, TSEL GTH										
bits	name	s/w	h/w	/w default description							
31:0	val	ro	wo	0x0	frequency reading (Hz)						

1.7.2	8 TSEL_DEBUG_IF_	SUPF		Reg.	0xA00900B8				
register used to suppress interface activity, debug feature									
bits	its name s/w h/w default description								
0	disable_if_gmii _tx	rw	ro	0x0	set to disable output TX GMII I/F to GDB, silently discards TX packets				
1	disable_if_gmii _rx	ut RX GMII I/F from GDB, silently discards							

2	disable_if_axis _rx	rw	ro	0x0	set to disable output RX AXI-S I/F, silently discards packet at RX output
23:8	disable_if_axis	rw	ro	0x0	set to disable selected TX AXI-S I/F source input
	_tx				(bit[8]=>src0, bit[9]=>src1, etc), holds TREADY low

1.7.29	9 RX_STATS_ENGIN	Reg.	0xA00900C0								
regist	register used to control stats engine.										
bits	name	s/w	h/w	default		description	١				
0	table_clear	rw	ro	0x0	write 1 to perform stats engine table clear						

1.7.3	0 RX_STATS_ENGI	NE_S		Reg.	0xA00900C4					
register used to return stats engine state										
bits	name	s/w	h/w	default	description					
0	busy	ro	wo	0x0	table_not_ready - when 1, stats table is busy (being cleared). Do not read stats engine until zero					
1	oor	ro	WO	0x0	out of range entry detected - when 1 it indicates stats engine was too small to capture statistics for input / outout packet type. reset by clearing stats table					
31:16	oor_pkt_type	ro	WO	0x0	out of range entry range. reset by cl		acket type that was out of			

1.7.3	1 TX_STATS_ENGIN	Reg.	0xA00900C8								
regist	register used to control stats engine.										
bits	bits name s/w h/w default description										
0	table_clear	rw	ro	0x0	write 1 to perform	stats engine table	e clear				

1.7.3	2 TX_STATS_ENGIN	NE_S1		Reg.	0xA00900CC					
register used to return stats engine state										
bits	bits name s/w h/w default description									
0	busy	ro	WO	0x0	table_not_ready - when 1, stats table is busy (being cleared). Do not read stats engine until zero					
1	oor	ro	WO	0x0	out of range entry detected - when 1 it indicates stats engine was too small to capture statistics for input / outout packet type. reset by clearing stats table					
31:16	oor_pkt_type	ro	WO	0x0		detected - last page earing stats table	acket type that was out of			

1.7.3	3 PACKET_GEN_CT	Reg.	0xA00900E0							
register used to control packet generator rate control.										
bits	name	s/w	h/w	default	description					
31:0	rate_ctrl	rw	ro	0x0	rate control to spa	ce packets. Rate	= 2**33 / value			

1.7.3	4 PACKET_GEN_CT	Reg.	0xA00900E4						
bits	name	s/w	h/w	default	description				
15:0	packet_type	rw	ro	0x0	packet generator packet type used in generating traffic.				
23:16	header_type	rw	ro	0x0	header type used	for packet genera	ation.		

1.7.35 PACKET_GEN_CTRL2	Reg.	0xA00900E8

regist	register used to control packet generator.										
bits	name	s/w	h/w	default	description						
0	enable	rw	ro	0x0	enable. $0 = off / 1 = on$						
1	mode	rw	ro	0x0	packet generator mode. 0 = fixed size (as defined in bits 31:15) / 1 = incremental 46 to 1500, incrementing by 1 on every packet						
15:8	seed	rw	ro	0x0	seed used for packet generator. Do not touch unless you know what you are doing						
31:16	packet_length	rw	ro	0x0	packet length used in mode 0 packet generator. Must be in range of 46 to 1500						

1.7.3	6 PACKET_GEN_CH	Reg.	0xA00900EC					
bits	name	s/w h/w default description						
15:0	packet_type	rw	ro	0x0	packet generator checker packet type used in checking traf- fic.			
23:16	header_type	rw	ro	0x0	header type used	for packet checki	ng.	

1.7.3	7 PACKET_GEN_CH	Reg	0xA00900F0							
register used to control generator checker.										
bits	name	s/w	h/w	default	description	description				
0	enable	rw	ro	0x0	enable. 0 = off / 1 = on					
15:8 seed rw ro 0x0 seed used for packet generator. Do not touch unless you know what you are doing										

1.7.3	8 PKT_COUNT_RX_	Reg.	1	0xA0090100						
generic free running counter										
bits	name	s/w	h/w	default		description				
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear					

1.7.39	BYTE_COUNT_RX	Reg.	0xA0090104							
generic free running counter										
bits	name	s/w	h/w	default		description				
31:0	count	rw	na	0x0		thering. Refer to	counter used for various register name for specific			

1.7.40	PKT_COUNT_RX_	Reg.	0xA0090108							
generic free running counter										
bits	name	s/w	h/w	default		description	า			
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear					

1.7.41	BYTE_COUNT_R	Reg.	0xA009010C								
generi	generic free running counter										
bits	bits name s/w h/w default description										

31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various
					diagnostic info gathering. Refer to register name for specific
					functionality. Write 0 to clear

1.7.42	2 PKT_COUNT_TX_		Reg.	0xA0090120							
gener	generic free running counter										
bits	name	s/w	h/w	default		description					
31:0	count	rw	na	0x0		thering. Refer to r	counter used for various register name for specific				

1.7.4	BYTE_COUNT_TX	Reg.	0xA0090124								
gener	generic free running counter										
bits	name	s/w	h/w	default		description					
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for variou diagnostic info gathering. Refer to register name for spec functionality. Write 0 to clear						

1.7.4	4 PKT_COUNT_TX_	Reg.	0xA0090128							
generic free running counter										
bits	name	s/w	h/w	default		descriptio	n			
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specif functionality. Write 0 to clear					

1.7.4	5 PKT_COUNT_TX_	Reg.	0xA009012C								
genei	generic free running counter										
bits	name	s/w	h/w	default		description					
31:0	count	rw	na	0x0		thering. Refer to r	counter used for various register name for specific				

1.7.40	6 PKT_COUNT_TX_	TOO_	?	Reg.	0xA0090130				
generic free running counter									
bits	name	s/w	h/w	default		description	n		
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specifi functionality. Write 0 to clear				

1.7.4	7 PKT_COUNT_TX_	TOO_		Reg.	0xA0090134				
generic free running counter									
bits	name	s/w	h/w	default	description				
31:0	count	rw	na	0x0	generic free running 32 bit packet counter used for various diagnostic info gathering. Refer to register name for specific functionality. Write 0 to clear				

1.7.48 CPU_INSERT_BUFFER_CNT	Reg.	0xA0090140
register used to return insert buffer counters		

bits	name	s/w	h/w	default	description
31:0	success	rw	na	0x0	successful packet insertion counter

1.7.4	9 CPU_CAPTURE_B	Reg.	0xA0090144								
regist	register used to return capture buffer counters										
bits	bits name s/w h/w default description										
31:0											

1.7.5	O CPU_CAPTURE_B	Reg.	0xA0090148						
bits	name		description	١					
31:0	overflow	rw	na	0x0	number of packets not captured due to CPU capture buffe being full.				

1.7.5	I LINK_DOWN_COU	Reg.	0xA0090150							
generic free running counter										
bits	name	s/w	h/w	default		description				
31:0	count		counter used for various register name for specific							

1.7.5	2 PACKET_GEN_ST	Reg.	0xA0090180								
register used to return packet generator info.											
bits name s/w h/w default description											
31:0 pkt_count ro wo 0x0 number of packets inserted by the packet generator											

1.7.5	3 PACKET_GEN_CH	Reg.	0xA0090184								
regist	register used to return packet checker info.										
bits name s/w h/w default description											
31:0											

1.7.5	4 PACKET_GEN_ST	Reg.	0xA0090188								
register used to return packet generator info.											
bits name s/w h/w default description											
31:0	bytes_count	number of bytes in	nserted by the pa	cket generator							

1.7.5	5 PACKET_GEN_CH	Reg.	0xA009018C									
regist	register used to return packet checker info.											
bits name s/w h/w default description												
31:0 bytes_count ro wo 0x0 number of bytes checked by the packet generator												

1.7.5	1.7.56 PACKET_GEN_CHECKER_STATUS2 0xA0090190												
regist	register used to return packet checker info.												
bits	bits name s/w h/w default description												
31:0 pkt_errors ro wo 0x0 number of packets with errors													

1.7.5	7 PACKET_GEN_CH	IECK	ER_S	TATUS3		Reg.	0xA0090194				
regist	register used to return packet checker info.										
bits name s/w h/w default description											
31:0 byte_errors ro wo 0x0 number of bytes with errors											

1.7.5	8 PACKET_GEN_CH	Reg.	0xA0090198							
register used to return packet checker info.										
bits name s/w h/w default description										
31:0	length_errors	number of packets	s with length erro	rs						

1.7.5	9 PACKET_GEN_CH	Reg.	0xA009019C							
register used to return packet checker info.										
bits name s/w h/w default description										
31:0 sequence_errors ro wo 0x0 number of packets with sequnce errors										

1.7.60 CPU_INSE	RT_BUFFER	CPU_	_INSERT_B	UFFER					0xA0091000, 0xA0091004 0xA00917FF
offset		depth	512	width	32	defa	ault	0x0	

This buffer is for CPU to be able to insert packets into TSEL GDB. This memory is implemented as a 4 packet FIFO that allows CPU to insert packets between 1 and 2044 bytes. Important: it is CPU responsibility to ensure inserted packet is in the correct format (i.e. ethernet packet) The following steps are to be performed in order for CPU to insert a packets: 1) check that insert packet FIFO is not full FIFO by reading IRQ\_RAW->cpu\_insert\_buffer\_fifo\_full = 0 (not full). 2) write insertion length in bytes (between 1-2044) to insert buffer entry [0] 3) write insertion data (between 1-2044 bytes) to insert buffer entries [1:511] 4) issue FIFO push by writting 1 to CPU\_INSERT\_BUFFER\_CTRL->fifo\_push. Packet will be inserted as soon as bus access is granted.

1.7.61		CPU_CAPTUR	RE_BUFFER		0xA0091800,	
CPU_CAP1	TURE_BUFFER					0xA0091804 0xA0091FFF
offset	de	pth 512	width 32	default	0x0	

This buffer is for CPU to be able to capture packets from TSEL GDB. The capture buffer is implemented as a 4 packet FIFO that allows CPU capture packets between 1 and 2044 bytes in length. The following steps are to be performed in order for CPU to capture packets: 1) set capture filter (TBD - not implemented yet) and enable capture engine CPU\_INSERT\_BUFFER\_CTRL->en = 1 2) wait for packet by reading IRQ\_RAW-cpu\_capture\_buffer\_pkt\_avail = 1 (or set up interrupt) 3) read capture buffer entry [0]. This entry holds the length of the captured packet in range of 1-2044 bytes 4) read captured data (between 1-2044 bytes form step 3) from capture buffer entries [1:511] 5) issue capture buffer FIFO pop by writting 1 to CPU\_INSERT\_BUFFER\_CTRL->cpu\_capture\_buffer\_ctrl.

1.7.62 RX_	STATS_ENG	SINE RX_S	TATS_EN	SINE					0xA0094000, 0xA0094004 0xA00947FF
offset		depth	512	width	32	defa	ault	0x0	

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

1.7.63 TX_STATS_ENGINE TX_STATS_ENGINE		0xA0096000, 0xA0096004 0xA00967FF
--	--	---

offset depth 512 width 32 default 0x0

This buffer is for CPU to be able to read stats engine (TX or RX). Before attempting to read the stats engine, check that stats engine entires are > 0. The stats engine is used to collect the following info (per packet type). Do not attempt to read more than stats engine entires defined. 1) number of packets detected since table cleared 2) number of bytes detected since table cleared 3) packet size info since table cleared [31:16] max packet size / [15:0] min packet size. 4) [31:16] last packet sequence number. [15:0] number of packet sequence errors - saturates at 0xFFFF

## 1.8 tselclient\_appl\_registers\_srdl OxA00A0000 - OxA00A00EB Register map used to access and control global FPGA functionality

1.8.1	tselclient_module_ı	Reg.	0xA00A0000							
Defin	Defines the module name									
bits	name	s/w	h/w	default		description	١			
31:0	module_name	odule name - tsel	client = tcli							

1.8.2	tselclient_module	Reg.	0xA00A0004						
Module version									
bits	name	des	scription						
31:16	rfu	ro	na	0x0	Reserver for Future Use - RFU				
15:8	major_revision	ro	wo	0x0	Major Revisoin of module - New features or capabilities defi- nition have been added.				
7:0 minor_revision ro wo 0x0 Minor Revision of module. This field indicates bug f have been applied. For any new features/capabilities ment, this field will reset to zero.									

1.8.3	tselclient_page_p	oroperti	0xA00A0008							
Address page properties										
bits	description									
31	present	ro	WO	0x1	Address page is present if '1', not present when '0'. It is in dicating that the logic accessed by this page is avalable/in plemented or not.					
30:16	rfu	ro	na	0x0	Reserver for Future Use - RFU					
15:8	page_size	ro	na	0x1	Address page size: 1 -> 4kB, 2 -> 8kB, etc. Divide the real value to 4k and enetr here.					
7:0	unified_header_ rev	ro	na	0x1	Unified Header Format common registers revision.					

1.8.4	tselclient_scratchre	Reg.	0xA00A000C							
Scrate	Scratchregister register									
bits	name	s/w	h/w	default		description	n			
31:0	for test purposes.									

1.8.5	tselclient_irq_enab	Reg.	0xA00A0010						
Interrupt Requests Enable/Mask Control Register									
bits	name	s/w	h/w	default		description	า		
0	irq0_enable	rw	ro	0x0	IRQ0 enable bit. Not implemented here/DTEC				
1	irq1_enable	rw	Not implemented	here/DTEC					

1.8.6	tselclient_irq_pend	Reg.	0xA00A0014					
Interrupt Pending Status Register								
bits	oits name s/w h/w default description							
0	irq0_pending	r/w1c	WO	0x0			Write '1' to clear. Asserts emented here/DTEC	
1	irq1_pending			Write '1' to clear. Asserts emented here/DTEC				

1.8.7	tselclient_irq_raw	Reg.	0xA00A0018							
Interru	Interrupt Raw Status Register									
bits	name	s/w	h/w	default		description	ı			
0	0 irq0_raw ro wo 0x0 IRQ0 raw status bit. Not implemented here/DTEC									
1	irq1_raw	ro	wo	0x0	IRQ1 raw status b	it. Not implement	ed here/DTEC			

1.8.8	tselclient_irq_force	Reg.	0xA00A001C						
Interrupt Force Control Register									
bits	name	s/w	h/w	default		description	า		
0	irq0_force	rw	ro	0x0	IRQ0 force bit. SV implemented here		nulate an interrupt. Not		
1 irq1_force rw ro 0x0 IRQ1 force bit. SW to write '1' to emulate an interrupt. Not implemented here/DTEC									

1.8.9	rt_data_handler_	_stat			0xA00A0060
video					nd receive) status overview. various errors details will be pro- packet2 while tranmit fsm transmits acknowledement pkt for
bits	name	s/w	h/w	default	description
0	rx_fsm_pkt_lgth _field_err	r/w1c	WO	0x0	1 = received a packet1/packet2 with length field not equal to 0x30/45 /0 = received packet with expected data in length filed.
1	rx_fsm_pload_er r	r/w1c	WO	0x0	1 = received a packet1/packet2 with pload type isn't 0x15 (ETEC sends DTEC) /0 = received packet with expected data in pload type field.
2	rx_fsm_e2d_hdr_ err	r/w1c	wo	0x0	1 = received a packet1 with e2d header is not 0x10/0x11 /0 = received packet with expected data in e2d header field.
3	pkt1_sync_hdr_e rr	r/w1c	wo	0x0	1 = received a packet1 with sync id field not equal to 0x04 / e received packet with expected data in sync id header field
4	pkt1_etecflags_ hdr_err	r/w1c	WO	0x0	1 = received a packet1 with etecflags header field not equal to 0x05 /0 = received packet with expected data in etecflags header field.
5	pkt1_zeropad_hd r_err	r/w1c	wo	0x0	1 = received a packet1 with zeropad field not equal to zero/0 = received packet with expected zeros in zeropad field.
6	rx_fsm_eot_err	r/w1c	wo	0x0	1 = received a packet1 with eot field not equal to 0xA5/0 = received packet with expected data in eot header field.
8:7	pkt1_seq_err	r/w1c	WO	0x0	MSB 1 = received a packet1 with sequence number er- ror/0 = received packet with expected sequence number. re ceived packet1 should be received in order. after reset the lsb bit is always set to 1 and ignore this
10:9	pkt2_seq_err	r/w1c	WO	0x0	MSB 1 = received a packet2 with sequence number er- ror/0 = received packet with expected sequence number. re ceived packet2 should be received in order. after reset the lsb bit is always set to 1 and ignore this
11	rx_fsm_eop_err	r/w1c	wo	0x0	1 = if packet1/packet2 received is terminated early or lasts longer than expected
12	link_loss	r/w1c	wo	0x0	1 = link loss/0 = link is established.
13	rx_fsm_wdog_err	r/w1c	wo	0x0	1 = real time receive fsm doesn't return to idle state within 100 clk cycles.

14	pkt1_wdog_err	r/w1c	WO	0x0	1 = not received packet1 within 100us where it is expected to be recived every 60KHz
15	not_rx_rd_pkt2_ axis	r/w1c	wo	0x0	1 = pkt2 axis tx fsm has valid data but not received ready with in valid time of 80us
16	pkt2_axis_fsm_w dog_err	r/w1c	wo	0x0	1 = pkt2 axis tx fsm didn't return to idle within valid time of 100us
17	reserved_byte_e rr	r/w1c	wo	0x0	<ul><li>1 = received a packet with reserved field not equal to zero/0</li><li>= received packet with expected zeros in reserved field.</li></ul>
18	pkt2_zeropad_hd r_err	r/w1c	wo	0x0	<ul><li>1 = received a packet2 with zeropad field not equal to zero/0</li><li>= received packet with expected zeros in zeropad field.</li></ul>
19	pkt1_detected	r/w1c	wo	0x0	1 = tsel client received packet1. these are provided to rdl counters to count how many packet1 being received
20	pkt2_detected	r/w1c	wo	0x0	1 = tsel client received packet2. these are provided to rdl counters to count how many packet2 being received
21	good_pkt2_detec ted	r/w1c	wo	0x0	1 = received good packet2. these are provided to rdl counters to count how many good packet2 being received
22	pkt2_data_lost	r/w1c	WO	0x0	1 = received good packet2 but the data got lost before axi- streaming it out. the reasons can be the fsm is either waiting for the ready signal so it can axis depacketized packet2 or its in the process of tranmitting an older pkt2
24:23	rx_fsm_reserved	r/w1c	wo	0x0	2 bits reserved for receive fsm future use
25	tx_fsm_link_los s	r/w1c	wo	0x0	1 = link loss/0 = link is established. same as the 12th bit, repeated again for easy redability(when testing tx fsm alone)
26	tx_fsm_axis_fif i_full	r/w1c	wo	0x0	transmit fsm tranmits the ack packtes to unified tsel interface through axis fifo.1= fifo is full/0 = fifo not full.
27	tx_fsm_internal _fifo_full	r/w1c	WO	0x0	transmit fsm receives input from receive fsm through inter- anl fifo. 1= fifo is full/0 =fifo not full. transmit fsm sends an acknowledement pkt for every packet1 received from etec, a fifo of depth 16 is added to store the response for packet1.
28	tx_fsm_internal _fifo_empty	r/w1c	WO	0x0	transmit fsm receives input from receive fsm through interanl fifo.1 = fifo is empty/0 = fifo not empty. transmit fsm sends an acknowledement pkt for every packet1 received from etec, a fifo of depth 16 is added to store the response for packet1.
29	tx_fsm_wdog_err	r/w1c	WO	0x0	1 = real time transmit fsm doesn't return to idle state within 3ms
31:30	tx_fsm_reserved	r/w1c	wo	0x0	3 bits reserved for transmit fsm future use

1.8.10	0 tx_fsm_dg_kpi_ct	Reg.	0xA00A0064							
ddm d	ddm dg kpi enable control									
bits	name	s/w	h/w	default	description					
0	tx_dg_kpi	rw	ro	0x1	packets) through	acknowledement 1 = send ddm bp	am1 metrics(send 7 ESM packet sent using real pam metrics / 0 = stop			

1.8.11 pkt1	RegGrp	0xA00A0068 - 0xA00A008F
received pkt1 data from etec after depacketisation. 25 bytes wide		

1.8.1	1.1 tag1				Reg.	0xA00A0068
tag fo	or sowftare to make sure a	III the registers	s are read at s	ame time		
bits	name	s/w h/w	default		description	١
15:0	tag	ro wo	0x0	synchronization re	egister	

1.8.11.2 timestamp_data	Reg.	0xA00A006C
packet1 timestamp data		

bits	name	s/w	h/w	default	description
31:0	timestamp	ro	wo	0x0	4 bytes long timestamp

1.8.1	1.3 sync_stat_data					Reg.	0xA00A0070
packe	et1 sync status data						
bits	name	s/w	h/w	default		descriptio	n
0	fire_droplet	ro	wo	0x0	ON -fire ON/OFF	droplet	
1	health_status	ro	wo	0x0	H-communication	health status '1'	
2	wc_trigger	ro	wo	0x0	waveform capture	e trigger	
3	ppec	ro	wo	0x0	perform pre pulse	energy control	
4	early_exp_gate_ indicator	ro	wo	0x0	Early indicator of	exposure gate	
5	sync_stat_bit5	ro	wo	0x0	spare		
6	sync_stat_bit6	ro	wo	0x0	spare		
7	sync_stat_bit7	ro	wo	0x0	spare		

1.8.1	1.4 shot_id_data					Reg.	0xA00A0074
packe	et1 shot ID data						
bits	name	s/w	h/w	default		description	١
31:0	shot_id	ro	wo	0x0	4 bytes long		

1.8.1	1.5 burst_id_data					Reg.	0xA00A0078
packe	et1 burst ID data						
bits	name	s/w	h/w	default		description	١
31:0	burst_id	ro	wo	0x0	4 bytes long		

1.8.1	1.6 msec_id_data					Reg.	0xA00A007C
packe	et1 msec ID data						
bits	name	s/w	h/w	default		description	ı
31:0	msec_id	ro	wo	0x0	4 bytes long		

1.8.1	1.7 lc_diag_data					Reg.	0xA00A0080
packe	et1 lc diagnostics data						
bits	name	s/w	h/w	default		des	scription
0	fast_euv_gaten	ro	wo	0x1	active low fast e	uv gate	
1	scanner_gaten	ro	wo	0x1	active low scan	ner gate	
2	exp_gaten	ro	wo	0x1	active low expos	sure gate	
3	lc_diag_bit3	ro	wo	0x0	spare		
4	lc_diag_bit4	ro	wo	0x0	spare		
5	lc_diag_bit5	ro	wo	0x0	spare		
6	lc_diag_bit6	ro	wo	0x0	spare		
7	lc_diag_bit7	ro	WO	0x0	spare		
8	lc_diag_bit8	ro	wo	0x0	spare		
9	lc_diag_bit9	ro	wo	0x0	spare		
10	lc_diag_bit10	ro	wo	0x0	spare		
11	lc_diag_bit11	ro	wo	0x0	spare		
12	lc_diag_bit12	ro	wo	0x0	spare		
13	lc_diag_bit13	ro	wo	0x0	spare		
14	lc_diag_bit14	ro	wo	0x0	spare		
15	lc_diag_bit15	ro	wo	0x0	spare		

1.8.1	1.8 pp2mp_tfire_to	otaldela	ıy_da	ıta		Reg.	0xA00A0084
packe	et1 pp2mp tfire totaldela	y data					
bits	name	s/w	h/w	default		desc	cription
31:0	pp2mp_tfire_tot aldelay	ro	wo	0x0	4 bytes long		
1.8.1	1.9 euv_value_dat	a				Reg.	0xA00A0088
packe	et1 euv value data						
bits	name	s/w	h/w	default		desc	cription
31:0	euv_value	ro	wo	0x0	4 bytes long		
1.8.1	1.10 tag2					Reg.	0xA00A008C
tan fo	or sowftare to make sure	all the re	egister	s are read at	same time		
tay it				1 ( 1			printion
bits	name	s/w	h/w	default		desc	cription
bits		s/w ro	h/w wo	0x0	synchronization RegGroup		ΣΗ <b>Ρ</b> ΙΙΟΠ
bits 15:0	name	ro	wo	0x0 End F			0xA00A0090
bits 15:0	tag	ro	wo	0x0 End F	RegGroup	register	
bits 15:0	name tag  2 ddm_bpam_sene	ro	wo	0x0 End F	RegGroup	register  Reg.	0xA00A0090
bits 15:0 1.8.1 regis	name tag  2 ddm_bpam_seneter used to return count	ro  d7_crc  of ddm b	wo  err_ pam se	0x0  End F  cnt  end7 crc error	RegGroup	register  Reg.  descrements when	0xA00A0090  cription the ddm bpam send7 crc erro
bits 15:0 1.8.1 regist	name tag  2 ddm_bpam_sene ter used to return count name	d7_crc_of ddm b	err_pam so	0x0  End F  cnt  end7 crc error  default	RegGroup	register  Reg.  descrements when	0xA00A0090  cription the ddm bpam send7 crc erro
bits 15:0 1.8.1 regist bits 31:0	name tag  2 ddm_bpam_sene ter used to return count name	d7_crc of ddm b s/w rw	err_pam so	0x0  End F  cnt  end7 crc error  default	RegGroup	register  Reg.  descrements when	0xA00A0090  cription the ddm bpam send7 crc erro
bits 15:0 1.8.1 regist bits 31:0	name tag  2 ddm_bpam_sene ter used to return count name err_count	d7_crc_of ddm b	err_pam se	end7 crc error default 0x0	RegGroup	register  descrements when od pkt2 is reco	0xA00A0090  cription the ddm bpam send7 crc erroreived
bits 15:0 1.8.1 regist bits 31:0	name tag  2 ddm_bpam_sene ter used to return count name err_count  3 ddm_data_lost_e	d7_crc_of ddm b	err_pam se	end7 crc error default 0x0	RegGroup	descrements when	0xA00A0090  cription the ddm bpam send7 crc erroreived
bits 15:0  1.8.1 regist bits 31:0	name tag  2 ddm_bpam_sence ter used to return count name err_count  3 ddm_data_lost_center used to return count	d7_crc_of ddm b s/w rw	err_pam so h/w na	End F  cnt end7 crc error default 0x0	RegGroup TS this counter incibit is 1 when go	descrements when od pkt2 is reco	0xA00A0090  cription the ddm bpam send7 crc erroreived  0xA00A0094
bits 15:0  1.8.1 regist bits 31:0	name tag  2 ddm_bpam_sence ter used to return count name err_count  3 ddm_data_lost_center used to return count name	d7_crc_of ddm b s/w rw	err_pam se h/w na	end7 crc error default 0x0	RegGroup  This counter incident in the second of the secon	descrements when od pkt2 is reco	0xA00A0090  cription the ddm bpam send7 crc erreleived  0xA00A0094  cription
bits 15:0 1.8.1 regist bits 31:0 1.8.1 regist bits 31:0	name tag  2 ddm_bpam_sence ter used to return count name err_count  3 ddm_data_lost_center used to return count name	d7_crc_of ddm b s/w rw	err_pam so h/w na	end7 crc error default 0x0	RegGroup  This counter incident in the second of the secon	descrements when od pkt2 is reco	0xA00A0090  cription the ddm bpam send7 crc erroreived  0xA00A0094  cription
bits 15:0 1.8.1 regist bits 31:0 1.8.1 1.8.1	name tag  2 ddm_bpam_sene ter used to return count name err_count  3 ddm_data_lost_eter used to return count name err_count	of ddm d s/w rw  cnt of ddm d s/w rw	err_pam so h/w na ata los h/w na	end Force error default 0x0	RegGroup  This counter incident in the second of the secon	descrements when od pkt2 is recorded to the control of the control	0xA00A0090  cription the ddm bpam send7 crc error elived  0xA00A0094  cription the ddm data received can't
bits 15:0 1.8.1 regist bits 31:0 1.8.1 1.8.1	name tag  2 ddm_bpam_sene ter used to return count name err_count  3 ddm_data_lost_eter used to return count name err_count  4 ddm_data_bytes	of ddm d s/w rw  cnt of ddm d s/w rw	err_pam so h/w na ata los h/w na	end Force error default 0x0	RegGroup  This counter incident in the second of the secon	descrements when od pkt2 is recorded to the mode fifo	0xA00A0090  cription the ddm bpam send7 crc error eleived  0xA00A0094  cription the ddm data received can't

1.8.1	6 rx_fsm_pload_	err_cnt			Reg.	0xA00A00A0
regis	ter used to return capt	tured packe	t paylo	ad field error		
bits	name	s/w	h/w	default	des	cription
	err count	rw	na	0x0	received packet payload field	Larrar captura countar

description

received packet length field error capture counter

default

register used to return captured packet length field errror

name

h/w

na 0x0

s/w

rw

bits

31:0 err\_count

			cnt				Reg.	
regis	ter used	to return the cour	nt of unl	known	packets recei	ved		
bits 31:0	rx_cnt	name	s/w rw	h/w na	default 0x0	+1 => the fsm that packet	descripti t recives the dat	on ta, detected an unknowr
.8.1	8 pkt1_	_sync_hdr_er	r_cnt				Reg.	0xA00A00A8
regis	ter used	to return captured	d packe	t1 syn	c header field	errror		
bits		name	s/w	h/w	default		descripti	
31:0	err_cou	nt	rw	na	0x0	packet1 sync hdr	field error captu	re counter
.8.1	9 pkt1_	_etecflags_hc	dr_err	_cnt			Reg.	0xA00A00AC
regis	ter used	to return captured	d packe	t1 ete	flags header	field errror		
bits		name	s/w	h/w	default		descripti	on
31:0	err_cou	nt	rw	na	0x0	packet1 etec flags	s hdr field error	capture counter
1.8.2	0 nkt1	_zeropad_hdr	err	cnt			Reg.	0xA00A00B0
	-	-			16.11			
	iter usea	to return captured				or		
bits		name	s/w	h/w	default		descripti	∩n
31:0	err cou	nt	rw	na	0x0	packet1 zeropad f	field error captu	
31:0	err_cou	nt	rw	na	0x0	packet1 zeropad f	field error captu	
		nt m_eot_err_c		na	0x0	packet1 zeropad f	Reg.	
1.8.2	21 rx_fs		nt			packet1 zeropad f	·	re counter
1.8.2	21 rx_fs	m_eot_err_c	nt			packet1 zeropad f	·	0xA00A00B4
regis	21 rx_fs	m_eot_err_cl to return captured name	nt d packe	t errro	r in eot	packet1 zeropad f	Reg.	0xA00A00B4
regis bits 51:0	21 rx_fs ster used err_cou	m_eot_err_cl to return captured name	nt d packe s/w	t errro h/w	r in eot default		Reg.	0xA00A00B4
regis bits 31:0	21 rx_fs ster used err_cou	m_eot_err_cl to return captured name nt	nt d packe s/w rw	t errro h/w na	r in eot default 0x0	received packet n	descriptiot terminated as	0xA00A00B4  on s expected
regis bits 31:0	21 rx_fs ster used err_cou	to return captured name nt	nt d packe s/w rw	t errro h/w na	r in eot default 0x0	received packet n	descripti ot terminated as	on s expected 0xA00A00B8
regis bits 31:0	21 rx_fs ster used err_cou	to return captured name nt seq_err_cnt to return captured name	nt d packe s/w rw	t errro h/w na t1 seq	r in eot default 0x0 uence errror in	received packet n	descripti ot terminated as	on s expected 0xA00A00B8
regis bits 1:0	err_cou	to return captured name nt seq_err_cnt to return captured name	nt d packe s/w rw d packe s/w	t errro h/w na t1 seq h/w	r in eot default 0x0  uence errror in	received packet n	descripti ot terminated as	on s expected 0xA00A00B8
regis bits 1:0	err_cou err_cou err_cou	to return captured name nt  seq_err_cnt to return captured name nt	nt d packe s/w rw d packe s/w rw	t errro h/w na t1 seq h/w na	r in eot default 0x0  uence errror in default 0x0	received packet none eot	descripti ot terminated as  Reg.  descripti	on on OxA00A00B8
regis bits 11:0	err_cou err_cou err_cou	to return captured name nt  seq_err_cnt to return captured name nt  seq_err_cnt to return captured name nt	nt d packe s/w rw d packe s/w rw	t errro h/w na  t1 seq h/w na	r in eot default 0x0  uence errror in default 0x0	received packet none eot	description descri	on on OxA00A00B8  OxA00A00B8  OxA00A00BC
regis bits 31:0	err_cou err_cou err_cou	to return captured name nt  seq_err_cnt to return captured name nt  seq_err_cnt to return captured name nt	nt d packe s/w rw d packe s/w rw	t errro h/w na t1 seq h/w na	r in eot default 0x0  uence errror in default 0x0	received packet none eot	description descri	on on OxA00A00B8  OxA00A00B8  OxA00A00BC
regis bits bits bits bits bits bits bits bi	err_cou  22 pkt1_ err_cou  22 pkt2_ err_cou	to return captured name nt  seq_err_cnt to return captured name nt  seq_err_cnt to return captured name nt	nt d packe s/w rw d packe s/w rw	t errro h/w na  t1 seq h/w na	r in eot default 0x0  uence errror in default 0x0  uence errror in default	received packet nonective packet1 not recieved	description descri	on on OxA00A00B8  OxA00A00B8  OxA00A00BC

bits

31:0 err\_count

description

0xA00A00C4

received packet terminated early or lasts longer

register used to return captured packet terminated early or lasts longer than expecte

h/w

na 0x0

default

s/w

rw

name

1.8.25 rx\_fsm\_wdog\_err\_cnt

•	ster used to return receiv	e ism wa	og erri	Or		
bits	name	s/w	h/w	default	descri	•
1:0	err_count	rw	na	0x0	real time receive fsm doesn't re	eturn to idle state within 3ms
8 2	26 pkt2_axis_fsm_v	wdoa e	rr Cr	nt	Reg.	0xA00A00C8
	· ·					
	ster used to return error				packet2 doen't return to idle with	
bits	name	s/w	h/w	default	descri	•
1:0	err_count	rw	na	0x0	pkt2 axis tx fsm didn't return to	idle within valid time 100us
8.2	?7 reserved_byte_e	err ont			Reg.	0xA00A00CC
	ster used to return error	when rece	eived p	_		
bits		s/w	h/w	default	descri	•
1:0	err_count	rw	na	0x0	packet1 zeropad field error cap	oture counter
.8.2	28 pkt2_zeropad_h	dr err	cnt		Reg.	0xA00A00D0
	ster used to return captu			nad field erri	ror	
bits	name	s/w	h/w	default	descri	ntion
1:0	err_count	rw	na	0x0	packet2 zeropad field error cap	•
.8.2	29 tx_fsm_wdog_e	rr cnt			Reg.	0xA00A00D4
	ster used to return transr		log err	ror		
regis bits	eter used to return transr		h/w	default	descri	•
regis bits	ster used to return transr	mit fsm wo			descri real time transmit fsm doesn't r	•
regis bits 1:0	name err_count	mit fsm wo	h/w	default	real time transmit fsm doesn't r	•
bits 1:0	name err_count	nit fsm wo	h/w na	default 0x0		eturn to idle state within 3m
bits 1:0	name err_count  80 pkt1_rx_cnt eter used to return count	s/w rw	h/w na	default 0x0	real time transmit fsm doesn't r	eturn to idle state within 3m
bits 1:0  .8.3 regis	name err_count  80 pkt1_rx_cnt ster used to return count name	s/w rw of packet	h/w na s rece	default 0x0 ived default	real time transmit fsm doesn't r	eturn to idle state within 3m
bits 1:0  .8.3 regis	name err_count  80 pkt1_rx_cnt eter used to return count	s/w rw	h/w na	default 0x0	real time transmit fsm doesn't r	eturn to idle state within 3m
bits 1:0 .8.3 regis bits 1:0	name err_count  80 pkt1_rx_cnt ster used to return count name	s/w rw of packet	h/w na s rece	default 0x0 ived default	real time transmit fsm doesn't r	eturn to idle state within 3m
regis bits 1:0  .8.3 regis bits 1:0	name err_count  80 pkt1_rx_cnt ster used to return count name count	of packet	h/w na s rece h/w na	default 0x0 ived default 0x0	real time transmit fsm doesn't r	eturn to idle state within 3m  0xA00A00D8  ption
bits 1:0  .8.3 regis bits 1:0	name err_count  80 pkt1_rx_cnt eter used to return count name count  81 pkt2_rx_cnt eter used to return count	of packet s/w rw of packet	h/w na s rece h/w na	default 0x0  ived default 0x0	real time transmit fsm doesn't r	eturn to idle state within 3m  0xA00A00D8  ption  0xA00A00DC
regis bits 1:0  .8.3 regis bits 1:0  .8.3 regis bits bits bits bits	name err_count  80 pkt1_rx_cnt eter used to return count name count  81 pkt2_rx_cnt eter used to return count	of packet	h/w na s rece h/w na	default 0x0 ived default 0x0	real time transmit fsm doesn't r	eturn to idle state within 3m  0xA00A00D8  ption  0xA00A00DC
regis bits bits bits bits bits bits bits bi	name err_count  80 pkt1_rx_cnt eter used to return count name count  81 pkt2_rx_cnt eter used to return count name count	of packet s/w rw  of packet s/w rw	h/w na s rece h/w na	ived default 0x0	real time transmit fsm doesn't real time transmit fsm doesn't	eturn to idle state within 3m  0xA00A00D8  ption  0xA00A00DC
regis bits 1:0  .8.3 regis bits 1:0  .8.3 regis bits 1:0	name err_count  30 pkt1_rx_cnt eter used to return count name count  31 pkt2_rx_cnt eter used to return count name count  32 good_pkt1_rx_c	of packet s/w rw  of packet s/w rw  of packet	h/w na s rece h/w na	ived default 0x0	real time transmit fsm doesn't real time transmit fsm doesn't	eturn to idle state within 3m  0xA00A00D8  ption  0xA00A00DC
regis bits 1:0  .8.3 regis bits 1:0  .8.3 regis bits 1:0  .8.3	name err_count  80 pkt1_rx_cnt eter used to return count name count  81 pkt2_rx_cnt eter used to return count name count	of packet s/w rw  of packet s/w rw  of packet	h/w na s rece h/w na	ived default 0x0	real time transmit fsm doesn't real time transmit fsm doesn't	eturn to idle state within 3n  0xA00A00D8  ption  0xA00A00DC
regis bits bits bits bits bits bits bits bi	ster used to return transr name err_count  80 pkt1_rx_cnt ster used to return count name count  81 pkt2_rx_cnt ster used to return count name count  82 good_pkt1_rx_c ster used to return count	of packet s/w rw  of packet s/w rw  of packet	h/w na s rece h/w na	ived default 0x0	real time transmit fsm doesn't real time transmit fsm doesn't	eturn to idle state within 3n  0xA00A00D8  ption  0xA00A00DC  ption  0xA00A00E0

1.8.3	3 good_pkt2_rx_c	Reg.		0xA00A00E4								
regist	register used to return count of packets received											
bits	name	s/w	h/w	default		description	1					
31:0	count	rw	na	0x0	+1 => new packet received							

1.8.3	4 good_pkt2_lost_c	Reg.	0xA00A00E8							
register used to return the count when tsel pkt received is lost due to lack of storage										
bits	name	s/w	h/w	default		description	า			
31:0 lost_cnt rw na 0x0 +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost										

1.9 tselbridge_appl_registers_srdl	Block □T	0xA00A1000 - 0xA00A110F
Register map used to access and control global FPGA functionality		

1.9.1	tselbridge_module_	Reg.		0xA00A1000							
Defin	Defines the module name										
bits	ts name s/w h/w default description										
31:0	module_name	ASCII code for module na	ame - tsel	bridge = tbrg							

1.9.2	tselbridge_modu	le_vers		Reg.	0xA00A1004					
Module version										
bits	bits name s/w h/w default description									
31:16	rfu	ro	na	0x0	Reserver for Futu	Reserver for Future Use - RFU				
15:8	major_revision	ro	wo	0x0	•	Major Revisoin of module - New features or capabilities defi- nition have been added.				
7:0	minor_revision	ro	WO	0x0	Minor Revision of module. This field indicates bug fixes have been applied. For any new features/capabilities increment, this field will reset to zero.					

1.9.3	tselbridge_page_	propert	R	eg.	0xA00A1008					
Address page properties										
bits	name	s/w		description	1					
31	present	ro	WO	0x1	Address page is present if '1', not present when '0'. It is indicating that the logic accessed by this page is avalable/implemented or not.					
30:16	rfu	ro	na	0x0	Reserver for Future	Use - RFU				
15:8	page_size	ro	na	0x1	Address page size: value to 4k and ene		kB, etc. Divide the real			
7:0	unified_header_ rev	ro	na	0x1	Unified Header Forn	mat common re	gisters revision.			

1.9.4	tselbridge_scratchr	Reg.	0xA00A100C								
Scrat	Scratchregister register										
bits name s/w h/w default description											
31:0	scratchregister	SW can write to it	and read from it	for test purposes.							

1.9.5	tselbridge_irq_enal	Reg.	0xA00A1010							
Interrupt Requests Enable/Mask Control Register										
bits	name	s/w	h/w	default		description				
0	0 irq0_enable rw ro 0x0 IRQ0 enable bit. Not implemented here/DTEC									
1	irq1_enable	rw	Not implemented	here/DTEC						

1.9.6	tselbridge_irq_pen	ding	Reg.	0xA00A1014					
Interrupt Pending Status Register									
bits	name	s/w	h/w	default	description				
0	irq0_pending	r/w1c	wo	0x0	IRQ0 pending status bit, sticky interrupt on positive edge. Not				
1	irq1_pending	r/w1c	wo	0x0	IRQ1 pending status bit, sticky interrupt on positive edge. Not				

1.9.7	tselbridge_irq_raw	Reg.	0xA00A1018								
Interrupt Raw Status Register											
bits	name	s/w	h/w	default		description	١				
0	irq0_raw	ro	WO	0x0	IRQ0 raw status bit. Not implemented here/DTEC						
1	irq1_raw	ro	wo	0x0	IRQ1 raw status b	it. Not implement	ed here/DTEC				

1.9.8	tselbridge_irq_forc		Reg.	0xA00A101C				
Interrupt Force Control Register								
bits	name	s/w	h/w	default	description			
0	irq0_force	rw	ro	0x0	IRQ0 force bit. SW implemented here		nulate an interrupt. Not	
1	irq1_force	rw	IRQ1 force bit. SW implemented here		nulate an interrupt. Not			

#### 1.9.9 rt\_data\_handler\_algo\_rx\_stat 0xA00A1060 real time datahandler (combination of real time transmit and receive) status overview, various errors details will be provided here for algo pkt receive fsm bits name h/w default s/w description 0 damp\_algo\_data\_ r/w1c wo 0x0 1 = new data arrived while sending the old damp algo data and the damp algo data is lost as there is no internal fifo lost 1 rx\_fsm\_eth\_lgth r/w1c 0x01 = pkt size doesn't match the expected size of the pkt /0 = wo \_field\_err received packet with expected data in length filed. 2 1 = received a packet with pload type which is not 0x18 rx\_fsm\_pload\_er r/w1c wo 0x0(DAMP sends DTEC) /0 = received packet with expected data in pload type field. 3 rx\_fsm\_eot\_err r/w1c wo 0x0 1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field. 4 rx\_fsm\_reserved 0x0 20th byte of the pkt rx from damp through tsel is reserved r/w1c wo \_byte\_err and is zero. 1=reserved byte mismatch 5 rx\_fsm\_eop\_er r/w1c 0x0 1 = tlast is received at unexpected byte position/0 = rewo ceived a right size packet. 1 = link loss/0 = link is established. GDB link status 6 link\_loss r/w1c wo 0x0 7 damp\_algo\_seq\_e r/w1c wo 0x0 1 = damp algo pkt numbers are not in order 8 0x0 1 = pkt received is not a known type unknown\_pkt\_hdr r/w1c wo \_err 9 1 = the fifo that receives the good 512 bytes of algo data is nonpkt\_mode\_fif r/w1c 0x0 wo full. o\_full 10 damp\_algo\_rx\_rd r/w1c 0x01 = when a valid damp algo data is available to be transmitwo ted and dtec simulink algo is not ready to receive within 2ms y\_wdog\_err 11 damp\_algo\_rx\_fs r/w1c 0x0 1 = receive fsm that receives the algo pkt doesn't return to wo m\_wdog\_err the idle state with in 3msec 15:12 rx\_fsm\_reserved r/w1c wo 0x0 3 bits reserved for receive fsm future use

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for boot receive fsm

bits	name	s/w	h/w	default	description
0	boot_data_lost	r/w1c	WO	0x0	1 = new data arrived while sending the old boot data and the damp boot data is lost as there is no internal fifo
1	rx_fsm_eth_lgth _field_err	r/w1c	wo	0x0	1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed.
2	rx_fsm_pload_er r	r/w1c	WO	0x0	1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field.
3	rx_fsm_eot_err	r/w1c	WO	0x0	1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field.
4	zeropad_err	r/w1c	wo	0x0	1 = zero padding error detected on the packet received
5	rx_fsm_reserved _byte_err	r/w1c	WO	0x0	20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch
6	rx_fsm_eop_er	r/w1c	wo	0x0	1 = tlast is received at unexpected byte position/0 = received a right size packet.
7	link_loss	r/w1c	wo	0x0	1 = link loss/0 = link is established. GDB link status
8	boot_seq_err	r/w1c	wo	0x0	1 = damp boot pkt numbers are not in order
9	boot_seg_seq_er r	r/w1c	WO	0x0	1 = damp boot segments (fragment pkt numbers) are not in order/sop err/eop err
10	unknown_pkt_hdr _err	r/w1c	wo	0x0	1 = pkt received is not a known type
11	nonpkt_mode_fif o_full	r/w1c	wo	0x0	1 = the fifo that receives the good 1024 bytes boot data from packet mode fifo is full.
12	pkt_mode_fifo_f ull	r/w1c	wo	0x0	1 = the fifo that receives the boot data from unifed TSEL IF is full. pkt mode is enabled for this fifo
13	boot_rx_fsm_wdo g_err	r/w1c	wo	0x0	1 = receive fsm that receives the boot pkt doesn't return to the idle state with in 3msec
14	sop_err	r/w1c	WO	0x0	1 = the boot pkt received has sop error => sop not set on 1st pkt or set on last pkt
15	eop_err	r/w1c	WO	0x0	1 = the boot pkt received has eop error => eop not set on last pkt
16	seg_seq_out_of_ order	r/w1c	WO	0x0	1 = boot segments (fragment pkt numbers) are not in order
31:17	rx_fsm_reserved	r/w1c	wo	0x0	15 bits reserved for receive fsm future use

## 1.9.11 rt\_data\_handler\_diag\_rx\_stat

Reg.

0xA00A1068

real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for diag receive fsm

bits	name	s/w	h/w	default	description
0	diag_data_lost	r/w1c	WO	0x0	1 = new data arrived while sending the old diag data and the damp diag data is lost as there is no internal fifo
1	rx_fsm_eth_lgth _field_err	r/w1c	wo	0x0	1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed.
2	rx_fsm_pload_er r	r/w1c	WO	0x0	1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field.
3	rx_fsm_eot_err	r/w1c	wo	0x0	1 = received a packet with eot field not equal to $0xA5/0$ = received packet with expected data in eot header field.
4	zeropad_err	r/w1c	wo	0x0	1 = zero padding error detected on the packet received
5	rx_fsm_reserved _byte_err	r/w1c	wo	0x0	20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch
6	rx_fsm_eop_er	r/w1c	wo	0x0	1 = tlast is received at unexpected byte position/0 = received a right size packet.
7	link_loss	r/w1c	wo	0x0	1 = link loss/0 = link is established. GDB link status
8	diag_seq_err	r/w1c	wo	0x0	1 = damp diagnostics pkt numbers are not in order
9	diag_seg_seq_er r	r/w1c	wo	0x0	1 = damp diag segments (fragment pkt numbers) are not in order/sop err/eop err
10	unknown_pkt_hdr _err	r/w1c	wo	0x0	1 = pkt received is not a known type
11	nonpkt_mode_fif o_full	r/w1c	WO	0x0	1 = the fifo that receives the good 512 bytes diag data from packet mode fifo is full.

12	pkt_mode_fifo_f ull	r/w1c	WO	0x0	1 = the fifo that receives the diag data from unifed TSEL IF is full. pkt mode is enabled for this fifo
13	diag_rx_fsm_wdo g_err	r/w1c	wo	0x0	1 = receive fsm that receives the diag pkt doesn't return to the idle state with in 3msec
14	sop_err	r/w1c	wo	0x0	1 = the diag pkt received has sop error => sop not set on 1st pkt or set on last pkt
15	eop_err	r/w1c	wo	0x0	1 = the diag pkt received has eop error => eop not set on last pkt
16	seg_seq_out_of_ order	r/w1c	wo	0x0	1 = diag segments (fragment pkt numbers) are not in order
31:17	rx_fsm_reserved	r/w1c	wo	0x0	15 bits reserved for receive fsm future use

#### 0xA00A106C Reg. 1.9.12 rt\_data\_handler\_wfm\_reg\_rx\_stat real time datahandler (combination of real time transmit and receive) status overview. various errors details will be provided here for wfm reg pkt name s/w h/w default description wfm\_reg\_data\_lo r/w1c wo 0x0 1 = new data arrived while sending the old wfm reg data and the damp wfm reg data is lost as there is no internal fifo 1 rx fsm eth lgth r/w1c wo 0x0 1 = pkt size doesn't match the expected size of the pkt /0 = field err received packet with expected data in length filed. 2 rx\_fsm\_pload\_er r/w1c wo 0x0 1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field. 3 1 = received a packet with eot field not equal to 0xA5/0 = rerx\_fsm\_eot\_err r/w1c 0x0wo ceived packet with expected data in eot header field. 1 = zero padding error detected on the packet received 4 0x0zeropad err r/w1c wο 20th byte of the pkt rx from damp through tsel is reserved 5 rx fsm reserved r/w1c 0x0WΩ byte err and is zero. 1=reserved byte mismatch r/w1c 6 0x01 = tlast is received at unexpected byte position/0 = rerx\_fsm\_eop\_er WΩ ceived a right size packet. 7 1 = link loss/0 = link is established. GDB link status link loss r/w1c wo 0x0 8 wfm reg seg err r/w1c wo 0x0 1 = damp waveform register pkt numbers are not in order wfm\_reg\_seg\_seq 9 r/w1c wo 0x0 1 = damp waveform register segments (fragment pkt numerr bers) are not in order 10 1 = pkt received is not a known type unknown\_pkt\_hdr r/w1c wo 0x0 err 11 nonpkt\_mode\_fif 0x0 1 = the fifo that receives the good 512 bytes wfm reg data r/w1c wο o\_full from packet mode fifo is full. 12 pkt\_mode\_fifo\_f r/w1c 0x0 1 = the fifo that receives the diag data from unifed TSEL IF wo ull is full, pkt mode is enabled for this fifo 13 wfm\_reg\_rx\_fsm\_ r/w1c wo 0x0 1 = receive fsm that receives the wfm reg pkt doesn't return wdog\_err to the idle state with in 3msec 14 sop\_err r/w1c wo 0x0 1 = the diag pkt received has sop error => sop not set on 1st pkt or set on last pkt 15 1 = the diag pkt received has eop error => eop not set on eop\_err r/w1c wo 0x0last pkt 16 0x0 1 = diag segments (fragment pkt numbers) are not in order seg\_seq\_out\_of\_ r/w1c WO order 31:17 rx\_fsm\_reserved wo 0x0 15 bits reserved for receive fsm future use r/w1c

1.9.1	3 rt_data_handler_v	ol_wf	m_sa	amp_rx_sta	at	Reg.	0xA00A1070
	me datahandler (combina here for wfm samp receiv		real tin	ne transmit an	d receive) status o	verview. various e	errors details will be pro-
bits	name	s/w	h/w	default		description	)
0	vol_wfm_samp_da ta_lost	r/w1c	WO	0x0		he damp voltage	the old voltage wfm wfm sample data is lost
1	rx_fsm_eth_lgth _field_err	r/w1c	wo	0x0	1 = pkt size doesn received packet w		ected size of the pkt /0 =
2	rx_fsm_pload_er r	r/w1c	WO	0x0		EC) $/0 = received$	pe which is not 0x18 packet with expected

3	rx_fsm_eot_err	r/w1c	WO	0x0	1 = received a packet with eot field not equal to 0xA5/0 = received packet with expected data in eot header field.
4	zeropad_err	r/w1c	wo	0x0	1 = zero padding error detected on the packet received
5	rx_fsm_reserved _byte_err	r/w1c	wo	0x0	20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch
6	rx_fsm_eop_er	r/w1c	wo	0x0	1 = tlast is received at unexpected byte position/0 = received a right size packet.
7	link_loss	r/w1c	wo	0x0	1 = link loss/0 = link is established. GDB link status
8	wfm_samp_seq_er r	r/w1c	wo	0x0	1 = damp waveform sample pkt numbers are not in order
9	wfm_samp_seg_ou t_of_order	r/w1c	wo	0x0	1 = damp voltage waveform sample segments (fragment pkt numbers) are not in order
10	vol_wfm_samp_se g_seq_err	r/w1c	wo	0x0	1 = damp voltage waveform sample segments (fragment pkt numbers) are not in order/sop err/ eop err
11	unknown_wfm_sam p_err	r/w1c	wo	0x0	1 = damp waveform sample received is neither voltage nor current
12	unknown_pkt_hdr _err	r/w1c	wo	0x0	1 = pkt received is not a known type
13	nonpkt_mode_fif o_full	r/w1c	wo	0x0	1 = the fifo that receives the good 16384 vol data from packet mode fifo is full.
14	pkt_mode_fifo_f ull	r/w1c	wo	0x0	1 = the fifo that receives the vol data from unifed TSEL IF is full. pkt mode is enabled for this fifo
15	vol_wfm_samp_rx _fsm_wdog_err	r/w1c	wo	0x0	1 = receive fsm that receives the vol wfm samp pkt doesn't return to the idle state with in 3msec
16	amp_wfm_samp_so p_err	r/w1c	wo	0x0	1 = the amp wfm samp pkt received has sop error => sop not set on 1st pkt or set on last pkt
17	amp_wfm_samp_eo p_err	r/w1c	wo	0x0	1 = the amp wfm samp pkt received has eop error => eop not set on last pkt
31:18	reserved	r/w1c	wo	0x0	reserved for future use

real t		nation of r		•	nd receive) status overview. various errors details will be pro-
bits	here for wfm samp recently name	s/w	h/w	default	description
0	amp_wfm_samp_da ta_lost	r/w1c	WO	0x0	1 = new data arrived while sending the old current wfm sample data and the damp current wfm sample data is lost as there is no internal fifo
1	rx_fsm_eth_lgth _field_err	r/w1c	wo	0x0	1 = pkt size doesn't match the expected size of the pkt /0 = received packet with expected data in length filed.
2	rx_fsm_pload_er r	r/w1c	WO	0x0	1 = received a packet with pload type which is not 0x18 (DAMP sends DTEC) /0 = received packet with expected data in pload type field.
3	rx_fsm_eot_err	r/w1c	WO	0x0	1 = received a packet with eot field not equal to 0xA5/0 = re ceived packet with expected data in eot header field.
4	zeropad_err	r/w1c	wo	0x0	1 = zero padding error detected on the packet received
5	rx_fsm_reserved _byte_err	r/w1c	wo	0x0	20th byte of the pkt rx from damp through tsel is reserved and is zero. 1=reserved byte mismatch
6	rx_fsm_eop_er	r/w1c	wo	0x0	1 = tlast is received at unexpected byte position/0 = received a right size packet.
7	link_loss	r/w1c	wo	0x0	1 = link loss/0 = link is established. GDB link status
8	wfm_samp_seq_er r	r/w1c	wo	0x0	1 = damp waveform sample pkt numbers are not in order
9	wfm_samp_seg_se q_out_of_order	r/w1c	wo	0x0	1 = damp current waveform sample segments (fragment pkinumbers) are not in order
10	amp_wfm_samp_se g_seq_err	r/w1c	WO	0x0	1 = damp current waveform sample segments (fragment pki numbers) are not in order/eop not set for last pkt/sop not set for 1st pkt
11	unknown_wfm_sam p_err	r/w1c	wo	0x0	1 = damp waveform sample received is neither voltage nor current
12	unknown_pkt_hdr _err	r/w1c	wo	0x0	1 = pkt received is not a known type
13	nonpkt_mode_fif o_full	r/w1c	WO	0x0	1 = the fifo that receives the good 16384 amp data from packet mode fifo is full.
14	pkt_mode_fifo_f ull	r/w1c	WO	0x0	1 = the fifo that receives the amp data from unifed TSEL IF is full. pkt mode is enabled for this fifo

15	amp_wfm_samp_rx _fsm_wdog_err	r/w1c	wo	0x0	1 = receive fsm that receives the amp wfm samp pkt doesn't return to the idle state with in 3msec
16	amp_wfm_samp_so p_err	r/w1c	wo	0x0	1 = the amp wfm samp pkt received has sop error => sop not set on 1st pkt or set on last pkt
17	amp_wfm_samp_eo p_err	r/w1c	wo	0x0	1 = the amp wfm samp pkt received has eop error => eop not set on last pkt
31:18	reserved	r/w1c	wo	0x0	reserved for future use

1.9.1	5 rt_data_handler	_tx_stat			0xA00A1078
	ime datahandler (comb here. the tranmit fsm t				nd receive) status overview. various errors details will be pro- nd ctrl data pkt
bits	name	s/w	h/w	default	description
0	link_loss	r/w1c	wo	0x0	1 = link loss/0 = link is established. depulicated the GDB link status. can also be found at rt_data_handler_rx_stat register
1	tx_fsm_algo_fif o_full	r/w1c	WO	0x0	1 = the fifo connected to the unified tsel interface that is receiving dtec2damp simulink algo data pkt from transmit state machine is full (data is still written to the fifo even its full) /0 = fifo is not full
2	tx_fsm_dtec_alg o_wdog_err	r/w1c	WO	0x0	1 = the fsm that recives dtec algo data from dtec simulink algo doesn't return back to idle within 3ms(dtec alog packet not recived from dtec simulink algo with in 3ms after after tvalid goes high initially)/0 = after initial tvalid, tlast is seen within 3ms
3	tx_fsm_dtec_alg o_data_err	r/w1c	wo	0x0	1 = dtec algo data with unexpected size received
4	tx_fsm_dtec_agl o_fifo_rx_rdy_e rr	r/w1c	WO	0x0	1 = the fifo that receiving the dtec algo pkt is not ready for some reason while a part of data is received
7:5	tx_fsm_dtec_alg o_reserved	r/w1c	wo	0x0	status bits reserved for dtec algo tx fsm
8	link_loss_dup	r/w1c	wo	0x0	1 = link loss/0 = link is established. depulicated the GDB link status. can also be found at rt_data_handler_rx_stat register
9	tx_fsm_ctrl_fif o_full	r/w1c	WO	0x0	1 = the fifo connected to the unified tsel interface that is receiving dtec2damp ctrl data pkt from transmit state machine is full (data is still written to the fifo even its full) /0 = fifo is not full
10	tx_fsm_dtec_ctr l_wdog_err	r/w1c	wo	0x0	1 = the fsm that transmits the ctrl data pkt doesn't return back to idle within 3ms
11	tx_fsm_ctrl_fif o_rx_rdy_err	r/w1c	WO	0x0	1 = the fifo that receiving the ctrl pkt is not ready for some reason while a part of data is received
15:12	tx_fsm_ctrl_res erved	r/w1c	WO	0x0	status bits reserved for control pkt tx fsm

1.9.16	6 ps_por_b					Reg.	0xA00A107C
issue	external por						
bits	name	s/w	h/w	default		description	า
0	external_reset	rw	ro	0x0	1 => issue externa	al reset to DAMP	using control data pkt

1.9.17	7 ps_srst_b					Reg.	0xA00A1080
issue	remote system reset						
bits	name	s/w	h/w	default		description	٦
0	remote_reset	rw	ro	0x0	1 => issue remote	e reset to DAMP u	sing control data pkt

1.9.18	enb_wfm_cap			Reg.	0xA00A1084
enables	the waveform capture				
bits	name	s/w h/w d	efault	description	)

	waveform_cap	rw	ro	0x0	1 => DAMP waveform cap trol data pkt	pture feature is enabled using con
1.9.1	9 direct_boot_offs	et_set			Reg.	0xA00A1088
boot	offset settings					
bits	name	s/w	h/w	default		description
31:0	boot_offset	rw	ro	0x0	32 bit boot offset for DAM	•
1.9.2	0 cntrl_pkt_rate_ct	trl			Reg.	0xA00A108C
Cont	rol packet rate control re	gister				
bits	name	s/w	h/w	default		description
31:0	rate_ctrl	rw	ro	0x3B9ACA0	32 bit rate control register value is 1sec. Clk used =	for Control data packet. Default 125MHz
	d also data social	fueres	t		Rea	0xA00A1090
	1 algo_data_good_				Reg.	074004 1030
	ter used to return the cou					
bits	name	s/w	h/w	default		description
1:0	good_cnt	rw	na	0x0	+1 => the ism that recives	s the data, detected a good frame
9.2	2 algo_data_bad_f	rame (	nt		Reg.	0xA00A1094
	ter used to return the cou			nes recoived	******	5.3 (00) (100 1
						da a aviatia a
bits 31:0	name bad_cnt	s/w rw	h/w na	default 0x0		description sthe data, detected a bad frame
.9.2	3 goodalgo_tsel_p	kt_lost	_cnt		Reg.	0xA00A1098
					ost due to lack of storage	
regis	ter used to return the co	unt when	tsel p	kt received is i	oot add to lack of otorago	
regis bits	ter used to return the countries name	unt when s/w	tsel p h/w	default	C	description
					C	description d but can't be processed so, the
bits	name	s/w	h/w	default	+1 = new TSEL pkt arrive	•
bits 31:0	name	s/w rw	h/w na	default	+1 = new TSEL pkt arrive	•
bits 31:0	name lost_cnt	s/w rw	h/w na _cnt	default 0x0	+1 = new TSEL pkt arrive data pkt is lost	d but can't be processed so, the
bits 31:0	name lost_cnt 4 boot_data_good_	s/w rw	h/w na _cnt	default 0x0	+1 = new TSEL pkt arrive data pkt is lost	d but can't be processed so, the
bits 31:0	name lost_cnt  4 boot_data_good_ ter used to return the cou	s/w rw  frame unt for go	h/w na nacnt	default 0x0	+1 = new TSEL pkt arrive data pkt is lost	0xA00A109C
bits 31:0 1.9.2 regis bits 31:0	name lost_cnt  4 boot_data_good_ ter used to return the couname good_cnt	_frame_ unt for go	h/w na  _cnt ood fra h/w na	default 0x0  mes received default	+1 = new TSEL pkt arrive data pkt is lost  Reg.  +1 => the fsm that recives	0xA00A109C  description s the data, detected a good frame
bits 11:0  1.9.2 regis bits 11:0	name lost_cnt  4 boot_data_good_ ter used to return the couname good_cnt  5 boot_data_bad_f	s/w rw  frame unt for go s/w rw	h/w na  cnt ood fra h/w na	default 0x0  mes received default 0x0	+1 = new TSEL pkt arrive data pkt is lost	0xA00A109C
bits s1:0	name lost_cnt  4 boot_data_good_ ter used to return the couname good_cnt	s/w rw  frame unt for go s/w rw	h/w na  cnt ood fra h/w na	default 0x0  mes received default 0x0	+1 = new TSEL pkt arrive data pkt is lost  Reg.  +1 => the fsm that recives	0xA00A109C  description s the data, detected a good frame
bits 51:0 l.9.2 regis bits 11:0 l.9.2 regis bits	name lost_cnt  4 boot_data_good_ ter used to return the core	s/w rw  frame unt for go s/w rw  frame_ount for bases/w	cnt ood fra h/w na	default 0x0  mes received default 0x0  nes received default	+1 = new TSEL pkt arrive data pkt is lost  Reg.  +1 => the fsm that recives	0xA00A109C  description s the data, detected a good frame  0xA00A10A0
bits 51:0 l.9.2 regis bits 11:0 l.9.2 regis bits	name lost_cnt  4 boot_data_good_ ter used to return the count of the c	s/w rw  frame unt for go s/w rw  frame_unt for ba	h/w na  cnt ood fra h/w na	default 0x0  mes received default 0x0	+1 = new TSEL pkt arrive data pkt is lost  Reg.  +1 => the fsm that recives	d but can't be processed so, the  0xA00A109C  description s the data, detected a good frame
bits 51:0  1.9.2  regis bits 11:0  1.9.2  regis bits 11:0	name lost_cnt  4 boot_data_good_ ter used to return the core	s/w rw  frame unt for go s/w rw  frame_ount for ba s/w rw	cnt ood fra h/w na	default 0x0  mes received default 0x0  nes received default	+1 = new TSEL pkt arrive data pkt is lost  Reg.  +1 => the fsm that recives	0xA00A109C  description s the data, detected a good frame  0xA00A10A0
bits 1:0  1.9.2 regis bits 1:0  1.9.2 1.9.2 1.9.2	name lost_cnt  4 boot_data_good_ ter used to return the conname good_cnt  5 boot_data_bad_f ter used to return the conname bad_cnt	s/w rw  frame unt for go s/w rw  frame_ount for ba s/w rw	cnt ood fra h/w na cnt d fram h/w na	default 0x0  mes received default 0x0  nes received default 0x0	+1 = new TSEL pkt arrive data pkt is lost  Reg.  Reg.  Reg.  Reg.  Reg.	OxA00A109C  description s the data, detected a good frame  0xA00A10A0  description s the data, detected a bad frame
bits 31:0  1.9.2 regis bits 31:0  1.9.2 1.9.2 1.9.2	name lost_cnt  4 boot_data_good_ ter used to return the conname good_cnt  5 boot_data_bad_f ter used to return the conname bad_cnt	s/w rw  frame unt for go s/w rw  frame_ount for ba s/w rw	cnt ood fra h/w na cnt d fram h/w na	default 0x0  mes received default 0x0  nes received default 0x0	+1 = new TSEL pkt arrive data pkt is lost  Reg.  +1 => the fsm that recives  +1 => the fsm that recives	OxA00A109C  description s the data, detected a good frame  0xA00A10A0  description s the data, detected a bad frame

1.9.2	7 diag_data_good_f	rame	_cnt		Reg. Ox	A00A10A8
regist	ter used to return the cour	nt for go	od fra	mes received		
bits	name	s/w	h/w	default	description	
31:0	good_cnt	rw	na	0x0	+1 => the fsm that recives the data, de	etected a good frame
1 0 2	8 diag_data_bad_fra	ame (	nt		Reg. Ox	:A00A10AC
	ter used to return the cour				d windi	
bits 31:0	name bad_cnt	s/w rw	h/w na	default 0x0	description +1 => the fsm that recives the data, do	etected a had frame
01.0	baa_ont	1 44	Πα	OXO	11 => the familiat receives the data, as	ciccica a baa mame
100						10011000
1.9.2	9 diag_tsel_pkt_los	t_cnt			Reg. Ox	:A00A10B0
regist	ter used to return the cour	nt when	tsel p	kt received is	lost due to lack of storage	
bits	name	s/w	h/w	default	description	
31:0	lost_cnt	rw	na	0x0	+1 = new TSEL pkt arrived but can't b data pkt is lost	e processed so, the
102	0 wfm_reg_data_go	od fr	amo	cnt	Reg. Ox	:A00A10B4
_	ter used to return the cour					
bits 31:0	name good_cnt	s/w rw	h/w na	default 0x0	description +1 => the fsm that recives the data, do	ataatad a good from
1.9.3	1 wfm_reg_data_ba	d_fra	me_c	ent	Reg. Ox	A00A10B8
	1 wfm_reg_data_bater used to return the cour				Reg. Ox	A00A10B8
regist	ter used to return the cour			nes received default	description	
regist	ter used to return the cour	nt for ba	ad fran	nes received	MARAM -	
regist	ter used to return the cour	nt for ba	ad fran	nes received default	description	
regist bits 31:0	ter used to return the cour	s/w rw	h/w na	nes received default	description +1 => the fsm that recives the data, do	
bits 31:0	name bad_cnt  2 wfm_reg_tsel_pkt	s/w rw	h/w na	default 0x0	description +1 => the fsm that recives the data, do	etected a bad frame
bits 31:0	name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour	s/w rw	h/w na cnt	default 0x0	description +1 => the fsm that recives the data, do	etected a bad frame
regist bits 31:0  1.9.3 regist bits	name bad_cnt  2 wfm_reg_tsel_pkt	s/w rw	h/w na	default 0x0	description +1 => the fsm that recives the data, do	etected a bad frame
bits 31:0  1.9.3 regist	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name	s/w rw  lost_ nt when s/w	h/w na  cnt tsel p	default 0x0  kt received is default	description +1 => the fsm that recives the data, do  Reg. 0x  lost due to lack of storage  description	etected a bad frame
bits 31:0  1.9.3 regist	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name	s/w rw  lost_ nt when s/w	h/w na  cnt tsel p	default 0x0  kt received is default	description +1 => the fsm that recives the data, do  Reg. 0x lost due to lack of storage  description +1 = new TSEL pkt arrived but can't b	etected a bad frame
bits 31:0 1.9.3 regist bits 31:0	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name	s/w rw lost_ nt when s/w rw	h/w na cnt tsel p h/w na	default 0x0  kt received is default 0x0	description +1 => the fsm that recives the data, do  Reg.  Ox  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't b data pkt is lost	etected a bad frame
regist bits 31:0 1.9.3 regist bits 31:0	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name lost_cnt	s/w rw lost_ nt when s/w rw	h/w na  cnt tsel p h/w na	default 0x0  kt received is default 0x0  frame_cnt	description +1 => the fsm that recives the data, do  Reg.  Ox  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't b data pkt is lost	etected a bad frame A00A10BC e processed so, the
regist bits 31:0 1.9.3 regist bits 31:0	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name lost_cnt  3 vol_wfm_samp_da	s/w rw lost_ nt when s/w rw	h/w na  cnt tsel p h/w na	default 0x0  kt received is default 0x0  frame_cnt	description +1 => the fsm that recives the data, do  Reg.  Ox  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't b data pkt is lost	etected a bad frame A00A10BC e processed so, the
regist bits 31:0  1.9.3 regist bits 31:0	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name lost_cnt  3 vol_wfm_samp_dater used to return the cour	s/w rw  lost_ nt when s/w rw  ata_g nt for go	cnt tsel p h/w na	default 0x0  kt received is default 0x0  frame_cnt mes received	description +1 => the fsm that recives the data, do  Reg.  Ox  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't b data pkt is lost  Reg.  Ox	etected a bad frame A00A10BC e processed so, the
regist bits 31:0  1.9.3 regist bits 31:0  1.9.3 regist bits	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name lost_cnt  3 vol_wfm_samp_dater used to return the cour name	s/w rw  lost_ nt when s/w rw  ata_g nt for go	h/w na  cnt tsel p h/w na  ood ood h/w	default 0x0  kt received is default 0x0  frame_cnt mes received default	description +1 => the fsm that recives the data, do  Reg.  Ox  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't b data pkt is lost  Reg.  Ox  description	etected a bad frame A00A10BC e processed so, the
regist bits 31:0  1.9.3 regist bits 31:0  1.9.3 regist bits 31:0	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name lost_cnt  3 vol_wfm_samp_dater used to return the cour name good_cnt	lost_nt when s/w rw  ata_g  t for go	cnt tsel p h/w na  cod_ h/w na  cod_ h/w na	default 0x0  kt received is default 0x0  frame_cnt mes received default 0x0	description +1 => the fsm that recives the data, do  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't be data pkt is lost  description  description +1 => the fsm that recives the data, do	etected a bad frame A00A10BC e processed so, the
regist bits 31:0 1.9.3 regist bits 31:0 1.9.3 1.9.3	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name lost_cnt  3 vol_wfm_samp_dater used to return the cour name good_cnt	lost_nt when s/w rw ata_g tf for go s/w rw	cnt tsel p h/w na  cod_ h/w na  ad_fr	default 0x0  kt received is default 0x0  frame_cnt mes received default 0x0	description +1 => the fsm that recives the data, do  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't be data pkt is lost  description  description +1 => the fsm that recives the data, do	etected a bad frame A00A10BC e processed so, the A00A10C0 etected a good frame
regist bits 31:0 1.9.3 regist bits 31:0 1.9.3 1.9.3	rer used to return the cour name bad_cnt  2 wfm_reg_tsel_pkt ter used to return the cour name lost_cnt  3 vol_wfm_samp_dater used to return the cour name good_cnt	lost_nt when s/w rw ata_g tf for go s/w rw	cnt tsel p h/w na  cod_ h/w na  ad_fr	default 0x0  kt received is default 0x0  frame_cnt mes received default 0x0	description +1 => the fsm that recives the data, do  lost due to lack of storage  description +1 = new TSEL pkt arrived but can't be data pkt is lost  description  description +1 => the fsm that recives the data, do	etected a bad frame A00A10BC e processed so, the A00A10C0 etected a good frame

1.9.3	5 vol_wfm_samp_ts	Reg.	0xA00A10C8							
register used to return the count when tsel pkt received is lost due to lack of storage										
bits	name	s/w	h/w	default		description	n			
31:0	lost_cnt rw na 0x0 +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost									

1.9.36 amp_wfm_samp_data_good_frame_cnt 0xA00A10CC											
regist	register used to return the count for good frames received										
bits	bits name s/w h/w default description										
31:0 good_cnt rw na 0x0 +1 => the fsm that recives the data, detected a good											

1.9.37 amp_wfm_samp_data_bad_frame_cnt 0xA00A10D0											
regist	register used to return the count for bad frames received										
bits	bits name s/w h/w default description										
31:0 bad_cnt rw na 0x0 +1 => the fsm that recives the data, detected a bad frame											

1.9.38	8 amp_wfm_samp_t	Reg.	0xA00A10D4								
regist	register used to return the count when tsel pkt received is lost due to lack of storage										
bits	name	s/w	h/w	default		description	า				
31:0	31:0 lost_cnt rw na 0x0 +1 = new TSEL pkt arrived but can't be processed so, the data pkt is lost										

1.9.3	9 wfm_samp_data_b	Reg.	0xA00A10D8									
regist	register used to return the count for bad frames received											
bits	bits name s/w h/w default description											
31:0	bad_cnt	t recives the data	, detected a bad frame									

1.9.4	0 unknown_pkt_cnt	Reg.	0xA00A10DC								
regist	register used to return the count of unknown packets received										
bits	name	s/w	h/w	default		description	า				
31:0	31:0 rx_cnt rw na 0x0 +1 => the fsm that recives the data, detected an unknown packet										

1.9.4	1 boot_data_sop_er	Reg.	0xA00A10E0								
regist	register used to return the count of sop errors received										
bits	name	s/w	h/w	default		description	า				
31:0 err_cnt rw na 0x0 +1 => the fsm that recives the data, detected sop not set on 1st pkt or set on last pkt											

1.9.4	2 boot_data_eop_er	Reg.	0xA00A10E4							
register used to return the count of eop err received										
bits	name	s/w	h/w	default		description	1			
31:0	err_cnt	rw	na	0x0	+1 => the fsm tha last pkt	t recives the data	, detected eop not set on			

1.9.4	3 boot_data_seg_oเ	Reg.	0xA00A10E8								
regist	register used to return the count of frames received out of order										
bits	name	s/w	h/w	default		description	٦				
31:0	rx_cnt	rw	na	0x0	+1 => the fsm that recives the data, detected segment of frames with pkt seq error						

1.9.4	4 diag_data_sop_er	Reg.	0xA00A10EC								
regist	register used to return the count of sop errors received										
bits	name	s/w	h/w	default		description	า				
31:0 err_cnt rw na 0x0 +1 => the fsm that recives the data, detected sop not set of 1st pkt or set on last pkt											

1.9.4	5 diag_data_eop_er	Reg.	0xA00A10F0								
regist	register used to return the count of eop err received										
bits	name	s/w	h/w	default		description	า				
31:0 err_cnt rw na 0x0 +1 => the fsm that recives the data, detected eop not set of last pkt											

1.9.4	6 diag_data_seg_ou	Reg.	0xA00A10F4					
register used to return the count of frames received out of order								
bits	name	s/w	h/w	default		description	า	
31:0 rx_cnt rw na 0x0 +1 => the fsm that recives the data, detected segment of frames with pkt seq error						, detected segment of		

1.9.4	7 amp_wfm_samp_s	Reg.	0xA00A10F8					
register used to return the count of sop errors received								
bits	name	s/w	h/w	default		description	n	
31:0 err_cnt rw na 0x0 +1 => the fsm that recives the data, detected sop not se 1st pkt or set on last pkt							, detected sop not set on	

1.9.4	8 amp_wfm_samp_e	Reg.	0xA00A10FC					
register used to return the count of eop err received								
bits	name	s/w	h/w	default		description	١	
31:0	err_cnt	rw na 0x0 +1 => the fsm that recives the data, detected eop not set last pkt					, detected eop not set on	

1.9.4	9 amp_wfm_samp_s	Reg.	0xA00A1100					
register used to return the count of frames received out of order								
bits	name	s/w	h/w	default		description	า	
31:0 rx_cnt rw na 0x0 +1 => the fsm that recives the data, detected segment of frames with pkt seq error							, detected segment of	

1.9.5	0 vol_wfm_samp_s	Reg.	0xA00A1104					
register used to return the count of sop errors received								
bits	name	s/w	h/w	default		description	n	
31:0	err_cnt	rw	na	0x0 +1 => the fsm that recives the data, detected sop not set of 1st pkt or set on last pkt				

1.9.5	1 vol_wfm_samp_ed	Reg.	0xA00A1108						
regist	register used to return the count of eop err received								
bits	name	s/w	h/w	default		description	n		
31:0	err_cnt	rw	na	0x0	+1 => the fsm that recives the data, detected eop not selast pkt				

1.9.5	2 vol_wfm_samp_se	Reg.	0xA00A110C						
register used to return the count of frames received out of order									
bits	name	s/w	h/w	default		description	n		
31:0	rx_cnt	rw	na	0x0	+1 => the fsm that recives the data, detected segment of frames with pkt seq error				

1.10 ipi_scratchpad	Block	0xA00C0000 - 0xA00FFFFF
Scratchpad RAM		

1.10.1 ram_256	kb_inst	ram_256	6kb_inst						0xA00C0000, 0xA00C0004 0xA00FFFF
offset	de	epth 6	5536	width	32	defa	ault	0x0	

1.11 esm_common_registers	Block	0xA0210000 - 0xA021171F
Register map used for ESMI_IF access		

1.11.1 esmi\_ctl1 0xA0210000

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name		h/w	default	E	description	
15	ce	ro	wo	0x0	-		ed message. 1 = error
14	fe	ro	WO	0x0	error		ceived message. 1 =
13	iatmo	rw	wo	0x0	1 = Indirect addressed Sequence complete		out after 50 ms. 0 =
12	iardy	ro	WO	0x0	= Command write	es will be ignored.	for new command. 0
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.		
10	to	rw	ro	0x0	Enables tref overide: used to ignore TREF signal to allow multiple read/writes Indicates when a receive message is in the ESM_DAT reg-		
9	rx	ro	wo	0x0	ister. 1 = messag	e available	_
8	tx	ro	wo	0x0	e.g., when the Co	rites to this register ommand FIFO, which er writes, is full. 1 = v	
7	es	rw	rw	0x0	Force energy sar forced, regardles	nple. One energy int s of the fire enable s	egration shot will be tate. Cleafred by HW.
6:5	tr	mar	ro	0x0	1 = force energy		nergy integration (and
0.5	u	rw	ro	OXO	waveform capture ured for TR1/TR0	e) cycles. Note that i 0 = 11, then all ESMs	f any ESM is config- s will begin their wave- MAP4 HOP mode oper-
					enum:esm_ctl_t	r_encoding	
					Name	Value	Description
					enc0	0	normal T0 o
							peration (T
							0 used as s
					4	4	ource)
					enc1	1	Reserved us ed by CTEC
							Operation
					enc2	2	normal MAP4
							operation
							(droplet de
							tection use
							d as source
							)
					enc3	3	enhanced MA P4 operatio
							n (HOP mode
							- see MAP4
							HOP regist
							er below)
4	fa	rw	ro	0x0		ies a fast ESM. It wi	
						rror if it does not deli	
							Γ register. If this bit is the time defined in the
					TDSLOW registe	•	i the time defined in the
1:0	m1_m0	rw	ro	0x1		operating mode for	this RJ45 port.
					enum:esm_ctl_		
					Name	Value	Description
					enc0	0	Port disabl
							ed - No err
							ors will be
							reported; Energy will
							be set to
							zero
					enc1	1	Normal ESM
					1.1	1	1

enc2	2	Reserved
enc3	3	Reserved

1.11.	2 esmi_cmd1					Reg.	0xA0210004
The E	SM Command register a	llows fo	r selec	tion of comm	ands to be perfo	ormed toward	ls an ESM/BPAM
bits	name	s/w	h/w	default		de	escription
15:14	c1_c0	rw	ro	0x0	ESM/BPAM C	cmd_c_encod	
					Name	Valu	ue Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
					enc1	1	Register wr ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma
					enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	ESM Register	Address	,
7:0	d7_d0	rw	ro	0x0	ESM Optional	Write Data F	ield

1.11.	3 esmi_32dat1				0xA0210008				
The I	oottom 16 bits of this i	register are	a mirro	or of esmi_da	t				
bits	name	s/w	h/w	default	description				
31	ce3	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)				
30	ce2	ro	wo	0x0	1 = CRC error on high received byte (BPAM indirect regist read)				
29	ce1	ro	wo	0x0	1 = CRC error on low received byte (BPAM indirect registeread, FN2 parameter read)				
28	ce0	ro	WO	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)				
26	fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM in rect register read)				
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)				
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)				
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without erro (BPAM indirect register read)				
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)				
20	rx0	ro	WO	0x0	1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or 1 = byte received in ESM_DAT[7:0] without error (direct register read)				

17	txfe	ro	WO	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.						
16	tx8e	ro	wo	0x0	1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions.						
15:12	t3_t0	ro	wo	0x0	enum:esmi_dat_t_encoding						
					Name	Value	Description				
					enc0	0	Framing or CRC error				
					enc5	5	SPM cable n ot connecte d				
					enc8	8	Normal, val id data				
					encE	14	ESM cable n ot connecte d				
					encF	15	Indicates E SM is in po wer up stat e				
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ct register read dat	a				

# 1.11.4 esmi\_tdly1 0xA021000C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	5 esmi_fncmd1			Reg.	0xA0210014						
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.											
bits	name	s/w	description								
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write						
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved						
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Numbe	er to be accessed				
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct addr	ess for the FN parameter				
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN p care for FN1 acce		igh byte (FN2 access). don't				
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN p	arameter lo	ow byte (FN2 or FN1 access)				

1.11.0	6 esmi_iacmd1	Reg.	0xA0210018									
This r	This register contains the read/write access to indirect registers in BPAM.											
bits	name	s/w	h/w	default		description	١					
14	iac rw ro 0x0 BPAM Indirect addressing Command type:											

				0 = Indirect register read 1 = Indirect register write
13:0	ia15_ia2	rw	ro	BPAM indirect register address to be accessed. Lowest 2
				bits IA1:0 are assumed to be always zero

### 1.11.7 esmi extdat1



0xA021001C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

bits	name	s/w	h/w	default	description
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

### 1.11.8 esmi\_ctl2



0xA0210030

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	wo	0x0	Flags a framing error on the latest received message. 1 = error
13	iatmo	rw	wo	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.
12	iardy	ro	wo	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes

9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available					
8	tx	ro	WO	0x0	e.	g., when the Comm	s to this register are land FIFO, which qu rites, is full. 1 = write	eues pending		
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample					
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.  enum:esm_ctl_tr_encoding					
						Name	Value	Description		
						enc0	0	normal T0 o peration (T 0 used as s ource)		
						enc1	Reserved us ed by CTEC Operation			
						enc2	2	normal MAP4 operation (droplet de tection use d as source )		
						enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)		
4	fa	rw	ro	0x0	ha w ne	ave a framing error in the time define	a fast ESM. It will be if it does not deliver d in the TDFAST re st respond within the	integration data gister. If this bit is		
1:0	m1_m0	rw	ro	0x1		lode bits set the ope enum:esm_ctl_m_e	erating mode for this	RJ45 port.		
						Name	Value	Description		
						enc0	0	Port disabl ed - No err ors will be reported; Energy will be set to zero		
						enc1	1	Normal ESM mode		
						enc2	2	Reserved		
						enc3	3	Reserved		

1.11.9	1.11.9 esmi_cmd2 0xA0210034												
The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM													
bits	name	descripti	on										
15:14 c1_c0 rw ro 0x0 ESM/BPAM Command Type enum:esmi_cmd_c_encoding													
					Name	Value	Description						
					enc0	0	Register Re ad. D7:D0 a						

								re 'don't c ares' for a read opera tion
						enc1	1	Register wr
								ite
						enc2	2	Tref with w
								ave sync (W
								aveform Cap
								ture) comma
								nd <sup>′</sup>
						enc3	3	Tref, no wa
								ve sync
13:8	a5_a0	rw	ro	0x0		SM Register Addre		
7:0	d7_d0	rw	ro	0x0	Е	SM Optional Write	Data Field	

1.11.	10 esmi_32d	at2				Reg.	0xA0210038
The b	oottom 16 bits of	this register are	a mirro	or of esmi_da	t		
bits	name	s/w	h/w	default		desc	ription
31	ce3	ro	WO	0x0	ister read)	_	eived byte (BPAM indirect reg
30	ce2	ro	WO	0x0	read)		ed byte (BPAM indirect regist
29	ce1	ro	wo	0x0	read, FN2 parar	meter read)	d byte (BPAM indirect registe
28	ce0	ro	wo	0x0	ister read, FN2   register read)	parameter rea	ived byte (BPAM indirect reg- id, FN1 parameter read, direc
27	fe3	ro	WO	0x0	indirect register	read)	nighest received byte (BPAM
26	fe2	ro	WO	0x0	rect register rea	d)	nigh received byte (BPAM ind
25	fe1	ro	WO	0x0	rect register rea	d, FN2 param	
24	fe0	ro	WO	0x0		read, FN2 pai	owest received byte (BPAM rameter read, FN1 parameter
23	rx3	ro	WO	0x0	1 = highest byte error (BPAM inc		SM_EXTDAT[31:24] without read)
22	rx2	ro	wo	0x0	1 = high byte re (BPAM indirect		1_EXTDAT[23:16] without erro
21	rx1	ro	wo	0x0			_EXTDAT[15:8] without error FN2 parameter read)
20	rx0	ro	WO	0x0	(BPAM indirect rameter read) or	register read,	SM_EXTDAT[7:0] without erro FN2 parameter read, FN1 pa T[7:0] without error (direct req
17	txfe	ro	wo	0x0			empty (512 positions). 0 = one command.
16	tx8e	ro	WO	0x0	1 = CMD_FIFO	has at least 8	empty positions. 0 = empty positions.
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Sta	tus	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n

							ot connecte d
					encF	15	Indicates E SM is in po wer up stat
							e
7:0	d7 d0	ro	wo	0x0	ESM/BPAM direct	t register read data	

## 1.11.11 esmi\_tdly2



0xA021003C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	12 esmi_fncmd2			Reg.	0xA0210044					
This r	This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.									
bits	name	s/w	h/w	default		description	า			
28	fnc	rw	ro	0x0	ESM/BPAM FN C 0 = FN parameter 1 = FN parameter	read				
27:26	f1_f0	rw	ro	0x0	FN access type: 10 = FN1 access 11 = FN2 access others = reserved	FN + 2 paramete	• ,			
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to be	e accessed			
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	the FN parameter			
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN pacare for FN1 acce	0 ,	te (FN2 access). don't			
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN pa	arameter low byte	e (FN2 or FN1 access)			

1.11.	13 esmi_iacmd2				Reg.	0xA0210048				
This	This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w	h/w	default		description	n			
14	iac	rw	ro	0x0	BPAM Indirect ad 0 = Indirect registe 1 = Indirect registe	er read	nd type:			
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		pe accessed. Lowest 2 vs zero			

1.11.	14 esmi_extdat2			Reg.	0xA021004C					
	This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.									
bits	name	s/w	h/w	default		description	n			
31:24	id31_id24	rw	rw	0x0	highest byte data read	[31:24] for BPAN	I indirect register write or			
23:16	id23_id16	rw	rw	0x0	high byte data [23 read	:16] for BPAM in	direct register write or			

15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

## 1.11.15 esmi\_ctl3 0xA0210060

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

	` –		,,				0,7
bits	name	s/w	h/w	default		description	
15	ce	ro	WO	0x0	Flags a bad CRC or	n the latest received	message. 1 = error
14	fe	ro	wo	0x0	Flags a framing erro	or on the latest receiv	ved message. 1 =
13	iatmo	rw	wo	0x0	1 = Indirect address Sequence complete	s sequencer timed ou ed normally.	ıt after 50 ms. 0 =
12	iardy	ro	WO	0x0	1 = Indirect address = Command writes	s sequencer ready fo will be ignored.	r new command. 0
11	iarx	ro	WO	0x0	progress.	read complete. 0 =	
10	to	rw	ro	0x0	Enables tref overide multiple read/writes	e : used to ignore TR	EF signal to allow
9	rx	ro	wo	0x0	Indicates when a re ister. 1 = message a	ceive message is in available	the ESM_DAT reg-
8	tx	ro	wo	0x0	e.g., when the Com	es to this register are mand FIFO, which q writes, is full. 1 = writ	ueues pending
7	es	rw	rw	0x0		le. One energy integ of the fire enable stat mple	
6:5	tr	rw	ro	0x0	waveform capture) of ured for TR1/TR0 =	source for ESM energ cycles. Note that if at 11, then all ESMs w etermined by the MAI	ny ESM is config- rill begin their wave-
					enum:esm_ctl_tr_e	encoding	
					Name	Value	Description
					enc0	0	normal T0 o

								peration (T 0 used as s ource)
						enc1	1	Reserved us ed by CTEC Operation
						enc2	2	normal MAP4 operation (droplet de tection use d as source
						enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)
4	fa	rw	ro		ha w no	he FA bit identifies a ave a framing error i ithin the time define of set, the ESM mus DSLOW register.	f it does not deliver d in the TDFAST re	integration data gister. If this bit is
1:0	m1_m0	rw	ro	0x1		ode bits set the ope enum:esm_ctl_m_e	-	RJ45 port.
					ľ	Name	Value	Description
						enc0	0	Port disabl ed - No err ors will be reported;
								Energy will be set to zero
						enc1	1	Normal ESM mode
						enc2	2	Reserved
						enc3	3	Reserved

1.11.	16 esmi_cmd3					Reg.	0xA0210064
The E	ESM Command register al	lows fo	r selec	ction of comm	ands to be perfor	med towards an E	ESM/BPAM
bits	name	s/w	h/w	default		descript	ion
15:14	c1_c0	rw	ro	0x0	enum:esmi_cr	ommand Type md_c_encoding	
					Name	Value	Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
					enc1	1	Register wr
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	ESM Register A	Address	
7:0	d7_d0	rw	ro	0x0	ESM Optional \	Write Data Field	

1.11.	17 esmi_32dat3					Reg.	0xA0210068
The I	oottom 16 bits of this	register are	a mirro	or of esmi_da	t		
bits	name	s/w	h/w	default			ription
31	ce3	ro	WO	0x0	ister read)	_	eived byte (BPAM indirect reg-
30	ce2	ro	wo	0x0	1 = CRC error or read)	high receive	ed byte (BPAM indirect register
29	ce1	ro	WO	0x0	read, FN2 param	eter read)	d byte (BPAM indirect register
28	ce0	ro	WO	0x0			ved byte (BPAM indirect reg- d, FN1 parameter read, direct
27	fe3	ro	wo	0x0	1 = Frame error (indirect register r		nighest received byte (BPAM
26	fe2	ro	WO	0x0	1 = Frame error ( rect register read		nigh received byte (BPAM indi-
25	fe1	ro	WO	0x0	1 = Frame error ( rect register read		ow received byte (BPAM indieter read)
24	fe0	ro	WO	0x0		ead, FN2 par	owest received byte (BPAM rameter read, FN1 parameter
23	rx3	ro	WO	0x0	1 = highest byte error (BPAM indi		SM_EXTDAT[31:24] without read)
22	rx2	ro	WO	0x0	1 = high byte rec (BPAM indirect re		I_EXTDAT[23:16] without error
21	rx1	ro	wo	0x0	(BPAM indirect re	egister read,	_EXTDAT[15:8] without error FN2 parameter read)
20	rx0	ro	WO	0x0	(BPAM indirect read) or	egister read,	SM_EXTDAT[7:0] without error FN2 parameter read, FN1 pa-T[7:0] without error (direct reg-
17	txfe	ro	wo	0x0			empty (512 positions). 0 = one command.
16	tx8e	ro	wo	0x0		as at least 8	empty positions. 0 =
15:12	t3_t0	ro	WO	0x0	ESM/BPAM State	us _t_encoding	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direc	rt register rea	

## 1.11.18 esmi\_tdly3



0xA021006C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	19 esmi_fncmd3	Reg.	0xA0210074							
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.										
bits	name	description								
28	fnc	rw	ro	0x0	ESM/BPAM FN C 0 = FN parameter 1 = FN parameter	read				
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved					
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to be	e accessed			
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	the FN parameter			
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN pacare for FN1 acce	• .	te (FN2 access). don't			
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN pa	arameter low byte	e (FN2 or FN1 access)			

1.11.	20 esmi_iacmd3	Reg.	0xA0210078						
This register contains the read/write access to indirect registers in BPAM.									
bits	name	description							
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write				
13:0	ia15_ia2	gister address to umed to be alwa	be accessed. Lowest 2 ays zero						

1.11.	21 esmi_extdat3	0xA021007C							
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.									
bits	name	s/w	h/w	default	description				
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read				
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read				
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read				
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read				

1.11.22 esmi_ctl4	Reg.	0xA0210090
ESMI control transactions are sent and received in the eight ESM con	trol blocks. Each block	is four 16-bit words

The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

1) metric parameters

2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

Writes and reads to/from ESM registers are unrestricted when the TEM\_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM\_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

bits	name	s/w	h/w	default	description
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	WO	0x0	Flags a framing error on the latest received message. 1 = error
13	iatmo	rw	WO	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.
12	iardy	ro	WO	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>
11	iarx	ro	WO	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.
10	to	rw	ro	0x0	Enables tref overide: used to ignore TREF signal to allow multiple read/writes
9	rx	ro	WO	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available
8	tx	ro	wo	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.

enum:esm\_ctl\_tr\_encoding

enum:esm_cti_tr_encoding								
Name	Value	Description						
enc0	0	normal T0 o						
		peration (T						
		0 used as s						
		ource)						
enc1	1	Reserved us						
		ed by CTEC						
		Operation						
enc2	2	normal MAP4						
		operation						
		(droplet de						
		tection use						
		d as source						
		)						

						enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)
4	fa	rw	ro	0x0	hav wit not TD	ve a framing error i hin the time define t set, the ESM mus SLOW register.	fast ESM. It will be f it does not deliver d in the TDFAST re t respond within the	integration data gister. If this bit is time defined in the
1:0	m1_m0	rw	ro	0x1		num:esm_ctl_m_e		
						Name	Value	Description
						enc0	0	Port disabl
								ed - No err
								ors will be
								reported;
								Energy will
								be set to
					L			zero
						enc1	1	Normal ESM mode
						enc2	2	Reserved
						enc3	3	Reserved

1.11.	23 esmi_cmd4			Reg.	0xA0210094			
The E	SM Command register a	allows fo	r seled	ction of comm	and	ls to be performe	d towards an ES	M/BPAM
bits	name	s/w	h/w	default			description	n
15:14	c1_c0	rw	ro	0x0		SM/BPAM Commenum:enum:esmi_cmd_	7.	
						Name	Value	Description
						enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
						enc1	1	Register wr ite
					-	enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
						enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	Е	SM Register Add	ress	
7:0	d7_d0	rw	ro	0x0	Е	SM Optional Writ	e Data Field	

1.11.	24 esmi_32dat4		Reg.	0xA0210098					
The bottom 16 bits of this register are a mirror of esmi_dat									
bits name s/w h/w default description									
31	ce3	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)				
30	ce2	ro	wo	0x0	1 = CRC error on high received byte (BPAM indirect register read)				
29	ce1	ro	wo	0x0	1 = CRC error on read, FN2 parame		byte (BPAM indirect register		

28	ce0	ro	wo	0x0		1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
27	fe3	ro	wo	0x0	1 = Frame error	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)				
26	fe2	ro	wo	0x0	rect register read	1 = Frame error (timeout) on high received byte (BPAM indirect register read)				
25	fe1	ro	wo	0x0	rect register read	l, FN2 parameter re				
24	fe0	ro	WO	0x0	indirect register r	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
23	rx3	ro	wo	0x0		received in ESM_E rect register read)	EXTDAT[31:24] without			
22	rx2	ro	wo	0x0	(BPAM indirect r	egister read)	DAT[23:16] without error			
21	rx1	ro	wo	0x0		eived in ESM_EXTI egister read, FN2 p	DAT[15:8] without error parameter read)			
20	rx0	ro	wo	0x0	(BPAM indirect r rameter read) or	egister read, FN2 p	XTDAT[7:0] without error parameter read, FN1 pa-			
17	txfe	ro	wo	0x0		1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.				
16	tx8e	ro	wo	0x0		nas at least 8 empty fewer than 8 empty				
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Stat					
					Name	Value	Description			
					enc0	0	Framing or CRC error			
					enc5	5	SPM cable n ot connecte d			
					enc8	8	Normal, val id data			
					encE	14	ESM cable n ot connecte d			
					encF	15	Indicates E SM is in po wer up stat e			
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ct register read dat	a			

## 1.11.25 esmi\_tdly4



0xA021009C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	26 esmi_fncmd4	Reg.	0xA02100A4							
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.										
bits	name	description	on							
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write					
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved					
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to b	oe accessed			
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address fo	or the FN parameter			
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN pacare for FN1 acce		yte (FN2 access). don't			
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN p	arameter low by	te (FN2 or FN1 access)			

1.11.	27 esmi_iacmd4	Reg.	0xA02100A8							
This	This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w	h/w	default		description				
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write					
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass	•	pe accessed. Lowest 2 vs zero			

1.11.	28 esmi_extdat4			Reg.	0xA02100AC					
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.										
bits	name	s/w	h/w	default		description	ı			
31:24	id31_id24	rw	rw	0x0	highest byte data read	[31:24] for BPAM	indirect register write or			
23:16	id23_id16	rw	rw	0x0	high byte data [23 read	3:16] for BPAM inc	direct register write or			
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15: OR low byte data [15:	•	ect register write or read eter read			
7:0	ifd7_ifd0	rw	rw	0x0	read OR	•	lirect register write or  N1 parameter read			

0xA02100C0 1.11.29 esmi\_ctl5 Reg.

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT reg-

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

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The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

## Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default		description			
15	ce	ro	wo	0x0			ived message. 1 = error		
14	fe	ro	WO	0x0	error		eceived message. 1 =		
13	iatmo	rw	WO	0x0	1 = Indirect add Sequence comp		ed out after 50 ms. 0 =		
12	iardy	ro	WO	0x0		ress sequencer read tes will be ignored.	dy for new command. 0		
11	iarx	ro	WO	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.				
10	to	rw	ro	0x0	Enables tref overide: used to ignore TREF signal to allow multiple read/writes				
9	rx	ro	WO	0x0	Indicates when ister. 1 = messa		is in the ESM_DAT reg-		
8	tx	ro	wo	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowe				
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by H\\ 1 = force energy sample				
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration waveform capture) cycles. Note that if any ESM is coured for TR1/TR0 = 11, then all ESMs will begin their form captures as determined by the MAP4 HOP modation.  enum:esm_ctl_tr_encoding				
							Description		
					Name	Value	Description normal T0 o		
					enc0	0	peration (T 0 used as s ource)		
					enc1	1	Reserved us ed by CTEC Operation		
					enc2	2	normal MAP4 operation (droplet de tection use d as source )		
					enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)		
4	fa	rw	ro	0x0	have a framing of within the time of not set, the ESN TDSLOW regist	error if it does not do defined in the TDFA If must respond with er.	will be considered to eliver integration data ST register. If this bit is in the time defined in the		
1:0	m1_m0	rw	ro	0x1	Mode bits set th	e operating mode for	or this RJ45 port.		
					enum:esm_ctl	m encodina			
					Name	Value	Description		
					IName	v alue	Description		

		ed - No err ors will be reported; Energy will be set to zero
enc1	1	Normal ESM mode
enc2	2	Reserved
enc3	3	Reserved

1.11.	30 esmi_cmd5			Reg.	0xA02100C4		
The E	SM Command register al	lows for	r selec	tion of comma	ands to be perform	ned towards an ES	SM/BPAM
bits	name	s/w	h/w	default		description	n
15:14	c1_c0	rw ro	ro	0x0	ESM/BPAM Comenum:esmi_cm		
					Name	Value	Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion Register wr
					0.101		ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	ESM Register Ad	ddress	
7:0	d7_d0	rw	ro	0x0	ESM Optional W	rite Data Field	

1.11.	31 esmi_32dat5		0xA02100C8					
The b	oottom 16 bits of this re	gister are	a mirro	or of esmi_da	t .			
bits	name	s/w	h/w	default	description			
31	ce3	ro	WO	0x0	1 = CRC error on highest received byte (BPAM indirect register read)			
30	ce2	ro	WO	0x0	1 = CRC error on high received byte (BPAM indirect register read)			
29	ce1	ro	wo	0x0	1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)			
28	ce0	ro	wo	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)			
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)			
26	fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM indirect register read)			
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)			
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)			
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)			
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)			

21	rx1	ro	wo	0x0		•	eived in ESM_EXTD egister read, FN2 p	OAT[15:8] without error arameter read)		
20	rx0	ro	WO	0x0	(E ra oi 1	1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or 1 = byte received in ESM_DAT[7:0] without error (direct register read)				
17	txfe	ro	wo	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.					
16	tx8e	ro	wo	0x0			nas at least 8 empty fewer than 8 empty			
15:12			WO	0x0	enum:esmi_dat_t_encoding    Name					
						enc0	0	Framing or CRC error		
						enc5	5	SPM cable n ot connecte d		
						enc8	8	Normal, val id data		
						encE	14	ESM cable n ot connecte d		
						encF	15	Indicates E SM is in po wer up stat e		
7:0	d7_d0	ro	wo	0x0	Е	SM/BPAM dire	ct register read data	1		

### 1.11.32 esmi tdly5



0xA02100CC

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

#### 1.11.33 esmi fncmd5 0xA02100D4 This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM. bits name s/w h/w default description 28 fnc 0x0 ESM/BPAM FN Command type: ro rw 0 = FN parameter read 1 = FN parameter write 27:26 f1\_f0 rw ro 0x0 FN access type: 10 = FN1 access (FN + 1 parameter byte) 11 = FN2 access (FN + 2 parameter bytes) others = reserved 25:22 fn3\_fn0 0x0 rw ro ESM/BPAM Function Number to be accessed 21:16 fa5\_fa0 0x0 ESM/BPAM start direct address for the FN parameter rw ro 15:8 fd15\_fd8 ro 0x0 ESM/BPAM FN parameter high byte (FN2 access). don't rw care for FN1 access

1.11.	34 esmi_iacmd5	Reg.	0xA02100D8						
This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w	description						
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write				
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass	•	be accessed. Lowest 2 ys zero		

### 1.11.35 esmi\_extdat5



0xA02100DC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

bits	name	s/w	h/w	default	description
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

# 1.11.36 esmi\_ctl6 0xA02100F0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	WO	0x0	Flags a framing error on the latest received message. 1 = error

13	iatmo	rw	wo	0x0	Sequence compl	eted normally.	ed out after 50 ms. 0 =		
12	iardy	ro	wo	0x0	= Command write	es will be ignored.	dy for new command. 0		
11	iarx	ro	wo	0x0	1 = Indirect address progress.	ess read complete	. 0 = Indirect read in		
10	to	rw	ro	0x0			e TREF signal to allow		
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available				
8	tx	ro	wo	0x0			er are not allowed,		
							ich queues pending = writes are not allowed.		
7	es	rw	rw	0x0		s of the fire enable	integration shot will be state. Cleafred by HW.		
6:5	tr	rw	ro	0x0	Selects the trigge waveform capture ured for TR1/TR0 form captures as ation.	er source for ESM e) cycles. Note that 0 = 11, then all ES determined by the	energy integration (and at if any ESM is config- Ms will begin their wave- e MAP4 HOP mode oper-		
					enum:esm_ctl_t Name	r_encoding Value	Description		
					enc0	0	normal T0 o		
					CHOO		peration (T 0 used as s ource)		
					enc1	1	Reserved us ed by CTEC Operation		
					enc2	2	normal MAP4 operation (droplet de tection use d as source )		
					enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)		
4	fa	rw	ro	0x0	have a framing e within the time de	rror if it does not d efined in the TDFA must respond with	will be considered to eliver integration data ST register. If this bit is nin the time defined in the		
1:0	m1_m0	rw	ro	0x1	Mode bits set the	operating mode f	or this RJ45 port.		
					enum:esm_ctl_	m_encoding			
					Name	Value	Description		
					enc0	0	Port disabl		
							ed - No err ors will be		
							reported;		
							Energy will be set to		
							zero		
					enc1	1	Normal ESM mode		
					enc2	2	Reserved		
					enc3	3	Reserved		

1.11.37 esmi\_cmd6

Reg.

0xA02100F4

bits	name	s/w	h/w	default		description	
5:14	c1_c0	rw	ro	0x0	ESM/BPAM Cor	· · · · · · · · · · · · · · · · · · ·	
					Name	Value Value	Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
					enc1	1	Register wr ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync
3:8	a5_a0	rw	ro	0x0	ESM Register A	ddress	·
:0	d7_d0	rw	ro	0x0	ESM Optional W	/rite Data Field	

1.11.	38 esmi_32dat6				0xA02100F8			
The b	oottom 16 bits of this r	egister are	a mirr	or of esmi_da	t			
bits	name	s/w	h/w	default	description			
31	ce3	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)			
30	ce2	ro	wo	0x0	1 = CRC error on high received byte (BPAM indirect register read)			
29	ce1	ro	wo	0x0	1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)			
28	ce0	ro	WO	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)			
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)			
26	fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM indirect register read)			
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)			
24	fe0	ro	wo	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)			
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)			
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without erro (BPAM indirect register read)			
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)			
20	rxO	ro	WO	0x0	1 = lowest byte received in ESM_EXTDAT[7:0] without erro (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or			
					1 = byte received in ESM_DAT[7:0] without error (direct register read)			
17	txfe	ro	wo	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.			
16	tx8e	ro	wo	0x0	1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions.			
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Status enum:esmi_dat_t_encoding			

					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ect register read data	 a

## 1.11.39 esmi\_tdly6

Reg.

0xA02100FC

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	40 esmi_fncmd6			Reg.	0xA0210104							
This r	This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.											
bits	name	description	n									
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write							
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved							
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to be	e accessed					
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	r the FN parameter					
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access							
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN p	arameter low byte	e (FN2 or FN1 access)					

1.11.	41 esmi_iacmd6			Reg.	0xA0210108			
This	egister contains the read/							
bits	name	description						
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write			
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect register address to be accessed. Lowest 2 bits IA1:0 are assumed to be always zero			

### 1.11.42 esmi extdat6

Reg.

0xA021010C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

bits	name	s/w	h/w	default	description
		5/ W	I I/ VV	ueiauit	•
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

### 1.11.43 esmi ctl7



0xA0210120

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
15	се	ro	WO	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	WO	0x0	Flags a framing error on the latest received message. 1 = error
13	iatmo	rw	WO	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.
12	iardy	ro	WO	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>
11	iarx	ro	WO	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.
10	to	rw	ro	0x0	Enables tref overide: used to ignore TREF signal to allow multiple read/writes
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available
8	tx	ro	wo	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample

6:5	tr	rw	ro	0x0	waveform captur ured for TR1/TR	e) cycles. Note that 0 = 11, then all ESN	energy integration (and if any ESM is config- As will begin their wave- MAP4 HOP mode oper-
					enum:esm_ctl_	tr_encoding	
					Name	Value	Description
					enc0	0	normal T0 o peration (T 0 used as s ource)
					enc1	1	Reserved us ed by CTEC Operation
					enc2	2	normal MAP4 operation (droplet de tection use d as source )
					enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)
4	fa	rw	ro	0x0	have a framing e within the time d not set, the ESM TDSLOW registe	error if it does not de efined in the TDFAS I must respond with er.	vill be considered to eliver integration data ST register. If this bit is in the time defined in the
1:0	m1_m0	rw	ro	0x1	Mode bits set the enum:esm_ctl_	e operating mode for mode for mode for modeling	r this RJ45 port.
					Name	Value	Description
					enc0	0	Port disabl ed - No err
							ors will be reported; Energy will be set to
					enc1	1	zero Normal ESM mode
					enc2	2	Reserved
					enc3	3	Reserved

1.11.4	44 esmi_cmd7		Reg.	0xA0210124				
The E	SM Command register al	lows fo	r selec	tion of comma	anc	ds to be performe	d towards an ES	SM/BPAM
bits	name	s/w	h/w	default			description	n
15:14	c1_c0	rw	ro	0x0	Ε	SM/BPAM Comn	nand Type	
						enum:esmi_cmd	_c_encoding	
						Name	Value	Description
						enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
						enc1	1	Register wr ite
						enc2	2	Tref with w ave sync (W

								aveform Cap ture) comma nd		
						enc3	3	Tref, no wa		
								ve sync		
13:8	a5_a0	rw	ro	0x0	ESM Register Address					
7:0	d7_d0	rw	ro	0x0	ESM Optional Write Data Field					

1.11.	45 esmi_32dat	7				Reg.	0xA0210128			
The b	oottom 16 bits of thi	s register are	a mirro	or of esmi_da	t					
bits	name	s/w	h/w	default		descrip	otion			
31	ce3	ro	wo	0x0	ister read)		ed byte (BPAM indirect reg			
30	ce2	ro	wo	0x0	read)	_	byte (BPAM indirect registe			
29	ce1	ro	wo	0x0	read, FN2 param	neter read)	byte (BPAM indirect register			
28	ce0	ro	WO	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)					
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)					
26	fe2	ro	wo	0x0	<ul><li>1 = Frame error (timeout) on high received byte (BPAM indirect register read)</li></ul>					
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)					
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)					
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)					
22	rx2	ro	WO	0x0	1 = high byte received in ESM_EXTDAT[23:16] without err (BPAM indirect register read)					
21	rx1	ro	WO	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)					
20	rx0	ro	wo	0x0	<ul> <li>1 = lowest byte received in ESM_EXTDAT[7:0] without erro (BPAM indirect register read, FN2 parameter read, FN1 parameter read)</li> <li>or</li> <li>1 = byte received in ESM_DAT[7:0] without error (direct register read)</li> </ul>					
17	txfe	ro	WO	0x0	1 = CMD_FIFO i CMD_FIFO cont		mpty (512 positions). 0 = ne command.			
16	tx8e	ro	wo	0x0	1 = CMD_FIFO has		mpty positions. 0 = mpty positions.			
15:12	t3_t0	ro	WO	0x0	ESM/BPAM State					
					Name	Value	Description			
					enc0	0	Framing or CRC error			
					enc5	5	SPM cable n ot connecte d			
					enc8	8	Normal, val id data			
					encE	14	ESM cable n ot connecte d			
					encF	15	Indicates E SM is in po wer up stat e			
	d7_d0			0x0	ESM/BPAM dire					

## 1.11.46 esmi\_tdly7



0xA021012C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	47 esmi_fncmd7	Reg.	0xA0210134							
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.										
bits	name		description							
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write					
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved					
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Fund	tion Number t	o be accessed			
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address	for the FN parameter			
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN p	9	byte (FN2 access). don't			
7:0	fd7 fd0	rw	ro	0x0	ESM/BPAM FN p	arameter low	byte (FN2 or FN1 access)			

1.11.	48 esmi_iacmd7	Reg.	0xA0210138						
This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w	h/w	default	description				
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write				
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		pe accessed. Lowest 2 vs zero		

1.11.	49 esmi_extdat7		Reg.	0xA021013C					
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.									
bits	name	s/w	h/w	default		desc	ription		
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read				
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read				
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8 OR low byte data [15:8	•	l indirect register write or read arameter read		
7:0	ifd7_ifd0	rw	rw	0x0	read OR	-	M indirect register write or or FN1 parameter read		

1.11.50 esmi\_ctl8

Reg.

0xA0210150

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

1) metric parameters

2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description			
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error			
14	fe	ro	wo	0x0	Flags a framing error on the latest received message. 1 = error			
13	iatmo	rw	WO	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.			
12	iardy	ro	wo	0x0	1 = Indirect address sequencer ready for new command. ( = Command writes will be ignored.			
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.			
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes			
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT relister. 1 = message available			
8	tx	ro	WO	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.			
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample			
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.			
					enum:esm_ctl_tr_encoding    Name			
					enc0 0 normal T0 o			
					Tiolinal 10 0			

Name	Value	Description
enc0	0	normal T0 o peration (T 0 used as s ource)
enc1	1	Reserved us ed by CTEC Operation
enc2	2	normal MAP4

							3	operation (droplet de tection use d as source )
						enc3	3	P4 operatio
								n (HOP mode
								- see MAP4
								HOP regist
								er below)
4	fa	rw	ro	0x0		he FA bit identifies a		
					w n	ave a framing error within the time define ot set, the ESM must DSLOW register.	d in the TDFAST re	
1:0	m1_m0	rw	ro	0x1		fode bits set the ope	arating mode for this	R 1/15 nort
1.0		1 **	10	OXI		lode bits set the ope	rading mode for this	rto-to port.
						enum:esm_ctl_m_e	ncoding	
						Name	Value	Description
						enc0	0	Port disabl
								ed - No err
								ors will be
								reported;
								Energy will
								be set to
								zero
						enc1	1	Normal ESM
								mode
						enc2	2	Reserved
						enc3	3	Reserved

1.11.	51 esmi_cmd8					Reg.	0xA0210154
The E	ESM Command registe	r allows fo	r selec	ction of comm	ands to be perfor	med towards a	ın ESM/BPAM
bits	name	s/w	h/w	default		desci	ription
5:14	c1_c0	rw	ro	0x0		md_c_encoding	
					Name	Value	Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
					enc1	1	Register wr ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	ESM Register A	Address	
7:0	d7_d0	rw	ro	0x0	ESM Optional V	Vrite Data Field	d

1.11.	52 esmi_32dat8	Reg.	0xA0210158							
The bottom 16 bits of this register are a mirror of esmi_dat										
bits	name	s/w	h/w	default		description	n			
31	ce3	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)					

30	ce2	ro	wo	0x0	1 = CRC error on high received byte (BPAM indirect register				
		10	WO		read)				
29	ce1	ro	WO	0x0	1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)				
28	ce0	ro	WO	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)				
26	fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM indirect register read)				
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)				
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)				
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)				
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)				
20	rx0	ro	wo	0x0	1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or 1 = byte received in ESM_DAT[7:0] without error (direct register read)				
17	txfe	ro	WO	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.				
16	tx8e	ro	wo	0x0	1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions.				
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Status  enum:esmi_dat_t_encoding				
					Name Value Description				
					enc0 0 Framing or CRC error				
					enc5 5 SPM cable n ot connecte d				
					enc8 8 Normal, val id data				
					encE 14 ESM cable n ot connecte d				
					encF 15 Indicates E SM is in po wer up stat e				
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direct register read data				

## 1.11.53 esmi\_tdly8



0xA021015C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	54 esmi_fncmd8		Reg.	0xA0210164						
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.										
bits	name	s/w		description						
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write					
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved					
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Fund	tion Number to be	e accessed			
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	the FN parameter			
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN p care for FN1 acce	,	te (FN2 access). don't			
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN p	arameter low byte	e (FN2 or FN1 access)			

1.11.	55 esmi_iacmd8	Reg.	0xA0210168					
This register contains the read/write access to indirect registers in BPAM.								
bits	s name s/w h/w default					description		
14	iac	rw	ro	0x0	BPAM Indirect ad 0 = Indirect regist 1 = Indirect regist	er read	nd type:	
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		be accessed. Lowest 2 ys zero	

1.11.	56 esmi_extdat8	Reg.	0xA021016C				
	register contains the write s, or the read data for ESN			•		ead data for BPA	M indirect register
bits	name	s/w	h/w	default		description	1
31:24	id31_id24	rw	rw	0x0	highest byte data read	[31:24] for BPAM	indirect register write or
23:16	id23_id16	rw	rw	0x0	high byte data [23 read	3:16] for BPAM inc	direct register write or
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15] OR low byte data [15]	•	ect register write or read eter read
7:0	ifd7_ifd0	rw	rw	0x0	read OR	-	lirect register write or N1 parameter read

1.11.57 esmi\_ctl9 0xA0210180

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

name

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

h/w

s/w

Writes and reads to/from ESM registers are unrestricted when the TEM\_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM\_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

description

default

DILS	name	S/W	I I/ VV	delault		description			
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error				
14	fe	ro	WO	0x0	Flags a framing error on the latest received message. 1 = error				
13	iatmo	rw	WO	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.				
12	iardy	ro	WO	0x0	1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored.				
11	iarx	ro	wo	0x0			0 = Indirect read in		
10	to	rw	ro	0x0			e TREF signal to allow		
9	rx	ro	wo	0x0		receive message i	s in the ESM_DAT reg-		
8	tx	ro	wo	0x0	Indicates when w e.g., when the Co	rites to this registe ommand FIFO, whi	ch queues pending		
7	es	rw	rw	0x0	ESM_CTL register writes, is full. 1 = writes are not allowed.  Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW.  1 = force energy sample				
6:5	tr	rw ro 0x0 Selects the trigger source for ESM en waveform capture) cycles. Note that ured for TR1/TR0 = 11, then all ESM form captures as determined by the I ation.					if any ESM is config- Is will begin their wave-		
					enum:esm_ctl_t Name	Value	Description		
					enc0	0	normal T0 o		
					enco		peration (T 0 used as s ource)		
					enc1	1	Reserved us ed by CTEC Operation		
					enc2	2	normal MAP4 operation (droplet de tection use d as source )		
					enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)		
4	fa	rw	ro	0x0	have a framing er within the time de	ror if it does not defined in the TDFAS must respond with	vill be considered to eliver integration data ST register. If this bit is in the time defined in the		

1:0	m1_m0	rw	ro	0x1	Mode bits set the operating mode for this RJ45 port.				
					enum:esm_ctl_m_encoding				
						Name	Value	Description	
						enc0	0	Port disabl	
								ed - No err	
								ors will be	
								reported;	
								Energy will	
								be set to	
								zero	
						enc1	1	Normal ESM	
								mode	
						enc2	2	Reserved	
						enc3	3	Reserved	

1.11.	58 esmi_cmd9	Reg.	0xA0210184					
The E	ESM Command registe	r allows fo	r seled	ction of comm	ands to be perfo	ormed towards an ES	M/BPAM	
bits	name	s/w	h/w	default		description	n	
15:14	c1_c0	rw	rw ro	0x0	ESM/BPAM Command Type enum:esmi_cmd_c_encoding			
					Name	Value	Description	
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion	
					enc1	1	Register wr	
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd	
					enc3	3	Tref, no wa ve sync	
13:8	a5_a0	rw	ro	0x0	ESM Register	Address		
7:0	d7_d0	rw	ro	0x0	ESM Optiona	l Write Data Field		

1.11.	59 esmi_32dat9	Reg.	0xA0210188						
The bottom 16 bits of this register are a mirror of esmi_dat									
bits	name	s/w	h/w		description	า			
31	ce3	ro	wo	0x0	1 = CRC error on ister read)	highest received	byte (BPAM indirect reg-		
30	ce2	ro	wo	0x0	1 = CRC error on read)	high received byt	e (BPAM indirect register		
29	ce1	ro	wo	0x0	1 = CRC error on read, FN2 parame	•	e (BPAM indirect register		
28	ce0	ro	WO	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
27	fe3	ro	wo	0x0	1 = Frame error (t indirect register re	, •	st received byte (BPAM		
26	fe2	ro	wo	0x0	1 = Frame error (t rect register read)	, •	eceived byte (BPAM indi-		
25	fe1	ro	wo	0x0	1 = Frame error (t rect register read,	,	ceived byte (BPAM indi- ead)		
24	fe0	ro	WO	0x0	,	ad, FN2 paramet	t received byte (BPAM er read, FN1 parameter		

23	rx3	ro	wo	0x0		e received in ESM_E direct register read)	EXTDAT[31:24] without			
22	rx2	ro	wo	0x0	(BPAM indirect	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)				
21	rx1	ro	wo	0x0		1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)				
20	rx0	ro	WO	0x0	(BPAM indirect rameter read) or	register read, FN2 p	XTDAT[7:0] without error parameter read, FN1 pa-			
17	txfe	ro	wo	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.					
16	tx8e	ro	wo	0x0	1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions.					
15:12	13_10	ro	WO	0x0	enum:esmi_da		Description			
					enc0	0	Framing or CRC error			
					enc5	5	SPM cable n ot connecte d			
					enc8	8	Normal, val id data			
					encE	14	ESM cable n ot connecte d			
					encF	15	Indicates E SM is in po wer up stat			
7:0	d7 d0	ro	wo	0x0	ESM/BPAM dire	ect register read dat	a e			

# 1.11.60 esmi\_tdly9



0xA021018C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

#### 0xA0210194 1.11.61 esmi fncmd9 This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM. bits name s/w h/w default description ESM/BPAM FN Command type: 28 fnc rw ro 0x0 0 = FN parameter read 1 = FN parameter write 27:26 f1\_f0 0x0 FN access type: rw 10 = FN1 access (FN + 1 parameter byte) 11 = FN2 access (FN + 2 parameter bytes) others = reserved 25:22 fn3\_fn0 0x0 ESM/BPAM Function Number to be accessed rw ro

21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start direct address for the FN parameter
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access
7:0	fd7 fd0	rw	ro	0x0	ESM/BPAM FN parameter low byte (FN2 or FN1 access)

1.11.	62 esmi_iacmd9	Reg.	0xA0210198						
This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w	h/w	default		description			
14	iac	rw	ro	0x0	0 = Indirect regist	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write			
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		pe accessed. Lowest 2 vs zero		

1.11.	63 esmi_extdat9					Reg.	0xA021019C		
	register contains the write s, or the read data for ESI				•	ead data fo	or BPAM indirect register		
bits	name	s/w	h/w	default		description			
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read				
23:16	id23_id16	rw	rw	0x0	high byte data [23 read	3:16] for BP	'AM indirect register write or		
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15: OR low byte data [15:	•	M indirect register write or read parameter read		
7:0	ifd7_ifd0	rw	rw	0x0	read OR	•	AM indirect register write or  2 or FN1 parameter read		

1.11.64 esmi\_ctl10 0xA02101B0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
------	------	-----	-----	---------	-------------

15	ce	ro	wo	0x0	Flags a bad CRC	on the latest recei	ved message. 1 = error	
14	fe	ro	wo	0x0			eceived message. 1 =	
					error			
13	iatmo	rw	wo	0x0	Sequence comple	eted normally.	ed out after 50 ms. 0 =	
12	iardy	ro	wo	0x0	= Command write	s will be ignored.	dy for new command. 0	
11	iarx	ro	WO	0x0	1 = Indirect addre progress.	ss read complete.	0 = Indirect read in	
10	to	rw	ro	0x0	Enables tref overide: used to ignore TREF signal to allow multiple read/writes			
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available			
8	tx	ro	WO	0x0	e.g., when the Co		r are not allowed, ch queues pending writes are not allowed.	
7	es	rw	rw	0x0		of the fire enable	ntegration shot will be state. Cleafred by HW.	
6:5	tr	rw	ro	0x0	waveform capture ured for TR1/TR0	e) cycles. Note that = 11, then all ESM	energy integration (and t if any ESM is config- As will begin their wave- MAP4 HOP mode oper-	
					enum:esm_ctl_t			
					Name	Value	Description normal T0 o	
					enc0	0	peration (T 0 used as s ource)	
					enc1	1	Reserved us ed by CTEC Operation	
					enc2	2	normal MAP4 operation (droplet de tection use d as source )	
					enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)	
4	fa	rw	ro	0x0	The FA bit identifi	es a fast ESM. It v	vill be considered to	
					have a framing er within the time de	ror if it does not de fined in the TDFAS must respond with	eliver integration data ST register. If this bit is in the time defined in the	
1:0	m1_m0	rw	ro	0x1		operating mode for	or this RJ45 port.	
					enum:esm_ctl_r			
					Name	Value	Description	
					enc0	0	Port disabled - No err	
							ors will be reported; Energy will be set to	
							zero	
					enc1	1	Normal ESM mode	
							1	
					enc2	2	Reserved	

#### 1.11.65 esmi\_cmd10 0xA02101B4 The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM s/w h/w default description 15:14 c1\_c0 ESM/BPAM Command Type ro 0x0 rw enum:esmi\_cmd\_c\_encoding Name Value Description Register Re enc0 0 ad. D7:D0 a re 'don't c ares' for a read opera tion Register wr enc1 Tref with w enc2 2 ave sync (W aveform Cap ture) comma nd Tref, no wa enc3 3 ve sync ESM Register Address a5\_a0 13:8 0x0 rw ro ESM Optional Write Data Field d7\_d0 7:0 0x0 rw ro

1.11	.66 esmi_32dat10	)			0xA02101B8		
The	bottom 16 bits of this	register are	a mirro	or of esmi_da	t		
bits	name	s/w	h/w	default	description		
31	ce3	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)		
30	ce2	ro	WO	0x0	<ul><li>1 = CRC error on high received byte (BPAM indirect register read)</li></ul>		
29	ce1	ro	WO	0x0	1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)		
28	ce0	ro	WO	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)		
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)		
26	fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM indirect register read)		
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM ind rect register read, FN2 parameter read)		
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)		
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)		
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)		
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)		
20	rx0	ro	WO	0x0	1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or 1 = byte received in ESM_DAT[7:0] without error (direct register read)		
17	txfe	ro	WO	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.		

16	tx8e	ro	wo	0x0	1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions.				
15:12	t3_t0	ro	ro wo	0x0	ESM/BPAM Status	3			
					Name	Value	Description		
					enc0	0	Framing or CRC error		
					enc5	5	SPM cable n ot connecte d		
					enc8	8	Normal, val id data		
					encE	14	ESM cable n ot connecte d		
					encF	15	Indicates E SM is in po wer up stat e		
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direct	register read dat	-		

# 1.11.67 esmi\_tdly10



0xA02101BC

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.0	68 esmi_fncmd10			Reg.	0xA02101C4						
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.											
bits	name	s/w	h/w	default		description	า				
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write						
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved						
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to be	accessed				
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	the FN parameter				
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN p care for FN1 acce		e (FN2 access). don't				
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN p	arameter low byte	e (FN2 or FN1 access)				

1.11.0	69 esmi_iacmd10			Reg.	0xA02101C8					
This register contains the read/write access to indirect registers in BPAM.										
bits	name	s/w	h/w	default	description					
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write					

13:0	ia15_ia2	rw	ro	0x0	BPAM indirect register address to be accessed. Lowest 2
					bits IA1:0 are assumed to be always zero

#### 1.11.70 esmi\_extdat10



0xA02101CC

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

bits	name	s/w	h/w	default	description
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

### 1.11.71 esmi\_ctl11



0xA02101E0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	wo	0x0	Flags a framing error on the latest received message. 1 = error
13	iatmo	rw	wo	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.
12	iardy	ro	wo	0x0	1 = Indirect address sequencer ready for new command. 0 = Command writes will be ignored.
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes
9	rx	ro	WO	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available

8	tx	ro	WO	0x0	e.g., when the C		er are not allowed, ich queues pending = writes are not allowed.
7	es	rw	rw	0x0		ss of the fire enable	ntegration shot will be state. Cleafred by HW.
6:5	tr	rw	ro	0x0	waveform captu ured for TR1/TR	re) cycles. Note tha 0 = 11, then all ESI	energy integration (and t if any ESM is config- Ms will begin their wave- MAP4 HOP mode oper-
					enum:esm_ctl_		
					Name	Value	Description
					enc0	0	normal T0 o peration (T 0 used as s ource)
					enc1	1	Reserved us ed by CTEC Operation
					enc2	2	normal MAP4 operation (droplet de tection use d as source )
					enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)
4	fa	rw	ro	0x0	have a framing e within the time d	error if it does not do efined in the TDFA I must respond with	will be considered to eliver integration data ST register. If this bit is in the time defined in the
1:0	m1_m0	rw	ro	0x1	Mode bits set the	e operating mode for	or this RJ45 port.
					enum:esm_ctl_	m encoding	
					Name	Value	Description
					enc0	0	Port disabl ed - No err
							ors will be reported; Energy will be set to zero
					enc1	1	Normal ESM mode
					enc2	2	Reserved
					enc3	3	Reserved

1.11.	72 esmi_cmd11				Reg.	0xA02101E4			
The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM									
bits	name	s/w	h/w	default			desc	cription	
15:14	c1_c0	rw	ro	0x0		enum:esmi_cmo	,,	ng	
						enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a	

						enc1	1	read opera tion Register wr ite
						enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
						enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	E	SM Register Addres	SS	-
7:0	d7_d0	rw	ro	0x0	E	SM Optional Write [	Data Field	

1.11.	73 esmi_32dat11					Reg.	0xA02101E8
The b	oottom 16 bits of this r	egister are	a mirr	or of esmi_da	t		
bits	name	s/w	h/w	default		descrip	
31	ce3	ro	WO	0x0	ister read)	_	ved byte (BPAM indirect reg-
30	ce2	ro	WO	0x0	1 = CRC error on read)	high received	byte (BPAM indirect registe
29	ce1	ro	wo	0x0	1 = CRC error on read, FN2 param		byte (BPAM indirect register
28	ce0	ro	wo	0x0			ed byte (BPAM indirect reg- , FN1 parameter read, direct
27	fe3	ro	wo	0x0	1 = Frame error ( indirect register re		ghest received byte (BPAM
26	fe2	ro	wo	0x0	1 = Frame error ( rect register read		gh received byte (BPAM indi-
25	fe1	ro	wo	0x0	1 = Frame error ( rect register read		w received byte (BPAM indier read)
24	fe0	ro	wo	0x0		ead, FN2 para	west received byte (BPAM meter read, FN1 parameter
23	rx3	ro	wo	0x0	1 = highest byte r error (BPAM indir		M_EXTDAT[31:24] without ad)
22	rx2	ro	wo	0x0	1 = high byte rece (BPAM indirect re		EXTDAT[23:16] without erro
21	rx1	ro	wo	0x0	1 = low byte rece	ved in ESM_E	EXTDAT[15:8] without error N2 parameter read)
20	rx0	ro	WO	0x0	(BPAM indirect re rameter read) or	gister read, FI	M_EXTDAT[7:0] without error N2 parameter read, FN1 pa- [7:0] without error (direct reg-
17	txfe	ro	wo	0x0			mpty (512 positions). 0 =
16	tx8e	ro	wo	0x0		as at least 8 e	mpty positions. 0 =
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Statu	IS	
					enum:esmi_dat_ Name	t_encoding Value	Docariation
							Description Framing or
					enc0	0	CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d

					encF	15	Indicates E SM is in po wer up stat
							е .
7:0	d7 d0	ro	wo	0x0	ESM/BPAM direct re-	gister read data	

# 1.11.74 esmi\_tdly11



0xA02101EC

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

#### 0xA02101F4 1.11.75 esmi\_fncmd11 Reg. This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM. bits name s/w h/w default description fnc 28 ro 0x0 ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write 27:26 f1\_f0 rw 0x0 FN access type: ro 10 = FN1 access (FN + 1 parameter byte) 11 = FN2 access (FN + 2 parameter bytes) others = reserved 25:22 fn3 fn0 rw ro 0x0 ESM/BPAM Function Number to be accessed 21:16 fa5\_fa0 ESM/BPAM start direct address for the FN parameter rw ro 0x0 15:8 fd15\_fd8 ESM/BPAM FN parameter high byte (FN2 access). don't ro 0x0 rw care for FN1 access 7:0 fd7\_fd0 0x0 ESM/BPAM FN parameter low byte (FN2 or FN1 access) rw ro

1.11.	76 esmi_iacmd11			Reg.	0xA02101F8				
This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w	h/w	default		descri	ption		
14	iac	rw	ro	0x0	BPAM Indirect ad 0 = Indirect regist 1 = Indirect regist	er read	nmand type:		
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass	•	to be accessed. Lowest 2 ways zero		

1.11.	77 esmi_extdat11			Reg.	0xA02101FC				
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.									
bits	name	s/w	h/w	default		description	n		
31:24	id31_id24	rw	rw	0x0	highest byte data read	[31:24] for BPAN	I indirect register write or		
23:16	id23_id16	rw	rw	0x0	high byte data [23 read	3:16] for BPAM in	direct register write or		
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15: OR	8] for BPAM indir	ect register write or read		

					low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or
					read
					OR
					lowest byte data [7:0] for FN2 or FN1 parameter read

#### 1.11.78 esmi\_ctl12

Reg.

0xA0210210

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default			description	
15	ce	ro	wo	0x0	FI	ags a bad CRC on	the latest received r	message. 1 = error
14	fe	ro	wo	0x0		ags a framing error ror	on the latest receive	ed message. 1 =
13	iatmo	rw	wo	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.			
12	iardy	ro	wo	0x0	<ul><li>1 = Indirect address sequencer ready for new command.</li><li>= Command writes will be ignored.</li></ul>			
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.			
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes			
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available			
8	tx	ro	WO	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.			
7	es	rw	rw	0x0	fo		<ul> <li>One energy integrate the fire enable state ple</li> </ul>	
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.			
					enum:esm_ctl_tr_encoding			
						Name	Value	Description
						enc0	0	normal T0 o peration (T 0 used as s

					1		ource)
					enc1	1	Reserved us
							ed by CTEC
							Operation
					enc2	2	normal MAP4
							operation
							(droplet de
							tection use
							d as source
							)
					enc3	3	enhanced MA P4 operatio
							n (HOP mode
							- see MAP4
							HOP regist
							er below)
4	fa	rw	ro	0x0	The FA bit identifies	a fast ESM. It will be	
					nave a framing error	if it does not deliver	integration data
						ed in the TDFAST re	
						st respond within the	time defined in the
					TDSLOW register.		
1:0	m1_m0	rw	ro	0x1 I	Mode bits set the op-	erating mode for this	RJ45 port.
					enum:esm_ctl_m_e	ancoding	
					Name	Value	Description
					enc0	0	Port disabl
					Crico		ed - No err
							ors will be
							reported;
							Energy will
							be set to
							zero
					enc1	1	Normal ESM
							mode
					enc2	2	Reserved
					enc3	3	Reserved

1.11.	79 esmi_cmd12					Reg.	0xA0210214
The I	ESM Command registe	r allows fo	r seled	ction of comm	ands to be perfo	rmed towards an	ESM/BPAM
bits	name	s/w	h/w	default		descrip	tion
15:14	c1_c0	rw	ro	0x0	enum:esmi_c	ommand Type	
					Name	Value	Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
					enc1	1	Register wr ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	ESM Register	Address	•
7:0	d7_d0	rw	ro	0x0	ESM Optional	Write Data Field	

bits 31 30	name ce3	s/w	h/w	default		description			
30		ro	wo	0x0	1 = CRC error or ister read)	highest received b	yte (BPAM indirect reg		
	ce2	ro	wo	0x0	read)		e (BPAM indirect registe		
29	ce1	ro	wo	0x0	read, FN2 param	eter read)	(BPAM indirect register		
28	ce0	ro	wo	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)				
26	fe2	ro	wo	0x0	1 = Frame error ( rect register read		ceived byte (BPAM indi		
25	fe1	ro	wo	0x0		timeout) on low red , FN2 parameter re	ceived byte (BPAM indi- ead)		
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)				
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)				
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)				
20	rx0	ro	WO	0x0	<ul> <li>1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read)</li> <li>or</li> <li>1 = byte received in ESM_DAT[7:0] without error (direct register read)</li> </ul>				
7	txfe	ro	wo	0x0		s completely empty ains at least one co	(512 positions). 0 = mmand.		
6	tx8e	ro	wo	0x0	1 = CMD_FIFO h	as at least 8 empty ewer than 8 empty	positions. 0 =		
5:12	t3_t0	ro	WO	0x0	ESM/BPAM Status  enum:esmi_dat_t_encoding				
					Name	Value	Description		
					enc0	0	Framing or CRC error		
					enc5	5	SPM cable n ot connecte d		
					enc8	8	Normal, val id data		
					encE	14	ESM cable n ot connecte d		
					encF	15	Indicates E SM is in po wer up stat e		

## 1.11.81 esmi\_tdly12

Reg.

0xA021021C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of

this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	82 esmi_fncmd12		0xA0210224		
This r	egister contains the read/	write a	ccess	to FN1 or FN2	2 parameters in ESM or BPAM.
bits	name	description			
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Function Number to be accessed
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start direct address for the FN parameter
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN parameter low byte (FN2 or FN1 access)

1.11.	83 esmi_iacmd12			Reg.	0xA0210228					
This	This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w		description						
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write					
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		be accessed. Lowest 2 ys zero			

1.11.	84 esmi_extdat12			Reg.	0xA021022C			
	register contains the write , or the read data for ESM			•		ead data for BPA	M indirect register	
bits	name	descriptio	n					
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write read			
23:16	id23_id16	rw	rw	0x0	high byte data [23 read	3:16] for BPAM in	direct register write or	
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15: OR low byte data [15:	-	rect register write or read leter read	
7:0	ifd7_ifd0	rw	rw	0x0	read OR	-	direct register write or N1 parameter read	

# 1.11.85 esmi\_ctl13 0xA0210240

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with [C1:C0] = [0:1]

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	wo	0x0	Flags a framing error on the latest received message. 1 = error
13	iatmo	rw	wo	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.
12	iardy	ro	wo	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available
8	tx	ro	WO	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.

enum:esm_ctl_tr_	encoding	
Name	Value	Description
enc0	0	normal T0 o peration (T 0 used as s ource)
enc1	1	Reserved us ed by CTEC Operation
enc2	2	normal MAP4 operation (droplet de tection use d as source )
enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)

4	fa	rw	ro	0x0	The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register.				
1:0	m1_m0	rw	ro	0x1	Mode bits set the operating mode for this RJ45 port.  enum:esm_ctl_m_encoding				
						Name	Value	Description	
						enc0	0	Port disabl	
								ed - No err	
								ors will be	
								reported;	
								Energy will	
								be set to	
								zero	
						enc1	1	Normal ESM	
								mode	
						enc2	2	Reserved	
						enc3	3	Reserved	

1.11.	86 esmi_cmd13					Reg.	0xA0210244
The E	ESM Command register a	allows fo	r seled	ction of comm	ands to be perforn	ned towards an	ESM/BPAM
bits	name	s/w	h/w	default		descrip	tion
15:14	c1_c0	rw	ro	0x0	ESM/BPAM Cor enum:esmi_cm	mmand Type	
					Name	Value	Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
					enc1	1	Register wr ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	ESM Register A	ddress	·
7:0	d7_d0	rw	ro	0x0	ESM Optional W	/rite Data Field	

1.11.	87 esmi_32dat13			Reg.	0xA0210248					
The I	The bottom 16 bits of this register are a mirror of esmi_dat									
bits	name	s/w	h/w	default		description	n			
31	ce3	ro	WO	0x0	1 = CRC error on ister read)	highest received	byte (BPAM indirect reg-			
30	ce2	ro	WO	0x0	1 = CRC error on read)	high received by	te (BPAM indirect register			
29	ce1	ro	wo	0x0	1 = CRC error on read, FN2 parame	•	e (BPAM indirect register			
28	ce0	ro	WO	0x0			byte (BPAM indirect reg- I1 parameter read, direct			
27	fe3	ro	WO	0x0	1 = Frame error ( indirect register re	, ,	st received byte (BPAM			
26	fe2	ro	wo	0x0	1 = Frame error ( rect register read		eceived byte (BPAM indi-			

25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)			
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)			
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)			
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)			
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)			
20	rx0	ro	WO	0x0	<ul> <li>1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or</li> <li>1 = byte received in ESM_DAT[7:0] without error (direct register read)</li> </ul>			
17	txfe	ro	wo	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.			
16	tx8e	ro	wo	0x0	1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions.			
15:12 1	t3_t0	ro v	WO	0x0	ESM/BPAM Status  enum:esmi_dat_t_encoding			
					Name Value Description			
					enc0 0 Framing or CRC error			
					enc5 5 SPM cable n ot connecte d			
					enc8 8 Normal, val id data			
					encE 14 ESM cable n ot connecte d			
					encF 15 Indicates E SM is in po wer up stat			
7.0	47 40			0.40	E CM/DDAM dispert register read data			
7:0	d7_d0	ro	WO	0x0	ESM/BPAM direct register read data			

#### 1.11.88 esmi tdly13

Reg.

0xA021024C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

#### 1.11.89 esmi fncmd13 0xA0210254 Reg. This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM. bits name s/w h/w default description fnc 28 0x0 ESM/BPAM FN Command type: ro 0 = FN parameter read 1 = FN parameter write

27:26	f1_f0	rw	ro	0x0	FN access type: 10 = FN1 access (FN + 1 parameter byte) 11 = FN2 access (FN + 2 parameter bytes) others = reserved
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Function Number to be accessed
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start direct address for the FN parameter
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN parameter low byte (FN2 or FN1 access)

1.11.	90 esmi_iacmd13			Reg.	0xA0210258				
This	This register contains the read/write access to indirect registers in BPAM.								
bits	name	s/w		description					
14	iac	rw	ro	0x0	BPAM Indirect ad 0 = Indirect registe 1 = Indirect registe	er read	nd type:		
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		pe accessed. Lowest 2 vs zero		

1.11.	91 esmi_extdat13			Reg.	0xA021025C			
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.								
bits	name	s/w	h/w	default		description	ı	
31:24	id31_id24	rw	rw	0x0	highest byte data read	[31:24] for BPAM	indirect register write or	
23:16	id23_id16	rw	rw	0x0	high byte data [23 read	:16] for BPAM ind	direct register write or	
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:: OR low byte data [15::	•	ect register write or read eter read	
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [	7:0] for BPAM ind	lirect register write or	

# 1.11.92 esmi\_ctl14 0xA0210270

read OR

lowest byte data [7:0] for FN2 or FN1 parameter read

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name		h/w	default	E	description		
15	ce	ro	wo	0x0	-		ed message. 1 = error	
14	fe	ro	WO	0x0	error		ceived message. 1 =	
13	iatmo	rw	wo	0x0	1 = Indirect addressed Sequence complete		out after 50 ms. 0 =	
12	iardy	ro	WO	0x0	= Command write	es will be ignored.	for new command. 0	
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.			
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes			
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available			
8	tx	ro	wo	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.			
7	es	rw	rw	0x0	Force energy sar forced, regardles	nple. One energy int s of the fire enable s	egration shot will be tate. Cleafred by HW.	
6:5	tr	mar	ro	0x0	1 = force energy		nergy integration (and	
0.5		rw		OXO	waveform capture ured for TR1/TR0	e) cycles. Note that i 0 = 11, then all ESMs	f any ESM is config- s will begin their wave- MAP4 HOP mode oper-	
					enum:esm_ctl_t	r_encoding		
					Name	Value	Description	
					enc0	0	normal T0 o	
							peration (T	
							0 used as s	
					4	4	ource)	
					enc1	1	Reserved us ed by CTEC	
							Operation	
					enc2	2	normal MAP4	
							operation	
							(droplet de	
							tection use	
							d as source	
							)	
					enc3	3	enhanced MA P4 operatio	
							n (HOP mode	
							- see MAP4	
							HOP regist	
							er below)	
4	fa	rw	ro	0x0		ies a fast ESM. It wi		
						rror if it does not deli		
							Γ register. If this bit is the time defined in the	
					TDSLOW registe	•	i the time defined in the	
1:0	m1_m0	rw	ro	0x1		operating mode for	this RJ45 port.	
					enum:esm_ctl_			
					Name	Value	Description	
					enc0	0	Port disabl	
							ed - No err	
							ors will be	
							reported; Energy will	
							be set to	
							zero	
					enc1	1	Normal ESM	
					1.1	1	1	

enc2	2	Reserved
enc3	3	Reserved

1.11.	93 esmi_cmd14	Reg.	0xA0210274				
The E	ESM Command register a	allows fo	r seled	ction of comm	ands to be perf	ormed toward	ls an ESM/BPAM
bits	name	s/w	h/w	default		de	escription
15:14	c1_c0	rw	ro	0x0	ESM/BPAM (	Command Typ cmd_c_enco	
					Name	Valu	ue Description
		enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion			
					enc1	1	Register wr ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma
					enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	ESM Register	r Address	
7:0	d7_d0	rw	ro	0x0	ESM Optiona		ield

1.11.	.94 esmi_32dat14				0xA0210278
The	bottom 16 bits of this r	egister are	a mirr	or of esmi_da	t
bits	name	s/w	h/w	default	description
31	ce3	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)
30	ce2	ro	wo	0x0	1 = CRC error on high received byte (BPAM indirect register read)
29	ce1	ro	wo	0x0	1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)
28	ce0	ro	WO	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)
26	fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM indirect register read)
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)
20	rx0	ro	WO	0x0	1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or 1 = byte received in ESM_DAT[7:0] without error (direct register read)

17	txfe	ro	WO	0x0		= CMD_FIFO is cor MD_FIFO contains		•
16	tx8e	ro	wo	0x0		= CMD_FIFO has a MD_FIFO has fewe		
15:12	ro wo 0x0 ESM/BPAM Status enum:esmi_dat_t_encoding							
						Name	Value	Description
						enc0	0	Framing or CRC error
						enc5	5	SPM cable n ot connecte d
						enc8	8	Normal, val id data
						encE	14	ESM cable n ot connecte d
						encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	Е	SM/BPAM direct rec	gister read data	

## 1.11.95 esmi\_tdly14

Reg. 0xA021027C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	96 esmi_fncmd14		Reg.	0xA0210284							
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.											
bits	name	desc	cription								
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write						
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved						
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number	r to be accessed				
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct addre	ess for the FN parameter				
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN pacare for FN1 acce		gh byte (FN2 access). don't				
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN p	arameter lov	w byte (FN2 or FN1 access)				

1.11.9	97 esmi_iacmd14	Reg.	0xA0210288									
This r	This register contains the read/write access to indirect registers in BPAM.											
bits	name	s/w	h/w	default		description	٦					
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type:							

					0 = Indirect register read 1 = Indirect register write
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect register address to be accessed. Lowest 2
					bits IA1:0 are assumed to be always zero

#### 1.11.98 esmi extdat14



0xA021028C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

bits	name	s/w	h/w	default	description
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

#### 1.11.99 esmi ctl15



0xA02102A0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	WO	0x0	Flags a framing error on the latest received message. 1 = error
13	iatmo	rw	WO	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.
12	iardy	ro	WO	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>
11	iarx	ro	WO	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes

9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available					
8	tx	ro	WO	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.					
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample					
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.  enum:esm_ctl_tr_encoding					
						Name	Value	Description		
						enc0	0	normal T0 o peration (T 0 used as s ource)		
						enc1	1	Reserved us ed by CTEC Operation		
						enc2	2	normal MAP4 operation (droplet de tection use d as source )		
						enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)		
4	fa	rw	ro	0x0	ha w ne	ave a framing error in the time define	a fast ESM. It will be if it does not deliver d in the TDFAST re st respond within the	integration data gister. If this bit is		
1:0	m1_m0	rw	ro	0x1		lode bits set the ope enum:esm_ctl_m_e	erating mode for this	RJ45 port.		
						Name	Value	Description		
						enc0	0	Port disabl ed - No err ors will be reported; Energy will be set to zero		
						enc1	1	Normal ESM mode		
						enc2	2	Reserved		
						enc3	3	Reserved		

1.11.100 esmi_cmd15 0xA02102A4												
The ESM Command register allows for selection of commands to be performed towards an ESM/BPAM												
bits	bits name s/w h/w default description											
15:14 c1_c0 rw ro 0x0 ESM/BPAM Command Type enum:esmi_cmd_c_encoding												
					Name	Value	Description					
					enc0	0	Register Re ad. D7:D0 a					

								re 'don't c ares' for a read opera tion	
						enc1	1	Register wr	
								ite	
						enc2	2	Tref with w	
								ave sync (W	
								aveform Cap	
								ture) comma	
								nd <sup>′</sup>	
						enc3	3	Tref, no wa	
								ve sync	
13:8	a5_a0	rw	ro	0x0		SM Register Addre			
7:0	d7_d0	rw	ro	0x0	ESM Optional Write Data Field				

1.11.	101 esmi_32dat15	5				Reg.	0xA02102A8	
The b	oottom 16 bits of this re	gister are	a mirro	or of esmi_da	t			
bits	name	s/w	h/w	default		descri		
31	ce3	ro	wo	0x0	ister read)	J	ved byte (BPAM indirect reg	
30	ce2	ro	wo	0x0	read)		d byte (BPAM indirect registe	
29	ce1	ro	WO	0x0	read, FN2 param	neter read)	byte (BPAM indirect register	
28	ce0	ro	WO	0x0	ister read, FN2 p register read)	arameter read	red byte (BPAM indirect reg- I, FN1 parameter read, direc	
27	fe3	ro	WO	0x0	indirect register r	ead)	ghest received byte (BPAM	
26	fe2	ro	wo	0x0	rect register read	d)	gh received byte (BPAM indi	
25	fe1	ro	wo	0x0	rect register read	l, FN2 parame		
24	fe0	ro	WO	0x0	indirect register r read, direct regis	ead, FN2 para ter read)	west received byte (BPAM ameter read, FN1 parameter	
23	rx3	ro	WO	0x0	1 = highest byte error (BPAM indi		SM_EXTDAT[31:24] without ead)	
22	rx2	ro	WO	0x0	(BPAM indirect re	egister read)	_EXTDAT[23:16] without erro	
21	rx1	ro	WO	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)			
20	rx0	ro	WO	0x0	(BPAM indirect read) or	egister read, F	M_EXTDAT[7:0] without erro  N2 parameter read, FN1 pa-  [7:0] without error (direct reg	
17	txfe	ro	wo	0x0			empty (512 positions). 0 = ne command.	
16	tx8e	ro	wo	0x0	1 = CMD_FIFO h		empty positions. 0 = mpty positions.	
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Stat enum:esmi_dat			
					Name	Value	Description	
					enc0	0	Framing or CRC error	
					enc5	5	SPM cable n ot connecte d	
					enc8	8	Normal, val id data	
					encE	14	ESM cable n	

								ot connecte d
						encF	15	Indicates E SM is in po wer up stat
								e
7:0	d7 d0	ro	wo	0x0	Е	SM/BPAM direct red	gister read data	

# 1.11.102 esmi\_tdly15



0xA02102AC

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	103 esmi_fncmd15	Reg.	0xA02102B4							
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.										
bits	name	s/w	h/w	default		description				
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write					
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved					
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to be	e accessed			
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	r the FN parameter			
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN pacare for FN1 acce	5 ,	te (FN2 access). don't			
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN pa	arameter low byte	e (FN2 or FN1 access)			

1.11.	104 esmi_iacmd15	Reg.	0xA02102B8						
This register contains the read/write access to indirect registers in BPAM.									
bits	name		description						
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write				
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass	•	be accessed. Lowest 2 /s zero		

1.11.	105 esmi_extdat15	Reg.	0xA02102BC							
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.										
bits	name	s/w	h/w	default		description				
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read					
23:16	id23_id16	rw	:16] for BPAM in	direct register write or						

15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

### 1.11.106 esmi\_ctl16



0xA02102D0

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

_	•		•		<u> </u>		
bits	name	s/w	h/w	default	description		
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error		
14	fe	ro	wo	0x0	Flags a framing error on the latest received message. 1 = error		
13	iatmo	rw	wo	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.		
12	iardy	ro	wo	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>		
11	iarx	ro	wo	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.		
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes		
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available		
8	tx	ro	WO	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.		
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample		
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.		
					enum:esm_ctl_tr_encoding		
					Name Value Description		
					enc0 0 normal T0 o		

								peration (T 0 used as s ource)
						enc1	1	Reserved us ed by CTEC Operation
						enc2	2	normal MAP4 operation (droplet de tection use d as source
						enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)
4	fa	rw	ro		ha w no	he FA bit identifies a ave a framing error i ithin the time define of set, the ESM mus DSLOW register.	f it does not deliver d in the TDFAST re	integration data gister. If this bit is
1:0	m1_m0	rw	ro	0x1		ode bits set the ope enum:esm_ctl_m_e	-	RJ45 port.
					ľ	Name	Value	Description
						enc0	0	Port disabl ed - No err ors will be reported;
								Energy will be set to zero
						enc1	1	Normal ESM mode
						enc2	2	Reserved
						enc3	3	Reserved

1.11.	107 esmi_cmd16					Reg.	0xA02102D4		
The E	ESM Command register al	lows fo	r selec	ction of comm	ands to be perfo	rmed towards an E	ESM/BPAM		
bits	name	s/w	h/w	default		descript	ion		
15:14	c1_c0	rw	ro	0x0	ESM/BPAM Command Type enum:esmi_cmd_c_encoding				
					Name	Value	Description		
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion		
					enc1	1	Register wr		
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd		
					enc3	3	Tref, no wa ve sync		
13:8	a5_a0	rw	ro	0x0	ESM Register	Address	,		
7:0	d7_d0	rw	ro	0x0	ESM Optional	Write Data Field			

1.11.	108 esmi_32dat1	16				Reg.	0xA02102D8		
The I	oottom 16 bits of this	register are	a mirro	or of esmi_da	:				
bits	name	s/w	h/w	default			ription		
31	ce3	ro	WO	0x0	ister read)	·			
30	ce2	ro	wo	0x0	1 = CRC error on high received byte (BPAM indirect registe read)				
29	ce1	ro	WO	0x0	1 = CRC error or read, FN2 param		d byte (BPAM indirect register		
28	ce0	ro	WO	0x0			ived byte (BPAM indirect reg- d, FN1 parameter read, direct		
27	fe3	ro	WO	0x0	1 = Frame error ( indirect register r		nighest received byte (BPAM		
26	fe2	ro	WO	0x0	1 = Frame error ( rect register read		nigh received byte (BPAM indi-		
25	fe1	ro	WO	0x0	1 = Frame error ( rect register read		ow received byte (BPAM indieter read)		
24	fe0	ro	WO	0x0		ead, FN2 par	owest received byte (BPAM rameter read, FN1 parameter		
23	rx3	ro	WO	0x0		1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)			
22	rx2	ro	WO	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)				
21	rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)				
20	rx0	ro	WO	0x0	1 = lowest byte received in ESM_EXTDAT[7:0] without error (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or 1 = byte received in ESM_DAT[7:0] without error (direct register read)				
17	txfe	ro	wo	0x0		s completely	empty (512 positions). 0 =		
16	tx8e	ro	wo	0x0		as at least 8	empty positions. 0 =		
15:12	t3_t0	ro	WO	0x0	ESM/BPAM State	us _t_encoding			
					Name	Value	Description		
					enc0	0	Framing or CRC error		
					enc5	5	SPM cable n ot connecte d		
					enc8	8	Normal, val		
					encE	14	ESM cable n ot connecte d		
					encF	15	Indicates E SM is in po wer up stat e		
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direct	ct register rea			

# 1.11.109 esmi\_tdly16



0xA02102DC

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	110 esmi_fncmd16	Reg.	0xA02102E4							
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.										
bits	name	s/w	h/w	default		description	n			
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write					
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved					
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to be	e accessed			
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	the FN parameter			
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN p care for FN1 acce	0 ,	te (FN2 access). don't			
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN p	arameter low byte	e (FN2 or FN1 access)			

1.11.	111 esmi_iacmd16	Reg.		0xA02102E8						
This register contains the read/write access to indirect registers in BPAM.										
bits name s/w h/w default description										
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write					
13:0	ia15_ia2	rw	BPAM indirect register ac bits IA1:0 are assumed to							

1.11.	112 esmi_extdat16	0xA02102EC								
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.										
bits	name	s/w	h/w	default	description					
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read					
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read					
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read					
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read					

1.11.113 esmi_ctl17	Reg.	0xA0210300
ESMI control transactions are sent and received in the eight ESM contr	ol blocks. Each block	is four 16-bit words.

The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

1) metric parameters

2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

Writes and reads to/from ESM registers are unrestricted when the TEM\_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM\_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

bits	name	s/w	h/w	default	description			
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error			
14	fe	ro	WO	0x0	Flags a framing error on the latest received message. 1 = error			
13	iatmo	rw	WO	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.			
12	iardy	ro	WO	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>			
11	iarx	ro	WO	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.			
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes			
9	rx	ro	WO	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available			
8	tx	ro	wo	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.			
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample			
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.			

enum:esm\_ctl\_tr\_encoding

enum.esm_cu_u_e	enum:esm_cti_tr_encoding								
Name	Value	Description							
enc0	0	normal T0 o							
		peration (T							
		0 used as s							
		ource)							
enc1	1	Reserved us							
		ed by CTEC							
		Operation							
enc2	2	normal MAP4							
		operation							
		(droplet de							
		tection use							
		d as source							
		)							

						enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)
4	fa	rw	ro	0x0	hav wit not TD	ve a framing error i hin the time define t set, the ESM mus SLOW register.	fast ESM. It will be f it does not deliver d in the TDFAST re t respond within the	integration data gister. If this bit is time defined in the
1:0	m1_m0	rw	ro	0x1		num:esm_ctl_m_e		
						Name	Value	Description
						enc0	0	Port disabl
								ed - No err
								ors will be
								reported;
								Energy will
								be set to
					L			zero
						enc1	1	Normal ESM mode
						enc2	2	Reserved
						enc3	3	Reserved

1.11.	114 esmi_cmd17						Reg.	0xA0210304
The E	ESM Command register a	allows fo	r seled	ction of comm	and	ls to be performed	d towards an ES	M/BPAM
bits	name	s/w	h/w	default			description	า
15:14	c1_c0	rw	ro	0x0		SM/BPAM Comm enum:esmi_cmd_	· ·	
						Name	Value	Description
						enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
						enc1	1	Register wr ite
					<u> </u>	enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
						enc3	3	Tref, no wa ve sync
13:8	a5_a0	rw	ro	0x0	Е	SM Register Add	ress	
7:0	d7_d0	rw	ro	0x0	Е	SM Optional Write	e Data Field	

1.11.	115 esmi_32dat17			Reg.	0xA0210308					
The bottom 16 bits of this register are a mirror of esmi_dat										
bits	bits name s/w h/w default description									
31	ce3	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)					
30	ce2	ro	wo	0x0	1 = CRC error on high received byte (BPAM indirect registeread)					
29	ce1	ro	wo	0x0	1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)					

28	ce0	ro	WO	0x0		n lowest received byte parameter read, FN1 p	e (BPAM indirect reg- parameter read, direct	
27	fe3	ro	WO	0x0		(timeout) on highest read)	eceived byte (BPAM	
26	fe2	ro	WO	0x0	1 = Frame error rect register read	` '	eived byte (BPAM indi-	
25	fe1	ro	WO	0x0		(timeout) on low recei d, FN2 parameter read	ved byte (BPAM indid)	
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)			
23	rx3	ro	WO	0x0		received in ESM_EX <sup>-</sup> irect register read)	TDAT[31:24] without	
22	rx2	ro	WO	0x0	1 = high byte red (BPAM indirect r		AT[23:16] without error	
21	rx1	ro	WO	0x0		eived in ESM_EXTDA egister read, FN2 par		
20	rx0	ro	WO	0x0	(BPAM indirect r rameter read) or	egister read, FN2 par	DAT[7:0] without error ameter read, FN1 pa-	
17	txfe	ro	WO	0x0		s completely empty (5 ains at least one com		
16	tx8e	ro	WO	0x0		has at least 8 empty p fewer than 8 empty po		
15:12	t3_t0	ro	WO	0x0	ESM/BPAM State			
					Name	Value	Description	
					enc0	0	Framing or CRC error	
					enc5	5	SPM cable n ot connecte d	
					enc8	8	Normal, val id data	
					encE	14	ESM cable n ot connecte d	
					encF	15	Indicates E SM is in po wer up stat e	
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ct register read data		

## 1.11.116 esmi\_tdly17



0xA021030C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	117 esmi_fncmd17		Reg.	0xA0210314							
This r	This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.										
bits	name		description	١							
28	fnc	rw	ro	0x0	ESM/BPAM FN C 0 = FN parameter 1 = FN parameter	read					
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes)  others = reserved						
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Funct	ion Number to be	accessed				
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start of	direct address for	the FN parameter				
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN pa care for FN1 acce		e (FN2 access). don't				
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN pa	arameter low byte	(FN2 or FN1 access)				

1.11.	118 esmi_iacmd17	Reg.	0xA0210318						
This register contains the read/write access to indirect registers in BPAM.									
bits	name	s/w	h/w	default	description				
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write				
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass	•	be accessed. Lowest 2 ys zero		

0xA021031C

	· · · · · · · · · · · · · · · · · · ·									
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.										
bits	name	s/w	h/w	default	description					
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read					
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read					
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read					
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read					

# 1.11.120 esmi\_ctl18 0xA0210330

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

1.11.119 esmi extdat17

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

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The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

# Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default		description			
15	ce	ro	wo	0x0			ived message. 1 = error		
14	fe	ro	WO	0x0	error		eceived message. 1 =		
13	iatmo	rw	WO	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.				
12	iardy	ro	WO	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>				
11	iarx	ro	WO	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.				
10	to	rw	ro	0x0	Enables tref overide : used to ignore TREF signal to allow multiple read/writes				
9	rx	ro	WO	0x0	Indicates when a receive message is in the ESM_DAT reg ister. 1 = message available				
8	tx	ro	wo	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.				
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW 1 = force energy sample				
6:5	tr	rw	ro	0x0	Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.  enum:esm_ctl_tr_encoding				
							Description		
					Name	Value	Description normal T0 o		
					enc0	0	peration (T 0 used as s ource)		
					enc1	1	Reserved us ed by CTEC Operation		
					enc2	2	normal MAP4 operation (droplet de tection use d as source )		
					enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)		
4	fa	rw	ro	0x0	have a framing of within the time of not set, the ESN TDSLOW regist	error if it does not do defined in the TDFA If must respond with er.	will be considered to eliver integration data ST register. If this bit is in the time defined in the		
1:0	m1_m0	rw	ro	0x1	Mode bits set th	e operating mode for	or this RJ45 port.		
					enum:esm_ctl	m encodina			
					Name	Value	Description		
					IName	value	Description		

		ed - No err ors will be reported; Energy will be set to zero
enc1	1	Normal ESM mode
enc2	2	Reserved
enc3	3	Reserved

1.11.	121 esmi_cmd18					Reg.	0xA0210334	
The E	ESM Command register a	llows fo	r selec	ction of comm	ands to be perfo	rmed towards an ES	SM/BPAM	
bits	name	s/w	h/w	default		descriptio	n	
15:14	c1_c0	rw ro	ro	0x0	ESM/BPAM Command Type enum:esmi_cmd_c_encoding			
					Name	Value	Description	
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion	
					enc1	1	Register wr ite	
						enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync	
13:8	a5_a0	rw	ro	0x0	ESM Register	Address		
7:0	d7_d0	rw	ro	0x0	ESM Optional	Write Data Field		

1.11.	122 esmi_32dat18				Reg. 0xA0210338				
The b	The bottom 16 bits of this register are a mirror of esmi_dat								
bits	name	s/w	h/w	default	description				
31	ce3	ro	WO	0x0	1 = CRC error on highest received byte (BPAM indirect register read)				
30	ce2	ro	WO	0x0	1 = CRC error on high received byte (BPAM indirect register read)				
29	ce1	ro	wo	0x0	1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)				
28	ce0	ro	wo	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
27	fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)				
26	fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM indirect register read)				
25	fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)				
24	fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
23	rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)				
22	rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without error (BPAM indirect register read)				

21	rx1	ro	WO	0x0	,	ceived in ESM_EXT	DAT[15:8] without error parameter read)
20	rx0	ro	WO	0x0	1 = lowest byte (BPAM indirect rameter read) or	e received in ESM_E t register read, FN2 p	XTDAT[7:0] without error parameter read, FN1 pawithout error (direct reg-
17	txfe	ro	wo	0x0		is completely empty ntains at least one co	y (512 positions). 0 = ommand.
16	tx8e	ro	wo	0x0		has at least 8 empt s fewer than 8 empty	
15:12				0x0	enum:esmi_d Name enc0	lat_t_encoding Value 0	Description Framing or
					erico	U	CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dir	ect register read dat	-

#### 1.11.123 esmi tdly18



0xA021033C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

#### 1.11.124 esmi fncmd18 0xA0210344 This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM. bits name s/w h/w default description 28 fnc 0x0 ESM/BPAM FN Command type: ro rw 0 = FN parameter read 1 = FN parameter write 27:26 f1\_f0 rw ro 0x0 FN access type: 10 = FN1 access (FN + 1 parameter byte) 11 = FN2 access (FN + 2 parameter bytes) others = reserved 25:22 fn3 fn0 0x0 rw ro ESM/BPAM Function Number to be accessed 21:16 fa5\_fa0 ro 0x0 ESM/BPAM start direct address for the FN parameter rw 15:8 fd15\_fd8 ro 0x0 ESM/BPAM FN parameter high byte (FN2 access). don't rw care for FN1 access

1.11.	125 esmi_iacmd18		Reg.	0xA0210348			
This register contains the read/write access to indirect registers in BPAM.							
bits	name	s/w	h/w	default		descr	iption
14	iac	rw	ro	0x0	BPAM Indirect add 0 = Indirect registe 1 = Indirect registe	er read	nmand type:
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg		s to be accessed. Lowest 2

### 1.11.126 esmi\_extdat18

Reg.

0xA021034C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

bits	name	s/w	h/w	default	description
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

## 1.11.127 esmi\_ctl19



0xA0210360

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI\_CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

1) metric parameters

2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI\_CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

bits	name	s/w	h/w	default	description
15	ce	ro	wo	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	wo	0x0	Flags a framing error on the latest received message. 1 =
					error

Sequence completed normally.   Sequence completed normally.	13	iatmo	rw	wo	0x0	1 = Indirect addr	ess sequencer time	ed out after 50 ms. 0 =			
= Command writes will be ignored.  10 to rw ov 0x0 1 = Indirect address read complete, 0 = Indirect read in progress.  10 to rw ro 0x0 Enables tred overide: used to ignore TREF signal to allow multiple read/writes  10 to rw ov 0x0 Indicates when a receive message is in the ESM_DAT register.  11 tx ro w 0x0 Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.  12 es rw rw 0x0 Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW 1 = force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW 1 = force energy sample. One energy integration pending welform captures as determined by the MAP4 HOP mode one ation.  13 enumesm_ctl_tr_encoding  14			'''		Ono	Sequence compl	leted normally.				
progress.    Progress	iardy	ro	WO	0x0	= Command writ	es will be ignored.					
multiple read/writes  8 tx	11	iarx	ro	wo	0x0		ess read complete.	0 = Indirect read in			
ister. 1 = message available  tx	10	to	rw	ro	0x0		_	e TREF signal to allow			
e.g., when the Command FIFO, which queues pending ESM_CTL register writes; is full. 1 = writes are not allower.  7 es	9	rx	ro	wo	0x0			is in the ESM_DAT reg-			
forced, regardless of the fire enable state. Cleafred by HW 1 = force energy sample  Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their wave form captures as determined by the MAP4 HOP mode operation.  enum:esm_ctl_tr_encoding    Name	8	tx	ro	WO	0x0	e.g., when the C	ommand FIFO, whi	ich queues pending			
6.5 tr rw ro 0x0 Selects the trigger source for ESM energy integration (and waveform capture) cycles. Note that if any ESM is configured for TR1/TR0 = 11, then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation.  enum:esm_ctl_tr_encoding    Name	7	es	rw	rw	0x0	forced, regardless of the fire enable state. Cleafred by HW.					
Name	6:5	tr	rw	ro	0x0	Selects the trigge waveform captur ured for TR1/TR form captures as ation.	er source for ESM en en en en en en en en en en en en en	t if any ESM is config- Ms will begin their wave-			
enc0 0 normal T0 o peration (T o used as source)  enc1 1 Reserved us ed by CTEC Operation  enc2 2 normal MAP4 operation (droplet de tection use d as source )  enc3 3 enhanced MA P4 operation (HOP mode - see MAP4 HOP regist er below)  4 fa rw ro 0x0 The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in the TDSLOW register.  1:0 m1_m0 rw ro 0x1 Mode bits set the operating mode for this RJ45 port.  enum:sem_ctl_m_encoding    Name								Description			
enc1						enc0	0	normal T0 o peration (T 0 used as s			
a fa  Tw  To  To  The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in to TDSLOW register.  To  To  To  To  To  To  To  To  To  T						enc1		Reserved us ed by CTEC Operation			
P4 operation (HOP mode - see MAP4 HOP regist er below)  4 fa rw ro 0x0 The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in t TDSLOW register.  1:0 m1_m0 rw ro 0x1 Mode bits set the operating mode for this RJ45 port.  enum:esm_ctl_m_encoding    Name   Value   Description     enc0   O   Port disableed - No errors will be reported; Energy will be set to zero						enc2	2	operation (droplet de tection use			
fa rw ro 0x0 The FA bit identifies a fast ESM. It will be considered to have a framing error if it does not deliver integration data within the time defined in the TDFAST register. If this bit is not set, the ESM must respond within the time defined in t TDSLOW register.  1:0 m1_m0 rw ro 0x1 Mode bits set the operating mode for this RJ45 port.    enum:esm_ctl_m_encoding   Name   Value   Description   enc0   0   Port disabled - No errors will be reported; Energy will be set to zero						enc3	3	P4 operatio n (HOP mode - see MAP4 HOP regist			
enum:esm_ctl_m_encoding    Name	4	fa	rw	ro	0x0	have a framing e within the time do not set, the ESM	error if it does not de efined in the TDFA must respond with	eliver integration data ST register. If this bit is			
Name Value Description enc0 0 Port disabl ed - No err ors will be reported; Energy will be set to zero	1:0	m1_m0	rw	ro	0x1	Mode bits set the	e operating mode for	or this RJ45 port.			
enc0 0 Port disabled - No errors will be reported; Energy will be set to zero											
ed - No err ors will be reported; Energy will be set to zero											
be set to zero						encu	U	ed - No err ors will be reported;			
								be set to			
mode						enc1	1	Normal ESM			
enc2 2 Reserved						enc2	2				
enc3 3 Reserved											

1.11.128 esmi\_cmd19

Reg.

0xA0210364

bits	name	s/w	h/w	default		description	
5:14	c1_c0	rw	ro	0x0	ESM/BPAM Cor	· · · · · · · · · · · · · · · · · · ·	
					Name	Value Value	Description
					enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
					enc1	1	Register wr ite
					enc2	2	Tref with w ave sync (W aveform Cap ture) comma nd
					enc3	3	Tref, no wa ve sync
3:8	a5_a0	rw	ro	0x0	ESM Register A	ddress	·
:0	d7_d0	rw	ro	0x0	ESM Optional W	/rite Data Field	

ottom 16 bits of this r name ce3	s/w		or of esmi_da	†				
ce3		h/w	default	description				
	ro	wo	0x0	1 = CRC error on highest received byte (BPAM indirect register read)				
ce2	ro	wo	0x0	<ul><li>1 = CRC error on high received byte (BPAM indirect registe read)</li></ul>				
ce1	ro	wo	0x0	<ul><li>1 = CRC error on low received byte (BPAM indirect register read, FN2 parameter read)</li></ul>				
ce0	ro	wo	0x0	1 = CRC error on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
fe3	ro	wo	0x0	1 = Frame error (timeout) on highest received byte (BPAM indirect register read)				
fe2	ro	wo	0x0	1 = Frame error (timeout) on high received byte (BPAM indirect register read)				
fe1	ro	wo	0x0	1 = Frame error (timeout) on low received byte (BPAM indirect register read, FN2 parameter read)				
fe0	ro	WO	0x0	1 = Frame error (timeout) on lowest received byte (BPAM indirect register read, FN2 parameter read, FN1 parameter read, direct register read)				
rx3	ro	wo	0x0	1 = highest byte received in ESM_EXTDAT[31:24] without error (BPAM indirect register read)				
rx2	ro	wo	0x0	1 = high byte received in ESM_EXTDAT[23:16] without erro (BPAM indirect register read)				
rx1	ro	wo	0x0	1 = low byte received in ESM_EXTDAT[15:8] without error (BPAM indirect register read, FN2 parameter read)				
rx0	ro	WO	0x0	1 = lowest byte received in ESM_EXTDAT[7:0] without erro (BPAM indirect register read, FN2 parameter read, FN1 parameter read) or				
				1 = byte received in ESM_DAT[7:0] without error (direct register read)				
txfe	ro	wo	0x0	1 = CMD_FIFO is completely empty (512 positions). 0 = CMD_FIFO contains at least one command.				
tx8e	ro	wo	0x0	1 = CMD_FIFO has at least 8 empty positions. 0 = CMD_FIFO has fewer than 8 empty positions.				
t3_t0	ro	wo	0x0	ESM/BPAM Status enum:esmi_dat_t_encoding				
f f r r	x3 x2 x1 x0 xfe x8e	ro re1 ro re0 ro x3 ro x2 ro x1 ro x0 ro x6e ro	ro wo re ro wo re ro wo re ro wo ro wo ro wo ro wo ro wo ro wo ro wo ro wo ro wo ro wo ro wo ro wo ro wo	ro wo 0x0 ro wo 0x0 ro wo 0x0 ro wo 0x0 rx3 ro wo 0x0 rx2 ro wo 0x0 rx1 ro wo 0x0 rx0 ro wo 0x0 rx6 ro wo 0x0 xx8e ro wo 0x0				

			Name	Value	Description
			enc0	0	Framing or CRC error
			enc5	5	SPM cable n ot connecte d
			enc8	8	Normal, val id data
			encE	14	ESM cable n ot connecte d
			encF	15	Indicates E SM is in po wer up stat e
_d0	ro	wo 0x0	ESM/BPAM dir	ect register read dat	 a

### 1.11.130 esmi\_tdly19



0xA021036C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

1.11.	131 esmi_fncmd19			Reg.	0xA0210374							
This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM.												
bits	name	s/w	h/w	default		description	n					
28	fnc	rw	ro	0x0	ESM/BPAM FN Command type: 0 = FN parameter read 1 = FN parameter write							
27:26	f1_f0	rw	ro	0x0	FN access type:  10 = FN1 access (FN + 1 parameter byte)  11 = FN2 access (FN + 2 parameter bytes) others = reserved							
25:22	fn3_fn0	rw	ro	0x0	ESM/BPAM Func	tion Number to be	e accessed					
21:16	fa5_fa0	rw	ro	0x0	ESM/BPAM start	direct address for	the FN parameter					
15:8	fd15_fd8	rw	ro	0x0	ESM/BPAM FN pacare for FN1 acce	0 ,	te (FN2 access). don't					
7:0	fd7_fd0	rw	ro	0x0	ESM/BPAM FN pa	arameter low byte	e (FN2 or FN1 access)					

1.11.	132 esmi_iacmd19			Reg.	0xA0210378							
This	This register contains the read/write access to indirect registers in BPAM.											
bits	name	description	า									
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write							
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		pe accessed. Lowest 2 vs zero					

### 1.11.133 esmi\_extdat19

Reg.

0xA021037C

This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.

bits	name	s/w	h/w	default	description
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15:8] for BPAM indirect register write or read OR low byte data [15:8] for FN2 parameter read
7:0	ifd7_ifd0	rw	rw	0x0	lowest byte data [7:0] for BPAM indirect register write or read OR lowest byte data [7:0] for FN2 or FN1 parameter read

### 1.11.134 esmi\_ctl20



0xA0210390

ESMI control transactions are sent and received in the eight ESM control blocks. Each block is four 16-bit words. The ESMI's registers are all accessed from the XTEC in an address portal fashion. Register writes and reads are directed through the ESM\_CMD register. The data returned from an ESM register read is available in the ESM\_DAT register.

To write to an ESMI register that is not a funtion parameter, load ESM\_CMD with

[C1:C0] = [0:1]

[A5:A0] = Address of ESM register to be written to

[D7:D0] = Data byte to be written to the byte wide register

Example:

To access the ESM's test register at ESM address 0x08:

Address Data

ESMI CMDx 0x4801 (point to Test Register, control test mux output with a 0x01)

The expanded ESM features now require more register space than what was available in the original design. To access the additional registers, a double address portal approach is employed. From an addressing point of view, there are two types of registers

- 1) metric parameters
- 2) all other registers

The metric parameters require the ESM's function select register to be first written to point to one of the potential nine funtions that are to be accessed.

Example:

If you want to write to any of the parameters affecting Function 1, you would write:

Address Data

ESMI\_CMDx 0x6001 (point to Function1 parameters by writing 0x01 to ESM addr 0x20)

ESMI CMDx 0x6107 (write a value of 0x07 in Function1's MS window delay register)

ESMI\_CMDx 0x6520 (write a value of 0x20 in Function1's LS window width register)

Writes and reads to/from ESM registers are unrestricted when the TEM\_CR[FE] bit is set to zero, otherwise ESM register accesses must be coordinated with firing operation. Although ESM register accesses are not restricted when running in free-run mode (TEM\_CR[IM] bit set), the user should note that the reads could interfere with energy returns.

bits	name	s/w	h/w	default	description
15	ce	ro	WO	0x0	Flags a bad CRC on the latest received message. 1 = error
14	fe	ro	wo	0x0	Flags a framing error on the latest received message. 1 = error
13	iatmo	rw	wo	0x0	1 = Indirect address sequencer timed out after 50 ms. 0 = Sequence completed normally.
12	iardy	ro	wo	0x0	<ul><li>1 = Indirect address sequencer ready for new command. 0</li><li>= Command writes will be ignored.</li></ul>
11	iarx	ro	WO	0x0	1 = Indirect address read complete. 0 = Indirect read in progress.
10	to	rw	ro	0x0	Enables tref overide: used to ignore TREF signal to allow multiple read/writes
9	rx	ro	wo	0x0	Indicates when a receive message is in the ESM_DAT register. 1 = message available
8	tx	ro	wo	0x0	Indicates when writes to this register are not allowed, e.g., when the Command FIFO, which queues pending ESM_CTL register writes, is full. 1 = writes are not allowed.
7	es	rw	rw	0x0	Force energy sample. One energy integration shot will be forced, regardless of the fire enable state. Cleafred by HW. 1 = force energy sample

6:5	tr	rw	ro	0x0	w ui fo	raveform capture) cy red for TR1/TR0 = 1 orm captures as dete tion.	ource for ESM energy ycles. Note that if an 1, then all ESMs wil ermined by the MAP	y ESM is config- Il begin their wave-
						enum:esm_ctl_tr_er	ncoding	
						Name	Value	Description
						enc0	0	normal T0 o peration (T 0 used as s ource)
						enc1	1	Reserved us ed by CTEC Operation
						enc2	2	normal MAP4 operation (droplet de tection use d as source )
						enc3	3	enhanced MA P4 operatio n (HOP mode - see MAP4 HOP regist er below)
4	fa	rw	ro	0x0	ha w no	ave a framing error ithin the time define	a fast ESM. It will be if it does not deliver ad in the TDFAST rest respond within the	integration data gister. If this bit is
1:0	m1_m0	rw	ro	0x1		lode bits set the ope enum:esm_ctl_m_e	erating mode for this	RJ45 port.
						Name	Value	Description
						enc0	0	Port disabl
								ed - No err ors will be reported; Energy will be set to zero
						enc1	1	Normal ESM mode
						enc2	2	Reserved
						enc3	3	Reserved

1.11.	135 esmi_cmd20		Reg.	0xA0210394				
The E	SM Command register al	lows fo	r selec	tion of comma	anc	ds to be performe	d towards an ES	SM/BPAM
bits	name	s/w	h/w	default			description	n
15:14	c1_c0	rw	ro	0x0		SM/BPAM Comr		
			enum:esmi_cmd	i_cmd_c_encoding				
						Name	Value	Description
						enc0	0	Register Re ad. D7:D0 a re 'don't c ares' for a read opera tion
						enc1	1	Register wr ite
						enc2	2	Tref with w ave sync (W

								aveform Cap ture) comma nd
						enc3	3	Tref, no wa
								ve sync
13:8	a5_a0	rw	ro	0x0	E	SM Register Addres	SS	
7:0	d7_d0	rw	ro	0x0	E	SM Optional Write [	Data Field	

1.11.	136 esmi_32dat	20				Reg.	0xA0210398			
The b	oottom 16 bits of this	register are	a mirro	or of esmi_da	t					
bits	name	s/w	h/w	default		descript	ion			
31	ce3	ro	wo	0x0	ister read)	J	ed byte (BPAM indirect reg			
30	ce2	ro	wo	0x0	read)	_	byte (BPAM indirect registe			
29	ce1	ro	wo	0x0	1 = CRC error on low received byte (BPAM indirect registeread, FN2 parameter read)					
28	ce0	ro	WO	0x0	ister read, FN2 pregister read)	arameter read,	d byte (BPAM indirect reg- FN1 parameter read, direc			
27	fe3	ro	wo	0x0	indirect register i	read)	nest received byte (BPAM			
26	fe2	ro	wo	0x0	rect register read	d)	n received byte (BPAM ind			
25	fe1	ro	wo	0x0	rect register read	d, FN2 paramete				
24	fe0	ro	WO	0x0	indirect register i read, direct regis	read, FN2 param ster read)	est received byte (BPAM neter read, FN1 parameter			
23	rx3	ro	wo	0x0	error (BPAM ind	rect register rea				
22	rx2	ro	WO	0x0	(BPAM indirect r	egister read)	EXTDAT[23:16] without erro			
21	rx1	ro	WO	0x0	(BPAM indirect r	egister read, FN	XTDAT[15:8] without error (2 parameter read)			
20	rx0	ro	wo	0x0	(BPAM indirect r rameter read) or	egister read, FN	_EXTDAT[7:0] without erro 2 parameter read, FN1 pa- 7:0] without error (direct reg			
17	txfe	ro	WO	0x0	1 = CMD_FIFO i CMD_FIFO cont		pty (512 positions). 0 = command.			
16	tx8e	ro	WO	0x0	1 = CMD_FIFO I CMD_FIFO has		npty positions. 0 =			
15:12	t3_t0	ro	WO	0x0	ESM/BPAM State					
					Name	Value	Description			
					enc0	0	Framing or CRC error			
					enc5	5	SPM cable n ot connecte d			
					enc8	8	Normal, val id data			
					encE	14	ESM cable n ot connecte d			
					encF	15	Indicates E SM is in po wer up stat e			
					I	1	1 -			

### 1.11.137 esmi\_tdly20



0xA021039C

The ESM\_TDLY register specifies the delay from the xTEC's master PrePulse or MainPulse timing references to when the Tref command is transmitted to the ESM. This register enables the timing reference received at each individual ESM to be delayed from the xTEC's internal PP/MP timing references.

Unlike the previous generation of ESMs, the Tref command at the ESM only defines the ESM's timing reference. It does not define the actual start of the metric and never defines the end of the active metric's processing. The ESM's metrics window delay and window width parameters determine the metric's window of operation as referenced from the received Tref command. This Tref command is sent to the ESM via a 10MHz asynchronous serial link. Because of this asynchronous communication link, the ESM 250MHz clock adds 4 ns of uncertainty to the absolute time of the received Tref command.

ESM\_TDLY is a 16-bit value, with units of 8 nanoseconds. The minimum value for this register is 0x21. This equates to a delay of 264ns from the cTEC's PP timing reference to when the ESM has detected its Tref timing reference. Explanation of why 0x21 is the minimum is beyond the scope of this document.

bits	name	s/w	h/w	default	description
15:0	esm_tdly	rw	ro	0x21	16-bit value for TDLY. Min 0x21. 8ns resolution.

#### 0xA02103A4 1.11.138 esmi fncmd20 Reg. This register contains the read/write access to FN1 or FN2 parameters in ESM or BPAM. name s/w h/w default description 28 fnc 0x0 ESM/BPAM FN Command type: ro 0 = FN parameter read 1 = FN parameter write 27:26 f1\_f0 rw ro 0x0 FN access type: 10 = FN1 access (FN + 1 parameter byte) 11 = FN2 access (FN + 2 parameter bytes) others = reserved 25:22 fn3 fn0 ESM/BPAM Function Number to be accessed rw ro 0x0 ESM/BPAM start direct address for the FN parameter 21:16 fa5 fa0 rw ro 0x0 15:8 fd15\_fd8 rw ro 0x0 ESM/BPAM FN parameter high byte (FN2 access). don't care for FN1 access 7:0 fd7\_fd0 0x0 ESM/BPAM FN parameter low byte (FN2 or FN1 access) rw ro

1.11.	139 esmi_iacmd20	Reg.	0xA02103A8								
This register contains the read/write access to indirect registers in BPAM.											
bits name s/w h/w default description											
14	iac	rw	ro	0x0	BPAM Indirect addressing Command type: 0 = Indirect register read 1 = Indirect register write						
13:0	ia15_ia2	rw	ro	0x0	BPAM indirect reg bits IA1:0 are ass		ess to be accessed. Lowest 2 e always zero				

1.11.	140 esmi_extdat20			Reg.	0xA02103AC						
This register contains the write data for BPAM indirect register writes, or the read data for BPAM indirect register reads, or the read data for ESM/BPAM FN1 or FN2 reads.											
bits	name	s/w	h/w	default		desc	cription				
31:24	id31_id24	rw	rw	0x0	highest byte data [31:24] for BPAM indirect register write or read						
23:16	id23_id16	rw	rw	0x0	high byte data [23:16] for BPAM indirect register write or read						
15:8	ifd15_ifd8	rw	rw	0x0	low byte data [15] OR low byte data [15]	•	Indirect register write or read parameter read				
7:0	ifd7_ifd0	rw	rw	0x0	read OR	· -	AM indirect register write or 2 or FN1 parameter read				

1.11.	141 esmi_crc				Reg.	0xA0210700
bits	name	s/w	h/w	default	de	scription
19:0	esmi_crc	ro	wo	0x0	Any CRC error detected on	on for each of the twenty ESMs. the associated ESM-to-xTEC ion. All latched bits are cleared FS register.

1.11.	142 esmi_crc_sel	Reg.	0xA0210704									
ESM	ESM CRC Error Select Register											
bits	name	s/w	h/w	default		description	١					
4:0 sel rw ro 0x0 Selects one of the 20 ESMs to source the CRC monitoring for the ESM_CRC_CNT.												

1.11.	143 esmi_crc_cnt		Reg.	0xA0210708							
ESM CRC Error Count Register											
bits	bits name s/w h/w default description										
9:0	cnt	ro	WO	0x0	CRC error count. The count increments with each CRC error detected on the ESM-to-xTEC link selected by ESM_CRC_SEL. The count freezes at 1,023, and is cleared via the CR bit in the RESETS register.						

1.11.	144 esmi_cab	Reg.	0xA0210710						
Indica	ites the status of the ESM	ls.							
bits	name	s/w	h/w	default		description			
19:0	esmi_cab	ro	wo	vo 0x0 ESM cable connect flag for each of the 20 ESMs. 1 is cab connected.					

1.11.	145 spm_cab	eg.	0xA0210714										
Indica	Indicates the status of the cable connection for SPM to its respective ESMs. One bit per ESM/SPM channel.												
bits	name	s/w	h/w	default		description	١						
19:0 spm_cab ro wo 0x0 SPM/CSPM cable connect flag for ESMs[20:1]. 1= cable connected													

1.11.	146 t9_esmi	0xA0210718								
This register indicates that an invalid (outdated T9) version device for each of the ESM is connected. When T9 ESM is detected, the ESM_CAB flag will be set to zero. There could be up to three seconds delay once the cable is inserted.										
bits	name	s/w	h/w	default		description	n			
19:0	t9_esmi	ro		ESM connect flags for each of the eight ESMs. 1=T9 dated, incompatible) ESM is connected.						

# 1.11.147 nrgy\_a1 0xA0210800

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits		s/w	h/w	default		description	1
31:28	f	ro	WO	0x0	enum:esm_sta	tus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM A C overload during inte gration
					enc6	6	ESM/xPAM D ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e

### 1.11.148 pkamp\_a1\_pktime\_a1



0xA0210804

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_status_p	okamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing

					-	enc3	3	error or n o reply  CRC error o n reply dat a from ESM/ xPAM
					-	enc4	4	SPM not con nected to E SM/xPAM
					-	enc5	5	ESM/xPAM AD C overload during inte gration
						enc6	6	ESM/xPAM Da ta not vali d
						enc8	8	BPAM Extend ed: warning condition
						encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12	2-bit amplitude valu	е	
13:0	pktime	ro	wo	0x0		ne 14-bit peak time not is fired. LSB is 4	values acquired eac ns	h time a system

# 1.11.149 nrgy\_b1 0xA0210808

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
			enc2	2	ESM/xPAM fr aming error or no repl y		
				enc3	3	CRC error o n reply dat a from ESM/ xPAM	
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali

					П			d
					Ì	enc8	8	BPAM Extend
								ed: warning
								condition
					Ì	encF	15	ESM/xPAM po
					П			wer up stat
								е
23:0	е	ro	wo	0x0	24	I-bit energy value		

### 1.11.150 pkamp\_b1\_pktime\_b1



0xA021080C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_pkamp_encodin	g
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSE		d each time a system

### 1.11.151 nrgy\_c1



0xA0210810

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits		name	s/w	h/w	default		description	
31:28	f		ro	wo	0x0			
							us_nrgy_encoding	
						Name	Value	Description
						enc0	0	Normal Ener
								gy or ESM/x
								PAM disable d
						enc1	1	ESM/xPAM ca
						enci	'	ble not con
								nected
						enc2	2	ESM/xPAM fr
								aming error
								or no repl
								у
						enc3	3	CRC error o
								n reply dat
								a from ESM/
						4	4	xPAM
						enc4	4	SPM not con
								nected to E SM/xPAM
						enc5	5	ESM/xPAM AD
						enco	3	C overload
								during inte
								gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
22.0					0.40	OA hit an annu !:		е
23:0	е		ro	wo	UXU	24-bit energy valu	ie	

### 1.11.152 pkamp\_c1\_pktime\_c1

Reg.

0xA0210814

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_statu	s_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d

					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
					enc3	3	o reply CRC error o
					encs	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
						45	condition
					encF	15	ESM/xPAM po
							wer up stat
27:16	pkamp	ro	WO	0x0	12-bit amplitude	value	e
13:0	pktime	ro	WO	0x0			red each time a system
13.0	Pittille	10	WO	UAU	shot is fired. LSE		ca caon time a system

# 1.11.153 nrgy\_a2 0xA0210818

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload

								during inte gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
								е
23:0	е	ro	wo	0x0	24	1-bit energy value		

### 1.11.154 pkamp\_a2\_pktime\_a2

Reg.

0xA021081C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	1
31:28	f	ro	wo	0x0	enum:esm_sta	itus_pkamp_encodi	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
7:16	pkamp	ro	wo	0x0	12-bit amplitude	value	,
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSI		ed each time a system

1.11.155 nrgy\_b2 0xA0210820

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
					enum:esm_status		
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
					enc3	3	CRC error o
					Crico		n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					enc6	6	gration ESM/xPAM Da
					erico	0	ta not vali
							d d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
23:0	е	ro	WO	0x0	24-bit energy value	9	

### 1.11.156 pkamp\_b2\_pktime\_b2

Reg.

0xA0210824

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_status_p	okamp_encoding	
					Name	Value	Description

					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					27.20		gration
					enc6	6	ESM/xPAM Da
							ta not vali
					enc8	8	BPAM Extend
					erico	0	ed: warning
							condition
					encF	15	ESM/xPAM po
					encr	10	wer up stat
							e wei up stat
27:16	pkamp	ro	wo	0x0	12-bit amplitude	a value	<u></u>
	pktime	ro	wo	0x0			ed each time a system
13.0	prune	10	WU	UAU	shot is fired. LS		ou each time a system

## 1.11.157 nrgy\_c2



0xA0210828

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28 f		ro	wo	0x0		utus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con

								nected to E SM/xPAM
					Ì	enc5	5	ESM/xPAM AD
								C overload
								during inte
								gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
					Ì	enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
								е
23:0	е	ro	WO	0x0	24	1-bit energy value		

### 1.11.158 pkamp\_c2\_pktime\_c2

Reg.

0xA021082C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

document.

. ..

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	

13:0	pktime	ro	wo	0x0	The 14-bit peak time values acquired each time a system
					shot is fired. LSB is 4ns

### 1.11.159 nrgy\_a3 0xA0210830

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
				Name	Value	Description	
					enc0	0	Normal Ener
							gy or ESM/x PAM disable
							d d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
					enc3	3	CRC error o
					Crico	9	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
					an oF	5	SM/xPAM ESM/xPAM AD
					enc5	5	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
						_	d
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	ESM/xPAM po
							wer up stat
00.0	_			00	04 hit		е
23:0	е	ro	wo	UXU	24-bit energy valu	ue	

### 1.11.160 pkamp\_a3\_pktime\_a3

Reg.

0xA0210834

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
						4	d FOM/ BANA
					enc1	1	ESM/xPAM ca
							ble not con
						2	nected
					enc2	2	ESM framing error or n
							o reply
					enc3	3	CRC error o
					erics	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
					01101		nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
	pkamp	ro	WO	0x0	12-bit amplitude v		
13:0	pktime	ro	WO	0x0		ime values acquired e	each time a system
					shot is fired. LSB	IS 4NS	

### 1.11.161 nrgy\_b3



0xA0210838

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28 f		ro	WO	0x0		us_nrgy_encoding	Description
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							y
					enc3	3	CRC error o

							n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy va	llue	

### 1.11.162 pkamp\_b3\_pktime\_b3



0xA021083C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po

							wer up stat e	
27:16	pkamp	ro	wo	0x0	12-bit amplitude value	e		
13:0	pktime	ro	WO	0x0	The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns			

### 1.11.163 nrgy\_c3



0xA0210840

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ta not vali
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy value	ue	

### 1.11.164 pkamp\_c3\_pktime\_c3



0xA0210844

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

document.

bits		name	s/w	h/w	default		description	
31:28	f		ro	wo	0x0			
							atus_pkamp_encoding	
						Name	Value	Description
						enc0	0	Normal Ener
								gy or ESM/x PAM disable
								d disable
						enc1	1	ESM/xPAM ca
								ble not con
								nected
						enc2	2	ESM framing
								error or n
						enc3	3	o reply CRC error o
						encs	3	n reply dat
								a from ESM/
								xPAM
						enc4	4	SPM not con
								nected to E
								SM/xPAM
						enc5	5	ESM/xPAM AD
								C overload
								during inte gration
						enc6	6	ESM/xPAM Da
						Crico		ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
27:16	pkamp		ro	wo	0x0	12-bit amplitude	value	е
13:0	pkamp		ro	WO			time values acquired e	ach time a system
.0.0	Pittino		10	****		shot is fired. LS		acii anio a oyotom

### 1.11.165 nrgy\_a4



0xA0210848

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_nrgy_encoding Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error

							1	
								or no repl
					Ш			y
					lĺ	enc3	3	CRC error o
					Ш			n reply dat
					Ш			a from ESM/
								xPAM
					Ì	enc4	4	SPM not con
								nected to E
								SM/xPAM
					Ì	enc5	5	ESM/xPAM AD
								C overload
								during inte
								gration
					ΠÌ	enc6	6	ESM/xPAM Da
								ta not vali
								d
					ΙÌ	enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
								e
23:0	е	ro	WO	0x0	24	1-bit energy value	·	`

### 1.11.166 pkamp\_a4\_pktime\_a4



0xA021084C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
						_	d
					enc8	8	BPAM Extend

					٠	encF	15	ed: warning condition ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12	2-bit amplitude value	9	
13:0	pktime	ro	WO	0x0		ne 14-bit peak time not is fired. LSB is 4	values acquired ead ns	ch time a system

### 1.11.167 nrgy\_b4



0xA0210850

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						s_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
					2021	1	ESM/xPAM ca
					enc1	I	ble not con
							nected
					enc2	2	ESM/xPAM fr
					01102		aming error
							or no repl
							y .
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
					27.25	5	SM/xPAM ESM/xPAM AD
					enc5	5	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
					000		ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
23:0	е	ro	wo	0x0	24-bit energy valu	е	

### 1.11.168 pkamp\_b4\_pktime\_b4



0xA0210854

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						tus_pkamp_encodir	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
	pkamp	ro	wo	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak the shot is fired. LSE	time values acquire 3 is 4ns	d each time a system

### 1.11.169 nrgy\_c4



There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28 f		ro	wo	0x0		tatus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con

							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							У
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
23:0	е	ro	wo	0x0	24-bit energy val	lue	

## 1.11.170 pkamp\_c4\_pktime\_c4

Reg.

0xA021085C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_statu	s_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
					ana4	4	xPAM
					enc4	4	SPM not con nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
					61100	3	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
					l euco	0	LOW/ALAW Da

								ta not vali d
					•	enc8	8	BPAM Extend ed: warning condition
						encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12	2-bit amplitude value	9	
13:0	pktime	ro	WO	0x0		ne 14-bit peak time not is fired. LSB is 4	values acquired eac ns	th time a system

### 1.11.171 nrgy\_a5



0xA0210860

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28 1	f	ro	WO	0x0	enum:esm_sta	utus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy va	llue	·

### 1.11.172 pkamp\_a5\_pktime\_a5



0xA0210864

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

/ 1/ 16/16

### A4 Spec TEM2 ESM Interface

#### document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_pkamp_encoding	- · · ·
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/ xPAM
						4	
					enc4	4	SPM not con
							nected to E SM/xPAM
					enc5	5	ESM/xPAM AD
					enco	5	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
					erico	· ·	ta not vali
							d
					enc8	8	BPAM Extend
					erico	O	ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
27:16	pkamp	ro	wo	0x0	12-bit amplitude v	/alue	-
13:0	pktime	ro	wo	0x0		me values acquired ea	ch time a system
	r · · · · ·				shot is fired. LSB		2. 3, 0.0

#### 1.11.173 nrgy\_b5

Reg.

0xA0210868

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_status_r	nrgy_encoding	
					Name	Value	Description

				enc0	0	Normal Ener
						gy or ESM/x
						PAM disable
						d
				enc1	1	ESM/xPAM ca
						ble not con
						nected
				enc2	2	ESM/xPAM fr
						aming error
						or no repl
						у
				enc3	3	CRC error o
						n reply dat
						a from ESM/
						xPAM
				enc4	4	SPM not con
						nected to E
						SM/xPAM
				enc5	5	ESM/xPAM AD
						C overload
						during inte
						gration
				enc6	6	ESM/xPAM Da
						ta not vali
						d
				enc8	8	BPAM Extend
						ed: warning
						condition
				encF	15	ESM/xPAM po
						wer up stat
						e
23:0	е	ro wo	0x0 2	24-bit energy value	·	

### 1.11.174 pkamp\_b5\_pktime\_b5



0xA021086C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	ntus_pkamp_encodir	ng
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E

					11		SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
27:16	pkamp	ro	WO	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LS		red each time a system

## 1.11.175 nrgy\_c5 0xA0210870

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description					
31:28	f	ro	wo	0x0							
						tus_nrgy_encoding					
					Name	Value	Description				
					enc0	0	Normal Ener gy or ESM/x PAM disable d				
					enc1	1	ESM/xPAM ca ble not con nected				
					enc2	2	ESM/xPAM fr aming error or no repl y				
				enc3	3	CRC error o n reply dat a from ESM/ xPAM					
			enc4	4	SPM not con nected to E SM/xPAM						
					enc5	5	ESM/xPAM AD C overload during inte gration				
					enc6	6	ESM/xPAM Da ta not vali d				
									enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e				
23:0	е	ro	wo	0x0	24-bit energy va	lue	<u> </u>				

### 1.11.176 pkamp\_c5\_pktime\_c5



0xA0210874

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm stat	us_pkamp_encoding	7
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
					4	4	d FONADANA
					enc1	1	ESM/xPAM ca ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/ xPAM
					enc4	4	SPM not con
					CHOT	-	nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da ta not vali
							d d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
27.40	nkomn		1440	0x0	12 hit amplitude	volue	е
13:0	pkamp pktime	ro ro	WO WO	0x0 0x0	12-bit amplitude		each time a system
13.0	pruitie	10	wo	UAU	shot is fired. LSB		each time a system

### 1.11.177 nrgy\_a6



0xA0210878

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d FOM/ BANA
					enc1	1	ESM/xPAM ca ble not con
							nected
					enc2	2	ESM/xPAM fr
					GIICZ	2	aming error
							or no repl
							у
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload during inte
							gration
					enc6	6	ESM/xPAM Da
					Crico		ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
23:0	е	ro	wo	0x0	24-bit energy valu	ıe	

### 1.11.178 pkamp\_a6\_pktime\_a6



0xA021087C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_st	tatus_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat

							a from ESM/ xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
27:16	pkamp	ro	WO	0x0	12-bit amplitude		
13:0	pktime	ro	wo	0x0	The 14-bit peak to shot is fired. LSE		ed each time a system

# 1.11.179 nrgy\_b6

0xA0210880

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description		
31:28	f	ro	wo	0x0	enum:esm_stat	us_nrgy_encoding		
					Name	Value	Description	
					enc0	0	Normal Ener	
							gy or ESM/x	
							PAM disable	
							d	
					enc1	1	ESM/xPAM ca	
							ble not con	
							nected	
					enc2	2	ESM/xPAM fr	
							aming error	
							or no repl	
				enc3	3	CRC error o		
							n reply dat	
								a from ESM/
						xPAM		
					enc4	4	SPM not con	
							nected to E	
							SM/xPAM	
					enc5	5	ESM/xPAM AD	
							C overload	
							during inte	
								gration
					enc6	6	ESM/xPAM Da	
							ta not vali	
					enc8	8	BPAM Extend	
				enc8	0	ed: warning		
							condition	
							CONGREGATI	

						encF	15	ESM/xPAM po
								wer up stat
								е
23:0	e	ro	wo	0x0	24	4-bit energy value		

### 1.11.180 pkamp\_b6\_pktime\_b6

Reg.

0xA0210884

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

document.

bits	name	s/w	h/w	default		description		
31:28	f	ro w	WO	0x0	enum:esm_status_pkamp_encoding			
					Name	Value	Description	
					enc0	0	Normal Ener	
					enco	U	gy or ESM/x	
							PAM disable	
							d	
					enc1	1	ESM/xPAM ca	
							ble not con	
							nected	
					enc2	2	ESM framing	
							error or n	
							o reply	
					enc3	3	CRC error o	
						n reply dat a from ESM/		
						xPAM		
				enc4	4	SPM not con		
					Ono i	'	nected to E	
						SM/xPAM		
					enc5	5	ESM/xPAM AD	
							C overload	
							during inte	
							gration	
					enc6	6	ESM/xPAM Da	
						ta not vali		
							d DDAM Fotond	
					enc8	8	BPAM Extend	
						ed: warning condition		
				encF	15	ESM/xPAM po		
				Crioi	10	wer up stat		
							e	
27:16	pkamp	ro	wo	0x0	12-bit amplitude va	alue		
13:0	pktime	ro	wo	0x0		ne values acquired ea	ch time a system	
					shot is fired. LSB is 4ns			

### 1.11.181 nrgy\_c6



0xA0210888

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

name	s/w	h/w	default		description		
f ro v	ro	WO	0x0	enum:esm_status_nrgy_encoding			
			Name	Value	Description		
			enc0	0	Normal Ener gy or ESM/x PAM disable d		
			enc1	1	ESM/xPAM ca ble not con nected		
			enc2 2	2	ESM/xPAM fr aming error or no repl y		
				enc3	3	CRC error o n reply dat a from ESM/ xPAM	
				enc4	4	SPM not con nected to E SM/xPAM	
			enc5	5	ESM/xPAM AD C overload during inte gration		
				enc6		ESM/xPAM Da ta not vali d	
				enc8	8	BPAM Extend ed: warning condition	
			encF	15	ESM/xPAM po wer up stat e		
					ro wo 0x0  enum:esm_sta  Name enc0  enc1  enc2  enc3  enc4  enc6  enc6	ro wo 0x0    enum:esm_status_nrgy_encoding   Name   Value   enc0   0     enc1	

### 1.11.182 pkamp\_c6\_pktime\_c6



0xA021088C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description		
31:28	f	ro	wo	0x0	enum:esm_status_pkamp_encoding			
					Name	Value	Description	
					enc0	0	Normal Ener gy or ESM/x PAM disable d	
					enc1	1	ESM/xPAM ca ble not con nected	
					enc2	2	ESM framing	

							error or n o reply		
					enc3	3	CRC error o		
							n reply dat a from ESM/		
							xPAM		
					enc4	4	SPM not con		
							nected to E		
							SM/xPAM		
					enc5	5	ESM/xPAM AD		
							C overload		
							during inte		
							gration		
					enc6	6	ESM/xPAM Da		
							ta not vali		
							d		
					enc8	8	BPAM Extend		
							ed: warning		
							condition		
					encF	15	ESM/xPAM po		
							wer up stat		
							е		
27:16	pkamp	ro	wo	0x0	12-bit amplitu		· · · · · · · · · · · · · · · · · · ·		
13:0	pktime	ro	wo	0x0	The 14-bit peak time values acquired each time a system				
			shot is fired. LSB is 4ns						

## 1.11.183 nrgy\_a7

0xA0210890

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro wo 0	0x0	enum:esm_status_nrgy_encoding			
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
				enc2	2	ESM/xPAM fr aming error or no repl y	
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
							enc4
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali

					11		d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
23:0	е	ro	wo	0x0	24-bit energy value	ue	

# 1.11.184 pkamp\_a7\_pktime\_a7

Reg.

0xA0210894

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

# document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	00110016577 51-1	up pkomp sesselies	
						us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
						_	nected
					enc2	2	ESM framing
							error or n
					enc3	3	o reply CRC error o
					erics	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte gration
					enc6	6	ESM/xPAM Da
					erico	0	ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
07:40	_1			00	40 hitlit- '		е
	pkamp	ro	WO		12-bit amplitude		
13:0	pktime	ro	WO		shot is fired. LSB	ime values acquired ea	ach time a system
					SHOURS HIEU. LSB	15 4115	

# 1.11.185 nrgy\_b7

Reg.

0xA0210898

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits		name	s/w	h/w	default		description	
31:28	f		ro	wo	0x0			
							us_nrgy_encoding	
						Name	Value	Description
						enc0	0	Normal Ener
								gy or ESM/x
								PAM disable d
						enc1	1	ESM/xPAM ca
						enci	'	ble not con
								nected
						enc2	2	ESM/xPAM fr
								aming error
								or no repl
								у
						enc3	3	CRC error o
								n reply dat
								a from ESM/
						4	4	xPAM
						enc4	4	SPM not con
								nected to E SM/xPAM
						enc5	5	ESM/xPAM AD
						enco	3	C overload
								during inte
								gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
22.0					0.40	OA hit an annu !:		е
23:0	е		ro	wo	UXU	24-bit energy valu	ie	

# 1.11.186 pkamp\_b7\_pktime\_b7



0xA021089C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_statu	us_pkamp_encoding	g
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d

					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
					enc3	3	o reply CRC error o
					encs	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
						45	condition
					encF	15	ESM/xPAM po
							wer up stat
27:16	pkamp	ro	WO	0x0	12-bit amplitude	value	e
13:0	pktime	ro	WO	0x0			red each time a system
13.0	Pittille	10	WO	UAU	shot is fired. LSE		ca caon time a system

# 1.11.187 nrgy\_c7 0xA02108A0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload

								during inte gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
								е
23:0	е	ro	wo	0x0	24	1-bit energy value		

# 1.11.188 pkamp\_c7\_pktime\_c7

Reg.

0xA02108A4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						tus_pkamp_encodin	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
	pkamp	ro	wo	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSE		l each time a system

1.11.189 nrgy\_a8 0xA02108A8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0			
						is_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x
							PAM disable
					enc1	1	ESM/xPAM ca
							ble not con nected
					enc2	2	ESM/xPAM fr aming error
							or no repl
							у
					enc3	3	CRC error o n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
						_	d
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	ESM/xPAM po
					encr	15	wer up stat
							e wer up stat
23:0	е	ro	wo	0x0	24-bit energy valu	e	-
	-			- •		-	

### 1.11.190 pkamp\_a8\_pktime\_a8

Reg.

0xA02108AC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
					enum:esm_status_p	okamp_encoding	
					Name	Value	Description

					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					27.20		gration
					enc6	6	ESM/xPAM Da
							ta not vali
					enc8	8	BPAM Extend
					erico	0	ed: warning
							condition
					encF	15	ESM/xPAM po
					encr	10	wer up stat
							e wei up stat
27:16	pkamp	ro	wo	0x0	12-bit amplitude	a value	<u></u>
	pktime	ro	wo	0x0			ed each time a system
13.0	prune	10	WU	UAU	shot is fired. LS		ou each time a system

# 1.11.191 nrgy\_b8



0xA02108B0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28 f		ro	wo	0x0		utus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con

							nected to E SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
23:0	е	ro	wo	0x0	24-bit energy v	alue	

# 1.11.192 pkamp\_b8\_pktime\_b8

Reg.

0xA02108B4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28 f		ro	WO	0x0	enum:esm_sta	tus_pkamp_encodir	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16 p	okamp	ro	WO	0x0	12-bit amplitude	value	<u> </u>

13:0	pktime	ro	wo	0x0	The 14-bit peak time values acquired each time a system
					shot is fired. LSB is 4ns

# 1.11.193 nrgy\_c8 0xA02108B8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x PAM disable
							d d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
					enc3	3	CRC error o
					Crico	9	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
					an oF	5	SM/xPAM ESM/xPAM AD
					enc5	5	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
						_	d
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	ESM/xPAM po
							wer up stat
00.0	_			00	04 hit		е
23:0	е	ro	wo	UXU	24-bit energy valu	ue	

# 1.11.194 pkamp\_c8\_pktime\_c8

Reg.

0xA02108BC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
						4	d FOM/ BANA
					enc1	1	ESM/xPAM ca
							ble not con
						2	nected
					enc2	2	ESM framing error or n
							o reply
					enc3	3	CRC error o
					erics	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
					01101		nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
	pkamp	ro	WO	0x0	12-bit amplitude v		
13:0	pktime	ro	WO	0x0		ime values acquired e	each time a system
					shot is fired. LSB	IS 4NS	

# 1.11.195 nrgy\_a9



0xA02108C0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							у
					enc3	3	CRC error o

							n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy va	alue	

# 1.11.196 pkamp\_a9\_pktime\_a9



0xA02108C4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

# A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
1:28 1	f	ro	WO	o 0x0	enum:esm_sta	atus_pkamp_encodi	ng
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AE C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po

							wer up stat
							e
27:16	pkamp	ro	WO	0x0	12-bit amplitude value		
13:0	pktime	ro	WO	0x0	The 14-bit peak time values acqueshot is fired. LSB is 4ns	iired ead	ch time a system

# 1.11.197 nrgy\_b9



0xA02108C8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error or no repl
							у
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E SM/xPAM
					enc5	5	ESM/xPAM AD
					GIICO	3	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	ESM/xPAM po
					31.01		wer up stat
							e
23:0	е	ro	wo	0x0	24-bit energy valu	ie	

# 1.11.198 pkamp\_b9\_pktime\_b9



0xA02108CC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm stati	us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	
13:0	pktime	ro	WO	0x0	The 14-bit peak to shot is fired. LSB	ime values acquired e is 4ns	ach time a system

# 1.11.199 nrgy\_c9



0xA02108D0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_status	s_nrgy_encoding Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error

							1	
								or no repl
					Ш			у
					lĺ	enc3	3	CRC error o
					Ш			n reply dat
					Ш			a from ESM/
								xPAM
					Ì	enc4	4	SPM not con
								nected to E
								SM/xPAM
					Ì	enc5	5	ESM/xPAM AD
								C overload
								during inte
								gration
					ΠÌ	enc6	6	ESM/xPAM Da
								ta not vali
								d
					ΙÌ	enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
								e
23:0	е	ro	WO	0x0	24	1-bit energy value	·	`

# 1.11.200 pkamp\_c9\_pktime\_c9



0xA02108D4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_statu	s_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
					27.2	2	nected
					enc2	2	ESM framing error or n
							o reply
					enc3	3	CRC error o
					01100	Ŭ	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					0006	6	gration
					enc6	6	ESM/xPAM Da ta not vali
							d lot vali
					enc8	8	BPAM Extend
					l euco	0	DI AW EXTERIO

					٠	encF	15	ed: warning condition ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12	2-bit amplitude value	9	
13:0	pktime	ro	WO	0x0		ne 14-bit peak time not is fired. LSB is 4	values acquired ead ns	ch time a system

# 1.11.201 nrgy\_a10



0xA02108D8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	e s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable d
					enc1	1	ESM/xPAM ca
					CHOT	'	ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							У
					enc3	3	CRC error o n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					enc6	6	gration ESM/xPAM Da
					erico	0	ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
00.0				0.0			е
23:0	е	ro	wo	0x0	24-bit energy valu	ne	

# 1.11.202 pkamp\_a10\_pktime\_a10



0xA02108DC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_pkamp_encodin	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x
							PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing
					CHOZ		error or n o reply
					enc3	3	CRC error o
					Crico		n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
						45	condition
					encF	15	ESM/xPAM po
							wer up stat
27:16	nkamn	ro	wo	0x0	12-bit amplitude	value	е
13:0	pkamp pktime	ro	WO	0x0			l each time a system
13.0	Prume	10	VVO	UAU	shot is fired. LSB		i each time a system

# 1.11.203 nrgy\_b10



0xA02108E0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0		tus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con

					1.1	1	
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							у
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
23:0	е	ro	WO	0x0	24-bit energy val	ue	

# 1.11.204 pkamp\_b10\_pktime\_b10

Reg.

0xA02108E4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_pkamp_encodin	g
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da

								ta not vali d
						enc8	8	BPAM Extend ed: warning condition
						encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12	!-bit amplitude value	Э	
13:0	pktime	ro	WO	0x0		ne 14-bit peak time of is fired. LSB is 4	values acquired eac ns	h time a system

# 1.11.205 nrgy\_c10



0xA02108E8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy va	lue	

# 1.11.206 pkamp\_c10\_pktime\_c10



0xA02108EC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						atus_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
						4	d FONA/-DAM
					enc1	1	ESM/xPAM ca ble not con
							nected
					enc2	2	ESM framing
					ericz	2	error or n
							o reply
					enc3	3	CRC error o
					01100		n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	
					encr	15	ESM/xPAM po wer up stat
							e e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	6
13:0	pktime	ro	WO	0x0		time values acquired ea	ach time a system
13.0	PRUME	10	WO	0.00	shot is fired. LSI		aon ume a system
					Shot is inca. Lot	D 10 1110	

# 1.11.207 nrgy\_a11

Reg.

0xA02108F0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_status_r	nrgy_encoding	
					Name	Value	Description

					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							У
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
						_	d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
23:0	е	ro	wo	0x0	24-bit energy va	lue	

# 1.11.208 pkamp\_a11\_pktime\_a11



0xA02108F4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28 f		ro	WO	0x0	enum:esm_sta	tus_pkamp_encodir	ng
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E

							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
27:16	pkamp	ro	wo	0x0	12-bit amplit		
13:0	pktime	ro	wo	0x0	The 14-bit pe shot is fired.	eak time values acquired LSB is 4ns	each time a system

# 1.11.209 nrgy\_b11



0xA02108F8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
					enum:esm_state	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable d
					enc1	1	ESM/xPAM ca
					enc i	1	ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							У
					enc3	3	CRC error o
							n reply dat
							a from ESM/ xPAM
					enc4	4	SPM not con
					01101		nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					_	_	gration
					enc6	6	ESM/xPAM Da
							ta not vali d
					enc8	8	BPAM Extend
					erico	0	ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е .
23:0	е	ro	wo	0x0	24-bit energy valu	ue	

# 1.11.210 pkamp\_b11\_pktime\_b11



-1 - - - -:-- 4: - --

0xA02108FC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

- l... |- l... |- |- f-...|t

#### A4 Spec TEM2 ESM Interface

#### document.

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bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_statu	us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
					enc3	3	o reply  CRC error o
					erics	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d BRAM Futural
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	ESM/xPAM po
					erici	13	wer up stat
							e wer up stat
27:16	pkamp	ro	wo	0x0	12-bit amplitude v	/alue	•
13:0	pktime	ro	wo	0x0		ime values acquired e	ach time a system
		-	-	-	shot is fired. LSB		<b>,</b>

# 1.11.211 nrgy\_c11



0xA0210900

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d FOM/ BANA
					enc1	1	ESM/xPAM ca ble not con
							nected
					enc2	2	ESM/xPAM fr
					GIICZ	2	aming error
							or no repl
							у
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload during inte
							gration
					enc6	6	ESM/xPAM Da
					Crico		ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							е
23:0	е	ro	wo	0x0	24-bit energy valu	ıe	

# 1.11.212 pkamp\_c11\_pktime\_c11



0xA0210904

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	)
31:28 f		ro	WO	0x0	enum:esm_state	us_pkamp_encodi Value	ng Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat

							a from ESM/ xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
27:16	pkamp	ro	WO	0x0	12-bit amplitude	value	
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSE		red each time a system

# 1.11.213 nrgy\_a12



0xA0210908

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
					enc3	3	CRC error o
					Crico		n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
					enc8	8	BPAM Extend
					enco	0	ed: warning
							condition
							CONGREGATI

						encF	15	ESM/xPAM po
								wer up stat
								е
23:0	е	ro	wo	0x0	24	4-bit energy value		

# 1.11.214 pkamp\_a12\_pktime\_a12

Reg.

0xA021090C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

- h... |- h... | -| -**f** - ...|t

#### A4 Spec TEM2 ESM Interface

document.

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bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_statu	us_pkamp_encoding	]
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x
							PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
	pkamp	ro	wo	0x0	12-bit amplitude v		
13:0	pktime	ro	WO	0x0	The 14-bit peak ti shot is fired. LSB		each time a system

# 1.11.215 nrgy\_b12



0xA0210910

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description		
31:28	f	ro	wo	0x0	enum:esm stat	us_nrgy_encoding		
					Name	Value	Description	
					enc0	0	Normal Ener gy or ESM/x PAM disable d	
					enc1	1	ESM/xPAM ca ble not con nected	
					enc2	2	ESM/xPAM fr aming error or no repl y	
						enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM	
					enc5	5	ESM/xPAM AD C overload during inte gration	
					enc6	6	ESM/xPAM Da ta not vali d	
					enc8	8	BPAM Extend ed: warning condition	
					encF	15	ESM/xPAM po wer up stat e	
23:0	е	ro	wo	0x0	24-bit energy val	ue		

# 1.11.216 pkamp\_b12\_pktime\_b12



0xA0210914

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_status_	pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing

							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
	pkamp	ro	WO	0x0	12-bit amplitu		
13:0	pktime	ro	WO	0x0			ed each time a system
					shot is fired.	LSB is 4ns	

# 1.11.217 nrgy\_c12



0xA0210918

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_sta	tus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali

								d
					enc8		8	BPAM Extend
								ed: warning
								condition
					encF		15	ESM/xPAM po
								wer up stat
								е
23:0	е	ro	wo	0x0	24-bit en	ergy value		

# 1.11.218 pkamp\_c12\_pktime\_c12

Reg.

0xA021091C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

# document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_pkamp_encodin	g
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSE		d each time a system

#### 1.11.219 nrgy\_a13



0xA0210920

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits		name	s/w	h/w	default		description	
31:28	f		ro	wo	0x0			
							us_nrgy_encoding	
						Name	Value	Description
						enc0	0	Normal Ener
								gy or ESM/x
								PAM disable d
						enc1	1	ESM/xPAM ca
						enci	'	ble not con
								nected
						enc2	2	ESM/xPAM fr
								aming error
								or no repl
								у
						enc3	3	CRC error o
								n reply dat
								a from ESM/
						4	4	xPAM
						enc4	4	SPM not con
								nected to E SM/xPAM
						enc5	5	ESM/xPAM AD
						enco	3	C overload
								during inte
								gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
22.0					0.40	OA hit anamay : :=!:		е
23:0	е		ro	wo	UXU	24-bit energy valu	ie	

# 1.11.220 pkamp\_a13\_pktime\_a13

Reg.

0xA0210924

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default	description				
31:28	f	ro	WO	0x0	enum:esm_stat	us_pkamp_encoding			
					Name	Value	Description		
					enc0	0	Normal Ener gy or ESM/x PAM disable d		

13:0	pktime	ro	wo	0x0	The		time values acquir	ed each time a system
27:16	pkamp	ro	wo	0x0	12-	bit amplitude	value	
						encF	15	ESM/xPAM po wer up stat e
							45	ed: warning condition
						enc8	8	ta not vali d BPAM Extend
						enc6	6	during inte gration ESM/xPAM Da
						enc5	5	ESM/xPAM AD C overload
						enc4	4	SPM not con nected to E SM/xPAM
						enc3	3	CRC error o n reply dat a from ESM/ xPAM
						enc2	2	ESM framing error or n o reply
						enc1	1	ESM/xPAM ca ble not con nected

# 1.11.221 nrgy\_b13



0xA0210928

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload

							during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	WO	0x0	24-bit energy val	ue	·

# 1.11.222 pkamp\_b13\_pktime\_b13

Reg.

0xA021092C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0		tue please englis	
						tus_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable d
					enc1	1	ESM/xPAM ca
					enci	Į į	ble not con
							nected
					enc2	2	ESM framing
					01102		error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
						-	SM/xPAM
					enc5	5	ESM/xPAM AD C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
					01100		ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
0= 40							е
	pkamp	ro	wo		12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSI	time values acquired B is 4ns	each time a system

#### 1.11.223 nrgy\_c13

Reg.

0xA0210930

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	Y =
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d FOM/ PANA
					enc1	1	ESM/xPAM ca
							ble not con nected
					enc2	2	ESM/xPAM fr
					encz	4	aming error
							or no repl
							у
					enc3	3	CRC error o
					Ciloo		n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
						45	condition
					encF	15	ESM/xPAM po
							wer up stat
00.0	_			00	0.4 1-14		е
23:0	е	ro	wo	0x0	24-bit energy val	ue	

# 1.11.224 pkamp\_c13\_pktime\_c13



0xA0210934

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
					enum:esm_status_pkamp_encoding		
					Name	Value	Description

					enc0	0	Normal Ener gy or ESM/x PAM disable
							d d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	
13:0	pktime	ro	WO	0x0		time values acquir	ed each time a system

# 1.11.225 nrgy\_a14



0xA0210938

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0.1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28 f		ro	wo	0x0		utus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con

								nected to E SM/xPAM
						enc5	5	ESM/xPAM AD
					Ш			C overload
					Ш			during inte
								gration
						enc6	6	ESM/xPAM Da
					Ш			ta not vali
					Ш			d
						enc8	8	BPAM Extend
					Ш			ed: warning
					Ш			condition
						encF	15	ESM/xPAM po
								wer up stat
								e
23:0	е	ro	WO	0x0	24	I-bit energy value	•	

# 1.11.226 pkamp\_a14\_pktime\_a14

Reg.

0xA021093C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description		
1:28 f		ro	WO	0x0		tus_pkamp_encodi		
					Name	Value	Description	
					enc0	0	Normal Ener gy or ESM/x PAM disable d	
					enc1	1	ESM/xPAM ca ble not con nected	
					enc2	2	ESM framing error or n o reply	
					enc3	3	CRC error o n reply dat a from ESM/ xPAM	
					enc4	4	SPM not con nected to E SM/xPAM	
					enc5	5	ESM/xPAM AI C overload during inte gration	
						enc6	6	ta not vali d
				enc8	8	BPAM Extend ed: warning condition		
					encF 12-bit amplitude	15	ESM/xPAM po wer up stat e	

13:0	pktime	ro	wo	0x0	The 14-bit peak time values acquired each time a system
					shot is fired. LSB is 4ns

# 1.11.227 nrgy\_b14

Reg.

0xA0210940

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
						gy or ESM/x PAM disable	
							d d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
						or no repl	
					enc3	3	CRC error o
					Cilco	9	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
				on oF	5	SM/xPAM ESM/xPAM AD	
					enc5	5	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
					_	_	d
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	ESM/xPAM po
							wer up stat
22.0		<b>nc</b>		0.40	24 bit on a ""!-		е
23:0	е	ro	wo	UXU	24-bit energy valu	ue	

# 1.11.228 pkamp\_b14\_pktime\_b14



0xA0210944

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
						4	xPAM
					enc4	4	SPM not con
							nected to E SM/xPAM
						5	ESM/xPAM AD
					enc5	5	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
					enco	0	ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e e
27:16	pkamp	ro	wo	0x0	12-bit amplitude va	lue	-
13:0	pktime	ro	wo	0x0	•	e values acquired ea	ch time a system
	•				shot is fired. LSB is		,

# 1.11.229 nrgy\_c14



0xA0210948

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description			
31:28 f		ro wo 0x0  enum:esm_status_nrgy_encoding							
					Name	Value	Description		
					enc0	0	Normal Ener		
							gy or ESM/x		
							PAM disable		
							d		
					enc1	1	ESM/xPAM ca		
							ble not con		
							nected		
					enc2	2	ESM/xPAM fr		
							aming error		
							or no repl		
							y		
					enc3	3	CRC error o		

							n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy va	alue	

# 1.11.230 pkamp\_c14\_pktime\_c14



0xA021094C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
					27.22	3	o reply  CRC error o
				ence	enc3	3	n reply dat
							a from ESM/
							xPAM
				enc4	4	SPM not con	
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
					<del>    </del>	1-	condition
					encF	15	ESM/xPAM po

						wer up stat		
						е		
27:16	pkamp	ro	WO	0x0	12-bit amplitude value			
13:0	pktime	ro	WO		The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns			

## 1.11.231 nrgy\_a15



0xA0210950

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ta not vali
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy value	ue	

#### 1.11.232 pkamp\_a15\_pktime\_a15



0xA0210954

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

document.

bits	name	s/w	h/w	default		description	า
31:28	f	ro	wo	0x0			
						tus_pkamp_encod	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	·
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSE		ed each time a system

## 1.11.233 nrgy\_b15



0xA0210958

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_nrgy_encoding Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error

					enc3	3	or no repl y CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	WO	0x0	24-bit energy val	ue	

## 1.11.234 pkamp\_b15\_pktime\_b15



0xA021095C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_statu	s_pkamp_encoding	
				Name	Value	Description	
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
					27.2	2	nected
					enc2	2	ESM framing error or n
							o reply
					enc3	3	CRC error o
					01100	Ŭ	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					0006	6	gration
					enc6	6	ESM/xPAM Da ta not vali
							d lot vali
					enc8	8	BPAM Extend
					l euco	0	DI AW EXTERIO

					٠	encF	15	ed: warning condition ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12	2-bit amplitude value	9	
13:0	pktime	ro	WO	0x0		ne 14-bit peak time not is fired. LSB is 4	values acquired ead ns	ch time a system

## 1.11.235 nrgy\_c15



0xA0210960

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
					enc1	1	ESM/xPAM ca
					enci	'	ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							у
					enc3	3	CRC error o
							n reply dat
							a from ESM/
					4	4	xPAM
					enc4	4	SPM not con nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
					GIICO	3	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
						15	condition
					encF	15	ESM/xPAM po
							wer up stat
22.0			1110	0.40	24 bit operation	10	е
23:0	е	ro	wo	UXU	24-bit energy valu	ıe	

## 1.11.236 pkamp\_c15\_pktime\_c15



0xA0210964

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

bits		name	s/w	h/w	default		description	
31:28	f		ro	wo	0x0			
							tus_pkamp_encodir	
						Name	Value	Description
						enc0	0	Normal Ener
								gy or ESM/x
								PAM disable
						4	4	d FOM/s DAM = =
						enc1	1	ESM/xPAM ca
								ble not con nected
						enc2	2	
						encz	2	ESM framing error or n
								o reply
						enc3	3	CRC error o
						erics	3	n reply dat
								a from ESM/
								xPAM
						enc4	4	SPM not con
								nected to E
								SM/xPAM
						enc5	5	ESM/xPAM AD
								C overload
								during inte
								gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
07.46						1017		е
	pkamp		ro	wo	0x0	12-bit amplitude		
13:0	pktime		ro	wo	0x0	shot is fired. LSE		d each time a system

# 1.11.237 nrgy\_a16



0xA0210968

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default	description				
31:28 f		ro	wo	0x0		tatus_nrgy_encoding			
					Name	Value	Description		
					enc0	0	Normal Ener gy or ESM/x PAM disable d		
					enc1	1	ESM/xPAM ca ble not con		

					1.1	1	1
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							у
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
23:0	е	ro	wo	0x0	24-bit energy value	ue	

# 1.11.238 pkamp\_a16\_pktime\_a16

Reg.

0xA021096C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

## A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_state	us_pkamp_encoding	3
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
					enc3	3	o reply  CRC error o
					enco	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da

								ta not vali d	
						enc8	8	BPAM Extend ed: warning condition	
						encF	15	ESM/xPAM po wer up stat e	
27:16	pkamp	ro	wo	0x0	12-bit amplitude value				
13:0	pktime	ro	WO	0x0	The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns				

## 1.11.239 nrgy\_b16



0xA0210970

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
						enc6	6
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy va	lue	

## 1.11.240 pkamp\_b16\_pktime\_b16



0xA0210974

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

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to E
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load
inte
PAM Da
/ali
Fytond
Extend rning
on
PAM po
stat
Julia
system
-,
ic

## 1.11.241 nrgy\_c16



0xA0210978

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_status_r	nrgy_encoding	
					Name	Value	Description

				enc0	0	Normal Ener
						gy or ESM/x
						PAM disable
						d
				enc1	1	ESM/xPAM ca
						ble not con
						nected
				enc2	2	ESM/xPAM fr
						aming error
						or no repl
						у
				enc3	3	CRC error o
						n reply dat
						a from ESM/
						xPAM
				enc4	4	SPM not con
						nected to E
						SM/xPAM
				enc5	5	ESM/xPAM AD
						C overload
						during inte
						gration
				enc6	6	ESM/xPAM Da
						ta not vali
						d
				enc8	8	BPAM Extend
						ed: warning
						condition
				encF	15	ESM/xPAM po
						wer up stat
						e
23:0	е	ro wo	0x0 2	24-bit energy value	·	

## 1.11.242 pkamp\_c16\_pktime\_c16



0xA021097C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

## A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28 f		ro	WO	0x0	enum:esm_sta	tus_pkamp_encodir	ng
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E

							SM/xPAM	
					enc5	5	ESM/xPAM AD	
							C overload	
							during inte	
							gration	
					enc6	6	ESM/xPAM Da	
							ta not vali	
							d	
					enc8	8	BPAM Extend	
							ed: warning	
							condition	
					encF	15	ESM/xPAM po	
							wer up stat	
							е	
27:16	pkamp	ro	wo	0x0	12-bit amplitude			
13:0	pktime	ro	WO	0x0	The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns			

## 1.11.243 nrgy\_a17

Reg.

0xA0210980

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits		name	s/w	h/w	default		description							
31:28	f		ro	wo	0x0									
							us_nrgy_encoding							
						Name	Value	Description						
						enc0	0	Normal Ener gy or ESM/x PAM disable d						
						enc1	1	ESM/xPAM ca ble not con nected						
						enc2	2	ESM/xPAM fr aming error or no repl y						
					enc3	3	CRC error o n reply dat a from ESM/ xPAM							
					enc4	4	SPM not con nected to E SM/xPAM							
						enc5	5	ESM/xPAM AD C overload during inte gration						
													enc6	6
												enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e							
23:0	е		ro	wo	0x0	24-bit energy val	ue							

## 1.11.244 pkamp\_a17\_pktime\_a17



0xA0210984

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

- h... l- h... -l-f-..lt

#### A4 Spec TEM2 ESM Interface

#### document.

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bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	tus_pkamp_encodin	g
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
						enc8	8
					encF	15	ESM/xPAM po wer up stat e
	pkamp	ro	wo	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak the shot is fired. LSE	time values acquired 3 is 4ns	d each time a system

## 1.11.245 nrgy\_b17



0xA0210988

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
					272	2	nected
					enc2	2	ESM/xPAM fr
							aming error or no repl
							у
					enc3	3	CRC error o
					Ciloo		n reply dat
							a from ESM/
						xPAM	
					enc4	4	SPM not con
							nected to E
						SM/xPAM	
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
						_	d
					enc8	8	BPAM Extend
							ed: warning
						4.5	condition
					encF	15	ESM/xPAM po
							wer up stat
22.0				0.40	O4 hit an arm : : : -!		е
23:0	е	ro	wo	0x0	24-bit energy value	ue	

## 1.11.246 pkamp\_b17\_pktime\_b17



0xA021098C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

## A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_sta	atus_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat

							a from ESM/ xPAM	
					enc4	4	SPM not con	
							nected to E SM/xPAM	
					enc5	5	ESM/xPAM AD	
							C overload	
							during inte	
							gration	
					enc6	6	ESM/xPAM Da	
							ta not vali	
							d	
					enc8	8	BPAM Extend	
							ed: warning	
							condition	
					encF	15	ESM/xPAM po	
							wer up stat	
							е	
	pkamp	ro	wo	0x0	12-bit amplitude va			
13:0	pktime	ro	wo	0x0	The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns			

## 1.11.247 nrgy\_c17



0xA0210990

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
				enc0	0	Normal Ener	
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
					enc3	3	CRC error o
					Crico		n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
					enc8	8	BPAM Extend
					enco	0	ed: warning
							condition
							CONGREGATI

					encF	15	ESN	//xPAM po
								up stat
							е	
23:0	е	ro	wo	0x0	24-bit energy va	alue	· · ·	

## 1.11.248 pkamp\_c17\_pktime\_c17

Reg.

0xA0210994

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_stat	us_pkamp_encodin	g
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable
					enc1	1	d ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
	pkamp	ro	wo	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak t shot is fired. LSB		d each time a system

## 1.11.249 nrgy\_a18



0xA0210998

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits		s/w	h/w	default		description	1
1:28	3 f	ro	WO	0x0	enum:esm_sta	tus_nrgy_encoding	
				Name	Value	Description	
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e

## 1.11.250 pkamp\_a18\_pktime\_a18



0xA021099C

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

## A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_status_	pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing

					-	enc3	3	error or n o reply  CRC error o n reply dat a from ESM/ xPAM
					-	enc4	4	SPM not con nected to E SM/xPAM
					-	enc5	5	ESM/xPAM AD C overload during inte gration
						enc6	6	ESM/xPAM Da ta not vali d
						enc8	8	BPAM Extend ed: warning condition
						encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12	2-bit amplitude valu	е	
13:0	pktime	ro	wo	0x0		ne 14-bit peak time not is fired. LSB is 4	values acquired eac ns	h time a system

## 1.11.251 nrgy\_b18



There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description			
31:28 f		ro wo 0	0x0	enum:esm_status_nrgy_encoding					
				Name	Value	Description			
				enc0 0		Normal Ener gy or ESM/x PAM disable d			
					enc1	1	ESM/xPAM ca ble not con nected		
					enc2	2	ESM/xPAM fr aming error or no repl y		
					enc3	3	CRC error o n reply dat a from ESM/ xPAM		
					enc4	4	SPM not con nected to E SM/xPAM		
					enc5	5	ESM/xPAM AD C overload during inte gration		
					enc6	6	ESM/xPAM Da ta not vali		

					11		d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
23:0	е	ro	wo	0x0	24-bit energy value	ue	

## 1.11.252 pkamp\_b18\_pktime\_b18

Reg.

0xA02109A4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

#### document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm sta	itus_pkamp_encodir	na
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
	pkamp	ro	WO	0x0	12-bit amplitude		
13:0	pktime	ro	WO	0x0	The 14-bit peak shot is fired. LSE		d each time a system

### 1.11.253 nrgy\_c18

Reg.

0xA02109A8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	tus_nrgy_encoding	
				Name	Value	Description	
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy va	lue	

# 1.11.254 pkamp\_c18\_pktime\_c18



0xA02109AC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

## A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default	description				
31:28	f	ro	WO	0x0	enum:esm_stat	us_pkamp_encoding			
					Name	Value	Description		
					enc0	0	Normal Ener gy or ESM/x PAM disable d		

					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	
13:0	pktime	ro	wo	0x0		time values acqui	red each time a system

# 1.11.255 nrgy\_a19



0xA02109B0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28 f		ro	WO	0x0	enum:esm_stat	tus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload

								during inte gration
						enc6	6	ESM/xPAM Da
								ta not vali
								d
						enc8	8	BPAM Extend
								ed: warning
								condition
						encF	15	ESM/xPAM po
								wer up stat
								е
23:0	е	ro	wo	0x0	24	1-bit energy value		

## 1.11.256 pkamp\_a19\_pktime\_a19

Reg.

0xA02109B4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0	enum:esm_sta	atus_pkamp_encodi	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	,
13:0	pktime	ro	wo	0x0	The 14-bit peak shot is fired. LS		ed each time a system

## 1.11.257 nrgy\_b19

Reg.

0xA02109B8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						s_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
							CRC error o
					enc3	3	I I
							n reply dat a from ESM/
							xPAM
					enc4	4	SPM not con
					enc4	4	nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
					Crico		C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e
23:0	е	ro	wo	0x0	24-bit energy valu	е	

## 1.11.258 pkamp\_b19\_pktime\_b19



0xA02109BC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_status_p	okamp_encoding	
					Name	Value	Description

					enc0	0	Normal Ener gy or ESM/x PAM disable
							d d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM framing error or n o reply
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ESM/xPAM Da ta not vali d
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	
13:0	pktime	ro	WO	0x0		time values acquir	ed each time a system

# 1.11.259 nrgy\_c19



0xA02109C0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0		atus_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con

								nected to E SM/xPAM
						enc5	5	ESM/xPAM AD C overload during inte gration
						enc6	6	ESM/xPAM Da ta not vali d
						enc8	8	BPAM Extend ed: warning condition
						encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24	-bit energy value	•	

## 1.11.260 pkamp\_c19\_pktime\_c19

Reg.

0xA02109C4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits nam	e s/w	h/w	default		description	1
1:28 f	ro	WO	0x0	enum:esm_sta	ntus_pkamp_encodi	
				Name	Value	Description
				enc0	0	Normal Ener gy or ESM/x PAM disable d
				enc1	1	ESM/xPAM ca ble not con nected
				enc2	2	ESM framing error or n o reply
				enc3	3	CRC error o n reply dat a from ESM/ xPAM
				enc4	4	SPM not con nected to E SM/xPAM
				enc5	5	ESM/xPAM AD C overload during inte gration
				enc6	6	ESM/xPAM Da ta not vali d
				enc8	8	BPAM Extend ed: warning condition
				encF 12-bit amplitude	15	ESM/xPAM po wer up stat e

13:0	pktime	ro	wo	0x0	The 14-bit peak time values acquired each time a system
					shot is fired. LSB is 4ns

## 1.11.261 nrgy\_a20

Reg.

0xA02109C8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x PAM disable
							d d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM/xPAM fr
							aming error
							or no repl
					enc3	3	CRC error o
					Crico	J	n reply dat
							a from ESM/
					xPAM		
					enc4	4	SPM not con
							nected to E
					an oF	5	SM/xPAM ESM/xPAM AD
					enc5	5	C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
						_	d
					enc8	8	BPAM Extend
							ed: warning condition
					encF	15	ESM/xPAM po
							wer up stat
00.0	_			00	04 hit		е
23:0	е	ro	wo	UXU	24-bit energy valu	ue	

## 1.11.262 pkamp\_a20\_pktime\_a20



0xA02109CC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
					enum:esm_statu	is_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d FOM/ BANA
					enc1	1	ESM/xPAM ca
							ble not con nected
					enc2	2	ESM framing
					ericz	2	error or n
							o reply
					enc3	3	CRC error o
							n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
					27.20	6	gration ESM/xPAM Da
					enc6	б	ta not vali
							d flot vali
					enc8	8	BPAM Extend
					Crico		ed: warning
							condition
					encF	15	ESM/xPAM po
							wer up stat
							e '
27:16	pkamp	ro	wo	0x0	12-bit amplitude v	alue	
13:0	pktime	ro	wo	0x0		me values acquired ea	nch time a system
					shot is fired. LSB	is 4ns	

## 1.11.263 nrgy\_b20



0xA02109D0

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

bits	name	s/w	h/w	default		description			
31:28 f		ro	WO	0x0	enum:esm_status_nrgy_encoding  Name Value Description				
					enc0	0	Normal Ener gy or ESM/x PAM disable d		
					enc1	1	ESM/xPAM ca ble not con nected		
					enc2	2	ESM/xPAM fr aming error or no repl y		
					enc3	3	CRC error o		

								n reply dat a from ESM/ xPAM
						enc4	4	SPM not con nected to E SM/xPAM
						enc5	5	ESM/xPAM AD C overload during inte gration
						enc6	6	ESM/xPAM Da ta not vali d
						enc8	8	BPAM Extend ed: warning condition
						encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24	-bit energy value		

## 1.11.264 pkamp\_b20\_pktime\_b20



0xA02109D4

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

#### A4 Spec TEM2 ESM Interface

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
							d
					enc1	1	ESM/xPAM ca
							ble not con
							nected
					enc2	2	ESM framing
							error or n
					27.22	3	o reply  CRC error o
					enc3	3	n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload
							during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
					<del>    </del>	1-	condition
					encF	15	ESM/xPAM po

						wer up stat		
						e		
27:16	pkamp	ro	WO	0x0	12-bit amplitude value			
13:0	pktime	ro	WO	0x0	The 14-bit peak time values acquired each time a system shot is fired. LSB is 4ns			

## 1.11.265 nrgy\_c20



0xA02109D8

There are three energy registers (NRGY\_a, NRGY\_b, NRGY\_c) in each ESM/xPAM. The first three metrics (Function 0,1,2) in each of

the ESMs/xPAMs provide a 24 bit integrated energy value. Each value has a four bit field that identifies the status of the energy data.

Bits E[23:0] are the 24-bit integrated energy value acquired each time a system shot is fired. This may be considered to be a positive integer ranging from

0 to 16meg (16,777,215). The data is biased such that zero energy returns nominal value 512, 1/8 of full range, allowing visibility of noise excursions or

offsets about the zero energy value. The exact gain scaling depends on setup factors in the ESM control registers; see the ESM manual.

bits	name	s/w	h/w	default		description	
31:28	f	ro	WO	0x0	enum:esm_stat	us_nrgy_encoding	
					Name	Value	Description
					enc0	0	Normal Ener gy or ESM/x PAM disable d
					enc1	1	ESM/xPAM ca ble not con nected
					enc2	2	ESM/xPAM fr aming error or no repl y
					enc3	3	CRC error o n reply dat a from ESM/ xPAM
					enc4	4	SPM not con nected to E SM/xPAM
					enc5	5	ESM/xPAM AD C overload during inte gration
					enc6	6	ta not vali
					enc8	8	BPAM Extend ed: warning condition
					encF	15	ESM/xPAM po wer up stat e
23:0	е	ro	wo	0x0	24-bit energy value	ue	

## 1.11.266 pkamp\_c20\_pktime\_c20



0xA02109DC

All energy registers (including Peak registers) are loaded at TDFAST or TDSLOW time, for fast and slow ESMs respectively. Framing, CRC, and no-reply errors are evaluated at these times. The 24-bit energy field is updated even if there is an error code. For example, it is possible to integrate ESM self-test levels even if an SPM is not connected. All energy registers (including Peak registers) are held all zero if the respective ESM mode is not 1 (i.e., if the respective ESM is not enabled).

Note: Since the Peak Amplitude and Peak Time are acquired by the same function within the ESM, the status bits of the PKAMP\_xx registers applies to the Peak Time values as well.

Full definitions of the meaning of all of these energy registers can be found in the

# A4 Spec TEM2 ESM Interface document.

bits	name	s/w	h/w	default		description	
31:28	f	ro	wo	0x0			
						us_pkamp_encoding	
					Name	Value	Description
					enc0	0	Normal Ener
							gy or ESM/x
							PAM disable
					enc1	1	ESM/xPAM ca
					0.101	·	ble not con
							nected
					enc2	2	ESM framing
							error or n
							o reply
					enc3	3	CRC error o n reply dat
							a from ESM/
							xPAM
					enc4	4	SPM not con
							nected to E
							SM/xPAM
					enc5	5	ESM/xPAM AD
							C overload during inte
							gration
					enc6	6	ESM/xPAM Da
							ta not vali
							d
					enc8	8	BPAM Extend
							ed: warning
						45	condition
					encF	15	ESM/xPAM po wer up stat
							e e
27:16	pkamp	ro	wo	0x0	12-bit amplitude	value	, ,
13:0	pktime	ro	wo	0x0		ime values acquired	each time a system
					shot is fired. LSB		-

1.11.	267 ffa_lk					Reg.	0xA0210FCC	
ESM	xPAM Channel 16 on	the eTEC i	s a de	dicated towar	ds the EESA to ga	ather the FFAQC	data	
bits	name	s/w	h/w	default		descript	ion	
15:12	ls	ro	wo	0x0	enum:eesa_sta	atus_lk_encoding	]	
					Name	Value	Description	
					enc0	0	Normal or E ESA disable d	
					enc1	1	EESA cable not connect ed	
					enc2	2	Framing err or or no re ply	
					enc3	3	CRC error o n reply dat a from EESA	
11:8	I	ro	wo	0x0	L0 and L1 are in	terlock status. L2	2 and L3 are reserved	
5:4	s2	ro	WO	0x0	Sensor 2 data status: bit 1 is spare, bit 0, when 1, indicated that the sensor 2 data (FFA_S2_X, Y and SUM) are valid			
1:0	s1	ro	WO	0x0	Sensor 1 data state that the sensor	•	re, bit 0, when 1, indicated	

1.11.	268 ffa_s1_x	Reg.	0xA0210FD0							
FFA	FFA Sensor X x-axis									
bits	name	s/w	h/w	default	des	cription				
15:0	ffa_sx_x	ro	WO	0x0	Sensor1: Signed, fixed-point Range -1 to 1-1LSB). Scaling the number with 150 in plasma coordinates. (1LSB = 4.593628 nm).	sixteen-bit X data value524 * 10^(-6) gives the position				

1.11.	269 ffa_s1_y	R	leg.	0xA0210FD4							
FFA :	FFA Sensor X y-axis										
bits	name	s/w	h/w	default		description	1				
15:0	ffa_sx_y	ro	wo	0x0	Sensor1: Signed, fix Range -1 to 1-1LSE Scaling the number in plasma coordinat (1LSB = 4.593628 r	3). with 150.524 * es.	n-bit Y data value. 10^(-6) gives the position				

1.11.	270 ffa_s1_sum	0xA0210FD8							
FFA Sensor X Sum									
bits	name	s/w	h/w	default	description				
15:0	ffa_sx_sum	ro	wo	0x0	Sensor1: Signed, fixed-point sixteen-bit Y data value. Range -1 to 1-1LSB). Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates. (1LSB = 4.593628 nm).				

1.11.	271 ffa_s2_x		0xA0210FDC								
FFA	FFA Sensor X x-axis										
bits	name	s/w	h/w	default	description						
15:0	ffa_sx_x	ro	wo	0x0	Sensor1: Signed, fixed-point sixteen-bit X data value. Range -1 to 1-1LSB). Scaling the number with 150.524 * 10^(-6) gives the position in plasma coordinates. (1LSB = 4.593628 nm).						

1.11.	272 ffa_s2_y	Reg.	0xA0210FE0							
FFA	FFA Sensor X y-axis									
bits	name	description								
15:0	ffa_sx_y	ro	WO	0x0	Range -1 to 1-1LS	SB). er with 150.524 ates.	en-bit Y data value. * 10^(-6) gives the position			

1.11.	273 ffa_s2_sum	Reg.	0xA0210FE4								
FFA S	FFA Sensor X Sum										
bits	name	s/w	h/w	default		description	١				
15:0 ffa_sx_sum ro wo 0x0 Sensor1: Signed, fixed-point sixteen-bit Y data value. Range -1 to 1-1LSB).											

Scaling the number with 150.524 * 10^(-6) gives the position
in plasma coordinates.
(1LSB = 4.593628  nm).

1.11.	274 quadcell_read_s	Reg.	0xA0210FE8							
quad	quadcell_read_sel									
bits	name	s/w	h/w	default		description	٦			
31:0	quadcell_read_s el	I								

1.11.	275 debug_wave	Reg.	0xA0210FEC							
debug_wave										
bits name s/w h/w default description										
31:0	debug_wave									

1.11.	276 wave_pkt_cnt	Reg.	0xA0210FF0								
Wave	Waveform Packet Counter										
bits	bits name s/w h/w default description										
31:0	wave_pkt_cnt	Waveform Packet	Counter								

# 1.11.277 map4\_hop 0xA0210FF4

The sixteen-bit MAP4\_HOP register determines how many droplets (as developed by the Timestamp module) must occur after the beginning of an EUV Gate before an ESM configured for MAP4 HOP mode (via b[6:5] of ESM\_CTL) initiates its next waveform capture.

Note that if any ESM is configured for TR1/TR0 = 11 (MAP4 HOP mode), then all ESMs will begin their waveform captures as determined by the MAP4 HOP mode operation. The sequence is as follows:

- 1) wait for the next scanner EUV Gate to go active (low);
- 2) count the quantity of droplets as configured via the MAP4\_HOP register;
- 3) wait for the next T0 -- waveform capture and subsequent upload occur for non-MAP4 ESMs;
- 4) wait for the next droplet detection -- waveform capture and subsequent upload occur for the MAP4 ESM (TR1/TR0 = 11).

Once a waveform has been captured by the ESMs, and uploaded to the TEM (265 droplets), then the ESMs again wait for the beginning of the next EUV Gate and MAP4\_HOP count before capturing a next waveform. Note that there is an additional 500ms delay inserted between waveform captures (the EUV Gate/HOP register operation begins after the 500ms inter-waveform period expires).

bits	name	s/w	h/w	default	description
15:0	hop	rw	ro	0x0	map4 hop

## 1.11.278 map4\_latch\_time

Reg.

0xA0210FF8

This sixteen-bit register determines the span of time (units of 8ns) after a droplet detection event (sourced from the Timestamper module) until the up-loaded MAP4 ESM metric data is latched in preparation for P2 pushes to the LC. This register is analogous to TDFAST and TDSLOW, except that, whereas those registers define counts that begin from T0 events, this register defines counts that begin with a DDM event.

bits	name	s/w	h/w	default	description
15:0	latch_time	rw	ro	0x0	map4_latch_time

#### 1.11.279 map4 keep time

Reg.

0xA0210FFC

In the absence of droplet detection events, this sixteen-bit register determines the amount of time before the FPGA switches to a keep-alive mode, whereby the TEM2 uses the internal T0 events to trigger the MAP4 ESM (instead of the normal MAP4 DDM event). When in this keep-alive mode, the MAP4 ESM is operating in tandem with the other non-MAP4 ESMs.

The resolution of this register is 10us. Thus, the keep-alive initiation timespan can be configured anywhere from 10us up to a maximum of 655ms, in increments of 10us. Writing a value of zero to this register disables the keep-alive mode, meaning that the TEM2 will never use T0 events for triggering the MAP4 ESM, and when droplet detection stops, the triggering of the DDM ESM stops as well.

This register powers-up with a value of 0x07D0, which corresponds to 20ms.

When the FPGA enters MAP4 keep-alive mode (i.e., when the keep-alive time is reached), the MAP4 HOP mode is automatically disabled. When this happens, waveform capture continues to operate normally. Note that the waveform GUI update rate is unaffected by this operation.

bits	name	s/w	h/w	default	description
15:0	keep time	rw	ro	0x7D0	map4 keep time

1.11.2	280 esmi_s0_cnt1	Reg.	0xA0211000							
	SEND0 Packet Count Register SEND0 total packet count									
bits name s/w h/w default description										
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt					

1.11.	281 esmi_s0_crc1	Reg.	0xA0211004							
	SEND0 CRC error Count Register total SEND0 CRC error count									
bits name s/w h/w default description										
3:0	s0_crc									

1.11.	282 esmi_s1_cnt1	Reg.	0xA0211008						
SEND1 Packet Count Register SEND1 total packet count									
bits	name	s/w	h/w	default		description	า		
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt				

1.11.	283 esmi_s1_crc1	Reg.	0xA021100C								
	SEND1 CRC error Count Register total SEND1 CRC error count										
bits	bits name s/w h/w default description										
3:0	s1_crc	esmi_s1_crc									

1.11.	284 esmi_s2_cnt1		Reg.	0xA0211010				
	SEND2 Packet Count Register SEND2 total packet count							
bits	name	s/w	h/w	default		description	١	
7:0	s2 cnt	rw	na	0x0	esmi_s2_cnt			

1.11.	285 esmi_s2_crc1		Reg.	0xA0211014				
	SEND2 CRC error Count Register total SEND2 CRC error count							
bits	bits name s/w h/w default description							
3:0	0 s2_crc rw na 0x0 esmi_s2_crc							

1.11.286 esmi_s7_cnt1	Reg.	0xA0211018
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	07 Packet Count Register 07 total packet count				
bits	name	s/w	h/w	default	description
7:0	s7_cnt	rw	na	0x0	esmi_s7_cnt

1.11.2	.11.287 esmi_s7_crc1 0xA021101C								
	SEND7 CRC error Count Register total SEND7 CRC error count								
bits	bits name s/w h/w default description								
3:0	o s7_crc rw na 0x0 esmi_s7_crc								

1.11.2	288 esmi_rd_cnt1			Reg.	0xA0211020			
	READ Packet Count Register READ total packet count							
bits	bits name s/w h/w default description							
7:0	rd_cnt	rw	na	0x0	esmi_rd_cnt			

1.11.	289 esmi_rd_crc1			Reg.	0xA0211024				
	READ CRC error Count Register total READ CRC error count								
bits	bits name s/w h/w default description								
3:0	O rd_crc rw na 0x0 esmi_rd_crc								

1.11.	290 esmi_da_cnt1	Reg.	0xA0211028					
Direct Address Request Count Register Direct Address request total count								
bits	bits name s/w h/w default description							
7:0	0 da_cnt rw na 0x0 esmi_da_cnt							

1.11.2	0xA021102C								
	InDirect Address Request Count Register InDirect Address request total count								
bits	bits name s/w h/w default description								
31:0	1:0 ia_cnt rw na 0x0 esmi_ia_cnt								

1.11.2	.11.292 esmi_tcmd_cnt1 0xA0211030								
	TREF without waveform Request Count Register TREF without waveform total count								
bits	bits name s/w h/w default description								
7:0	tcmd_cnt	rw	na	0x0	esmi_tcmd_cnt				

1.11.	293 esmi_twcmd_d	ent1		Reg.	0xA0211034			
TREF with waveform Request Count Register TREF with waveform total count								
bits	name	s/w	h/w	default		description	า	
31:0	twcmd_cnt	rw	esmi_twcmd_cnt					

I.11.294 esmi_dm_cn	it1				Reg.	0xA0211038
DOMO total write to read L Counts the total time for DO				art of first write to e	end of first re	ad
bits name	s/w	h/w	default		des	cription
dm_cnt	rw	na	0x0	esmi_dm_cnt		
I.11.295 esmi_s0_cnt	2				Reg.	0xA0211040
SEND0 Packet Count Regi SEND0 total packet count	ster					
bits name	s/w	h/w	default		des	cription
7:0 s0_cnt	rw	na	0x0	esmi_s0_cnt		
I.11.296 esmi_s0_crc	2				Reg.	0xA0211044
SEND0 CRC error Count R total SEND0 CRC error cou						
bits name	s/w	h/w	default		des	cription
3:0 s0_crc	rw	na	0x0	esmi_s0_crc		
1.11.297 esmi_s1_cnt	2				Reg.	0xA0211048
SEND1 Packet Count Regi SEND1 total packet count	ster					
bits name	s/w	h/w	default		des	cription
7:0 s0_cnt	rw	na	0x0	esmi_s0_cnt		
1.11.298 esmi_s1_crc	2				Reg.	0xA021104C
SEND1 CRC error Count R total SEND1 CRC error cou						
bits name	s/w	h/w	default		des	cription
3:0 s1_crc	rw	na	0x0	esmi_s1_crc		
1.11.299	2				Reg.	0xA0211050
SEND2 Packet Count Regi SEND2 total packet count	ster					
bits name	s/w	h/w	default		des	cription
7:0 s2_cnt	rw	na	0x0	esmi_s2_cnt		
1.11.300 esmi_s2_crc	2				Reg.	0xA0211054
SEND2 CRC error Count R total SEND2 CRC error cou						
bits name	s/w	h/w	default		des	cription
3:0 s2_crc	rw	na	0x0	esmi_s2_crc		
1.11.301 esmi_s7_cnt	2				Reg.	0xA0211058
SEND7 Packet Count Regi						
SEND7 Facket Count Regi	JULI I					

bits		name	s/w	h/w	default		desc	ription
:0	s7_cnt		rw	na	0x0	esmi_s7_cnt		
.11.	302 esr	ni_s7_crc2					Reg.	0xA021105C
		error Count Regis RC error count	ster					
bits		name	s/w	h/w	default		desc	ription
5:0	s7_crc		rw	na	0x0	esmi_s7_crc		
.11.	303 esr	mi_rd_cnt2					Reg.	0xA0211060
		Count Register cket count						
bits		name	s/w	h/w	default		desc	ription
<b>'</b> :0	rd_cnt		rw	na	0x0	esmi_rd_cnt		
	004	-1 -1 -					Pag	0,,10044004
.11.	304 esr	ni_rd_crc2					Reg.	0xA0211064
		ror Count Registo CC error count	er					
bits		name	s/w	h/w	default		desc	ription
:0	rd_crc		rw	na	0x0	esmi_rd_crc		
144	20E 00r	mi da anto					Reg.	0xA0211068
	305 esr	ni_da_cnt2					Reg.	0XA0211000
		Request Count request total co		er				
bits		name	s/w	h/w	default		desc	ription
<b>'</b> :0	da_cnt		rw	na	0x0	esmi_da_cnt		
1.11.	306 esr	mi_ia_cnt2					Reg.	0xA021106C
		ss Request Cour ss request total o		ster				
bits		name	s/w	h/w	default		desc	ription
31:0	ia_cnt		rw	na	0x0	esmi_ia_cnt		
1.11	307 esr	ni_tcmd_cnt2	2				Reg.	0xA0211070
TREF	without	waveform Reque	st Cou	nt Reg	gister		*****	5.0.13211010
	- without	waveform total co						
bits	tomd on	name t	s/w	h/w	default	osmi toma ont	desc	ription
':0	tcmd_cn	ι	rw	na	0x0	esmi_tcmd_cnt		
1.11.	308 esr	mi_twcmd_cr	nt2				Reg.	0xA0211074
TREF	with wav	ni_twcmd_cr veform Request ( veform total coun	Count F	Registe	er		Reg	0xA0211074
TREF	with wav	veform Request (	Count F	Registe	er default			0xA0211074

1.11.309 esmi\_dm\_cnt2

Reg.

0xA0211078

DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write to end of first read									
bits	name	s/w	h/w	default	description				
31:0									

1.11.3	310 esmi_s0_cnt3	Reg.	0xA0211080				
	00 Packet Count Register 00 total packet count						
bits	name	s/w	h/w	default		description	า
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt		

1.11.	311 esmi_s0_crc3	Reg.	0xA0211084				
	00 CRC error Count Regis SEND0 CRC error count	ter					
bits	name	s/w	h/w	default		description	า
3:0	s0_crc	rw	na	0x0	esmi_s0_crc		

1.11.	312 esmi_s1_cnt3	Reg.	0xA0211088						
SEND1 Packet Count Register SEND1 total packet count									
bits	name	s/w	h/w	default		description	า		
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt				

1.11.	313 esmi_s1_crc3	Reg.	0xA021108C							
SEND1 CRC error Count Register total SEND1 CRC error count										
bits	name	s/w	h/w	default		description	า			
3:0	s1_crc	rw	na	0x0	esmi_s1_crc					

1.11.3	314 esmi_s2_cnt3	Reg.	0xA0211090				
	02 Packet Count Register 02 total packet count						
bits	name	s/w	h/w	default		description	١
7:0	s2_cnt	rw	na	0x0	esmi_s2_cnt		

1.11.	315 esmi_s2_crc3	Reg.	0xA0211094				
	D2 CRC error Count Regis SEND2 CRC error count	ter					
bits	name	s/w	h/w	default		description	n
3:0	s2_crc	rw	na	0x0	esmi_s2_crc		

1.11.	316 esmi_s7_cnt3	Reg.	0xA0211098						
SEND7 Packet Count Register SEND7 total packet count									
bits	name	s/w	h/w	default		description	ı		
7:0	s7_cnt	rw	na	0x0	esmi_s7_cnt				

	smi_s7_crc3					Reg.	0xA021109C
	error Count Regis CRC error count	ster					
bits	name	s/w	h/w	default		desc	cription
3:0 s7_crc		rw	na	0x0	esmi_s7_crc		
I.11.318 es	smi_rd_cnt3					Reg.	0xA02110A0
READ Packe READ total p	t Count Register acket count						
bits	name	s/w	h/w	default		desc	cription
7:0 rd_cnt		rw	na	0x0	esmi_rd_cnt		
1 44 040						Reg	0vA02440A4
1.11.319 es	mi_rd_crc3					Reg.	0xA02110A4
	error Count Regist RC error count	er					
bits	name	s/w	h/w	default		desc	cription
3:0 rd_crc		rw	na	0x0	esmi_rd_crc		
1.11.320 es	smi_da_cnt3					Reg.	0xA02110A8
	ss Request Count ss request total co		er				
	ss request total co	unt	er h/w	default		desc	cription
Direct Addres	ss request total co			default 0x0	esmi_da_cnt	desc	cription
Direct Address bits 7:0 da_cnt	ss request total co name	unt s/w	h/w		esmi_da_cnt		
Direct Address bits 7:0 da_cnt	ss request total co	unt s/w	h/w		esmi_da_cnt	desc	0xA02110AC
bits 7:0 da_cnt  1.11.321 es  InDirect Addres	ss request total co name	s/w rw	h/w na		esmi_da_cnt		
Direct Address bits 7:0 da_cnt  1.11.321 es  InDirect Addr InDirect Addr bits	ss request total con name  smi_ia_cnt3 ess Request Cou	s/w rw	h/w na	0x0		Reg.	
Direct Address bits 7:0 da_cnt  1.11.321 es  InDirect Addr InDirect Addr	ss request total con name  smi_ia_cnt3  ess Request Coursess request total of	s/w rw nt Regis	h/w na	0x0	esmi_da_cnt	Reg.	0xA02110AC
Direct Address bits 7:0 da_cnt  1.11.321 es  InDirect Addr InDirect Addr bits	ss request total con name  smi_ia_cnt3  ess Request Coursess request total of	s/w rw  nt Regis count s/w	h/w na	0x0		Reg.	0xA02110AC
Direct Address bits 7:0 da_cnt  1.11.321 es  InDirect Addr InDirect Addr bits 31:0 ia_cnt	ss request total con name  smi_ia_cnt3  ess Request Coursess request total of	nt Regiscount s/w rw	h/w na	0x0		Reg.	0xA02110AC
Direct Address bits 7:0 da_cnt  1.11.321 es InDirect Addr InDirect Addr bits 31:0 ia_cnt  1.11.322 es TREF without	ss request total con name  smi_ia_cnt3  ess Request Couless request total of name	nt Regiscount s/w rw  s/w rw	h/w na ster h/w na	0x0  default 0x0		Reg.	0xA02110AC cription
Direct Address bits 7:0 da_cnt  1.11.321 es InDirect Addr InDirect Addr bits 31:0 ia_cnt  1.11.322 es TREF without	smi_ia_cnt3 ess Request Coursess Request total of name  smi_tcmd_cnt t waveform Request waveform total of name	nt Regiscount s/w rw  s/w rw	h/w na ster h/w na	0x0  default 0x0		desc	0xA02110AC cription

.11.	323 esmi_twcmd_cı	nt3				Reg.	0xA02110B4
IKE	with waveform Request	Count i	Registe	er			
TREF	with waveform total cour	nt				door	printion
	•		h/w	default	esmi twcmd cnt	desc	cription

1.11.324 esmi_dm_cnt3	Reg.	0xA02110B8
DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write	te to end of first rea	ad

Dits									
1.11.325 esmi_s0_cnt4			name	s/w				desc	cription
SENDO Packet Count Register   SENDO total packet count	31:0	dm_cnt		rw	na	0x0	esmi_dm_cnt		
SENDO Packet Count Register SENDO total packet count bits									
11.326 esmi_s0_crc4	.11.	325 esr	mi_s0_cnt4					Reg.	0xA02110C0
11.326 esmi_s0_crc4									
SENDO CRC error Count Register total SENDO CRC error count	bits		name	s/w	h/w	default		desc	cription
SENDO CRC error Count Register total SENDO CRC error count bits name s/w na 0x0 esmi_s0_crc  1.11.327 esmi_s1_cnt4	':0	s0_cnt		rw	na	0x0	esmi_s0_cnt		
total SENDO CRC error count bits	l.11.	326 esr	mi_s0_crc4					Reg.	0xA02110C4
Dits				ter					
1.1.327 esmi_s1_cnt4				s/w	h/w	default		desc	cription
SEND1 Packet Count Register SEND1 total packet count  bits name s/w h/w default description  7:0 s0_cnt nw na 0x0 esmi_s0_cnt  1.11.328 esmi_s1_crc4  SEND1 CRC error Count Register total SEND1 CRC error count  bits name s/w h/w default description  3:0 s1_crc nw na 0x0 esmi_s1_crc  1.11.329 esmi_s2_cnt4  SEND2 Packet Count Register SEND2 total packet count  bits name s/w h/w default description  3:0 s2_cnt nw na 0x0 esmi_s2_cnt  1.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  3:0 s2_crc nw na 0x0 esmi_s2_crc  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register		s0_crc					esmi_s0_crc		1 · ·
SEND1 Packet Count Register SEND1 total packet count  bits name s/w h/w default description  7:0 s0_cnt nw na 0x0 esmi_s0_cnt  1.11.328 esmi_s1_crc4  SEND1 CRC error Count Register total SEND1 CRC error count  bits name s/w h/w default description  3:0 s1_crc nw na 0x0 esmi_s1_crc  1.11.329 esmi_s2_cnt4  SEND2 Packet Count Register SEND2 total packet count  bits name s/w h/w default description  3:0 s2_cnt nw na 0x0 esmi_s2_cnt  1.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  3:0 s2_crc nw na 0x0 esmi_s2_crc  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register									
SEND1 total packet count bits name s/w h/w default description  7:0 s0_cnt rw na 0x0 esmi_s0_cnt  1.11.328 esmi_s1_crc4  SEND1 CRC error Count Register total SEND1 CRC error count bits name s/w h/w default description  3:0 s1_crc rw na 0x0 esmi_s1_crc  1.11.329 esmi_s2_cnt4  SEND2 Packet Count Register SEND2 total packet count bits name s/w h/w default description  7:0 s2_cnt rw na 0x0 esmi_s2_cnt  1.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  1.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register	1.11.	327 esr	mi_s1_cnt4					Reg.	0xA02110C8
I.11.328 esmi_s1_crc4  SEND1 CRC error Count Register total SEND1 CRC error count  bits name s/w h/w default description  I.11.329 esmi_s2_cnt4  SEND2 Packet Count Register SEND2 total packet count  bits name s/w h/w default description  SEND2 Packet Count Register SEND2 total packet count  bits name s/w h/w default description  7.0 s2_cnt rw na 0x0 esmi_s2_cnt  I.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  I.11.331 esmi_s7_cnt4  SEND7 Packet Count Register									
SEND1 CRC error Count Register total SEND1 CRC error count bits name s/w h/w default description  SEND2 Packet Count Register SEND2 total packet count bits name s/w h/w default description  SEND2 Packet Count Register SEND2 total packet count bits name s/w h/w default description  SEND2 Packet Count Register SEND2 total packet count bits name s/w h/w default description  SEND2 CRC error Count Register total SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  SEND3 CRC error Count Register total SEND3 CRC error count bits name s/w h/w default description  SEND3 Packet Count Register			name	s/w	h/w			desc	cription
SEND1 CRC error Count Register total SEND1 CRC error count  bits	7:0	s0_cnt		rw	na	0x0	esmi_s0_cnt		
SEND1 CRC error Count Register total SEND1 CRC error count  bits	1 11	328 oct	ni s1 crc/					Reg.	0xA02110CC
bits				tor					0.0.10211000
I.11.329 esmi_s2_cnt4  SEND2 Packet Count Register SEND2 total packet count bits name s/w h/w default description  I.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error count bits name s/w h/w default description  I.11.331 esmi_s7_cnt4  SEND7 Packet Count Register  OxA02110D0  OxA02110D4									
I.11.329 esmi_s2_cnt4  SEND2 Packet Count Register SEND2 total packet count  bits name s/w h/w default description  7:0 s2_cnt rw na 0x0 esmi_s2_cnt  I.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error count  bits name s/w h/w default description  3:0 s2_crc rw na 0x0 esmi_s2_crc  I.11.331 esmi_s7_cnt4  SEND7 Packet Count Register		s1 crc	name				esmi s1 cre	desc	cription
SEND2 Packet Count Register SEND2 total packet count  bits	5.0	31_00		I VV	Па	UXU	esiii_s1_cic		
SEND2 Packet Count Register SEND2 total packet count  bits	1 11	320 oer	ni s2 cnt/					Reg.	0xA02110D0
SEND2 total packet count  bits name s/w h/w default description  7:0 s2_cnt rw na 0x0 esmi_s2_cnt    .11.330 esmi_s2_crc4   Reg. OxA02110D4    SEND2 CRC error Count Register total SEND2 CRC error count  bits name s/w h/w default description   3:0 s2_crc rw na 0x0 esmi_s2_crc      .11.331 esmi_s7_cnt4   Reg. OxA02110D8    SEND7 Packet Count Register									00/10211000
7:0 s2_cnt rw na 0x0 esmi_s2_cnt  1.11.330 esmi_s2_crc4  SEND2 CRC error Count Register total SEND2 CRC error count  bits name s/w h/w default description 3:0 s2_crc rw na 0x0 esmi_s2_crc  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register									
SEND2 CRC error Count Register total SEND2 CRC error count  bits name s/w h/w default description 3:0 s2_crc rw na 0x0 esmi_s2_crc  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register			name					desc	cription
SEND2 CRC error Count Register total SEND2 CRC error count  bits name s/w h/w default description 3:0 s2_crc rw na 0x0 esmi_s2_crc  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register	7:0	s2_cnt		rw	na	0x0	esmi_s2_cnt		
SEND2 CRC error Count Register total SEND2 CRC error count  bits name s/w h/w default description 3:0 s2_crc rw na 0x0 esmi_s2_crc  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register	1 4 4	220	m: e2 eve4					Reg	0v402110D4
total SEND2 CRC error count  bits				ter				17.091	0XA02110D4
8:0 s2_crc rw na 0x0 esmi_s2_crc  1.11.331 esmi_s7_cnt4  SEND7 Packet Count Register  0xA02110D8	total								
1.11.331 esmi_s7_cnt4		02 050	name				osmi o2 oro	des	cription
SEND7 Packet Count Register	5.0	SZ_CIC		TW	па	UXU	esmi_sz_crc		
	l.11.	331 esr	mi_s7_cnt4					Reg.	0xA02110D8
SEND7 total packet count									
bits name s/w h/w default description	bits		name	s/w	h/w	default		desc	cription
7:0 s7_cnt rw na 0x0 esmi_s7_cnt		s7_cnt		rw			esmi_s7_cnt		

1.11.332 esmi\_s7\_crc4

Reg.

0xA02110DC

	SEND7 CRC error Count Register total SEND7 CRC error count									
bits	name	s/w	h/w	default	description					
3:0	s7_crc	rw	na	0x0	esmi_s7_crc					

1.11.3	1.11.333 esmi_rd_cnt4 0xA02110E0										
	READ Packet Count Register READ total packet count										
bits	bits name s/w h/w default description										
7:0	rd_cnt	rw	na	0x0	esmi_rd_cnt						

1.11.3	334 esmi_rd_crc4	Reg.	0xA02110E4								
	READ CRC error Count Register total READ CRC error count										
bits name s/w h/w default description											
3:0	rd_crc	rw	na	0x0	esmi_rd_crc						

1.11.	335 esmi_da_cnt4	Reg.	0xA02110E8								
	Direct Address Request Count Register Direct Address request total count										
bits	name	s/w	h/w	default		description	n				
7:0	da_cnt	rw	na	0x0	esmi_da_cnt						

1.11.	336 esmi_ia_cnt4	Reg.	0xA02110EC								
	InDirect Address Request Count Register InDirect Address request total count										
bits	name	s/w	h/w	default		description	1				
31:0	ia_cnt	rw	na	0x0	esmi_ia_cnt						

1.11.3	.11.337 esmi_tcmd_cnt4 0xA02110F0											
	without waveform Reque without waveform total co		nt Reg	ister								
bits	bits name s/w h/w default description											
7:0	7:0 tcmd_cnt rw na 0x0 esmi_tcmd_cnt											

1.11.	1.11.338 esmi_twcmd_cnt4 0xA02110F4											
	TREF with waveform Request Count Register TREF with waveform total count											
bits	name	s/w	h/w	default		description	ı					
31:0	31:0 twcmd_cnt rw na 0x0 esmi_twcmd_cnt											

1.11.	1.11.339 esmi_dm_cnt4 0xA02110F8											
	O total write to read Lat	•	•		rt of first write to en	d of first read						
bits	name	s/w	h/w	default		description	n					
31:0	31:0 dm_cnt rw na 0x0 esmi_dm_cnt											

1.11	.340 esi	mi_s0_cnt5					Reg.	0xA0211100
		t Count Register acket count						
bits		name	s/w	h/w	default		des	cription
:0	s0_cnt		rw	na	0x0	esmi_s0_cnt		
.11	.341 esı	mi_s0_crc5					Reg.	0xA0211104
		error Count Regis CRC error count	ter					
bits		name	s/w	h/w	default		des	cription
:0	s0_crc		rw	na	0x0	esmi_s0_crc		
.11	.342 esı	mi_s1_cnt5					Reg.	0xA0211108
		t Count Register acket count						
bits		name	s/w	h/w	default		des	cription
':0	s0_cnt		rw	na	0x0	esmi_s0_cnt		
.11	.343 esı	mi_s1_crc5					Reg.	0xA021110C
		error Count Regis CRC error count	ter					
bits		name	s/w	h/w	default		des	cription
3:0	s1_crc		rw	na	0x0	esmi_s1_crc		
.11.	.344 esı	mi_s2_cnt5					Reg.	0xA0211110
		et Count Register acket count						
bits		name	s/w	h/w	default		des	cription
':0	s2_cnt	namo	rw	na	0x0	esmi_s2_cnt	400	onp.ion
.11.	.345 esı	mi_s2_crc5					Reg.	0xA0211114
		error Count Regis	ter					
bits		name	s/w	h/w	default		des	cription
3:0	s2_crc		rw	na	0x0	esmi_s2_crc		
.11.	.346 esı	mi_s7_cnt5					Reg.	0xA0211118
		t Count Register acket count						
bits	-	name	s/w	h/w	default		des	cription
':0	s7_cnt		rw	na	0x0	esmi_s7_cnt		1 ·
						<u> </u>		
.11.	.347 esı	mi_s7_crc5					Reg.	0xA021111C

SEND7 CRC error Count Register total SEND7 CRC error count

_		name	s/w	h/w	default		des	cription
:0	s7_crc		rw	na	0x0	esmi_s7_crc		
.11.	348 esr	mi_rd_cnt5					Reg.	0xA0211120
REAL	) Packet	Count Register						
	o total pa	cket count						
bits 7:0	rd_cnt	name	s/w rw	h/w na	default 0x0	esmi_rd_cnt	des	cription
.0	ru_ont		1 44	Πα	OXO	com_ra_ont		
I.11.	349 esr	mi_rd_crc5					Reg.	0xA0211124
		ror Count Regist RC error count	er					
bits		name	s/w	h/w	default		des	cription
3:0	rd_crc		rw	na	0x0	esmi_rd_crc		
1.11.	350 esr	mi_da_cnt5					Reg.	0xA0211128
		Request Count request total co		er				
bits		name	s/w	h/w	default		des	cription
7:0	da_cnt		rw	na	0x0	esmi_da_cnt		
1.11.	351 esr	mi_ia_cnt5					Reg.	0xA021112C
InDire		ss Request Cou		ster				
	ot madio							
	Jot 7 tadio	name	s/w	h/w	default		des	cription
InDire bits	ia_cnt	name		h/w na	default 0x0	esmi_ia_cnt	des	cription
InDire bits		name	s/w			esmi_ia_cnt	des	cription
InDire bits 31:0	ia_cnt	name ni_tcmd_cnt	s/w rw			esmi_ia_cnt	des	0xA0211130
InDire bits 31:0	ia_cnt 352 esr	mi_tcmd_cnt	s/w rw	na	0x0	esmi_ia_cnt		
InDirection bits 31:0	ia_cnt  352 esr		s/w rw	na	0x0	esmi_ia_cnt		
InDire bits 31:0  1.11. TREFTREF bits	ia_cnt  352 esr  without without	mi_tcmd_cnt waveform Reque waveform total c name	s/w rw	na nt Reg	0x0 gister default		Reg.	
InDire bits 31:0 1.11. TREF	ia_cnt  352 esr	mi_tcmd_cnt waveform Reque waveform total c name	s/w rw 5 est Cou	na nt Reg	0x0 gister	esmi_ia_cnt	Reg.	0xA0211130
InDire bits 31:0 1.11. TREF TREF bits 7:0	ia_cnt  352 esr  without without tcmd_cn	mi_tcmd_cnt waveform Reque waveform total c name it	s/w rw 5 est Cou ount s/w rw	na nt Reg	0x0 gister default		Reg.	0xA0211130
InDire bits 31:0 1.11. TREF TREF bits 7:0	ia_cnt  352 esr  without without tcmd_cn	mi_tcmd_cnt waveform Reque waveform total c name	s/w rw 5 est Cou ount s/w rw	na nt Reg	0x0 gister default		Reg.	0xA0211130
InDire bits 31:0  I.11.  TREF bits 7:0	352 esr without tcmd_cn  353 esr	mi_tcmd_cnt waveform Reque waveform total c name it	s/w rw  5  est Coulount s/w rw  1t5  Count I	nt Reg	oxo gister default 0x0		Reg.	0xA0211130 cription
InDirection bits 31:0  1.11. TREF bits 7:0  TREF TREF bits 7:0	352 esr without tcmd_cn with way	mi_tcmd_cnt waveform Reque waveform total c name it mi_twcmd_cr veform Request veform total cour name	s/w rw  5  est Coulount s/w rw  1t5  Count I	nt Reg	oxo  gister  default  oxo  er  default	esmi_tcmd_cnt	des des	0xA0211130 cription
InDirection bits 31:0  1.11. TREFTREFT bits 7:0  1.11. TREFTREFTREFTREFTREFT	352 esr without tcmd_cn  353 esr	mi_tcmd_cnt waveform Reque waveform total c name it mi_twcmd_cr veform Request veform total cour name	s/w rw  5  est Count s/w rw  nt5  Count Int	nt Reg h/w na	oxo  gister  default oxo		des des	0xA0211130 cription 0xA0211134
InDirection bits 31:0  1.11. TREFTER bits 7:0  TREFTER bits 7:0	352 esr without tcmd_cn with way	mi_tcmd_cnt waveform Reque waveform total c name it mi_twcmd_cr veform Request veform total cour name	s/w rw  5  est Count s/w rw  1t5  Count Int s/w	nt Reg	oxo  gister  default  oxo  er  default	esmi_tcmd_cnt	des des	0xA0211130 cription 0xA0211134
InDirection bits 31:0  I.11. TREFTEF bits 7:0  TREFTEF bits 31:0	352 esr without tcmd_cn with way with way	mi_tcmd_cnt waveform Reque waveform total c name it mi_twcmd_cr veform Request veform total cour name	s/w rw  5  est Count s/w rw  1t5  Count Int s/w	nt Reg	oxo  gister  default  oxo  er  default	esmi_tcmd_cnt	des des	0xA0211130 cription 0xA0211134

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bits

31:0 dm\_cnt

name

1.11.355 esmi\_s0\_cnt6

esmi\_dm\_cnt

description

Reg.

0xA0211140

default

s/w h/w

na 0x0

	00 Packet Count Register 00 total packet count					
bits	name	s/w	h/w	default	de	scription
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt	
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt	

1.11.	1.11.356 esmi_s0_crc6 0xA0211144										
	00 CRC error Count Regis SEND0 CRC error count	ster									
bits	name	s/w	h/w	default		description	า				
3:0 s0_crc rw na 0x0 esmi_s0_crc											

1.11.	357 esmi_s1_cnt6	Reg.	0xA0211148								
	SEND1 Packet Count Register SEND1 total packet count										
bits	bits name s/w h/w default description										
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt						

1.11.	358 esmi_s1_crc6	Reg.	0xA021114C							
	01 CRC error Count Regis SEND1 CRC error count	ster								
bits	name	s/w	h/w	default		description	า			
3:0 s1_crc rw na 0x0 esmi_s1_crc										

1.11.3	359 esmi_s2_cnt6	Reg.	0xA0211150						
SEND2 Packet Count Register SEND2 total packet count									
bits	name	s/w	h/w	default		description	า		
7:0	s2_cnt	rw	na	0x0	esmi_s2_cnt				

1.11.	360 esmi_s2_crc6	Reg.	0xA0211154				
	02 CRC error Count Regis SEND2 CRC error count	ster					
bits	name	s/w	h/w	default		description	١
3:0	s2_crc						

1.11.	361 esmi_s7_cnt6	Reg.	0xA0211158							
	SEND7 Packet Count Register SEND7 total packet count									
bits	name	s/w	h/w	default		description	١			
7:0	s7_cnt	rw	na	0x0	esmi_s7_cnt					

1.11.	362 esmi_s7_crc6	Reg.	0xA021115C							
SEND7 CRC error Count Register total SEND7 CRC error count										
bits	name	s/w	h/w	default		description	n			
3:0	s7_crc	rw	na	0x0	esmi_s7_crc					

1.11	.363 esmi_rd_cnt6					Reg.	0xA0211160
	D Packet Count Register D total packet count						
bits	name	s/w	h/w	default		des	cription
7:0	rd_cnt	rw	na	0x0	esmi_rd_cnt		
1.11	.364 esmi_rd_crc6					Reg.	0xA0211164
	D CRC error Count Regis	ter					
bits	name	s/w	h/w	default		des	cription
bits		s/w rw	h/w na	default 0x0	esmi_rd_crc	des	cription
bits	name				esmi_rd_crc	des	cription
bits 3:0	name				esmi_rd_crc	des	cription  0xA0211168
bits 3:0 <b>1.11</b>	name rd_crc	rw t Registe	na		esmi_rd_crc		
bits 3:0 1.11 Direct Direct bits	name rd_crc  .365 esmi_da_cnt6  ct Address Request Count ct Address request total co	rw t Registe	na			Reg.	
bits 3:0 1.11 Direction	name rd_crc  .365 esmi_da_cnt6  ct Address Request Count ct Address request total co	rw t Registe	na	0x0	esmi_rd_crc	Reg.	0xA0211168
bits 3:0 1.11 Direct Direct bits	name rd_crc  .365 esmi_da_cnt6 ct Address Request Count ct Address request total co	rw t Registe	na er h/w	0x0		Reg.	0xA0211168

1.11.	Joo esiiii_ia_ciito						0,0 10211100				
InDirect Address Request Count Register InDirect Address request total count											
bits	name	s/w	h/w	default		description	1				
31:0	ia_cnt	rw	na	0x0	esmi_ia_cnt						

1.11.	1.11.367 esmi_tcmd_cnt6 0xA0211170										
	without waveform Reque without waveform total co		nt Reg	ister							
bits	name	s/w	h/w	default		description	٦				
7:0											

1.11.	368 esmi_twcmd_cr	Reg.	0xA0211174				
	with waveform Request ( with waveform total coun		Registe	er			
bits	name	s/w	h/w	default		description	ı
31:0	twcmd_cnt	rw	na	0x0	esmi_twcmd_cnt		

1.11.3	1.11.369 esmi_dm_cnt6 0xA0211178											
	O total write to read Latents the total time for DOMO	-	_		t of first write to en	d of first read						
bits	name	s/w	h/w	default		description	n					
31:0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1											

1.11.370 esmi_s0_cnt7	Reg.	0xA0211180
SEND0 Packet Count Register SEND0 total packet count		

bits name	s/w	h/w	default		des	scription
7:0 s0_cnt	rw	na	0x0	esmi_s0_cnt		
I.11.371 esmi_s0_crc7					Reg.	0xA0211184
	niotor					
SENDO CRC error Count Reg total SENDO CRC error count						
bits name	s/w	h/w	default		des	scription
3:0 s0_crc	rw	na	0x0	esmi_s0_crc		· · · · ·
					<b>P</b> 345%	0.40044400
1.11.372 esmi_s1_cnt7					Reg.	0xA0211188
SEND1 Packet Count Registe SEND1 total packet count	er					
bits name	s/w	h/w	default		des	scription
7:0 s0_cnt	rw	na	0x0	esmi_s0_cnt		
1 44 272					Rec	0v40044490
I.11.373 esmi_s1_crc7					Reg.	0xA021118C
SEND1 CRC error Count Reg total SEND1 CRC error count						
bits name	s/w	h/w	default		des	scription
3:0 s1_crc	rw	na	0x0	esmi_s1_crc		
I.11.374 esmi_s2_cnt7 SEND2 Packet Count Registe SEND2 total packet count	er				Reg.	0xA0211190
bits name	s/w	h/w	default		des	scription
7:0 s2_cnt	rw	na	0x0	esmi_s2_cnt		
1 44 275 com: c0 cro7					Reg	0xA0211194
1.11.375 esmi_s2_crc7					Reg.	UXAU211194
SEND2 CRC error Count Reg total SEND2 CRC error count						
bits name	s/w	h/w	default		des	scription
3:0 s2_crc	rw	na	0x0	esmi_s2_crc		
1.11.376 esmi_s7_cnt7					Reg.	0xA0211198
SEND7 Packet Count Registe	er					
SEND7 total packet count						
bits name 7:0 s7_cnt	s/w rw	h/w na	default 0x0	esmi_s7_cnt	des	scription
.o or_on	I VV	IId	UAU	C31111_31_UIII		
1.11.377 esmi_s7_crc7					Reg.	0xA021119C
SEND7 CRC error Count Reg						
	[					
total SEND7 CRC error count		h/w	default		des	scription
total SEND7 CRC error count bits name 3:0 s7_crc	s/w rw	h/w na	default 0x0	esmi_s7_crc	des	scription

1.11.378 esmi\_rd\_cnt7

Reg.

0xA02111A0

	D Packet Count Register D total packet count				
bits	name	s/w	h/w	default	description
7:0	rd cnt	rw	na	0x0	esmi rd cnt

1.11.3	379 esmi_rd_crc7	Reg.	0xA02111A4						
	READ CRC error Count Register total READ CRC error count								
bits name s/w h/w default description									
3:0	rd_crc	rw	esmi_rd_crc						

1.11.3	380 esmi_da_cnt7	Reg.	0xA02111A8						
Direct Address Request Count Register Direct Address request total count									
bits	name	s/w	h/w	default		description	า		
7:0	da_cnt	rw	na	0x0	esmi_da_cnt				

1.11.	381 esmi_ia_cnt7	Reg.	0xA02111AC							
	InDirect Address Request Count Register InDirect Address request total count									
bits	name	s/w h/w default description								
31:0	31:0 ia_cnt rw na 0x0 esmi_ia_cnt									

1.11.	382 esmi_tcmd_cnt	Reg.	0xA02111B0						
TREF without waveform Request Count Register TREF without waveform total count									
bits	name	s/w	h/w	default		description	า		
7:0	tcmd_cnt rw na 0x0 esmi_tcmd_cnt								

1.11.3	383 esmi_twcmd_cr	Reg.	0xA02111B4							
	TREF with waveform Request Count Register TREF with waveform total count									
bits	bits name s/w h/w default description									
31:0	twcmd_cnt									

1.11.	384 esmi_dm_cnt7		Reg.	0xA02111B8							
	DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write to end of first read										
bits	bits name s/w h/w default description										
31:0	dm_cnt	rw	na	0x0	esmi_dm_cnt						

1.11.	385 esmi_s0_cnt8	Reg.	0xA02111C0						
SEND0 Packet Count Register SEND0 total packet count									
bits	name	s/w	h/w	default		description	า		
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt				

	.386 esmi_s0_crc8	5				Reg.	0xA02111C4
	D0 CRC error Count Re SEND0 CRC error cour						
bits		s/w	h/w	default		des	cription
:0	s0_crc	rw	na	0x0	esmi_s0_crc		
.11	.387 esmi_s1_cnt8	3				Reg.	0xA02111C8
	D1 Packet Count Regis D1 total packet count	ter					
bits		s/w	h/w	default		des	cription
':0	s0_cnt	rw	na	0x0	esmi_s0_cnt		
.11	.388 esmi_s1_crc8	3				Reg.	0xA02111CC
	D1 CRC error Count Re SEND1 CRC error cour						
bits	name	s/w	h/w	default		des	cription
3:0	s1_crc	rw	na	0x0	esmi_s1_crc		
	.389 esmi_s2_cnt8					Reg.	0xA02111D0
	D2 Packet Count Regis D2 total packet count	ter					
bits ':0	name s2_cnt	s/w	h/w	default 0x0	aami a2 ant	des	cription
.0	52_UII	rw	na	OXO	esmi_s2_cnt		
1.11	.390 esmi_s2_crc8	3				Reg.	0xA02111D4
	D2 CRC error Count Re SEND2 CRC error cour						
bits	name	s/w	h/w	default		des	cription
3:0	s2_crc	rw	na	0x0	esmi_s2_crc		
1.11	.391 esmi_s7_cnt8	3				Reg.	0xA02111D8
	D7 Packet Count Regis D7 total packet count	ter					
bits		s/w	h/w	default		des	cription
<b>'</b> :0	s7_cnt	rw	na	0x0	esmi_s7_cnt		
1.11	.392 esmi_s7_crc8	3				Reg.	0xA02111DC
	D7 CRC error Count Re SEND7 CRC error cour						
		s/w	h/w	default		des	cription
	name	3/ W					
total	name s7_crc	rw	na	0x0	esmi_s7_crc		

bits		name	s/w	h/w	default		des	cription
7:0	rd_cnt		rw	na	0x0	esmi_rd_cnt		
1.11.	394 esr	mi_rd_crc8					Reg.	0xA02111E4
		ror Count Regist RC error count	er					
bits		name	s/w	h/w	default		des	cription
3:0	rd_crc		rw	na	0x0	esmi_rd_crc		
I.11.	395 esr	mi_da_cnt8					Reg.	0xA02111E8
		s Request Count s request total co		er				
bits		name	s/w	h/w	default		des	cription
7:0	da_cnt		rw	na	0x0	esmi_da_cnt		
1.11.	396 esr	mi_ia_cnt8					Reg.	0xA02111EC
		ess Request Cour ess request total o		ster				
bits		name	s/w	h/w	default		des	cription
31:0	ia_cnt		rw	na	0x0	esmi_ia_cnt		
TREF	= without	mi_tcmd_cnt waveform Reque waveform total c	est Cou	nt Reg	gister		Reg.	0xA02111F0
bits		name	s/w	h/w	default		des	cription
7:0	tcmd_cr	nt	rw	na	0x0	esmi_tcmd_cnt		•
1.11.	398 esr	mi_twcmd_cr	nt8				Reg.	0xA02111F4
		veform Request ( veform total cour		Registe	er			
bits		name	s/w	h/w	default		des	cription
31:0	twcmd_c	cnt	rw	na	0x0	esmi_twcmd_cnt		
1.11.	399 esr	mi_dm_cnt8					Reg.	0xA02111F8
		rite to read Laten al time for DOMC				rt of first write to er	nd of first rea	ad
bits		name	s/w	h/w	default		des	cription
31:0	dm_cnt		rw	na	0x0	esmi_dm_cnt		
1.11.	400 esr	mi_s0_cnt9					Reg.	0xA0211200
		t Count Register acket count						
bits		name	s/w	h/w	default		des	cription
7:0	s0_cnt		rw	na	0x0	esmi_s0_cnt		

1.11.401 esmi\_s0\_crc9

Reg.

0xA0211204

SEND0 CRC error Count Register total SEND0 CRC error count											
bits	bits name s/w h/w default description										
3:0	s:0 s0_crc rw na 0x0 esmi_s0_crc										

1.11.4	402 esmi_s1_cnt9	Reg.	0xA0211208							
SEND1 Packet Count Register SEND1 total packet count										
bits name s/w h/w default description										
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt					

1.11.	403 esmi_s1_crc9	Reg.	0xA021120C									
	SEND1 CRC error Count Register total SEND1 CRC error count											
bits	bits name s/w h/w default description											
3:0	s1_crc	rw	na	0x0	esmi_s1_crc							

1.11.4	404 esmi_s2_cnt9	Reg.	0xA0211210								
SEND2 Packet Count Register SEND2 total packet count											
bits name s/w h/w default description											
7:0	s2_cnt	rw	na	0x0	esmi_s2_cnt						

1.11.	405 esmi_s2_crc9	Reg.	0xA0211214									
SEND2 CRC error Count Register total SEND2 CRC error count												
bits	bits name s/w h/w default description											
3:0	s2_crc	rw	na	0x0	esmi_s2_crc							

1.11.4	406 esmi_s7_cnt9	Reg.	0xA0211218								
	SEND7 Packet Count Register SEND7 total packet count										
bits	bits name s/w h/w default description										
7:0	s7_cnt	rw	na	0x0	esmi_s7_cnt						

1.11.4	407 esmi_s7_crc9	Reg.	0xA021121C									
	SEND7 CRC error Count Register total SEND7 CRC error count											
bits	bits name s/w h/w default description											
3:0	s7_crc	rw	na	0x0	esmi_s7_crc							

1.11.	408 esmi_rd_cnt9	Reg.	0xA0211220								
	READ Packet Count Register READ total packet count										
bits	name	s/w	h/w	default		description	n				
7:0	rd_cnt	rw	na	0x0	esmi_rd_cnt						

	09 esmi_rd_crc9	Reg.	0xA0211224									
READ CRC error Count Register total READ CRC error count												
bits	name	s/w	h/w	default		description	ı					
3:0 rc	3:0 rd_crc rw na 0x0 esmi_rd_crc											

1.11.	410 esmi_da_cnt9	Reg.	0xA0211228									
Direct Address Request Count Register Direct Address request total count												
bits	bits name s/w h/w default description											
7:0	da_cnt	rw	na	0x0	esmi_da_cnt							

1.11.4	411 esmi_ia_cnt9	0xA021122C										
	InDirect Address Request Count Register InDirect Address request total count											
bits	bits name s/w h/w default description											
31:0	ia_cnt	rw	esmi_ia_cnt									

1.11.	412 esmi_tcmd_cnt	Reg.	0xA0211230									
TREF without waveform Request Count Register TREF without waveform total count												
bits	bits name s/w h/w default description											
7:0	tcmd_cnt	esmi_tcmd_cnt										

1.11.	413 esmi_twcmd_cr	Reg.	0xA0211234								
	TREF with waveform Request Count Register TREF with waveform total count										
bits	bits name s/w h/w default description										
31:0	twcmd_cnt										

1.11.	414 esmi_dm_cnt9		Reg.	0xA0211238						
DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write to end of first read										
bits	bits name s/w h/w default description									
31:0	dm_cnt	rw	na	0x0	esmi_dm_cnt					

1.11.	415 esmi_s0_cnt10	Reg.	0xA0211240								
	SEND0 Packet Count Register SEND0 total packet count										
bits	bits name s/w h/w default description										
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt						

1.11.416 esmi_s0_crc10	Reg.	0xA0211244
SEND0 CRC error Count Register total SEND0 CRC error count		

bits		name	s/w	h/w	default		des	cription
3:0	s0_crc		rw	na	0x0	esmi_s0_crc		
11	417 oct	mi s1 ont10					Reg.	0xA0211248
		mi_s1_cnt10						0XA02112 <del>4</del> 0
		t Count Register acket count						
bits	-01	name	s/w	h/w	default		des	cription
7:0	s0_cnt		rw	na	0x0	esmi_s0_cnt		
.11.	.418 esr	mi_s1_crc10					Reg.	0xA021124C
SENI	D1 CRC e	error Count Regis	ster					
bits	SENDIC	name	s/w	h/w	default		aah	cription
3:0	s1_crc	папте	rw	na	0x0	esmi_s1_crc	ues	Olipaoli
	_							
.11.	.419 esr	mi_s2_cnt10					Reg.	0xA0211250
		t Count Register acket count						
bits		name	s/w	h/w	default		des	cription
<b>7</b> :0	s2_cnt		rw	na	0x0	esmi_s2_cnt		•
SENI	D2 CRC e	mi_s2_crc10 error Count Regis RC error count	ster				Reg.	
bits	_	name	s/w	h/w	default		des	cription
3:0	s2_crc		rw	na	0x0	esmi_s2_crc		
1 11	121 oct	mi s7 cnt10					Reg.	0xA0211258
		t Count Register					*******	070 102 1 1200
		acket count						
bits		name	s/w	h/w	default		des	cription
<b>7</b> :0	s7_cnt		rw	na	0x0	esmi_s7_cnt		
l.11.	.422 esr	mi_s7_crc10					Reg.	0xA021125C
SENI	D7 CRC e	error Count Regis	ster					
bits	SEND/ C	RC error count	s/w	h/w	default		des	cription
3:0	s7_crc	папто	rw	na	0x0	esmi_s7_crc	ues	onpuon
l.11.	.423 esr	mi_rd_cnt10					Reg.	0xA0211260
		Count Register cket count						
bits		name	s/w	h/w	default		des	cription
7:0	rd_cnt		rw	na	0x0	esmi_rd_cnt		

1.11.424 esmi\_rd\_crc10

Reg.

0xA0211264

READ CRC error Count Register total READ CRC error count									
bits	name	s/w	h/w	default	description				
3:0	rd_crc	rw	na	0x0	esmi_rd_crc				

1.11.4	425 esmi_da_cnt10	Reg.	0xA0211268								
	Direct Address Request Count Register Direct Address request total count										
bits	bits name s/w h/w default description										
7:0	da_cnt	rw	esmi_da_cnt								

1.11.	426 esmi_ia_cnt10	Reg.	0xA021126C								
	InDirect Address Request Count Register InDirect Address request total count										
bits	bits name s/w h/w default description										
31:0	ia_cnt	rw	na	0x0	esmi_ia_cnt						

1.11.	427 esmi_tcmd_cnt1	Reg.	0xA0211270								
	TREF without waveform Request Count Register TREF without waveform total count										
bits	bits name s/w h/w default description										
7:0	tcmd_cnt	esmi_tcmd_cnt									

1.11.	428 esmi_twcmd_cr	Reg.	0xA0211274								
	TREF with waveform Request Count Register TREF with waveform total count										
bits	name	s/w	h/w	default		description	ı				
31:0	twcmd_cnt										

1.11.4	429 esmi_dm_cnt10	Reg.	0xA0211278									
	DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write to end of first read											
bits	bits name s/w h/w default description											
31:0	dm_cnt	esmi_dm_cnt										

1.11.	430 esmi_s0_cnt11	Reg.	0xA0211280							
	SEND0 Packet Count Register SEND0 total packet count									
bits	bits name s/w h/w default description									
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt					

1.11.	431 esmi_s0_crc11	Reg.	0xA0211284						
	SEND0 CRC error Count Register total SEND0 CRC error count								
bits	name	s/w	h/w	default		description	n		
3:0	s0_crc	rw	na	0x0	esmi_s0_crc				

1.11.432 esmi_s1_cnt11					Reg.	0xA0211288
SEND1 Packet Count Register SEND1 total packet count						
bits name	s/w	h/w	default		des	cription
':0 s0_cnt	rw	na	0x0	esmi_s0_cnt		
.11.433 esmi_s1_crc11					Reg.	0xA021128C
SEND1 CRC error Count Registotal SEND1 CRC error count	ster					
bits name	s/w	h/w	default		des	cription
3:0 s1_crc	rw	na	0x0	esmi_s1_crc		
.11.434 esmi_s2_cnt11					Reg.	0xA0211290
SEND2 Packet Count Register SEND2 total packet count						
bits name	s/w	h/w	default		des	cription
7:0 s2_cnt	rw	na	0x0	esmi_s2_cnt		
.11.435 esmi_s2_crc11					Reg.	0xA0211294
SEND2 CRC error Count Regis total SEND2 CRC error count	ster					
bits name	s/w	h/w	default		des	cription
3:0 s2_crc	rw	na	0x0	esmi_s2_crc		
1.11.436 esmi_s7_cnt11					Reg.	0xA0211298
SEND7 Packet Count Register SEND7 total packet count						
bits name	s/w	h/w	default		des	scription
7:0 s7_cnt	rw	na	0x0	esmi_s7_cnt		
.11.437 esmi_s7_crc11					Reg.	0xA021129C
SEND7 CRC error Count Registotal SEND7 CRC error count	ster					
bits name	s/w	h/w	default		des	scription
3:0 s7_crc	rw	na	0x0	esmi_s7_crc		
.11.438 esmi_rd_cnt11					Reg.	0xA02112A0
READ Packet Count Register READ total packet count						
bits name	s/w	h/w	default		des	scription
7:0 rd_cnt	rw	na	0x0	esmi_rd_cnt	5.30	
I.11.439 esmi_rd_crc11					Reg.	0xA02112A4

READ CRC error Count Register total READ CRC error count

name	s/w	h/w	default	description
_crc	rw	na	0x0	esmi_rd_crc
-				

1.11.4	.11.440 esmi_da_cnt11 0xA02112A8									
	Direct Address Request Count Register Direct Address request total count									
bits	bits name s/w h/w default description									
7:0	da_cnt	rw	na	0x0	esmi_da_cnt					

1.11.	1.11.441 esmi_ia_cnt11 0xA02112AC										
	InDirect Address Request Count Register InDirect Address request total count										
bits	name	s/w	h/w	default		description	n				
31:0	ia_cnt	rw	na	0x0	esmi_ia_cnt						

1.11.	.11.442 esmi_tcmd_cnt11 0xA02112B0									
	TREF without waveform Request Count Register TREF without waveform total count									
bits	name	s/w	h/w	default		description	n			
7:0	tcmd_cnt	rw	na	0x0	esmi_tcmd_cnt					

1.11.	1.11.443 esmi_twcmd_cnt11 0xA02112B4										
	with waveform Request with waveform total cour		Registe	er							
bits	name	s/w	h/w	default		description	า				
31:0	twcmd_cnt	rw	na	0x0	esmi_twcmd_cnt						

1.11.	.11.444 esmi_dm_cnt11 0xA02112B8									
	DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write to end of first read									
bits	bits name s/w h/w default description									
31:0	dm_cnt	rw	na	0x0	esmi_dm_cnt					

1.11.	445 esmi_s0_cnt12	Reg.	0xA02112C0						
	SEND0 Packet Count Register SEND0 total packet count								
bits	name	s/w	h/w	default		description	١		
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt				

1.11.	446 esmi_s0_crc12		Reg.	0xA02112C4					
	SEND0 CRC error Count Register total SEND0 CRC error count								
bits	bits name s/w h/w default description								
3:0	s0_crc	rw	na	0x0	esmi_s0_crc				

1.11.447 esmi_s1_cnt12	Reg.	0xA02112C8

	SEND1 Packet Count Register SEND1 total packet count								
bits	name	s/w	h/w	default	description				
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt				

1.11.448 esmi_s1_crc12 0xA02112CC											
SEND1 CRC error Count Register total SEND1 CRC error count											
bits	bits name s/w h/w default description										
3:0	s1_crc	rw	na	0x0	esmi_s1_crc						

1.11.4	449 esmi_s2_cnt12	Reg.	0xA02112D0							
SEND2 Packet Count Register SEND2 total packet count										
bits	name	s/w	h/w	default		description	า			
7:0	s2_cnt	rw	na	0x0	esmi_s2_cnt					

1.11.	450 esmi_s2_crc12	Reg.	0xA02112D4								
SEND2 CRC error Count Register total SEND2 CRC error count											
bits	bits name s/w h/w default description										
3:0	s2_crc	rw	na	0x0	esmi_s2_crc						

1.11.451 esmi_s7_cnt12 0xA02112D8									
SEND7 Packet Count Register SEND7 total packet count									
bits name s/w h/w default description									
7:0	s7_cnt	rw	na	0x0	esmi_s7_cnt				

1.11.4	452 esmi_s7_crc12	Reg.	0xA02112DC								
SEND7 CRC error Count Register total SEND7 CRC error count											
bits	bits name s/w h/w default description										
3:0 s7_crc rw na 0x0 esmi_s7_crc											

1.11.	453 esmi_rd_cnt12					Reg.	0xA02112E0		
READ Packet Count Register READ total packet count									
bits	name	s/w	h/w	default		description	า		
7:0	rd_cnt	rw	na	0x0	esmi_rd_cnt				

1.11.454 esmi_rd_crc12 0xA02112E4											
READ CRC error Count Register total READ CRC error count											
bits name s/w h/w default description											
Dito											

1.11.455 esmi_da_cnt12 0xA02112E8											
Direct Address Request Count Register Direct Address request total count											
bits	name	s/w	h/w	default		descrip	tion				
7:0 da_	cnt	rw	na	0x0	esmi_da_cnt						

1.11.	456 esmi_ia_cnt12	Reg.	0xA02112EC							
InDirect Address Request Count Register InDirect Address request total count										
bits	name	s/w	h/w	default		description	n			
31:0	ia_cnt	rw	na	0x0	esmi_ia_cnt					

1.11.	1.11.457 esmi_tcmd_cnt12 0xA02112F0										
TREF without waveform Request Count Register TREF without waveform total count											
bits	bits name s/w h/w default description										
7:0 tcmd_cnt rw na 0x0 esmi_tcmd_cnt											

1.11.458 esmi_twcmd_cnt12 0xA02112F4											
TREF with waveform Request Count Register TREF with waveform total count											
bits	bits name s/w h/w default description										
31:0 twcmd_cnt rw na 0x0 esmi_twcmd_cnt											

1.11.4	459 esmi_dm_cnt12	Reg.	0xA02112F8									
DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write to end of first read												
bits	bits name s/w h/w default description											
31:0	dm_cnt											

1.11.	460 esmi_s0_cnt13					Reg.	0xA0211300
	00 Packet Count Register 00 total packet count						
bits	name	s/w	h/w	default		description	1
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt		

1.11.	461 esmi_s0_crc13	Reg.	0xA0211304				
	D0 CRC error Count Regis SEND0 CRC error count	ster					
bits	name	s/w	h/w	default		description	n
3:0	s0_crc	rw	na	0x0	esmi_s0_crc		

1.11.462 esmi_s1_cnt13	Reg.	0xA0211308
SEND1 Packet Count Register SEND1 total packet count		

bits		name	s/w	h/w	default		des	cription
<b>'</b> :0	s0_cnt		rw	na	0x0	esmi_s0_cnt		
.11.	463 esr	mi_s1_crc13					Reg.	0xA021130C
		error Count Regis RC error count	ter					
bits		name	s/w	h/w	default		des	cription
3:0	s1_crc		rw	na	0x0	esmi_s1_crc		
1 11	464 est	mi_s2_cnt13					Reg	0xA0211310
SEN	D2 Packe	t Count Register						
	D2 total p	acket count	,	. ,				
bits 7:0	s2_cnt	name	s/w rw	h/w na	default 0x0	esmi_s2_cnt	des	cription
.0	o∠_UIII		ı vv	IId	UXU	esiii_82_Ciil		
1.11.	465 esr	mi_s2_crc13					Reg.	0xA0211314
		error Count Regis	ter					
bits		name	s/w	h/w	default		des	cription
3:0	s2_crc		rw	na	0x0	esmi_s2_crc		
111	166 061	mi_s7_cnt13					Reg.	0xA0211318
		t Count Register						03/10211010
SEN		acket count						
bits 7:0	s7_cnt	name	s/w rw	h/w na	default 0x0	esmi_s7_cnt	des	cription
7.0	S7_CIII		I VV	IIa	OXO	esiii_s/_ciit		
I <b>.11</b> .	467 esr	mi_s7_crc13					Reg.	0xA021131C
		error Count Regis	ter					
bits		name	s/w	h/w	default		des	cription
3:0	s7_crc	·	rw	na	0x0	esmi_s7_crc		,
I.11.	468 esr	mi_rd_cnt13					Reg.	0xA0211320
		Count Register cket count						
bits		name	s/w	h/w	default		des	cription
7:0	rd_cnt		rw	na	0x0	esmi_rd_cnt		
1,11.	469 esi	mi_rd_crc13					Reg.	0xA0211324
		ror Count Registe	ər					
total	READ CF		- /					
		name	s/w rw	h/w na	default 0x0	esmi_rd_crc	des	cription

1.11.470 esmi\_da\_cnt13

Reg.

0xA0211328

	t Address Request Count t Address request total cou	•	ər		
bits	name	s/w	h/w	default	description
7:0	da_cnt	rw	na	0x0	esmi_da_cnt

1.11.4	471 esmi_ia_cnt13	Reg.	0xA021132C								
	ect Address Request Cour ect Address request total o	•	ster								
bits	bits name s/w h/w default description										
31:0	ia_cnt	rw	na	0x0	esmi_ia_cnt						

1.11.4	472 esmi_tcmd_cnt	Reg.	0xA0211330								
	TREF without waveform Request Count Register TREF without waveform total count										
bits	bits name s/w h/w default description										
7:0	tcmd_cnt	rw	na	0x0	esmi_tcmd_cnt						

1.11.	473 esmi_twcmd_cr	Reg.	0xA0211334								
	TREF with waveform Request Count Register TREF with waveform total count										
bits	bits name s/w h/w default description										
31:0	twcmd_cnt	rw	na	0x0	esmi_twcmd_cnt						

1.11.	474 esmi_dm_cnt13	Reg.	0xA0211338								
	O total write to read Laten ts the total time for DOMC	•	-		t of first write to en	d of first read					
bits	bits name s/w h/w default description										
31:0	dm_cnt	rw	na	0x0	esmi_dm_cnt						

1.11.4	475 esmi_s0_cnt14					Reg.	0xA0211340
	00 Packet Count Register 00 total packet count						
bits	name	s/w	h/w	default		description	n
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt		

1.11.	476 esmi_s0_crc14	Reg.	0xA0211344							
	SEND0 CRC error Count Register total SEND0 CRC error count									
bits	name	s/w	h/w	default		description	n			
3:0	s0_crc	rw	na	0x0	esmi_s0_crc					

1.11.	477 esmi_s1_cnt14	Reg.	0xA0211348				
	01 Packet Count Registe 01 total packet count	er					
bits	name	s/w	h/w	default		desc	ription
7:0	s0 cnt	rw	na	0x0	esmi s0 cnt		

.11.	4/8 esn	ni_s1_crc14					Reg.	0xA021134C
		rror Count Regis RC error count	ster					
bits		name	s/w	h/w	default		des	cription
0	s1_crc		rw	na	0x0	esmi_s1_crc		
.11.	479 esn	ni_s2_cnt14					Reg.	0xA0211350
		Count Register						
bits		name	s/w	h/w	default		des	cription
:0	s2_cnt		rw	na	0x0	esmi_s2_cnt		
.11.	480 esn	ni_s2_crc14					Reg.	0xA0211354
		rror Count Regis RC error count	ster					
bits		name	s/w	h/w	default		des	cription
3:0	s2_crc		rw	na	0x0	esmi_s2_crc		
.11.	481 esn	ni_s7_cnt14					Reg.	0xA0211358
		Count Register						
bits		name	s/w	h/w	default		des	cription
':0	s7_cnt		rw	na	0x0	esmi_s7_cnt		
l.11.	482 esn	ni_s7_crc14					Reg.	0xA021135C
		rror Count Regis RC error count	ster					
bits		name	s/w	h/w	default		des	cription
:0	s7_crc		rw	na	0x0	esmi_s7_crc		
.11.	483 esn	ni_rd_cnt14					Reg.	0xA0211360
	D Packet ( D total pac	Count Register cket count						
bits		name	s/w	h/w	default		des	cription
':0	rd_cnt		rw	na	0x0	esmi_rd_cnt		
.11.	484 esn	ni_rd_crc14					Reg.	0xA0211364
		or Count Regist C error count	er					
		name	s/w	h/w	default		des	cription
bits	rd_crc		rw	na	0x0	esmi_rd_crc		·
bits 3:0								
:0	485 esn	ni_da_cnt14					Reg.	0xA0211368

bits		name	s/w	h/w	default		des	cription
:0	da_cnt		rw	na	0x0	esmi_da_cnt		
.11.	.486 esı	mi_ia_cnt14					Reg.	0xA021136C
		ess Request Cou ess request total		ster				
bits		name	s/w	h/w	default		des	cription
1:0	ia_cnt		rw	na	0x0	esmi_ia_cnt		·
		mi_tcmd_cnt		nt Des			Reg.	0xA0211370
		waveform Requ waveform total of		nt Reç	jister			
bits		name	s/w	h/w	default		des	cription
	tcmd_cr		s/w rw	h/w na	default 0x0	esmi_tcmd_cnt	des	cription
':0   <b>.11.</b> TRE	tcmd_cr		rw nt14 Count F	na	0x0	esmi_tcmd_cnt	des	OxA0211374
7:0 <b>I.11.</b> TREI	tcmd_cr	ni_twcmd_c veform Request	rw nt14 Count F	na	0x0	esmi_tcmd_cnt	Reg.	
7:0  I.11.  TREI  TREI  bits	tcmd_cr	mi_twcmd_c veform Request veform total cou name	rw nt14 Count F	na Registe	0x0 er default	esmi_tcmd_cnt	Reg.	0xA0211374
7:0 1.11. TREI TREI	tcmd_cr	mi_twcmd_c veform Request veform total cou name	rw nt14 Count F	na Registo	0x0 er default		Reg.	0xA0211374
7:0  1.11.  TREI  TREI  bits 31:0	tcmd_cr .488 esi F with wa F with wa twcmd_c	mi_twcmd_c veform Request veform total cou name	rw nt14 Count F nt s/w rw	na Registo	0x0 er default		Reg.	0xA0211374
TREI TREI bits 31:0	tcmd_cr .488 esi F with wa F with wa twcmd_c	mi_twcmd_c veform Request veform total cou name cnt mi_dm_cnt14 rite to read Late	rw nt14 Count F nt s/w rw	na Registo h/w na	er default 0x0		des	0xA0211374  cription  0xA0211378
7:0  TREI TREI bits 31:0	tcmd_cr .488 esi F with wa F with wa twcmd_c	mi_twcmd_c veform Request veform total cou name cnt mi_dm_cnt14 rite to read Late	rw nt14 Count F nt s/w rw	na Registo h/w na	er default 0x0	esmi_twcmd_cn	des	0xA0211374  cription  0xA0211378
TREI TREI bits 31:0	tcmd_cr .488 esi F with wa F with wa twcmd_c	mi_twcmd_c veform Request veform total cou name cnt mi_dm_cnt14 rite to read Late al time for DOM	rw  nt14  Count F nt  s/w rw  4  ncy Cou	na Registe h/w na	er  default 0x0  gister ction, from sta	esmi_twcmd_cn	des	0xA0211374  cription  0xA0211378
TREITREID bits bits 1:0	tcmd_cr  488 esi  F with wa  twcmd_c  489 esi  O total w  nts the tot	mi_twcmd_c veform Request veform total cou name cnt mi_dm_cnt14 rite to read Late al time for DOM	rw  nt14  Count Fint  s/w rw  4  ncy Cou	na Registe h/w na ant Regransac	er default 0x0 gister ction, from sta	esmi_twcmd_cn	des	0xA0211374  cription  0xA0211378

.11.491 esmi_s0_crc15  SEND0 CRC error Count Register  0xA0211384	bits	name s/w h/w default description								
.11.491 esmi_s0_crc15  SEND0 CRC error Count Register total SEND0 CRC error count	':0	s0_cnt	rw	na	0x0	esmi_s0_cnt				
SEND0 CRC error Count Register										
· ·	1.11.491 esmi s0 crc15 0xA0211384									
	1.11	491 esmi_s0_crc15					Reg.	0xA0211384		

1.11.4	92 esmi_s1_cnt15				Reg.	0xA0211388
	1 Packet Count Register 1 total packet count					
bits	name	s/w	h/w	default	descript	ion

esmi\_s0\_crc

7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt		
							_
1.11.4	493 esmi_s1_crc15					Reg.	0xA021138C
20							

3:0 s0\_crc

rw

na 0x0

	SEND1 CRC error Count Register total SEND1 CRC error count										
bits	name	s/w	h/w	default	description						
3:0	3:0 s1_crc rw na 0x0 esmi_s1_crc										

1.11.4	494 esmi_s2_cnt15		Reg.	0xA0211390			
	02 Packet Count Register 02 total packet count						
bits	name	s/w	h/w	default		description	n
7:0	s2_cnt	rw	na	0x0	esmi_s2_cnt		

1.11.	495 esmi_s2_crc15				Reg.	0xA0211394
	D2 CRC error Count Regis SEND2 CRC error count	ster				
bits	name	s/w	h/w	default	description	١
3:0						

1.11.	.11.496 esmi_s7_cnt15 0xA0211398										
	07 Packet Count Register 07 total packet count										
bits	name	s/w	h/w	default		description	١				
7:0	s7_cnt	rw	na	0x0	esmi_s7_cnt						

1.11.4	497 esmi_s7_crc15	Reg.	0xA021139C				
	D7 CRC error Count Regis SEND7 CRC error count	ster					
bits	name	s/w	h/w	default		description	า
3:0	s7_crc	rw	esmi_s7_crc				

1.11.4	198 esmi_rd_cnt15					Reg.	0xA02113A0
	Packet Count Register total packet count						
bits	name	s/w	h/w	default		description	١
7:0	rd_cnt	rw	na	0x0	esmi_rd_cnt		

1.11.	499 esmi_rd_crc1	5				Reg.	0xA02113A4					
	O CRC error Count Reg READ CRC error count											
bits	name	s/w	h/w	default		description	n					
3:0	·											

1.11.	500 esmi_da_cnt	15			Reg.	0xA02113A8
	t Address Request Co t Address request tota		er			
			1 /	-l - <b>f</b> l4	_1	
bits	name	s/w	h/w	default	aesc	ription

1.11.	<b>501 esmi</b>	i_ia_cnt15					Reg.	0xA02113AC
		Request Cour request total o		ster				
bits	r	name	s/w	h/w	default		des	cription
31:0	ia_cnt		rw	na	0x0	esmi_ia_cnt		
1.11.	502 esmi	i_tcmd_cnt1	15				Reg.	0xA02113B0
		aveform Reque aveform total co		nt Reg	jister			
bits	r	name	s/w	h/w	default		des	cription
7:0	tcmd_cnt		rw	na	0x0	esmi_tcmd_cnt		
1.11.	<b>503 es</b> mi	i_twcmd_cr	t15				Reg.	0xA02113B4
		form Request ( form total coun		Registe	er			
bits	r	name	s/w	h/w	default		des	cription
31:0	twcmd_cn	t	rw	na	0x0	esmi_twcmd_cn		
		e to read Laten time for DOMC				rt of first write to e	nd of first rea	ad
bits 31:0		name	s/w rw	h/w na	default			cription
31:0	dm_cnt		s/w rw	h/w na	default 0x0	esmi_dm_cnt	des	
31:0  1.11.	dm_cnt  505 esmi  00 Packet (	i_s0_cnt16 Count Register						cription
31:0  1.11.	dm_cnt  505 esmi  D0 Packet C	_s0_cnt16 Count Register ket count	rw	na	0x0		des	0xA02113C0
31:0  1.11.  SENE SENE bits	dm_cnt  505 esmi  D0 Packet C	i_s0_cnt16 Count Register					des	cription
31:0  1.11.  SENE SENE bits	dm_cnt  505 esmi  00 Packet 0  00 total pace	_s0_cnt16 Count Register ket count	rw s/w	na h/w	0x0	esmi_dm_cnt	des	0xA02113C0
31:0 1.11. SENI SENI bits 7:0	dm_cnt  505 esmi  D0 Packet C  D0 total pace  r  s0_cnt	_s0_cnt16 Count Register ket count	rw s/w	na h/w	0x0	esmi_dm_cnt	des	0xA02113C0
31:0  1.11.  SENE SENE bits 7:0  1.11.	dm_cnt  505 esmi  D0 Packet C  D0 total pace r s0_cnt  506 esmi	i_s0_cnt16 Count Register sket count	rw s/w rw	na h/w	0x0	esmi_dm_cnt	des des	0xA02113C0 cription
31:0  1.11.3  SENE SENE bits 7:0  1.11.3  SENE total SENE bits	dm_cnt  505 esmi  D0 Packet C  D0 total pace  r  s0_cnt  506 esmi  D0 CRC err  SENDO CRC	i_s0_cnt16 Count Register sket count name  i_s0_crc16 or Count Regis	rw s/w rw	h/w na	0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	0xA02113C0 cription
31:0  1.11.  SENE SENE bits 7:0  1.11.  SENE total Sene bits	505 esmi D0 Packet C D0 total pac r s0_cnt  506 esmi D0 CRC err SENDO CRC	i_s0_cnt16 Count Register eket count name i_s0_crc16 or Count Regist C error count	s/w rw	h/w na	default 0x0	esmi_dm_cnt	des des	0xA02113C0  cription  0xA02113C4
31:0  1.11.  SENE SENE bits 7:0  1.11.  SENE total Sibits 3:0	dm_cnt  505 esmi  D0 Packet C  D0 total pace  r  s0_cnt  506 esmi  D0 CRC err  SENDO CRC  r  s0_crc	i_s0_cnt16 Count Register eket count name i_s0_crc16 or Count Regist C error count name	s/w rw	h/w na	0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	OxA02113C0  Cription  OxA02113C4  Cription
31:0  1.11.  SENE SENE bits 7:0  1.11.  SENE total S bits 3:0	dm_cnt  505 esmi  D0 Packet C  D0 total pace  r  s0_cnt  506 esmi  D0 CRC err  SENDO CRC  r  s0_crc	i_s0_cnt16 Count Register cket count name  i_s0_crc16 or Count Regis C error count name	s/w rw	h/w na	0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	0xA02113C0  cription  0xA02113C4
31:0  1.11.3  SENI SENI bits 7:0  1.11.3  SENI total Sibits 3:0  1.11.4	dm_cnt  505 esmi  D0 Packet C  D0 total pace  r  s0_cnt  506 esmi  D0 CRC err  SENDO CRC  r  s0_crc	i_s0_cnt16 Count Register cket count name i_s0_crc16 or Count Regist C error count name i_s1_cnt16 Count Register	s/w rw	h/w na	0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	OxA02113C0  Cription  OxA02113C4  Cription
31:0  1.11.  SENE SENE bits 7:0  1.11.  SENE total Sign bits 3:0  1.11.  SENE SENE bits	dm_cnt  505 esmi  D0 Packet (CD) total pace s0_cnt  506 esmi  D0 CRC err SENDO CR r s0_crc  507 esmi  D1 Packet (CD) total pace r	i_s0_cnt16 Count Register cket count name i_s0_crc16 or Count Regist C error count name i_s1_cnt16 Count Register	s/w rw	h/w na h/w	default 0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt esmi_s0_crc	des des	0xA02113C0  cription  0xA02113C4  cription
31:0  1.11.  SENE SENE bits 7:0  1.11.  SENE total Sign bits 3:0  1.11.	dm_cnt  505 esmi  D0 Packet (CD) total pace  s0_cnt  506 esmi  D0 CRC err SENDO CRC  r s0_crc  507 esmi  D1 Packet (CD) total pace	i_s0_cnt16 Count Register ket count name i_s0_crc16 or Count Regist C error count name i_s1_cnt16 Count Register ket count	s/w rw	h/w na h/w	default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	oxA02113C0  cription  0xA02113C4  cription  0xA02113C8
31:0  1.11.3  SENE SENE bits 7:0  1.11.3  SENE total Signature of the sene sene sene sene sene sene sene se	dm_cnt  505 esmi  D0 Packet C  D0 total pace rs0_cnt  506 esmi  D0 CRC err SENDO CR rs0_crc  507 esmi  D1 Packet C  D1 total pace rs0_cnt	i_s0_cnt16 Count Register ket count name i_s0_crc16 or Count Regist C error count name i_s1_cnt16 Count Register ket count	s/w rw	h/w na h/w	default 0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt esmi_s0_crc	des des	oxA02113C0  cription  0xA02113C4  cription  0xA02113C8

SEND1 CRC error Count Register total SEND1 CRC error count

bits	name	s/w	h/w	default		des	cription
6:0 s1_cr		rw	na	0x0	esmi_s1_crc	uco	op.1011
.11.509 e	smi_s2_cnt16					Reg.	0xA02113D0
	ket Count Register I packet count	•					
bits	name	s/w	h/w	default		des	cription
7:0 s2_cr	t	rw	na	0x0	esmi_s2_cnt		
11 510 6	smi_s2_crc16					Reg.	0xA02113D4
	C error Count Regis	ster				*******	0X (02 ) 10D 1
	2 CRC error count						
bits	name	s/w	h/w	default		des	cription
3:0 s2_cr	С	rw	na	0x0	esmi_s2_crc		
1 11 511 5	smi_s7_cnt16					Reg.	0xA02113D8
							UNAUZIIJUO
	ket Count Register I packet count	•					
bits	name	s/w	h/w	default	. =	des	cription
7:0 s7_cr	t	rw	na	0x0	esmi_s7_cnt		
	smi_s7_crc16					Reg.	0xA02113DC
SEND7 CR	esmi_s7_crc16 C error Count Regis 7 CRC error count	ster				Reg.	0xA02113DC
SEND7 CR total SEND7 bits	C error Count Regis 7 CRC error count name	s/w	h/w	default			0xA02113DC
SEND7 CR total SEND7 bits	C error Count Regis 7 CRC error count name		h/w na	default 0x0	esmi_s7_crc		
SEND7 CR total SEND7 bits	C error Count Regis 7 CRC error count name	s/w			esmi_s7_crc		
SEND7 CRI total SEND7 bits 3:0 s7_cr	C error Count Regis 7 CRC error count name	s/w			esmi_s7_crc		
SEND7 CRI total SEND7 bits 3:0 s7_cr	C error Count Regis 7 CRC error count name c	s/w			esmi_s7_crc	des	cription
SEND7 CRI total SEND7 bits 3:0 s7_cr	C error Count Registront Count name c csmi_rd_cnt16 et Count Register	s/w			esmi_s7_crc	des.	cription
SEND7 CRI total SEND7 bits 3:0 s7_cr 1.11.513 e READ Pack READ total bits	C error Count Register packet count name	s/w rw	na	0x0	esmi_s7_crc	des.	oxA02113E0
SEND7 CRI total SEND7 bits 3:0 s7_cr 1.11.513 e READ Pack READ total bits	C error Count Register packet count name	s/w rw	na h/w	0x0		des.	oxA02113E0
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e  READ Pack READ total bits 7:0 rd_cn	C error Count Register packet count name	s/w rw	na h/w	0x0		des.	oxA02113E0
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e  READ Pack READ total bits 7:0 rd_cn  1.11.514 e  READ CRC	C error Count Registr CRC error count name  c  smi_rd_cnt16  et Count Register packet count name t	s/w rw	na h/w	0x0		des.	0xA02113E0
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e  READ Pack READ total bits 7:0 rd_cn  READ CRC total READ bits	C error Count Regist C CRC error count name c csmi_rd_cnt16 et Count Register packet count name t esmi_rd_crc16 error Count Regist CRC error count name	s/w rw	na h/w	0x0  default 0x0	esmi_rd_cnt	Reg.	0xA02113E0
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e  READ Pack READ total bits 7:0 rd_cn  I.11.514 e  READ CRC total READ bits	C error Count Regist C CRC error count name c csmi_rd_cnt16 et Count Register packet count name t esmi_rd_crc16 error Count Regist CRC error count name	s/w rw	h/w na	0x0  default 0x0		Reg.	oxA02113E0  cription  0xA02113E4
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e  READ Pack READ total bits 7:0 rd_cn  READ CRC total READ bits	C error Count Regist C CRC error count name c csmi_rd_cnt16 et Count Register packet count name t esmi_rd_crc16 error Count Regist CRC error count name	s/w rw	h/w na	0x0  default 0x0	esmi_rd_cnt	Reg.	oxA02113E0  cription  0xA02113E4
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e READ Pack READ total bits 7:0 rd_cn  1.11.514 e READ CRC total READ bits 3:0 rd_crc	C error Count Regist C CRC error count name c csmi_rd_cnt16 et Count Register packet count name t esmi_rd_crc16 error Count Regist CRC error count name	s/w rw	h/w na	0x0  default 0x0	esmi_rd_cnt	Reg.	oxA02113E0  cription  0xA02113E4
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e READ Pack READ total bits 7:0 rd_cn  1.11.514 e READ CRC total READ bits 3:0 rd_crc  1.11.515 e Direct Addre	C error Count Regist C CRC error count name c esmi_rd_cnt16 et Count Register packet count name t esmi_rd_crc16 error Count Regist CRC error count name c esmi_da_cnt16 ess Request Count	s/w rw s/w rw	h/w na h/w	0x0  default 0x0	esmi_rd_cnt	des	oxA02113E0  OxA02113E4  cription
SEND7 CRI total SEND7 bits 3:0 s7_cr  1.11.513 e  READ Pack READ total bits 7:0 rd_cn  1.11.514 e  READ CRC total READ bits 3:0 rd_crc  1.11.515 e  Direct Addre	c error Count Regist c CRC error count name c esmi_rd_cnt16 et Count Register packet count name t esmi_rd_crc16 error Count Regist CRC error count name c esmi_da_cnt16	s/w rw s/w rw	h/w na h/w	0x0  default 0x0	esmi_rd_cnt	desi Reg.	oxA02113E0  OxA02113E4  cription

1.11.516 esmi\_ia\_cnt16

Reg.

0xA02113EC

	ect Address Request Cour ect Address request total c	_	ster		
bits	name	s/w	h/w	default	description
31:0	ia_cnt	rw	na	0x0	esmi_ia_cnt

1.11.	517 esmi_tcmd_cnt	16				Reg.	0xA02113F0
	without waveform Reque without waveform total co		nt Reg	ister			
bits	name	s/w	h/w	default		description	n
7:0	tcmd_cnt	rw	na	0x0	esmi_tcmd_cnt		

1.11.	518 esmi_twcmd_cr	nt16				Reg.	0xA02113F4
	with waveform Request ( with waveform total coun		Registe	er			
bits	name	s/w	h/w	default		description	n
31:0	twcmd_cnt	rw	na	0x0	esmi_twcmd_cnt		

1.11.	519 esmi_dm_cnt16					Reg.	0xA02113F8
	O total write to read Laten ts the total time for DOMC	,	_		t of first write to en	d of first read	
bits	name	s/w	h/w	default		description	า
31:0	dm_cnt	rw	na	0x0	esmi_dm_cnt		

1.11.	520 esmi_s0_cnt17					Reg.	0xA0211400
	00 Packet Count Register 00 total packet count						
bits	name	s/w	h/w	default		description	١
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt		

1.11.	521 esmi_s0_crc17					Reg.	0xA0211404
	00 CRC error Count Regis SEND0 CRC error count	ster					
bits	name	s/w	h/w	default		description	า
3:0	s0_crc	rw	na	0x0	esmi_s0_crc		

1.11.	522 esmi_s1_cnt17					Reg.	0xA0211408
	01 Packet Count Register 01 total packet count						
bits	name	s/w	h/w	default		description	n
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt		

1.11.	523 esmi_s1_crc17					Reg.	0xA021140C
	01 CRC error Count Regis SEND1 CRC error count	ster					
bits	name	s/w	h/w	default		description	า
3:0	s1_crc	rw	na	0x0	esmi_s1_crc		

.11.524 esmi_s2_cnt17					Reg.	0xA0211410
SEND2 Packet Count Register SEND2 total packet count						
bits name	s/w	h/w	default		desc	cription
:0 s2_cnt	rw	na	0x0	esmi_s2_cnt		
44 505					Pag	0.40004444
.11.525 esmi_s2_crc17					Reg.	0xA0211414
SEND2 CRC error Count Regis total SEND2 CRC error count	ster					
bits name	s/w	h/w	default		desc	cription
:0 s2_crc	rw	na	0x0	esmi_s2_crc		
44 500 0000: 07 00447					Reg	0xA0211418
.11.526 esmi_s7_cnt17					Reg.	UXAU211416
SEND7 Packet Count Register SEND7 total packet count						
bits name	s/w	h/w	default		desc	cription
:0 s7_cnt	rw	na	0x0	esmi_s7_cnt		
.11.527 esmi_s7_crc17					Reg.	0xA021141C
SEND7 CRC error Count Regis	etor				======	0XA0211410
otal SEND7 CRC error count	SIG1					
bits name	s/w	h/w	default		desc	cription
:0 s7_crc	rw	na	0x0	esmi_s7_crc		
.11.528 esmi_rd_cnt17					Reg.	0xA0211420
READ Packet Count Register READ total packet count						
bits name	s/w	h/w	default		desc	cription
:0 rd_cnt	rw	na	0x0	esmi_rd_cnt		•
.11.529 esmi_rd_crc17					Reg.	0xA0211424
.11.529 esmi_rd_crc17 READ CRC error Count Regist total READ CRC error count	er				Reg.	0xA0211424
READ CRC error Count Regist	er s/w	h/w	default			0xA0211424
READ CRC error Count Regist total READ CRC error count	-	h/w na	default 0x0	esmi_rd_crc		
READ CRC error Count Regist total READ CRC error count bits name :0 rd_crc	s/w			esmi_rd_crc	desc	cription
READ CRC error Count Regist total READ CRC error count bits name :0 rd_crc	s/w rw	na		esmi_rd_crc		
READ CRC error Count Regist total READ CRC error count bits name:  o rd_crc  .11.530 esmi_da_cnt17  Direct Address Request Count	s/w rw	na	0x0	esmi_rd_crc	desc	cription
READ CRC error Count Regist total READ CRC error count  bits name :0 rd_crc  .11.530 esmi_da_cnt17  Direct Address Request Count Direct Address request total co bits name	s/w rw	na	0x0		deso	cription
READ CRC error Count Regist total READ CRC error count bits name :0 rd_crc  .11.530 esmi_da_cnt17  Direct Address Request Count Direct Address request total co	s/w rw Registe	na er	0x0	esmi_rd_crc esmi_da_cnt	deso	OxA0211428
READ CRC error Count Regist total READ CRC error count  bits name  :0 rd_crc  .11.530 esmi_da_cnt17  Direct Address Request Count Direct Address request total co bits name	s/w rw Registe unt	na er h/w	0x0		deso	OxA0211428

bits	name	s/w	h/w	default		des	cription
1:0 ia	_cnt	rw	na	0x0	esmi_ia_cnt		
11 53	2 esmi_tcmd_cn	nt17				Reg.	0xA0211430
TREF w	ithout waveform Requ	uest Cou	nt Reg	jister			
	ithout waveform total			1.6.16			• •
bits 7:0 tc	name md_cnt	s/w rw	h/w na	default 0x0	esmi_tcmd_cnt	aes	cription
.0 10	ma_one	1 44	Πα	ONO	oom_toma_om		
.11.53	3 esmi_twcmd_d	cnt17				Reg.	0xA0211434
	ith waveform Reques		Registe	er			
bits	name	s/w	h/w	default		des	cription
	rcmd_cnt	rw	na	0x0	esmi_twcmd_cnt	430	
1.11.53	4 esmi_dm_cnt1	17				Reg.	0xA0211438
DOMO t	otal write to read Late	encv Cou	nt Red	nictor			
	the total time for DOM				rt of first write to en	d of first re	ad
					art of first write to en		ad cription
Counts to	the total time for DOM	//O W/R t	ransad	ction, from sta	esmi_dm_cnt		
Counts to	the total time for DOM name	NO W/R to	ransad h/w	ction, from sta default			
Counts to bits 31:0 dr	the total time for DOM name	MO W/R to	ransad h/w	ction, from sta default			
bits 31:0 dr 1.11.53	the total time for DOM name n_cnt	S/W rW	ransad h/w	ction, from sta default		des	cription
Dits 31:0 dr 1.11.53	name n_cnt  5 esmi_s0_cnt18	S/W rW	ransad h/w	ction, from sta default		des	cription
bits 31:0 dr  1.11.53 SENDO SENDO bits	name n_cnt  5 esmi_s0_cnt18 Packet Count Registe total packet count	MO W/R to	h/w na h/w	default 0x0		des	0xA0211440
bits 31:0 dr 1.11.53 SENDO SENDO bits	name n_cnt  5 esmi_s0_cnt18  Packet Count Registe total packet count name	MO W/R to s/w rw	h/w na h/w	default 0x0	esmi_dm_cnt	des	0xA0211440
bits 31:0 dr  1.11.53 SENDO SENDO bits 7:0 s0	name n_cnt  5 esmi_s0_cnt18  Packet Count Registe total packet count name	MO W/R to s/w rw	h/w na h/w	default 0x0	esmi_dm_cnt	des	0xA0211440
bits 31:0 dr  1.11.53 SENDO bits 7:0 s0	name n_cnt  5 esmi_s0_cnt18  Packet Count Registe total packet count name 0_cnt	S/W rw s/w rw s/w rw	h/w na h/w	default 0x0	esmi_dm_cnt	des	0xA0211440
bits 31:0 dr  1.11.53 SENDO bits 7:0 s0	name n_cnt  5 esmi_s0_cnt18 Packet Count Registe total packet count name 0_cnt  6 esmi_s0_crc18 CRC error Count Reg	S/W rw s/w rw s/w rw	h/w na h/w	default 0x0	esmi_dm_cnt	des des	0xA0211440
Counts to bits 31:0 dr 1.11.53 SENDO SENDO bits 7:0 s0	name n_cnt  5 esmi_s0_cnt18 Packet Count Registe total packet count name 0_cnt  6 esmi_s0_crc18	MO W/R to s/w rw	h/w na h/w	default 0x0	esmi_dm_cnt	des	0xA0211440 cription
bits 31:0 dr  1.11.53 SENDO bits 7:0 s0  1.11.53 SENDO total SE bits	name n_cnt  5 esmi_s0_cnt18 Packet Count Registe total packet count name 0_cnt  6 esmi_s0_crc18 CRC error Count Reg	S/W rW rW rW rW	h/w na h/w na	default 0x0  default 0x0	esmi_dm_cnt	des des	0xA0211440  OxA0211444
bits 31:0 dr  1.11.53 SENDO bits 7:0 s0  1.11.53 SENDO total SE bits 3:0 s0	name n_cnt  5 esmi_s0_cnt18 Packet Count Registe total packet count name 0_cnt  CRC error Count RegND0 CRC error count	S/W rw  8 er  8 gister t s/w rw	h/w na h/w na	default 0x0  default 0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	0xA0211440  OxA0211444
Counts to bits 31:0 dr 1.11.53 SENDO bits 7:0 s0 s0 s1.11.53 SENDO total SE bits 3:0 s0 s0 senDO senDO bits 7:0 s0	name n_cnt  5 esmi_s0_cnt18 Packet Count Registe total packet count name 0_cnt  CRC error Count RegND0 CRC error count name	S/W rw  S/W rw  S/W rw  S/W rw  S/W rw	h/w na h/w na	default 0x0  default 0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	0xA0211440  OxA0211444  OxA0211444  Oxinity in the content of the
Counts to bits 31:0 dr 1.11.53 SENDO bits 7:0 s0 s0 s1.11.53 SENDO total SE bits 3:0 s0 s0 senDO senDO bits 7:0 s0	name n_cnt  5 esmi_s0_cnt18 Packet Count Registe total packet count name 0_cnt  6 esmi_s0_crc18 CRC error Count RegND0 CRC error count name 0_crc 7 esmi_s1_cnt18 Packet Count Registe	S/W rw  S/W rw  S/W rw  S/W rw  S/W rw	h/w na h/w na	default 0x0  default 0x0  default 0x0	esmi_dm_cnt esmi_s0_cnt	des des	0xA0211440  OxA0211444  OxA0211444  Oxinity in the content of the

1.11.538	8 esmi_s1_crc18					Reg.	0xA021144C
	CRC error Count Regist ID1 CRC error count	ter					
bits	name	s/w	h/w	default		des	cription
3:0 s1_	_crc	rw	na	0x0	esmi_s1_crc		

	02 Packet Count Register 02 total packet count				
bits	name	s/w	h/w	default	description
7:0	s2_cnt	rw	na	0x0	esmi_s2_cnt

1.11.	540 esmi_s2_crc18					Reg.	0xA0211454
	02 CRC error Count Regis SEND2 CRC error count	ster					
bits	name	s/w	h/w	default		description	า
3:0	s2_crc	rw	na	0x0	esmi_s2_crc		

1.11.	541 esmi_s7_cnt18		Reg.	0xA0211458			
	07 Packet Count Register 07 total packet count						
bits	name	s/w	h/w	default		description	า
7:0	s7_cnt	rw	na	0x0	esmi_s7_cnt		

1.11.	542 esmi_s7_crc18	I.11.542 esmi_s7_crc18									
	07 CRC error Count Regis SEND7 CRC error count	ster									
bits	name	s/w	h/w	default		description	า				
3:0	s7_crc	rw	na	0x0	esmi_s7_crc						

1.11.	543 esmi_rd_cnt18		Reg.	0xA0211460			
	Packet Count Register  total packet count						
bits	name	s/w	h/w	default		description	า
7:0	rd_cnt	rw	na	0x0	esmi_rd_cnt		

1.11.	544 esmi_rd_crc18					Reg.	0xA0211464
	OCRC error Count Regist READ CRC error count	er					
bits	name	s/w	h/w	default		description	n
3:0	rd_crc	rw	na	0x0	esmi_rd_crc		

1.11.	545 esmi_da_cnt18					Reg.	0xA0211468
	t Address Request Count t Address request total co		er				
bits	name	s/w	h/w	default		description	ı
7:0	da_cnt	rw	na	0x0	esmi_da_cnt		

1.11.	546 esmi_ia_cnt	18	R	eg.	0xA021146C		
	ect Address Request ( ect Address request to		ster				
bits	name	s/w	h/w	default		descri	ption
31:0	ia cnt	rw	na	0x0	esmi ia cnt		

.11.5	)41 CSI	mi_tcmd_cnt	10				Reg.	
		waveform Reque waveform total c		nt Reg	gister			
bits		name	s/w	h/w	default		des	cription
7:0	tcmd_cr	nt	rw	na	0x0	esmi_tcmd_cnt		
1.11.5	548 es	mi_twcmd_cı	nt18				Reg.	0xA0211474
		veform Request veform total cour		Registe	er			
bits		name	s/w	h/w	default		des	cription
31:0	twcmd_	cnt	rw	na	0x0	esmi_twcmd_cn	t	
		mi_dm_cnt18		nt Red	aister		Reg.	0xA0211478
Count			) W/R t	ransad	ction, from sta	rt of first write to e		
bits	dm ont	name	s/w	h/w	default	oomi dm oot	des	cription
31:0	dm_cnt		rw	na	0x0	esmi_dm_cnt		
		mi_s0_cnt19					Reg.	0xA0211480
SEND	0 Packe	mi_s0_cnt19 et Count Register acket count						
SEND SEND bits	00 Packe 00 total p	et Count Register	s/w	h/w	default	anni a0 ant		0xA0211480
SEND SEND bits	0 Packe	et Count Register eacket count		h/w na	default 0x0	esmi_s0_cnt		
SEND SEND bits	00 Packe 00 total p	et Count Register eacket count	s/w			esmi_s0_cnt		
SEND SEND bits 7:0	00 Packe 00 total p s0_cnt	et Count Register eacket count	s/w			esmi_s0_cnt		
SEND SEND bits 7:0	00 Packe 00 total p s0_cnt	et Count Register packet count name	s/w rw			esmi_s0_cnt	des	cription
SEND SEND bits 7:0	00 Packe 00 total p s0_cnt	et Count Register packet count name  mi_s0_crc19  error Count Register	s/w rw			esmi_s0_cnt	des	cription
SEND SEND bits 7:0	00 Packe 00 total p s0_cnt	et Count Register packet count name  mi_s0_crc19  error Count Register CRC error count	s/w rw	na	0x0	esmi_s0_cnt	des	OxA0211484
SEND SEND bits 7:0	s0_cnt  551 esi 00 CRC 6	et Count Register packet count name  mi_s0_crc19  error Count Register CRC error count	s/w rw	na h/w	0x0		des	OxA0211484
SEND SEND bits 7:0 1.11.5 SEND total S bits 3:0	s0_cnt  551 esi 60 CRC 66 6END0 C	et Count Register packet count name  mi_s0_crc19  error Count Register CRC error count	s/w rw	na h/w	0x0		des	OxA0211484
SEND SEND bits 7:0 1.11.5 SEND total S bits 3:0	s0_cnt  551 esi 60 CRC 6 6END0 C  552 esi 61 Packe	et Count Register backet count name  mi_s0_crc19  error Count Regis CRC error count name	s/w rw	na h/w	0x0		des des	0xA0211484
SEND SEND bits 7:0 1.11.5 SEND total S bits 3:0	s0_cnt  551 esi 60 CRC 6 6END0 C  552 esi 61 Packe	et Count Register backet count name  mi_s0_crc19 error Count Register cRC error count name  mi_s1_cnt19 et Count Register	s/w rw	na h/w	0x0		des des	0xA0211484
SEND SEND bits 7:0 I.11.5 SEND total S bits 3:0 SEND SEND bits	s0_cnt  551 esi 60 CRC 6 6END0 C  552 esi 61 Packe	mi_s0_crc19 error Count Register cacket count name  mi_s0_crc19 error Count Regist cacket count name  mi_s1_cnt19 et Count Register cacket count	s/w rw	h/w na	0x0  default 0x0		des des	0xA0211484 cription 0xA0211488
SEND SEND bits 7:0 SEND total S bits 3:0 SEND SEND bits	s0_cnt  551 esi 0 CRC 6 SENDO C  552 esi 1 Packe	mi_s0_crc19 error Count Register cacket count name  mi_s0_crc19 error Count Regist cacket count name  mi_s1_cnt19 et Count Register cacket count	s/w rw	h/w na	0x0  default 0x0	esmi_s0_crc	des des	0xA0211484 cription 0xA0211488
SEND SEND bits 7:0 SEND total S bits 3:0 SEND bits 7:0	s0_cnt  551 esi 50 CRC 6 6END0 C  552 esi 11 Packe 11 total p	mi_s0_crc19 error Count Register cacket count name  mi_s0_crc19 error Count Regist cacket count name  mi_s1_cnt19 et Count Register cacket count	s/w rw	h/w na	0x0  default 0x0	esmi_s0_crc	des des	0xA0211484 cription 0xA0211488
SEND SEND bits 7:0 I.11.5 SEND total S bits 3:0 SEND bits 7:0	s0_cnt  551 esi  0 CRC 6  END0 C  552 esi  1 Packe 1 total p	et Count Register packet count name  mi_s0_crc19  error Count Register cRC error count name  mi_s1_cnt19  et Count Register packet count name	s/w rw	h/w na	0x0  default 0x0	esmi_s0_crc	des des	0xA0211484  OxA0211488  Oxample of the content of t
SEND SEND bits 7:0 I.11.5 SEND total S bits 3:0 SEND bits 7:0	s0_cnt  551 esi  0 CRC 6  END0 C  552 esi  1 Packe 1 total p	et Count Register packet count name  mi_s0_crc19 error Count Register packet error count name  mi_s1_cnt19 et Count Register packet count name  mi_s1_crc19 error Count Register packet count name	s/w rw	h/w na	0x0  default 0x0	esmi_s0_crc	des des	0xA0211484  OxA0211488  Oxample of the content of t

1.11.554 esmi\_s2\_cnt19

SEND2 Packet Count Register SEND2 total packet count

0xA0211490

Reg.

bits	00 == 1	name	s/w	h/w	default	oomi 50	descri	ption
<b>'</b> :0	s2_cnt		rw	na	0x0	esmi_s2_cnt		
.11.5	55 esr	ni_s2_crc19					Reg.	0xA0211494
		error Count Regis RC error count	ter					
bits		name	s/w	h/w	default		descri	ption
3:0	s2_crc		rw	na	0x0	esmi_s2_crc		
								0.40044400
1.11.5	56 esr	ni_s7_cnt19					Reg.	0xA0211498
		t Count Register acket count						
bits		name	s/w	h/w	default		descri	ption
7:0	s7_cnt		rw	na	0x0	esmi_s7_cnt		
1.11.5	57 esr	ni_s7_crc19					Reg.	0xA021149C
SEND total S	7 CRC e END7 C	error Count Regis RC error count	ter					
bits		name	s/w	h/w	default		descri	ption
3:0	s7_crc		rw	na	0x0	esmi_s7_crc		
1.11.5	58 esr	ni_rd_cnt19					Reg.	0xA02114A0
		Count Register cket count						
bits		name	s/w	h/w	default		descri	ption
7:0	rd_cnt		rw	na	0x0	esmi_rd_cnt		
1.11.5	59 esr	ni_rd_crc19					Reg.	0xA02114A4
		ror Count Registe C error count	er					
bits		name	s/w	h/w	default		descri	ption
3:0	rd_crc		rw	na	0x0	esmi_rd_crc		
1.11.5	60 esr	ni_da_cnt19					Reg.	0xA02114A8
		Request Count l		er				
bits		name	s/w	h/w	default		descri	ption
7:0	da_cnt		rw	na	0x0	esmi_da_cnt		
1.11.5	i61 esr	ni_ia_cnt19					Reg.	0xA02114AC
		ss Request Coun ss request total c		ster				
bits 31:0	ia_cnt	name	s/w rw	h/w na	default 0x0	esmi_ia_cnt	descri	ption

1.11.562 esmi\_tcmd\_cnt19

Reg.

0xA02114B0

TREF without waveform Request Count Register TREF without waveform total count										
bits name s/w h/w default description										
7:0	tcmd cnt	rw	na	0x0	esmi tcmd cnt					

1.11.	563 esmi_twcmd_cr	Reg.	0xA02114B4							
TREF with waveform Request Count Register TREF with waveform total count										
bits name s/w h/w default description										
31:0	twcmd_cnt	rw	na	0x0	esmi_twcmd_cnt					

1.11.	564 esmi_dm_cnt19	Reg.	0xA02114B8						
	O total write to read Laten ts the total time for DOMC	t of first write to end	d of first read						
bits name s/w h/w default description									
31:0	dm_cnt	rw	na	0x0	esmi_dm_cnt				

1.11.	565 esmi_s0_cnt20					Reg.	0xA02114C0			
	SEND0 Packet Count Register SEND0 total packet count									
bits	name	s/w	h/w	default		description	n			
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt					

1.11.	566 esmi_s0_crc20	Reg.	0xA02114C4							
SEND0 CRC error Count Register total SEND0 CRC error count										
bits name s/w h/w default description										
3:0	s0_crc	rw	na	0x0	esmi_s0_crc					

1.11.	567 esmi_s1_cnt20					Reg.	0xA02114C8				
	SEND1 Packet Count Register SEND1 total packet count										
bits	name	s/w	h/w	default		description	١				
7:0	s0_cnt	rw	na	0x0	esmi_s0_cnt						

1.11.	568 esmi_s1_crc20	Reg.	0xA02114CC								
	SEND1 CRC error Count Register total SEND1 CRC error count										
bits	bits name s/w h/w default description										
3:0	s1_crc	rw	na	0x0	esmi_s1_crc						

1.11.	569 esmi_s2_cnt20	Reg.	0xA02114D0								
	SEND2 Packet Count Register SEND2 total packet count										
bits	name	s/w	h/w	default		description	١				
7:0	s2_cnt	rw	na	0x0	esmi_s2_cnt						

.11.57	'0 esmi_s2_cro	20				Reg.	0xA02114D4	
	CRC error Count F ND2 CRC error co							
bits	name	s/w	h/w	default		des	cription	
:0 s2	2_crc	rw	na	0x0	esmi_s2_crc			
.11.57	'1 esmi_s7_cn	t20				Reg.	0xA02114D8	
SEND7	Packet Count Reg total packet count							
bits	name	s/w	h/w	default		des	cription	
	7_cnt	rw	na	0x0	esmi_s7_cnt	400		
.11.57	'2 esmi_s7_cro	20				Reg.	0xA02114DC	
	CRC error Count F ND7 CRC error co							
bits	name	s/w	h/w	default		des	cription	
:0 s7	7_crc	rw	na	0x0	esmi_s7_crc			
.11.57	/3 esmi_rd_cnt	20				Reg.	0xA02114E0	
READ P	Packet Count Regis							
	otal packet count	,	/	1.6.16			• •	
bits :0 rd	name I_cnt	s/w rw	h/w na	default 0x0	esmi_rd_cnt	des	scription	
.11.57	'4 esmi_rd_cro	:20				Reg.	0xA02114E4	
	CRC error Count Ro AD CRC error cou							
bits	name	s/w	h/w	default		des	cription	
:0 rd	I_crc	rw	na	0x0	esmi_rd_crc			
.11.57	'5 esmi_da_cn	t20				Reg.	0xA02114E8	
	ddress Request Co		er					
bits	name	s/w	h/w	default		des	cription	
:0 da	a_cnt	rw	na	0x0	esmi_da_cnt			
.11.57	′6 esmi_ia_cnt	20				Reg.	0xA02114EC	
InDirect	Address Request Address request to	Count Regis	ster					
bits	name	s/w	h/w	default		description		
	_cnt	rw	na	0x0	esmi_ia_cnt			
.11.57	7 esmi_tcmd_	cnt20				Reg.	0xA02114F0	
			at Dar	nictor				
	rithout waveform R rithout waveform to		ıı ıve(	yısı <del>c</del> ı				

bits	name	s/w	h/w	default	description
7:0	tcmd_cnt	rw	na	0x0	esmi_tcmd_cnt

1.11.	578 esmi_twcmd_cr	Reg.	0xA02114F4									
	TREF with waveform Request Count Register TREF with waveform total count											
bits	bits name s/w h/w default description											
31:0	twcmd_cnt	esmi_twcmd_cnt										

1.11.	579 esmi_dm_cnt20	Reg.	0xA02114F8								
	DOMO total write to read Latency Count Register Counts the total time for DOMO W/R transaction, from start of first write to end of first read										
bits	bits name s/w h/w default description										
31:0	dm_cnt	esmi_dm_cnt									

1.11.	580 esmi_tref_int1	Reg.	0xA0211500							
	Internal TREF Enable Register Enables internal TREF									
bits	name	s/w	h/w	default		description	n			
0	tref_int	rw	ro	0x0	esmi_tref_int					

1.11.	581 esmi_tref_freq1	Reg.	0xA0211504							
Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ										
bits	name	s/w	h/w	default		description	1			
31:0	tref_freq	esmi_tref_freq								

1.11.	582 esmi_clk_type	1				Reg.	0xA0211508
clk_d	Type Register uty_cycle: See esmi_clk eq : See esmi_clk_freq_			ncoding			
bits	name	s/w	h/w	default		des	cription
3	clk_duty_cycle	ro	WO	X	esmi_clk_duty	•	
						clk_duty_cycle	
					Name	Value	
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
2:0	clk_freq	ro	WO	X		clk_freq_encod	
					Name	Value	e Description
					enc0	0	No clock de
							tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

## 

1.11.	584 esmi_tref_freq2	Reg.	0xA0211510									
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ											
bits	bits name s/w h/w default description											
31:0	tref_freq	esmi_tref_freq										

1.11.	585 esmi_clk_type2					Reg.	0xA0	211514
clk_d	Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding				
bits	name	s/w	h/w	default		descr	iption	
3	clk_duty_cycle	ro	WO	X	smi_clk_duty_cy enum:esmi_clk_c		encodina	
					Name	Value	<u> </u>	Description
					enc0	0		50% duty cy cle.
					enc1	1		25% duty cy cle.
::0	clk_freq	ro	WO	X	smi_clk_type enum:esmi_clk_f	req_encodir	ng	`
					Name	Value		Description
					enc0	0		No clock de tected
					enc1	1		10.41 MHz
					enc2	2		12.5 MHz
					enc3	3		31.25 MHz
					enc4	4		50 MHz
					enc5	5		62.5 MHz

1.11.	586 esmi_tref_int3	Reg.	0xA0211518							
	Internal TREF Enable Register Enables internal TREF									
bits	name	s/w	h/w	default		description	n			
0	tref_int	rw	ro	0x0	esmi_tref_int					

1.11.	587 esmi_tref_freq3	Reg.	0xA021151C								
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ										
bits	name	n									
31:0	tref_freq	esmi_tref_freq									

1.11.588 esmi_clk_type3	Reg.	0xA0211520
Clock Type Register clk_duty_cycle: See esmi_clk_duty_cycle_encoding clk_freq: See esmi_clk_freq_encoding		

bits	name	s/w	h/w	default			description	
3	clk_duty_cycle	ro	WO	Х		mi_clk_duty_cycle enum:esmi_clk_duty	v cvcle encodina	
						Name	Value	Description
						enc0	0	50% duty cy cle.
					j	enc1	1	25% duty cy cle.
2:0	clk_freq	ro	wo	Х		mi_clk_type enum:esmi_clk_freq	encoding	
						Name	Value	Description
						enc0	0	No clock de tected
						enc1	1	10.41 MHz
						enc2	2	12.5 MHz
						enc3	3	31.25 MHz
						enc4	4	50 MHz
						enc5	5	62.5 MHz

1.11.	589 esmi_tref_int4	Reg.	0xA0211524							
	Internal TREF Enable Register Enables internal TREF									
bits	name	s/w	h/w	default		description	n			
0	tref_int	rw	ro	0x0	esmi_tref_int					

1.11.	590 esmi_tref_freq4	Reg.	0xA0211528							
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ									
bits name s/w h/w default description										
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq					

1.11.	591 esmi_clk_type4	ŀ				Reg.	0xA021152C
clk_d	Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding			
bits	name	s/w	h/w	default		descr	ription
3	clk_duty_cycle	ro	WO	X	esmi_clk_duty_cy		encoding
					Name	Value	Description
					enc0	0	50% duty cy
							cle.
					enc1	1	25% duty cy
							cle.
2:0	clk_freq	ro	wo	X	esmi_clk_type enum:esmi_clk_	_freq_encodir	ng
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.5	592 esmi_tref_int5	Reg.	0xA0211530				
	al TREF Enable Register es internal TREF						
bits	name	s/w	h/w	default		description	n
0	tref_int	rw	ro	0x0	esmi_tref_int		

1.11.	593 esmi_tref_freq5	Reg.	0xA0211534						
Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ									
bits	name	s/w	h/w	default	description				
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq				

1.11.	594 esmi_clk_type5	5				Reg.	0xA0211538
clk_d	Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding			
bits	name	s/w	h/w	default		descript	ion
1	clk_duty_cycle	ro		X	esmi_clk_duty_d	cycle c_duty_cycle_end	coding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
:0	clk_freq	ro	WO	X	esmi_clk_type enum:esmi_clk	_freq_encoding	
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.	595 esmi_tref_int6					Reg.	0xA021153C
	al TREF Enable Register es internal TREF						
bits	name	s/w	h/w	default		description	n
0	tref_int	rw	ro	0x0	esmi_tref_int		

1.11.	596 esmi_tref_freq6	Reg.	0xA0211540							
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ									
bits	name	s/w	h/w	default	description					
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq					

1.11.597 esmi_clk_type6	Reg.	0xA0211544

Clock Type Register clk\_duty\_cycle: See esmi\_clk\_duty\_cycle\_encoding clk\_freq : See esmi\_clk\_freq\_encoding bits s/w h/w default description name clk\_duty\_cycle ro wo X esmi\_clk\_duty\_cycle enum:esmi\_clk\_duty\_cycle\_encoding Name Value Description enc0 0 50% duty cy cle. 1 25% duty cy enc1 cle. 2:0 clk\_freq esmi\_clk\_type ro wo X enum:esmi\_clk\_freq\_encoding Name Value Description 0 No clock de enc0 tected 10.41 MHz enc1 1 12.5 MHz enc2 2 3 31.25 MHz enc3 enc4 4 50 MHz

1.11.	598 esmi_tref_int7					Reg.	0xA0211548
	al TREF Enable Register es internal TREF						
bits	name	s/w	h/w	default		description	١
0	tref_int	rw	ro	0x0	esmi_tref_int		

enc5

5

62.5 MHz

1.11.	599 esmi_tref_freq7	Reg.	0xA021154C						
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ								
bits	name	s/w	h/w	default	description				
31:0	tref freq	rw	ro	0x824	esmi tref freq				

1.11.	600 esmi_clk_typ	e7		Reg.	0xA0211550		
clk_d	Type Register uty_cycle: See esmi_c eq : See esmi_clk_fred			ncoding			
bits	name	s/w	h/w	default		descript	ion
3	clk_duty_cycle	ro	wo	X	esmi_clk_duty_d	cycle <_duty_cycle_end	coding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
2:0	clk_freq	ro	WO	X	esmi_clk_type	c_freq_encoding	
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz

enc4	4	50 MHz
enc5	5	62.5 MHz

1.11.0	601 esmi_tref_int8	Reg.	0xA0211554				
	al TREF Enable Register les internal TREF						
bits	name	s/w	h/w	default	description		
0	tref int	rw	ro	0x0	esmi tref int		

1.11.	602 esmi_tref_freq8	}		Reg.	0xA0211558				
Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ									
bits	name	s/w	h/w	default	description				
31:0	tref freq	rw	ro	0x824	esmi_tref_freq				

1.11.	603 esmi_clk_type8					Reg.	0xA021155C
clk_d	.Type Register uty_cycle: See esmi_clk_c eq : See esmi_clk_freq_e			ncoding			
bits	name	s/w	h/w	default		description	on
3	clk_duty_cycle	ro	wo	X	esmi_clk_duty_cy enum:esmi_clk_		oding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
2:0	clk_freq	ro	WO	X	esmi_clk_type enum:esmi_clk_	frog opcoding	
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.6	604 esmi_tref_int9	Reg.	0xA0211560								
Internal TREF Enable Register Enables internal TREF											
bits name s/w h/w default description											
0	tref_int	rw	ro	0x0	esmi_tref_int						

1.11.	605 esmi_tref_freq9	Reg.	0xA0211564									
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ											
bits	bits name s/w h/w default description											
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq							

1.11.	606 esmi_clk_type	9				Reg.	0xA0211568
clk_d	Type Register uty_cycle: See esmi_clk eq : See esmi_clk_freq_			ncoding			
bits	name	s/w	h/w	default		description	n
	clk_duty_cycle	ro	WO	Х	esmi_clk_duty enum:esmi_	y_cycle _clk_duty_cycle_enco	ding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
::0	clk_freq	ro	wo	X	esmi_clk_type	e clk_freq_encoding	
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.	607 esmi_tref_int10					Reg.	0xA021156C		
Internal TREF Enable Register Enables internal TREF									
bits	name	s/w	h/w	default		description	١		
0	tref_int	rw	ro	0x0	esmi_tref_int				

1.11.0	608 esmi_tref_freq1	Reg.	0xA0211570									
	al TREF Period Register nternal TREF period - De	fault fre	quenc	y 0x0824 -> 6	0 kHZ							
bits	bits name s/w h/w default description											
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq							

1.11.	609 esmi_clk_type1	0				Reg.	0xA0211574	
clk_d	Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding				
bits	name	s/w	h/w	default		descrip	otion	
3 clk_duty_cycle ro wo X esmi_clk_duty_cycle enum:esmi_clk_duty_cycle_encoding								
					Name	Value	Description	
					enc0	0	50% duty cy cle.	
					enc1	1	25% duty cy cle.	
2:0	clk_freq	ro	wo	Х	esmi_clk_type enum:esmi_clk	_freq_encoding	)	
					Name	Value	Description	
					enc0	0	No clock de tected	
					enc1	1	10.41 MHz	
					enc2	2	12.5 MHz	

enc3	3	31.25 MHz
enc4	4	50 MHz
enc5	5	62.5 MHz

1.11.6	610 esmi_tref_int11					Reg.	0xA0211578			
	Internal TREF Enable Register Enables internal TREF									
bits	name	s/w	h/w	default		description	١			
0	tref_int	rw	ro	0x0	esmi_tref_int					

1.11.0	611 esmi_tref_freq1	Reg.	0xA021157C									
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ											
bits	bits name s/w h/w default description											
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq							

1.11.	612 esmi_clk_type1	1				Reg.	0xA0211580
clk_d	:Type Register uty_cycle: See esmi_clk_c eq : See esmi_clk_freq_e			ncoding			
bits	name	s/w	h/w	default		descriptio	n
3	clk_duty_cycle	ro	wo	Х	mi_clk_duty_cyc num:esmi_clk_d	le luty_cycle_enco	ding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
2:0	clk_freq	ro	wo	Х	mi_clk_type num:esmi_clk_fi	eq_encoding	
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.0	613 esmi_tref_int12					Reg.	0xA0211584			
Internal TREF Enable Register Enables internal TREF										
bits	name	s/w	h/w	default		description	n			
0	tref_int	rw	ro	0x0	esmi_tref_int					

1.11.	614 esmi_tref_freq1	Reg.	0xA0211588							
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ									
bits	name	s/w	h/w	default		description	1			
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq					

1.11.	615 esmi_clk_type1	2		Reg.	0xA021158C			
clk_d	x Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding				
bits	name	s/w	h/w	default			descripti	ion
3	clk_duty_cycle ro wo X		Х			clk_duty_cycle ::esmi_clk_duty_cycle_encoding		
					N	ame	Value	Description
					е	nc0	0	50% duty cy cle.
					е	nc1	1	25% duty cy cle.
2:0	clk_freq	ro	WO	X		_clk_type ım:esmi_clk_f	req_encoding	
						ame	Value	Description
					е	nc0	0	No clock de tected
					е	nc1	1	10.41 MHz
					е	nc2	2	12.5 MHz
					е	nc3	3	31.25 MHz
					е	nc4	4	50 MHz
					е	nc5	5	62.5 MHz

1.11.616 esmi_tref_int13						Reg.	0xA0211590
	al TREF Enable Register les internal TREF						
bits	name	s/w	h/w	default		description	١
0	tref_int	rw	ro	0x0	esmi_tref_int		

1.11.0	617 esmi_tref_freq1	Reg.	0xA0211594						
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ								
bits	name	s/w	h/w	default	description				
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq				

1.11.	618 esmi_clk_type1	3			Reg.	0xA	\0211598		
clk_d	Type Register uty_cycle: See esmi_clk_i eq : See esmi_clk_freq_e			ncoding					
bits	name	s/w	h/w	default				description	
3	clk_duty_cycle	ro	WO	X		mi_clk_duty_cy enum:esmi_clk_		cycle_encoding	
						Name		Value	Description
						enc0		0	50% duty cy cle.
						enc1		1	25% duty cy cle.
2:0	clk_freq	ro	wo	X	es	mi_clk_type			
					e	enum:esmi_clk_	freq_	encoding	
						Name		Value	Description
						enc0		0	No clock de

		tected
enc1	1	10.41 MHz
enc2	2	12.5 MHz
enc3	3	31.25 MHz
enc4	4	50 MHz
enc5	5	62.5 MHz

1.11.619 esmi_tref_int14						Reg.	0xA021159C
	al TREF Enable Register es internal TREF						
bits	name	s/w	h/w	default		description	1
0	tref_int	rw	ro	0x0	esmi_tref_int		

1.11.0	620 esmi_tref_freq1	4			Reg.	0xA02115A0			
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ								
bits	name	s/w	h/w	default	description				
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq				

1.11.	621 esmi_clk_type1	4				Reg.	0xA02115A4
clk_d	Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding			
bits	name	s/w	h/w	default		descrip	tion
3	clk_duty_cycle ro v		wo	X	esmi_clk_duty enum:esmi_c	_cycle clk_duty_cycle_en	acoding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
2:0	clk_freq	ro	wo	X	esmi_clk_type enum:esmi_c	clk_freq_encoding	
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.0	622 esmi_tref_int15	Reg.	0xA02115A8					
	Internal TREF Enable Register Enables internal TREF							
bits	name	s/w	h/w	default	description			
0	tref_int	rw	ro	0x0	esmi_tref_int			

1.11.623 esmi_tref_freq15	Reg.	0xA02115AC
Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ		

bits	name	s/w	h/w	default	description
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq

1.11.	624 esmi_clk_typ	Reg.	0xA02115B0				
clk_d	Type Register uty_cycle: See esmi_cl eq : See esmi_clk_frec			ncoding			
bits	name	s/w	h/w	default		descripti	on
3	clk_duty_cycle	ro	wo	X	esmi_clk_duty_	cycle k_duty_cycle_end	coding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
:0	clk_freq	ro	WO	X	esmi_clk_type enum:esmi_cll	k_freq_encoding	
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.	625 esmi_tref_int16	Reg.	0xA02115B4							
	Internal TREF Enable Register Enables internal TREF									
bits	bits name s/w h/w default description									
0	tref_int	rw	ro	0x0	esmi_tref_int					

1.11.0	1.11.626 esmi_tref_freq16										
Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ											
bits	bits name s/w h/w default description										
31:0	31:0 tref_freq rw ro 0x824 esmi_tref_freq										

1.11.	627 esmi_clk_type1	6				Reg.	0xA02115BC
clk_d	Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding			
bits	name	description	1				
3	clk_duty_cycle	ro	wo	X	esmi_clk_duty_cy enum:esmi_clk_ Name enc0 enc1	duty_cycle_encod Value 0 1	Description 50% duty cy cle. 25% duty cy cle.
2:0	clk_freq	ro	WO	Х	esmi_clk_type enum:esmi_clk_	_freq_encoding	1

Name	Value	Description
enc0	0	No clock de
		tected
enc1	1	10.41 MHz
enc2	2	12.5 MHz
enc3	3	31.25 MHz
enc4	4	50 MHz
enc5	5	62.5 MHz

1.11.0	628 esmi_tref_int17		Reg.	0xA02115C0					
	Internal TREF Enable Register Enables internal TREF								
bits	name	s/w	h/w	default		description	١		
0	tref_int	rw	ro	0x0	esmi_tref_int				

1.11.	.11.629 esmi_tref_freq17									
	al TREF Period Register Internal TREF period - Def	ault fre	quenc	y 0x0824 -> 6	0 kHZ					
bits	bits name s/w h/w default description									
31:0	31:0 tref_freq rw ro 0x824 esmi_tref_freq									

1.11.	630 esmi_clk_type1	7				Reg.	0xA02115C8			
clk_d	Type Register uty_cycle: See esmi_clk_ eq : See esmi_clk_freq_e			ncoding						
bits	name	s/w	h/w	default		descri	ption			
3	clk_duty_cycle	ro	wo	Х	esmi_clk_duty_cy		ncoding			
					Name	Value	Description			
					enc0	0	50% duty cy			
							cle.			
					enc1	1	25% duty cy			
							cle.			
2:0	clk_freq	ro	WO	X	esmi_clk_type enum:esmi_clk_freq_encoding					
					Name	Value	Description			
					enc0	0	No clock de tected			
					enc1	1	10.41 MHz			
					enc2	2	12.5 MHz			
					enc3	3	31.25 MHz			
					enc4	4	50 MHz			
					enc5	5	62.5 MHz			

1.11.	631 esmi_tref_int18	Reg.	0xA02115CC							
	Internal TREF Enable Register Enables internal TREF									
bits	name	s/w	h/w	default		description	n			
0	tref_int	rw	ro	0x0	esmi_tref_int					

1.11.632 esmi_tref_freq18	Reg.	0xA02115D0
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	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ										
bits	bits name s/w h/w default description										
31:0	ı										

1.11.	633 esmi_clk_typ	e18				Reg.	0xA02115D4
clk_d	cType Register uty_cycle: See esmi_c eq : See esmi_clk_frec			coding			
bits	name	s/w	h/w	default		descr	ription
3	clk_duty_cycle	ro	WO	X	esmi_clk_duty_ enum:esmi_cl	cycle k_duty_cycle_e	encoding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
2:0	clk_freq	ro	WO	X	esmi_clk_type enum:esmi_cl	k_freq_encodir	ng
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.	634 esmi_tref_int19					Reg.	0xA02115D8				
	Internal TREF Enable Register Enables internal TREF										
bits	name	s/w	h/w	default		description	า				
0	tref_int	rw	ro	0x0	esmi_tref_int						

1.11.0	635 esmi_tref_freq1	9				Reg.	0xA02115DC					
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ											
bits	name	s/w	h/w	default		descriptio	n					
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq							

1.11.	636 esmi_clk_type1	9				Reg.	0xA02115E0					
clk_d	Clock Type Register clk_duty_cycle: See esmi_clk_duty_cycle_encoding clk_freq : See esmi_clk_freq_encoding											
bits	name	s/w	h/w	default		descriptio	n					
3	clk_duty_cycle	ro	WO	X	esmi_clk_duty_cycle enum:esmi_clk_duty_cycle_encoding							
					Name	Value	Description					
					enc0	0	50% duty cy cle.					
					enc1	1	25% duty cy cle.					

2:0	clk_freq	ro	wo	X	es	smi_clk_type		
					(	enum:esmi_clk_frec	_encoding	
						Name	Value	Description
						enc0	0	No clock de
								tected
						enc1	1	10.41 MHz
						enc2	2	12.5 MHz
						enc3	3	31.25 MHz
						enc4	4	50 MHz
						enc5	5	62.5 MHz

1.11.0	637 esmi_tref_int20					Reg.	0xA02115E4				
	Internal TREF Enable Register Enables internal TREF										
bits	name	s/w	h/w	default		description	n				
0	tref_int	rw	ro	0x0	esmi_tref_int						

1.11.	638 esmi_tref_freq2	0				Reg.	0xA02115E8					
	Internal TREF Period Register Sets internal TREF period - Default frequency 0x0824 -> 60 kHZ											
bits	name	s/w	h/w	default		description	n					
31:0	tref_freq	rw	ro	0x824	esmi_tref_freq							

1.11.	639 esmi_clk_type	20				Reg.	0xA02115EC
clk_d	Type Register uty_cycle: See esmi_clk eq : See esmi_clk_freq_			ncoding			
bits	name	s/w	h/w	default		descri	ption
3	clk_duty_cycle	ro	wo	Х	esmi_clk_duty_d	cycle <_duty_cycle_e	encoding
					Name	Value	Description
					enc0	0	50% duty cy cle.
					enc1	1	25% duty cy cle.
2:0	clk_freq	ro	WO	X	esmi_clk_type enum:esmi_cll	<_freq_encodin	g
					Name	Value	Description
					enc0	0	No clock de tected
					enc1	1	10.41 MHz
					enc2	2	12.5 MHz
					enc3	3	31.25 MHz
					enc4	4	50 MHz
					enc5	5	62.5 MHz

1.11.0	640 euv_sim1		Reg.	0xA02115F0				
bits	bits name s/w h/w default description							
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.			

bits	name	s/w	h/w	default	de	scription		
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.			

1.11.	642 euv_sim3	Reg.	0xA02115F8					
bits name s/w h/w default description								
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.			

1.11.0	643 euv_sim4	Reg.		0xA02115FC					
bits	bits name s/w h/w default description								
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.				

1.11.	644 euv_sim5			Reg.	0xA0211600			
bits	bits name s/w h/w default description							
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.			

1.11.0	645 euv_sim6	Reg.	0xA0211604						
bits	bits name s/w h/w default description								
23:0	euv_sim	rw	ro	0x0		ets the simulated energy value when simulation is enled. This is a HW only feature.			

1.11.0	646 euv_sim7	Reg.	0xA0211608						
bits	bits name s/w h/w default description								
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.				

1.11.0	647 euv_sim8	Reg.	0xA021160C						
bits name s/w h/w default description									
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.				

1.11.0	648 euv_sim9	Reg.	0xA0211610						
bits name s/w h/w default description									
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.				

1.11.0	649 euv_sim10	Reg.	0xA0211614						
bits name s/w h/w default description									
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy value when simulation is enabled. This is a HW only feature.				

l.11.	650 euv_sim11				Reg.	0xA0211618
bits 23:0	name euv_sim	s/w rw	h/w ro	default 0x0		escription value when simulation is en- ature.
I.11.	651 euv_sim12				Reg.	0xA021161C
bits	name	s/w	h/w	default	do	escription
23:0	euv_sim	rW	ro	0x0		value when simulation is en-
1.11.	652 euv_sim13				Reg.	0xA0211620
bits	name	s/w	h/w	default		escription
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy abled. This is a HW only fe	value when simulation is enature.
l.11.	653 euv_sim14				Reg.	0xA0211624
1	_	,	/	1.6.16		. ,.
bits 23:0	name euv_sim	s/w rw	h/w ro	default 0x0		escription value when simulation is en- ature.
.11.	654 euv_sim15				Reg.	0xA0211628
bits	name	s/w	h/w	default		escription
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy abled. This is a HW only fe	value when simulation is enature.
1.44	CEE and aim 10				Ren	0xA021162C
	655 euv_sim16				Reg.	0XA021102C
bits	name	s/w	h/w	default		escription
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy abled. This is a HW only fe	value when simulation is enature.
l.11.	656 euv_sim17				Reg.	0xA0211630
bits	name	s/w	h/w	default		escription
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy abled. This is a HW only fe	value when simulation is enature.
l.11.	657 euv_sim18				Reg.	0xA0211634
bits 23:0	name euv_sim	s/w rw	h/w ro	default 0x0		escription value when simulation is en-
.0.0		I VV	10		abled. This is a HW only fe	

bits

1.11.658 euv\_sim19

name

default

s/w h/w

Reg.

description

0xA0211638

23:0	euv_sim	rw	ro	0x0	Sets the simulated energy va abled. This is a HW only feat				
					,				
.11	.659 euv_sim20				Reg.	0xA021163C			
bits	name	s/w	h/w	default	desi	cription			
23:0	euv_sim	rw	ro	0x0	Sets the simulated energy va abled. This is a HW only feat	alue when simulation is en-			
1.11.	.660 esmi_scratch				Reg.	0xA0211640			
	tchpad Test Register tchpad test register to e	ensure pro	per R/	W communca	ution				
bits	name	s/w	h/w	default		cription			
31:0	scratch	rw	na	0x0	esmi_scratch	•			
1.11.	.661 esmi_s7_1ms	_cnt			Reg.	0xA0211644			
SEN	D7 1ms packet counter								
bits	name	s/w	h/w	default	des	cription			
:3:16	rxd_min	ro	wo	0x0	Minimum number of Send7 packets received in a 1ms wir dow				
5:8	rxd_max	ro	wo	0x0	Maximum number of Send7 packets received in a 1ms will dow				
7:0	rxd_last	ro	WO	0x0		ceived in the last 1ms window			
	rxd_last			0x0		oceived in the last 1ms window 0xA0211648			
1.11	.662 esmi_xpam_b	ow_ovld		0x0	Number of Send7 packets re				
I <b>.</b> 11.		ow_ovld		0x0	Number of Send7 packets re	0xA0211648			
1.11 xPAI bits	.662 esmi_xpam_b	ow_ovld		, ,	Number of Send7 packets re				
.11   xPAI   bits   9:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld	ow_ovld register s/w rw	h/w	default	Number of Send7 packets re	0xA0211648			
xPAI bits 19:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld .663 esmi_xpam_i	register s/w rw	h/w	default	Number of Send7 packets re	0xA0211648 cription			
xPAI bits 19:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld .663 esmi_xpam_in M Initialization Error reg	ow_ovld register s/w rw nit_err	h/w rw	default 0x0	Number of Send7 packets re	0xA0211648 cription 0xA021164C			
1.11.xPAI bits 19:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld .663 esmi_xpam_i	register s/w rw	h/w	default	Number of Send7 packets re	0xA0211648 cription			
bits 9:0	.662 esmi_xpam_b  M Bandwidth Overload r name bw_ovld  .663 esmi_xpam_in  M Initialization Error reginame	register s/w rw  nit_err ister s/w rw	h/w rw	default 0x0	Number of Send7 packets re  Reg.  description  Reg.  Reg.  description   0xA0211648 cription 0xA021164C				
bits 19:0 1.11 xPAI bits 19:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld  .663 esmi_xpam_in M Initialization Error reg name init_err	register s/w rw  nit_err ister s/w rw	h/w rw	default 0x0	Number of Send7 packets re  Reg.  desc  Bandwidth Overload  Reg.  Initialization Error	0xA0211648 cription 0xA021164C cription			
bits 19:0 1.11 xPAI bits 19:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld  .663 esmi_xpam_in M Initialization Error reginame init_err	register s/w rw  nit_err ister s/w rw	h/w rw	default 0x0	Number of Send7 packets re  Reg.  Bandwidth Overload  Reg.  Initialization Error	0xA0211648 cription 0xA021164C cription			
bits 9:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld  .663 esmi_xpam_i M Initialization Error reginame init_err  .664 esmi_xlam_ca M Cable Disconnect reginates	register s/w rw  nit_err ister s/w rw  ab_disc	h/w rw	default 0x0	Number of Send7 packets re  Reg.  Bandwidth Overload  Reg.  Initialization Error	0xA0211648  cription  0xA021164C  cription  0xA0211650			
bits 9:0 1.11 xPAI bits 9:0 1.11 xLAM bits 9:0	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld  .663 esmi_xpam_i M Initialization Error reginame init_err  .664 esmi_xlam_ca M Cable Disconnect reginame	ow_ovld register s/w rw  nit_err ister s/w rw  ab_disc ister s/w rw	h/w rw	default 0x0  default 0x0	Number of Send7 packets re  Reg.	0xA0211648  cription  0xA021164C  cription  0xA0211650			
1.11. xPAI bits 19:0 1.11. xPAI bits 19:0 1.11.	.662 esmi_xpam_b M Bandwidth Overload r name bw_ovld  .663 esmi_xpam_i M Initialization Error reg name init_err  .664 esmi_xlam_ca M Cable Disconnect reg name cab_disc	register s/w rw  nit_err ister s/w rw  ab_disc ister s/w rw	h/w rw	default 0x0  default 0x0	Number of Send7 packets re  Reg.  Bandwidth Overload  Reg.  Initialization Error  desc.  Cable Disconnect	0xA0211648  cription  0xA021164C  cription  0xA0211650  cription			
1.11. xPAI bits 19:0	M Bandwidth Overload raname bw_ovld  .663 esmi_xpam_in  M Initialization Error reganame init_err  .664 esmi_xlam_ca  M Cable Disconnect reganame cab_disc  .665 esmi_adc_clip  M ADC Clip Count Regis	register s/w rw  nit_err ister s/w rw  ab_disc ister s/w rw	h/w rw	default 0x0  default 0x0	Number of Send7 packets re  Reg.  Reg.  Reg.  Reg.  Reg.  Cable Disconnect  Reg.  Reg.  Reg.	0xA0211648  cription  0xA021164C  cription  0xA0211650  cription			

1.11.666 esmi\_adc\_clip\_cnt2

xPAM ADC Clip Count Register

Reg.

0xA0211684

)211688 )21168C
21168C
21168C
21168C
21168C
211690
211694
211698
21169C
2116A0
2116A4
12110A4

bits name
7:0 adc\_clip\_cnt

esmi\_adc\_clip\_cnt

description

s/w h/w default

na 0x0

	.675 esmi_adc_	_clip_cnt11			Reg		0xA02116A8
xPA	M ADC Clip Count F	Register					
bits	name	s/w	h/w	default		description	on
7:0	adc_clip_cnt	rw	na	0x0	esmi_adc_clip_cnt		
1.11	.676 esmi_adc_	clip cnt12			Reg.		0xA02116AC
	M ADC Clip Count F	-				-	
bits		s/w	h/w	default		description	n .
7:0	adc_clip_cnt	rw	na	0x0	esmi_adc_clip_cnt	doddiptii	011
44	<b>677</b>	alin anti			Reg		0xA02116B0
1.11	.677 esmi_adc_	clip_cnt13			Regu		UXAU2116BU
xPA	M ADC Clip Count F	Register					
bits 7:0	name adc_clip_cnt	s/w rw	h/w na	default 0x0	esmi_adc_clip_cnt	description	on
.0	auc_clip_crit	I VV	IIa	UXU	esiii_auc_clip_clit		
1.11	.678 esmi_adc_	clip_cnt14			Reg	1	0xA02116B4
xPA	M ADC Clip Count F	Register					
bits	name	s/w	h/w	default		description	on
7:0	adc_clip_cnt	rw	na	0x0	esmi_adc_clip_cnt		
1 11	.679 esmi_adc_	clin ent15			Reg	-	0xA02116B8
		• —					0,0,102,1,020
	M ADC Clip Count F	-	I- /	-1 - 4 14		-li ti	
bits 7:0	name adc_clip_cnt	s/w rw	h/w na	default 0x0	esmi_adc_clip_cnt	description	UII
1.11	.680 esmi_adc_	clip_cnt16			Reg.		0xA02116BC
xPA	M ADC Clip Count F	Register					
bits		s/w	h/w	default		description	on
7:0	adc_clip_cnt	rw	na	0x0	esmi_adc_clip_cnt		
1.11	.681 esmi_adc_	clip cnt17			Reg.		0xA02116C0
	M ADC Clip Count F	• -				•	
bits	<u> </u>	s/w	h/w	default		description	n .
7:0	adc_clip_cnt	rw	na	0x0	esmi_adc_clip_cnt	doddipti	511
1 4 4	C02 com! - !	alin artido			0		0xA02116C4
	.682 esmi_adc_				Reg.	1	UXAUZ 1 10U4
	M ADC Clip Count F						
bits	name	S/W	h/w	default	esmi_adc_clip_cnt	description	on
7.∩	adc_clip_cnt	rw	na	0x0	esiii_auc_dip_dit		
7:0							
7:0					Reg.		0xA02116C8
	.683 esmi_adc_	clip_cnt19					0000
1.11						1	0.7.10211000
1.11	M ADC Clip Count F		h/w	default	-	descriptio	

1.11.	1.11.684 esmi_adc_clip_cnt20 0xA02116CC											
xPAN	xPAM ADC Clip Count Register											
bits	name	s/w	h/w	default	description							
7:0	adc_clip_cnt	rw	na	0x0	esmi_adc_clip_cn	nt						

1.11.	685 esmi_dat1					Reg.	0xA02116D0			
THIS	REGISTER IS RESERVE	ED								
bits	name	s/w	h/w	default		descri	ption			
15:12	t3_t0	ro v	WO	0x0	ESM/BPAM Status enum:esmi_dat_t_encoding					
					Name	Value	Description			
					enc0	0	Framing or CRC error			
					enc5	5	SPM cable n ot connecte d			
					enc8	8	Normal, val id data			
					encE	14	ESM cable n ot connecte d			
					encF	15	Indicates E SM is in po wer up stat e			
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ct register reac	data			

1.11.	686 esmi_dat2						Reg.	0xA02116D4	
THIS	REGISTER IS RESERVE	D							
bits	name	s/w	h/w	default			description	on	
15:12	t3_t0	ro	WO	0x0	ES				
						Name	Value		Description
						enc0	0		Framing or CRC error
						enc5	5		SPM cable n ot connecte d
						enc8	8		Normal, val id data
						encE	14		ESM cable n ot connecte d
						encF	15		Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ES	SM/BPAM direct	register read da	ata	

1.11.6	687 esmi_dat3	Reg.	0xA02116D8							
THIS	THIS REGISTER IS RESERVED									
bits	bits name s/w h/w default description									
15:12	t3_t0	ro	wo	0x0	ESM/BPAM Statu	S				

						enum:esmi_dat_t_	encoding	
						Name	Value	Description
						enc0	0	Framing or CRC error
						enc5	5	SPM cable n ot connecte d
						enc8	8	Normal, val id data
						encE	14	ESM cable n ot connecte d
						encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	E	SM/BPAM direct re	egister read data	·

1.11.0	688 esmi_dat4					Reg.	0xA02116DC
THIS	REGISTER IS RESERVE	Đ					
bits	name	s/w	h/w	default		description	n
15:12	t3_t0	ro	WO	0x0	enum:esmi_da		
					Name	Value	Description
					enc0	0	Framing or CRC error
		enc5	5	SPM cable n ot connecte d			
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ct register read da	ta

1.11.0	689 esmi_dat5					Reg.	0xA02116E0
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descripti	on
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Stat enum:esmi_dat		
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat

						e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direct register read data	

1.11.0	690 esmi_dat6					Reg.	0xA02116E4
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descripti	on
15:12	t3_t0	ro	WO	0x0	enum:esmi_da		
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat
	I= 10						е
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ect register read d	ata

1.11.	691 esmi_dat7					Reg.	0xA02116E8
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		description	on
15:12	t3_t0	ro	wo	0x0	ESM/BPAM State		
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ct register read d	ata

1.11.0	692 esmi_dat8			Reg.	0xA02116EC						
THIS	THIS REGISTER IS RESERVED										
bits	name	s/w	h/w	default		description	on				
15:12	t3_t0	ro	WO	0x0	enum:esmi_dat_t_encoding  Name Value Description						
					enc0	0	Framing or CRC error				
					enc5	5	SPM cable n				

								ot connecte d
					enc8		8	Normal, val id data
					encE		14	ESM cable n ot connecte d
					encF		15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BP/	AM direct re	gister read data	· ·

1.11.0	693 esmi_dat9					Reg.	0xA02116F0
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descript	tion
15:12	t3_t0	ro	wo	0x0	enum:esmi_dat_	t_encoding	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direct	t register read	data

1.11.0	694 esmi_dat10						Reg.	0xA021	16F4
THIS	REGISTER IS RESERVE	D							
bits	name	s/w	h/w	default			description	า	
15:12	t3_t0	ro	s t_encoding						
						Name	Value		Description
						enc0	0		Framing or CRC error
						enc5	5		SPM cable not connecte
						enc8	8		Normal, val d data
						encE	14		SM cable not connecte
						encF	15	5	ndicates E SM is in po ver up stat
7:0	d7_d0	ro	wo	0x0	ES	M/BPAM direct	register read da	ta	

1.11.695 esmi_dat11	Reg.	0xA02116F8
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THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		description	
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Stat enum:esmi_dat		
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n
							ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direct	ct register read data	a

1.11.	696 esmi_dat12					Reg.	0xA02116FC
THIS	REGISTER IS RESERVE	:D					
bits	name	s/w	h/w	default		descrip	otion
15:12	t3_t0	ro	wo	0x0	enum:esmi_da	t_t_encoding	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ct register read	data

1.11.0	1.11.697 esmi_dat13 0xA0211700										
THIS	REGISTER IS RESERVE	D									
bits	name	s/w	h/w	default			descript	tion			
15:12	t3_t0	ro	WO	0x0		SM/BPAM Statu enum:esmi_dat_					
						Name	Value	Description			
						enc0	0	Framing or CRC error			
						enc5	5	SPM cable n ot connecte d			
						enc8	8	Normal, val id data			
						encE	14	ESM cable n ot connecte			

								d
						encF	15	Indicates E
								SM is in po
								wer up stat
								e
7:0	d7_d0	ro	wo	0x0	E	SM/BPAM direct reg	gister read data	

1.11.6	698 esmi_dat14					Reg.	0xA0211704
THIS	REGISTER IS RESER	RVED					
bits	name	s/w	h/w	default		desc	ription
15:12	t3_t0	ro	WO	0x0	ESM/BPAM Sta		
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat
							e .
<b>'</b> :0	d7_d0	ro	wo	0x0	ESM/BPAM dire	ect register rea	ad data

1.11.0	699 esmi_dat15					Reg.	0xA0211708
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descript	ion
15:12	t3_t0	ro	WO	0x0	ESM/BPAN enum:esm	/I Status ni_dat_t_encoding	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAN	d direct register read of	

1.11.7	700 esmi_dat16	Reg.	0xA021170C				
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		description	١
15:12	t3_t0	ro	wo	0x0	ESM/BPAM Statu	-	
					enum:esmi_dat_	_t_encoding	

					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
0	d7_d0	ro	wo	0x0	ESM/BPAM dir	ect register read dat	

1.11.	701 esmi_dat17					Reg.	0xA0211710
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descriptio	n
15:12	t3_t0	ro	wo	0x0	enum:esmi_c	tatus dat_t_encoding	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM di	rect register read da	-

1.11.	702 esmi_dat18					Reg.	0xA0211714
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descripti	on
15:12	t3_t0	ro	WO	0x0		_dat_t_encoding	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM	direct register read d	ata

1.11.	703 esmi_dat19					Reg.	0xA0211718
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descript	ion
15:12	t3_t0	ro	WO	0x0	enum:esmi_dat		
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAM direct	ct register read o	-

1.11.	704 esmi_dat20					Reg.	0xA021171C
THIS	REGISTER IS RESERVE	D					
bits	name	s/w	h/w	default		descri	ption
15:12	t3_t0	ro	WO	0x0	enum:esn	/I Status ni_dat_t_encoding	
					Name	Value	Description
					enc0	0	Framing or CRC error
					enc5	5	SPM cable n ot connecte d
					enc8	8	Normal, val id data
					encE	14	ESM cable n ot connecte d
					encF	15	Indicates E SM is in po wer up stat e
7:0	d7_d0	ro	wo	0x0	ESM/BPAN	/I direct register reac	l data

1.12 mcdma_feed_registers_srdl	Block	0xA0240000 - 0xA0240F73
Register map if the ingress(machine constatns) Open Loop algo Inputs		

1.12.	1 mcdma_feed_mod	Reg.	0xA0240000						
Defines the module name									
bits	name	s/w	h/w	default		description	1		
31:0	module_name	ro	na	0x77687765	ASCII code for me	odule name for M	CDMA IP in PS = MDMA		

1.12.	2 mcdma_feed_mod	0xA0240004								
Modu	Module version									
bits	name	s/w	h/w	default	description					
31:16	rfu	ro	na	0x521	Algo IO Date					
15:8	major_revision	ro	na	0x3	Major revision - 01 = MCDMA					
7:0	minor_revision	ro	na	0x1	Minor revisoin - 01 = TPG packet rate control					

1.12.	3 mcdma_feed_pag	e_pro	perti	es		Reg.	0xA0240008			
Addre	Address page properties									
bits	name	s/w	h/w	default		description	n			
31	present	ro	wo	0x1		ogic accessed by	present when '0'. It is inthis page is available/im-			
30:16	rfu	ro	na	0x0	Reserver for Futu	ire Use - RFU				
15:8	page_size	ro	na	0x1	Address page siz value to 4k and e		BkB, etc. Divide the real			
7:0	unified_header_ rev	ro	na	0x1	Unified Header Formatial unified header		gisters revision - 01 = ini-			

1.12.	4 mcdma_feed_scra	Reg.	0xA024000C							
Scrat	Scratchregister register									
bits	bits name s/w h/w default description									
31:0	scratchregister									

1.12.	5 mcdma_feed_irq_		Reg.	0xA0240010				
Interrupt Requests Enable/Mask Control Register								
bits	name	s/w	h/w	default	description			
0	irq0_enable	rw	ro	0x0	IRQ0 enable bit. N	Not in use.		
1	irq1_enable	rw	ro	0x0	IRQ1 enable bit. N	Not in use.		

1.12.	6 mcdma_feed_irq_	Reg.	0xA0240014					
Interrupt Pending Status Register								
bits	name	s/w	h/w	default		description	n	
0	irq0_pending	r/w1c	wo	0x0	IRQ0 pending sta interrupt on positi		Write '1' to clear. Asserts se.	
1	irq1_pending	r/w1c	wo	0x0	IRQ1 pending sta interrupt on positi		Write '1' to clear. Asserts se.	

1.12.	7 mcdma_feed_irq_	Reg.	0xA0240018						
Interr	Interrupt Raw Status Register								
bits	name	s/w	h/w		description	า			
0	irq0_raw	ro	WO	0x0	IRQ0 raw status b	it. Not in use.			
1	irq1_raw	ro	wo	0x0	IRQ1 raw status b	it. Not in use.			

1.12.8	mcdma_feed_irq_	Reg.	0xA024001C			
Interrup	ot Force Control Registe	er				
bits	name	s/w h/w	default		descriptio	n

0	irq0_force	rw	ro	0x0	IRQ0 force bit. SW to write '1' to emulate an interrupt. Write '0' to clear. Not in use.
1	irq1_force	rw	ro	0x0	IRQ1 force bit. SW to write '1' to emulate an interrupt. Write
					'0' to clear. Not in use.

# 1.12.9 streamtpg\_en\_ctrl

Reg.

0xA0240020

Control register - Data streams and Test Packet Generators(TPG) Enable. Data Streams are enabled by the 16LSB. TPG are enabled by 16MSB. Stream 0-15 & TPG 0-15 are mapped to MCDMA Channel 1-16.

bits	name	s/w	h/w	default	description
31:0	streamtpg_en	rw	ro	0xFFFF	Bits 15-0 - Data streams 15-0. Bits 31-16 - TPG 15-0. By default all are disabled. Avoid enabling Data streams and TPG on the same channel at the same time!

# 1.12.10 streamsx16\_err\_stat



0xA0240024

Status register - All x16 Data streams errors. One sticky bit per stream/channel, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

bits	name	s/w	h/w	default	description
0	stream0_err	r/w1c	wo	0x0	Stream 0 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
1	stream1_err	r/w1c	wo	0x0	Stream 1 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
2	stream2_err	r/w1c	wo	0x0	Stream 2 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
3	stream3_err	r/w1c	WO	0x0	Stream 3 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
4	stream4_err	r/w1c	wo	0x0	Stream 4 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
5	stream5_err	r/w1c	WO	0x0	Stream 5 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
6	stream6_err	r/w1c	wo	0x0	Stream 6 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
7	stream7_err	r/w1c	wo	0x0	Stream 7 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
8	stream8_err	r/w1c	wo	0x0	Stream 8 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
9	stream9_err	r/w1c	wo	0x0	Stream 9 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
10	stream10_err	r/w1c	wo	0x0	Stream 10 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
11	stream11_err	r/w1c	wo	0x0	Stream 11 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
12	stream12_err	r/w1c	WO	0x0	Stream 12 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
13	stream13_err	r/w1c	wo	0x0	Stream 13 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
14	stream14_err	r/w1c	wo	0x0	Stream 14 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.
15	stream15_err	r/w1c	wo	0x0	Stream 15 error condition, check the channel status regiser for details. Sticky bit. Write '1' to clear.

1.12.	11 tpg0_packet_rate	Reg.	0xA0240034							
Control register - TPG Stream Packet rate										
bits	name	name s/w h/w default description								
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823					

1.12.	12 tpg0_packet_size	Reg.	0xA0240038								
Control register - TPG Stream Packet size											
bits	bits name s/w h/w default description										
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64l register value of 0 clock sample of 1 128bit(16Byte) w	Bytes(4 clock sam 0x40. The 4 LSBit 6Bytes. Each cloo ide bus sample or tains a 4bit strean	125MHz clock. Minimum ples x16Bytes each) = s count the Bytes in one ck period generates a the AXI-Stream bus. In number in the MSB in the LSB 32bit.				

1.12.	13 stream0_expsize	_dis_	Reg.	0xA024003C						
Control register - Data stream expected packet size.										
bits	bits name s/w h/w default description									
31:0	stream0_expsize _dis	rw	ro	0x4D	Bits 15-0 - Data stream expected packet size in 4Byte incoments (LSbit = 4Bytes). Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.					

1.12.	14 stream0_exprate	Reg.	0xA0240040							
Control register - Data stream expected packet rate.										
bits	name	description	1							
31:0	stream0_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set D tion in 125MHz cl Bit 31 - set to 1 to	distance between in clocks. I disable packet rate with deviation + lata stream expectocks. Default 0x76 disable rate deviation to the control of the control	ed packet rate in 125MHz in two start of packet ate match against the ex- /-, by default enabled. ted packet rate +/- devia- f=+/-127 clocks. ation match against the by default enabled.			

1.12.	15 stream0_err_sta	t	Reg. 0xA024	40044								
	Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.											
bits name s/w h/w default description												
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet size not matching to configured. Sticky bit. Write '1' to clear.							
1	stream_err_pfif ofull	r/w1c	wo	0x0	Packet FIFO is full. Sticky bit. Write '1' to c	lear.						
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full. Sticky bit. Write '1' to cle	ear.						
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger than 512*4Bytes. Sticky biclear.	t. Write '1' to						
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller than 3*4Bytes. Sticky bit.	. Write '1' to clear.						
5	stream_err_notl ast	r/w1c	WO	0x0	No tlast after tvalid goes low(tvalid goes lo the packet). Sticky bit. Write '1' to clear.	w in the middle of						
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. 1' to clear.	Sticky bit. Write						
7	stream_err_watc hdog	r/w1c	WO	0x0	FSM not hitting IDLE for more than 20us. Sto clear.	Sticky bit. Write '1'						

1.12.1	6 stream0_err_exp	Reg.	0xA0240048							
Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w		descriptio	n					

15:	0 stream_err_exps	rw	na	0x0	Counting expected packet size errors. This counter satu-
	ize_cntr				rates at 0xFFFF and is cleared by writting zero.

1.12.	17 stream0_err_pfife	Reg.	0xA024004C							
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_pfif ofull_cntr	rw	na	0x0	• •	t FIFO full errors. This counter saturate cleared by writting zero.				

1.12.	18 stream0_err_bfife	Reg.	0xA0240050							
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_bfif ofull_cntr	rw	na	0x0		FIFO full errors. This counter saturates at eared by writting zero.				

1.12.	19 stream0_err_max	Reg.	0xA0240054							
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_maxs ize_cntr	rw	na	0x0	Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	20 stream0_err_min	Reg.	0xA0240058								
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.											
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_mins ize_cntr	rw	na	0x0	• •	minimum size errors. This counter satu- and is cleared by writting zero.					

1.12.	21 stream0_err_not	Reg.	0xA024005C								
Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.											
bits	name	s/w	h/w	default		description	า				
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF				

1.12.	22 stream0_err_mir	Reg.	0xA0240060						
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.									
bits	name	s/w	h/w	default		description	า		
15:0	stream_err_mini pg_cntr	rw	na	0x0	Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.	23 stream0_err_wat		Reg.	0xA0240064					
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.									
bits	name	s/w	h/w	default		description	n		
15:0	stream_err_watc rw na 0x0 Counting FSM watchdog errors. This counter saturates a 0xFFFF and is cleared by writting zero.								

### 0xA0240068 1.12.24 stream0\_exc\_exprate\_cntr\_stat Reg. Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation. bits h/w default description s/w name 0x0 Counting expected packet rate exceptions. The rate is mea-15:0 stream\_exc\_expr na rw sured in 125MHz clocks between two start of packet events, ate\_cntr and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero.

1.12.	1.12.25 stream0_exc_expratedeviate_cntr_stat 0xA024006C										
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.											
bits	name	s/w	h/w	default		description	n				
	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	26 stream0_rate_m	Reg.	0xA0240070						
Status register - Data stream packet rate. Measured in clocks.									
bits	name	s/w	h/w	default		description			
23:0	stream_rate_mea sured	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823				

1.12.	27 tpg1_packet_rate		Reg.	0xA0240134					
Control register - TPG Stream Packet rate									
bits	name	s/w	h/w	default	description				
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823				

1.12.	28 tpg1_packet_siz	e_clks	Reg.	0xA0240138						
Control register - TPG Stream Packet size										
bits name s/w h/w default description										
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64Bytes(4 cloc	pple on the AXI-Stream bus. stream number in the MSB				

1.12.	29 stream1_expsize	Reg.	0xA024013C						
Control register - Data stream expected packet size.									
bits	name	s/w	h/w	default	description				
31:0	stream1_expsize _dis	rw	ro	0x2C	Bits 15-0 - Data stream expected packet size in 4Byte increments (LSbit = 4Bytes).  Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.				

1.12.	30 stream1_exprat	Reg.	0xA0240140							
Control register - Data stream expected packet rate.										
bits	name	s/w		description						
31:0	stream1_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set E tion in 125MHz cl Bit 31 - set to 1 to	e distance betwee in clocks. o disable packet ra e with deviation + pata stream expect ocks. Default 0x7 o disable rate devi	ed packet rate in 125MHz in two start of packet ate match against the ex- /-, by default enabled. ited packet rate +/- devia- f=+/-127 clocks. ation match against the by default enabled.			

### 0xA0240144 1.12.31 stream1 err stat Reg. Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped. bits name s/w h/w default description 0 stream\_err\_exps r/w1c wo 0x0 Expected packet size not matching to configured. Sticky bit. Write '1' to clear. 1 stream\_err\_pfif r/w1c wo 0x0 Packet FIFO is full. Sticky bit. Write '1' to clear. 2 Buffer FIFO is full. Sticky bit. Write '1' to clear. stream err bfif r/w1c wo 0x0 ofull 3 Packet is larger than 512\*4Bytes. Sticky bit. Write '1' to stream\_err\_maxs r/w1c wo 0x0 clear. Packet is smaller than 3\*4Bytes. Sticky bit. Write '1' to clear. 4 0x0 stream\_err\_mins r/w1c wo ize 5 No tlast after tvalid goes low(tvalid goes low in the middle of r/w1c 0x0 stream\_err\_notl wo the packet). Sticky bit. Write '1' to clear. ast 6 r/w1c 0x0 Packets arrive with IPG less than 7 clocks. Sticky bit. Write stream\_err\_mini wo '1' to clear. FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' stream\_err\_watc r/w1c wo 0x0 hdog to clear.

1.12.	32 stream1_err_exp	Reg.	0xA0240148						
Status register - Data stream expected packet size error. The packet size doesn't match configured size.									
bits	name	s/w	h/w	default		description	١		
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.	33 stream1_err_pfife	Reg.	0xA024014C							
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits	name	s/w	h/w	default		description	٦			
15:0	stream_err_pfif ofull_cntr	rw	na	0x0	Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	34 stream1_err_bfife	Reg.	0xA0240150						
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.									
bits	name	s/w	h/w	default		description	า		
15:0	15:0 stream_err_bfif rw na 0x0 Counting Buffer FIFO full errors. This counter saturates at ofull_cntr 0xFFFF and is cleared by writting zero.								

1.12.35 stream1_err_maxsize_cntr_stat	Reg.	0xA0240154
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Statu	Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.								
bits	bits name s/w h/w default description								
15:0									

1.12.	36 stream1_err_min	Reg.	0xA0240158							
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	n			
15:0 stream_err_mins rw na 0x0 Counting packet minimum size errors. This counter satu-										

1.12.	37 stream1_err_notl	Reg.	0xA024015C							
	Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.									
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_notl ast_cntr	Counting no-tlast and is cleared by		ter saturates at 0xFFFF						

1.12.	38 stream1_err_min	Reg.	0xA0240160								
Statu	Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.										
bits	name	s/w	h/w	default		description	า				
15:0 stream_err_mini rw na 0x0 Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	39 stream1_err_wat	Reg.	0xA0240164							
Statu	Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.									
bits	name	s/w	h/w	default		description	١			
15:0 stream_err_watc rw na 0x0 Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero.										

1.12.	40 stream1_exc_exp	Reg.	0xA0240168								
	Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.										
bits	name	s/w	h/w	default		description	n				
15:0	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between the clocks between the contraction of the contraction o	eptions. The rate is mea- wo start of packet events, n expected. This counter I by writting zero.				

1.12.41 stream1_exc_expratedeviate_cntr_stat 0xA024016C										
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is n	nesured by subtra	riation exceptions. The acting two rate measure- cFFFF and is cleared by			

1.12.	42 stream1_rate_me	Reg.	0xA0240170							
Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default		description	n			
23:0	stream_rate_mea sured	rw	wo	0x0	Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823					

1.12.	43 tpg2_packet_rate	Reg.	0xA0240234							
Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default		descriptio	n			
23:0	tpg_packet_rate _clks	rw	ro	0x823			25MHz clock. For his value is 2083 clocks =			

1.12.	44 tpg2_packet_siz	ze_clks		Reg.	0xA0240238		
Contr	ol register - TPG Stream	Packet	size				
bits	name	s/w	h/w	default		des	scription
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64 register value of clock sample of 128bit(16Byte) we Each sample cor	Bytes(4 clo 0x40. The 16Bytes. Ea ide bus sai ntains a 4bi	ocks of 125MHz clock. Minimum ock samples x16Bytes each) = 4 LSBits count the Bytes in one ach clock period generates a mple on the AXI-Stream bus. It stream number in the MSB og value in the LSB 32bit.

1.12.45 stream2_expsize_dis_ctrl 0xA024023C										
Control register - Data stream expected packet size.										
bits	bits name s/w h/w default description									
31:0	stream2_expsize _dis	rw	ro	0x13	ments (LSbit = 4Byt	tes). icket match aga	acket size in 4Byte incr- inst the expected packet d.			

1.12.	46 stream2_exprate	e_dis_	Reg.	0xA0240240								
Contr	Control register - Data stream expected packet rate.											
bits	name	s/w	h/w	default		des	cription					
31:0	stream2_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set E tion in 125MHz cl Bit 31 - set to 1 to	e distance b in clocks. o disable pa e with devia data stream ocks. Defau o disable rat	expected packet rate in 125MHz between two start of packet cket rate match against the exation +/-, by default enabled.  expected packet rate +/- deviault 0x7f=+/-127 clocks.  the deviation match against the bon +/-, by default enabled.					

1.12.	47 stream2_err_sta	Reg.	0xA0240244							
Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.										
bits	name	s/w	h/w	default		descriptio	n			
bits 0	name stream_err_exps ize	s/w r/w1c	h/w wo	default 0x0	Expected packet write '1' to clear.		n g to configured. Sticky bit.			

	ofull				
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	WO	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	48 stream2_err_exp	Reg.	0xA0240248								
Statu	Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default		description	٦				
15:0 stream_err_exps rw na 0x0 Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	49 stream2_err_pfife	Reg.	0xA024024C								
Statu	Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits	name	s/w	h/w	default		description	า				
15:0 stream_err_pfif rw na 0x0 Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	50 stream2_err_bfif	Reg.	0xA0240250								
Statu	Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	n				
15:0 stream_err_bfif rw na 0x0 Counting Buffer FIFO full errors. This counter saturates at ofull_cntr 0xFFFF and is cleared by writting zero.											

1.12.	51 stream2_err_max	Reg.	0xA0240254								
Statu	Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	1				
15:0 stream_err_maxs rw na 0x0 Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	52 stream2_err_min	Reg.	0xA0240258								
Statu	Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	า				
15:0 stream_err_mins rw na 0x0 Counting packet minimum size errors. This counter satu- ize_cntr rates at 0xFFFF and is cleared by writting zero.											

1.12.	53 stream2_err_not	Reg.	0xA024025C								
	Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.										
bits	name	s/w	h/w	default		description	ı				
15:0	stream_err_notl ast_cntr	ter saturates at 0xFFFF									

1.12.	54 stream2_err_min	Reg.	0xA0240260									
Statu	Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.											
bits	name	s/w	h/w	default	descriptio	n						
15:0	15:0 stream_err_mini rw na 0x0 Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	55 stream2_err_wat	Reg.	0xA0240264							
Statu	Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.									
bits	name	s/w	h/w	default		description	n			
15:0 stream_err_watc rw na 0x0 Counting FSM watchdog errors. This counter saturates at hdog_cntr 0xFFFF and is cleared by writting zero.										

1.12.	56 stream2_exc_exp	Reg.	0xA0240268					
Status	s register - Data stream extion.	te doesn't match	configured including the					
bits	name	s/w	h/w	default		description		
	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between twithin the deviation	eptions. The rate is mea- wo start of packet events, n expected. This counter I by writting zero.	

1.12.	57 stream2_exc_exp	nt	Reg.	0xA024026C						
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.										
bits	name	s/w	h/w	default		description	n			
	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is n	nesured by subtra	riation exceptions. The acting two rate measure- kFFFF and is cleared by			

1.12.	58 stream2_rate_me	Reg.	0xA0240270								
Status register - Data stream packet rate. Measured in clocks.											
bits	name	s/w	h/w	default		description	n				
23:0	stream_rate_mea sured	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured aftevery packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823						

1.12.	59 tpg3_packet_rate	Reg.	0xA0240334								
Contr	Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default		description	ı				
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823						

1.12.60 t	pg3_packet_s	Reg.	0xA0240338					
Control register - TPG Stream Packet size								
bits	name	s/w h/w		descripti	on			

15:0	tpg_packet_size _clks	rw	ro	0x40	Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit.
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1.12.0	61 stream3_expsize	Reg.		0xA024033C							
Contr	Control register - Data stream expected packet size.										
bits	name	s/w	h/w	default	ult description						
31:0	stream3_expsize _dis	rw	ro	0xD	Bits 15-0 - Data stream expected packet size in 4Byte incoments (LSbit = 4Bytes).  Bit 31 - Diasable packet match against the expected packets, by default matching is enabled.						

1.12.	62 stream3_exprate	I	Reg.	0xA0240340						
Control register - Data stream expected packet rate.										
bits	name	s/w	h/w	default		description	า			
31:0	stream3_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured i Bit 30 - set to 1 to pected packet rate Bits 27-16 - Set Dation in 125MHz clo Bit 31 - set to 1 to	distance between clocks.  disable packet rate with deviation + cata stream expectocks. Default 0x71 disable rate deviation to the cata stream expectors.	ed packet rate in 125MHz in two start of packet ate match against the ex- /-, by default enabled. eted packet rate +/- devia- f=+/-127 clocks. ation match against the by default enabled.			

#### 0xA0240344 1.12.63 stream3\_err\_stat Reg. Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped. bits h/w default s/w description name 0 Expected packet size not matching to configured. Sticky bit. stream\_err\_exps r/w1c wo 0x0 Write '1' to clear. 1 0x0 Packet FIFO is full. Sticky bit. Write '1' to clear. stream\_err\_pfif r/w1c wo ofull 2 Buffer FIFO is full. Sticky bit. Write '1' to clear. stream\_err\_bfif r/w1c 0x0 wo ofull 3 Packet is larger than 512\*4Bytes. Sticky bit. Write '1' to r/w1c 0x0 stream\_err\_maxs wo ize 4 Packet is smaller than 3\*4Bytes. Sticky bit. Write '1' to clear. stream\_err\_mins r/w1c wo 0x0 ize 5 r/w1c 0x0 No tlast after tvalid goes low(tvalid goes low in the middle of stream\_err\_notl wo the packet). Sticky bit. Write '1' to clear. ast 6 stream\_err\_mini r/w1c 0x0 Packets arrive with IPG less than 7 clocks. Sticky bit. Write wo '1' to clear. pg stream\_err\_watc r/w1c wo 0x0 FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' hdog to clear.

1.12.	64 stream3_err_exp	Reg.	0xA0240348								
Status register - Data stream expected packet size error. The packet size doesn't match configured size.											
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	65 stream3_err_pfif	Reg.	0xA024034C								
Statu	Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits	name	s/w	h/w	default		description	า				
15:0	stream_err_pfif ofull_cntr	rw	na	0x0	Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	66 stream3_err_bfife	Reg.	0xA0240350									
Statu	Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.											
bits	name	s/w	h/w	default		description	n					
15:0	stream_err_bfif ofull cntr	rw	na	0x0	•	Buffer FIFO full errors. This counter saturates a and is cleared by writting zero.						

1.12.	67 stream3_err_max	Reg.	0xA0240354								
Statu	Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	า				
15:0	stream_err_maxs ize_cntr	rw	na	0x0	Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	68 stream3_err_min	Reg.	0xA0240358						
Statu	s register - Data stream pa	er than 3*4Bytes.							
bits	name	s/w	h/w	default		description	n		
15:0	stream_err_mins ize_cntr	rw	na	0x0		g packet minimum size errors. This counter satu- 0xFFFF and is cleared by writting zero.			

1.12.	69 stream3_err_not	Reg.	0xA024035C				
	s register - Data stream p acket.	oes low error. The	tvalid should not g	go low in the middle of			
bits	name	s/w	h/w	default		description	ı
15:0	stream_err_notl ast_cntr	m_err_notl rw na 0x0 Counting no-tlast errors. This counter saturates at 0					

1.12.	70 stream3_err_min	Reg.	0xA0240360						
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.									
bits	name	s/w	h/w	default	description				
15:0	stream_err_mini pg_cntr	rw	na	0x0		counting minimum IPG errors. This counter saturates at xFFFF and is cleared by writting zero.			

1.12.	71 stream3_err_wat	Reg.	0xA0240364						
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.									
bits	name	s/w	h/w	default	description				
15:0	stream_err_watc hdog_cntr	rw	na	0x0	Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.72	stream3_exc_	Reg.	0xA0240368					
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.								
bits	name	s/w	h/w	default		descrip	tion	

15:0	stream_exc_expr	rw	na	0x0	Counting expected packet rate exceptions. The rate is mea-
	ate_cntr				sured in 125MHz clocks between two start of packet events,
					and it should be within the deviation expected. This counter
					saturates at 0xFFFF and is cleared by writting zero.

1.12.	73 stream3_exc_exp	orated	it	Reg.	0xA024036C					
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.										
bits	name	s/w	h/w	default	description					
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is m	esured by subtra	iation exceptions. The acting two rate measure- FFFF and is cleared by			

1.12.	74 stream3_rate_me		Reg.	0xA0240370						
Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default		descriptio	n			
23:0	stream_rate_mea sured	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured af every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823					

1.12.	75 tpg4_packet_rate	e_clks		Reg.	0xA0240434					
Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default		description				
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823					

1.12.	76 tpg4_packet_size	e_clks		Reg.	0xA0240438					
Control register - TPG Stream Packet size										
bits	bits name s/w h/w default description									
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64 register value of clock sample of 1 128bit(16Byte) w Each sample cor	Bytes(4 clock sam 0x40. The 4 LSBit 6Bytes. Each clor ide bus sample or tains a 4bit strear	125MHz clock. Minimum ples x16Bytes each) = s count the Bytes in one ck period generates an the AXI-Stream bus. In number in the MSB in the LSB 32bit.			

1.12.	77 stream4_expsize	_dis_		Reg.	0xA024043C				
Control register - Data stream expected packet size.									
bits	name	s/w	h/w	default	description				
31:0	stream4_expsize _dis	rw	ro	0xC	Bits 15-0 - Data stream expected packet size in 4Byte incrments (LSbit = 4Bytes).  Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.				

1.12.	78 stream4_exprate	Reg.	0xA0240440								
Contr	Control register - Data stream expected packet rate.										
bits	name	s/w	h/w	default	description						
31:0	stream4_exprate	rw	ro	0x7F0040							

_dis	Bits 15-0 - Set Data stream expected packet rate in 125MHz clocks. This is the distance between two start of packet events measured in clocks.
	Bit 30 - set to 1 to disable packet rate match against the expected packet rate with deviation +/-, by default enabled.
	Bits 27-16 - Set Data stream expected packet rate +/- devia-
	tion in 125MHz clocks. Default 0x7f=+/-127 clocks.
	Bit 31 - set to 1 to disable rate deviation match against the
	expected packet rate deviation +/-, by default enabled.

1.12.	79 stream4_err_s	tat				Reg.	0xA0240444		
	is register - Data strear Any of these events wil						ld be all '0' in normal opera- ped.		
bits	name	s/w	h/w	default		descr	iption		
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet size not matching to configured. Sticky b Write '1' to clear.				
1	stream_err_pfif ofull	r/w1c	wo	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.				
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.				
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger the clear.	nan 512*4Byt	tes. Sticky bit. Write '1' to		
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller	than 3*4Byte	es. Sticky bit. Write '1' to clea		
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvali the packet). Stick	•	valid goes low in the middle ' to clear.		
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive wit	th IPG less th	nan 7 clocks. Sticky bit. Write		
7	stream_err_watc hdog	r/w1c	wo	0x0	FSM not hitting ID to clear.	DLE for more	than 20us. Sticky bit. Write		

1.12.	80 stream4_err_exp	Reg.	0xA0240448							
Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default		description				
15:0	stream_err_exps ize_cntr	rw	na	0x0	• .	ed packet size errors. This counter satu- and is cleared by writting zero.				

1.12.	81 stream4_err_pfife	ofull_		Reg.	0xA024044C					
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_pfif ofull_cntr	rw	na	0x0	Counting packet FIFO full errors. This counter saturates a 0xFFFF and is cleared by writting zero.					

1.12.	82 stream4_err_bfife	ofull_		Reg.	0xA0240450					
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_bfif ofull_cntr	rw	na	0x0		FIFO full errors. This counter saturates at leared by writting zero.				

1.12.	83 stream4_err_max	Reg.	0xA0240454						
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.									
bits	name	s/w	h/w	default	description				
15:0	stream_err_maxs ize_cntr	rw	na	0x0	Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.	84 stream4_err_min	Reg.	0xA0240458							
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default	description					
15:0	stream_err_mins ize_cntr	rw	na	0x0	Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	85 stream4_err_n	Reg.	0xA024045C							
Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF			

1.12.	86 stream4_err_min	Reg.	0xA0240460							
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_mini pg_cntr	rw	na	0x0	Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	87 stream4_err_wat	Reg.	0xA0240464						
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.									
bits	name	s/w	h/w	default		description	า		
15:0	stream_err_watc hdog_cntr	rw	na	0x0		atchdog errors. This counter saturates at leared by writting zero.			

1.12.	88 stream4_exc_exp	Reg.	0xA0240468						
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.									
bits	name	s/w	h/w	default		description	n		
15:0	stream_exc_expr ate_cntr	rw	na	0x0	Counting expected packet rate exceptions. The rate is me sured in 125MHz clocks between two start of packet even and it should be within the deviation expected. This counters saturates at 0xFFFF and is cleared by writting zero.				

1.12.	89 stream4_exc_exp	Reg.	0xA024046C							
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.										
bits	name	s/w	h/w	default		description				
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.90 stream4_rate_measured_stat 0xA0240470										
Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default	fault description					

23:0	stream_rate_mea	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured after
	sured				every packet. For 60kHz(16.7us period) packet rate this val-
					ue should be around 2083 clocks = 0x823

1.12.9	91 tpg5_packet_rate	Reg.	0xA0240534							
Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default	default description					
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823					

1.12.	92 tpg5_packet_size	e_clks	0xA0240538						
Control register - TPG Stream Packet size									
bits	name	s/w	h/w	default	description				
15:0	tpg_packet_size _clks	rw	ro	0x40	Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit.				

1.12.	93 stream5_expsiz	e_dis_	Reg.	0xA024053C					
Control register - Data stream expected packet size.									
bits	name	s/w	h/w	default	description				
31:0	stream5_expsize _dis	rw	ro	0x7A	Bits 15-0 - Data stream expected packet size in 4Byte ments (LSbit = 4Bytes).  Bit 31 - Diasable packet match against the expected p size, by default matching is enabled.				

1.12.	94 stream5_exprate	e_dis_	ctrl		Reg.	0xA0240540				
Control register - Data stream expected packet rate.										
bits	name	s/w		des	scription					
31:0	stream5_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set E tion in 125MHz cl Bit 31 - set to 1 to	e distance to in clocks. In clocks. In disable particular disable particular disable rapid disable r	expected packet rate in 125MHz petween two start of packet packet rate match against the exation +/-, by default enabled. In expected packet rate +/- deviault 0x7f=+/-127 clocks. It deviation match against the ion +/-, by default enabled.			

1.12.	95 stream5_err_sta	Reg.	0xA0240544								
	Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.										
bits	name	s/w	h/w	default		description	n				
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet s Write '1' to clear.	size not matching	to configured. Sticky bit.				
1	stream_err_pfif ofull	r/w1c	wo	0x0	Packet FIFO is ful	I. Sticky bit. Write	e '1' to clear.				
2	stream_err_bfif ofull	r/w1c	WO	0x0	Buffer FIFO is full	. Sticky bit. Write	'1' to clear.				

3	stream_err_maxs ize	r/w1c	WO	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	WO	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	WO	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	wo	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	96 stream5_err_exp	Reg.	0xA0240548							
Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_exps ize cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	97 stream5_err_pfife	Reg.	0xA024054C						
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.									
bits	name	s/w	h/w	default		description	า		
15:0	stream_err_pfif ofull_cntr	rw	na	0x0		FIFO full errors. This counter saturates a leared by writting zero.			

1.12.	98 stream5_err_bfife	Reg.	0xA0240550							
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_bfif ofull_cntr	rw	na	0x0		FIFO full errors. This counter saturates at cleared by writting zero.				

1.12.	99 stream5_err_max	Reg.	0xA0240554							
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_maxs ize_cntr	rw	na	0x0	Ų i	ng packet maximum size errors. This counter satutoxFFFF and is cleared by writting zero.				

1.12.	100 stream5_err_r	Reg.	0xA0240558							
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_mins ize_cntr	rw	na	0x0	Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	101 stream5_err_no	tlast_		Reg.	0xA024055C					
	Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.									
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF			

1.12.102 stream5_err_minipg_cntr_stat	Reg.	0xA0240560

Statu	Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.									
bits	name	s/w	h/w	default	description					
15:0	stream_err_mini pg_cntr	rw	na	0x0	Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	103 stream5_err_wa	Reg.	0xA0240564							
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_watc hdog_cntr	rw	na	0x0	•	atchdog errors. This counter saturates at eared by writting zero.				

1.12.	104 stream5_exc_ex	Reg.	0xA0240568						
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.									
bits	name	s/w	h/w	default		description	n		
	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between to vithin the deviation	eptions. The rate is mea- wo start of packet events, n expected. This counter I by writting zero.		

1.12.	105 stream5_exc_ex	tat	Reg.	0xA024056C				
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.								
bits	name	s/w	h/w	default		description	า	
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is m	nesured by subtra	iation exceptions. The acting two rate measure- FFFF and is cleared by	

1.12.	106 stream5_rate_m	Reg.	0xA0240570						
Status register - Data stream packet rate. Measured in clocks.									
bits	name	s/w	h/w	default	description				
23:0	stream_rate_mea sured	rw	WO	0x0		60kHz(16.7us pe	Iz clocks. Measured after riod) packet rate this val- 0x823		

1.12.	107 tpg6_packet_rat	Reg.	0xA0240634						
Control register - TPG Stream Packet rate									
bits	name	s/w	h/w	default	description				
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masu 60kHz(16.7us per 0x823		25MHz clock. For his value is 2083 clocks =		

1.12.	108 tpg6_packet_si	ze_cll	ks_ct	0xA0240638				
Control register - TPG Stream Packet size								
bits	name	s/w	h/w	default	description			
15:0	tpg_packet_size _clks	rw	ro	0x40	Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus.			

Each sample contains a 4bit stream number in the MSB
32bit, and 16bit incrementing value in the LSB 32bit.

1.12.	109 stream6_expsiz		Reg.	0xA024063C					
Control register - Data stream expected packet size.									
bits	name	s/w	h/w	default		description	ı		
31:0	stream6_expsize _dis	rw	ro	0xBD	ments (LSbit = 4B)	ytes). acket match aga	acket size in 4Byte incr- inst the expected packet d.		

1.12.	110 stream6_exprat	Reg.	0xA0240640							
Contr	Control register - Data stream expected packet rate.									
bits	name	s/w	h/w	default		description	n			
31:0	stream6_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set D tion in 125MHz cl Bit 31 - set to 1 to	e distance between in clocks. In disable packet rate with deviation + lata stream expectocks. Default 0x7 in disable rate devi	ed packet rate in 125MHz n two start of packet ate match against the ex- /-, by default enabled. cted packet rate +/- devia- f=+/-127 clocks. ation match against the by default enabled.			

1.12.	111 stream6_err_	stat	0xA0240644		
	•				e of error, write 1 to clear. Should be all '0' in normal opera- one packet or more will be dropped.
bits	name	s/w	h/w	default	description
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet size not matching to configured. Sticky bit. Write '1' to clear.
1	stream_err_pfif ofull	r/w1c	wo	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	WO	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	112 stream6_err_ex	Reg.	0xA0240648						
Status register - Data stream expected packet size error. The packet size doesn't match configured size.									
bits	name	s/w	h/w	default		description	١		
15:0	stream_err_exps ize cntr	rw	na	0x0	Counting expecterates at 0xFFFF a	•	ors. This counter satu-		

1.12.113 stream6_err_pfifofull_cntr_stat 0xA024064C									
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.									
bits	name	s/w	h/w	default		descriptio	n		

15:0	stream_err_pfif	rw	na	0x0	Counting packet FIFO full errors. This counter saturates at
	ofull_cntr				0xFFFF and is cleared by writting zero.

1.12.	114 stream6_err_bfi	Reg.	0xA0240650							
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	า			
15:0 stream_err_bfif rw na 0x0 Counting Buffer FIFO full errors. This counter saturates at ofull_cntr 0xFFFF and is cleared by writting zero.										

1.12.	115 stream6_err_ma	Reg.	0xA0240654								
Statu	Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	า				
15:0	15:0 stream_err_maxs rw na 0x0 Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.										

1.12.	116 stream6_err_mi	Reg.	0xA0240658								
Statu	Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	n				
15:0 stream_err_mins rw na 0x0 Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	117 stream6_err_no	Reg.	0xA024065C							
Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.										
bits	name	s/w	h/w	default		description	า			
15:0 stream_err_notl rw na 0x0 Counting no-tlast errors. This counter saturates at 0xFFFF and is cleared by writting zero.										

1.12.	118 stream6_err_mi	Reg.	0xA0240660								
Statu	Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.										
bits	name	s/w	h/w	default		description	า				
15:0	15:0 stream_err_mini rw na 0x0 Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.										

1.12.	119 stream6_err_w	Reg.	0xA0240664								
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.											
bits	name	s/w	h/w	default		description	٦				
15:0	15:0 stream_err_watc rw na 0x0 Counting FSM watchdog errors. This counter saturates at hdog_cntr 0xFFFF and is cleared by writting zero.										

1.12.	120 stream6_exc_ex	Reg.	0xA0240668						
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.									
bits	name	s/w	h/w	default		description	า		
15:0	stream_exc_expr ate_cntr	rw	na	0x0	Counting expected packet rate exceptions. The rate is a sured in 125MHz clocks between two start of packet evand it should be within the deviation expected. This cousaturates at 0xFFFF and is cleared by writting zero.				

1.12.	121 stream6_exc_ex	Reg.	0xA024066C							
	Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.									
bits	name	s/w	h/w	default		description	า			
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is n	nesured by subtra	iation exceptions. The acting two rate measure- FFFF and is cleared by			

1.12.	122 stream6_rate_m	Reg.	0xA0240670							
Statu	s register - Data stream pa									
bits	name	s/w	h/w	default		description				
23:0	stream_rate_mea sured	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured aft every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823					

1.12.	123 tpg7_packet_rat	Reg.	0xA0240734								
Contr	Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default		description					
23:0	tpg_packet_rate _clks	packet_rate rw ro 0x823 Packet rate masured in clocks of 125MHz clock. For									

1.12.	124 tpg7_packet_si	Reg.	0xA0240738								
Control register - TPG Stream Packet size											
bits name s/w h/w default description											
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64E register value of 0 clock sample of 1 128bit(16Byte) wi Each sample con	Bytes(4 clood) 0x40. The 4 6Bytes. Ea de bus san tains a 4bit	cks of 125MHz clock. Minimum ck samples x16Bytes each) = LSBits count the Bytes in one ch clock period generates a nple on the AXI-Stream bus. stream number in the MSB g value in the LSB 32bit.				

1.12.	125 stream7_expsiz	Reg.	0xA024073C						
Control register - Data stream expected packet size.									
bits	n								
31:0	stream7_expsize _dis	rw	ro	0x1D	Bits 15-0 - Data stream expected packet size in 4Byte incr ments (LSbit = 4Bytes). Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled.				

1.12.	126 stream7_expi	rate_dis	_ctrl		Reg.	0xA0240740
Conti	rol register - Data strea	m expecte	ed pacl	ket rate.		
bits	name	s/w	h/w	default	desc	ription
31:0	stream7_exprate _dis	rw	ro	0x7F0040	clocks. This is the distance be events measured in clocks.	cket rate match against the ex-

Bits 27-16 - Set Data stream expected packet rate +/- devia-
tion in 125MHz clocks. Default 0x7f=+/-127 clocks.
Bit 31 - set to 1 to disable rate deviation match against the
expected packet rate deviation +/-, by default enabled.

# 1.12.127 stream7\_err\_stat OxA0240744 Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

	,	00		•	
bits	name	s/w	h/w	default	description
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet size not matching to configured. Sticky bit. Write '1' to clear.
1	stream_err_pfif ofull	r/w1c	wo	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	WO	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	128 stream7_err_ex	Reg.	0xA0240748					
Status register - Data stream expected packet size error. The packet size doesn't match configured size.								
bits	name	s/w	h/w	default		description	٦	
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.			

1.12.	129 stream7_err_pfi	Reg.	0xA024074C				
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.							
bits	name	s/w	h/w	default		description	n
15:0 stream_err_pfif rw na 0x0 Counting packet FIFO full errors. This counter satura ofull_cntr 0xFFFF and is cleared by writting zero.							

1.12.	1.12.130 stream7_err_bfifofull_cntr_stat 0xA0240750								
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.									
bits	name	s/w	h/w	default		description	٦		
15:0	I I								

1.12.	131 stream7_err_ma	Reg.	0xA0240754				
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.							
bits	name	s/w	h/w	default		description	١
15:0	·						

1.12.132 stream7_err_minsize_cntr_stat	0xA0240758	
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Status	Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.						
bits	name	s/w	h/w	default	description		
15:0	stream_err_mins	rw	na	0x0	Counting packet minimum size errors. This counter satu-		
	ize_cntr				rates at 0xFFFF and is cleared by writting zero.		

1.12.	133 stream7_err_r	Reg.	0xA024075C				
Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.							
bits	name	s/w	h/w	default		description	1
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF

1.12.	134 stream7_err_mi	Reg.	0xA0240760						
Statu	s register - Data stream m	between packets	is less than 7 clocks.						
bits	name	s/w	h/w	default		description	١		
15:0	stream_err_mini	rw	na	0x0	Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.	1.12.135 stream7_err_watchdog_cntr_stat 0xA0240764								
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.									
bits	name	s/w	h/w	default		description	า		
15:0	stream_err_watc	rw	na	0x0	Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.	136 stream7_exc_ex	Reg.	0xA0240768						
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.									
bits	name	s/w	h/w	default	description				
	stream_exc_expr ate_cntr	rw	na	0x0	Counting expected packet rate exceptions. The rate sured in 125MHz clocks between two start of packe and it should be within the deviation expected. This saturates at 0xFFFF and is cleared by writting zero.				

1.12.	137 stream7_exc_ex	tat	Reg.	0xA024076C					
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.									
bits	name	s/w	h/w	default	description				
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. Trate deviation is mesured by subtracting two rate meanments. This counter saturates at 0xFFFF and is cleared writting zero.				

1.12.	138 stream7_rate_r	Reg.	0xA0240770							
Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default		description				
23:0	stream_rate_mea sured	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured a every packet. For 60kHz(16.7us period) packet rate this ue should be around 2083 clocks = 0x823					

1.12.	139 tpg8_packet_rate	Reg.	0xA0240834							
Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default	description					
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823					

1.12.	140 tpg8_packet_siz	ze_cll	Reg.	0xA0240838						
Contr	Control register - TPG Stream Packet size									
bits	name	s/w	h/w	default	desc	ription				
15:0	tpg_packet_size _clks	rw	ro	0x40	Packet size measured in cloc packet size is 64Bytes(4 clocl register value of 0x40. The 4 clock sample of 16Bytes. Each 128bit(16Byte) wide bus same Each sample contains a 4bit of 32bit, and 16bit incrementing	LSBits count the Bytes in one the clock period generates a ple on the AXI-Stream bus.				

1.12.	141 stream8_expsiz	Reg.	0xA024083C						
Control register - Data stream expected packet size.									
bits	name	s/w	h/w	default	description				
31:0	stream8_expsize _dis	rw	ro	0x110	Bits 15-0 - Data stream expected packet size in 4Byte inc ments (LSbit = 4Bytes). Bit 31 - Diasable packet match against the expected pack size, by default matching is enabled.				

1.12.	142 stream8_expr	ate_dis		Reg.	0xA0240840					
Control register - Data stream expected packet rate.										
bits	name	s/w	h/w	default		des	scription			
31:0	stream8_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet range Bits 27-16 - Set tion in 125MHz of Bit 31 - set to 1 to 1 to 1 to 1 to 1 to 1 to 1 to	e distance I d in clocks. o disable pa te with devi Data stream clocks. Defa o disable ra	expected packet rate in 125MHz between two start of packet acket rate match against the exiation +/-, by default enabled. In expected packet rate +/- deviault 0x7f=+/-127 clocks. In the deviation match against the ion +/-, by default enabled.			

1.12.	143 stream8_err_	stat				Reg.	0xA0240844				
Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.											
bits	name	s/w	h/w	default		description	า				
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet Write '1' to clear.	size not matching	to configured. Sticky bit.				
1	stream_err_pfif ofull	r/w1c	WO	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.						
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full	. Sticky bit. Write	'1' to clear.				
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger the clear.	nan 512*4Bytes. S	Sticky bit. Write '1' to				
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller	than 3*4Bytes. St	ticky bit. Write '1' to clear.				
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvali the packet). Stick	•	goes low in the middle of lear.				

6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	wo	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	144 stream8_err_ex	Reg.	0xA0240848							
Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.145 stream8_err_pfifofull_cntr_stat 0xA024084C									
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.									
bits	name	s/w	h/w	default		description	n		
15:0	stream_err_pfif ofull_cntr	rw	na	0x0	• •	ng packet FIFO full errors. This counter saturates a F and is cleared by writting zero.			

1.12.	146 stream8_err_bfi	Reg.	0xA0240850						
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.									
bits	name	s/w	h/w	default	description				
15:0	stream_err_bfif ofull_cntr	rw	na	0x0	Counting Buffer FIFO full errors. This counter saturates a 0xFFFF and is cleared by writting zero.				

1.12.	147 stream8_err_ma		Reg.	0xA0240854							
Statu	Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	١				
15:0	15:0 stream_err_maxs rw na 0x0 Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.										

1.12.	148 stream8_err_m	Reg.	0xA0240858								
Statu	Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	n				
15:0 stream_err_mins rw na 0x0 Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	149 stream8_err_no	Reg.	0xA024085C								
	Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.										
bits	name	s/w	h/w	default		description	٦				
15:0	stream_err_notl ast_cntr	errors. This count writting zero.	ter saturates at 0xFFFF								

1.12.	150 stream8_err_mi	Reg.	0xA0240860									
Statu	Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.											
bits	name	s/w	h/w	default		description	٦					
15:0 stream_err_mini rw na 0x0 Counting minimum IPG errors. This counter saturates at pg_cntr 0xFFFF and is cleared by writting zero.												

1.12.	151 stream8_err_wa		Reg.	0xA0240864						
Statu	Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.									
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_watc hdog_cntr	Counting FSM was 0xFFFF and is cle		is counter saturates at zero.						

1.12.	152 stream8_exc_ex	Reg.	0xA0240868						
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.									
bits	name	s/w	h/w	default		description	٦		
15:0	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between twithin the deviation	eptions. The rate is mea- wo start of packet events, n expected. This counter by writting zero.		

1.12.	153 stream8_exc_ex	at	Reg.	0xA024086C					
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.									
bits	name	s/w	h/w	default		description	n		
	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is m	nesured by subtra	iation exceptions. The acting two rate measure- FFFF and is cleared by		

1.12.	154 stream8_rate_m	Reg.	0xA0240870								
Statu	Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default		description	n				
23:0	stream_rate_mea sured	rw	wo	0x0		60kHz(16.7us pe	Hz clocks. Measured after priod) packet rate this value 0x823				

1.12.	155 tpg9_packet_ra	Reg.	0xA0240934						
Control register - TPG Stream Packet rate									
bits	name	s/w	h/w	default		description	n		
23:0	tpg_packet_rate _clks	Packet rate masu 60kHz(16.7us per 0x823		25MHz clock. For his value is 2083 clocks =					

1.12.	156 tpg9_packet_s	size_clk		Reg.	0xA0240938						
Control register - TPG Stream Packet size											
bits name s/w h/w default description											
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 641 register value of 0 clock sample of 1 128bit(16Byte) w Each sample con	Bytes(4 clock 0x40. The 4 l 6Bytes. Eac ide bus samp tains a 4bit s	ks of 125MHz clock. Minimum c samples x16Bytes each) = LSBits count the Bytes in one h clock period generates a ble on the AXI-Stream bus. stream number in the MSB value in the LSB 32bit.				

1.12.	157 stream9_expsiz	Reg.	0xA024093C							
Control register - Data stream expected packet size.										
bits	bits name s/w h/w default description									
31:0	stream9_expsize _dis	rw	ro	0x34	ments (LSbit = 4B	Bytes). Dacket match aga	acket size in 4Byte incr- ninst the expected packet d.			

1.12.	158 stream9_expr	ate_dis		Reg.	0xA0240940						
Control register - Data stream expected packet rate.											
bits	name	scription									
31:0	stream9_exprate _dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rai Bits 27-16 - Set I tion in 125MHz c Bit 31 - set to 1 to	e distance to a distance to disable parties with devi- Data stream locks. Defaronce to disable parties disable parties disable rapido disable	expected packet rate in 125MHz between two start of packet between two start of packet acket rate match against the exation +/-, by default enabled. In expected packet rate +/- deviault 0x7f=+/-127 clocks. It deviation match against the on +/-, by default enabled.				

#### 1.12.159 stream9\_err\_stat Reg. 0xA0240944 Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped. bits default s/w h/w description name 0x0 Expected packet size not matching to configured. Sticky bit. 0 r/w1c stream\_err\_exps wo Write '1' to clear. ize Packet FIFO is full. Sticky bit. Write '1' to clear. 1 stream\_err\_pfif r/w1c 0x0 wo ofull 2 Buffer FIFO is full. Sticky bit. Write '1' to clear. stream\_err\_bfif r/w1c 0x0 wo ofull 3 0x0 Packet is larger than 512\*4Bytes. Sticky bit. Write '1' to stream\_err\_maxs r/w1c wo ize stream\_err\_mins r/w1c 0x0 Packet is smaller than 3\*4Bytes. Sticky bit. Write '1' to clear. wo 5 No tlast after tvalid goes low(tvalid goes low in the middle of stream\_err\_notl r/w1c wo 0x0 the packet). Sticky bit. Write '1' to clear. 6 Packets arrive with IPG less than 7 clocks. Sticky bit. Write stream\_err\_mini r/w1c wo 0x0 '1' to clear. 7 FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' stream\_err\_watc r/w1c 0x0 wo hdog to clear.

1.12.	1.12.160 stream9_err_expsize_cntr_stat 0xA0240948										
Status register - Data stream expected packet size error. The packet size doesn't match configured size.											
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	161 stream9_err_pf	Reg.	0xA024094C							
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_pfif ofull_cntr	rw	na	0x0		t FIFO full errors. This counter saturates at cleared by writting zero.				

1.12.	162 stream9_err_bfi	Reg.	0xA0240950							
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	n			
15:0	ream_err_bfif rw na 0x0 Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.									

1.12.	163 stream9_err_ma	Reg.	0xA0240954							
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	٦			
15:0	stream_err_maxs rw na 0x0 Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.									

1.12.	164 stream9_err_mi	Reg.	0xA0240958							
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	า			
15:0 stream_err_mins rw na 0x0 Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.										

1.12.	165 stream9_err_no	Reg.	0xA024095C							
Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_notl ast_cntr	rrors. This counter saturates at 0xFFFF ritting zero.								

1.12.	166 stream9_err_mi	Reg.	0xA0240960							
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.										
bits	name	s/w	h/w	default		description	٦			
15:0	stream_err_mini pg_cntr	rw	na	0x0	Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	1.12.167 stream9_err_watchdog_cntr_stat 0xA0240964										
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.											
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_watc hdog_cntr	rw	na	0x0		ng FSM watchdog errors. This counter saturates at and is cleared by writting zero.					

1.12.	168 stream9_exc_ex	Reg.	0xA0240968							
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.										
bits	name	s/w	h/w	default		descriptio	n			
15:0	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between to vithin the deviation	eptions. The rate is mea- wo start of packet events, n expected. This counter d by writting zero.			

1.12.169 stream9_exc_expratedeviate_cntr_stat	Reg.	0xA024096C
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Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

bits	name	s/w	h/w	default	description
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero.

1.12.	170 stream9_rate_m	Reg.	0xA0240970							
Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default		description	n			
23:0	stream_rate_mea sured	rw	wo	0x0	Measures the packet rate in 125MHz clocks. Measured aft every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823					

1.12.	171 tpg10_packet_ra	Reg.	0xA0240A34							
Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default		descriptio	n			
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823					

1.12.	172 tpg10_packet	_size_c		Reg.	0xA0240A38		
Conti	rol register - TPG Strea	m Packet	size				
bits	name	s/w	h/w	default		de	scription
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64 register value of clock sample of 128bit(16Byte) we Each sample con	Bytes(4 clo 0x40. The 16Bytes. Ea ride bus san ntains a 4bi	ocks of 125MHz clock. Minimum ock samples x16Bytes each) = 4 LSBits count the Bytes in one ach clock period generates a mple on the AXI-Stream bus. it stream number in the MSB ag value in the LSB 32bit.

1.12.	173 stream10_expsi	Reg.	0xA0240A3C								
Contr	Control register - Data stream expected packet size.										
bits	name s/w h/w default description										
31:0	stream10_expsiz e_dis	rw	ro	0x83	Bits 15-0 - Data stream expected packet size in 4Byte inc ments (LSbit = 4Bytes).  Bit 31 - Diasable packet match against the expected pack size, by default matching is enabled.						

1.12.	174 stream10_exp	rate_di	s_ctr	1		Reg.	0xA0240A40					
Control register - Data stream expected packet rate.												
bits name s/w h/w default description												
31:0	stream10_exprat e_dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set I tion in 125MHz c Bit 31 - set to 1 to	e distance be I in clocks. In clocks. In disable pac te with deviat Data stream of locks. Defaul In disable rate	expected packet rate in 125MHz between two start of packet externate match against the extion +/-, by default enabled. expected packet rate +/- deviate 0x7f=+/-127 clocks. e deviation match against the n +/-, by default enabled.					

## 1.12.175 stream10\_err\_stat

Reg.

0xA0240A44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

	•	00		•	• • • • • • • • • • • • • • • • • • • •
bits	name	s/w	h/w	default	description
0	stream_err_exps ize	r/w1c	WO	0x0	Expected packet size not matching to configured. Sticky bit. Write '1' to clear.
1	stream_err_pfif ofull	r/w1c	WO	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.
2	stream_err_bfif ofull	r/w1c	WO	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.
3	stream_err_maxs ize	r/w1c	WO	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	WO	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	wo	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

#### 0xA0240A48 1.12.176 stream10\_err\_expsize\_cntr\_stat Status register - Data stream expected packet size error. The packet size doesn't match configured size. h/w bits default description name s/w Counting expected packet size errors. This counter satu-15:0 stream\_err\_exps na 0x0 rw ize\_cntr rates at 0xFFFF and is cleared by writting zero.

1.12.	177 stream10_err_p	Reg.	0xA0240A4C								
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.											
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_pfif ofull_cntr	rw	na	0x0	Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	178 stream10_err_b	Reg.	0xA0240A50								
Statu	Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	٦				
15:0 stream_err_bfif rw na 0x0 Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	179 stream10_err_m	Reg.	0xA0240A54								
Statu	Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	n				
15:0 stream_err_maxs rw na 0x0 Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.											

1.12.	1.12.180 stream10_err_minsize_cntr_stat 0xA0240A58											
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.												
bits	name	s/w	h/w	default		description	٦					
15:0 stream_err_mins rw na 0x0 Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.												

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and is cleared by writting zero.

1.12.	182 stream10_err_m	Reg.	0xA0240A60								
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.											
bits	name	s/w	h/w	default		description	า				
15:0 stream_err_mini rw na 0x0 Counting minimum IPG errors. This counter saturates at pg_cntr 0xFFFF and is cleared by writting zero.											

1.12.	183 stream10_err_w	Reg.	0xA0240A64									
Statu	Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.											
bits	name	s/w	h/w	default		description	ı					
15:0 stream_err_watc rw na 0x0 Counting FSM watchdog errors. This counter saturates at hdog_cntr 0xFFFF and is cleared by writting zero.												

1.12.	184 stream10_exc_e	Reg.	0xA0240A68							
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_exc_expr ate_cntr	rw	na	0x0	Counting expected packet rate exceptions. The rate is sured in 125MHz clocks between two start of packet exand it should be within the deviation expected. This consaturates at 0xFFFF and is cleared by writting zero.					

1.12.	185 stream10_exc_e	Reg.	0xA0240A6C							
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.										
bits	name	s/w	h/w	default	description					
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is n	nesured by subtra	riation exceptions. The acting two rate measure- FFFF and is cleared by			

1.12.	186 stream10_rate_	Reg.	0xA0240A70							
Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default		description	า			
23:0	stream_rate_mea sured	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823					

1.12.187	tpg11_packe	t_rate_clks_ctrl		Reg.	0xA0240B34				
Control register - TPG Stream Packet rate									
bits	name	s/w h/w	default	description					

ast\_cntr

23:0	tpg_packet_rate	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For
	_clks				60kHz(16.7us period) packet rate this value is 2083 clocks =
					0x823

1.12.	188 tpg11_packet_s	size_c	lks_c	0xA0240B38						
Control register - TPG Stream Packet size										
bits	name	s/w	h/w	default	description					
15:0	tpg_packet_size _clks	rw	ro	0x40	Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit.					

1.12.	189 stream11_expsi	Reg.	0xA0240B3C								
Contr	Control register - Data stream expected packet size.										
bits	name	s/w	h/w	default	description						
31:0	stream11_expsiz e_dis	rw	ro	0x1E	Bits 15-0 - Data stream expected packet size in 4Byte inc ments (LSbit = 4Bytes).  Bit 31 - Diasable packet match against the expected pack size, by default matching is enabled.						

1.12.	190 stream11_expra	ıte_di		Reg.	0xA0240B40						
Contr	Control register - Data stream expected packet rate.										
bits	name	description									
31:0	stream11_exprat e_dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set D tion in 125MHz cl Bit 31 - set to 1 to	e distance between in clocks. In disable packet rate with deviation +, lata stream expect ocks. Default 0x71 In disable rate deviate	ed packet rate in 125MHz in two start of packet ate match against the ex- /-, by default enabled. ted packet rate +/- devia- =+/-127 clocks. ation match against the by default enabled.				

#### 0xA0240B44 1.12.191 stream11\_err\_stat Reg. Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped. bits h/w default name s/w description Expected packet size not matching to configured. Sticky bit. 0 stream\_err\_exps r/w1c wo 0x0 Write '1' to clear. ize 0x0 Packet FIFO is full. Sticky bit. Write '1' to clear. stream\_err\_pfif r/w1c wo ofull 2 stream\_err\_bfif r/w1c 0x0 Buffer FIFO is full. Sticky bit. Write '1' to clear. wo ofull 3 Packet is larger than 512\*4Bytes. Sticky bit. Write '1' to stream\_err\_maxs r/w1c wo 0x0 ize clear. 4 Packet is smaller than 3\*4Bytes. Sticky bit. Write '1' to clear. stream\_err\_mins r/w1c wo 0x0 ize 5 0x0 No tlast after tvalid goes low(tvalid goes low in the middle of stream\_err\_notl r/w1c wo the packet). Sticky bit. Write '1' to clear. ast 6 Packets arrive with IPG less than 7 clocks. Sticky bit. Write stream\_err\_mini r/w1c 0x0 wo '1' to clear. 0x0 FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' stream\_err\_watc r/w1c wo to clear. hdog

1.12.	192 stream11_err_e	Reg.	0xA0240B48							
Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default	description	n				
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	193 stream11_err_p	fifofu	i	Reg.	0xA0240B4C					
Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_pfif	rw	na	0x0	Counting packet FIFO full errors. This counter saturates a 0xFFFF and is cleared by writting zero.					

1.12.	194 stream11_err_b	fifofu		Reg.	0xA0240B50					
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	٦			
15:0	stream_err_bfif ofull cntr	rw	na	0x0	Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	195 stream11_err_n	Reg.	0xA0240B54							
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_maxs ize_cntr	rw	na	0x0	Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	196 stream11_err_m	Reg.	0xA0240B58							
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	٦			
15:0	stream_err_mins ize_cntr	rw	na	0x0	Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	197 stream11_err_r	Reg.	0xA0240B5C						
Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.									
bits	name	s/w	h/w	default		description	า		
15:0 stream_err_notl rw na 0x0 Counting no-tlast errors. This counter saturates at 0xFF ast_cntr and is cleared by writting zero.									

1.12.	198 stream11_err_n	Reg.	0xA0240B60						
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.									
bits	name	s/w	h/w	default		description			
15:0 stream_err_mini rw na 0x0 Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.									

1.12.199 stream11_err_watchdog_cntr_stat	Reg.	0xA0240B64
Status register - FSM watchdog error. The FSM was not in IDLE state fo	r longer than 20us	

bits	name	s/w	h/w	default	description	
15:0	stream_err_watc hdog_cntr	rw	na	0x0	Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero.	

1.12.	200 stream11_exc_e	0xA0240B68									
	Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.										
bits	name	s/w	h/w	default	description						
15:0	stream_exc_expr ate_cntr	rw	na	0x0	Counting expected packet rate exceptions. The rate is measured in 125MHz clocks between two start of packet events, and it should be within the deviation expected. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	201 stream11_exc_e	Reg.	0xA0240B6C						
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.									
bits	name	s/w	h/w	default		description	า		
	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.	<b>202</b> stream11_rate_	Reg.	0xA0240B70						
Status register - Data stream packet rate. Measured in clocks.									
bits	name	s/w	h/w	default		descriptio	n		
23:0	stream_rate_mea sured	rw	WO	0x0	Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823				

1.12.	203 tpg12_packet_ra	Reg.	0xA0240C34						
Control register - TPG Stream Packet rate									
bits	name	s/w	h/w	default		description			
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823				

1.12.	204 tpg12_packet_s	0xA0240C38							
Control register - TPG Stream Packet size									
bits	name	s/w	h/w	default	description				
15:0	tpg_packet_size _clks	rw	ro	0x40	Packet size measured in clocks of 125MHz clock. Minimum packet size is 64Bytes(4 clock samples x16Bytes each) = register value of 0x40. The 4 LSBits count the Bytes in one clock sample of 16Bytes. Each clock period generates a 128bit(16Byte) wide bus sample on the AXI-Stream bus. Each sample contains a 4bit stream number in the MSB 32bit, and 16bit incrementing value in the LSB 32bit.				

1.12.2	05 stream12_expsi	Reg.	0xA0240C3C							
Contro	Control register - Data stream expected packet size.									
bits name s/w h/w default description										

31:0	stream12_expsiz	rw	ro	0x40	Bits 15-0 - Data stream expected packet size in 4Byte incr-
	e_dis				ments (LSbit = 4Bytes).
					Bit 31 - Diasable packet match against the expected packet
					size, by default matching is enabled.
					Default is TBDWords=0xTBD (equal to TBDWords when
					add x2 tags and x padding words)
					Allowed min packet size = 3(3*4Bytes), allowed max packet
					size = 512(512*4Bytes).

1.12.	206 stream12_expi	Reg.	0xA0240C40								
Contr	Control register - Data stream expected packet rate.										
bits	name		des	cription							
31:0	stream12_exprat e_dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set E tion in 125MHz cl Bit 31 - set to 1 to	e distance b in clocks. o disable pa e with devia data stream ocks. Defau o disable rat	expected packet rate in 125MHz etween two start of packet cket rate match against the exation +/-, by default enabled. expected packet rate +/- deviault 0x7f=+/-127 clocks. the deviation match against the pon +/-, by default enabled.				

## 1.12.207 stream12\_err\_stat Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped. name s/w h/w default description stream\_err\_exps r/w1c wo 0x0 Expected packet size not matching to configured. Sticky bit.

0xA0240C44

U	ize	I/WTC	wo	UXU	Write '1' to clear.
1	stream_err_pfif ofull	r/w1c	WO	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	WO	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	1.12.208 stream12_err_expsize_cntr_stat 0xA0240C48									
Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_exps ize cntr	rw	na	0x0	Counting expecte rates at 0xFFFF a		ors. This counter satu-			

1.12.	209 stream12_err_p	Reg.	0xA0240C4C							
Statu	Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.									
bits	name	s/w	h/w	default		description				
15:0	stream_err_pfif ofull_cntr	rw	na	0x0	Counting packet for 0xFFFF and is clean		his counter saturates at zero.			

1.12.	210 stream12_err_b	Reg.	0xA0240C50						
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.									
bits	name	s/w	h/w	default		description	า		
15:0	stream_err_bfif ofull_cntr	rw	na	0x0	Counting Buffer F 0xFFFF and is cle		nis counter saturates at zero.		

1.12.	211 stream12_err_m	Reg.	0xA0240C54					
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.								
bits	name	s/w	h/w	default		description	1	
15:0	stream_err_maxs	rw	na	0x0	Counting packet nates at 0xFFFF a		ors. This counter satu-	

1.12.	<b>212</b>	Reg.	0xA0240C58						
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.									
bits	name	s/w	h/w	default		description	n		
15:0	stream_err_mins ize_cntr	rw	na	0x0	Counting packet r rates at 0xFFFF a		ors. This counter satu- writting zero.		

1.12.	213 stream12_err_n	Reg.	0xA0240C5C							
	Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.									
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF			

1.12.	214 stream12_err_m	Reg.	0xA0240C60						
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.									
bits	name	s/w	h/w	default		description	١		
15:0	stream_err_mini pg_cntr	rw	na	0x0	Counting minimur 0xFFFF and is cle		s counter saturates at ero.		

1.12.	1.12.215 stream12_err_watchdog_cntr_stat 0xA0240C64									
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_watc hdog_cntr	rw	na	0x0	Counting FSM wa		nis counter saturates at zero.			

1.12.	216 stream12_exc_e	Reg.	0xA0240C68						
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.									
bits	name	s/w	h/w	default		description	n		
15:0	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between to vithin the deviation	eptions. The rate is mea- wo start of packet events, n expected. This counter I by writting zero.		

1.12.217 stream12_exc_expratedeviate_cntr_stat	Reg.	0xA0240C6C	
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Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.

bits	name	s/w	h/w	default	description
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measurements. This counter saturates at 0xFFFF and is cleared by writting zero.

1.12.	218 stream12_rate_	Reg.	0xA0240C70				
Statu							
bits	name	s/w	h/w	default		description	n
23:0	stream_rate_mea sured	rw	wo	0x0		60kHz(16.7us pe	Hz clocks. Measured after eriod) packet rate this val- cox823

1.12.	219 tpg13_packet_ra	Reg.	0xA0240D34				
Control register - TPG Stream Packet rate							
bits	name	s/w	h/w	default		description	n
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masu 60kHz(16.7us per 0x823		25MHz clock. For his value is 2083 clocks =

1.12.	220 tpg13_packet_s	size_c		Reg.	0xA0240D38		
Control register - TPG Stream Packet size							
bits	name	s/w	h/w	default		des	scription
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64 register value of clock sample of 128bit(16Byte) we Each sample cor	Bytes(4 clo 0x40. The 4 16Bytes. Ea ride bus san ntains a 4bi	ocks of 125MHz clock. Minimum ock samples x16Bytes each) = 4 LSBits count the Bytes in one ach clock period generates a mple on the AXI-Stream bus. It stream number in the MSB ig value in the LSB 32bit.

1.12.	221 stream13_exps	ize_di	s_ctr	1	0xA0240D3C
Contr	ol register - Data stream	expecte	ed pack	ket size.	
bits	name	s/w	h/w	default	description
31:0	stream13_expsiz e_dis	rw	ro	0x40	Bits 15-0 - Data stream expected packet size in 4Byte incrments (LSbit = 4Bytes). Bit 31 - Diasable packet match against the expected packet size, by default matching is enabled. Default is TBDWords=0xTBD (equal to TBDWords when add x2 tags and x padding words) Allowed min packet size = 3(3*4Bytes), allowed max packet size = 512(512*4Bytes).

1.12.	222 stream13_expra	Reg.	0xA0240D40				
Control register - Data stream expected packet rate.							
bits	name	s/w	h/w	default		description	า
31:0	stream13_exprat e_dis	rw	ro	0x7F0040	clocks. This is the devents measured in Bit 30 - set to 1 to 0	distance betwee n clocks. disable packet ra	ed packet rate in 125MHz n two start of packet ate match against the ex- /-, by default enabled.

Bits 27-16 - Set Data stream expected packet rate +/- devia-
tion in 125MHz clocks. Default 0x7f=+/-127 clocks.
Bit 31 - set to 1 to disable rate deviation match against the
expected packet rate deviation +/-, by default enabled.

#### 1.12.223 stream13\_err\_stat

Reg.

0xA0240D44

Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

bits	name	s/w	h/w	default	description
0	stream_err_exps ize	r/w1c	WO	0x0	Expected packet size not matching to configured. Sticky bit. Write '1' to clear.
1	stream_err_pfif ofull	r/w1c	WO	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.
2	stream_err_bfif ofull	r/w1c	WO	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.
3	stream_err_maxs ize	r/w1c	WO	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	WO	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	WO	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	wo	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

## 1.12.224 stream13\_err\_expsize\_cntr\_stat



0xA0240D48

Status register - Data stream expected packet size error. The packet size doesn't match configured size.

	bits	name	s/w	h/w	default	description
15	5:0	stream_err_exps	rw	na		Counting expected packet size errors. This counter saturates at 0xEEEE and is cleared by writing zero
		ize_cntr				rates at 0xFFFF and is cleared by writting zero.

#### 1.12.225 stream13\_err\_pfifofull\_cntr\_stat



0xA0240D4C

Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.

Statu	Status register - Data stream Facket FIFO full effor. The packet FIFO should hever get full.								
bits	bits name s/w h/w default description								
15:0	stream_err_pfif ofull_cntr	rw	na		Counting packet FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

#### 1.12.226 stream13\_err\_bfifofull\_cntr\_stat



0xA0240D50

Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.

0.0.0							
bits	name	s/w	h/w	default	description		
15:0	stream_err_bfif ofull_cntr	rw	na	0x0	Counting Buffer FIFO full errors. This counter saturates at 0xFFFF and is cleared by writting zero.		

## 1.12.227 stream13\_err\_maxsize\_cntr\_stat



0xA0240D54

Status register - Data stream packet maximum size error. The packet is bigger than 512\*4Bytes.

bits	name	s/w	h/w	default	description
15:0	stream_err_maxs ize_cntr	rw	na		Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.

#### 1.12.228 stream13\_err\_minsize\_cntr\_stat



0xA0240D58

Statu	Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.								
bits	name	s/w	h/w	default	description				
15:0	stream_err_mins ize_cntr	rw	na	0x0	Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.				

1.12.	229 stream13_err_ı	Reg.	0xA0240D5C						
Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.									
bits	name	s/w	h/w	default		description	า		
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF		

1.12.	230 stream13_err_n	Reg.	0xA0240D60								
Statu	Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.										
bits	name	s/w	h/w	default		description	า				
15:0	stream_err_mini pg_cntr	rw	na	0x0	Counting minimur 0xFFFF and is cle		s counter saturates at ero.				

1.12.	231 stream13_err_w	Reg.	0xA0240D64								
Statu	Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.										
bits	name	s/w	h/w	default		description	า				
15:0	stream_err_watc hdog_cntr	rw	na	0x0	Counting FSM wa 0xFFFF and is cle		is counter saturates at ero.				

1.12.	232 stream13_exc_e	Reg.	0xA0240D68				
Status	s register - Data stream extion.	te doesn't match	configured including the				
bits	name	s/w	h/w	default		descriptio	n
15:0	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between the clocks between the control of the control of the clocks are controls.	eptions. The rate is mea- wo start of packet events, n expected. This counter d by writting zero.

1.12.	233	Reg.	0xA0240D6C							
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	rate deviation is m	esured by subtra	iation exceptions. The acting two rate measure- FFFF and is cleared by			

1.12.	234 stream13_rate_	Reg.	0xA0240D70							
Status register - Data stream packet rate. Measured in clocks.										
bits	name	s/w	h/w	default		descriptio	n			
23:0	stream_rate_mea sured	rw	WO	0x0	· ·	60kHz(16.7us pe	Hz clocks. Measured after eriod) packet rate this val- = 0x823			

1.12.	235 tpg14_packet_ra	Reg.	0xA0240E34							
Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default		description				
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masu 60kHz(16.7us per 0x823		25MHz clock. For his value is 2083 clocks =			

1.12.	236 tpg14_packet_s	ize_c	lks_c	trl	Reg.	0xA0240E38				
Conti	Control register - TPG Stream Packet size									
bits	name	s/w	h/w	default	descri	iption				
15:0	tpg_packet_size _clks	rw	ro	0x40	Packet size measured in clock packet size is 64Bytes(4 clock register value of 0x40. The 4 L clock sample of 16Bytes. Each 128bit(16Byte) wide bus samp Each sample contains a 4bit st 32bit, and 16bit incrementing v	samples x16Bytes each) = SBits count the Bytes in one a clock period generates a le on the AXI-Stream bus. tream number in the MSB				

1.12.	237 stream14_exps	size_di	is_ctı	rl		Reg.	0xA0240E3C		
Control register - Data stream expected packet size.									
bits	name	s/w	h/w	default		des	cription		
31:0	stream14_expsiz e_dis	rw	ro	0x40	ments (LSbit = 4B) Bit 31 - Diasable p size, by default ma Default is TBDWor add x2 tags and x	ytes). acket mate atching is e rds=0xTBE padding w et size = 3(	(equal to TBDWords when		

1.12.	238 stream14_exp	orate_di	s_ctı	1		Reg.	0xA0240E40			
Contr	Control register - Data stream expected packet rate.									
bits	name	s/w	h/w	default		descri	ption			
31:0	stream14_exprat e_dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set I tion in 125MHz cl Bit 31 - set to 1 to	e distance bet in clocks. o disable pack e with deviatio Data stream ex ocks. Default o disable rate	pected packet rate in 125MHz ween two start of packet  et rate match against the expon +/-, by default enabled.  expected packet rate +/- devia- 0x7f=+/-127 clocks.  deviation match against the +/-, by default enabled.			

1.12.	239	Reg.	0xA0240E44							
Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.										
bits	name	s/w	h/w	default		description	า			
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet Write '1' to clear.	size not matching	to configured. Sticky bit.			
1	stream_err_pfif ofull	r/w1c	wo	0x0	Packet FIFO is fu	II. Sticky bit. Write	e '1' to clear.			
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full	. Sticky bit. Write	'1' to clear.			
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger the clear.	nan 512*4Bytes. S	Sticky bit. Write '1' to			
4	stream_err_mins	r/w1c	wo	0x0	Packet is smaller	than 3*4Bytes. St	ticky bit. Write '1' to clear.			

	ize				
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	wo	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	240 stream14_err_e	Reg.	0xA0240E48								
Statu	Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	241 stream14_err_p	Reg.	0xA0240E4C								
Statu	Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.										
bits name s/w h/w default description											
bits	name	s/w	h/w	default		description	n				

1.12.	242 stream14_err_b	Reg.	0xA0240E50								
Statu	Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	n				
15:0 stream_err_bfif rw na 0x0 Counting Buffer FIFO full errors. This counter saturates ofull_cntr 0xFFFF and is cleared by writting zero.											

1.12.	243 stream14_err_m	Reg.	0xA0240E54									
Statu	Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.											
bits	name	s/w	h/w	default		description	n					
15:0	stream_err_maxs ize_cntr	rw	na	0x0	Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.							

1.12.	1.12.244 stream14_err_minsize_cntr_stat 0xA0240E58										
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.											
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_mins ize cntr	rw	na	0x0	Counting packet minimum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.						

1.12.	245 stream14_err_n	Reg.	0xA0240E5C								
	Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.										
bits	name	s/w	h/w	default		description	n				
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF				

1.12.246 stream14_err_minipg_cntr_stat 0xA0240E60										
	Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.									
bits	name	description	า							

15:0	stream_err_mini	rw	na	0x0	Counting minimum IPG errors. This counter saturates at
	pg_cntr				0xFFFF and is cleared by writting zero.

1.12.	247 stream14_err_w	Reg.	0xA0240E64							
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.										
bits	name	s/w	h/w	default		description	n			
15:0 stream_err_watc rw na 0x0 Counting FSM watchdog errors. This counter saturates 0xFFFF and is cleared by writting zero.										

1.12.	248 stream14_exc_e	Reg.	0xA0240E68							
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_exc_expr ate_cntr	rw	na	0x0	sured in 125MHz	clocks between twithin the deviation	eptions. The rate is mea- wo start of packet events, n expected. This counter by writting zero.			

1.12.249 stream14_exc_expratedeviate_cntr_stat 0xA0240E6C										
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measu ments. This counter saturates at 0xFFFF and is cleared writting zero.					

1.12.	250 stream14_rate_	Reg.	0xA0240E70								
Status register - Data stream packet rate. Measured in clocks.											
bits	name	s/w	h/w	default		description					
23:0	stream_rate_mea sured	rw	WO	0x0		60kHz(16.7us pe	Hz clocks. Measured after eriod) packet rate this val- = 0x823				

1.12.	251 tpg15_packet_r	ate_c		Reg.	0xA0240F34					
Control register - TPG Stream Packet rate										
bits	name	s/w	h/w	default	description					
23:0	tpg_packet_rate _clks	rw	ro	0x823	Packet rate masured in clocks of 125MHz clock. For 60kHz(16.7us period) packet rate this value is 2083 clocks 0x823					

1.12.	252 tpg15_packet_s	ize_c	Reg.	0xA0240F38					
Control register - TPG Stream Packet size									
bits	name	s/w	h/w	default	desc	cription			
15:0	tpg_packet_size _clks	rw	ro	0x40	packet size is 64Bytes(4 cloc	LSBits count the Bytes in one ch clock period generates a uple on the AXI-Stream bus. stream number in the MSB			

1.12.	253 stream15_exps	ize_di		Reg.	0xA0240F3C							
Contr	Control register - Data stream expected packet size.											
bits	name	s/w		descrip	tion							
31:0	stream15_expsiz e_dis	rw	ro	0x40	ments (LSbit = 48 Bit 31 - Diasable size, by default m Default is TBDW add x2 tags and x	Bytes).  packet match a patching is enab ords=0xTBD (e- x padding word set size = 3(3*4)	qual to TBDWords when					

1.12.	254 stream15_expı	rate_di		Reg.	0xA0240F40				
Control register - Data stream expected packet rate.									
bits	name	s/w		desc	cription				
31:0	stream15_exprat e_dis	rw	ro	0x7F0040	clocks. This is the events measured Bit 30 - set to 1 to pected packet rat Bits 27-16 - Set E tion in 125MHz cl Bit 31 - set to 1 to	e distance be in clocks.  In clocks.  In disable pace with devia pata stream ocks. Defau disable rate	expected packet rate in 125MHz etween two start of packet cket rate match against the extion +/-, by default enabled. expected packet rate +/- deviation x7f=+/-127 clocks. e deviation match against the on +/-, by default enabled.		

## Status register - Data stream errors. One sticky bit per type of error, write 1 to clear. Should be all '0' in normal operation. Any of these events will trigger output pipe reset and one packet or more will be dropped.

0xA0240F44

bits	name	s/w	h/w	default	description
0	stream_err_exps ize	r/w1c	wo	0x0	Expected packet size not matching to configured. Sticky bit. Write '1' to clear.
1	stream_err_pfif ofull	r/w1c	wo	0x0	Packet FIFO is full. Sticky bit. Write '1' to clear.
2	stream_err_bfif ofull	r/w1c	wo	0x0	Buffer FIFO is full. Sticky bit. Write '1' to clear.
3	stream_err_maxs ize	r/w1c	wo	0x0	Packet is larger than 512*4Bytes. Sticky bit. Write '1' to clear.
4	stream_err_mins ize	r/w1c	wo	0x0	Packet is smaller than 3*4Bytes. Sticky bit. Write '1' to clear.
5	stream_err_notl ast	r/w1c	wo	0x0	No tlast after tvalid goes low(tvalid goes low in the middle of the packet). Sticky bit. Write '1' to clear.
6	stream_err_mini pg	r/w1c	wo	0x0	Packets arrive with IPG less than 7 clocks. Sticky bit. Write '1' to clear.
7	stream_err_watc hdog	r/w1c	wo	0x0	FSM not hitting IDLE for more than 20us. Sticky bit. Write '1' to clear.

1.12.	256 stream15_err_e	xpsiz		Reg.	0xA0240F48					
Status register - Data stream expected packet size error. The packet size doesn't match configured size.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_exps ize_cntr	rw	na	0x0	Counting expected packet size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.257 stream15_err_pfifofull_cntr_stat	Reg.	0xA0240F4C

1.12.255 stream15\_err\_stat

Statu	Status register - Data stream Packet FIFO full error. The packet FIFO should never get full.									
bits	name	s/w	h/w	default	description					
15:0	stream_err_pfif rw na 0x0		0x0	Counting packet FIFO full errors. This counter saturates at						
	ofull_cntr				0xFFFF and is cleared by writting zero.					

1.12.	258 stream15_err_b	Reg.	0xA0240F50							
Status register - Data stream Buffer FIFO full error. The Buffer FIFO should never get full.										
bits	name	s/w	h/w	default		description	า			
15:0	stream_err_bfif ofull cntr	rw	na	0x0	Counting Buffer FIFO full errors. This counter saturates a 0xFFFF and is cleared by writting zero.					

1.12.	259 stream15_err_m	Reg.	0xA0240F54							
Status register - Data stream packet maximum size error. The packet is bigger than 512*4Bytes.										
bits	name	s/w	h/w	default		description	١			
15:0	stream_err_maxs ize_cntr	rw	na	0x0	Counting packet maximum size errors. This counter saturates at 0xFFFF and is cleared by writting zero.					

1.12.	260 stream15_err_m	ninsiz	Reg.	0xA0240F58						
Status register - Data stream packet minimum size error. The packet is smaller than 3*4Bytes.										
bits	name	s/w	h/w	default		description	n			
15:0	stream_err_mins ize_cntr	rw	na	0x0	•	et minimum size errors. This counter satu- F and is cleared by writting zero.				

1.12.	261 stream15_err_n	otlast		Reg.	0xA0240F5C						
	Status register - Data stream packet no-tlast when tvalid goes low error. The tvalid should not go low in the middle of the packet.										
bits	name	s/w	h/w	default		description	٦				
15:0	stream_err_notl ast_cntr	rw	na	0x0	Counting no-tlast and is cleared by		ter saturates at 0xFFFF				

1.12.	262 stream15_err_n	Reg.	0xA0240F60					
Status register - Data stream minumim Inter-Packet-Gap(IPG) error. The gap between packets is less than 7 clocks.								
bits	name	s/w	h/w	default		description	า	
15:0	stream_err_mini pg_cntr	rw	na	0x0	Counting minimum IPG errors. This counter saturates at 0xFFFF and is cleared by writting zero.			

1.12.	263 stream15_err_w	Reg.	0xA0240F64				
Status register - FSM watchdog error. The FSM was not in IDLE state for longer than 20us.							
bits	name	s/w	h/w	default	description		n
15:0	stream_err_watc hdog cntr	rw	na	0x0	Counting FSM watchdog errors. This counter saturates at 0xFFFF and is cleared by writting zero.		

1.12.	264 stream15_exc_e	Reg.	0xA0240F68				
Status register - Data stream expected packet rate exceptions. The packet rate doesn't match configured including the deviation.							
bits	name	s/w	h/w	default		description	n
15:0	stream_exc_expr ate_cntr	rw	na	0x0	0 1	•	eptions. The rate is meawo start of packet events,

and it should be within the deviation expected. This counter
saturates at 0xFFFF and is cleared by writting zero.

1.12.265 stream15_exc_expratedeviate_cntr_stat						Reg.	0xA0240F6C
Status register - Data stream expected packet rate deviation exceptions. The packet rate deviation doesn't match configured.							
bits	name	s/w	h/w	default		description	า
	stream_exc_expr atedeviate_cntr	rw	na	0x0	Counting expected packet rate deviation exceptions. The rate deviation is mesured by subtracting two rate measur ments. This counter saturates at 0xFFFF and is cleared writting zero.		cting two rate measure-

1.12.	266 stream15_rate_	_meas	Reg.	0xA0240F70			
Statu	s register - Data stream p	oacket ra	ate. Me	easured in clo	ocks.		
bits	name	s/w	h/w	default		description	
23:0	stream_rate_mea sured	rw	wo	0x0	Measures the packet rate in 125MHz clocks. Measured after every packet. For 60kHz(16.7us period) packet rate this value should be around 2083 clocks = 0x823		

1.13 ipi_mcdma_axilite_pg288	Block	0xA1000000 - 0xA1001FFF
MCDMA IP		

1.13.1 ram_8kb_inst	ram_8kb_inst	t		0xA1000000, 0xA1000004 0xA1001FFF
offset	depth 2048	width 32	default	0x0

1.14 ipi_gpio_cache_control	Block ■T■	0xA2000000 - 0xA2000003
GPIO Cache Control		

1.14.	1 gpio_cache_contr	Reg.	0xA2000000					
GPIO IP used to control the cache and protection flags on MCDMA AXI-MM busses								
bits	name	s/w	h/w	default		description		
6:0	gpio_cache_cont rol	ro	na	0x2B	The 4bit cache flag default value is 0xb. The 3bit prot fla default value is 0x2		0xb. The 3bit prot flag	

1.15 ipi_mcdma_bd_ram	Block	0xAA000000 - 0xAA007FFF
MCDMA BD RAM for Sim and HW debug		



1.16 ipi_mcdma_debug_	Block □ T□	0xAB000000 - 0xAB007FFF	
MCDMA Debug Ram for Sim a	nd HW debug		
1.16.1 ram_32kb_inst	ram_32kb_inst		0xAB000000, 0xAB000004 0xAB007FFF
offset	depth 8192 width 32	default	0x0