

# JORDAN, CHAK-WA PUI

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## INTERESTS AND EXPERTISE

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- Physical design for both ASICs and FPGAs

## EDUCATION

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- **The Chinese University of Hong Kong, Hong Kong, China** *Aug. 2015 – Aug. 2019*  
Doctor of Philosophy, Computer Science and Engineering  
Advisor: Evangeline F. Y. Young
- **Shanghai Jiao Tong University, Shanghai, China** *Sep. 2011 – Jul. 2015*  
Bachelor of Science, Computer Science and Technology

## WORK EXPERIENCE

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- **Huawei, Shenzhen, China** *Mar. 2021 – present*  
Senior Research Engineer in Decision Making & Reasoning Lab of Noah's Ark Lab
- **Cadence Design Systems, Shanghai, China** *May. 2020 – Mar. 2021*  
Lead Software Engineer in Detailed Placement Team of Innovus
- **The Chinese University of Hong Kong, Hong Kong, China** *Aug. 2019 – Nov. 2019*  
Research Assistant in CSE Department
- **Synopsys, Hillsboro, OR, U.S.** *May. 2018 – Aug. 2018*  
Technical-Engineering Intern in Zebu Back-End Team
- **Cadence Design Systems, San Jose, CA, U.S.** *May. 2017 – Sep. 2017*  
Software Engineering Intern in Detailed Routing Team of Innovus
- **The Chinese University of Hong Kong, Hong Kong, China** *Sep. 2015 – Aug. 2018*  
Teaching Assistant in CSE Department

## PUBLICATIONS

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### Conference Papers

- [C11] Dan Zheng, Xiaopeng Zhang, **Chak-Wa Pui**, Evangeline F.Y. Young, "Multi-FPGA Co-optimization: Hybrid Routing and Competitive-based Time Division Multiplexing Assignment", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Virtual Conference, Jan. 18-21, 2021.
- [C10] Jinwei Liu, **Chak-Wa Pui**, Fangzhou Wang, Evangeline F.Y. Young, "CUGR: Detailed-Routability-Driven 3D Global Routing with Probabilistic Resource Model", ACM/IEEE Design Automation Conference (DAC), Virtual Conference, July 19-23, 2020.
- [C9] **Chak-Wa Pui**, Evangeline F.Y. Young, "Lagrangian Relaxation-Based Time-Division Multiplexing Optimization for Multi-FPGA Systems", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Westminster, CO, USA, Nov. 4-7, 2019.
- [C8] **Chak-Wa Pui**, Gang Wu, Freddy Y. C. Mang, Evangeline F Y. Young, "An Analytical Approach for Time-Division Multiplexing Optimization in Multi-FPGA based Systems", ACM/IEEE International Workshop on System-Level Interconnect Prediction (SLIP), Las Vegas, NV, USA, June 2, 2019.
- [C7] Biying Xu, Shaolan Li, **Chak-Wa Pui**, Derong Liu, Linxiao Shen, Yibo Lin, Nan Sun and David Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits", ACM International Symposium on Physical Design (ISPD), San Francisco, CA, USA, Apr. 14-17, 2019.
- [C6] Gengjie Chen, **Chak-Wa Pui**, Haocheng Li, Jingsong Chen, Bentian Jiang, Evangeline F.Y. Young, "Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Tokyo, Japan, Jan. 21-24, 2019.
- [C5] Peishan Tu, **Chak-Wa Pui**, Evangeline F.Y. Young, "Simultaneous Timing Driven Tree Surgery in Routing with Machine Learning-based Acceleration", ACM Great Lakes Symposium on VLSI (GLSVLSI), Chicago, IL, USA, May 23-25, 2018

- [C4] **Chak-Wa Pui**, Peishan Tu, Haocheng Li, Gengjie Chen, Evangeline F.Y. Young, “A Two-Step Search Engine For Large Scale Boolean Matching Under NP3 Equivalence”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Jeju Island, Korea, Jan. 22-25, 2018.
- [C3] **Chak-Wa Pui**, Gengjie Chen, Yuzhe Ma, Evangeline F.Y. Young, Bei Yu, “Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Irvine, CA, USA, Nov. 13-16, 2017.
- [C2] **Chak-Wa Pui**, Gengjie Chen, Wing-Kai Chow, Jian Kuang, Ka-Chun Lam, Peishan Tu, Hang Zhang, Evangeline F.Y. Young, Bei Yu, “RippleFPGA: A Routability-Driven Placement for Large-Scale Heterogeneous FPGAs”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, USA, Nov. 7-10, 2016.
- [C1] Wing-Kai Chow, **Chak-Wa Pui**, Evangeline F.Y. Young, “Legalization Algorithm for Multiple-Row Height Standard Cell Design”, ACM/IEEE Design Automation Conference (DAC), Austin, TX, USA, June 5-9, 2016.

## Journal Papers

- [J4] **Chak-Wa Pui**, Evangeline F.Y. Young, “Lagrangian Relaxation-Based Time-Division Multiplexing Optimization for Multi-FPGA Systems”, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2020.
- [J3] Gengjie Chen, **Chak-Wa Pui**, Haocheng Li, Evangeline F.Y. Young, “Dr. CU: Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020.
- [J2] Peishan Tu, **Chak-Wa Pui**, Evangeline F.Y. Young, “Simultaneous Reconnection Surgery Technique of Routing with Machine Learning-based Acceleration”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020.
- [J1] Gengjie Chen, **Chak-Wa Pui**, Wing-Kai Chow, Ka-Chun Lam, Jian Kuang, Evangeline F.Y. Young and Bei Yu, “RippleFPGA: Routability-Driven Simultaneous Packing and Placement for Modern FPGAs”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018.

## RESEARCH AND PROJECT EXPERIENCE

- Routing
  - 2D module-level routing *Apr. 2021 – present*
  - Multi-FPGA routing with time-division multiplexing technique *May. 2019 – Sep. 2019*
  - Detailed routability-driven global routing *May. 2019 – Sep. 2019*
  - Time-division multiplexing optimization for multi-FPGA systems *May. 2018 – Apr. 2019*
  - Initial detailed routing *Jan. 2018 – Mar. 2018*
  - Tree surgery with machine learning *Sep. 2017 – Nov. 2017*
  - DRC removal on transition layers *May. 2017 – Aug. 2017*
  - Net open location finder with obstacles *May. 2017 – Aug. 2017*
- Placement
  - 2D floorplanning *Apr. 2021 – present*
  - Improving legalization in N3 hybrid row design *Nov. 2020 – Feb. 2021*
  - Improving stability and scalability of data structure in rule checking *Jun. 2020 – Oct. 2020*
  - Multi-FPGA partitioning *Sep. 2019 – Nov. 2019*
  - Analytical analog placement *Jul. 2018 – Aug. 2018*
  - Clock-aware FPGA placement (Routability-driven & Clock-aware) *Feb. 2016 – Aug. 2017*
  - Multi-row height standard cell placement *Aug. 2015 – Dec. 2015*
- Logic Synthesis
  - Gate sizing and postmapping PPA optimization *Apr. 2021 – present*
  - Non-exact projective NPNP Boolean matching *Jun. 2016 – Dec. 2016*

## SELECTED AWARDS AND HONORS

- |   |       |      |
|---|-------|------|
| • 3rd Place Award in CAD Contest on “System-level FPGA Routing with TDM Technique”    | ICCAD | 2019 |
| • 1st Place Award in CAD Contest on “LEF/DEF Based Open-Source Global Router”         | ICCAD | 2019 |
| • Best Paper Award Nomination   | ISPD  | 2019 |
| • 2nd Place Award in CAD Contest on “Initial Detailed Routing”                        | ISPD  | 2018 |
| • 3rd Place Award in CAD Contest on “Clock-Aware FPGA Placement”                      | ISPD  | 2017 |
| • 1st Place Award in CAD Contest on “NP3: Non-exact Projective NPNP Boolean Matching” | ICCAD | 2016 |
| • Best Paper Award Nomination   | DAC   | 2016 |
| • 2nd Place Award in CAD Contest on “Routability-Driven FPGA Placement”               | ISPD  | 2016 |
| • Full Postgraduate Studentship   | CUHK  | 2015 |

## PROFESSIONAL SERVICES

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### Reviewer/ External Reviewer

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- ACM/IEEE Design Automation Conference (DAC)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM International Symposium on Physical Design (ISPD)
- IEEE International Conference on Computer Design (ICCD)
- ACM Great Lakes Symposium on VLSI (GLSVLSI)
- Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI)

### Technical Program Committee

- ACM/IEEE Design Automation Conference (DAC)

## TECHNICAL SKILLS

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|--------------------------|--|
| <b>Languages</b>         | C/C++, $\text{\LaTeX}$ , Python, Shell Programming |
| <b>Operating Systems</b> | Linux/UNIX   |