DATA SHEETS

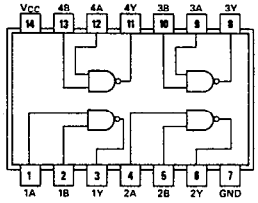
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

00

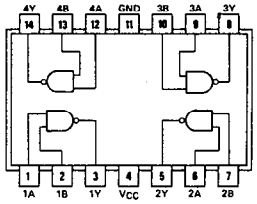
positive logic:
$Y = \overline{AB}$

See page 6-2



SN5400 (J)
SN54H00 (J)
SN54L00 (J)
SN54LS00 (J, W)
SN54S00 (J, W)

SN7400 (J, N)
SN74H00 (J, N)
SN74L00 (J, N)
SN74LS00 (J, N)
SN74S00 (J, N)



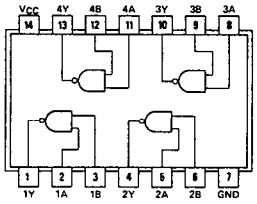
SN5400 (W)
SN54H00 (W)
SN54L00 (T)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

01

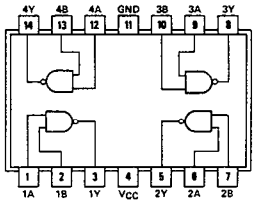
positive logic:
$Y = \overline{AB}$

See page 6-4

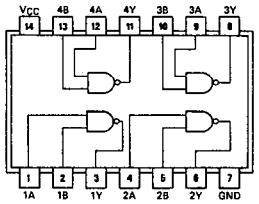


SN5401 (J)
SN54LS01 (J, W)

SN7401 (J, N)
SN74LS01 (J, N)



SN5401 (W)
SN54H01 (W)
SN54L01 (T)



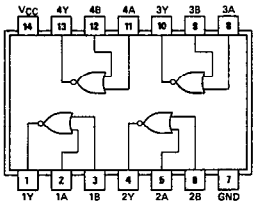
SN54H01 (J)
SN74H01 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

02

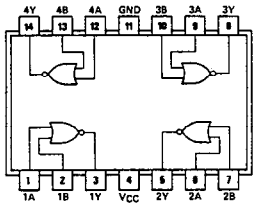
positive logic:
$Y = \overline{A+B}$

See page 6-8



SN5402 (J)
SN54L02 (J)
SN54LS02 (J, W)
SN54S02 (J, W)

SN7402 (J, N)
SN74L02 (J, N)
SN74LS02 (J, N)
SN74S02 (J, N)



SN5402 (W)
SN54L02 (T)

5

1076

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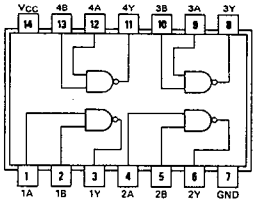
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:
$Y = \overline{AB}$

See page 6-4



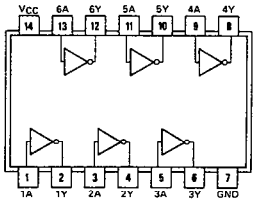
SN5403 (J) SN7403 (J, N)
SN54L03 (J) SN74L03 (J, N)
SN54LS03 (J, W) SN74LS03 (J, N)
SN54S03 (J, W) SN74S03 (J, N)

HEX INVERTERS

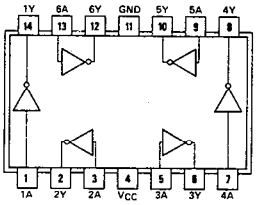
04

positive logic:
$Y = \overline{A}$

See page 6-2



SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)



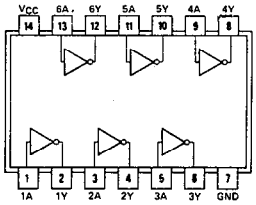
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

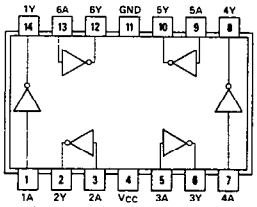
05

positive logic:
$Y = \overline{A}$

See page 6-4



SN5405 (J) SN7405 (J, N)
SN54H05 (J) SN74H05 (J, N)
SN54LS05 (J, W) SN74LS05 (J, N)
SN54S05 (J, W) SN74S05 (J, N)



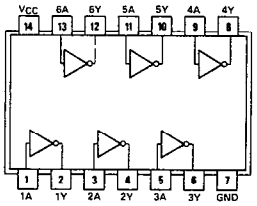
SN5405 (W)
SN54H05 (W)

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

06

positive logic:
$Y = \overline{A}$

See page 6-24



SN5406 (J, W) SN7406 (J, N)

5

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

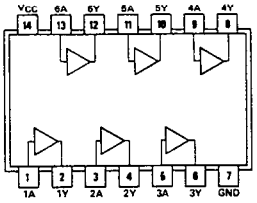
PIN ASSIGNMENTS (TOP VIEWS)

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

07

positive logic:
Y = A

See page 6-24



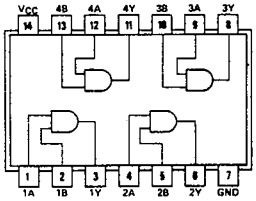
SN5407 (J, W) SN7407 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
Y = AB

See page 6-10



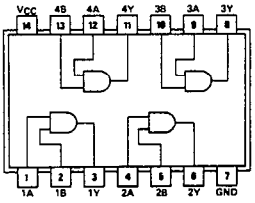
SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

09

positive logic:
Y = AB

See page 6-12



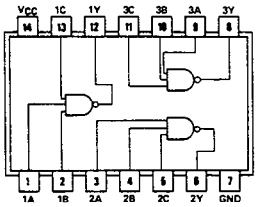
SN5409 (J, W) SN7409 (J, N)
SN54LS09 (J, W) SN74LS09 (J, N)
SN54S09 (J, W) SN74S09 (J, N)

TRIPLE 3-INPUT
POSITIVE-NAND GATES

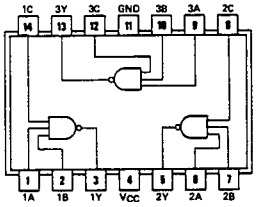
10

positive logic:
$Y = \overline{ABC}$

See page 6-2



SN5410 (J) SN7410 (J, N)
SN54H10 (J) SN74H10 (J, N)
SN54L10 (J) SN74L10 (J, N)
SN54LS10 (J, W) SN74LS10 (J, N)
SN54S10 (J, W) SN74S10 (J, N)



SN5410 (W)
SN54H10 (W)
SN54L10 (T)

5

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54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

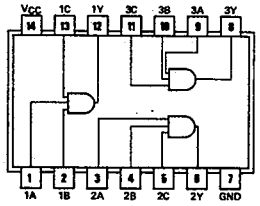
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

15

positive logic:
Y = ABC

See page 6-12



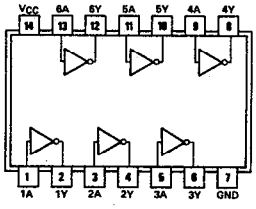
SN54H15 (J, W) SN74H15 (J, N)
SN54LS15 (J, W) SN74LS15 (J, N)
SN54S15 (J, W) SN74S15 (J, N)

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

16

positive logic:
Y = $\overline{A}$

See page 6-24



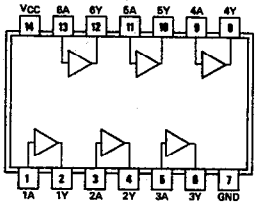
SN5416 (J, W) SN7416 (J, N)

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

17

positive logic:
Y = A

See page 6-24



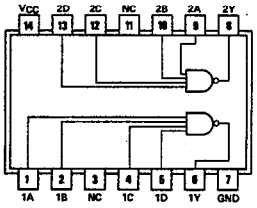
SN5417 (J, W) SN7417 (J, N)

DUAL 4-INPUT POSITIVE-NAND GATES

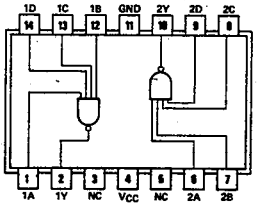
20

positive logic:
Y = $\overline{ABCD}$

See page 6-2



SN5420 (J) SN7420 (J, N)
SN54H20 (J) SN74H20 (J, N)
SN54L20 (J) SN74L20 (J, N)
SN54LS20 (J, W) SN74LS20 (J, N)
SN54S20 (J, W) SN74S20 (J, N)



SN5420 (W)
SN54H20 (W)
SN54L20 (T)

NC—No internal connection

TEXAS INSTRUMENTS
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54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

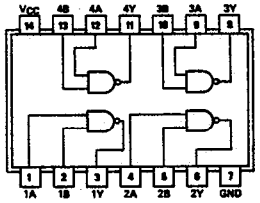
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

26

positive logic:
$Y = \overline{AB}$

See pages 6-24 and 6-26



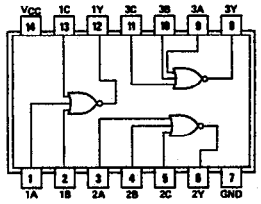
SN5426 (J) SN7426 (J, N)
SN54LS26 (J, W) SN74LS26 (J, N)

TRIPLE 3-INPUT POSITIVE-NOR GATES

27

positive logic:
$Y = \overline{A+B+C}$

See page 6-8



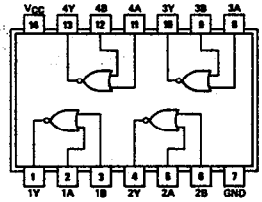
SN5427 (J, W) SN7427 (J, N)
SN54LS27 (J, W) SN74LS27 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

28

positive logic:
$Y = \overline{A+B}$

See page 6-20



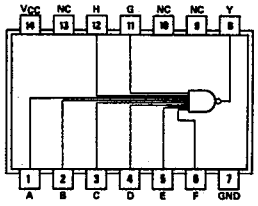
SN5428 (J, W) SN7428 (J, N)
SN54LS28 (J, W) SN74LS28 (J, N)

8-INPUT POSITIVE-NAND GATES

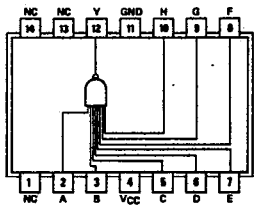
30

positive logic:
$Y = \overline{ABCDEFGH}$

See page 6-2



SN5430 (J) SN7430 (J, N)
SN54H30 (J) SN74H30 (J, N)
SN54L30 (J) SN74L30 (J, N)
SN54LS30 (J, W) SN74LS30 (J, N)
SN54S30 (J, W) SN74S30 (J, N)



SN5430 (W)
SN54H30 (W)
SN54L30 (T)

NC—No internal connection

TEXAS INSTRUMENTS
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PIN ASSIGNMENTS (TOP VIEWS)

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

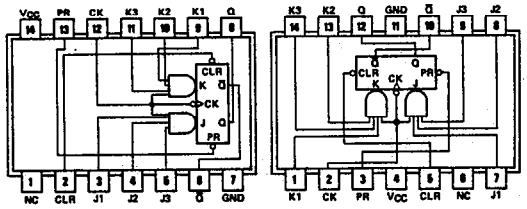
72

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q_0	$\bar{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

positive logic: J = J1·J2·J3; K1·K2·K3

See pages 6-46, 6-50, and 6-54



SN5472 (J) SN7472 (J, N) SN5472 (W)
SN54H72 (J) SN74H72 (J, N) SN54H72 (W)
SN54L72 (J) SN74L72 (J, N) SN54L72 (T)

NC—No internal connection

DUAL J-K FLIP-FLOPS WITH CLEAR

73

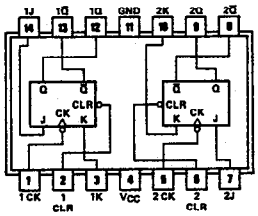
'73, 'H73, 'L73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

'LS73A
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56



SN5473 (J, W) SN7473 (J, N)
SN54H73 (J, W) SN74H73 (J, N)
SN54L73 (J, T) SN74L73 (J, N)
SN54LS73A (J, W) SN74LS73A (J, N)

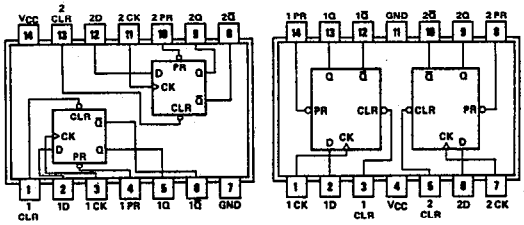
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56



SN5474 (J) SN7474 (J, N) SN5474 (W)
SN54H74 (J) SN74H74 (J, N) SN54H74 (W)
SN54L74 (J) SN74L74 (J, N) SN54L74 (T)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)

See explanation of function tables on page 3-8.

*This configuration is nonstable; that is, it will not persist when preset or clear inputs return to their inactive (high) level. Furthermore, the output levels of the 'LS74A in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum.

TEXAS INSTRUMENTS
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TTL MSI

TYPES SN5475, SN5477, SN54L75, SN54L77, SN54LS75, SN54LS77, SN7475, SN74L75, SN74L77, SN74LS75 4-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7611851, MARCH 1974—REVISED OCTOBER 1976

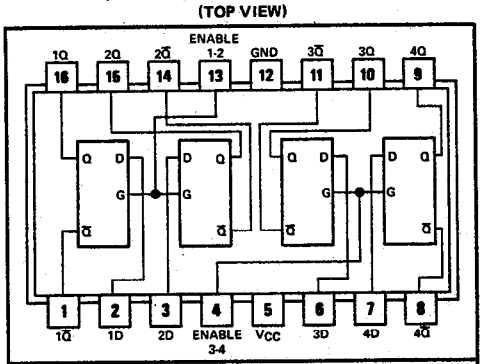
logic

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

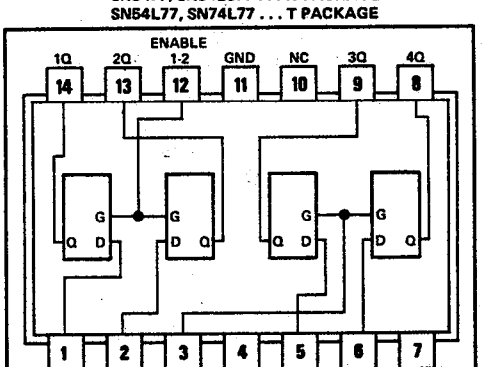
H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

SN5475, SN54LS75 . . . J OR W PACKAGE
SN54L75 . . . J PACKAGE
SN7475, SN74L75, SN74LS75 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

SN5477, SN54LS77 . . . W PACKAGE
SN54L77, SN74L77 . . . T PACKAGE



logic: see function table

NC—No internal connection

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The '75, 'L75, and 'LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77, 'L77, and 'LS77 4-bit latches are available in 14-pin flat packages.

These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54, 54L, and 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, 74L, and 74LS devices are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '75, 'L75, '77, 'L77	5.5 V
'LS75, 'LS77	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54L', SN54LS' Circuits	−55°C to 125°C
SN74', SN74L', SN74LS' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

TTL
MSI

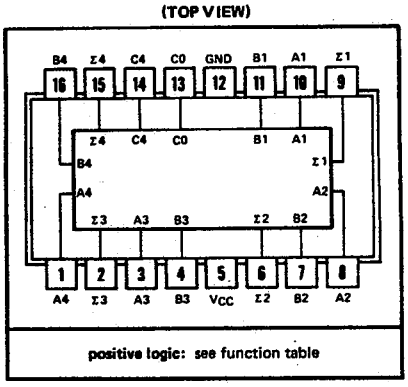
TYPES SN5483A, SN54LS83A, SN7483A, SN74LS83A
4-BIT BINARY FULL ADDERS WITH FAST CARRY

BULLETIN NO. DL-S 7611853, MARCH 1974—REVISED OCTOBER 1976

- Full-Carry Look-Ahead across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- SN54283/SN74283 and SN54LS283/SN74LS283 Are Recommended For New Designs as They Feature Supply Voltage and Ground on Corner Pins to Simplify Board Layout

TYPE	TYPICAL ADD TIMES: TWO 8-BIT WORDS	TYPICAL ADD TIMES: TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER 4-BIT ADDER
'83A	23 ns	43 ns	310 mW
'LS83A	25 ns	45 ns	95 mW

SN5483A, SN54LS83A . . . J OR W PACKAGE
SN7483A, SN74LS83A . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These improved full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Designed for medium-speed applications, the circuits utilize transistor-transistor logic that is compatible with most other TTL families and other saturated low-level logic families.

Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUT				OUTPUT: WHEN C0 = L			OUTPUT: WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '83A . . . . . 5.5 V
'LS83A . . . . . 7 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5483A, SN54LS83A . . . . . −55°C to 125°C
SN7483A, SN74LS83A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '83A only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

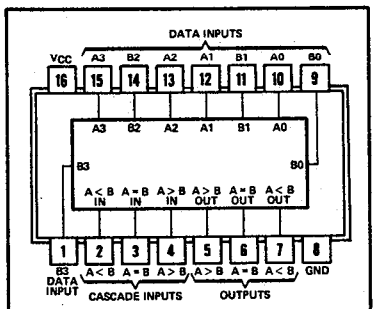
TTL
MSI

TYPES SN5485, SN54L85, SN54LS85, SN54S85, SN7485, SN74L85, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS

BULLETIN NO. DL-S 7611810, MARCH 1974—REVISED OCTOBER 1976

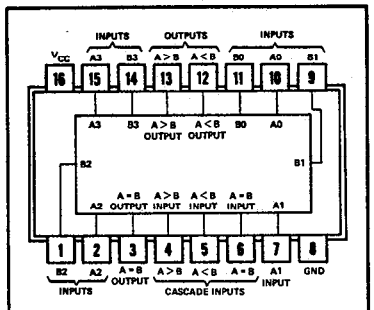
TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'L85	20 mW	90 ns
'LS85	52 mW	24 ns
'S85	365 mW	11 ns

SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE
SN7485, SN74LS85, SN74S85 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function tables

SN54L85 . . . J PACKAGE
SN74L85 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function tables

description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and in addition for the 'L85, low-level voltages applied to the A > B and A < B inputs. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

'85, 'LS85, 'S85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

'L85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

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TEXAS INSTRUMENTS
INCORPORATED
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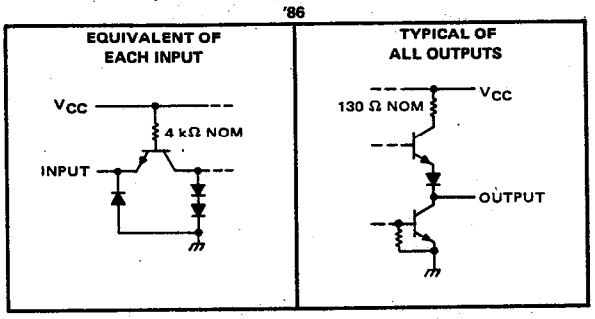
TTL
MSI

TYPES SN5486, SN54L86, SN54LS86, SN54S86, SN7486, SN74L86, SN74LS86, SN74S86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

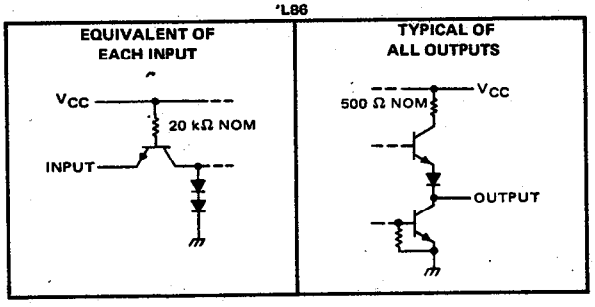
BULLETIN NO. DL-S 7611825, DECEMBER 1972—REVISED OCTOBER 1976

schematics of inputs and outputs

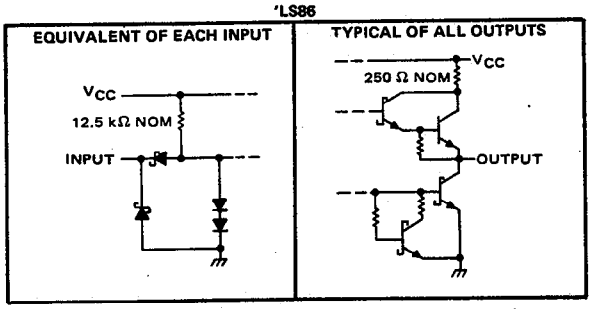
'86



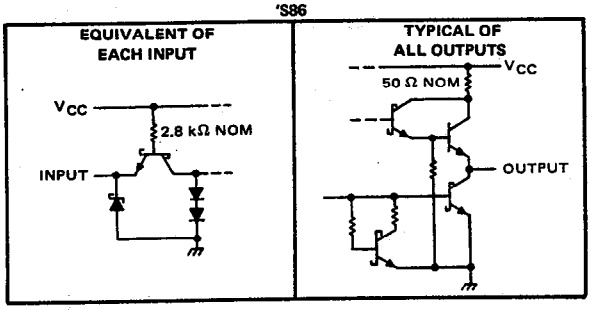
'L86



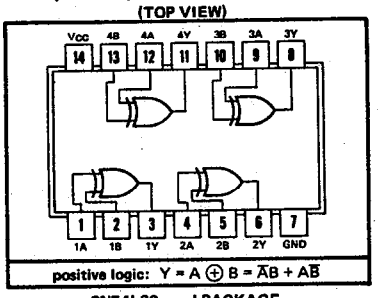
'LS86



'S86

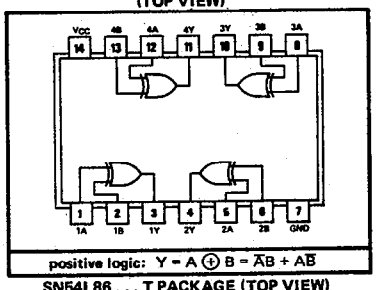


SN54', SN54LS', SN54S' . . . J OR W PACKAGE
SN74', SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)



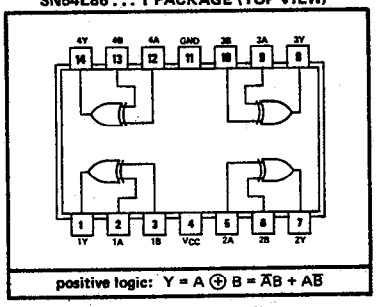
positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

SN54L86 . . . J PACKAGE
SN74L86 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

SN54L86 . . . T PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	55 ns	15 mW
'LS86	10 ns	30.5 mW
'S86	7 ns	250 mW

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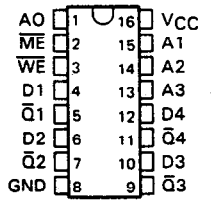
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN7489
64-BIT RANDOM-ACCESS READ/WRITE MEMORY

D1416, DECEMBER 1972—REVISED FEBRUARY 1984

- **For Application as a "Scratch Pad" Memory with Nondestructive Read-Out**
- **Fully Decoded Memory Organized as 16 Words of Four Bits Each**
- **Fast Access Time . . . 33 ns Typical**
- **Diode-Clamped, Buffered Inputs**
- **Open-Collector Outputs Provide Wire-AND Capability**
- **Typical Power Dissipation . . . 375 mW**
- **Compatible with Most TTL Circuits**

SN7489 . . . J OR N PACKAGE
(TOP VIEW)

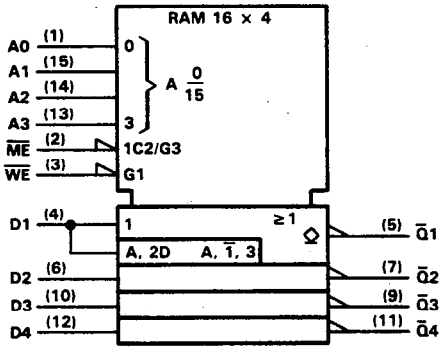


description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wired-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

logic symbol



FUNCTION TABLE

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

write operation

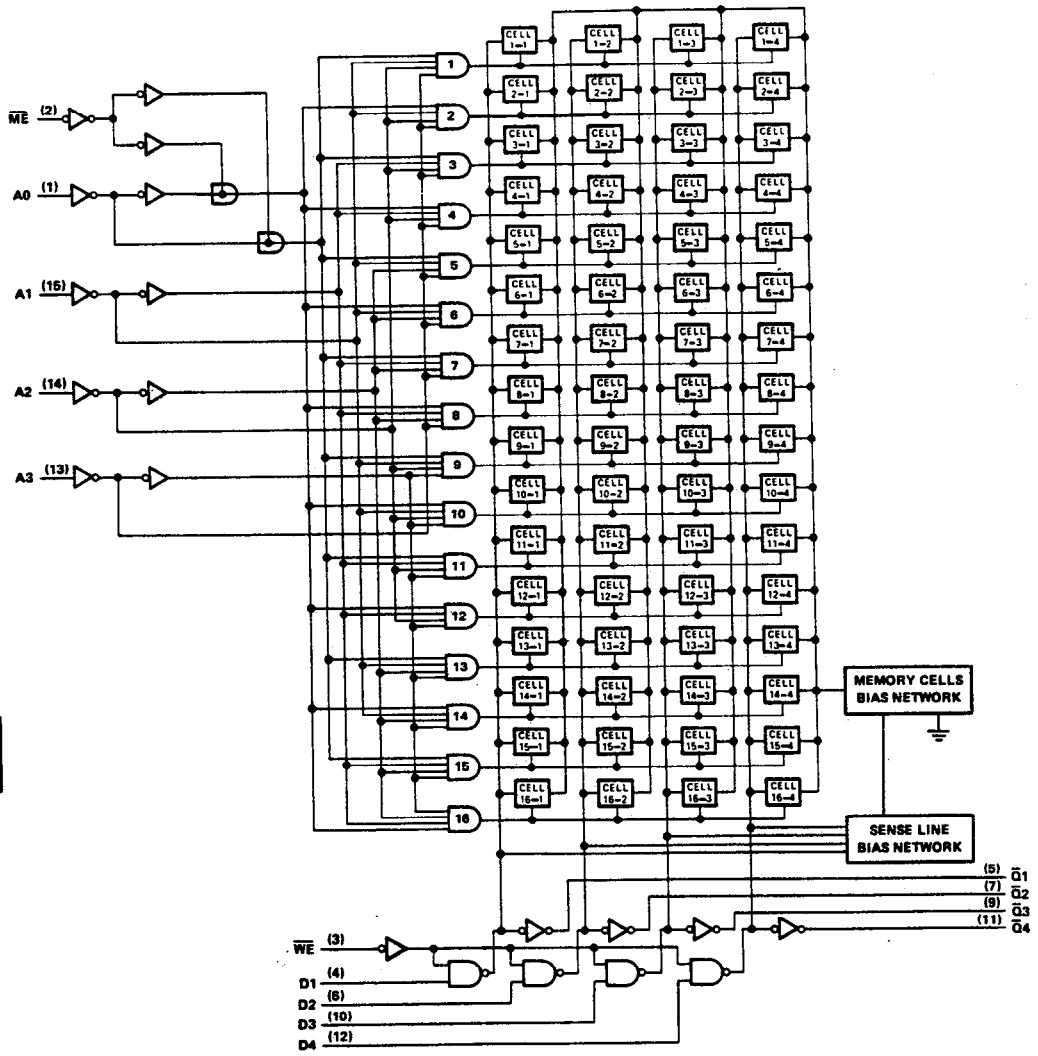
Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

SN7489
64-BIT RANDOM-ACCESS READ/WRITE MEMORY

logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TTL
MSI

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

BULLETIN NO. DL-S 7611807, MARCH 1974—REVISED OCTOBER 1976

'90A, 'L90, 'LS90 . . . DECADE COUNTERS

'92A, 'LS92 . . . DIVIDE-BY-TWELVE COUNTERS

'93A, 'L93, 'LS93 . . . 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW
'L93	16 mW

description

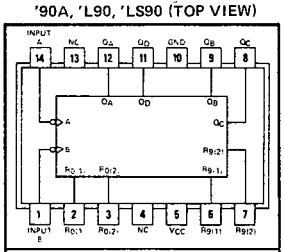
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

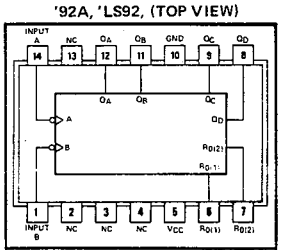
SN54', SN54LS' . . . J OR W PACKAGE
SN54L' . . . J OR T PACKAGE
SN54', SN74L', SN74LS' . . . J OR N PACKAGE

'90A, 'L90, 'LS90 (TOP VIEW)



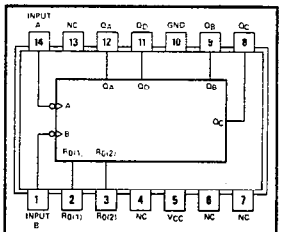
positive logic: see function tables

'92A, 'LS92, (TOP VIEW)



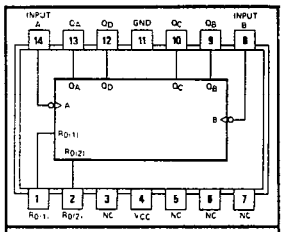
positive logic: see function tables

'93A, 'LS93 (TOP VIEW)



positive logic: see function tables

'L93 (TOP VIEW)



positive logic: see function tables

NC—No internal connection

7

TEXAS INSTRUMENTS
INCORPORATED
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TYPES SN5490A, '92A, '93A, SN54L90, 'L93, SN54LS90, 'LS92, 'LS93, SN7490A, '92A, '93A, SN74L90, 'L93, SN74LS90, 'LS92, 'LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

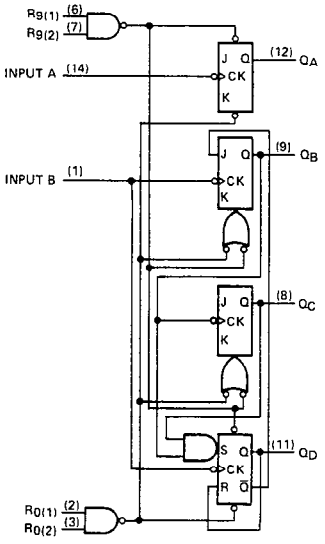
'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

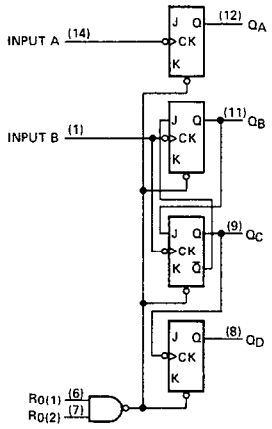
NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

functional block diagrams

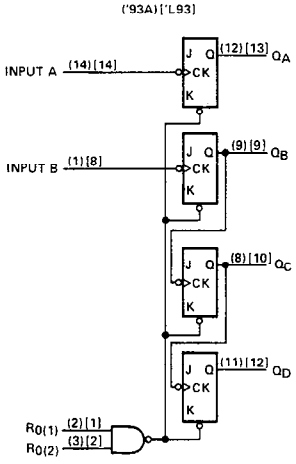
'90A, 'L90, 'LS90



'92A, 'LS92



'93A, 'L93, 'LS93



The J and K inputs shown without connection are for reference only and are functionally at a high level.

TTL
MSI

TYPES SN5495A, SN54L95, SN54LS95B, SN7495A, SN74L95, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7611872, MARCH 1974—REVISED OCTOBER 1976

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'L95	5 MHz	19 mW
'LS95B	36 MHz	65 mW

description

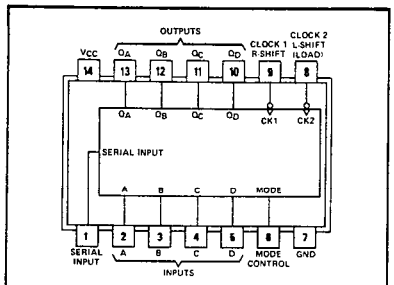
These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

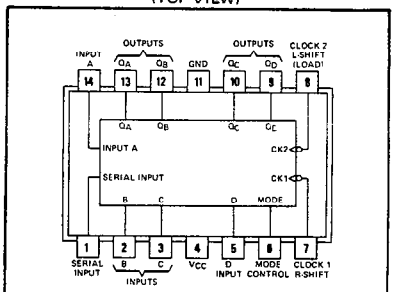
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

SN5495A, SN54LS95B . . . J OR W PACKAGE
SN7495A, SN74LS95B . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54L95 . . . J OR T PACKAGE
SN74L95 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

FUNCTION TABLE

INPUTS								OUTPUTS			
MODE	CLOCKS		SERIAL	PARALLEL							
CONTROL	2 (L)	1 (R)		A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

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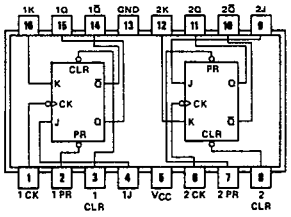
PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

106

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54H106 (J, W) SN74H106 (J, N)

See page 6-52

DUAL J-K FLIP-FLOPS WITH CLEAR

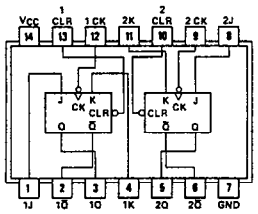
107

'107 FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

'LS107A FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN54107 (J) SN74107 (J, N)
SN54LS107A (J) SN74LS107A (J, N)

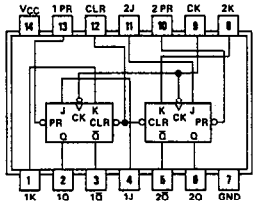
See pages 6-46 and 6-56

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

108

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54H108 (J, W) SN74H108 (J, N)

See page 6-52

See explanation of function tables on page 3-8.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

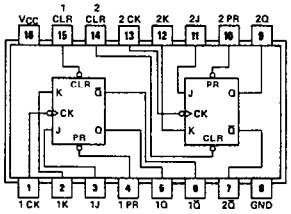
PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

112

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS112A (J, W) SN74LS112A (J,N)
SN54S112 (J, W) SN74S112 (J, N)

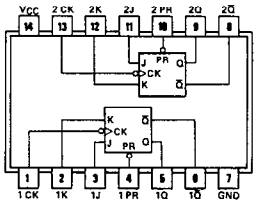
See pages 6-56 and 6-58

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

113

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS113A (J, W) SN74LS113A (J, N)
SN54S113 (J, W) SN74S113 (J, N)

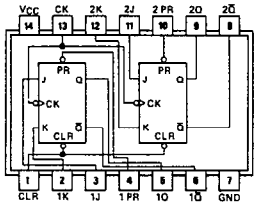
See pages 6-56 and 6-58

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

114

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS114A (J, W) SN74LS114A (J, N)
SN54S114 (J, W) SN74S114 (J,N)

See pages 6-56 and 6-58

See explanation of function tables on page 3-8.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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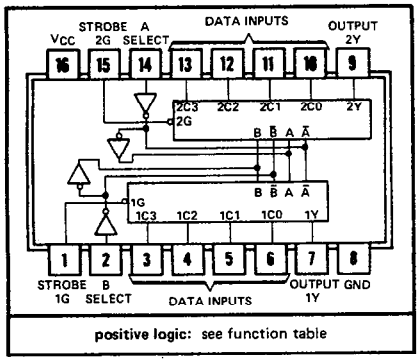
TTL
MSI

TYPES SN54153, SN54L153, SN54LS153, SN54S153, SN74153, SN74L153, SN74LS153, SN74S153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611852, DECEMBER 1972 – REVISED OCTOBER 1976

SN54153, SN54LS153, SN54S153 . . . J OR W PACKAGE
SN54L153 . . . J PACKAGE
SN74153, SN74L153, SN74LS153, SN74S153 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES FROM DATA	FROM STROBE	FROM SELECT	TYPICAL POWER DISSIPATION
'153	14 ns	17 ns	22 ns	180 mW
'L153	27 ns	34 ns	44 ns	90 mW
'LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '153, 'L153, 'S153 . . . . . 5.5 V
'LS153 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611819, DECEMBER 1972—REVISED OCTOBER 1976

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	11 ns	200 mW
'151A	8 ns	145 mW
'152A	8 ns	130 mW
'LS151	11 ns†	30 mW
'LS152	11 ns†	28 mW
'S151	4.5 ns	225 mW

†Tentative data

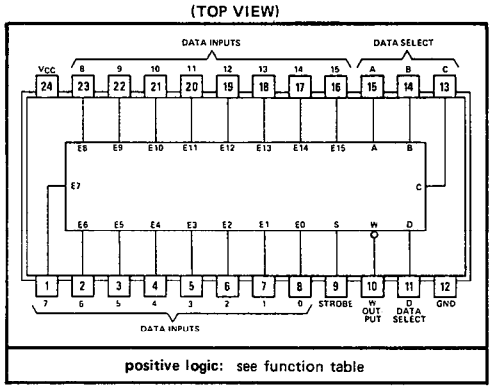
description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

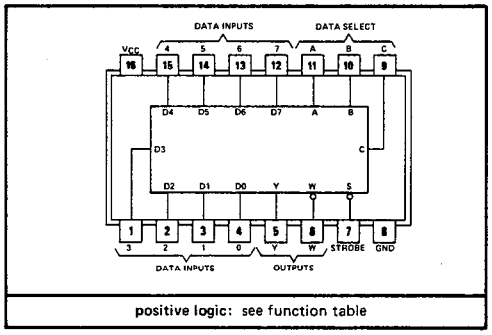
The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

SN54150 . . . J OR W PACKAGE
SN74150 . . . J OR N PACKAGE
(TOP VIEW)



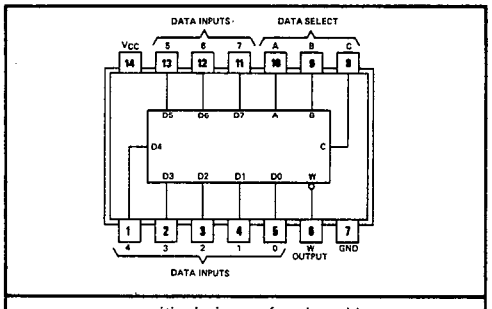
positive logic: see function table

SN54151A, SN54LS151, SN54S151 . . . J OR W PACKAGE
SN74151A SN74LS151, SN74S151 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54152A, SN54LS152 . . . W PACKAGE
(TOP VIEW)



positive logic: see function table

7

TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74L157, SN74LS157, SN74LS158, SN74S157, SN74S158
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7711847, MARCH 1974—REVISED AUGUST 1977

features

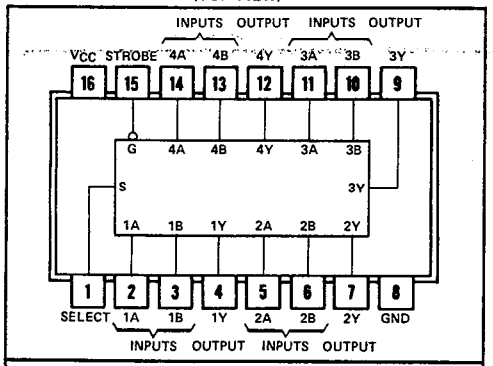
- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

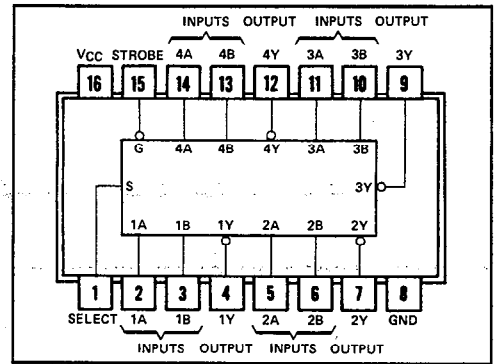
- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

SN54157, SN54LS157, SN54S157 . . . J OR W PACKAGE
SN54L157 . . . J PACKAGE
SN74157, SN74L157, SN74LS157, SN74S157 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74LS158, SN74S158 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '157, 'L157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TTL
MSI

TYPES SN54LS169A, SN54S168, SN54S169
SN74LS169A, SN74S168, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

BULLETIN NO. DL-S 12068, OCTOBER 1976 – REVISED DECEMBER 1980

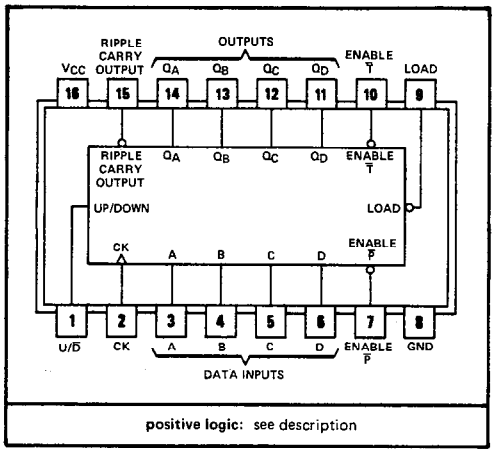
'S168 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS169A, 'S169 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS169A	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW

SERIES SN54LS', SN54S' . . . J OR W PACKAGE
SERIES SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'S168 is a decade counter and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

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1280

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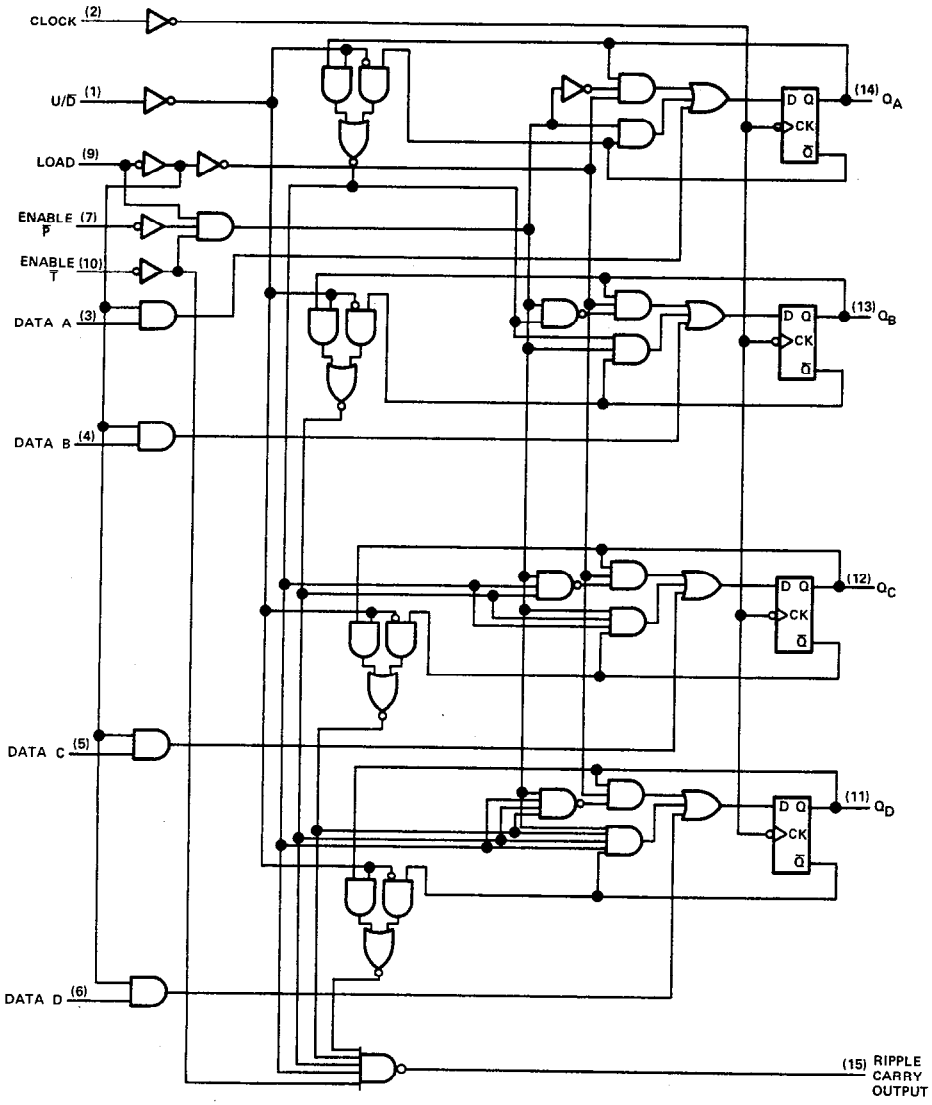
REVISED DECEMBER 1980

functional block diagrams



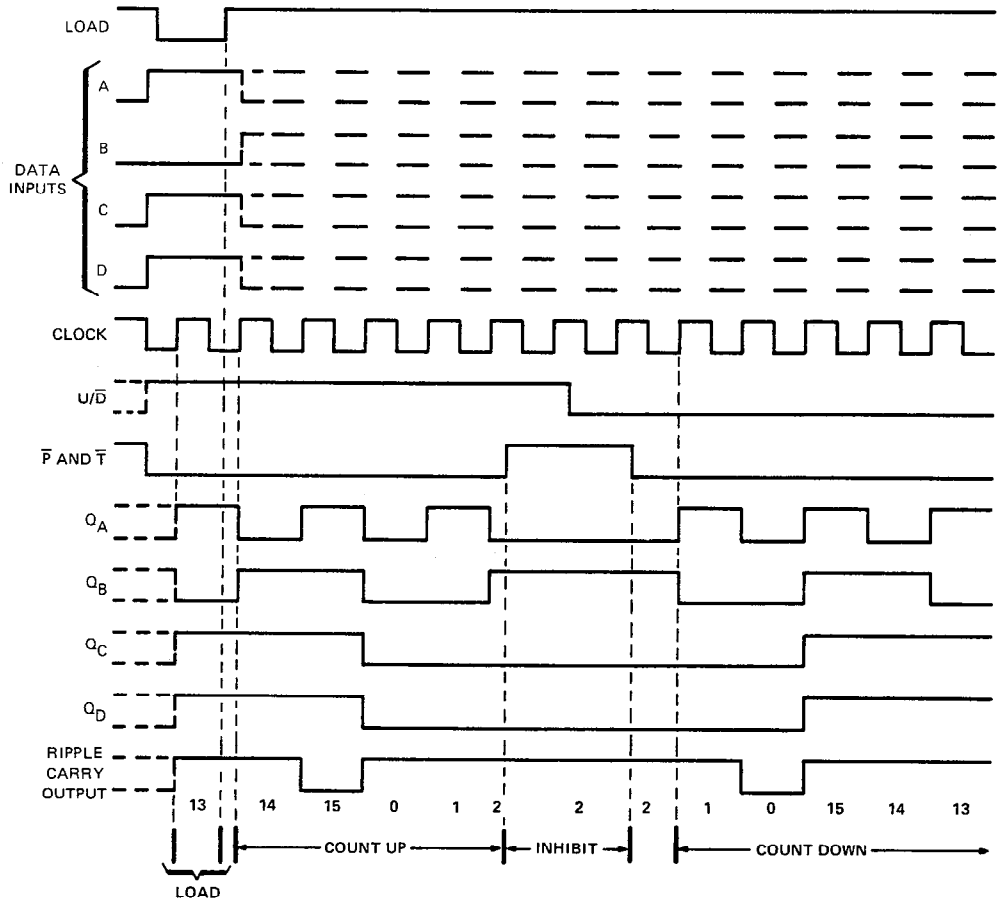
TYPES SN54LS169A, SN54S169, SN74LS169A, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

'LS169A, 'S169 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



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TEXAS INSTRUMENTS
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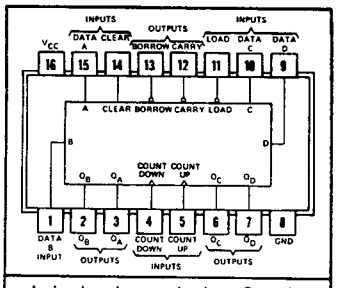
TYPES SN54192, SN54193, SN54L192, SN54L193, SN54LS192, SN54LS193 SN74192, SN74193, SN74L192, SN74L193, SN74LS192, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

BULLETIN NO. DL-S 7711828, DECEMBER 1972—REVISED AUGUST 1977

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'L192, 'L193	7 MHz	43 mW
'LS192, 'LS193	32 MHz	95 mW

SN54', SN54LS' . . . J OR W PACKAGE
SN54L' . . . J PACKAGE
SN74', SN74L', SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



logic: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, 'L192, and 'LS192 circuits are BCD counters and the '193, 'L193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

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These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54L'	SN54LS'	SN74'	SN74L'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	8	7	7	8	7	V
Input voltage	5.5	5.5	7	5.5	5.5	7	V
Operating free-air temperature range	−55 to 125			0 to 70			°C
Storage temperature range	−65 to 150			−65 to 150			°C

NOTE 1: Voltage values are with respect to network ground terminal.

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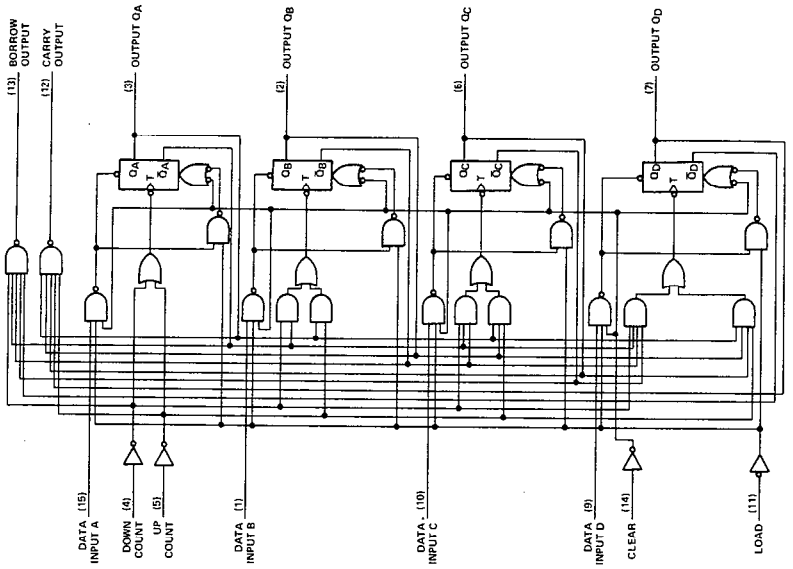
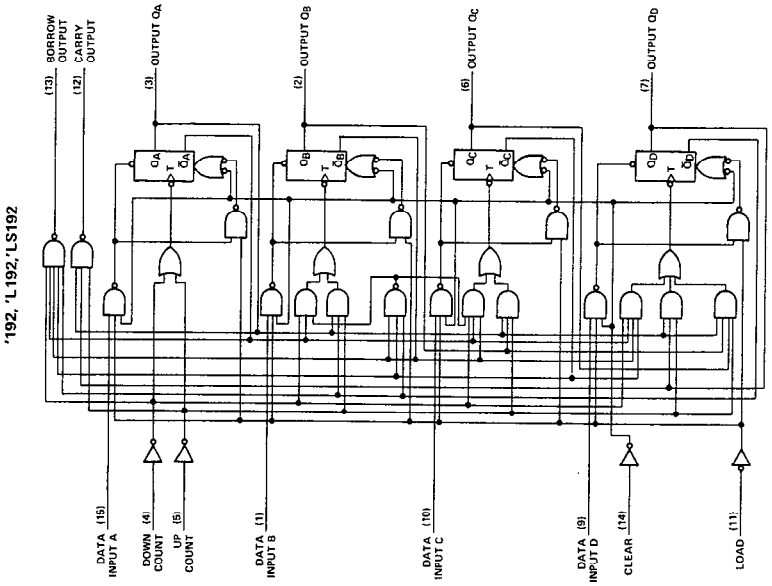
TYPES SN54192, SN54193, SN54L192, SN54L193, SN54LS192, SN54LS193, SN74192, SN74193, SN74L192, SN74L193, SN74LS192, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

functional block diagrams

'193, 'L193, 'LS193



'192, 'L192, 'LS192



⏚ . . . Dynamic input activated by a transition from a high level to a low level.

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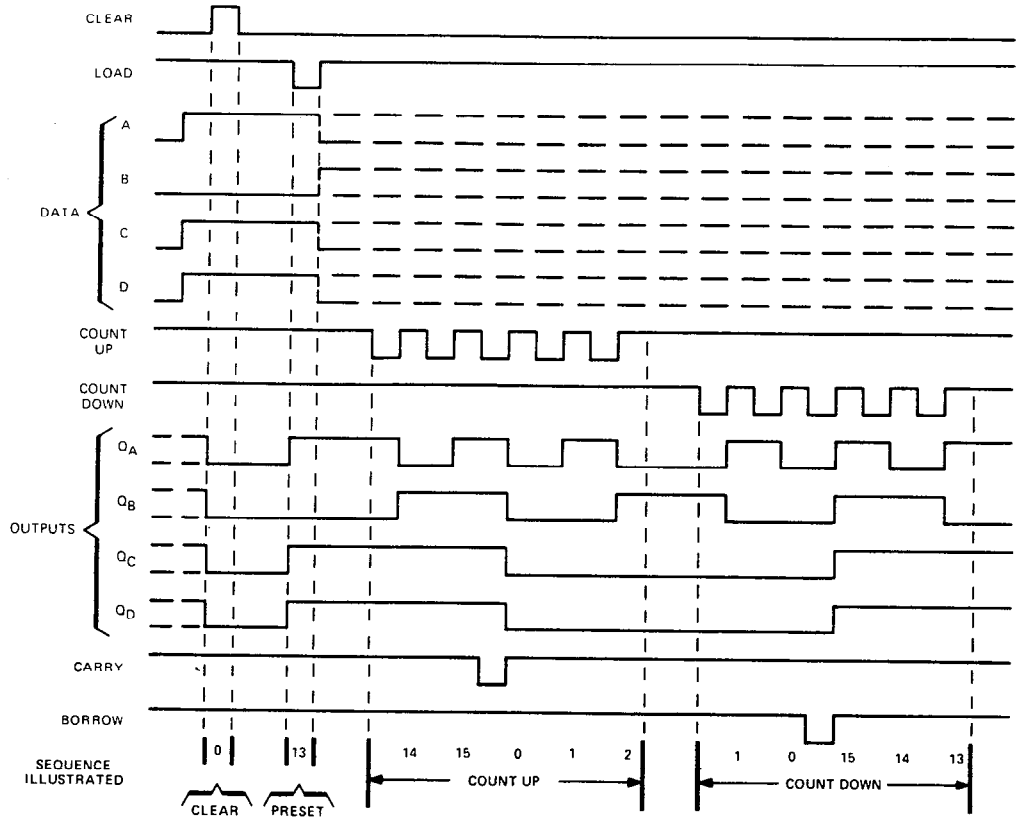
TYPES SN54193, SN54L193, SN54LS193, SN74193, SN74L193, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

'193, 'L193, 'LS193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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MSI

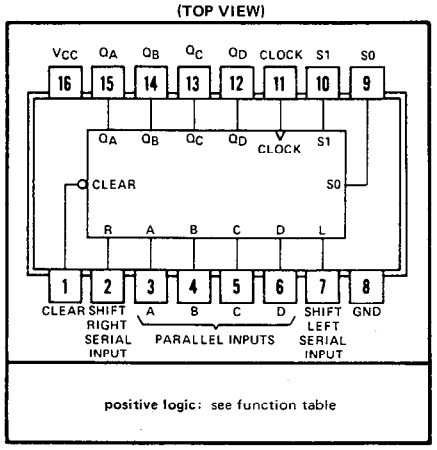
TYPES SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

BULLETIN NO. DL-S 7611866, MARCH 1974–REVISED OCTOBER 1976

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

SN54194, SN54LS194A, SN54S194 . . . J OR W PACKAGE
SN74194, SN74LS194A, SN74S194 . . . J OR N PACKAGE
(TOP VIEW)



description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transistion of the clock input. During loading, serial data flow is inhibited.

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Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

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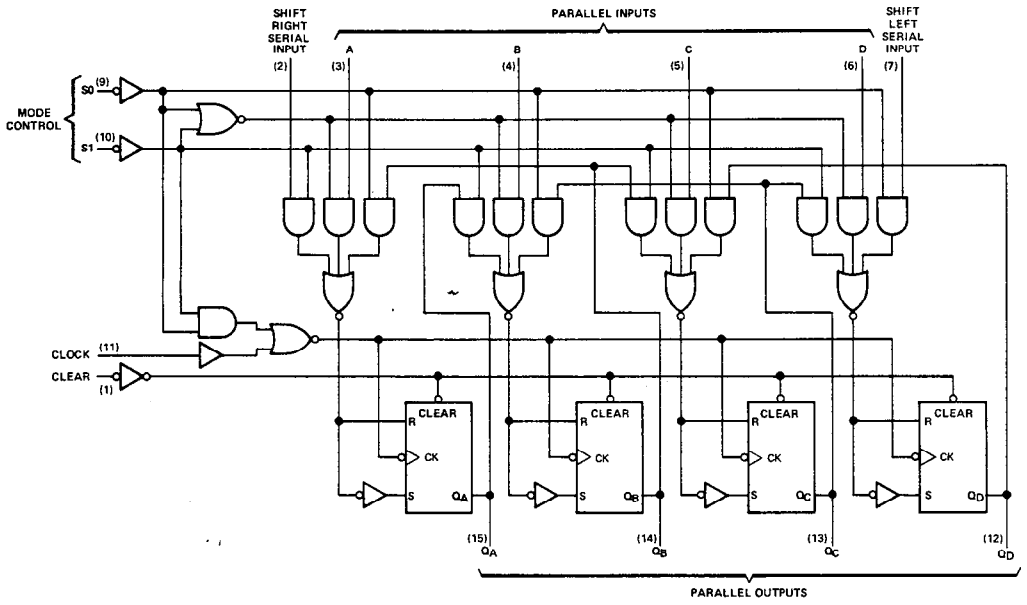
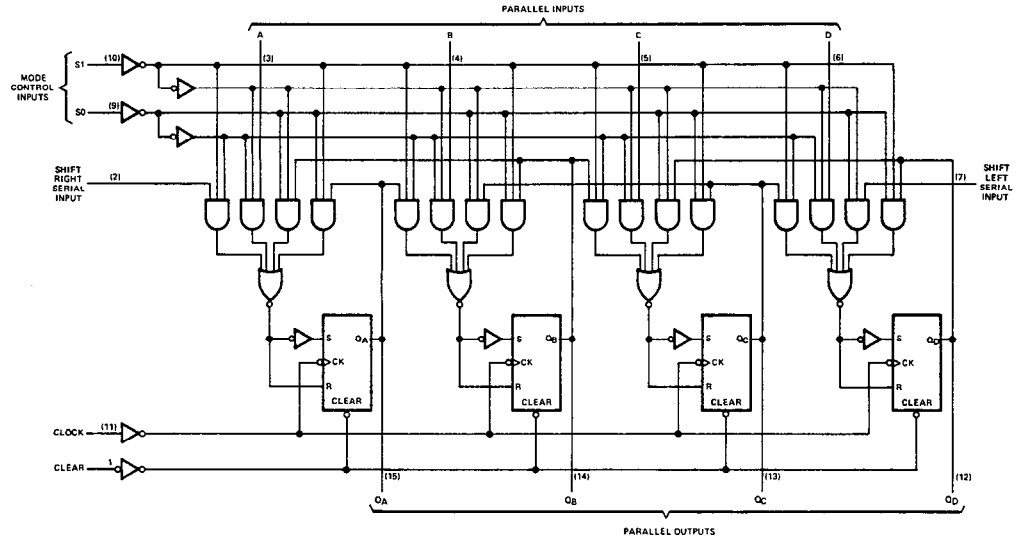
functional block diagrams

'194



'LS194A, 'S194



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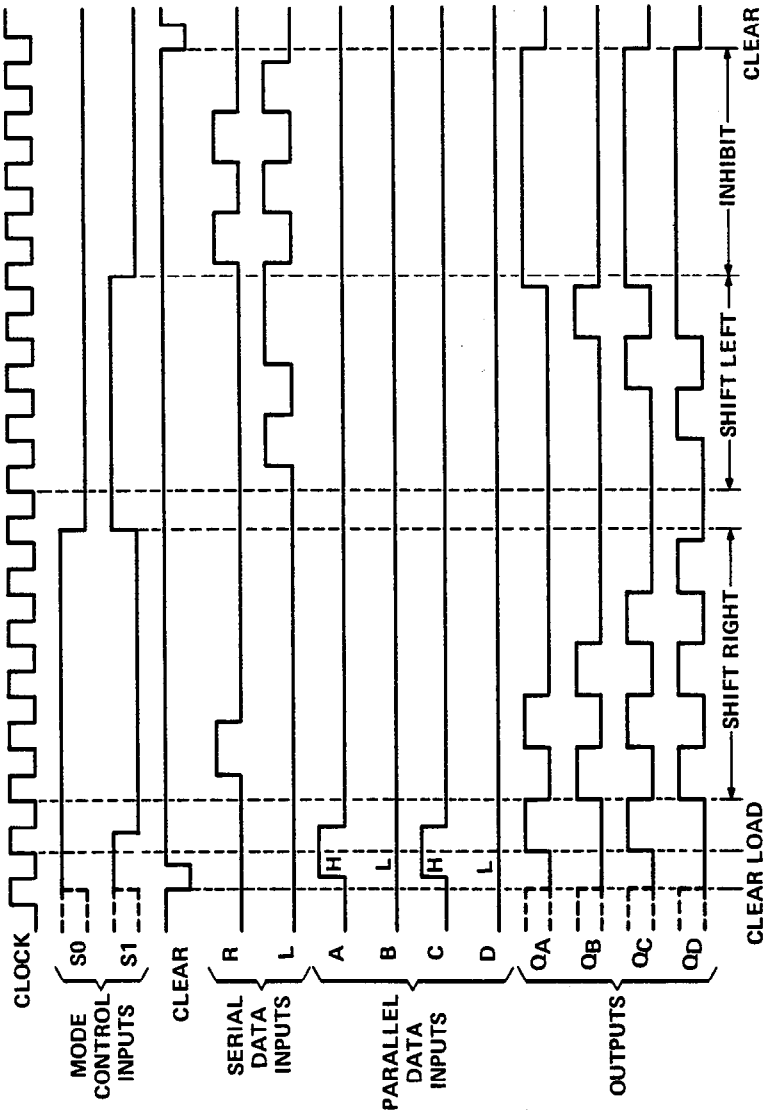
typical clear, load, right-shift, left-shift, inhibit, and clear sequences



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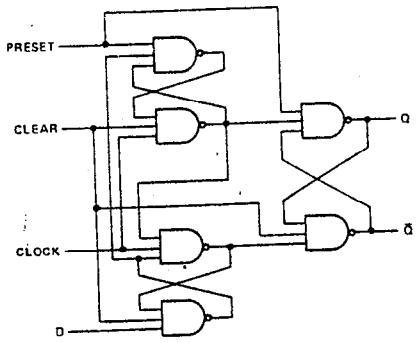
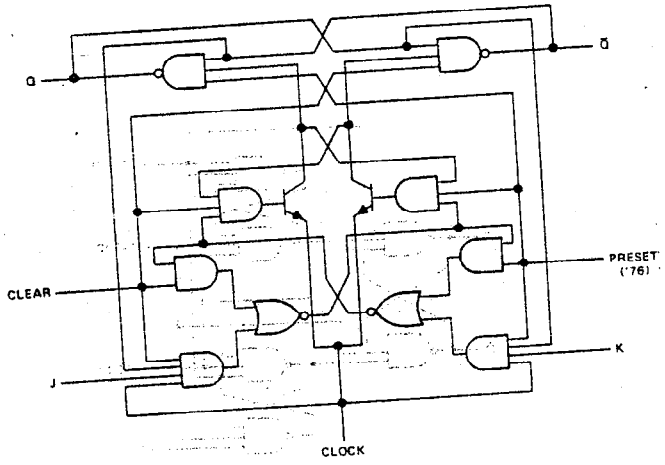
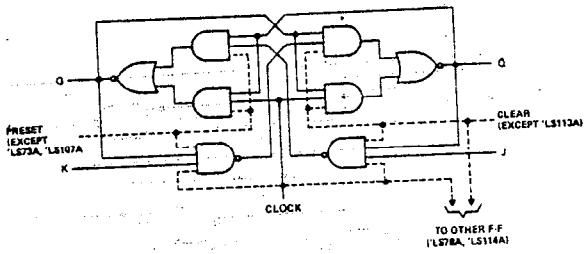


'74—DUAL D WITH CLEAR AND PRESET



'73—DUAL J-K WITH CLEAR
'76—DUAL J-K WITH CLEAR AND PRESET
'107—DUAL J-K WITH CLEAR



'LS73A, 'LS107A—DUAL J-K WITH CLEAR
'LS76A, 'LS112A—DUAL J-K WITH CLEAR AND PRESET
'LS78A, 'LS114A—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK
'LS113A—DUAL J-K WITH PRESET

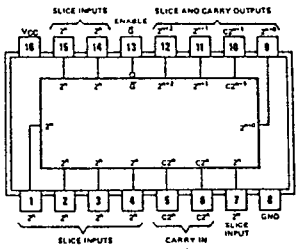
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEW)

7-BIT SLICE WALLACE TREES

275 3-STATE OUTPUTS

See page 7-391

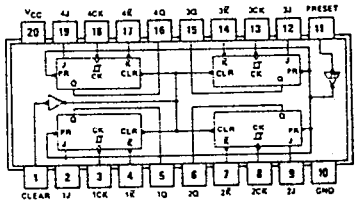


SN54LS275 (J) SN74LS275 (J, N)
SN54S275 (J) SN74S275 (J, N)

QUAD J-$\overline{K}$ FLIP-FLOPS

276 SEPARATE CLOCKS
EDGE-TRIGGERING
COMMON DIRECT CLEAR AND PRESET

See page 7-401

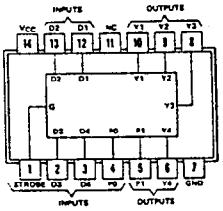


SN54276 (J) SN74276 (J, N)

4-BIT CASCADEABLE PRIORITY REGISTERS

278 LATCHED DATA INPUTS
PRIORITY OUTPUT GATING

See page 7-403



SN54278 (J, W) SN74278 (J, N)

NC — No internal connection

QUAD $\overline{S}$-$\overline{R}$ LATCHES

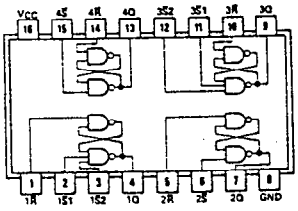
279 DIODE-CLAMPED INPUTS
TOTEM-POLE OUTPUTS

FUNCTION TABLE

INPUTS $\overline{S}$†	INPUTS $\overline{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

See page 6-60



SN54279 (J, W) SN74279 (J, N)
SN54LS279 (J, W) SN74LS279 (J, N)

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