Experiment 1, Introduction Experiment ECE 385

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1 Introduction

In this lab we created a 2-to-1 multiplexer using 4 NAND gates. There are 3 inputs, a, b, and c. B is defined as the select bit when a passes when the select bit 1 and c passes when the select bit 0. Our first circuit had a static hazard that made it not work properly when the select bit changes at a high frequency. Because of this we had to add another NAND gate that fixes this hazard.

2 Component layout sheet

3 Prelab

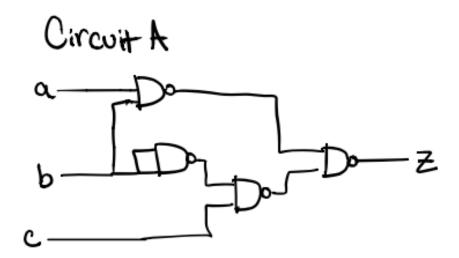


Figure 1: 2 to 1 Mux with a static hazard. This mux is controlled by the select bit defined as B. When B is high then the C input is passed through the multiplexer. When B is low then the A input is passed through the multiplexer.

Circuit B

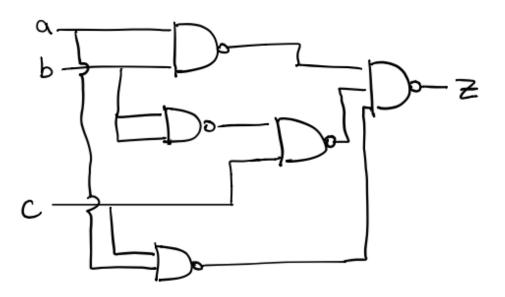


Figure 2: 2 to 1 Mux without a static hazard. This circuit fixes the static hazard by adding an extra NAND gate and changes the last 2 input NAND gate with a 3 input NAND gate. The reason behind this change is because when the select bit is changing quickly there is a gap between the two cases covered by the other NAND gates. This causes the mux to output the wrong values.

4 Oscilloscope outputs

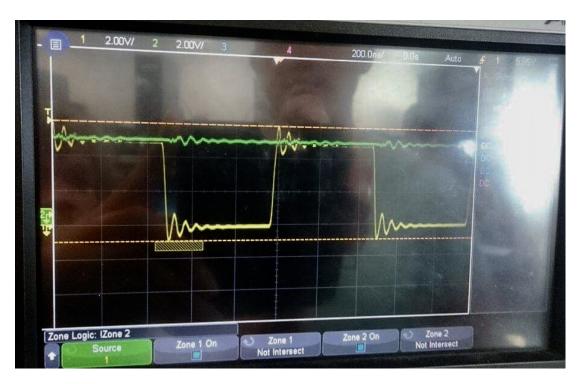


Figure 3: 2 to 1 Mux with the static hazard output on the oscilloscope. This hazard keeps the output value at 1. The green waveform represents the B input, the green waveform represents the output of the circuit



Figure 4: 2 to 1 Mux with a propagation delay. This is the output from circuit B, because of the gates the output lags 20ns behind the value of B. The yellow waveform represents the B input, the green waveform represents the output of the circuit.

5 Postlab

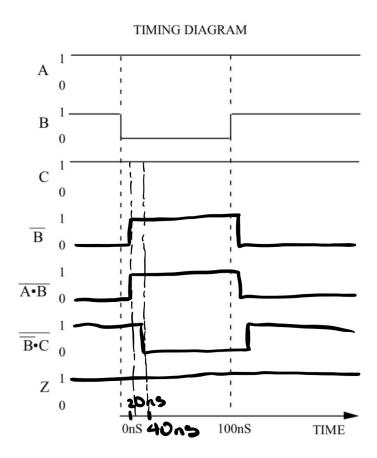


Figure 5: Postlab question 1

5.1 Question 2

6 Documentation

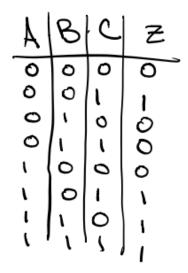


Figure 6: This is the truth table of circuit A and B.

7 Conclusion

Our lab went well overall. We had a couple hiccups in lab but they were mostly silly mistakes such as not hooking up our circuit to power. We ran into a two hour road block because of this when we were testing. Another issue was our 3 input NAND gate was faulty. Other than that, our lab went swimmingly.