ECE 385 Lab 8 Report Outline

❏ **Introduction**
  ❏ Briefly summarize the operation of the USB/VGA interface
❏ **Written Description of Lab 8 System**
  ❏ Written Description of the entire Lab 8 system
    ❏ Describe in words how the NIOS interacts with both the CY7C67200 USB chip and the VGA components
  ❏ Written description of the USB protocol
    ❏ Describe the purpose of the USBRead, USBWrite, IO_read and IO_write functions in the C code
  ❏ Block diagram
    ❏ This diagram should represent the placement of all your modules in the top level. *Please only include the top level diagram and not the RTL view of every module*. The Qsys view of the NIOS processor is not necessary for this portion.
  ❏ Module descriptions
    ❏ A guide on how to do this was shown in the Lab 5 report outline. Do not forget to describe the Qsys generated file for your Nios system! When describing the generated file, you should describe the PIO blocks added beyond those just needed to make the NIOS system run (i.e. the ones needed to communicate with the USB chip).
❏ **Answers to both hidden questions**
  ❏ These can be found in the provided SystemVerilog files.
❏ **Answer to Post Lab Questions**
  ❏ What is the difference between VGA_clk and Clk?
  ❏ In the file io_handler.h, why is it that the otg_hpi_data is defined as an integer pointer while the otg_hpi_r is defined as a char pointer?
  ❏ Document the Design Resources and Statistics in following table.

LUT	
DSP	
Memory (BRAM)	
Flip-Flop	
Frequency	
Static Power	
Dynamic Power	
Total Power	

❏ **Conclusion**

- ❏ Discuss functionality of your design. If parts of your design didn't work, discuss what could be done to fix it
- ❏ Was there anything ambiguous, incorrect, or unnecessarily difficult in the lab manual or given materials which can be improved for next semester? You can also specify what we did right so it doesn't get changed.