General Guide

Part IV – Design Technique

* NAND gate: implemented using less transistors than AND gate.

: any function can be implemented with NAND gate.

* All unused inputs must be tied to some logic level. “*Floating pin*” concept.
* To pull an input to a logic one, a ‘pull-up’ resistor (nominally 1k ohms for 74xxx and 10k for 74LSxxx) must be inserted between the input and the +5V power supply.

\*A single resistor may be used to hold <= 10 input at the logic 1 level.

* All logic gates have a nonzero propagation delay from input to output. Which may lead to glitches in signal.

\*may be detected by the use of timing diagram – when preparing one, always use the worst-case propagation delays.

* “the output of B cannot be guaranteed until T=22ns. C, which B is its input, cannot guarantee its output until 30ns after the value of B is known. So C’s output is unknown for 52ns.”
* OR gate with inputs NOTted = NAND gate.

NAND gates or OR gates with one input going in as two inputs = NOT gate

Part V – Lab Techniques

* Red and only red for +5V wires; and black for GRD.
* Do not ‘daisy chain’. Eg: A1 output to A2, A3 and A4. Daisy chain = A1 link to A2, then another wire from A2 to A3, another from A3 to A4.

Do: 1 to 3.

* Do not run wires tightly over the top of ICs. (For removal if bad).
* A floating input is interpreted as a logic 1. So either ground it or pull it high with a pull-up resistor.

Part VI – Debugging Outside The Lab

* One use of the DIP switch will be to form a switch register. (the pull-up resistor should be used for noise immunity when the switch is open even though TTL interprets floating inputs as logic ‘1’). So, +5V -> 1K ohm -> DIP switch -> GRN.
* Switches like this (employing contact closures), bounce when they are closed or opened. “Contact bounce”. (If a switch is used to clock a counter circuit, the counter may advance several times per flip of the switch).
* Figure 17 – debouncer circuit. How any why it works? (Hint: the