AN4661
Application note

Getting started with STM32F74xxx/STM32F75xxx MCU hardware development

Introduction

This application note is intended for system designers who require an hardware implementation overview of the development board, with focus on features:

- Power supply,
- Package selection,
- Clock management,
- Reset control,
- Boot mode settings,
- Debug management.

This document describes the minimum hardware resources required to develop an application based on the STM32F74xxx/STM32F75xxx devices.

Table 1. Applicable products

Type	Part number
Microcontrollers	STM32F745IE, STM32F745VE, STM32F745IG, STM32F745VG, STM32F745ZE, STM32F745ZG
	STM32F746VG, STM32F746ZG, STM32F746IG, STM32F746BG, STM32F746NG, STM32F746IE, STM32F746VE, STM32F746ZE, STM32F746BE, STM32F746NE
	STM32F756VG, STM32F756ZG, STM32F756IG, STM32F756BG, STM32F756NG

Contents

List of tables

List of figures

1 Power supplies

1.1 Introduction

The device requires a 1.8 to 3.6 V operating voltage supply (V_{DD}), which can be reduced down to 1.7 V with PDR OFF, as detailed in the product datasheets. The embedded linear voltage regulator is used to supply the internal 1.2 V digital power.

The real-time clock (RTC), the RTC backup registers, and the backup SRAM (BKP SRAM) can be powered from the V_{BAT} voltage when the main V_{DD} supply is powered off.

1.1.1 Independent A/D converter supply and reference voltage

To improve the conversion accuracy, the ADC has an independent power supply which can be separately filtered and shielded from noise on the PCB.

- The ADC voltage supply input is available on a separate V_{DDA} pin.
- An isolated supply ground connection is provided on pin V_{SSA}.

To ensure a better accuracy of low voltage inputs, the user can connect a separate external reference voltage ADC input on V_{REF}. The voltage on V_{REF} ranges from 1.8 V to V_{DDA}.

When available (depending on package), $V_{REF\_}$ must be externally tied to V_{SSA}.

1.1.2 Independent USB transceivers supply

The USB transceivers are supplied from a separated V_{DDUSB} power supply pin.

V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to *Figure 1* and *Figure 2*). For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions V_{DDUSB} must be respected:

- During power-on phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- V_{DDSUB} rising and falling time rate specifications must be respected (refer to *operating conditions at power-up / power-down (regulator ON)* table and *operating conditions at power-up / power-down (regulator OFF) t*able of STM32F74xxx/STM32F75xxx datasheet).
- In operating mode phase, V_{DDUSB} could be lower or higher than V_{DD}:
  - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.
  - The V_{DDUSB} supply both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB}.
  - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Figure 1. V_{DDUSB} connected to V_{DD} power supply

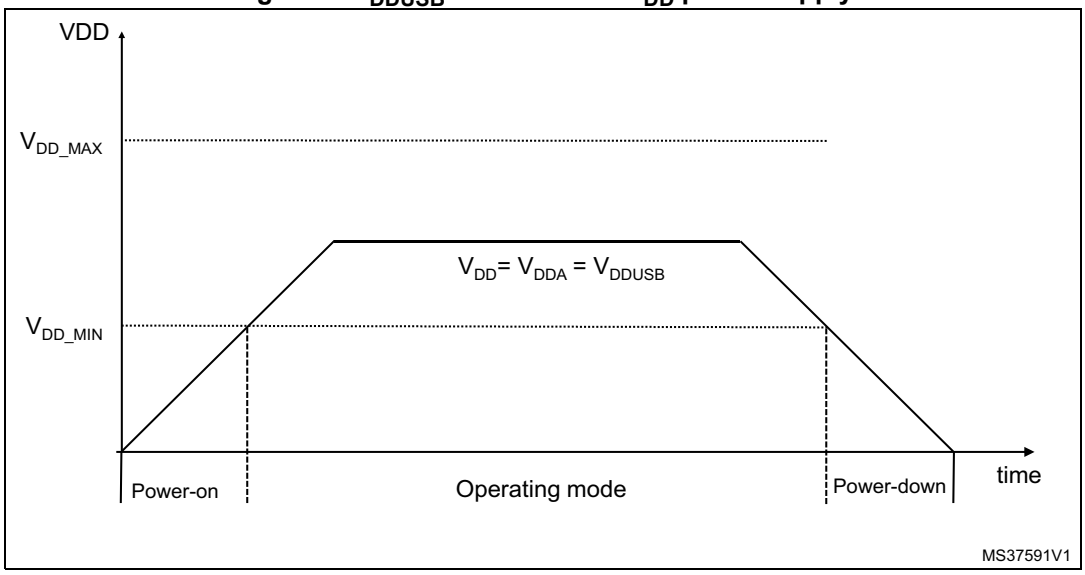
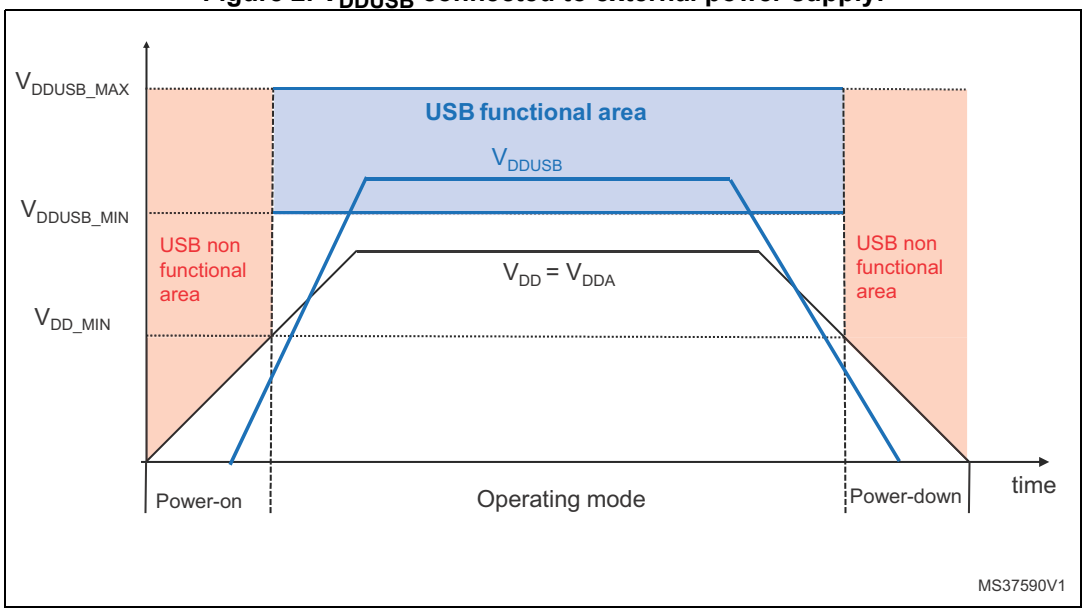


Figure 2. V_{DDUSB} connected to external power supply.



1.1.3 Battery backup domain

Backup domain description

To retain the content of the RTC backup registers, backup SRAM, and supply the RTC when V_{DD} is turned off, V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or by another source.

When the backup domain is supplied by V_{BAT} (analog switch connected to V_{BAT} because V_{DD} is not present), the following functions are available:

- PC14 and PC15 can be used as LSE pins only.
- PC13 can be used as tamper pin (TAMP1).
- PI8 can be used as tamper pin (TAMP2).

1.1.4 Voltage regulator

The voltage regulator is always enabled after reset. It works in three different modes depending on the application modes.

- In Run mode, the regulator supplies full power to the 1.2 V domain (core, memories and digital peripherals).
- In Stop mode, the regulator supplies low power to the 1.2 V domain, preserving the contents of the registers and SRAM.
- In Standby mode, the regulator is powered down. The contents of the registers and SRAM are lost except for those concerned with the standby circuitry and the backup domain.

Note: Depending on the selected package, there are specific pins that should be connected either to V_{SS} or V_{DD} to activate or deactivate the voltage regulator. Refer to the voltage regulator section in the datasheet for more details.

1.2 Power supply scheme

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins. The V_{DD} pins must be connected to V_{DD} with external decoupling capacitors: one single tantalum or ceramic capacitor (min. 4.7 µF) for the package + one 100 nF ceramic capacitor for each V_{DD} pin.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

  The V_{DDA} pin must be connected to two external decoupling capacitors (100 nF ceramic + 1 µF tantalum or ceramic).
- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers. For example, when the device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB}.

  The V_{DDUSB} pin must be connected to two external decoupling capacitors (100 nF ceramic + 1 µF tantalum or ceramic).
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

  The V_{BAT} pin can be connected to the external battery (1.65 V < V_{BAT} < 3.6 V). If no external battery is used, it is recommended to connect this pin to V_{DD} with a 100 nF external ceramic decoupling capacitor.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 1.3.5: Internal reset OFF).

- The V_{REF+} pin can be connected to the V_{DDA} external power supply. If a separate, external reference voltage is applied on V_{REF+}, a 100 nF and a 1 µF capacitors must be

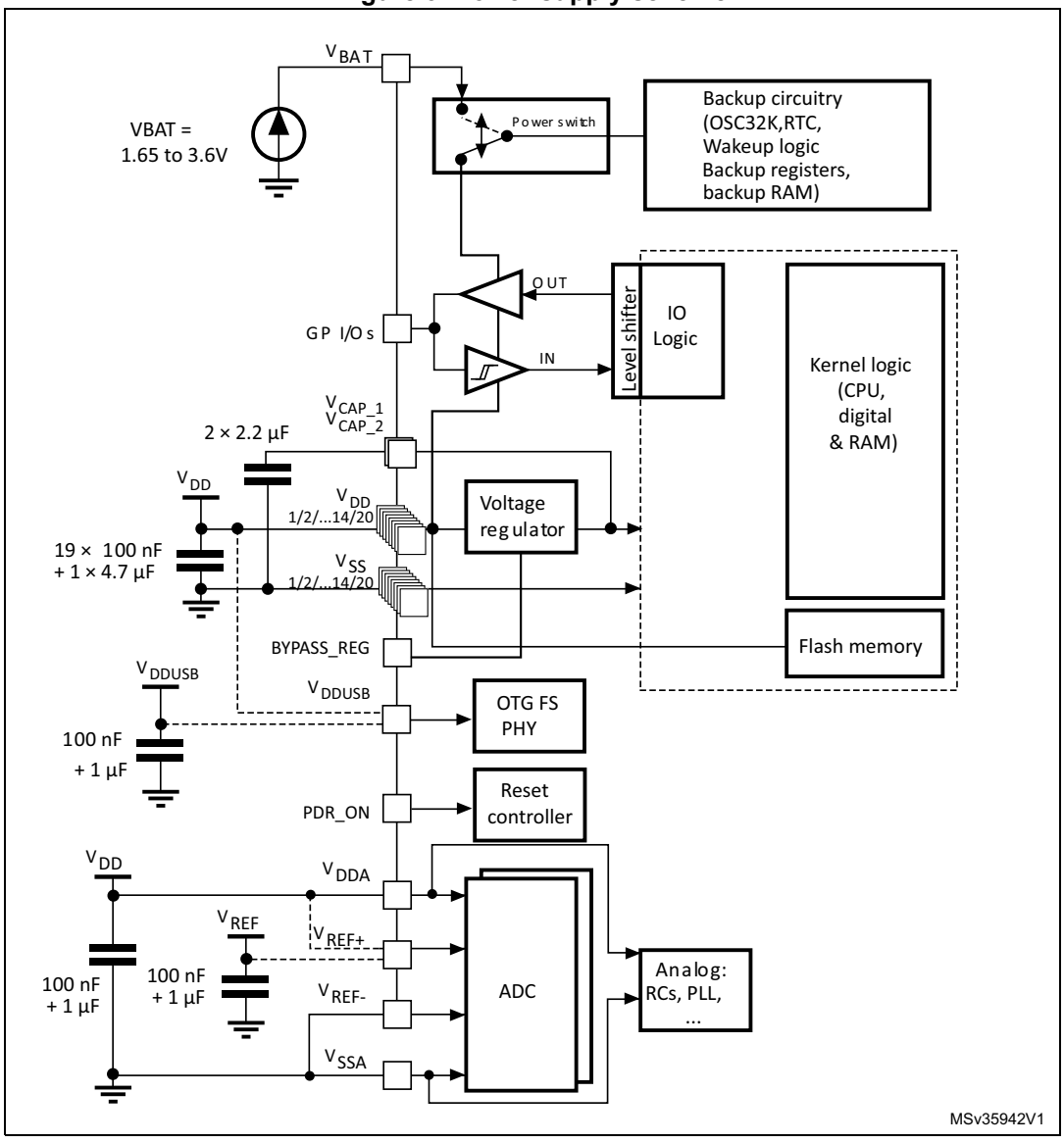
connected on this pin. In all cases, V_{REF+} must be kept between (V_{DDA}-1.2 V) and V_{DDA} with minimum of 1.7 V.

- Additional precautions can be taken to filter analog noise:
  - V_{DDA} can be connected to V_{DD} through a ferrite bead.
  - The V_{REF+} pin can be connected to V_{DDA} through a resistor (typ. 47 Ω).
- For the voltage regulator configuration, there is specific BYPASS_REG pin (not available on all packages) that should be connected either to V_{SS} or V_{DD} to activate or deactivate the voltage regulator specific.

Note: Refer to the voltage regulator section of the related device datasheet for more details.

- When the voltage regulator is enabled, VCAP1 and VCAP2 pins must be connected to 2*2.2 µF low ESR < 2Ω ceramic capacitor.

Figure 3. Power supply scheme



1. Optional. If a separate, external reference voltage is connected on V_{REF+}, the two capacitors (100 nF and 1

µF) must be connected.

2. V_{REF+} is either connected to V_{REF+} or to V_{DDA} (depending on package).
3. V_{REF-} is either connected to V_{REF-} or to V_{SSA} (depending on package).
4. 19 is the number of V_{DD} and V_{SS} inputs.
5. Refer to *Section 1.3.7: Regulator ON/OFF and internal reset ON/OFF availability* to connect BYPASS_REG and PDR_ON pins.

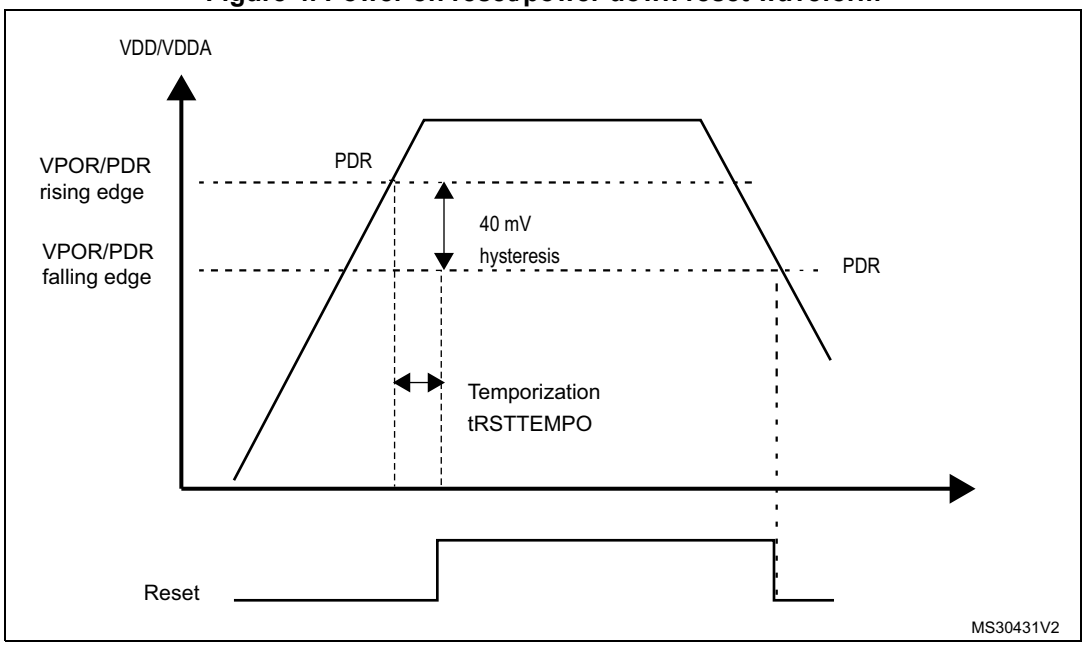
1.3 Reset & power supply supervisor

1.3.1 Power-on reset (POR)/power-down reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from 1.8 V.

The device remains in reset mode when V_{DD}/V_{DDA} is below a specified threshold, VPOR/PDR, without the need for an external reset circuit. For more details concerning the power on/power-down reset threshold, refer to the electrical characteristics of the datasheet.

Figure 4. Power on reset/power down reset waveform



1. tRSTTEMPO is approximately 2.6 ms. VPOR/PDR rising edge is 1.74 V (typ.) and VPOR/PDR falling edge is 1.70 V (typ.). Refer to STM32F756xx datasheets for the actual value.

On the packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

1.3.2 Programmable voltage detector (PVD)

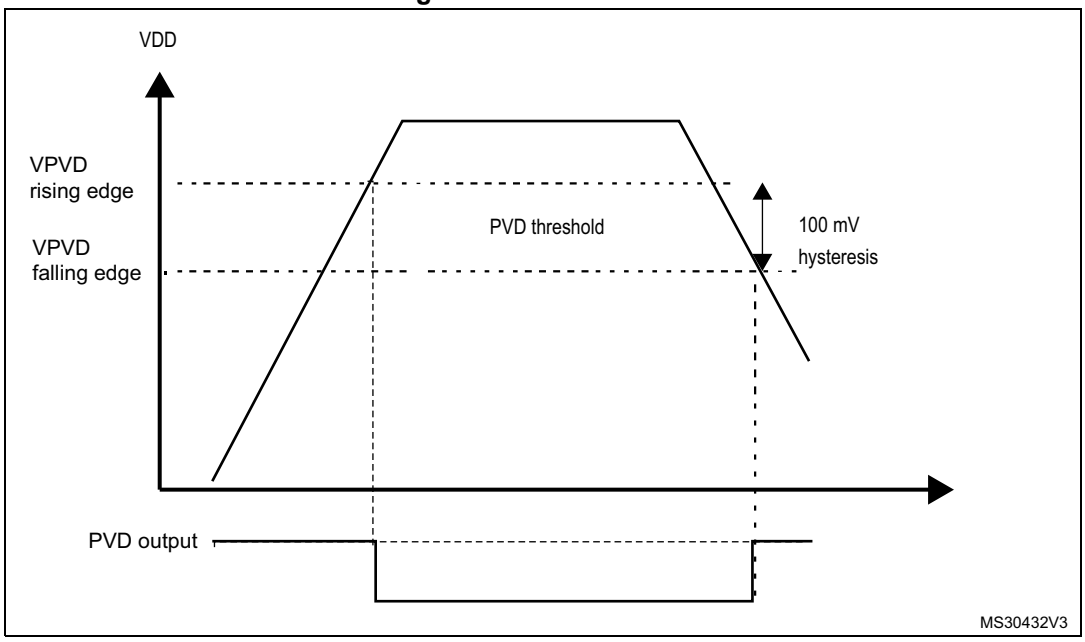
The PVD can be used to monitor the V_{DD} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the PWR power control register (PWR_CR1).

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the PWR power control/status register (PWR_CSR1), to indicate if V_{DD} is higher or lower than the PVD threshold. This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers.

The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example the service routine could perform emergency shutdown tasks.

Figure 5. PVD threshold



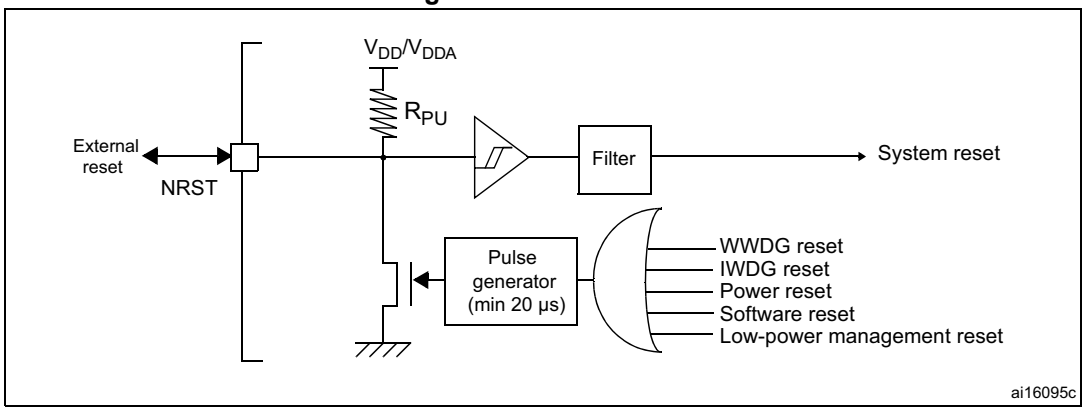
1.3.3 System reset

A system reset sets all the registers to their reset values except the reset flags in the clock controller CSR register and the registers in the backup domain (see *Figure 6*).

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset).
2. Window watchdog end of count condition (WWDG reset).
3. Independent watchdog end of count condition (IWDG reset).
4. A software reset (SW reset) (see software reset).
5. Low-power management reset (see Low-power management reset).

Figure 6. Reset circuit



1.3.4 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

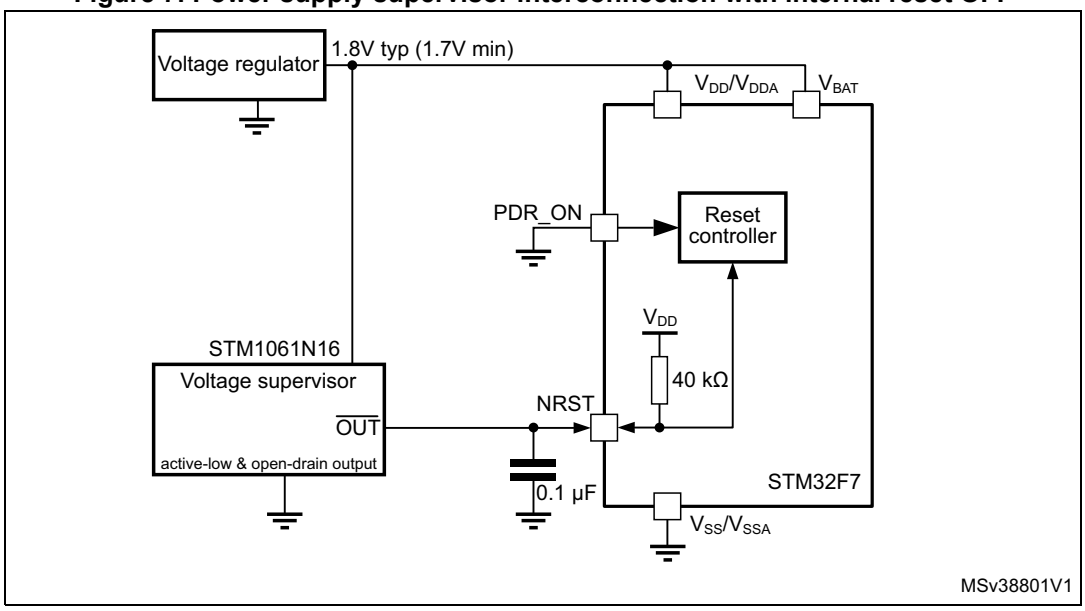
For more details about the internal reset ON, refer to the datasheets (DS10915, DS10916).

1.3.5 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to V_{SS}. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 7. Power supply supervisor interconnection with internal reset OFF



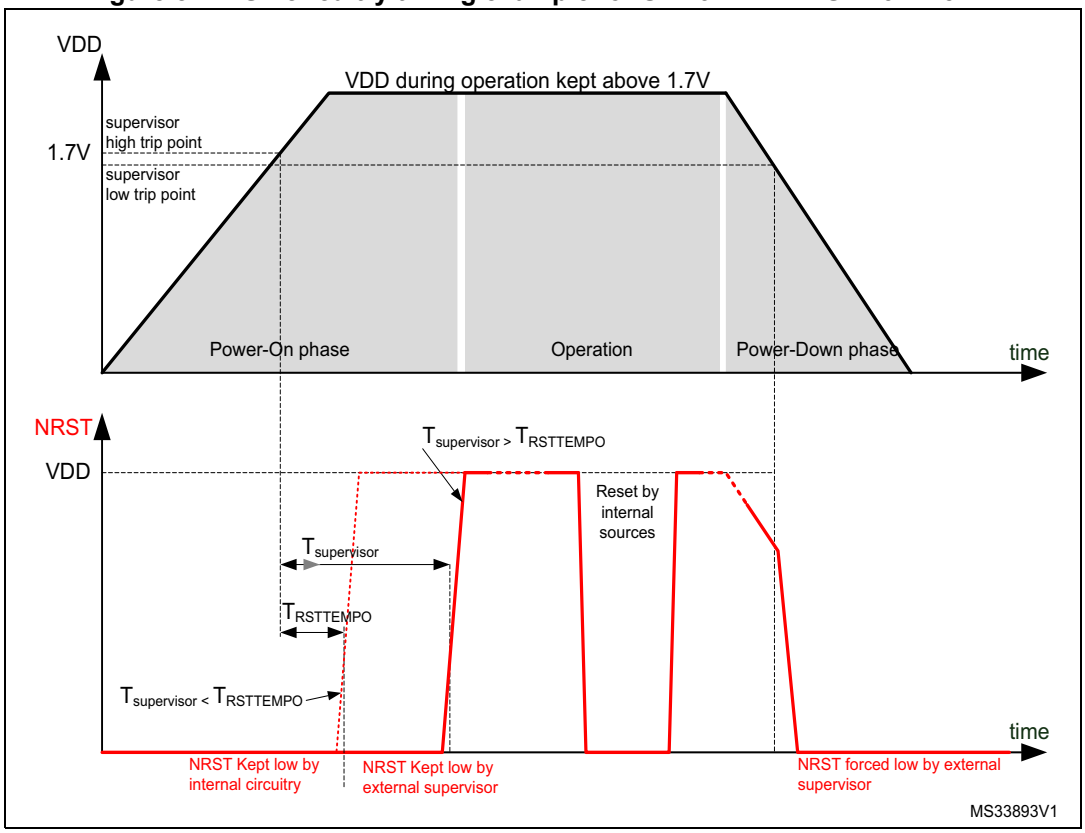
The supply ranges which never go below 1.8V minimum should be better managed by the internal circuitry (no additional component needed, thanks to the fully embedded reset controller).

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All the packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal when connected to V_{SS}.

Figure 8. NRST circuitry timing example for STM32F74xxx/STM32F75xxx



1.3.6 Regulator OFF mode

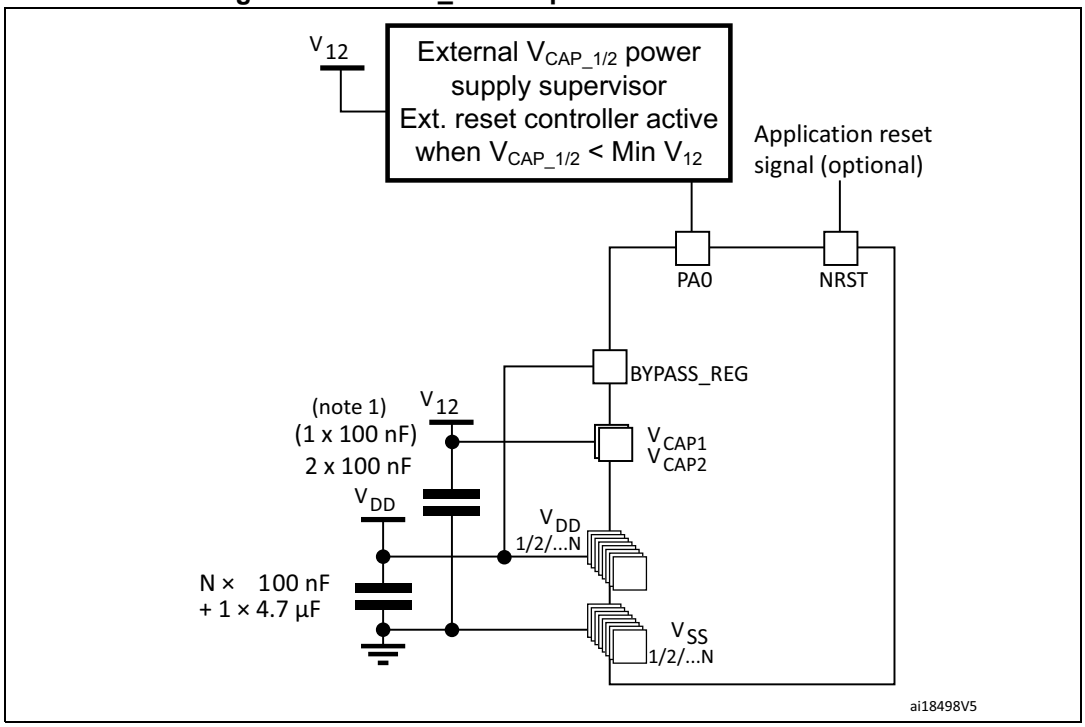
Refer to “Voltage regulator” section in the datasheet for details.

- When BYPASS_REG = V_{DD}, the core power supply should be provided through V_{CAP1} and V_{CAP1} pins connected together.
  - The two V_{CAP} ceramic capacitors should be replaced by two 100 nF decoupling capacitors.
  - Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.
  - When the internal regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the

logic power domain (V_{CAP}).
PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

- In regulator OFF mode, the following features are no more supported:
  - PA0 cannot be used as a GPIO pin since it allows to reset a part of the V12 logic power domain which is not reset by the NRST pin.
  - As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
  - The over-drive and under-drive modes are not available.
  - The Standby mode is not available.

Figure 9. BYPASS_REG supervisor reset connection



1. V_{CAP2} is not available on all packages. In that case, a single 100 nF decoupling capacitor is connected to V_{CAP1}

The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP} to avoid current injection between power domains.
- If the time for V_{CAP} to reach V12 minimum value is smaller than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP} reaches V12 minimum value and until V_{DD} reaches 1.7 V.
- Otherwise, if the time for V_{CAP} to reach V12 minimum value is smaller than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally.
- If V_{CAP} goes below V12 minimum value and V_{DD} is higher than 1.7 V, then PA0 must be asserted low externally.

1.3.7 Regulator ON/OFF and internal reset ON/OFF availability

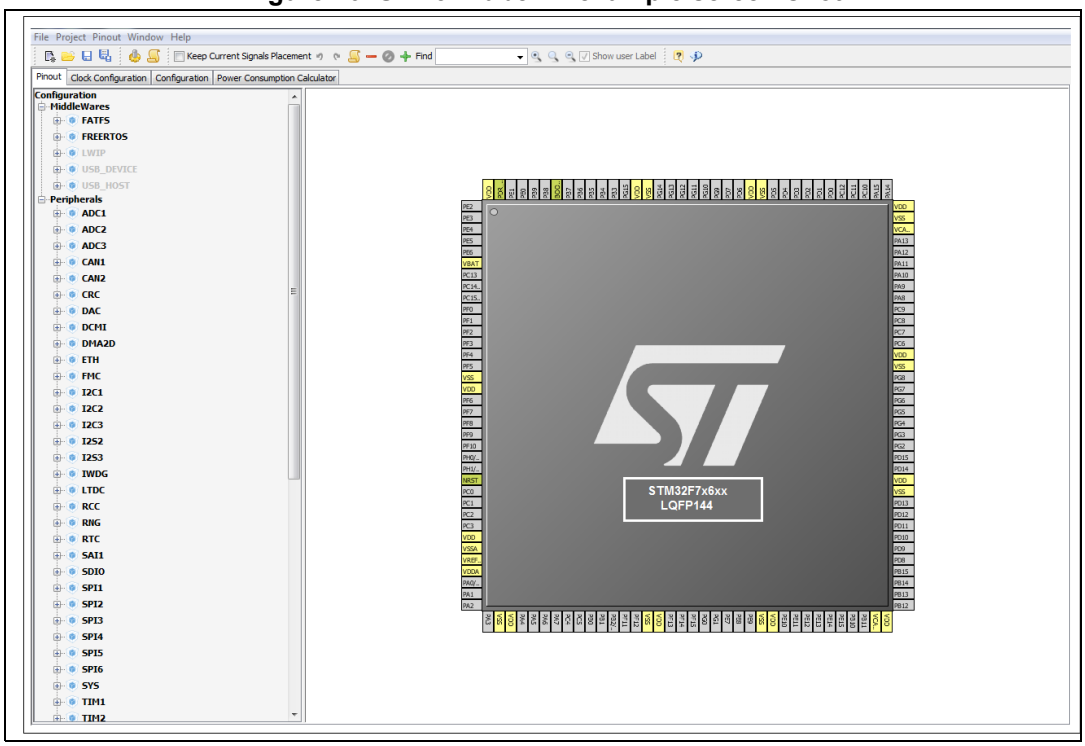
Table 2. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP100	Yes	No	Yes	No
LQFP144, LQFP208			Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP176, WLCSP143, UFBGA176, TFBGA216	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

2 Alternate function mapping to pins

In order to easily explore peripheral alternate functions mapping to pins it is recommended to use the STM32CubeMX tool available on *www.st.com*.

Figure 10. STM32CubeMX example screen-shot



3 Clocks

Three different clock sources can be used to drive the system clock (SYSCLK):

- HSI oscillator clock.
- HSE oscillator clock.
- Main PLL (PLL) clock.

The devices have the two following secondary clock sources:

- 32 kHz low-speed internal RC (LSI RC) which drives the independent watchdog and, optionally, the RTC used for Auto-wakeup from the Stop/Standby mode.
- 32.768 kHz low-speed external crystal (LSE crystal) which optionally drives the RTC clock (RTCCLK).

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

Refer to the RM0385 reference manual for the description of the clock tree.

3.1 HSE OSC clock

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external user clock (see *Figure 11*).
- HSE external crystal/ceramic resonator (see *Figure 12*).

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Figure 11. HSE external clock

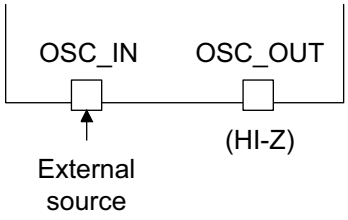
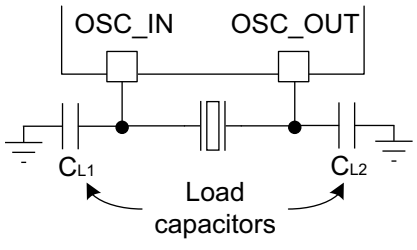


Figure 12. HSE crystal/ceramic resonators



3.1.1 External user clock (HSE bypass)

In this mode, an external clock source must be provided. The user selects this mode by setting the HSEBYP and HSEON bits in the RCC clock control register (RCC_CR). The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC_IN pin while the OSC_OUT pin should be left HI-Z.

3.1.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from 4 to 26 MHz. The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in *Figure 12*. Using a 25 MHz oscillator frequency is a good choice to get accurate Ethernet, USB OTG high-speed peripheral, I2S and SAI.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF-to-25 pF range (typ.), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. CL1 and CL2, are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of CL1 and CL2. The PCB and MCU pin capacitances must be included when sizing CL1 and CL2 (10 pF can be used as a rough estimate of the combined pin and board capacitance).

The HSERDY flag in the RCC clock control register (RCC_CR) indicates if the high-speed external oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIR).

The HSE crystal can be switched on and off using the HSEON bit in the RCC clock control register (RCC_CR).

3.2 LSE OSC clock

The low-speed external clock signal (LSE) can be generated from two possible clock sources:

- LSE user external clock (see *Figure 13*).
- LSE external crystal/ceramic resonator (see *Figure 14*).

Figure 13. LSE external clock

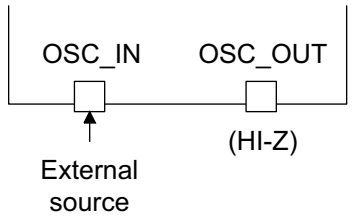
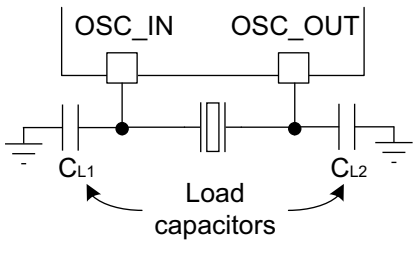


Figure 14. LSE crystal/ceramic resonators



1. *Figure 14: LSE crystal/ceramic resonators*:
   To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤ 7 pF.
2. *Figure 13: LSE external clock* and *Figure 14: LSE crystal/ceramic resonators*:
   OSC32_IN and OSC32_OUT pins can be used also as GPIO, but it is recommended not to use them as both RTC and GPIO pins in the same application.

The LSE oscillator is switched on and off using the LSEON bit in RCC backup domain control register (RCC_BDCR).

The LSE oscillator includes new modes and has a configurable drive using the LSEDRV [1:0] in RCC_BDCR register:

- 00: Low drive.
- 10: Medium low drive.
- 01: Medium high drive.
- 11: High drive.

The LSERDY flag in the RCC backup domain control register (RCC_BDCR) indicates if the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the RCC clock interrupt register (RCC_CIR).

3.2.1 External clock (LSE bypass)

In this mode, an external clock source must be provided. It must have a frequency up to 1 MHz. The user selects this mode by setting the LSEBYP and LSEON bits in the RCC backup domain control register (RCC_BDCR). The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin should be left HI-Z. See *Figure 13*.

3.2.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

3.3 Clock security system (CSS)

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

- If a failure is detected on the HSE clock, this oscillator is automatically disabled, a clock failure event is sent to the break inputs of advanced-control timers TIM1 and TIM8, and an interrupt is generated to inform the software about the failure (clock security system interrupt CSSI), allowing the MCU to perform rescue operations. The CSSI is linked to the Cortex®-M7 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator is used directly or indirectly as the system clock (indirectly meaning that it is directly used as PLL input clock, and that PLL clock is the system clock) and a failure is detected, then the system clock switches to the HSI oscillator and the HSE oscillator is disabled.
- If the HSE oscillator clock was the clock source of PLL used as the system clock when the failure occurred, PLL is also disabled. In this case, if the PLLI2S or PLLSAI was enabled, it is also disabled when the HSE fails.

4 Boot configuration

4.1 Boot mode selection

In the STM32F74xxx/STM32F75xxx devices, two different boot spaces can be selected through the BOOT pin and the boot base address programmed in the BOOT_ADD0 or BOOT_ADD1 option bytes as shown in the *Table 3*.

Table 3. Boot modes

STM32F74xxx/STM32F75xxx		
Boot mode selection		**Boot space**
BOOT pin	**Boot address option bytes**	
0	BOOT_ADD0 [15:0]	– Boot address defined by user option byte BOOT_ADD0[15:0] - ST programmed value: Flash on ITCM at 0x0020 0000
1	BOOT_ADD1 [15:0]	– Boot address defined by user option byte BOOT_ADD1[15:0] - ST programmed value: System bootloader at 0x0010 0000

The BOOT_ADD0 and BOOT_ADD1 address option bytes allow to program any boot memory address from 0x0000 0000 to 0x2004 FFFF which include:

- All Flash memory address space mapped on ITCM or AXIM interface.
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface.
- The system memory bootloader.

The BOOT_ADD0 / BOOT_ADD1 option bytes can be modified after reset in order to boot from any other boot address after next reset.

If the programmed boot memory address is out of the memory mapped area or a reserved area, the default boot fetch address is programmed as follows:

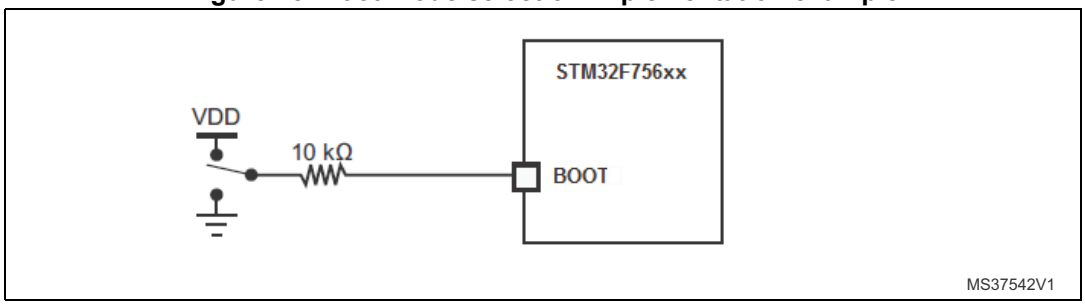
- Boot address 0: ITCM-FLASH at 0x0020 0000
- Boot address 1: ITCM-RAM at 0x0000 0000

When flash level 2 protection is enabled, only boot from Flash memory (on ITCM or AXIM interface) or system bootloader will be available. If the already programmed boot address in the BOOT_ADD0 and/or BOOT_ADD1 option bytes is out of the memory range or RAM address (on ITCM or AXIM) the default fetch will be forced from Flash memory on ITCM interface at address 0x00200000.

4.2 Boot pin connection

Figure 15 shows the external connection required to select the boot memory of the STM32F756xx.

Figure 15. Boot mode selection implementation example



1. Resistor values are given only as a typical example.

4.3 System bootloader mode

The embedded bootloader code is located in system memory. It is programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 4 shows the supported communication peripherals by the system bootloader.

Table 4. STM32F74xxx/STM32F75xxx bootloader communication peripherals

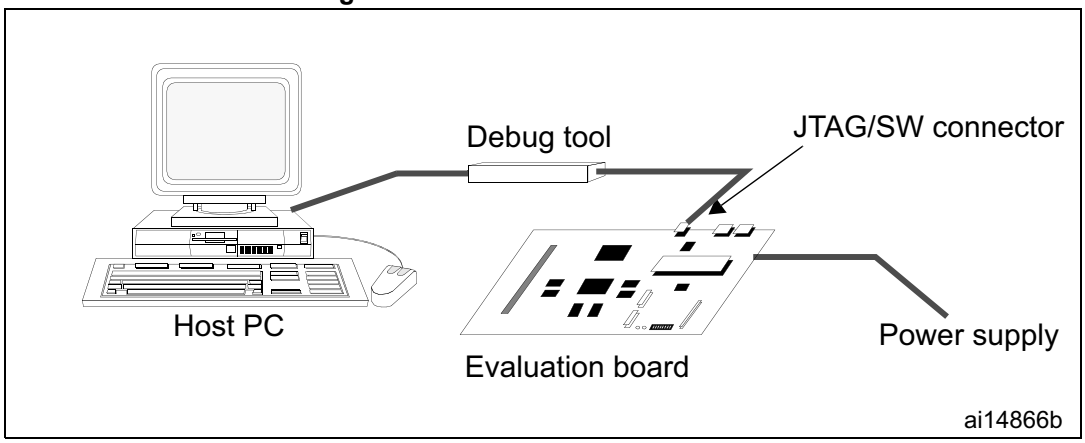
Bootloader peripherals	STM32F74xxx/STM32F75xxx
DFU	USB OTG FS (PA11 / PA12) in device mode
USART1	PA9 / PA10
USART3	PB10 / PB11 and PC10 / PC11
CAN2	PB5 / PB13
I2C1	PB6 / PB9
I2C2	PF0 / PF1
I2C3	PA8 / PC9

5 Debug management

5.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SW connector and a cable connecting the host to the debug tool. *Figure 16* shows the connection of the host to the evaluation board.

Figure 16. Host to board connection



5.2 SWJ debug port (serial wire and JTAG)

The core of the STM32F74xxx/STM32F75xxx integrates the Serial Wire / JTAG Debug Port (SWJ-DP). It is an ARM® standard CoreSight debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG Debug Port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The Serial Wire Debug Port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port.

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

For more details on the SWJ debug port refer to RM0385 SWJ debug port section (serial wire and JTAG).

5.3 Pinout and debug port pins

The STM32F74xxx/STM32F75xxx devices are available in various packages with different numbers of available pins. As a result, some functionality related to pin availability (TPIU parallel output interface) may differ between packages.

5.3.1 SWJ debug port pins

Five pins are used as outputs from the STM32F74xxx/STM32F75xxx for the SWJ-DP as alternate functions of general-purpose I/Os. These pins are available on all packages.

Table 5. SWJ debug port pins

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode Selection	IO	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if async trace is enabled	PB3
NJTRST	I	JTAG test nReset	-	-	PB4

5.3.2 Flexible SWJ-DP pin assignment

After RESET (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32F74xxx/STM32F75xxx devices offer the possibility of disabling some or all of the SWJ-DP ports and so, of releasing the associated pins for general-purpose IO (GPIO) usage.

Table 6 shows the different possibilities to release some pins.

Table 6. Flexible SWJ-DP assignment

Available debug ports	SWJ IO pin assigned				
	PA13 / JTMS / SWDIO	PA14 / JTCK / SWCLK	PA15 / JTDI	PB3 / JTDO	PB4 / NJTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without NJTRST	X	X	X	X	-
JTAG-DP disabled and SW-DP enabled	X	X	-		
JTAG-DP disabled and SW-DP disabled	Released				

For more details on how to disable SWJ-DP port pins, please refer to RM0385 I/O pin alternate function multiplexer and mapping section.

5.3.3 Internal pull-up and pull-down on JTAG pins

It is necessary to ensure that the JTAG input pins are not floating since they are directly connected to flip-flops to control the debug mode features. A special care must be taken with the SWCLK/TCK pin which is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled IO levels, the device embeds internal pull-ups and pull-downs on the JTAG input pins:

- NJTRST: Internal pull-up.
- JTDI: Internal pull-up.
- JTMS/SWDIO: Internal pull-up.
- TCK/SWCLK: Internal pull-down.

Once a JTAG IO is released by the user software, the GPIO controller takes control again.

The reset states of the GPIO control registers put the I/Os in the equivalent state:

- NJTRST: AF input pull-up.
- JTDI: AF input pull-up.
- JTMS/SWDIO: AF input pull-up.
- JTCK/SWCLK: AF input pull-down.
- JTDO: AF output floating.

The software can then use these I/Os as standard GPIOs.

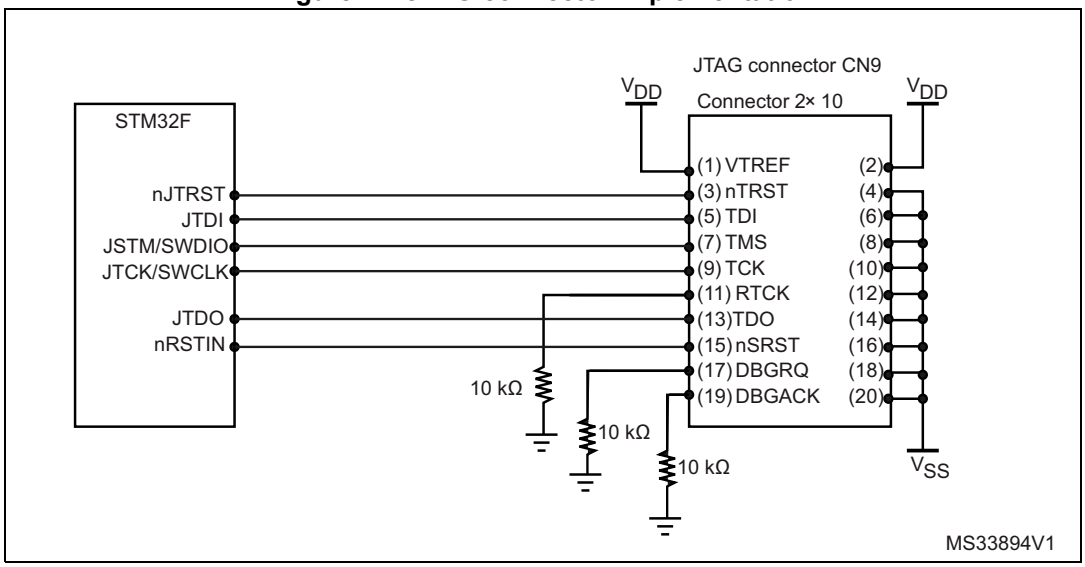
Note: The JTAG IEEE standard recommends to add pull-ups on TDI, TMS and nTRST but there is no special recommendation for TCK. However, for JTCK, the device needs an integrated pull-down.

Having embedded pull-ups and pull-downs removes the need to add external resistors.

5.3.4 SWJ debug port connection with standard JTAG connector

Figure 17 shows the connection between the STM32F7xxxx and a standard JTAG connector.

Figure 17. JTAG connector implementation



6 Recommendations

6.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

6.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

6.3 Ground and power supply (V_{SS},V_{DD})

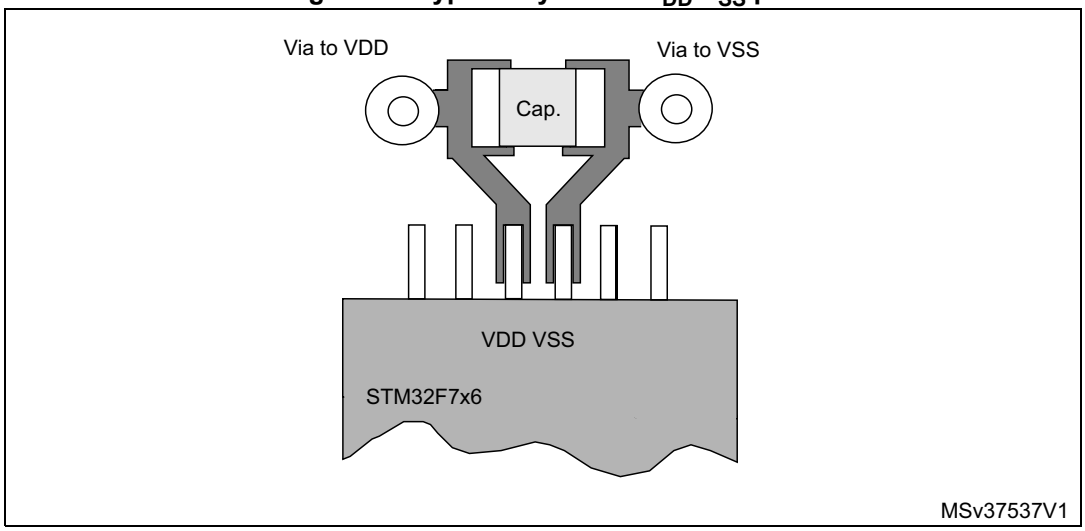
Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the area of the supply loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

6.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and one single tantalum or ceramic capacitor (min. 4.7 µF) connected in parallel. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but the exact values depend on the application needs. *Figure 18* shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 18. Typical layout for V_{DD}/V_{SS} pair



6.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands). For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (clock, etc.).
- Sensitive signals (high impedance, etc.).

6.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources. To increase EMC performance, unused clocks, counters or I/Os, should not be left free, e.g. I/Os should be set to “0” or “1” (pull-up or pull-down to the unused I/O pins.) and unused features should be “frozen” or disabled.

7 Reference design

7.1 Description

The reference design shown in *Figure 19*, is based on the STM32F756NGH6, a highly integrated microcontroller running at 216 MHz, that combines the Cortex®-M7 32-bit RISC CPU core with 1 Mbyte of embedded Flash memory and system SRAM up to 320 Kbytes (including Data TCM RAM 64 Kbytes), 16 Kbytes of instruction RAM (ITCM-RAM) and 4 Kbytes of backup SRAM.

7.1.1 Clocks

Two clock sources are used for the microcontroller:

- LSE: X2– 32.768 kHz crystal for the embedded RTC.
- HSE: X1– 25 MHz crystal.

Refer to *Section 3: Clocks on page 18*.

7.1.2 Reset

The reset signal of STM32F74xxx/STM32F75xxx devices is low active and the reset sources include:

- Reset button B1
- Debugging Tools from JTAG/SWD connector CN15 and ETM trace connector CN12

Refer to *Section 1.3: Reset & power supply supervisor on page 11*.

7.1.3 Boot mode

The STM32F74xxx/STM32F75xxx devices can boot from any region from 0x0000 0000 to 0x2004 FFFF.

The boot space is configured by setting BOOT pin and the boot base address programmed in the BOOT_ADD0 and BOOT_ADD1 option bytes.

For more details refer to *Section 4: Boot configuration on page 21*.

Note: In Low-power mode (more specially in Standby mode) the boot mode is mandatory to be able to connect to tools (the device should boot from the SRAM).

7.1.4 SWJ interface

Refer to *Section 5: Debug management on page 23*.

7.1.5 Power supply

Refer to *Section 1: Power supplies on page 7*.

7.2 Component references

Table 7. Mandatory components

Id	Component name	Reference	Quantity	Comments
1	Microcontroller	STM32F756NGH6	1	TFBGA216 package
2	Capacitor	100 nF	19	Ceramic capacitors (decoupling capacitors)
3	Capacitor	4.7 µF	1	Ceramic capacitor (decoupling capacitor)

Table 8. Optional components

Id	Components name	Reference	Quantity	Comments
1	Resistor	10 kΩ	6	Pull-up and pull-down for JTAG, BOOT pin, PDR and bypass regulator
2	Resistor	0 Ω	2	– Used as star connection point between V_{DDA} and V_{REF+} – Used as star connection point between V_{DD_MCU} and V_{DDUSB}
3	Capacitor	100 nF	5	Ceramic capacitor.
4	Capacitor	1.5 pF	2	Used for LSE: the value depends on the crystal characteristics.
5	Capacitor	1 µF	3	Used for V_{DDA} and V_{REF} and V_{DDUSB}.
6	Capacitor	2.2 µF	2	Used for internal regulator when it is on.
7	Capacitor	20 pF	2	Used for HSE: the value depends on the crystal characteristics.
8	Quartz	25 MHz	1	Used for HSE.
9	Quartz	32.768 kHz	1	Used for LSE.
10	JTAG connector	HE10-20	1	-
11	Battery	3V	1	If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.
12	Switch	SPDT	1	Used to select the right boot mode.
13	Push-button	B1	1	Reset button
14	Jumper	3 pins	2	Used to select V_{BAT} source, and BYPASS_REG pin.
15	Ferrite bead	FCM1608KF-601T03	1	Additional decoupling for V_{DDA}

Figure 19. STM32F756NGH6 reference schematic

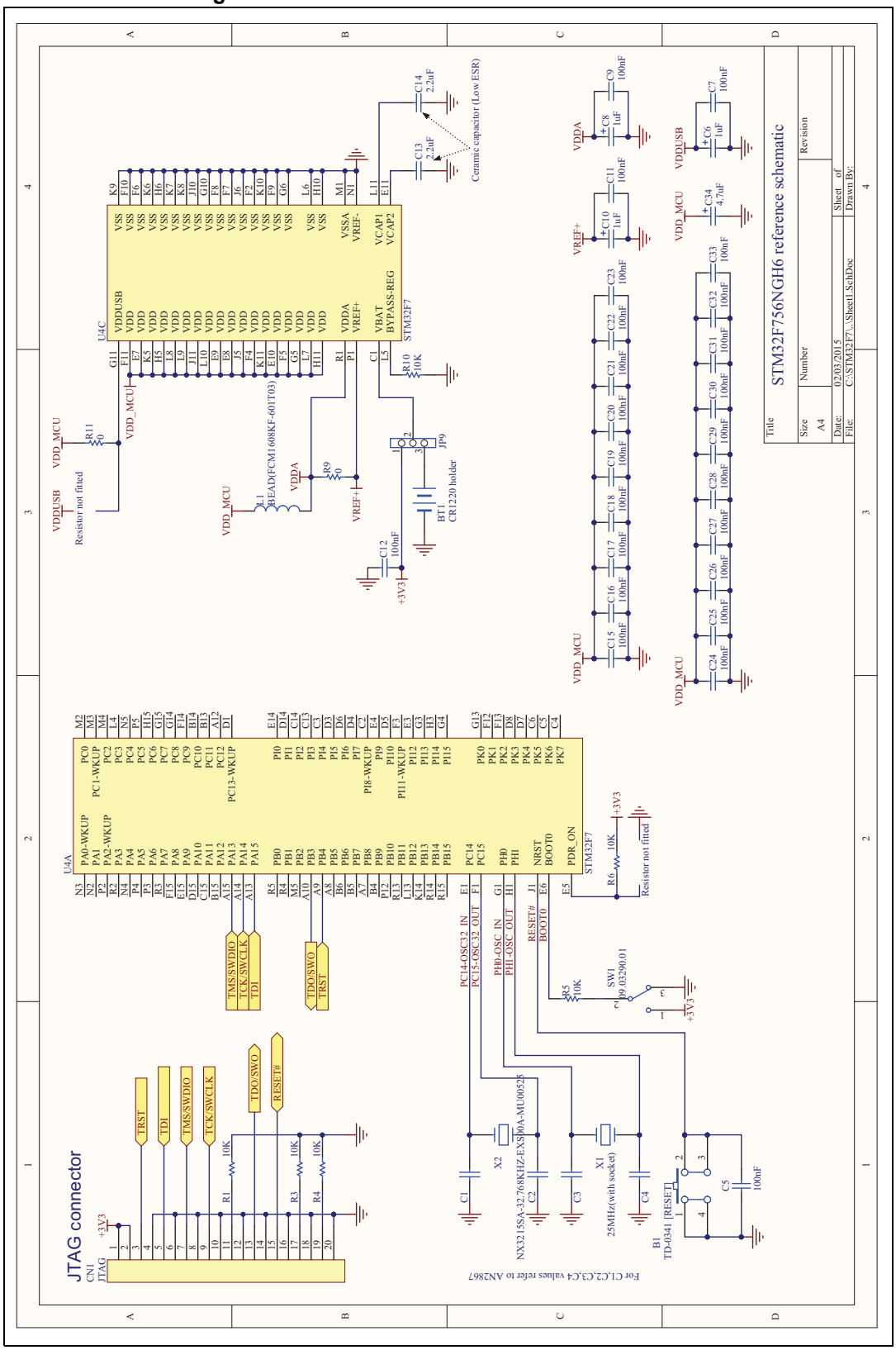


Table 9. Reference connection for all packages

Pin Name	LQFP100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216
PA13 (JTMS-SWDIO)	72	D3	105	A15	124	147	A15
PA14 (JTCK-SWCLK)	76	B1	109	A14	137	159	A14
PA15 (JTDI)	77	C2	110	A13	138	160	A13
PB3 (JTDO/TRACESWO)	89	B7	133	A10	161	192	A10
PB4 (NJTRST)	90	C7	134	A9	162	193	A9
PC14 (PC14-OSC32_IN)(1)(2)	8	D11	8	E1	9	9	E1
PC15 (PC15-OSC32_OUT)(1)(2)	9	E11	9	F1	10	10	F1
PH0 (PH0-OSC_IN)(2)	12	J11	23	G1	29	32	G1
PH1 (PH1-OSC_OUT)(2)	13	H10	24	H1	30	33	H1
BOOT	94	C9	138	D6	166	197	E6
NRST	14	H9	25	J1	31	34	J1
BYPASS_REG	-	N11	-	L4	48	-	L5
PDR_ON	-	A11	143	C6	171	203	E5
V_{BAT}	6	C11	6	C1	6	6	C1
V_{DDA}	21	L10	33	R1	39	42	R1
V_{REF+}	20	L11	32	P1	38	41	P1
V_{SSA}	19	K10	31	M1	37	40	M1
V_{REF-}	-	-	-	N1	-	-	N1
V_{CAP1}	48	N2	71	M10	81	92	L11
V_{CAP2}	73	D1	106	F13	125	148	E11
V_{DD}	50	J6	72	N10	82	94	L10
V_{DD}	75	C1	108	G13	127	150	F11
V_{DD}	100	D7	144	C5	172	204	E7
V_{DDUSB}	-	G1	95	H13	114	137	G11
V_{DD}	27	J8	39	K4	49	52	K5
V_{DD}	11	-	17	G3	23	26	H5
V_{DD}	-	-	52	N8	62	73	L8
V_{DD}	-	J5	62	N9	72	83	L9
V_{DD}	-	L1	84	J13	103	115	J11
V_{DD}	-	C5	121	C8	149	171	E9
V_{DD}	-	E6	131	C7	159	185	E8

Table 9. Reference connection for all packages (continued)

Pin Name	LQFP100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216
V_{DD}	-	G7	30	G3	36	39	J5
V_{DD}	-	E10	-	F3	15	15	F4
V_{DD}	-	-	-	J12	91	103	K11
V_{DD}	-	A1	-	C9	136	158	E10
V_{DD}	-	-	-	-	-	-	F5
V_{DD}	-	-	-	-	-	-	G5
V_{DD}	-	J7	-	-	-	59	L7
V_{DD}	-	-	-	-	-	124	H11
V_{SS}	49	H2	-	-	-	93	K9
PA0-WKUP(3)	22	K9	34	N3	40	43	N3
PC13(1)	7	D10	7	D1	8	8	D1
PI8(1)	-	-	-	D2	7	7	C2
V_{SS}	74	D2	107	F12	126	149	F10
V_{SS}	99	-	-	D5	-	202	F6
V_{SS}	26	-	38	-	-	51	K6
V_{SS}	10	H7	16	G2	22	25	H6
V_{SS}	-	-	51	M8	61	72	K7
V_{SS}	-	H3	61	M9	71	82	K8
V_{SS}	-	-	83	-	102	114	J10
V_{SS}	-	D2	94	G12	113	136	G10
V_{SS}	-	-	120	D8	148	170	F8
V_{SS}	-	-	130	D7	158	184	F7
V_{SS}	-	-	-	-	-	-	J6
V_{SS}	-	-	-	-	-	-	F2
V_{SS}	-	-	-	H12	90	-	K10
V_{SS}	-	F5	-	D9	135	-	F9
V_{SS}	-	-	-	-	-	-	G6
V_{SS}	-	-	-	-	-	-	F2
V_{SS}	-	-	-				
V_{SS}	-	-	-	-	-	125	H10

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:

- The speed should not exceed 2 MHz with a maximum load of 30 pF.

- These I/Os must not be used as a current source (e.g. to drive an LED).

2. 5 V tolerant except when in analog mode or oscillator mode for PC14, PC15, PH0 and PH1.

3. If the device is delivered in an WLCSP143, UFBGA176, LQFP176 or TFBGA216 package, and the BYPASS_REG pin is set to VDD (Regulator OFF/internal reset ON mode), then PA0-WKUP is used as an internal reset (active low).

8 Recommended PCB routing guidelines for STM32F745xx/STM32F756xx devices

8.1 PCB stack-up

In order to reduce the reflections on high speed signals, it is necessary to match the impedance between the source, sink and transmission lines. The impedance of a signal trace depends on its geometry and its position with respect to any reference planes.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized.

The minimum configuration that can be used is 4 or 6 layers stack-up. An 8 layers boards may be required for a very dense PCBs that have multiple SDRAM/SRAM/NOR/LCD components.

The following stack-ups are intended as examples which can be used as a starting point for helping in a stack-up evaluation and selection. These stack-up configurations are using a GND plane adjacent to the power plane to increase the capacitance and reduce the gap between GND and power plane. So high speed signals on top layer will have a solid GND reference plane which helps to reduce EMC emissions, as going up in number of layers and having a GND reference for each PCB signal layer will improve further the radiated EMC performance.

Figure 20. Four layer PCB stack-up example

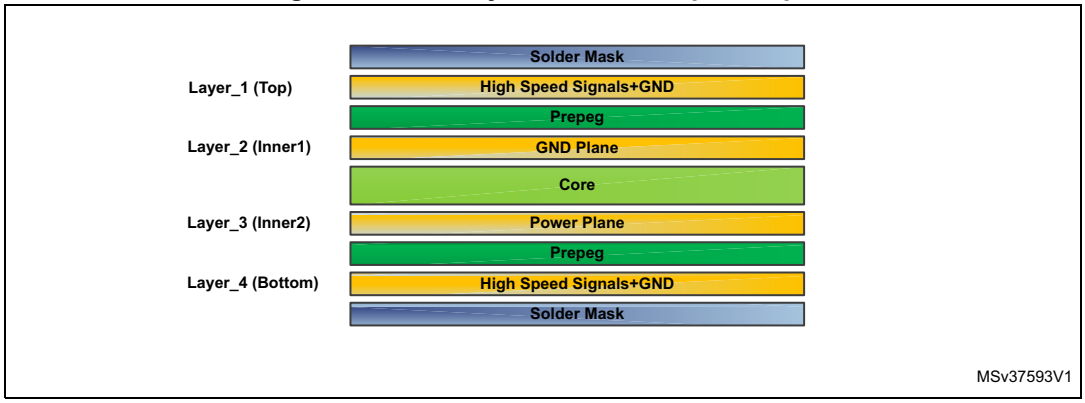
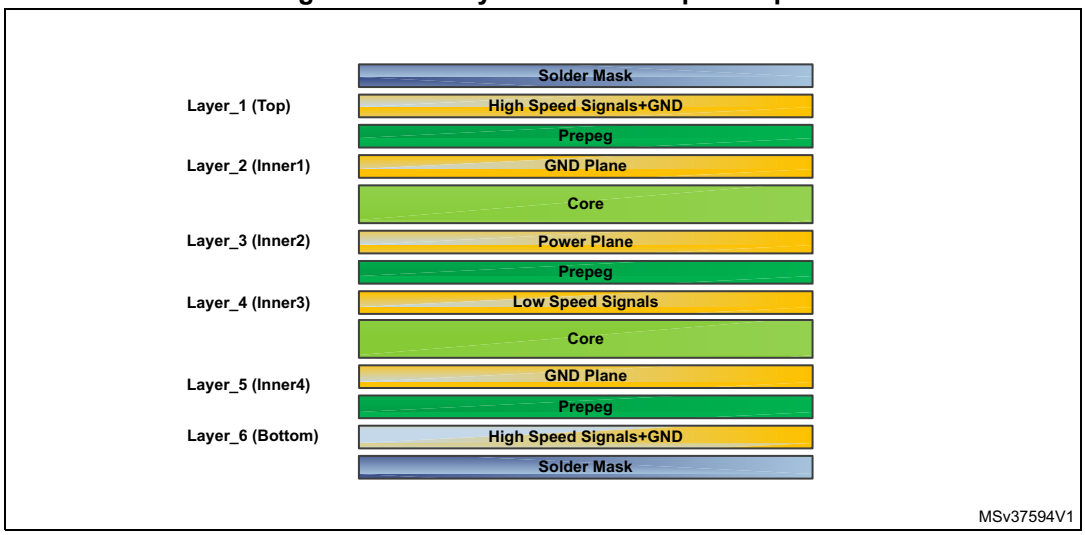


Figure 21. Six layer PCB stack-up example



8.2 Crystal oscillator

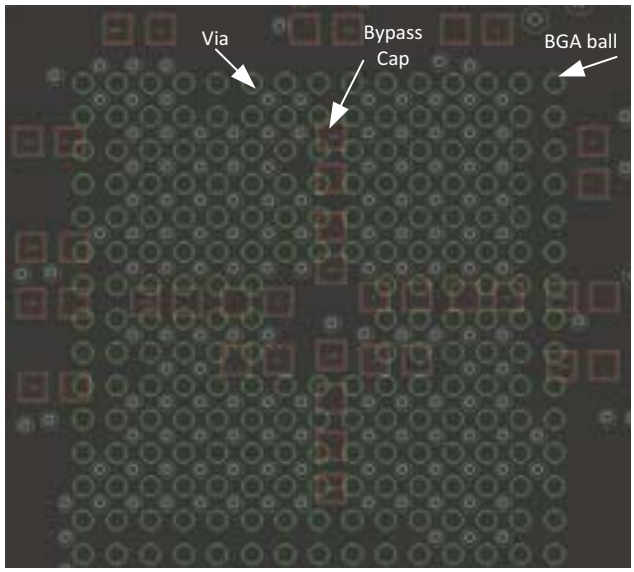
Use the application note: Oscillator design guide for STM8S, STM8A and STM32 microcontrollers (AN2867), for further guidance on how to layout and route crystal oscillator circuits.

8.3 Power supply decoupling

An adequate power decoupling for STM32F74xxx/STM32F75xxx devices is necessary to prevent an excessive power noise and ground bounce noise. Please refer to *Section 1.2: Power supply scheme*.

Figure 22 shows an example of placing bypass capacitors underneath STM32F74xxx/STM32F75xxx closer to pins and with less vias:

Figure 22. Example of bypass cap placed underneath the STM32F74xxx/STM32F75xxx



- Place the bypass capacitors as close as possible to the power and ground pins of the MCU.
- Add the recommended bypass capacitors for as many V_{DD}/GND pairs as possible.
- Connect the bypass capacitor pad to the power and ground plane with a wider, short trace/via to reduce the serie inductance, allow a maximum current flow and reduce the transient voltage drops from the power plane. Which also reduces the possibility of ground bounce.

8.4 High speed signal layout

8.4.1 SDMMC bus interface

Interface connectivity

The SD/SDIO MMC card host interface (SDMMC) provides an interface between the APB2 peripheral bus and Multi Media Cards (MMCs), SD memory cards and SDIO cards. The SDMMC interface is a serial data bus interface, that consists of a clock (CK), command signal (CMD) and 8 data lines (D[0:7]).

Interface signal layout guidelines:

- Reference the plane using GND or PWR (if PWR, add 10nf switching cap between PWR and GND)
- Trace the impedance: 50Ω ± 10%
- The skew being introduced into the clock system by unequal trace lengths and loads, minimize the board skew, keep the trace lengths equal between the data and clock.
- The maximum skew between data and clock should be below 250 ps @ 10mm
- The maximum trace length should be below 120mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- The trace capacitance should not exceed 20 pF at 3.3V and 15pF at 1.8V
- The maximum signal trace inductance should be less than 16nH
- Use the recommended pull-up resistance for CMD and data signals to prevent bus floating.
- The mismatch within data bus, data and CK or CK and CMD should be below 10mm.
- Keep the same number of vias between the data signals

Note: The total capacitance of the SD memory card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line. The total bus capacitance is $C_L = C_{Host} + C_{Bus} + N*C_{Card}$ where Host is STM32F74xxx/STM32F75xxx, bus is all the signals and Card is SD card.

8.4.2 Flexible memory controller (FMC) interface

Interface connectivity

The FMC controller and in particular SDRAM memory controller which has many signals, most of them have a similar functionality and work together. The controller I/O signals could be splitted in four groups as follow:

- An address group which consists of row/column address and bank address
- A command group which includes the row address strobe (NRAS), the column address strobe (NCAS), and the write enable (SDWE)
- A control group which includes a chip select bank1 and bank2 (SDNE0/1), a clock enable bank1 and bank2 (SDCKE0/1), and an output byte mask for the write access (DQM).
- A data group/lane which contains 8 signals [(a)]: the eight D (D7–D0) and the data mask (DQM).

a.It depends of the used memory: SDRAM with x8 bus widths have only one data group, while x16 and x32 bus-width SDRAM have two and four lanes, respectively.

Interface signal layout guidelines:

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50Ω ± 10%
- The maximum trace length should be below 120mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Reduce the crosstalk, place data tracks on the different layers from the address and control lanes, if possible. However, when the data and address/control tracks coexist on the same layer they must be isolated from each other by at least 5 mm.
- Match the trace lengths for the data group within ± 10 mm of each other to diminish the skew. Serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be used to match the lengths.
- Placing the clock (SDCLK) signal on an internal layer, minimizes the noise (EMI). Route the clock signal at least 3x of the trace away from others signals. Use as less vias as possible to avoid impedance change and reflection. Avoid using serpentine routing.
- Match the clock traces to the data/address group traces within ±10mm.
- Match the clock traces to each signal trace in the address and command groups to within ±10mm (with maximum of <= 20mm).
- Trace the capacitances:
  - At 3.3 V keep the trace within 20 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 30pF.
  - At 1.8 V keep the trace within 15 pF with overall capacitive loading (including Data, Address, SDCLK and Control) no more than 20pF.

8.4.3 Quadrature serial parallel interface (Quad SPI)

Interface connectivity

The QUADSPI is a specialized communication interface targeting single, dual or Quad SPI FLASH memories. The QUAD SPI interface is a serial data bus interface, that consists of a clock (SCLK), a chip select signal (nCS) and 4 data lines (IO[0:3]).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50Ω ± 10%
- The maximum trace length should be below 120mm. If the signal trace exceeds this trace-length/speed criterion, then a termination should be used
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least 3x of the trace away from other signals. Use as less vias as possible to avoid the impedance change and reflection. Avoid using a serpentine routing.
- Match the trace lengths for the data group within ± 10 mm of each other to diminish skew. Serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be used to match the lengths.

Avoid using a serpentine routing for the clock signal and as less via(s) as possible for the whole path. a via alter the impedance and add a reflection to the signal.

8.4.4 Embedded trace macrocell (ETM)

Interface connectivity

The ETM enables the reconstruction of the program execution. The data are traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the data bus of 4 lines D[0:3] and the clock signal CLK.

Interface signals layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10nf stitching cap between PWR and GND
- Trace the impedance: 50Ω ± 10%
- All the data trace should be as short as possible (<=25 mm),
- Trace the lines which should run on the same layer with a solid ground plane underneath it without a via.
- Trace the clock which should have only point-to-point connection. Any stubs should be avoided.
- It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they should be as short as possible. If longer are required, there should be a possibility to optionally disconnect them (e.g. by jumpers).

8.5 Package layout recommendation

8.5.1 BGA 216 0.8 mm pitch design example

Table 10. BGA 216 0.8 mm pitch package information

Package information (mm)	Design parameters (mm)
Ball pitch : 0.8	Via size : hole size ∅= 0.2, pad size: 0.45, plane clearance: 0.65
Ball size : 0.4	Trace width : 0.10/0.125
Number of rows/columns : 15x15	Trace/trace space : 0.10/0.125
Package solder Pad: SMD	BGA land size (Ball pad): ∅= 0.4, solder mask: 0.5

With 0.8 mm pitch BGA balls, fan-out vias are needed to route the balls to other layers on the PCB. Through-vias are used in this example, which cost less than blind, buried vias. For four adjacent BGA land pads, we can have only one via as showing in *Figure 23* and *Figure 24*. The traces are routed of two first row and two first colon without fan-out via. The current pitch size allows to route only one trace between two adjacent BGA land pads.

Figure 25 shows an example of ideal SDRAM signals fan-out vias with power and gnd signals. These signals can be optimized to achieve the routing and length matching in an another layer before connecting to an SDRAM IC.

Figure 23. BGA 0.8mm pitch example of fan-out

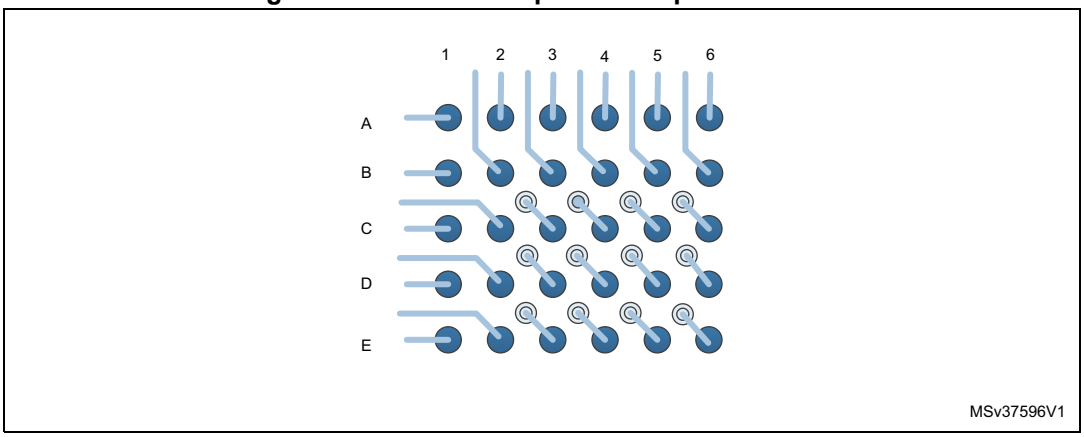


Figure 24. Via fan-out

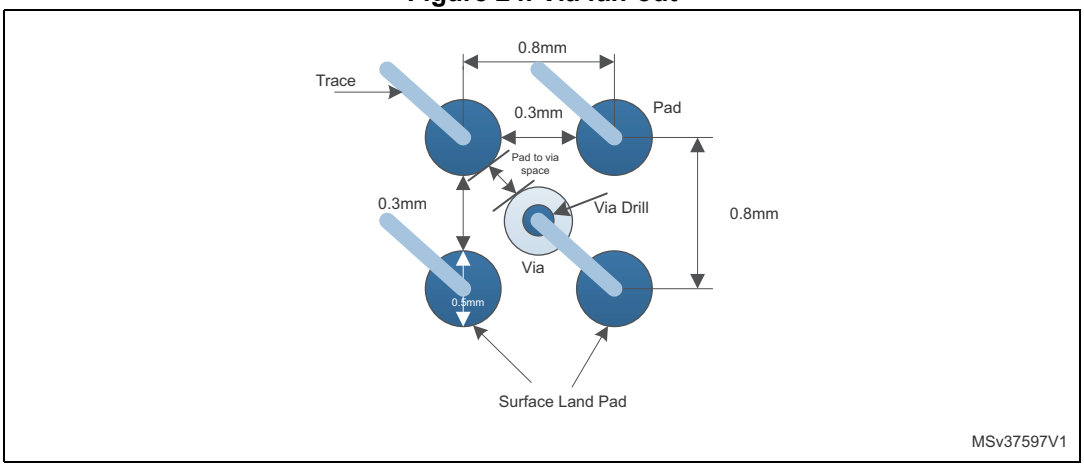
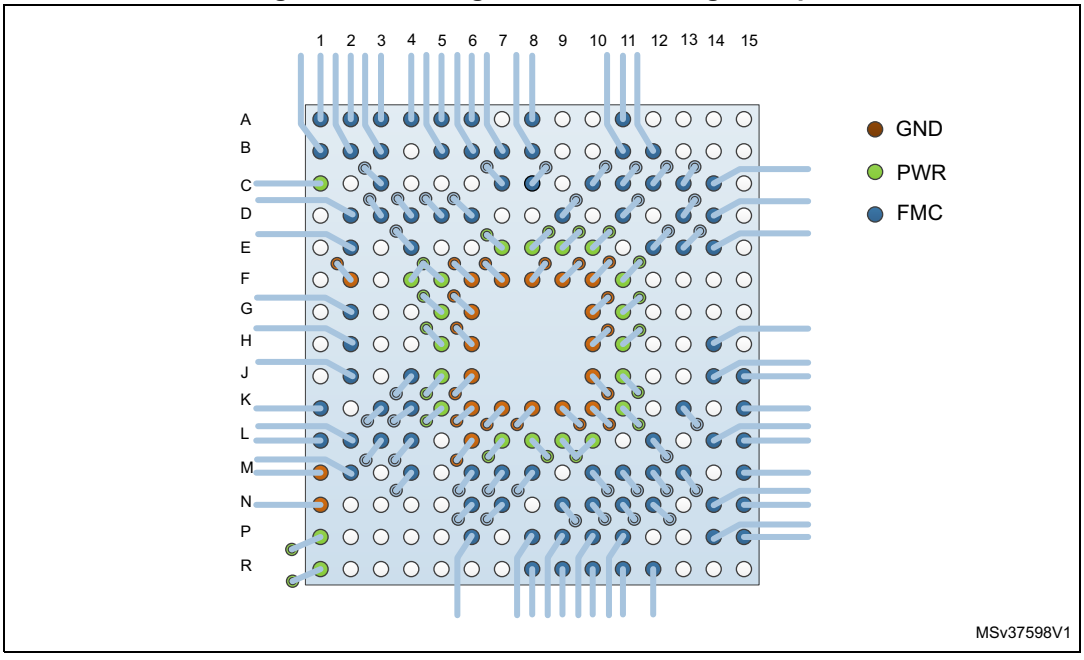


Figure 25. FMC signal fan-out routing example



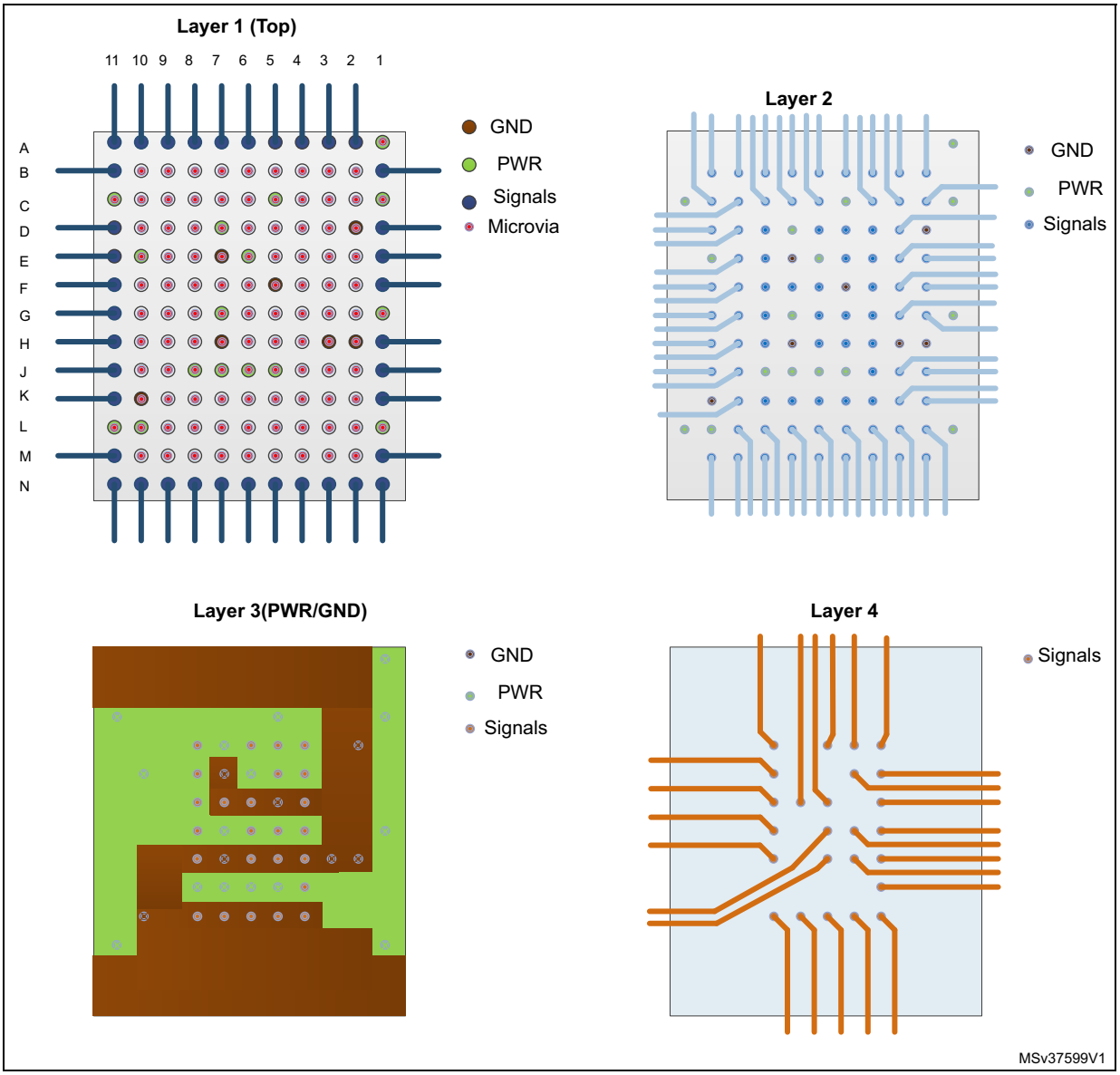
8.5.2 WLCSP143 0.4 mm pitch design example

Table 11. Wafer level chip scale package information

Package information (mm)	Design parameters (mm)
Bump pitch : 0.4	Microvia size : hole size ∅= 0.1, via land: 0.2
Bump size : 0.25	Trace width/space : 0.07/0.05 or 0.07/0.07
Number of rows/columns : 13x11	Bump pad size ∅= 0.26 max – 0.22 recommended
Non-solder mask defined via underbump allowed	Solder mask opening bump ∅=0.3 min (for 0.26 diameter pad)

A better way to route this package and the fan-out signals is to use a through microvia technology. Microvia will route out internal bumps to a buried layers inside the PCB. To achieve this, WLCSP package pads have to be connected to this internal layer through microvia. In case of four layers PCB, the first layer is WLCSP component, the second layer will be used as a signal layer, the third layer as the power and ground and the bottom layer for a signal layout. *Figure 26* shows an example of the layout for four layers PCB.

Figure 26. 143-bumps WLCSP, 0.40 mm pitch routing example



9 Conclusion

This application note should be used as a starting reference for a new design with STM32F74xxx and STM32F75xxx devices.

10 Revision history

Table 12. Document revision history

Date	Revision	Changes
24-Mar-2015	1	Initial release.
08-Jun-2015	2	Added *Section 8: Recommended PCB routing guidelines for STM32F745xx/STM32F756xx devices*. Updated title and the whole document changing STM32F746xx/STM32F756xx by STM32F74xxx/STM32F75xxx. Updated *Table 1: Applicable products* adding STM32F745xx RPNs. Updated *Section 1.1.2: Independent USB transceivers supply* similar to the corresponding datasheet. Updated *Section 1.3.6: Regulator OFF mode*. Updated *Figure 9: BYPASS_REG supervisor reset connection* and the whole document changing BOOT0 by BOOT. Updated *Section 1.1.1: Independent A/D converter supply and reference voltage*. Updated *Section 1.1.3: Battery backup domain*. Updated *Section 1.2: Power supply scheme* adding a note. Updated *Section 1.3.5: Internal reset OFF* adding a paragraph, modifying *Figure 7: Power supply supervisor interconnection with internal reset OFF* and adding *Figure 8: NRST circuitry timing example for STM32F74xxx/STM32F75xxx*. Updated *Section 7.1: Description* changing the frequency at 216 MHz.