AN4676
Application note

STM32F7 Series peripheral interconnections

Introduction

This application note describes how peripherals of the STM32F7 Series microcontrollers can communicate autonomously without any intervention from the CPU via a network known as peripheral interconnect matrix.

This new STM32F7 Series feature enhances the CPU real-time performance while substantially reducing its power consumption.

The present document first describes the peripheral interconnect matrix features and then provides an overview of the peripheral interconnections and how to configure them depending of the application. This description is completed by a detailed application example.

This application note must be read in conjunction with the STM32F75xxx and STM32F74xxx reference manual (RM0385) available from www.st.com/stm32.

This application note concerns all the devices of the STM32F7 Series.

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1 Module overview

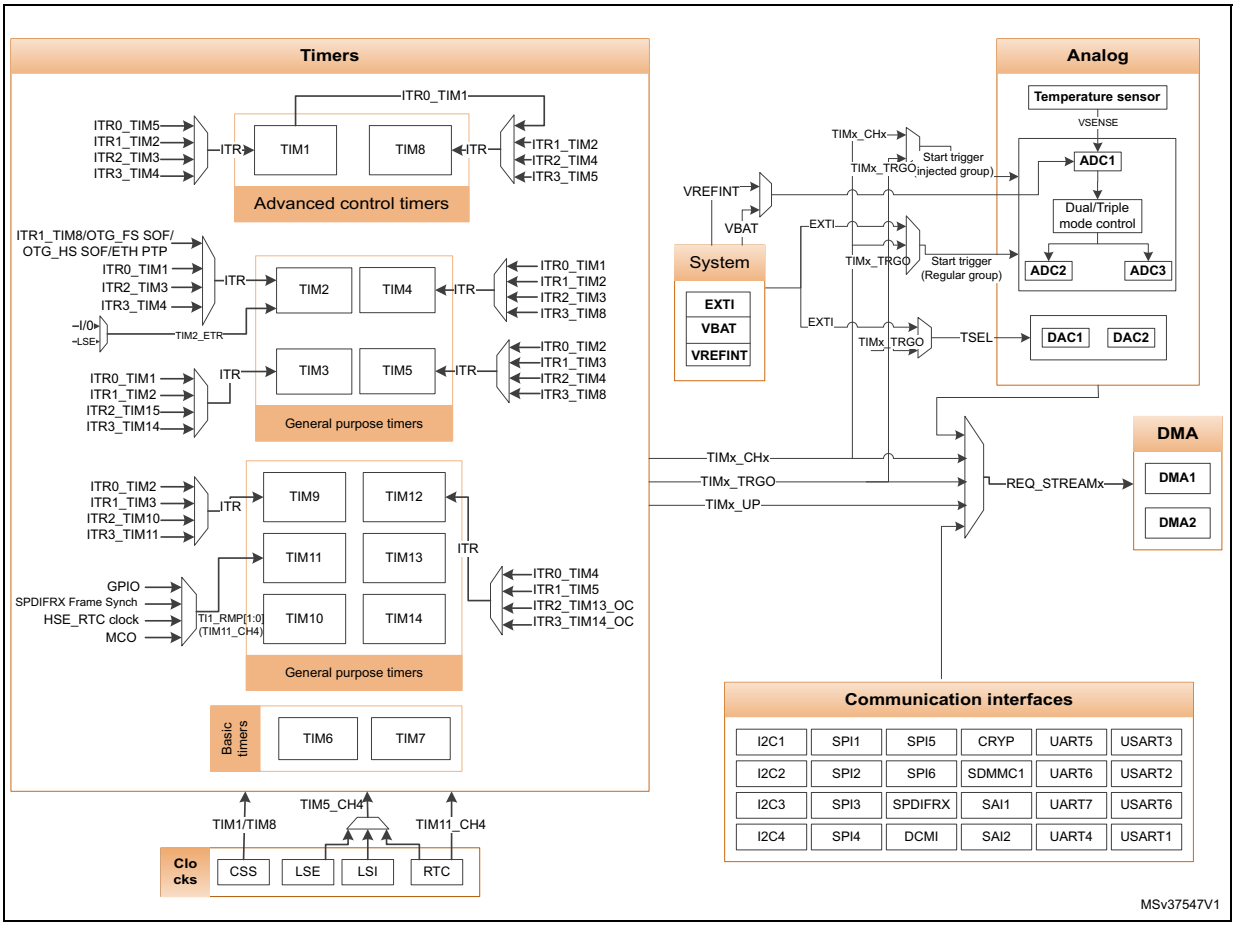
Several peripherals can be directly interconnected and configured to send or respond to event signals than can be internally routed to/from other peripherals in the device.

The STM32F7 Series autonomous peripherals include:

- **Timers** that can be internally connected to each other or connected to the DMA or to the analog block.
- **Analog block** that can receive events from a timer or send events to the DMA.
- **Clocks block** that can send events to the timers.
- **System block** that can send events to the analog block.
- **Communication interface block** that can send events to the timers or to the DMA.

An overview of STM32F7 Series peripheral interconnections is given in *Figure 1: STM32F7 Series peripheral interconnection overview*.

Figure 1. STM32F7 Series peripheral interconnection overview



2 Peripheral interconnect matrix

STM32F7 Series peripheral are interconnected through a network named peripheral interconnect matrix, that allows to directly connect one peripheral to another without waking up the CPU. Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

The peripherals that respond to events are called users while the peripherals that send events are called generators. Both types are listed in *Table 1*.

Table 1. STM32F7 Series peripheral interconnect matrix

Generators			Users																		
			Timers												DMA		Analog				
																	ADC			DAC	
			TIM1	TIM2	TIM3	TIM4	TIM5	TIM6	TIM7	TIM8	TIM9	TIM10	TIM11	TIM12	DMA1	DMA2	1	2	3	1	2
TIMERS	TIM1		-	X	X	X	-	-	-	X	-	-	-	-	-	X	X	X	X	-	-
	TIM2		X	-	X	X	X	-	-	X	X	-	-	-	X	-	X	X	X	X	X
	TIM3		X	X	-	X	X	-	-		X	-	-	-	X	-	X	X	X	-	-
	TIM4		X	X	X	-	X	-	-	X	-	-	-	X	X	-	X	X	X	X	X
	TIM5		X	-	-	-	-	-	-	X	-	-	-	X	X	-	X	X	X	X	X
	TIM6		-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X
	TIM7		-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	X	X
	TIM8		-	X	-	X	X	-	-	-	-	-	-	-	-	X	X	X	X	X	X
	TIM10		-	-	-	-	-	-	-	-	X	-	-	-	-	-	-	-	-	-	-
	TIM11		-	-	-	-	-	-	-	-	X	-	-	-	-	-	-	-	-	-	-
	TIM13		-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-	-
	TIM14		-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-	-
	TIM15		-	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Analog	ADC	1	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	X	X	-	-
		2	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
		3	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	DAC	1	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
		2	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	VSENSE		-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-
Clocks	LSI		-	-	-	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	LSE		-	-	-	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	RTC			-	-	-	X	-	-	-	-	-	X	-	-	-	-	-	-	-	-
	CSS		X	-	-	-	-	-	-	X	-	-	-	-	-	-	-	-	-	-	-

Table 1. STM32F7 Series peripheral interconnect matrix (continued)

Generators		Users																		
		Timers												DMA		Analog				
																ADC			DAC	
		TIM1	TIM2	TIM3	TIM4	TIM5	TIM6	TIM7	TIM8	TIM9	TIM10	TIM11	TIM12	DMA1	DMA2	1	2	3	1	2
Communication interfaces	OTG_FS	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	OTG_HS	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	SPI1	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	SPI2	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	SPI3	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	SPI4	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	SPI5	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	SPI6	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	CRYP	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	HASH	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	ETH	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	SPDIFRX	-	-	-	-	-	-	-	-	-	-	X	-	X	-	-	-	-	-	-
	QSPI	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	I2C1	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	I2C2	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	I2C3	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	I2C4	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	I2S2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	I2S3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	SAI1	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	SAI2	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	USART1	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	USART2	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	USART3	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	USART6	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	UART4	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	UART5	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	UART7	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	UART8	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-
	DCMI	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-
	SDMMC1	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-	-

Table 1. STM32F7 Series peripheral interconnect matrix (continued)

		Users																		
		Timers												DMA		Analog				
Generators		TIM1	TIM2	TIM3	TIM4	TIM5	TIM6	TIM7	TIM8	TIM9	TIM10	TIM11	TIM12	DMA1	DMA2	ADC			DAC	
																1	2	3	1	2
System	V_{BAT}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-
	V_{REFINT}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	-	-
	EXTI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	X	X

2.1 Timers block

2.1.1 From TIM to TIM

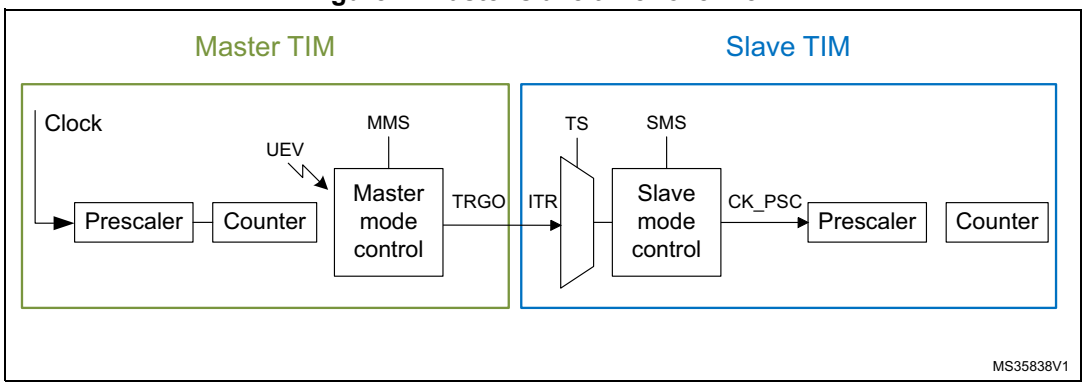
Some timers are linked together internally for timer synchronization or chaining. When one timer is configured in Master mode, it can reset, start, stop or clock the counter of an another timer configured in Slave mode.

A description of this feature is provided in the *timer synchronization* section and *TIM2 option register (TIM2_OR)* of RM0385 reference manual.

The output (from Master) is on TIM_TRGO signal following a configurable timer event. The input (to Slave) is on TIM_ITR0/ITR1/ITR2/ITR3 signal events.

Figure 2 gives an overview of the trigger selection and the Master mode selection blocks.

Figure 2. Master/slave timer overview



For more details on the possible master/slave connections, refer to *TIMx internal trigger connection* tables of RM0385 reference manual.

2.1.2 From TIM to ADC

As shown in *Figure 3*, some timers can be used to generate an ADC trigger event.

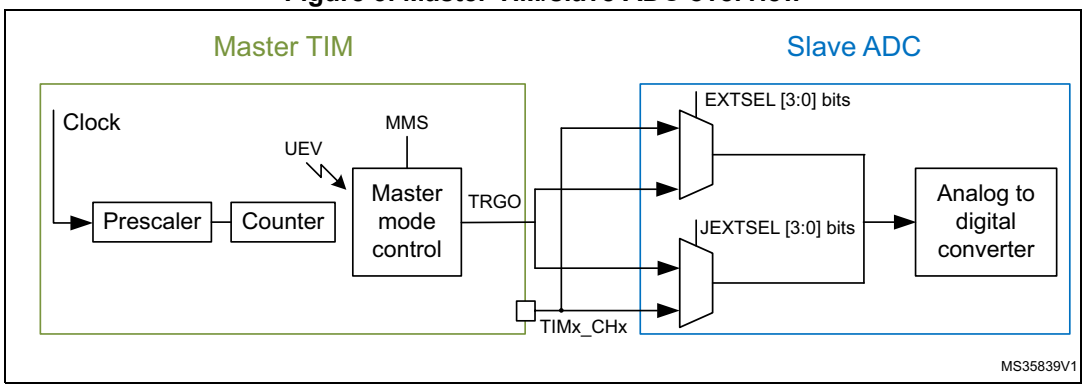
The ADC synchronization is described in the *conversion on external trigger and trigger polarity* section of RM0385 reference manual.

For more details on the connection between timers and ADCs regular and injected channels, refer to *external trigger for regular channels* table and *external trigger for injected channels* table of RM0385 reference manual.

The output (from timer) is on TIMx_TRGO or TIM_CHx signal event.

The input (to ADC) is on EXTSEL [3:0], JEXTSEL [3:0] signal event.

Figure 3. Master TIM/slave ADC overview



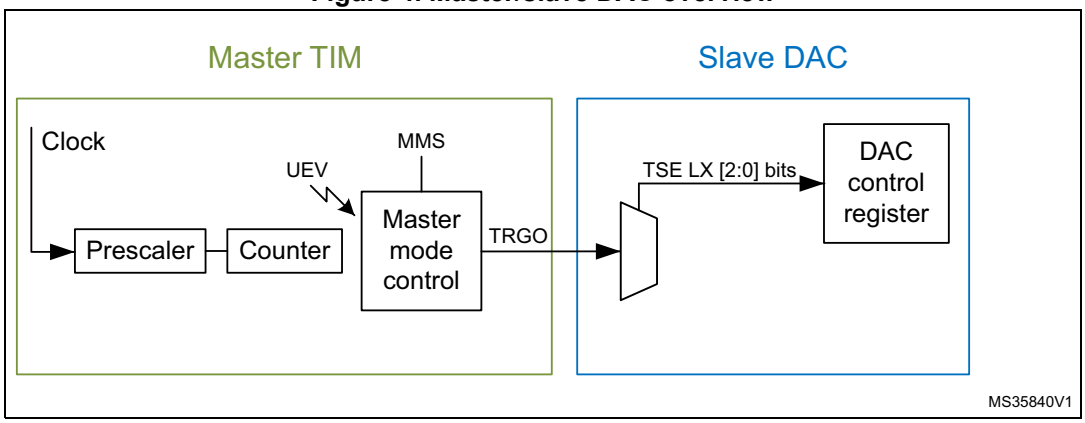
2.1.3 From TIM to DAC

Some timers can be used as triggering an event to start a DAC conversion (see *Figure 4*).

The selection on input triggers in DAC is provided in the *DAC trigger selection* section of RM0385 reference manual.

The output (from timer) is on TIM_TRGO signal directly connected to the corresponding DAC inputs.

Figure 4. Master/slave DAC overview



2.1.4 FROM TIM to DMA

Refer to *Section 2.6: DMA block*.

2.2 Analog block

The analog block includes:

- The ADC block (three ADCs)
- The DAC block (two DACs)
- The temperature sensor block

2.2.1 From ADC to ADC

In the multi ADC mode, the start of conversion is triggered alternately or simultaneously by the ADC1 master to the ADC2 and ADC3 slaves depending on the mode selected by the MULITI [4:0] bits in the ADC_CCR register.

For more details, refer to *multi ADC mode section* of RM0385 reference manual.

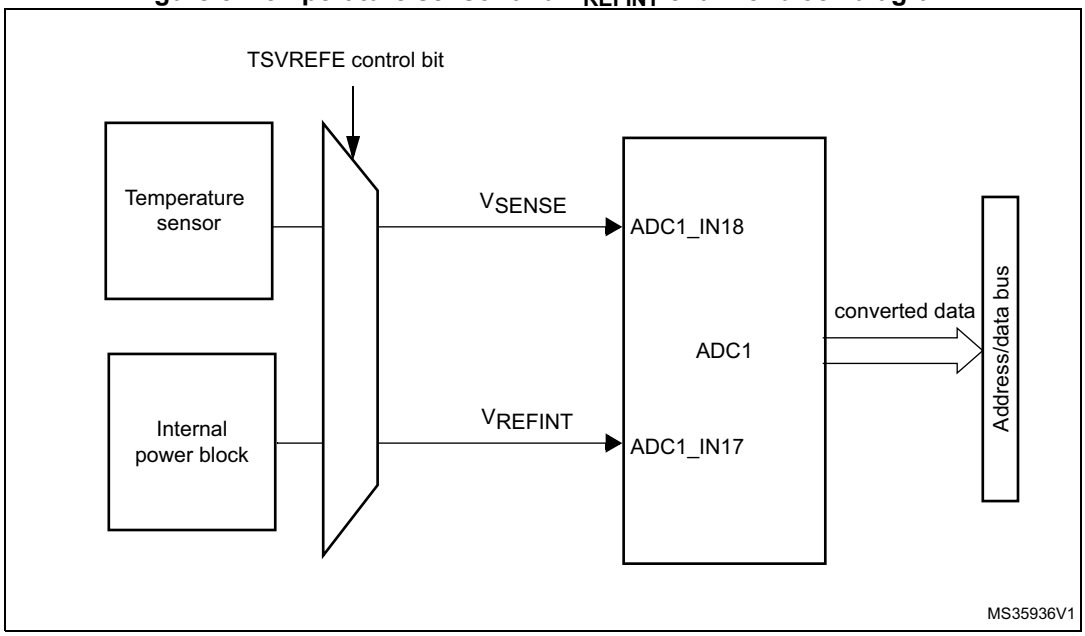
2.2.2 From the temperature sensor to ADC1

The temperature sensor can be used to measure the ambient temperature (Ta) of the device.

The V_{BAT} and temperature sensor are connected to the same ADC internal channel (ADC1_IN18). Only one conversion, either the temperature sensor or V_{BAT}, must be selected at a time. When both conversion are enabled simultaneously, only the V_{BAT} conversion is performed.

Figure 5 shows the block diagram of the temperature sensor.

Figure 5. Temperature sensor and V_{REFINT} channel block diagram



The *temperature sensor* section of RM0385 reference manual describes the connection between the sensor and the ADC as well as the procedure to read the converted value.

2.2.3 From the analog block to DMA

Refer to *Section 2.6: DMA block*.

2.3 Clock block

System block includes:

- The LSE clock
- The LSI clock
- The clock security system (CSS)
- The real-time clock (RTC)

2.3.1 From CSS to TIM

The CSS can generate system errors in the form of timer break toward timers.

The purpose of the break function is to protect power switches driven by PWM signals generated by the timers.

The list of possible break sources is given in the *using the break function (TIM1/TIM8)* section of RM0385 reference manual.

2.3.2 From LSE, LSI,RTC to TIM

The external clock (LSE), internal clock (LSI) and RTC wakeup interrupt can be used as input to general-purpose timer (TIM5 channel 4/TIM11 channel 1).

This feature is described in the following sections of RM0385 reference manual:

- *Internal/external clock measurement using TIM5/TIM11*
- *TIM5 option register (TIM5_OR)*
- *TIM11 option register (TIM11_OR)*

2.4 System block

The system block includes:

- The internal reference voltage (V_{REFINT})
- V_{BAT} supply voltage
- External interrupt/event controller (EXTI)

2.4.1 From V_{BAT}, V_{REFINT} to ADC

The V_{BAT} pin is internally connected to a bridge divider ($V_{BAT}/4$). It can be converted either as an injected or as a regular channel through ADC_IN18 channel.

The V_{REFINT} is connected to ADC_IN17 channel.

This interconnection is explained in the following sections of RM0385 reference manual:

- *Channel selection*
- *Battery charge monitoring*

2.4.2 From EXTI to the analog block

EXTI can be used to generate an ADC trigger event or to start a DAC conversion.

The ADC synchronization is described in the *conversion on external trigger and trigger polarity* section of RM0385 reference manual.

The selection of input triggers on DAC is provided in the *DAC trigger selection* section of RM0385 reference manual.

2.5 Communication interface block

2.5.1 From SPDIFRX to TIM

SPDIFRX (SPDIFRX_FRAME_SYNC) is connected to TIM11_CH1 to measure the clock drift of received SPDIFRX frames.

This interconnection is explained in the *TIM11 option register (TIM11_OR)* section of RM0385 reference manual.

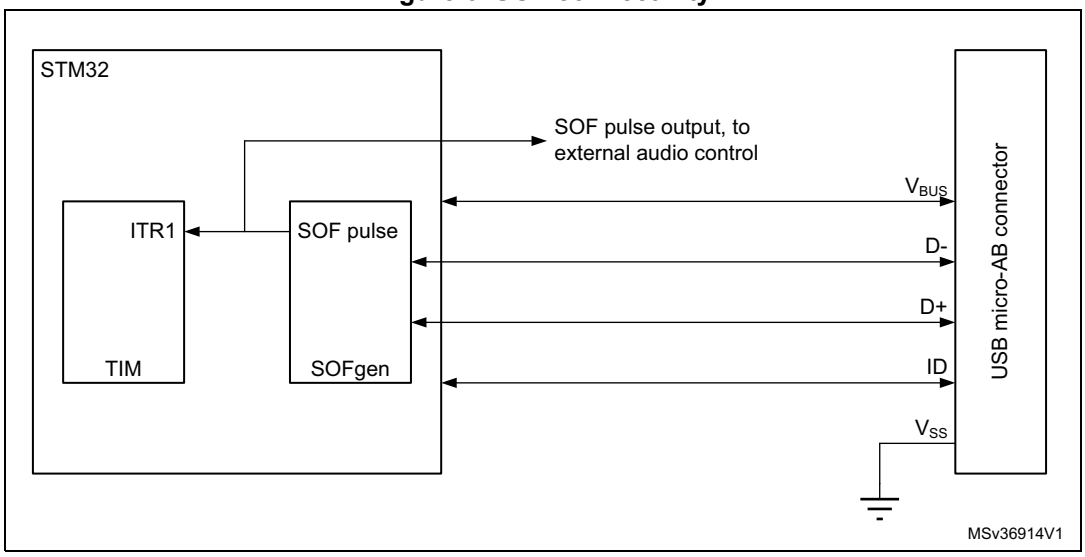
2.5.2 From USB block to TIM

The USB block includes:

- USB on-the-go full-speed (OTG_FS)
- USB on-the-go high-speed (OTG_HS)

USB (OTG_FS SOF) and USB (OTG HS SOF) can generate a trigger to a general-purpose timer (TIM2), as shown in *Figure 6*.

Figure 6. SOF connectivity



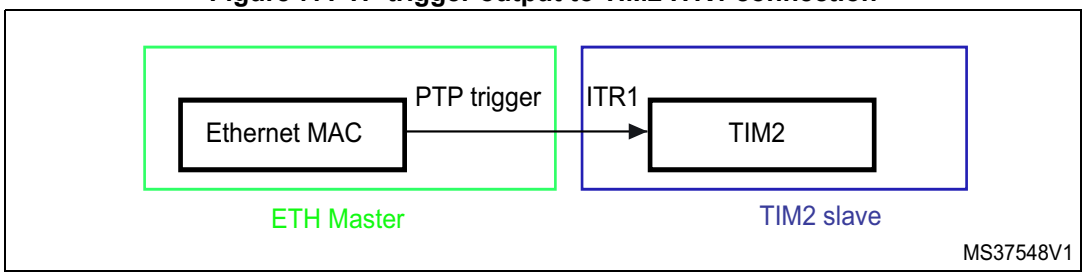
The interconnection between USB and TIM2 is described in the *SOF trigger* section of RM0385 reference manual.

2.5.3 From ETH to TIM

The MAC can generate a trigger to general-purpose timer (TIM2).

This PTP trigger signal is connected to the TIM2 ITR1 input selectable by software. The connection is enabled through ITR1_RMP (bits 11 and 10) in the TIM2 option register (TIM2_OR).

Figure 7. PTP trigger output to TIM2 ITR1 connection



The interconnection between ETH and TIM2 is described in the *precision time protocol (IEEE 1588 PTP)* section of RM0385 reference manual.

2.5.4 From communication interfaces to DMA

Refer to *Section 2.6: DMA block*.

2.6 DMA block

Each stream is associated with a DMA request that can be selected out of 8 possible channel requests. The selection is controlled by the CHSEL [2:0 bits] of the DMA_SxCR register. The 8 requests from the peripherals (TIM, ADC, SPI, I2C, etc.) are independently connected to each channel and their connection depends on the product implementation.

This interconnection is explained in the following tables of RM0385 reference manual:

- *DMA1 request mapping*
- *DMA2 request mapping*

For more details on the DMA description, refer to *DMA general description* of RM0385 reference manual.

3 Application example

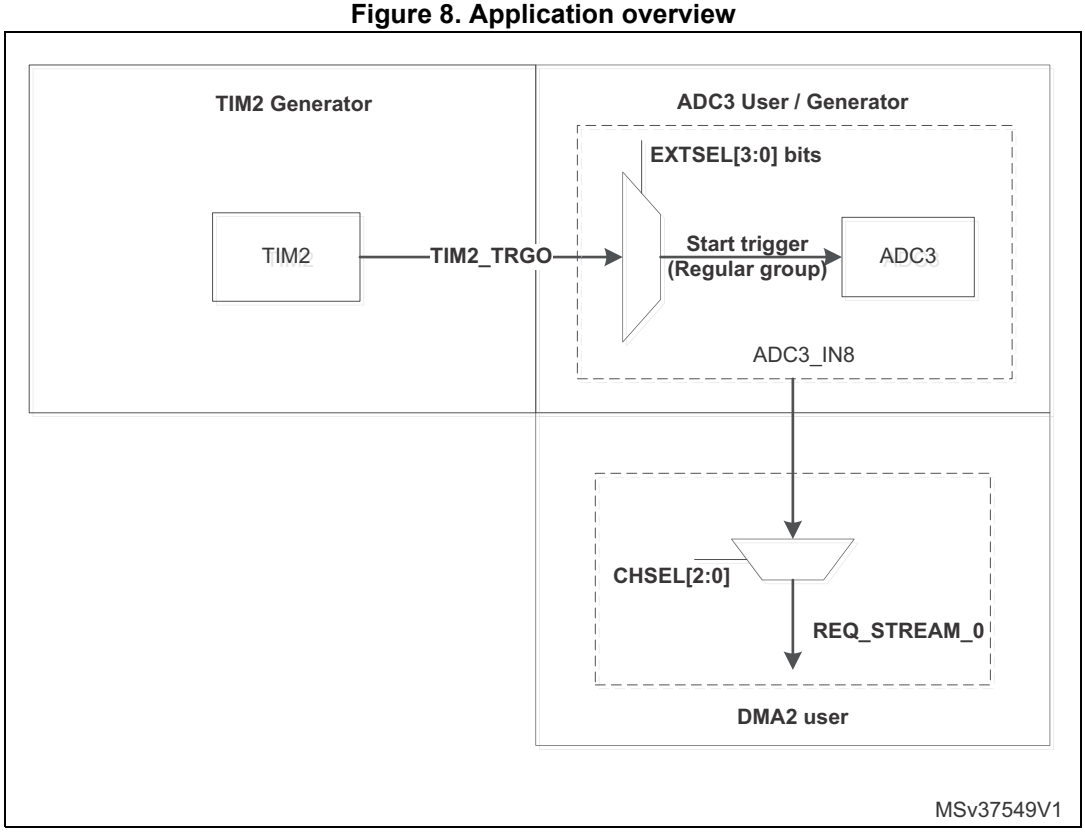
This application example demonstrates how to use the peripheral interconnect matrix on STM32F7 Series microcontrollers, how to set up ADC3 to start a single conversion at each TIM2 time overflow. At each end of conversion the DMA transfers the converted data from the ADC to the memory.

This application uses the STM32F7xx HAL API.

3.1 Hardware description

- TIM2 peripheral: used to generate an ADC trigger event
- ADC3 peripheral: used in Slave mode
- DMA2 peripheral: used to transmit data from the slave ADC3 to the memory

Figure 8. Application overview



3.2 Software description

The ADC3 is configured to start single conversions on the external trigger from TIM2. The output from TIM2 is on TIM2_TRGO signal. Each time an end of conversion occurs, the DMA transfers in normal mode the converted data from ADC3 DR register to the destination variable (uhADCxConvertedValue).

/* Enables ADC DMA request after last transfer (Single-ADC mode) and enables ADC peripheral*/

HAL_ADC_Start_DMA(&AdcHandle, (uint32_t*)&uhADCxConvertedValue, BUFFER_SIZE);

In this example: system clock = 216 MHz, APB2 = 108 MHz and ADC clock = APB2/4.

As ADC3 frequency is 25MHz, the sampling time is set to 3 cycles and the conversion time for a 12-bit data is 12 cycles so the total conversion time is (12+3)/25= 0.6 µs.

Table 2 presents the peripheral interconnect configurations.

Table 2. Peripheral interconnect configuration details

Interconnect	Code example	Comments

TIM2_TRGO selection	sMasterConfig.MasterOutputTrigger = TIM_TRGO_UPDATE;
	sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
	HAL_TIMEx_MasterConfigSynchronization(&htim, &sMasterConfig);
		Configures the Master TIM to generate a triggering event (TIM_TRGO_UPDATE).

ADC3 external trigger source	AdcHandle.Init.ExternalTrigConv = ADC_EXTERNALTRIGCONV_T2_TRGO AdcHandle.Init.ExternalTrigConvEdge = ADC_EXTERNALTRIGCONVEDGE_RISING; AdcHandle.Init.DMAContinuousRequests = ENABLE; HAL_ADC_Init(&AdcHandle) ;	The TIM2_TRGO event triggers conversion for regular group with rising edge. Since converted regular channel values are stored into a unique data register, the DMA mode is enabled.
DMA handle	HAL_LINKDMA(hadc, DMA_Handle, hdma_adc);	Associate the initialized DMA handle to the ADC handle.

4 Conclusion

This application note describes the peripheral interconnection features integrated into the STM32F7 Series that optimize the trade-off between the power efficiency and the high performance.

It also gives a description of a basic example of an autonomous communication between TIM2, ADC3 and DMA2 that can be used as a starting point to develop your own application.

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
30-Apr-2015	1	Initial release.
18-May-2015	2	Scope of the document changed from ST Restricted to public.
02-Jun-2015	3	Updated *Section 3.2: Software description* modifying the system clock at 216 MHz and APB2 at 108 MHz.