AN4660
Application note

Migration of microcontroller applications from STM32F42xxx/STM32F43xxx to STM32F74xxx/STM32F75xxx

Introduction

Designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product Series. Reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require to switch to smaller components and shrink the PCB area.

This application note is written as an help with the analysis of the steps involved when migrating from an existing STM32F42xxx/STM32F43xxx device to STM32F74xxx/STM32F75xxx device based design.

This application note provides a guideline on hardware migration and peripheral migration. To better understand the information inside this application note, the user should be familiar with the STM32 microcontroller family.

For additional information, please refer to STM32F42xxx/STM32F43xxx and STM32F74xxx/STM32F75xxx reference manuals (RM0090 and RM0385) and datasheets. Documents are available for download at *www.st.com*.

Table 1. Applicable products

Type	Part number
Microcontrollers	STM32F427AG, STM32F427AI, STM32F427IG, STM32F427II, STM32F427VG, STM32F427VI, STM32F427ZG, STM32F427ZI
	STM32F437AI, STM32F437IG, STM32F437II, STM32F437VG, STM32F437VI, STM32F437ZG, STM32F437ZI
	STM32F429AG, STM32F429AI, STM32F429BE, STM32F429BI, STM32F429IE, STM32F429IG, STM32F429II, STM32F429NE, STM32F429NI, STM32F429VE, STM32F429VG, STM32F429VI, STM32F429ZE, STM32F429ZG, STM32F429ZI
	STM32F439AI, STM32F439BG, STM32F439BI, STM32F439IG, STM32F439II, STM32F439JG, STM32F439NG, STM32F439NI, STM32F439VG, STM32F439VI, STM32F439ZG, STM32F439ZI
	STM32F745ZG, STM32F745VG, STM32F745ZE, STM32F745IE, STM32F745VE
	STM32F746VG, STM32F746ZG, STM32F746IG, STM32F746BG, STM32F746NG, STM32F746IE, STM32F746VE, STM32F746ZE, STM32F746BE, STM32F746NE
	STM32F756VG, STM32F756ZG, STM32F756IG, STM32F756BG, STM32F756NG

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1 Hardware migration

1.1 Pinout compatibility

The STM32F74xxx/F75xxx devices are fully pin-to-pin compatible with the STM32F42xxx/F43xxx devices except for the LQFP100 package, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

Figure 1. Incompatible board design for LQFP100 package

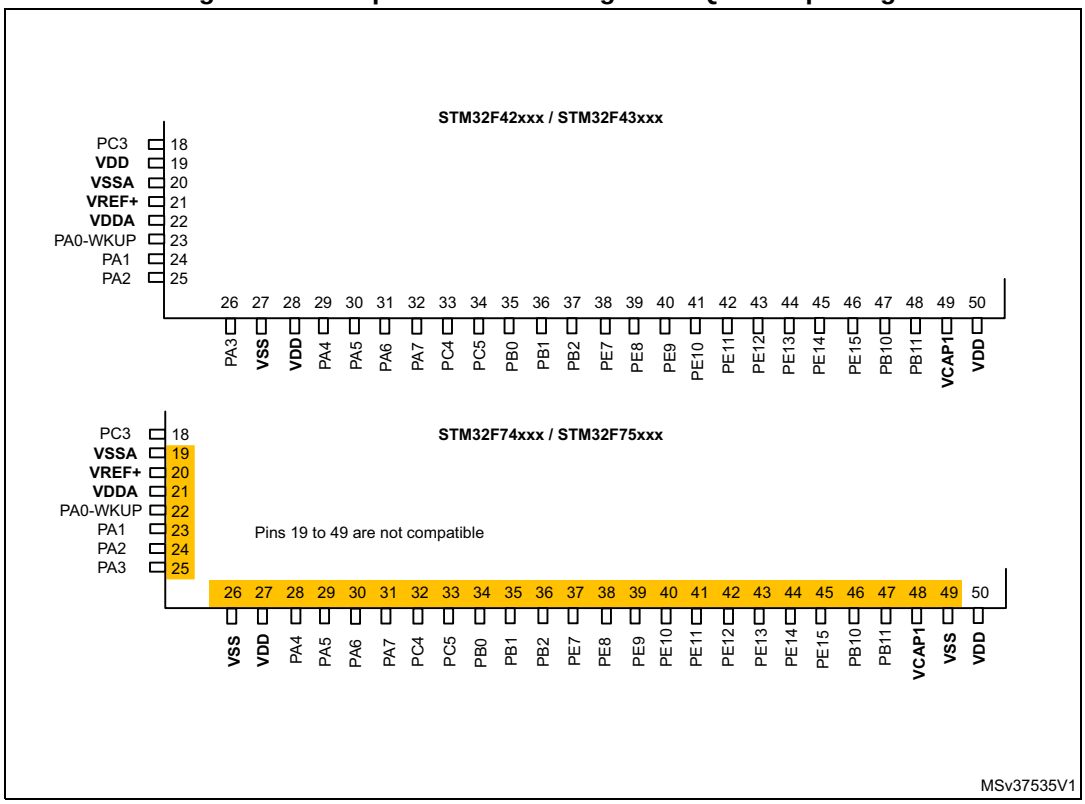

Table 2 presents the pinout differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx for the LQFP100 package.

Table 2. STM32F42xxx/F43xxx and STM32F74xxx/F75xxx pinout differences (LQFP100)

LQFP100	STM32F42xxx/F43xxx pinout	STM32F74xxx/F75xxx pinout
19	VDD	VSSA
20	VSSA	VREF+
21	VREF+	VDDA
22	VDDA	PA0-WKUP
23	PA0-WKUP	PA1
24	PA1	PA2

Table 2. STM32F42xxx/F43xxx and STM32F74xxx/F75xxx pinout differences (LQFP100) (continued)

LQFP100	STM32F42xxx/F43xxx pinout	STM32F74xxx/F75xxx pinout
25	PA2	PA3
26	PA3	VSS
27	VSS	VDD
28	VDD	PA4
29	PA4	PA5
30	PA5	PA6
31	PA6	PA7
32	PA7	PC4
33	PC4	PC5
34	PC5	PB0
35	PB0	PB1
36	PB1	PB2
37	PB2	PE7
38	PE7	PE8
39	PE8	PE9
40	PE9	PE10
41	PE10	PE11
42	PE11	PE12
43	PE12	PE13
44	PE13	PE14
45	PE14	PE15
46	PE15	PB10
47	PB10	PB11
48	PB11	VCAP1
49	VCAP1	VSS

1.2 Boot mode compatibility

The STM32F42xxx/F43xxx boot space is based on boot mode selection pins: BOOT0 and BOOT1 while STM32F74xxx/F75xxx is based on BOOT0 and boot address option bytes as described in *Table 3*.

For STM32F74xxx/F75xxx, the boot base address supports any address in the range from 0x0000 0000 to 0x2004 FFFF.

Table 3. Boot mode selection comparison between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

<table>
<tr><th colspan="4">STM32F74xxx/F75xxx</th></tr>
<tr><td colspan="2">Boot mode selection</td><td rowspan="2">Boot space</td></tr>
<tr><td>BOOT</td><td>Boot address Option Bytes</td></tr>
<tr><td>0</td><td>BOOT_ADD0 [15:0]</td><td>Boot address defined by user option byte BOOT_ADD0[15:0]
- ST programmed value: Flash on ITCM at 0x0020 0000</td></tr>
<tr><td>1</td><td>BOOT_ADD1 [15:0]</td><td>Boot address defined by user option byte BOOT_ADD1[15:0]
- ST programmed value: system bootloader at 0x0010 0000</td></tr>
<tr><th colspan="4">STM32F42xxx/F43xxx</th></tr>
<tr><td colspan="2">Boot mode selection Pins</td><td rowspan="2">Boot Mode</td><td rowspan="2">Aliasing</td></tr>
<tr><td>BOOT1</td><td>BOOT0</td></tr>
<tr><td>x</td><td>0</td><td>Main Flash memory</td><td>Main Flash memory is selected as the boot space at 0x0800 0000</td></tr>
<tr><td>0</td><td>1</td><td>System memory</td><td>System memory is selected as the boot space at 0x1FFF 0000</td></tr>
</table>

1.3 System bootloader

The system bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

Table 4 shows the supported communication peripherals by the system bootloader.

Table 4. STM32F42xxx/F43xxx and STM32F74xxx/F75xxx bootloader communication peripherals

System bootloader peripherals	STM32F42xxx/F43xxx I/O pin	STM32F74xxx/F75xxx I/O pin
DFU	USB OTG FS (PA11 / PA12) in device mode	
USART1	PA9 / PA10	
USART3	PB10 / PB11 and PC10 / PC11	
CAN2	PB5 / PB13	
I2C1	NA	PB6 / PB9
I2C2	NA	PF0 / PF1
I2C3	NA	PA8 / PC9

By default, in STM32F74xxx/F75xxx, when the boot from system bootloader is selected, the code is executed from ITCM interface. It could be reprogrammed by option byte executed from AXIM interface. For more details on system bootloader refer to AN2606.

2 Peripheral migration

2.1 STM32 product cross-compatibility

The STM32 Series embed a set of peripherals which can be classed in three categories:

- The first category is for the peripherals which are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals which are shared by all STM32 products but have only minor differences (in general to support new features), so migration from one product to another is very easy and does not need any significant new development effort.
- The third category is for peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, the migration will require a new development at application level.
- The SW compatibility mentioned in the *Table 5* only refers to the register description for "low level" drivers.

The Cube Hardware Abstraction Layer (HAL) is compatible between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 5 shows STM32 peripheral compatibility between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 5. STM32 peripheral compatibility analysis STM32F42xxx/F43xxx versus STM32F74xxx/F75xxx

Peripherals		STM32F42xxx/ F43xxx	STM32F74xxx/ F75xxx	Compatibility	
-		-	-	SW	Comments
Flash memory in Kbyte		2048	1024	-	-
SRAM(KB)	System	256 (115+16+64+64)	320 (240+16+64)		
	Instruction	NA	16		
	Backup	4	4		
Timers	GP	10	10	Yes	-
	Advanced control	2	2	Yes	-
	Basic	2	2	Yes	-
	Low-power	NA	1	NA	-

Table 5. STM32 peripheral compatibility analysis STM32F42xxx/F43xxx versus STM32F74xxx/F75xxx (continued)

Peripherals		STM32F42xxx/ F43xxx	STM32F74xxx/ F75xxx	Compatibility	
Communication interfaces	QuadSPI	No	Yes	NA	-
	SPI / I2S	6/2 (full duplex)	4/3 (simplex) 6/3 (simplex)(1)	No / Yes	I2S compatible.
	I2C	3	4	No	Programmable clock source for STM32F74xxx/F75xxx
	USART/UART	4/4	4/4	No	Additional features on STM32F74xxx/F75xxx
	USB OTG FS	Yes	Yes	No	Dedicated VDDUSB More endpoints on STM32F74xxx/F75xxx
	USB OTG HS	Yes	Yes	No	More endpoints and host channels
	CAN	2	2	Yes	-
	SAI	1	2	Yes	-
	SDIO/SDMMC1	Yes	Yes	Yes	New clock source for SDMMC1 on STM32F74xxx/F75xxx
	SPDIFRX	No	4 inputs	NA	-
RNG		Yes	Yes	Yes	-
FMC memory controller		Yes	Yes	Yes	-
Ethernet		Yes	Yes	Yes	-
HDMI-CEC		No	Yes	NA	-
DCMI		Yes	Yes	Yes	-
WWDG		Yes	Yes	Yes	-
IWDG		Yes	Yes	Yes	-
CRC		Yes	Yes	Yes	Additional features on STM32F74xxx/F75xxx
LCD-TFT		No | Yes(2)	Yes	Yes	-
DMA		DMA1-DMA2 (8 stream each)		Yes	-
Chrom-ART-Acc (DMA2D)		Yes	Yes	Yes	-
Crypto		Yes	Yes	Yes	-
Hash		Yes	Yes	Yes	-
GPIO		Up to 168	Up to 168	Yes	-
ADC	12 bits	3	3	Yes	ADC Timer Trigger not compatible
	Number of channels	16|24	16|24		

Table 5. STM32 peripheral compatibility analysis STM32F42xxx/F43xxx versus STM32F74xxx/F75xxx (continued)

Peripherals		STM32F42xxx/ F43xxx	STM32F74xxx/ F75xxx	Compatibility	
DAC	12 bits	Yes	Yes	Yes	-
	Number of channels	2	2		
EXTI		Yes	Yes	Yes	New EXTI line for LPTIM1
RCC		Yes	Yes	Yes	New LSE drive modes.
RTC		Yes	Yes	Yes	Additional features on STM32F74xxx/F75xxx
PWR		Yes	Yes	Yes	New wakeup pins with configurable polarity on STM32F74xxx/F75xxx
SYSCFG		Yes	Yes	Yes	-

1. SPI / I2S:

- 4/3 for 100 pin package and 6/3 for other packages.

2. LCD - TFT:

- No: not available for STM32F437xx.

- Yes: available for STM32F439xx.

2.2 Memory mapping

Table 6 presents the peripheral address mapping differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 6. IP bus mapping differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

Peripheral	Bus	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
		Base address	Base address
QuadSPI control register	AHB3	NA	0xA000 1000 - 0xA0001FFF
SAI2	APB2	NA	0x4001 5C00 - 0x4001 5FFF
HDMI-CEC	APB1	NA	0x4000 6C00 - 0x4000 6FFF
I2C4		NA	0x4000 6000 - 0x4000 63FF
I2S3ext		0x4000 4000 - 0x4000 43FF	NA
SPDIFRX		NA	0x4000 4000 - 0x4000 43FF
I2S2ext		0x4000 3400 - 0x4000 37FF	NA
LPTIM1		NA	0x4000 2400 - 0x4000 27FF

2.3 Flash memory

Table 7 presents the differences between the Flash memory interface of STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

The STM32F74xxx/F75xxx devices instantiate a different Flash module both in terms of architecture and interface. For more information on programming, erasing and protection of the STM32F74xxx/F75xxx Flash memory, please refer to the STM32F74xxx and STM32F75xxx reference manual (RM0385).

Table 7. Flash memory differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

Flash		STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Main/program memory		0x0800 0000 – 0x081F FFFF	0x0800 0000 - 0x080F FFFF (on AXIM interface)
		– Up to 2 Mbyte – Split in 2 Banks – 4 sectors of 16 Kbyte – 1 sector of 64 Kbyte – 6 sectors of 128 Kbyte	– Up to 1 Mbyte – Split in 1 Bank – 4 sectors of 32 Kbyte – 1 sector of 128 Kbyte – 3 sectors of 256 Kbyte
Features		– 128 bit wide data read – Read while Write (RWW)	– 256 bit wide data read
Wait State		Up to 8 (depending on the supply voltage and frequency)	Up to 9 (depending on the supply voltage and frequency)
One time programmable (OTP)		512 OTP bytes	1024 OTP bytes
Flash interface register		0x4002 3C00 - 0x4002 3FFF	
Option Bytes	Base address	0x1FFF C000 - 0x1FFF C00F 0x1FFE C000 - 0x1FFE C00F	0x1FFF 0000 - 0x1FFF 001F (on AXIM interface)
Option Bytes	FLASH_ OPTCR register	– Bit 31 SPRMOD – Bit 30 DB1M – Bits 29:28 Reserved – Bits 27:16 nWRP[11:0] – Bits 15:8 RDP – Bits 7:5 USER - Bit 7: nRST_STDBY - Bit 6: nRST_STOP - Bit 5: WDG_SW – Bit 4 BFB2 – Bits 3:2 BOR_LEV – Bit 1 OPTSTRT – Bit 0 OPTLOCK	– Bit 31 IWDG_STOP – Bit 30 IWDG_STDBY – Bits 29:24 Reserved – Bits 23:16 nWRP[7:0] – Bits 15:8 RDP[7:0] – Bits 7:4 USER - Bit 7: nRST_STDBY - Bit 6: nRST_STOP - Bit 5: IWDG_SW – Bit 4: WWDG_SW – Bits 3:2 BOR_LEV[1:0] – Bit 1 OPTSTRT – Bit 0 OPTLOCK

2.4 Embedded Flash memory

The main memory and information block organization are shown in *Table 8*.

Table 8. Flash module 1 Mbyte single bank organization (STM32F74xxx/F75xxx)

Block	Name	Bloc base addresses on AXIM interface	Block base addresses on ITCM interface	Sector size
Main memory block	Sector 0	0x0800 0000 - 0x0800 7FFF	0x0020 0000 - 0x0020 7FFF	32 KB
	Sector 1	0x0800 8000 - 0x0800 FFFF	0x0020 8000 - 0x0020 FFFF	32 KB
	Sector 2	0x0801 0000 - 0x0801 7FFF	0x0021 0000 - 0x0021 7FFF	32 KB
	Sector 3	0x0801 8000 - 0x0801 FFFF	0x0021 8000 - 0x0021 FFFF	32 KB
	Sector 4	0x0802 0000 - 0x0803 FFFF	0x0022 0000 - 0x0023 FFFF	128 KB
	Sector 5	0x0804 0000 - 0x0807 FFFF	0x0024 0000 - 0x0027 FFFF	256 KB
	Sector 6	0x0808 0000 - 0x080B FFFF	0x0028 0000- 0x002B FFFF	256 KB
	Sector 7	0x080C 0000 - 0x080F FFFF	0x002C 0000 - 0x02F FFFF	256 KB
Information block	System memory	0x1FF0 0000 - 0x1FF0 EDBF	0x0010 0000- 0x0010 EDBF	60 Kbyte
	OTP	0x1FF0 F000 - 0x1FF0 F41F	0x0010 F000 - 0x0010 F41F	1024 byte
	Option bytes	0x1FFF 0000 - 0x1FFF 001F	-	32 byte

2.5 Flexible memory controller (FMC)

Table 9 presents the FMC differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 9. FMC differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

FMC		STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
External memory interfaces		– SRAM – NOR/NAND memories – PSRAM – Two banks of NAND Flash memory with ECC hardware – 16-bit PC Card compatible devices	– SRAM – NOR/NAND memories – PSRAM – NAND Flash memory with ECC hardware
Data bus width		8-,16- or 32-bit	
FMC Bank memory mapping	Bank1 4×64MB	NOR/PSRAM/SRAM	NOR/PSRAM/SRAM
	Bank2 4×64MB	NAND Flash memory	Reserved
	Bank3 4×64MB		NAND Flash memory
	Bank4 4×64MB	PC Card	Reserved
	SDRAM bank1 4×64MB	SDRAM	SDRAM
	SDRAM bank2 4×64MB		
Memory mapping swap: (SYSCFG_MEMRMP) Bits 11:10 SWP_FMC[1:0] = 01b		NOR/PSRAM/SRAM 256MB	SDRAM bank1 256MB
		NAND bank1 256MB	SDRAM bank2 256MB
		SDRAM bank1 256MB	NAND bank3 256MB
		SDRAM bank2 256MB	Reserved
		Reserved	Reserved
		NAND bank2 256MB	NOR/PSRAM/SRAM 256MB
		PC card 256MB	Reserved

2.6 Interrupt vectors

Table 10 presents the interrupt vector differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 10. Interrupt vector differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

Position	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
91	NA	SAI2
92	NA	QuadSPI
93	NA	LPTIM1
94	NA	HDMI-CEC
95	NA	I2C4_EV
96	NA	I2C4_ER
97	NA	SPDIFRX

2.7 External interrupt lines (EXTI)

Table 11 presents the EXTI line differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 11. EXTI line differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

EXTI line	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
0 to 15	16 external interrupt lines	
16	PVD output	
17	RTC alarm event	
18	USB OTG FS wakeup event	
19	Ethernet wakeup event	
20	USB OTG HS (configured in FS) wakeup event	
21	RTC tamper and TimeStamp events	
22	RTC wakeup event	
23	NA	LPTIM1 asynchronous event

2.8 RCC

Table 12 presents the main differences related to the RCC (Reset and Clock Controller) between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 12. RCC differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

Peripherals	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
	Clock sources	
USB OTG FS	– PLL48MHz derived from main PLL VCO (PLLQ Clock)	– PLL48MHz derived from main PLL VCO (PLLQ Clock) – PLLSAI VCO (PLLSAI clock)
RNG		
SDIO/SDMMC1	– PLL48CLK	– PLL48CLK – SYSCLK
U(S)ARTs	– APB1 or APB2 clock (PCLK1 or PCLK2)	– System clock (SYSCLK) – HSI clock – LSE clock – APB1 or APB2 clock (PCLK1 or PCLK2)
I2Cs	– APB1 clock (PCLK1)	– System clock (SYSCLK) – HSI clock – APB1 or APB2 clock (PCLK1 or PCLK2)
I2S	– PLLI2S – External clock mapped on I2S_CKIN pin	
SAI1	– PLLI2S_Q – PLLSAI_Q – External clock mapped on the I2S_CKIN pin.	
SAI2	NA	– PLLI2S_Q – PLLSAI_Q – External clock mapped on the I2S_CKIN pin.
LTDC	– PLLSAI_R	
LPTIM1	NA	– LSI clock – LSE clock – HSI clock – APB1 clock (PCLK1)
USB OTG HS	– 24 to 60 MHz to external PHY	
ETHERNET MAC	– 25 to 50 MHz external PHY	
SPDIFRX	NA	– PLLI2SP VCO
HDMI-CEC	NA	– LSE clock – HSI clock divided by 488

Table 12. RCC differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx (continued)

Peripherals	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
	Clock sources	
RTC	– LSE clock – LSI clock – HSE clock divided by 32	
IWDG	LSI	
LSE	NA	Configurable LSE drive in RCC_BDCR register: LSEDRV[1:0]: – 00: Low drive – 10: Medium low drive – 01: Medium high drive – 11: High drive
RCC dedicated clock configuration register	– RCC_DCKCFGR	– RCC_DKCFGR1 – RCC_DKCFGR2

2.8.1 Maximum frequency according to power scale parameter

Table 13 shows the comparison of maximum frequency that the MCU can reach between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 13. Maximum frequency comparison between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

Symbol	Parameter	Conditions		F4 max Freq	F7 max Freq	Unit
fHCLK	Internal AHB clock frequency	Power scale 3 (Over-drive OFF)		120	144	MHz
		Power scale 2	Over-drive OFF	144	168	
			Over-drive ON	168	180	
		Power scale 1	Over-drive OFF	168	180	
			Over-drive ON	180	216	
fPCLK1	Internal APB1 clock frequency	Over-drive OFF		42	45	
		Over-drive ON		45	54	
fPCLK2	Internal APB2 clock frequency	Over-drive OFF		84	90	
		Over-drive ON		90	108	

2.9 PWR

Table 14 presents the PWR controller differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 14. PWR differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

PWR	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Power supplies	NA	– Independent USB transceivers supply: VDDUSB: range is from 3.0 V to 3.6 V and is completely independent from VDD or VDDA
Standby mode wakeup sources	– WKUP pin PA0 on rising edge – RTC event (RTC ALARM, Tamper event,Time stamp event) – IWDG reset – External reset in NRST pin	– WKUP pin with configurable polarity on rising or falling edge: – PA0 – PA2 – PC1 – PC13 – PI8 – PI11 – RTC event (RTC ALARM, tamper event, time stamp event) – IWDG reset – External reset in NRST pin
Power control registers	PWR_CR PWR_CSR	PWR_CR1 PWR_CSR1
	NA	PWR_CR2 PWR_CSR2 Comment : – PWR_CR2: Used to configure the wakeup pin polarity, or to clear the wakeup pins flags. – PWR_CSR2: Used either to enable the wakeup pins or used to detect an event on the wakeup pin

2.10 RTC

Table 15 shows the RTC comparison between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 15. RTC comparison between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

RTC	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Calendar in BCD	Yes	
Calendar sub seconds access	Yes Resolution down to RTCCLK	
Calendar synchronization on the fly	Yes	
Alarm on calendar	2 w/ subseconds	
Calendar calibration	Calibration window: 8s/16s/32s Calibration step: 3.81ppm/1.91ppm/0.95 ppm Range [-480ppm +480ppm]	
Synchronization on mains	Yes	
Periodic wakeup	Yes	
Timestamp	Yes Sec, Min, Hour, Date, Sub seconds	
Timestamp on VBAT switch	No	Yes
Tamper	2 pins/ 2 events	3 pins/ 3 events
	Edge or level detection with configurable filtering	
External interrupt and trigger with filtering	No	Yes
32-bit backup registers	20	32
RTC in VBAT	Yes	

2.11 U(S)ART

The U(S)ART is not SW compatible with STM32F42xxx/F43xxx and includes new additional features detailed in *Table 16*.

Table 16. U(S)ART differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

U(S)ART	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
UART/USART	4/4	
Baud rate	– Up to 4x11.25 Mbit/s	– Up to 13.5 Mbit/s – (clock frequency is 100 MHz and oversampling is by 8)
Clock	– Single clock domain	– Dual clock domain: Convenient baud rate programming independent from the PCLK reprogramming
Data	– Word length: Programmable (8 or 9 bits)	– Word length: Programmable (7, 8 or 9 bits) – Programmable data order with MSB-first or LSB-first shifting
interrupt	– 10 interrupt sources with flags	– 14 interrupt sources with flags
Features	– LIN mode – SPI Master – IrDA SIR ENDEC block – Hardware flow control (CTS/RTS) – Continuous communication using DMA – Multiprocessor communication – Single-wire half-duplex communication	
	Smartcard mode T = 0 and T= 1 has to be implemented by software. Number of stop bits: 0.5, 1, 1.5, 2	Support the T=0 and T=1 asynchronous protocols. Number of stop bits: 1, 1.5, 2 smartcard operation.
	NA	– Support for ModBus communication - Timeout feature - CR/LF character recognition – Receiver timeout interrupt – Auto baud rate detection – Driver Enable – Swappable Tx/Rx pin configuration
U(S)ART registers	– Software not compatible	

2.12 I2C

The STM32F42xxx/F43xxx and STM32F74xxx/F75xxx share the same features on the I2C, but the software and register configuration are not compatible.

Table 17 presents the I2C differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 17. I2C differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

I2C	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Instances	– x3 (I2C1, I2C2, I2C3)	– x4 (I2C1, I2C2, I2C3, I2C4)
Features	– 7-bit and 10-bit addressing mode – SMBus – Standard mode (up to 100 kbit/s) – Fast mode (up to 400 kbit/s)	
	– Single clock source	– Programmable clock source
I2C registers	– Software not compatible.	

2.13 SPI

The STM32F42xxx/F43xxx and STM32F74xxx/F75xxx implement different features on the SPI.

Table 18 presents the SPI differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 18. SPI differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

SPI	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Instances	x6	x4 | x6
Features	SPI + I2S	
Data size	Fixed, configurable to 8 or 16 bits	Programmable from 4 to 16-bit
Data buffer	Tx & Rx 16-bit buffers (single data frame)	Two 32-bit embedded Rx and Tx FIFOs (up to 4 data frames)
Data packing	No (16-bit access only)	Yes
Mode	SPI TI mode SPI Motorola mode	SPI TI SPI Motorola mode NSSP mode
Speed	up to 45Mbits/s	Up to 50Mbits/s (TBC)
SPI registers	Software not compatible	

2.14 CRC

The STM32F74xxx/F75xxx implements similar CRC (Cyclic redundancy check) calculation unit as STM32F42xxx/F43xxx.

Table 19 presents the CRC differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 19. CRC differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

CRC	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Features	– Single input/output 32-bit data register – CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size – General-purpose 8-bit register (can be used for temporary storage)	
	– Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7 – Handles 32-bit data size	– Fully programmable polynomial with programmable size (7, 8, 16, 32bits) – Handles 8-,16-, 32-bit data size – Programmable CRC initial value – Input buffer to avoid bus stall during calculation – Reversibility option on I/O data
CRC registers	– Software compatible. – STM32F74xxx/F75xxx include new features.	

2.15 USB OTG

Table 20 presents USB OTG differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

Table 20. USB OTG differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

USB	STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Features	– Universal Serial Bus revision 2.0 – Full support for the USB On-The-Go (USB OTG).	
	FS mode: – 1 bidirectional control endpoint – 3 IN endpoints (bulk, interrupt, isochronous) – 3 OUT endpoints (bulk, interrupt, isochronous HS mode: – 6 bidirectional endpoints (including EP0) – 12 host mode channels	FS mode: – 1 bidirectional control endpoint – 5 IN endpoints (bulk, interrupt, isochronous) – 5 OUT endpoints (bulk, interrupt, isochronous) HS mode: – 8 bidirectional endpoints (including EP0) – 16 host channels with periodic
	– USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line.	
	NA	– Independent VDDUSB power supply allowing lower VDDCORE while using USB.
Buffer memory	FS mode: – 1.25Kbytes data FIFOs – Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO. HS mode: – 4 KB total RAM	FS mode: – 1.25Kbytes data FIFOs – Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO. HS mode: – 4 KB total RAM
Low-power modes	FS mode: – USB suspend and resume HS mode: – No LPM supported	FS mode: – USB suspend and resume – Link power management (LPM) support HS mode: – Yes LPM supported
Configuration	– SW not compatible	

2.16 ADC

The STM32F74xxx/F75xxx devices embed the same ADC peripherals with the same features except for external triggers in regular and injected channels.

Table 21 and *Table 22* present the differences of external trigger for regular channels and injected channels between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx.

2.16.1 External trigger for regular channels

Table 21. External trigger for regular channel differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

Type	EXTSEL[3:0]	Source	
		STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Internal signal from on-chip timers	0000	TIM1_CH1 event	TIM1_CC1 event
	0001	TIM1_CH2 event	TIM1_CC2 event
	0010	TIM1_CH3 event	TIM1_CC3 event
	0011	TIM2_CH2 event	TIM2_CC2 event
	0100	TIM2_CH3 event	TIM5_TRGO event
	0101	TIM2_CH4 event	TIM4_CC4 event
	0110	TIM2_TRGO event	TIM3_CC4
	0111	TIM3_CH1 event	TIM8_TRGO event
	1000	TIM3_TRGO event	TIM8_TRGO(2) event
	1001	TIM4_CH4 event	TIM1_TRGO event
	1010	TIM5_CH1 event	TIM1_TRGO(2) event
	1011	TIM5_CH2 event	TIM2_TRGO event
	1100	TIM5_CH3 event	TIM4_TRGO event
	1101	TIM8_CH1 event	TIM6_TRGO event
	1110	TIM8_TRGO event	NA
External pin	1111	EXTI line11	

2.16.2 External trigger for injected channels

Table 22. External trigger for injected channel differences between STM32F42xxx/F43xxx and STM32F74xxx/F75xxx

Type	EXTSEL[3:0]	Source	
		STM32F42xxx/F43xxx	STM32F74xxx/F75xxx
Internal signal from on-chip timers	0000	TIM1_CH4 event	TIM1_TRGO event
	0001	TIM1_TRGO event	TIM1_CC4 event
	0010	TIM2_CH1 event	TIM2_TRGO event
	0011	TIM2_TRGO event	TIM2_CC1 event
	0100	TIM3_CH2 event	TIM3_CC4 event
	0101	TIM3_CH4 event	TIM4_TRGO event
	0110	TIM4_CH1 event	NA
	0111	TIM4_CH2 event	TIM8_CC4 event
	1000	TIM4_CH3 event	TIM1_TRGO(2) event
	1001	TIM4_TRGO event	TIM8_TRGO event
	1010	TIM5_CH4 event	TIM8_TRGO(2) event
	1011	TIM5_TRGO event	TIM3_CC3 event
	1100	TIM8_CH2 event	TIM5_TRGO event
	1101	TIM8_CH3 event	TIM3_CC1 event
	1110	TIM8_CH4 event	TIM6_TRGO event
External pin	1111	EXTI line15	NA

3 Conclusion

This application note is a useful complement to the datasheets and reference manuals, which gives a simple guideline to migrate from an existing STM32F42xxx/F43xxx device to STM32F74xxx/F75xxx device.

4 Revision history

Table 23. Document revision history

Date	Revision	Changes
31-Mar-2015	1	Initial release.
26-May-2015	2	Updated: – *Section 2.1: STM32 product cross-compatibility* with a new paragraph about software compatibility, – *Table 5: STM32 peripheral compatibility analysis STM32F42xxx/F43xxx versus STM32F74xxx/F75xxx* for RNG, ADC, and DAC peripherals, – *Section 2.8.1: Maximum frequency according to power scale parameter* setting F7 max at 216 MHz, 108 MHz and 54 MHz in over-drive ON conditions, – *Section 2.11: U(S)ART* with baud rate up to 13.5 Mbit/s.