Power Electronics - 12V Universal Supply Design and Measurement Report

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1 Introduction/Specification

Our project proposed for the power electronics course unit was the universal 12V power supply. The original specifications were as follows:

• Output voltage: 12V

• Input voltage: min. 5V; max. 18V

• Output Current: 1A

Considering these, the team attempted to overdimension the circuit in order to output more current (2A) and accept a higher range of input voltages (min. 5V and max. 24V).

2 Design

2.1 Circuit

As the basis for the design, the LM5175 buck-boost converter controller by Texas Instruments [1] was chosen. Since the design requires 2A of output current, a externally switched solution is a safer approach and as such the LM5175 presents a relatively modern design without many features such as I²C that would not be utilized. Also the four switch buck-boost converter approach as some advantages over traditional single or dual switch topologies, since at any given time two of the MOSFETs are in either on or off state while the other commutate. This has the benefit that no diodes are needed, and thus lower forward voltage drops are present in both modes of operation.

An example circuit schematic for the circuit can be seen in figure 1. The circuit developed is based around this initial design and uses follows the dimensioning procedure that is described in the IC's datasheet [1].

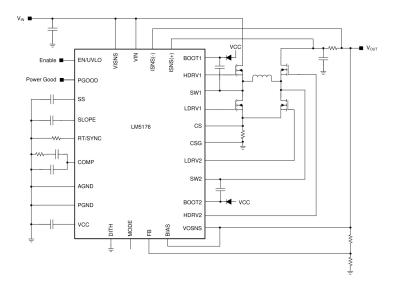


Figure 1: Simplified LM5175 Schematic

As for the final schematic, a simplified version without connectors and testpoints can be found at the end of this document as an appendix.

2.1.1 Switching Frequency

The LM5175's switching frequency can be programmed between 100 and 600 kHz using a resistor from the RT/SYNC pin to ground. Higher values lead to higher overall efficiency but with added EMI and noise. The switching frequency was chosen to be $300 \rm kHz$, as most examples featured in the datasheet used this value.

$$R_T = \frac{1/F_{SW} - 190\text{ns}}{116\text{pF}} = 27.4\text{k}\Omega \tag{1}$$

2.1.2 Feedback Network

The output voltage of the circuit is set using a the feedback network between the output and the IC's FB pin.

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{out} - 0.8}{0.8} = 14\tag{2}$$

Choosing E48 series resistor values, a perfect ratio can be obtained:

$$R_{FB1} = 7.5 \text{k}\Omega; R_{FB2} = 105 \text{k}\Omega$$

2.1.3 Inductor Selection

The target inductance for Buck mode is given by the following formula:

$$L_{buck} = \frac{(V_{inMAX} - V_{out})V_{out}}{0.4I_{outMAX}F_{SW}V_{inMAX}} = 25\mu\text{H}$$
(3)

And the target for boost mode is the following:

$$L_{boost} = \frac{V_{inMIN}^2(V_{out} - V_{inMIN})}{0.3I_{outMAX}F_{SW}V_{out}^2} = 4.93\mu\text{H}$$

$$\tag{4}$$

The maximum average inductor current is the following if we assume 90% efficiency:

$$I_{Lmax} = \frac{V_{out}I_{outMAX}}{0.9V_{inMIN}} = 6.66A \tag{5}$$

Given this, the datasheet actually under specifies this component. A $4.7\mu\mathrm{H}$ inductor can be utilized and as such, the XAL1010-472MED from Coilcraft [4] was chosen.

As for the peak inductor following through the inductor it is:

$$I_{Lpeak} = I_{Lmax} + \frac{V_{inMIN}(V_{out} - V_{inMIN})}{2L_1 F_{sin} V_{out}} \approx 6.66$$
 (6)

2.1.4 Output Capacitors

The value for the main output capacitor can be determined by the capacitive ripple voltage:

$$\Delta V_{ripple} = \frac{I_{out}(1 - \frac{V_{inMIN}}{V_{out}})}{C_{out}F_{SW}} \tag{7}$$

And so, for a 10mV ripple from the capacitor, a value of $444.44\mu F$ is required. As such $C_{out} = 470\mu F$, which can be achieved with a small electrolytic capacitor. For this purpose Panasonic's 25SPVK470M Polymer Aluminum capacitor was chosen, which has a maximum voltage rating of 25V and a ESR of $14\text{m}\Omega$.

Along side this, three smaller $15\mu F$ tantalum capacitors are placed in parallel, such as to minimize output ESR. So, the TPSA156K006R0700 from Kyocera Avx was chosen, each featuring an ESR of $7m\Omega$.

For the boost mode of operation the RMS current through the capacitor is given by:

$$I_{Cout_{RMS}} = I_{out} \sqrt{\frac{V_{out}}{V_{in}} - 1}$$
 (8)

2.1.5 Input Capacitors

As for the input capacitors, in the buck operating region, they need to be able to supply high ripple current. It's RMS current is given by the following equation, where the worst case scenario of D=0.5 should be considered:

$$I_{C_{in}rms} = I_{out}\sqrt{D(1-D)} = 1A \tag{9}$$

So in a similar fashion as for the output, a bulk electrolytic capacitor of $68\mu F$ was placed in parallel with several $15\mu F$ tantalum capacitors. The bulk capacitor chosen was the Panasonic EEHZT1J680P featuring a maximum voltage rating of 63V and a ESR of $25 \mathrm{m}\Omega$.

2.1.6 Current Limit

The circuit's current limit is set by the R_{sense} resistor at the tail of the 4 mosfet switch bridge.

$$R_{senseBUCK} = \frac{80\text{mV}}{I_{outMAX}} = 40\text{m}\Omega \tag{10}$$

$$R_{senseBOOST} = \frac{120\text{mV}}{I_{Lpeak}} = 18\text{m}\Omega \tag{11}$$

This value is then set to $R_{sense} = 18 \text{m}\Omega$ based on the boost mode operation. The power loss experienced by the R_{sense} is the following:

$$P_{senseMAX} = \left(\frac{120mV}{R_{sense}}\right)^2 R_{sense} \left(1 - \frac{V_{inMIN}}{V_{out}}\right) = 0.53W$$
 (12)

Hence a 1W sense resistor is sufficient. As for the sense lines R_{CS} and R_{CSG} the values were chosen according to the example schematic provided on the datasheet: $R_{CS} = R_{CSG} = 100\Omega$. A filter capacitor is also needed to attenuate the noise that can occur in these lines due to the large amounts of current passing through R_{sense} , as such a 47pF capacitor is utilized as a part of a differential mode filter in the CS and CSG pins to the LM5175.

2.1.7 MOSFETs

The LM5175 features four built-in N-channel MOSFET gate drivers. In buck operation, QL1 and QH1 are switched by the IC's PWM controller while QH2 is continuously on and QL2 off. As for boost operation, QL2 and QH2 are switching while QH1 remains continuously on and QL2 is off.

For the QH1 and QL2 MOSFETs on the input side, these need to withstand the maximum input voltage of the circuit, plus the possible voltage transient spikes. Considering the extended specifications, this value comes to $V_{DS_{max}} \ge 24 + 20V$. As for the output, transistors QH2 and QL2 should be rated for 12V plus the transient spikes. When choosing a MOSFET for this circuit, it is also important to consider the rise/fall time and gate charges of the transistor, in order to minimize switching time and thus minimize switching loss. Also, the drain-to-source on-resistance should be minimal in order to lower the conduction losses.

Considering these requirements, the MOSFET chosen for the 4 switches was the Texas Instruments' CSD18532Q5B n-channel MOSFET [2], claiming to feature maximum V_{gs} of 60V and ultra-low gate charges.

2.1.8 Frequency Compensation

At the maximum load of 2A, output resistance is $R_{out} = V_{out}/I_{outMAX}6\Omega$

$$f_{p1(boost)} = \frac{2}{2\pi R_{out} C_{out}} = 112 \text{Hz}$$
 (13)

$$f_{z1} = \frac{1}{2\pi R_{esr} C_{out}} = 226 \text{Hz}$$
 (14)

The boost power stage RHP zero location is given by:

$$f_{RHP} = \frac{R_{out}(1 - D_{max})^2}{2\pi L_1} = 22.57 \text{kHz}$$
 (15)

Where D_{max} is the maximum duty cycle at the minimum V_{in} : $D = 1 - \frac{V_i}{V_o} = 0.667$

$$f_{p1(buck)} = \frac{1}{2\pi R_{out} C_{out}} = 56.4379 \tag{16}$$

From these, it is clear that the RHP zero is the main factor limiting the achievable bandwidth.

$$f_{bw} = \frac{f_{RHP}}{3} = 7.52 \text{kHz}$$
 (17)

The compensation zero can be placed at 1.5 times the boost frequency pole.

$$f_{zc} = 1.5 f_{p1(boost)} = 168 \text{Hz}$$
 (18)

Then the values for R_{c1} , C_{c1} and C_{c2} can be figured out through the following expressions:

$$R_{c1} = \frac{2\pi f_{bw}}{gm_{EA}} \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \frac{A_{cs}R_{sense}C_{out}}{1 - D_{max}} = 68656\Omega \approx 68k\Omega$$
 (19)

$$C_{c1} = \frac{1}{2\pi f_{rc} R_{c1}} = 13.79 \text{nF} \approx 13 \text{nF}$$
 (20)

$$C_{c2} = \frac{1}{2\pi 5 f_{bw} R_{c1}} = 61.65 \text{pF} \approx 62 \text{pF}$$
 (21)

2.1.9 Boilerplate Circuitry

In order to turn-on the IC, an appropriate voltage divider has to be built around the Enable/UVLO pin of the LM5175, which also functions as an undervoltage lockout, providing hysteresis between the turn-on and turn-off voltages. Using the following equation, the E96 values for the resistors can be calculated:

$$\begin{cases} V_{UV} = V_{en} \left(1 + \frac{R_{UV1}}{R_{UV2}} \right) - R_{UV2} I_{en} \\ R_{UV1} = 59 \text{k}\Omega; R_{UV1} = 249 \text{k}\Omega \end{cases}$$
 (22)

The LM5175 also features what is called soft start, which charges an external capacitor whenever the converter is powered up, replacing the internal reference voltage for the feedback in the error amplifier. Once fully charged, the internal error amplifier is then referenced to V_{ref} again.

A 20ms soft-start should be plenty for this circuit:

$$\begin{cases} I_{ss} = 5\mu A \\ C_{ss} = \frac{t_{ss}I_{ss}}{V_{ref}} = 125\text{nF} \approx 120\text{nF} \end{cases}$$
 (23)

Apart from the frequency compensation dimensioned previously, slope compensation is also an important step in the design of any current-mode controlled converters in order to avoid oscillations. For the case of the LM5175 it should be dimensioned as such:

$$C_{slope} = g_{m_{slope}} \frac{L1}{R_{sense} A_{cs}} = 100 \text{pF}$$
 (24)

Finally, the bootstrap capacitors and diodes also have to be chosen in order for the integrated MOSFET drivers to function as intended. For this purpose, 100nF ceramic caps were chosen. Also the SS24 Schottky Barrier Rectifier by Multicomp Pro was decided upon for the diodes due to it's 2A forward current and 40V peak reverse voltage [3]. It doesn't matter all that much as long as it's a schottky, but this diode was chosen also because it could withstand the possible peak voltages from the MOSFET bridge, and reusing it throughout the circuit reduces the final BOM.

2.2 Power Losses & Efficiency

2.2.1 MOSFETs

In the buck mode of operation, the conduction and switching losses are given by the following formulas [1]:

$$\begin{cases}
P_{cond(QH1)} = \frac{V_{out}}{V_{in}} I_{out}^2 R_{DSon} \\
P_{SW(QH1)} = \frac{1}{2} V_{in} I_{out} (t_r + t_f) F_{SW} \\
P_{cond(QL1)} = \left(1 - \frac{V_{out}}{V_{in}}\right) I_{out}^2 R_{DSon} \\
P_{cond(QH2)} = I_{out}^2 R_{DSon}
\end{cases}$$
(25)

As for when the converter is operating in boost mode:

$$\begin{cases}
P_{cond(QH1)} = \left(\frac{V_{out}}{V_{in}}I_{out}\right)^{2}R_{DSon} \\
P_{cond(QL2)} = \left(1 - \frac{V_{out}}{V_{in}}\right)\left(\frac{V_{out}}{V_{in}}I_{out}\right)^{2}R_{DSon} \\
P_{SW(QL2)} = \frac{1}{2}V_{out}\left(\frac{V_{out}}{V_{in}}I_{out}\right)(t_{r} + t_{f})F_{SW} \\
P_{cond(QH2)} = \frac{V_{in}}{V_{out}}\left(I_{out}\frac{V_{out}}{V_{in}}\right)^{2}R_{DSon}
\end{cases} (26)$$

If we plug some of the datasheet specifications into the power loss equations, along with the worst case values for V_{in} and I_{out} then the results on table 1 are obtained. It should be taken into account that the actual rise/fall switching times have to be determined empirically in the lab, so the values used consider a much higher current than what our circuit consumes.

Buc	k	Boost		
$P_{cond(QH1)}$	$8.6 \mathrm{mW}$	$P_{cond(QH1)}$	99.1mW	
$P_{SW(QH1)}$	$74.2 \mathrm{mW}$	$P_{cond(QL2)}$	$57.8 \mathrm{mW}$	
$P_{cond(QL1)}$	$8.6\mathrm{mW}$	$P_{SW(QL2)}$	$59.4 \mathrm{mW}$	
$P_{cond(QH2)}$	$17.2 \mathrm{mW}$	$P_{cond(QH2)}$	$41.3 \mathrm{mW}$	

Table 1: Maximum MOSFET Power Losses

From these it is also to obtain an idea of the thermal performance of these MOSFETs (table 2), which even at 2A barely heat up indicating very strong efficiency. This is mostly due to the transistors chosen having both very low gate charges and low R_{DSon} .

Transistor	Temperature Rise $\Delta T(^{\circ}C)$
$QH1_{Buck}$	4.14
$QL1_{Buck}$	0.43
$QH2_{Buck}$	0.86
$QH1_{Boost}$	4.96
$QL2_{Boost}$	5.86
$QH2_{Boost}$	2.07

Table 2: Junction-ambient temperature rise

Figures 2 and 3 show how these losses are related to both the output current and varying input voltage.

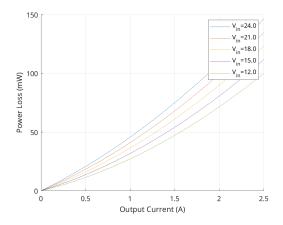


Figure 2: Buck mode MOSFET losses

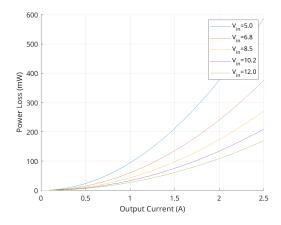


Figure 3: Boost mode MOSFET losses

2.2.2 Inductor

Taking the formula for the RMS current through the inductor (with the previous assumption of 90% efficiency, which certainly is a gross approximation especially when considering lower output currents), an estimate for dissipated power can be obtained if we consider the inductor's wire resistance $R_w = 5.70 \text{m}\Omega$ [4]:

$$P_{inductor} = I_{L_{RMS}}^2 R_w = \left(\frac{V_{out}I_{out}}{0.9V_{in}}\right)^2 R_w \tag{27}$$

This gives a maximum power loss when the current is maximum and the input voltage is minimum, with a value of $P_{Lmax} = 162$ mW. In figure 4 we can observe the power loss in relation to the output current that is drawn from the converter, for varying input voltages.

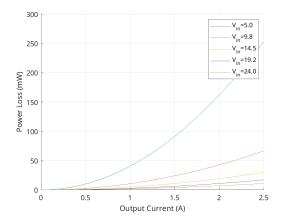


Figure 4: Inductor power losses

2.2.3 Capacitor Losses

During the boost mode of operation the output capacitors are responsible for conducting high ripple current. Using formula 8 for the output current, capacitor buck-mode power losses can be estimated. The total ESR for the output capacitances is $ESR = 2.0 \text{m}\Omega$.

$$P_{C_{out}} = I_{C_{rms}}^2 ESR = I_{out}^2 \left(\frac{V_{out}}{V_{in}} - 1 \right) ESR$$
 (28)

Figure 5 shows these losses as a function of the output current and the input voltage. It is possible to see that the biggest losses are when the input voltage is minimum where $P_{Cout}=11\mathrm{mW}$.

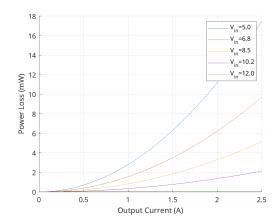


Figure 5: Output capacitor power losses

As for the input capacitances, the formula for the RMS current in equation 9 can be utilized to figure out the power losses. The total ESR for the input capacitors is $2.13 \mathrm{m}\Omega$.

$$P_{C_{in}} = I_{C_{rms}}^2 ESR = I_{out}^2 D(1 - D)ESR$$
 (29)

Using this, figure 6 displays a plot of the power losses in respect to the output current. The maximum power loss is then obtained when the duty cycle is D = 0.5, where $P_{C_{in}} = 2.1$ mW

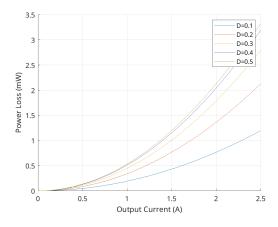


Figure 6: Input capacitor power losses

2.2.4 Sense resistor

A formula for determining the power loss in R_{sense} was already shown in equation 12, but only for the boost mode. In this case the power loss was the following, in the worst case scenario:

$$P_{sense_{Boost}} = 530 \text{mW}$$

For the buck mode, the formula is pretty much the same, only that the duty cycle is different and now we use the buck current limit threshold $V_{CS(BUCK)} = 80 \text{mV}$ for the calculation.

$$P_{sense_{Buck}} = \left(\frac{80mV}{R_{sense}}\right)^2 R_{sense} \left(\frac{V_{out}}{V_{inMAX}}\right) = 178 \text{mW}$$
 (30)

2.2.5 Total Losses

From the previous analysis, the total losses for each mode of operation can be calculated. Firstly the buck mode losses can be seen in figure 7 which consider the worst case of $V_{in} = 24$ V.

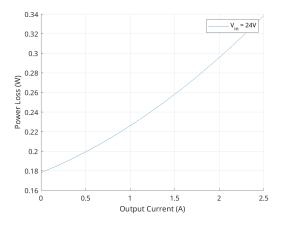


Figure 7: Total buck mode losses

Figure 8 shows the same, but for the boost mode of operation, in the worst case when the input voltage is 5V.

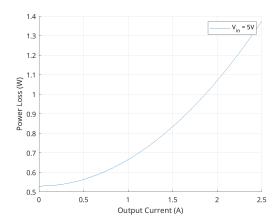


Figure 8: Total boost mode losses

2.2.6 Efficiency

From the total losses, it is then possible to see what the theoretical efficiency of the converter is. Figure 9 shows the worst case scenario efficiency for both the Boost and Buck modes ($V_{in} = 5V$ and $V_{in} = 24V$ respectively), as a function of output current.

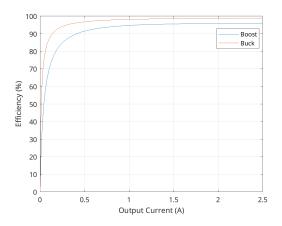


Figure 9: Buck and Boost efficiency

2.3 Board

The board was designed utilizing KiCad 7 for both the schematic capture and PCB layout. Some of the specifications for the board were based on the project limitations and the constraints posed by JLCPCB manufacturing. These were was follows:

• 2 layers, bottom GND plane

• SMD only, except for connectors/testpoints

 \bullet Min. copper clearence: 0.2mm

• Min. track width: 0.2mm

• Min. annular width: 0.13mm

• Min. via diameter: 0.7mm

• Min. copper to hole clearence: 0.25mm

• Min. through-hole diameter: 0.3mm

• Min. hole-to-hole clearence: 0.254mm

Considering these, a relatively simple and compact layout was achieved, whose routing can be seen in figure 10, without any of the filled zones to better visualize the trace routing. For this, the recommended layout for the LM5175 [1] was used as a base, while following the remaining guidelines imposed by the manufacturer.

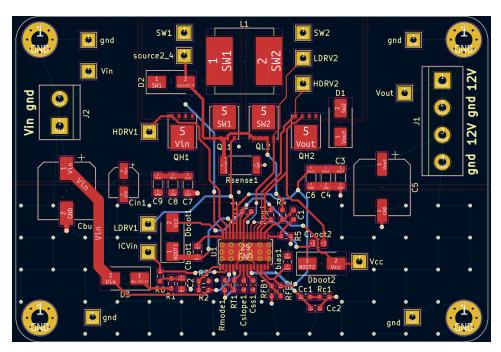


Figure 10: PCB routing

In figures 11 and 12, 3D renders of the populated boards can be seen, while figure 13 shows the final board fully assembled.

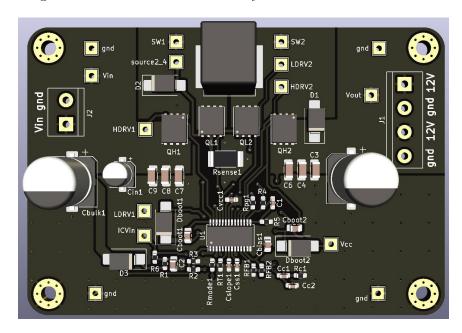


Figure 11: Front of the PCB - 3D render

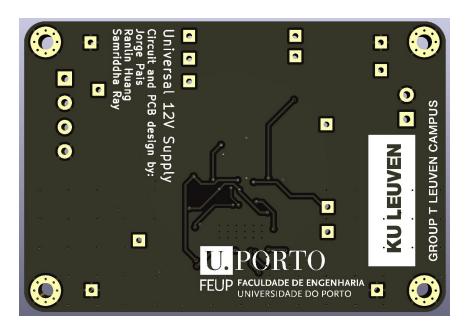


Figure 12: Back of the PCB - 3D render

Building the board was a matter of first laying solder paste across all

SMD connections, carefully placing the components using tweezers and finally baking everything in the oven. The testpoints were then populated with small lugs which were hand soldered.

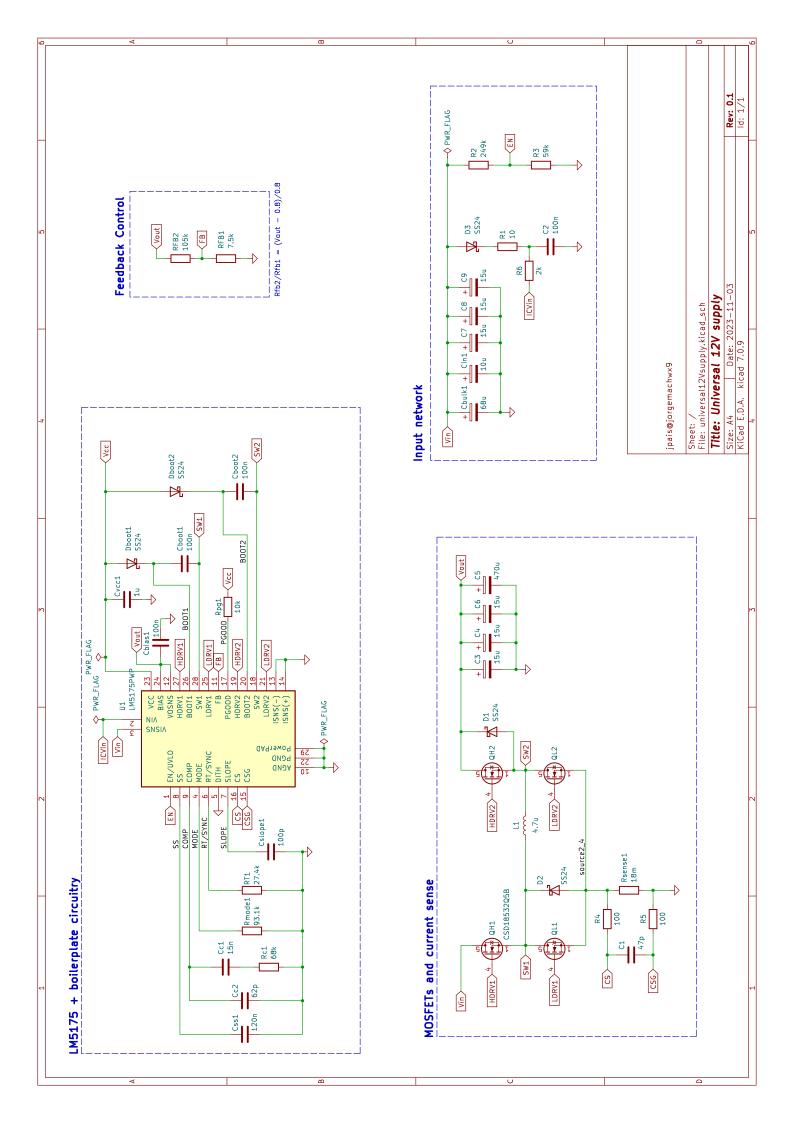


Figure 13: Final assembled board

3 Measurements

References

- [1] 42-v wide vin synchronous 4-switch buck-boost controller, LM5174, Rev. A, Texas Instruments, May 2016.
- [2] 60-v n-channel nexfet^{\mathbb{M}} power mosfets, CSD18532Q5B, Rev. D, Texas Instruments, Feb. 2018.
- [3] Schottky rectifier, SS24+, V1.1, Multicomp Pro, Sep. 2019.
- [4] Shielded power inductors, XAL1010, Doc. 804, Coilcraft, Jun. 2021.



Reference	Value	Footprint Datasheet	Farnell Qty	Farnell (Farnell Order Code
C1	47p	Capacitor{.~	https://be.farnell.com/en-BE/kemet/c0603c470f1gact	1	2820807
C2	100n	Capacitor_{~~	https://be.farnell.com/en-BE/kemet/c0805x104j5rac3	1	2666904
C3, C4, C6, C7, C8, C9	15u	Capacitor_{~~	https://be.farnell.com/en-BE/avx/tpsa156k006r0700/c	9	1658485
C5	470u	Capacitor_{~~	https://be.farnell.com/en-BE/panasonic/25svpk470m/	1	2759084
Cbias1	100n	Capacitor_{~~	https://be.farnell.com/en-BE/kemet/c0805x104j5rac3	1	2666904
Cboot1, Cboot2	100n	Capacitor_{~~	https://be.farnell.com/en-BE/kemet/c0805x104j5rac3	2	2666904
Cbulk1	n89	Capacitor_{~~	https://be.farnell.com/en-BE/panasonic/eehzt1j680p/	1	3584428
Cc1	15n	Capacitor_{~~	https://be.farnell.com/en-BE/multicomp/mc0603b153	1	2320805
Cc2	62p	Capacitor_{~~	https://be.farnell.com/en-BE/kemet/c0603c620j5gacti	1	1865482
Cin1	10u	Capacitor_{~~	https://be.farnell.com/en-BE/kemet/exv106m035a9da	1	2069187
Cslope1	100p	Capacitor_{~~	https://be.farnell.com/en-BE/kemet/c0603x101f5gaca	1	2904893
Cvcc1	1u	Capacitor	https://be.farnell.com/en-BE/kemet/c0805c105j8ractu	1	2773210
Css1	120n	Capacitor_{~~	https://be.farnell.com/en-BE/kemet/c0603c124k8ract	1	2821085
D1-D3	SS24	Diode_SML~	https://be.farnell.com/en-BE/multicomp/ss24/schottk	8	2675138
Dboot1, Dboot2	SS24	Diode_SML~	https://be.farnell.com/en-BE/multicomp/ss24/schottk	2	2675138
L1	4.7u	Inductor_SI~	https://be.farnell.com/en-BE/coilcraft/xal1010-472me	1	2289017
QH1, QH2	CSD18532Q5B	Package_T(http://www.ti.com/	/ https://be.farnell.com/en-BE/texas-instruments/csd18	2	3009663
QL1, QL2	CSD18532Q5B		.ti.com/ https://be.farnell.com/en-BE/texas-instruments/csd18	2	3009663
R1	10R	Resistor_S^~	https://be.farnell.com/en-BE/rohm/ktr03ezpf10r0/res	1	2919225
R2	249k	Resistor_S^~	https://be.farnell.com/en-BE/panasonic/erjpa3f2493v,	1	2561907
R3	59k	Resistor_S^~	https://be.farnell.com/en-BE/panasonic/erjpa3f5902v,	1	2562106
R4, R5	100R	Resistor_S^~	https://be.farnell.com/en-BE/vishay/rca0603100rfkea	2	2616583
R6	2k	Resistor_S^~	https://be.farnell.com/en-BE/panasonic/era3arw202v,	1	2797306
Rc1	68k	Resistor_S^~	https://be.farnell.com/en-BE/te-connectivity/crgcq06C	1	2861483
RFB1	7.5k	Resistor_S^~	https://be.farnell.com/en-BE/multicomp-pro/mcsr06x	1	2074303
RFB2	105k	Resistor_S^~	https://be.farnell.com/en-BE/panasonic/erjpa3f1053v,	1	2561729
Rmode1	93.1k	Resistor_S^~	https://be.farnell.com/en-BE/panasonic/erjpa3f9312v,	1	2562207
Rpg1	10k	Resistor_S^~	https://be.farnell.com/en-BE/vishay/rca060310k0fkea,	1	2616584
Rsense1	18m	Resistor_S^~	https://be.farnell.com/en-BE/multicomp/mchvr12ftft1	1	2826912
RT1	27.4k	Resistor_S^~	https://be.farnell.com/en-BE/panasonic/erjpa3f2742v,	1	2561929
U1	LM5175PWP	ttp://www	.ti.com/ https://be.farnell.com/en-BE/texas-instruments/lm517.	1	3008670