```asm
.nolist
.include "m328pdef.inc"
.list

.cseg
.org 0x0000
reset:    JMP main

.org 0x0040
main:
        LDI R16, 0x96 // se declaran las variables
        LDI R17, 0x00
        LDI R18, 0x00
        LDI R19, 0x00
        LDI R20, 0x0
loop:  //loop para sumar
        CPI R20, 0x0A
        BREQ result //salta  si la bandera z es 1
        ADD R18,R16
        ADC R19,R17
        INC R20
        RJMP loop
result:
        STS 0x0100, R19 //se guarda el resultado en la posicion de memoria indicada
        STS 0x0101, R18
break
```
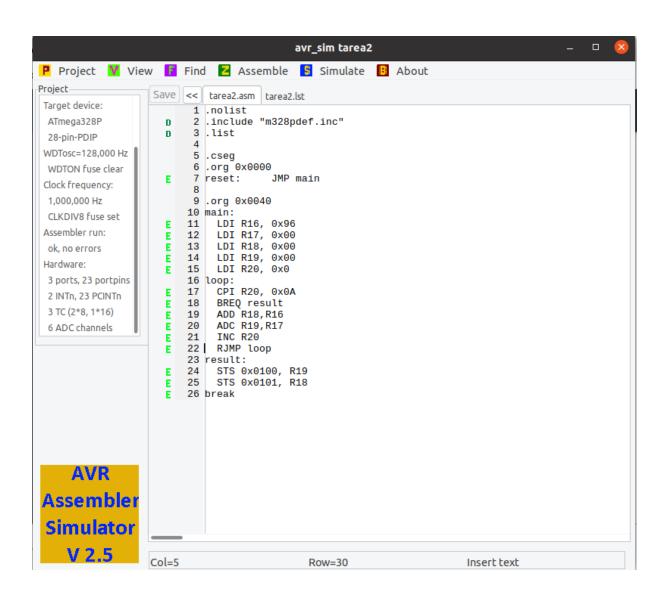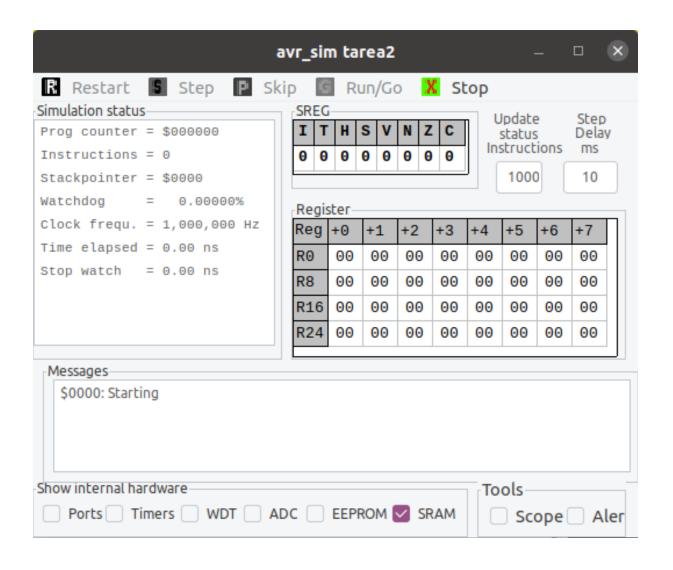
avr_sim tarea2

P Project   **V** View   **F** Find   **Z** Assemble   **S** Simulate   **B** About

Project

Target device:
ATmega328P
28-pin-PDIP
WDTosc=128,000 Hz
WDTON fuse clear
Clock frequency:
1,000,000 Hz
CLKDIV8 fuse set
Assembler run:
ok, no errors
Hardware:
3 ports, 23 portpins
2 INTn, 23 PCINTn
3 TC (2*8, 1*16)
6 ADC channels

AVR Assembler Simulator V 2.5

Save   <<   tarea2.asm   tarea2.lst

```
    1 .nolist
D   2 .include "m328pdef.inc"
D   3 .list
    4
    5 .cseg
    6 .org 0x0000
E   7 reset:      JMP main
    8
    9 .org 0x0040
   10 main:
E  11   LDI R16, 0x96
E  12   LDI R17, 0x00
E  13   LDI R18, 0x00
E  14   LDI R19, 0x00
E  15   LDI R20, 0x0
   16 loop:
E  17   CPI R20, 0x0A
E  18   BREQ result
E  19   ADD R18,R16
E  20   ADC R19,R17
E  21   INC R20
E  22   RJMP loop
   23 result:
E  24   STS 0x0100, R19
E  25   STS 0x0101, R18
E  26 break
```

Col=5   Row=30   Insert text

SRAM

	+00	+01	+02	+03	+04	+05	+06	+07	+08	+09	+0A	+0B	+0C	+0D	+0E	+0F	ASCII text
$0100	05	DC	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0110	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0120	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0130	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0140	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0150	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0160	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0170	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....
$0180	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	....

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