

Assembly para mainframe.

Registradores

Os registradores são pequenas e rápidas áreas de memória utilizada para diversos fins. Alguns desses registradores são utilizados para designar os locais da memória em que o processador vai executar ou pegar informações.

Registradores de segmento

Segmento é uma área da memória usada para armazenar instruções, dados ou usado pela [pilha^{\[4\]}](#). Os seguintes registradores são usados para designar estas áreas:

- CS - Code Segment, segmento de código em execução.
- DS - Data Segment, segmento de dados.
- SS - Stack Segment, segmento de pilha.
- ES - Extra Segment, segmento extra para armazenamento de dados.
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Registradores ponteiros

Esses registradores são utilizados para indicar posições da memória de instruções e dados.

- BP - Base Pointer, usado como ponteiro para indicar a base da *stack frame* atual. É usado por linguagens de programação de alto nível, como [C](#), para controlar a área de memória na pilha usada por cada função.
- IP - Instruction Pointer, aponta para a próxima instrução que será executada.
- SP - Stack Pointer, aponta para o final da pilha.
- SI - Source Index, usado em operações com blocos de dados para apontar para o bloco de memória fonte.
- DI - Destination Index, usado em operações com blocos de dados para apontar para o bloco de memória de destino.

Registradores de dados

Usado de forma geral no programa, para várias operações. Embora possam ser utilizados em outras ocasiões, cada um desses registradores foram feitos para tarefas específicas.

- AX - Registrador Acumulador, usado para operações aritméticas.
- BX - Registrador de Base, usado para indexar endereços na memória.
- CX - Registrador Contador, usado para contagem usando a instrução de loop.
- DX - Registrador de Dados, usado para armazenar dados de forma geral. Seja para cálculos ou operações de [I/O].

Esses registradores na verdade são uma junção de dois registradores de 8bits, somando ao todo 16bits. Eles são [AH, AL, BH, BL, CH, CL, DH, DL](#).

Também existem versões de 32 e 64bits desses registradores. Onde eles são:

- 32 bits - **EAX, EBX, ECX, EDX**
- 64 bits - **RAX, RBX, RCX, RDX**

EAX usado como um acumulador (recebe resultados de operações)

EBX seria usado como dado base para operações

ECX é um contador (vai incrementando algo)

EDX age como dado geral a ser usado na operação.

ESP (Stack Pointer - indicador de onde está o final da pilha na memória)

EBP (Base Pointer - indicador de onde está o escopo agora, os acessos ao dado na pilha são sempre relativos a esse endereço, em geral ele indica o começo dos dados da função em execução, por isso há uma aritmética em cada acesso a um dado)

ESI (Source, alguma vezes chamado de *index*)

EDI (Destination, esses últimos são usados por instruções otimizadas de acesso a dados múltiplos como *arrays*, incluindo *strings*)

Sufixos:

- **b** = byte (8 bit).
- **s** = single (32-bit floating point).
- **w** = word (16 bit).
- **l** = long (32 bit integer or 64-bit floating point).
- **q** = quad (64 bit).
- **t** = ten bytes (80-bit floating point).

Nome Nome estendido Tamanho do operando (em bytes)

byte	1
word	2
dword double word	4
qword quad word	8
tword ten word	10
oword	16
yword	32
zword	64

```
SEG1      EQU      $1000
CONTADOR  DC.L     100
ARR1      DC.W     0,1,1,2,3,5,8,13
MENSAGEM  DC.B     'Alo, pessoal!'
```

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```

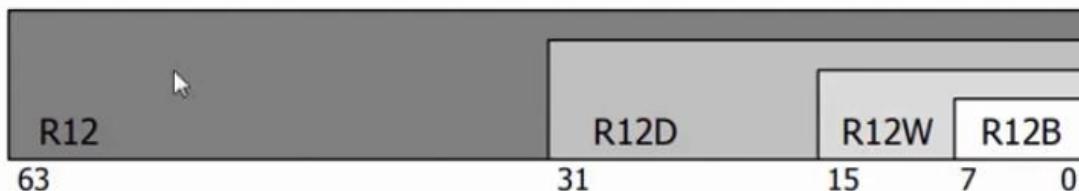
mov byte ptr [rax],0
mov word ptr [rax],0
mov dword ptr [rax],0
mov qword ptr [rax],0
MOV AH,[200]      ; Movimenta o byte contido em 200h para o registro AH
SUB AH,2          ; Subtrai de 2 o valor do registro AH
MOV [201],AH      ; Armazena conteúdo de AH na memória DS:201h
MOV AX,[200]      ; Movimenta o word contido em 200h para o registro AH
INC AX            ; Incrementa de 1 o valor do registro AH
MOV [205],AX      ; Armazena conteúdo de AH na memória DS:205h

```

Exemplo Formato

0b0111	Binário
0o10	Octal
9	Decimal
0x0a	Hexadecimal
11.0	Ponto flutuante

Registradores de uso geral:



Registradores de 8 bits:

AL BL CL DL armazena de 0 a 255.

Registradores de 16 bits:

AX BX CX DX armazena de 0 a 65535.

Registradores de 32 bits:

EAX EBX ECX EDX armazena de 0 a 4294967295.

Registradores de 64 bits:

RAX RBX RCX RDX armazena de 0 a ...

- R0 – Program Counter (PC)
 - Endereço da próxima instrução
- R1 – Stack Pointer (SP)
 - Endereço da Pilha
- R2 – Status Register (SR)
 - Guarda os flags da última operação
 - Carry, oVerflow, Negative, Zero
- R3 – Constant Generator (CG)

Registradores de Uso Geral: R0 até R12

R13 -> SP (Stack Point) - Ponteiro de Pilha

R14 -> LR (Link Register) - Registrador de Ligação

R15 -> PC (Program Counter)

Algumas instruções assembly

• ADD

- Soma o conteúdo de um registrador com um determinado valor ou com o conteúdo de outro registrador.
- O resultado é guardado no primeiro operando.
- Faz um papel semelhante a **ADD** no Simbler.
- Exemplos:

• **ADD BL,15** ; Faz $BL = BL + 15$

Algumas instruções assembly

• SUB – Subtrai o conteúdo de um registrador.

• MUL – Multiplica o conteúdo de um registrador.

• DIV – Divide o conteúdo de um registrador.

• AND – Realiza um AND bit-a-bit com o conteúdo de um registrador.

• OR – Realiza um OR bit-a-bit com o conteúdo de um registrador.

• XOR – Realiza um XOR bit-a-bit com o conteúdo de um registrador.

• Essas operações são realizadas de forma semelhante ao ADD.

- Copia um dado da memória do simulador para um registrador ou vice-versa.
- Faz um papel semelhante a **STORE** e **LOAD**.
- Exemplos:

- **MOV BL,15** ; copia 15 no registrador BL.
- **MOV CL,[12]** ; copia no reg. CL o conteúdo do endereço 12h da memória
- **MOV [12],BL** ; copia no endereço 12h da memória o conteúdo do reg. BL
- **MOV AL,[DL]** ; copia no reg. AL o conteúdo do end. de memória indicado por DL
- **MOV [AL],DL** ; copia no end. de memória indicado por AL o conteúdo do reg. DL

- mov eax,Y - Está movendo para o registrador chamado EAX o valor que está na memória em certo endereço que é conceitualmente indicado por Y
- add eax,4 - Está fazendo uma operação de adição entre o valor que está em EAX e a constante 4, obviamente que o resultado alterará alguns registradores de bits e manterá o resultado em EAX mesmo, portanto é uma operação com efeito colateral ao que está sendo usado no cálculo
- mov ebx,3 - Está armazenando o número 3 no registrador EBX, é como se fizesse um ebx = 3;
- imul ebx - Está realizando uma multiplicação de inteiros, que é mais simples que um de ponto flutuante usando o EBX com multiplicador, o multiplicando é implicitamente o EAX, e o resultado será armazenado em EAX, como de costume
- mov X,eax - Está movendo para o que se chama conceitualmente X (na prática é um endereço de memória) o que está armazenado em EAX nesse momento.

MVC TARGET,SOURCE	; Move SOURCE para o TARGET
MVC TARGET(40),SOURCE	; Move 40 bytes do source para o TARGET
MVC TARGET+10(20),SOURCE+3	; Move 20 primeiros Bytes do SOURCE+3 ; para o TARGET+10
MVC 5(3,14),SOURCE	; Move 3 Bytes do SOURCE para o inicio do registrador 14 mais 5

Address	Value
0x100	\$0xFF
0x104	\$0xAB
0x108	\$0x13
0x10C	\$0x11

Register	Value
%eax	\$0x100
%ebx	\$0x104
%ecx	\$0x001
%edx	\$0x003

A pseudo-instrução de **substituição simbólica**, EQU, associa um valor definido pelo programador a um símbolo. Por exemplo, a linha de instrução

```
SIZE      EQU      100
```

associa o valor decimal 100 ao símbolo SIZE, que pode ser posteriormente referenciado em outras instruções, como em

```
MOVE      #SIZE, D0
```

Type of Constant	Function	Example		
Address	Defines address mainly for the use of fixed-point and other instructions	ADCON	L DC	5 , ADCON A (SOMWHERE)
Binary	Defines bit patterns	FLAG	DC	B'00010000'
Character	Defines character strings or messages	CHAR	DC	C'string of characters'
Decimal	Used by decimal instructions	ZAP	AREA, PCON	
		PCON	DC	P'100'
		AREA	DS	PL3
Fixed-point	Used by the fixed-point and other instructions	FCON	L DC	3 , FCON F'100'
Floating-point	Used by floating-point instructions	ECON	LE DC	2 , ECON E'100.50'
Graphic	Defines character strings or messages that contain pure double-byte data	DBCS	DC	G'<.D.B.C.S. .S.T.R.I.N.G>'
Hexadecimal	Defines large bit patterns	PATTERN	DC	X'FF00FF00'
Zoned	Defines numeric characters			

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
0101	<u>PR</u>	Program Return	E	<u>Control Flow Instructions</u>	390
0102	<u>UPT</u>	Update Tree	E	<u>Data Transfer Instructions</u>	390
0104	<u>PTFF</u>	Perform Timing Facility Function	E	<u>Control Flow Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
0105	<u>CMSG</u>	Clear Message	E	<u>Data Transfer Instructions</u>	390
0106	<u>TMSG</u>	Test Message	E	<u>Data Transfer Instructions</u>	390
0107	<u>SCKPF</u>	Set (TOD) Clock Programmable Field	E	<u>Control Flow Instructions</u>	390
0108	<u>TMPS</u>	Test Message Path State	E	<u>Data Transfer Instructions</u>	390
0109	<u>CMPS</u>	Clear Message Path State	E	<u>Data Transfer Instructions</u>	390
010A	<u>PFPO</u>	Perform Floating Point Operation	E	<u>Data Transfer Instructions</u>	390
010B	<u>TAM</u>	Test Addressing Mode	E	<u>Control Flow Instructions</u>	390
010C	<u>SAM24</u>	Set Addressing Mode (to 24 bits)	E	<u>Control Flow Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
010D	<u>SAM31</u>	Set Addressing Mode (to 31 bits)	E	<u>Control Flow Instructions</u>	390
010E	<u>SAM64</u>	Set Addressing Mode (to 64 bits)	E	<u>Control Flow Instructions</u>	Z
01FF	<u>TRAP2</u>	Trap	E	<u>Control Flow Instructions</u>	390
04	<u>SPM</u>	Set Program Mask	RR	<u>Other Instructions</u>	360
05	<u>BALR</u>	Branch And Link Register	RR	<u>Branch Instructions</u>	360
06	<u>BCTR</u>	Branch on Count Register	RR	<u>Branch Instructions</u>	360
07	<u>BCR</u>	Branch on Condition Register	RR	<u>Branch Instructions</u>	360
070	<u>NOPR</u>	No Operation Register	RR	<u>Branch Instructions</u>	360
07F	<u>BR</u>	Branch Register (Unconditional)	RR	<u>Branch Instructions</u>	360
08	<u>SSK</u>	Set Storage Key	RR	360 Only <u>Privileged</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
				<u>ed Instructions</u>	
09	<u>ISK</u>	Insert Storage Key	RR	360 Only <u>Privileged Instructions</u>	360
0A	<u>SVC</u>	SuperVisor Call	I	<u>Control Flow Instructions</u>	360
0B	<u>BSM</u>	Branch and Set Mode	RR	<u>Branch Instructions</u>	390
0C	<u>BASSM</u>	Branch and Save and Set Mode	RR	<u>Branch Instructions</u>	390
0D	<u>BASR</u>	Branch And Save Register	RR	<u>Branch Instructions</u>	360
0E	<u>MVCL</u>	MoVe Character Long	RR	<u>Data Transfer Instructions</u>	370
0F	<u>CLCL</u>	Compare Logical Character Long	RR	<u>Logic Instructions</u>	370
10	<u>LPR</u>	Load Positive Register	RR	<u>Data Transfer Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
11	<u>LNR</u>	Load Negative Register	RR	<u>Data Transfer Instructions</u>	360
12	<u>LTR</u>	Load and Test Register	RR	<u>Data Transfer Instructions</u>	360
13	<u>LCR</u>	Load and Complement Register	RR	<u>Arithmetic Instructions</u>	360
14	<u>NR</u>	aNd Register	RR	<u>Arithmetic Instructions</u>	360
15	<u>CLR</u>	Compare Logical Register	RR	<u>Logic Instructions</u>	360
16	<u>OR</u>	Or Register	RR	<u>Arithmetic Instructions</u>	360
17	<u>XR</u>	eXclusive-or Register	RR	<u>Arithmetic Instructions</u>	360
18	<u>LR</u>	Load Register	RR	<u>Data Transfer Instructions</u>	360
19	<u>CR</u>	Compare Register	RR	<u>Logic Instructions</u>	360

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
1A	<u>AR</u>	Add Register	RR	<u>Arithmetic Instructions</u>	360
1B	<u>SR</u>	Subtract Register	RR	<u>Arithmetic Instructions</u>	360
1C	<u>MR</u>	Multiply Register	RR	<u>Arithmetic Instructions</u>	360
1D	<u>DR</u>	Divide Register	RR	<u>Arithmetic Instructions</u>	360
1E	<u>ALR</u>	Add Logical Register	RR	<u>Arithmetic Instructions</u>	360
1F	<u>SLR</u>	Subtract Logical Register	RR	<u>Arithmetic Instructions</u>	360
20	<u>LPDR</u>	Load Positive (Long)	RR	<u>Data Transfer Instructions</u>	360
21	<u>LNDR</u>	Load Negative	RR	<u>Data Transfer Instructions</u>	360
22	<u>LTDR</u>	Load and Test	RR	<u>Data Transfer Instructions</u>	360

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
23	<u>LCDR</u>	Load Complement (Long)	RR	<u>Data Transfer Instructions</u>	360
24	<u>HDR</u>	Halve	RR	<u>Arithmetic Instructions</u>	360
25	<u>LDXR</u>	Load Rounded	RR	<u>Data Transfer Instructions</u>	390
25	<u>LRDR</u>	Load Rounded	RR	360 Only <u>Data Transfer Instructions</u>	360
26	<u>MXR</u>	Multiply	RR	<u>Arithmetic Instructions</u>	360
27	<u>MXDR</u>	Multiply	RR	<u>Arithmetic Instructions</u>	360
28	<u>LDR</u>	Load	RR	<u>Data Transfer Instructions</u>	360
29	<u>CDR</u>	Compare Double Reg.	RR	<u>Logic Instructions</u>	360
2A	<u>ADR</u>	Add Double Register	RR	<u>Arithmetic Instructions</u>	360

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
2B	<u>SDR</u>	Subtract Double Reg.	RR	<u>Arithmetic Instructions</u>	360
2C	<u>MDR</u>	Multiply Double Reg.	RR	<u>Arithmetic Instructions</u>	360
2D	<u>DDR</u>	Divide Double Reg.	RR	<u>Arithmetic Instructions</u>	360
2E	<u>AWR</u>	Add Unnormalized	RR	<u>Arithmetic Instructions</u>	360
2F	<u>SWR</u>	Subtract Unnormalized	RR	<u>Arithmetic Instructions</u>	360
30	<u>LPER</u>	Load Positive (Short)	RR	<u>Data Transfer Instructions</u>	360
31	<u>LNER</u>	Load Negative	RR	<u>Data Transfer Instructions</u>	360
32	<u>LTER</u>	Load and Test	RR	<u>Data Transfer Instructions</u>	360
33	<u>LCER</u>	Load Complement (Short)	RR	<u>Data Transfer Instructions</u>	360

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
34	<u>HER</u>	Halve	RR	<u>Arithmetic Instructions</u>	360
35	<u>LEDR</u>	Load Rounded	RR	<u>Data Transfer Instructions</u>	370
35	<u>LRER</u>	Load Rounded	RR	360 Only <u>Data Transfer Instructions</u>	360
36	<u>AXR</u>	Add Normalized	RR	<u>Arithmetic Instructions</u>	360
37	<u>SXR</u>	Subtract Normalized	RR	<u>Arithmetic Instructions</u>	360
38	<u>LER</u>	Load	RR	<u>Data Transfer Instructions</u>	360
39	<u>CER</u>	Compare	RR	<u>Logic Instructions</u>	360
3A	<u>AER</u>	Add Normalized	RR	<u>Arithmetic Instructions</u>	360
3B	<u>SER</u>	Subtract Normalized	RR	<u>Arithmetic Instructions</u>	360

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
3C	<u>MER</u>	Multiply Normalized	RR	<u>Arithmetic Instructions</u>	360
3D	<u>DER</u>	Divide Normalized	RR	<u>Arithmetic Instructions</u>	360
3E	<u>AUR</u>	Add Unnormalized	RR	<u>Arithmetic Instructions</u>	360
3F	<u>SUR</u>	Subtract Unnormalized	RR	<u>Arithmetic Instructions</u>	360
40	<u>STH</u>	STore Halfword	RX	<u>Data Transfer Instructions</u>	360
41	<u>LA</u>	Load Address	RX	<u>Data Transfer Instructions</u>	360
42	<u>STC</u>	STore Character	RX	<u>Data Transfer Instructions</u>	360
43	<u>IC</u>	Insert Character	RX	<u>Data Transfer Instructions</u>	360
44	<u>EX</u>	EXecute	RX	<u>Data Transfer Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
45	<u>BAL</u>	Branch And Link	RX	<u>Branch Instructions</u>	360
46	<u>BCT</u>	Branch on Count	RX	<u>Branch Instructions</u>	360
47	<u>BC</u>	Branch on Condition	RX	<u>Branch Instructions</u>	360
470	<u>NOP</u>	No Operation	RX	<u>Branch Instructions</u>	360
471	<u>BO</u>	Branch on Overflow/Ones	RX	<u>Branch Instructions</u>	360
472	<u>BH</u>	Branch (a High)	RX	<u>Branch Instructions</u>	360
472	<u>BP</u>	Branch on Plus	RX	<u>Branch Instructions</u>	360
474	<u>BL</u>	Branch (a Low)	RX	<u>Branch Instructions</u>	360
474	<u>BM</u>	Branch on Minus/Mixed	RX	<u>Branch Instructions</u>	360
477	<u>BNE</u>	Branch Not Equal	RX	<u>Branch Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
477	<u>BNZ</u>	Branch Not Zero	RX	<u>Branch Instructions</u>	360
478	<u>BE</u>	Branch (a Equal b)	RX	<u>Branch Instructions</u>	360
478	<u>BZ</u>	Branch on Zero	RX	<u>Branch Instructions</u>	360
47B	<u>BNL</u>	Branch (a Not Low)	RX	<u>Branch Instructions</u>	360
47B	<u>BNM</u>	Branch Not Minus	RX	<u>Branch Instructions</u>	360
47D	<u>BNH</u>	Branch Not High	RX	<u>Branch Instructions</u>	360
47D	<u>BNP</u>	Branch Not Plus	RX	<u>Branch Instructions</u>	360
47E	<u>BNO</u>	Branch Not Ones	RX	<u>Branch Instructions</u>	360
47F	<u>B</u>	Branch (unconditional)	RX	<u>Branch Instructions</u>	360
48	<u>LH</u>	Load Halfword	RX	<u>Data Transfer Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
49	<u>CH</u>	Compare Halfword	RX	<u>Logic Instructions</u>	360
4A	<u>AH</u>	Add Halfword	RX	<u>Arithmetic Instructions</u>	360
4B	<u>SH</u>	Subtract Halfword	RX	<u>Arithmetic Instructions</u>	360
4C	<u>MH</u>	Multiply Halfword	RX	<u>Arithmetic Instructions</u>	360
4D	<u>BAS</u>	Branch And Save	RX	<u>Branch Instructions</u>	360
4E	<u>CVD</u>	ConVert to Decimal	RX	<u>Data Transfer Instructions</u>	360
4F	<u>CVB</u>	ConVert to Binary	RX	<u>Data Transfer Instructions</u>	360
50	<u>ST</u>	STore	RX	<u>Data Transfer Instructions</u>	360
51	<u>LAE</u>	Load Address Extended	RX	<u>Data Transfer Instructions</u>	390

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
54	<u>N</u>	aNd	RX	<u>Arithmetic Instructions</u>	360
55	<u>CL</u>	Compare Logical	RX	<u>Logic Instructions</u>	360
56	<u>O</u>	Or	RX	<u>Arithmetic Instructions</u>	360
57	<u>X</u>	eXclusive or	RX	<u>Arithmetic Instructions</u>	360
58	<u>L</u>	Load	RX	<u>Data Transfer Instructions</u>	360
59	<u>C</u>	Compare	RX	<u>Logic Instructions</u>	360
5A	<u>A</u>	Add	RX	<u>Arithmetic Instructions</u>	360
5B	<u>S</u>	Subtract	RX	<u>Arithmetic Instructions</u>	360
5C	<u>M</u>	Multiply	RX	<u>Arithmetic Instructions</u>	360
5D	<u>D</u>	Divide	RX	<u>Arithmetic Instructions</u>	360

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
5E	<u>AL</u>	Add Logical	RX	<u>Arithmetic Instructions</u>	360
5F	<u>SL</u>	Subtract Logical	RX	<u>Arithmetic Instructions</u>	360
60	<u>STD</u>	Store Double	RX	<u>Data Transfer Instructions</u>	360
67	<u>MXD</u>	Multiply Double	RX	<u>Arithmetic Instructions</u>	360
68	<u>LD</u>	Load Double	RX	<u>Data Transfer Instructions</u>	360
69	<u>CD</u>	Compare Double	RX	<u>Logic Instructions</u>	360
6A	<u>AD</u>	Add Double normalized	RX	<u>Arithmetic Instructions</u>	360
6B	<u>SD</u>	Subtract Double normalized	RX	<u>Arithmetic Instructions</u>	360
6C	<u>MD</u>	Multiply Double	RX	<u>Arithmetic Instructions</u>	360

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
6D	<u>DD</u>	Divide Double	RX	<u>Arithmetic Instructions</u>	360
6E	<u>AW</u>	Add unnormalized Word	RX	<u>Arithmetic Instructions</u>	360
6F	<u>SW</u>	Subtract unnormalized Word	RX	<u>Arithmetic Instructions</u>	360
70	<u>STE</u>	Store short	RX	<u>Data Transfer Instructions</u>	360
71	<u>MS</u>	Multiply Single	RX	<u>Data Transfer Instructions</u>	370
78	<u>LE</u>	Load short	RX	<u>Data Transfer Instructions</u>	360
79	<u>CE</u>	Compare short	RX	<u>Logic Instructions</u>	360
7A	<u>AE</u>	Add normalized short	RX	<u>Arithmetic Instructions</u>	360
7B	<u>SE</u>	Subtract normalized short	RX	<u>Arithmetic Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
7C	<u>MDE</u>	Multiply short	RX	<u>Arithmetic Instructions</u>	390
7C	<u>ME</u>	Multiply short	RX	<u>Arithmetic Instructions</u>	360
7D	<u>DE</u>	Divide short	RX	<u>Arithmetic Instructions</u>	360
7E	<u>AU</u>	Add Unnormalized short	RX	<u>Arithmetic Instructions</u>	360
7F	<u>SU</u>	Subtract Unnormalized short	RX	<u>Arithmetic Instructions</u>	360
80	<u>SSM</u>	Set System Mask	SI	<u>Privileged Instructions</u>	360
82	<u>LPSW</u>	Load Program Status Word	S	<u>Privileged Instructions</u>	360
83	<u>DIAGNOSE</u>	Diagnose ^[1]	RX	<u>Privileged Instructions</u>	360
84	<u>WRD</u>	Write Direct	RX	360 Only <u>Privileged Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
85	<u>RDD</u>	Read Direct	RX	360 Only <u>Privileged Instructions</u>	360
84	<u>BRXH</u>	Branch Relative on indeX High	RSI	<u>Branch Instructions</u>	370
84	<u>JXH</u>	Jump on indeX High	RSI	<u>Branch Instructions</u>	370
85	<u>BRXLE</u>	Branch Relative on indeX Low or Equal	RSI	<u>Branch Instructions</u>	370
85	<u>JXLE</u>	Jump on indeX Low or Equal	RSI	<u>Branch Instructions</u>	370
86	<u>BXH</u>	Branch on indeX High	RS	<u>Branch Instructions</u>	360
87	<u>BXLE</u>	Branch on indeX Low or Equal	RS	<u>Branch Instructions</u>	360
88	<u>SRL</u>	Shift Right single Logical	RS	<u>Shift and Rotate Instructions</u>	360
89	<u>SLL</u>	Shift Left Logical	RS	<u>Shift and Rotate Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
8A	<u>SRA</u>	Shift Right Arithmetic	RS	<u>Shift and Rotate Instructions</u>	360
8B	<u>SLA</u>	Shift Left Arithmetic	RS	<u>Shift and Rotate Instructions</u>	360
8C	<u>SRDL</u>	Shift Right Double Logical	RS	<u>Shift and Rotate Instructions</u>	360
8D	<u>SLDL</u>	Shift Left Double Logical	RS	<u>Shift and Rotate Instructions</u>	360
8E	<u>SRDA</u>	Shift Right Double Arithmetic	RS	<u>Shift and Rotate Instructions</u>	360
8F	<u>SLDA</u>	Shift Left Double Arithmetic	RS	<u>Shift and Rotate Instructions</u>	360
90	<u>STM</u>	STore Multiple	RS	<u>Data Transfer Instructions</u>	360
91	<u>TM</u>	Test under Mask	SI	<u>Logic Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
92	<u>MVI</u>	MoVe Immediate	SI	<u>Data Transfer Instructions</u>	360
93	<u>TS</u>	Test and Set	SI	<u>Logic Instructions</u>	360
94	<u>NI</u>	aNd Immediate	SI	<u>Data Transfer Instructions</u>	360
95	<u>CLI</u>	Compare Logical Immediate	SI	<u>Logic Instructions</u>	360
96	<u>OI</u>	Or Immediate	SI	<u>Data Transfer Instructions</u>	360
97	<u>XI</u>	eXclusive-or Immediate	SI	<u>Data Transfer Instructions</u>	360
98	<u>LM</u>	Load Multiple	RS	<u>Data Transfer Instructions</u>	360
99	<u>TRACE</u>	Trace	RS	<u>Privileged Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
9A	<u>LAM</u>	Load Access Multiple	RS	<u>Data Transfer Instructions</u>	370
9B	<u>STAM</u>	Store Access Multiple	RS	<u>Data Transfer Instructions</u>	370
9C	<u>SIO</u>	Start I/O	SI	360 Only <u>Privileged Instructions</u>	360
9C00	<u>SIO</u>	Start I/O	SI	<u>Privileged Instructions</u>	370
9C01	<u>SIOF</u>	Start I/O Fast release	SI	<u>Privileged Instructions</u>	370
9C00	<u>RIO</u>	Resume I/O	SI	<u>Privileged Instructions</u>	370
9D	<u>TIO</u>	Test I/O	SI	360 Only <u>Privileged Instructions</u>	360
9D00	<u>TIO</u>	Test I/O	SI	370 Only <u>Privileged Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
9D01	<u>CLRIO</u>	CLeaR I/O	SI	370 Only <u>Privileged Instructions</u>	370
9E	<u>HIO</u>	Halt I/O	SI	360 Only <u>Privileged Instructions</u>	360
9E00	<u>HIO</u>	Halt I/O	SI	370 Only <u>Privileged Instructions</u>	370
9E01	<u>HDV</u>	Halt Device	SI	370 Only <u>Privileged Instructions</u>	370
9F	<u>TCH</u>	Test CHannel	SI	360, 370 Only <u>Privileged Instructions</u>	360
9F00	<u>TCH</u>	Test CHannel	SI	390 & Z <u>Privileged Instructions</u>	390
9F01	<u>CLRCH</u>	Clear CHannel	SI	<u>Privileged Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B258	<u>BSG</u>	Branch in Subspace Group	RRE	<u>Branch Instructions</u>	390
A4--		Vector Instructions	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A400	<u>VAE</u>	Add Exponential (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A401	<u>VSE</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A402	<u>VME</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A403	<u>VDE</u>	Divide (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A404	<u>VMAE</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A405	<u>VMSE</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A406	<u>VMCE</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A407	<u>VACE</u>	ACcumulate Exponential (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A408	<u>VCE</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A409	<u>VL</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A40A	<u>VLM</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A40B	<u>VLY</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A40D	<u>VST</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A40E	<u>VSTM</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A40F	<u>VSTK</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A410	<u>VAD</u>	Add Double (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A411	<u>VSD</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A412	<u>VMD</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A413	<u>VDD</u>	Divide (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A414	<u>VMAD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A414	<u>VMSD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A416	<u>VMCD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A417	<u>VACD</u>	ACcumulate Double (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A418	<u>VCD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A419	<u>VLD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A41A	<u>VLMD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A41B	<u>VLYD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A41D	<u>VSTD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A41E	<u>VSTMD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A41F	<u>VSTKD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A420	<u>VA</u>	Add (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A421	<u>VS</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A422	<u>VM</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A424	<u>VN</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A425	<u>VO</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A426	<u>VX</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A428	<u>VC</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A429	<u>VLH</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A42A	<u>VLINT</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A42D	<u>VSTH</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A443	<u>VSQE</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A444	<u>VTAE</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A445	<u>VTSE</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A453	<u>VSQD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A454	<u>VTAD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A455	<u>VTSD</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A480	<u>VAES</u>	Add Exponential to Storage (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A481	<u>VSES</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A482	<u>VMES</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A483	<u>VDES</u>	Divide (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A484	<u>VMAES</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A485	<u>VMSES</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A488	<u>VCES</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A490	<u>VADS</u>	Add Double to Storage (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A491	<u>VSDS</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A492	<u>VMDS</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A493	<u>VDDS</u>	Divide (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A494	<u>VMADS</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A495	<u>VMSDS</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A498	<u>VCDS</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A4A0	<u>VAS</u>	Add (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A4A1	<u>VSS</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
				tic Instructions	
A4A2	VMS	Multiply (Vector)	RI-a	370 and 390 Only Arithmetic Instructions	370
A4A4	VNS	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A4A5	VOS	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A4A6	VXS	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A4A8	VCS	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A5--		Vector Instructions	RI-a	370 and 390 Only Other Instructions	370
A500	VAER	Add Exponential Register (Vector)	RI-a	370 and 390 Only Arithmetic Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A501	<u>VSER</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A502	<u>VMER</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A503	<u>VDER</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A506	<u>VMCER</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A507	<u>VACER</u>	ACcumulate Exponential Reg. (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A508	<u>VCER</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A509	<u>VLR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A50A	<u>VLMR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A50B	<u>VLZR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A510	<u>VADR</u>	Add Double to Register (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A511	<u>VSDR</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A512	<u>VMDR</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A513	<u>VDDR</u>	Divide (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A516	<u>VMCER</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A517	<u>VACDR</u>	Accumulate Double Register (Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A518	<u>VCDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A519	<u>VLDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A51A	<u>VLMDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A51B	<u>VLZDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A520	<u>VAR</u>	Add to Register (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A521	<u>VSR</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A522	<u>VMR</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
				tic Instructions	
A524	VNR	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A525	VOR	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A526	VXR	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A528	VCR	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A540	VLPER	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A541	VLNER	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A542	VLKER	(Vector)	RI-a	370 and 390 Only Other Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A543	<u>VSQER</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A550	<u>VLPDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A551	<u>VLNDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A552	<u>VLCDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A553	<u>VSQDR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A560	<u>VLPR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A561	<u>VLNR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A562	<u>VLCR</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A580	<u>VAEQ</u>	Add Exponential (Vector)	RI-a	370 and 390 Only Arithmetic Instructions	370
A581	<u>VSEQ</u>	Subtract (Vector)	RI-a	370 and 390 Only Arithmetic Instructions	370
A582	<u>VMEQ</u>	Multiply (Vector)	RI-a	370 and 390 Only Arithmetic Instructions	370
A583	<u>VDEQ</u>	Divide (Vector)	RI-a	370 and 390 Only Arithmetic Instructions	370
A584	<u>VMAEQ</u>	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A585	<u>VMSEQ</u>	(Vector)	RI-a	370 and 390 Only Other Instructions	370
A588	<u>VCEQ</u>	(Vector)	RI-a	370 and 390 Only Other Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A589	<u>VLEQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A58A	<u>VLMEQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A590	<u>VADQ</u>	Add Double to Qualified Reg. (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A591	<u>VSDQ</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A592	<u>VMDQ</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A593	<u>VDDQ</u>	Divide (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A594	<u>VMADQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A595	<u>VMSDQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A598	<u>VCDQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A599	<u>VLDQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A5A0	<u>VLMDQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A5A0	<u>VAQ</u>	Add to Qualified reg. (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A5A1	<u>VSQ</u>	Subtract (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370
A5A2	<u>VMQ</u>	Multiply (Vector)	RI-a	370 and 390 Only <u>Arithmetic Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A5A4	<u>VNQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A5A5	<u>VOQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A5A6	<u>VXQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A5A8	<u>VCQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A5A9	<u>VLQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A5AA	<u>VLMQ</u>	(Vector)	RI-a	370 and 390 Only <u>Other Instructions</u>	370
A50	<u>IIHH</u>	Insert Immediate High High	RI-a	<u>Data Transfer Instructions</u>	Z
A51	<u>IIHL</u>	Insert Immediate High Low	RI-a	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A52	<u>IILH</u>	Insert Immediate Low High	RI-a	Data Transfer Instructions	Z
A53	<u>IILL</u>	Insert Immediate Low Low	RI-a	Data Transfer Instructions	Z
A54	<u>NIHH</u>	And Immediate High High	RI-a	Arithmetic Instructions	Z
A55	<u>NIHL</u>	And Immediate High Low	RI-a	Arithmetic Instructions	Z
A56	<u>NILH</u>	And Immediate Low High	RI-a	Arithmetic Instructions	Z
A57	<u>NILL</u>	And Immediate Low Low	RI-a	Arithmetic Instructions	Z
A58	<u>OIHH</u>	Or Immediate High High	RI-a	Arithmetic Instructions	Z
A59	<u>OIHL</u>	Or Immediate High Low	RI-a	Arithmetic Instructions	Z
A5A	<u>OILH</u>	Or Immediate Low High	RI-a	Arithmetic Instructions	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A5B	<u>OILL</u>	Or Immediate Low Low	RI-a	<u>Arithmetic Instructions</u>	Z
A5C	<u>LLIHH</u>	Load Logical Immediate High High	RI-a	<u>Data Transfer Instructions</u>	Z
A5D	<u>LLIHL</u>	Load Logical Immediate High Low	RI-a	<u>Data Transfer Instructions</u>	Z
A5E	<u>LLILH</u>	Load Logical Immediate Low High	RI-a	<u>Data Transfer Instructions</u>	Z
A5F	<u>LLILL</u>	Load Logical Immediate Low Low	RI-a	<u>Data Transfer Instructions</u>	Z
A6--		Vector Instructions	RRE	370 and 390 Only <u>Other Instructions</u>	370
A600	<u>VMXSE</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A601	<u>VMNSE</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A602	<u>VMXAE</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A608	<u>VLELE</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A609	<u>VXELE</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A610	<u>VMXDS</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A611	<u>VMNSD</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A612	<u>VMXAD</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A618	<u>VLELD</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A619	<u>VXELD</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A61A	<u>VSPSD</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A61B	<u>VZPSD</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A640	<u>VTVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A641	<u>VCVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A642	<u>VCZVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A643	<u>VCOVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A644	<u>VXVC</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A645	<u>VLVCU</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A646	<u>VXVMM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A648	<u>VRRS</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A649	<u>VRSVC</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A64A	<u>VRSV</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A680	<u>VLVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A681	<u>VLCVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A682	<u>VSTVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A684	<u>VNVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A685	<u>VOVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A686	<u>VXVM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6C0	<u>VSRSV</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6C1	<u>VMRSV</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6C2	<u>VSRRS</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6C3	<u>VMRRS</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6V4	<u>VLVCA</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6C5	<u>VRCL</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A6C6	<u>VSVMM</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6C7	<u>VLVXA</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6C8	<u>VSTVP</u>	(Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6CA	<u>VACSV</u>	Activity Count SaVe (Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A6CB	<u>VACRS</u>	Activity Count ReStore (Vector)	RRE	370 and 390 Only <u>Other Instructions</u>	370
A70	<u>TMH</u>	Test under Mask High	RI-a	<u>Logic Instructions</u>	390
A70	<u>TMLH</u>	Test under Mask Low High	RI-a	<u>Logic Instructions</u>	390
A71	<u>TML</u>	Test under Mask Low	RI-a	<u>Logic Instructions</u>	390
A71	<u>TMLL</u>	Test under Mask Low Low	RI-a	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A72	<u>TMHH</u>	Test under Mask High High	RI-a	<u>Logic Instructions</u>	390
A73	<u>TMHL</u>	Test under Mask High Low	RI-a	<u>Logic Instructions</u>	390
A74	<u>BRC</u>	Branch Relative on Condition	RI-c	<u>Branch Instructions</u>	390
A74	<u>JC</u>	Jump on Condition	RI-c	<u>Branch Instructions</u>	390
A74-0	<u>BRNOP</u>	Branch Relative No Operation	RI-c	<u>Branch Instructions</u>	390
A74-0	<u>JNOP</u>	Jump No Operation	RI-c	<u>Branch Instructions</u>	390
A74-1	<u>BRO</u>	Branch Relative on Overflow	RI-c	<u>Branch Instructions</u>	390
A74-1	<u>JO</u>	Jump on Overflow	RI-c	<u>Branch Instructions</u>	390
A74-2	<u>BRH</u>	Branch Relative on High	RI-c	<u>Branch Instructions</u>	390
A74-2	<u>JH</u>	Jump on High	RI-c	<u>Branch Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A74-2	<u>BRP</u>	Branch Relative on Plus	RI-c	<u>Branch Instructions</u>	390
A74-2	<u>JP</u>	Jump on Plus	RI-c	<u>Branch Instructions</u>	390
A74-4	<u>BRL</u>	Branch Relative on Low	RI-c	<u>Branch Instructions</u>	390
A74-4	<u>JL</u>	Jump on Low	RI-c	<u>Branch Instructions</u>	390
A74-4	<u>BRM</u>	Branch Relative on Minus	RI-c	<u>Branch Instructions</u>	390
A74-4	<u>JM</u>	Jump on Minus	RI-c	<u>Branch Instructions</u>	390
A74-7	<u>BRNE</u>	Branch Relative on Not Equal	RI-c	<u>Branch Instructions</u>	390
A74-7	<u>JNE</u>	Jump on Not Equal	RI-c	<u>Branch Instructions</u>	390
A74-7	<u>BRNZ</u>	Branch Relative on Not Zero	RI-c	<u>Branch Instructions</u>	390
A74-7	<u>JNZ</u>	Jump on Not Zero	RI-c	<u>Branch Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A74-8	<u>BRE</u>	Branch Relative on Equal	RI-c	Branch Instructions	390
A74-8	<u>JE</u>	Jump on Equal	RI-c	Branch Instructions	390
A74-B	<u>BRNL</u>	Branch Relative on Not Low	RI-c	Branch Instructions	390
A74-B	<u>JNL</u>	Jump on Not Low	RI-c	Branch Instructions	390
A74-B	<u>BRNM</u>	Branch Relative on Not Minus	RI-c	Branch Instructions	390
A74-B	<u>JNM</u>	Jump on Not Minus	RI-c	Branch Instructions	390
A74-D	<u>BRNH</u>	Branch Relative on Not High	RI-c	Branch Instructions	390
A74-D	<u>JNH</u>	Jump on Not High	RI-c	Branch Instructions	390
A74-D	<u>BRNP</u>	Branch Relative on Not Plus	RI-c	Branch Instructions	390
A74-D	<u>JNP</u>	Jump on Not Plus	RI-c	Branch Instructions	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A74-E	<u>BRNO</u>	Branch Relative on No Overflow	RI-c	<u>Branch Instructions</u>	390
A74-E	<u>JNO</u>	Jump on No Overflow	RI-c	<u>Branch Instructions</u>	390
A74-F	<u>BRU</u>	Branch Relative Unconditional	RI-c	<u>Branch Instructions</u>	390
A74-F	<u>JU</u>	Jump Unconditional	RI-c	<u>Branch Instructions</u>	390
A75	<u>BRAS</u>	Branch Relative and Save	RI-b	<u>Branch Instructions</u>	390
A76	<u>BRCT</u>	Branch Relative on Count	RI-b	<u>Branch Instructions</u>	390
A76	<u>JCT</u>	Jump on Count	RI-b	<u>Branch Instructions</u>	390
A77	<u>BRCTG</u>	Branch Relative on Count 64	RI-b	<u>Branch Instructions</u>	Z
A77	<u>JCTG</u>	Jump on Count 64	RI-b	<u>Branch Instructions</u>	Z
A78	<u>LHI</u>	Load Halfword Immediate	RI-a	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
A79	<u>LGHI</u>	Load Halfword Immediate 64	RI-a	<u>Data Transfer Instructions</u>	Z
A7A	<u>AHI</u>	Add Halfword Immediate	RI-a	<u>Arithmetic Instructions</u>	390
A7B	<u>AGHI</u>	Add Halfword Immediate 64	RI-a	<u>Arithmetic Instructions</u>	Z
A7C	<u>MHI</u>	Multiply Halfword Immediate	RI-a	<u>Arithmetic Instructions</u>	390
A7D	<u>MGHI</u>	Multiply Halfword Immediate 64	RI-a	<u>Arithmetic Instructions</u>	Z
A7E	<u>CHI</u>	Compare Halfword Immediate	RI-a	<u>Logic Instructions</u>	390
A7F	<u>CGHI</u>	Compare Halfword Immediate 64	RI-a	<u>Logic Instructions</u>	Z
A8	<u>MVCLE</u>	Move Long Extended	RS	<u>Data Transfer Instructions</u>	390
A9	<u>CLCLE</u>	Compare Logical Long Extended	RS	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
AC	<u>STNSM</u>	Store Then aNd System Mask	SI	<u>Privileged Instructions</u>	370
AD	<u>STOSM</u>	Store Then Or System Mask	SI	<u>Privileged Instructions</u>	370
AE	<u>SIGP</u>	Signal Processor	RS	<u>Privileged Instructions</u>	370
AF	<u>MC</u>	Monitor Call	SI	<u>Other Instructions</u>	370
B1	<u>LRA</u>	Load Real Address	RX	<u>Privileged Instructions</u>	370
B200	<u>CONCS</u>	Connect Channel Set	S	<u>Privileged Instructions</u>	370
B201	<u>DISCS</u>	DISconnect Channel Set	S	<u>Privileged Instructions</u>	370
B202	<u>STIDP</u>	Store CPU ID	S	<u>Privileged Instructions</u>	370
B204	<u>SCK</u>	Set Clock	S	<u>Privileged Instructions</u>	370
B205	<u>STCK</u>	Store Clock	S	<u>Data Transfer Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B206	<u>SCKC</u>	Set Clock Comparator	S	<u>Privileged Instructions</u>	370
B207	<u>STCKC</u>	Store Clock Comparator	S	<u>Privileged Instructions</u>	370
B208	<u>SPT</u>	Set CPU Timer	S	<u>Privileged Instructions</u>	370
B209	<u>STPT</u>	Store CPU Timer	S	<u>Privileged Instructions</u>	370
B20A	<u>SPKA</u>	Set PSW Key From Address	S	<u>Privileged Instructions</u>	370
B20B	<u>IPK</u>	Insert PSW Key	S	<u>Privileged Instructions</u>	370
B20D	<u>PTLB</u>	Purge TLB	S	<u>Privileged Instructions</u>	390
B210	<u>SPX</u>	Set Prefix	S	<u>Privileged Instructions</u>	370
B211	<u>STPX</u>	Store Prefix	S	<u>Privileged Instructions</u>	370
B212	<u>STAP</u>	Store CPU Address	S	<u>Privileged Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B213	<u>RRB</u>	Reset Reference Bit	S	<u>Privileged Instructions</u>	370
B214	<u>SIE</u>		RI-a	390 Only <u>Other Instructions</u>	390
B218	<u>PC</u>	Program Call	S	<u>Control Flow Instructions</u>	390
B218	<u>PCF</u>	Program Call Fast	S	<u>Control Flow Instructions</u>	390
B219	<u>SAC</u>	Set Address Space Control	S	<u>Control Flow Instructions</u>	390
B21A	<u>CFC</u>	Compare and Form Codeword	S	<u>Logic Instructions</u>	390
B21B	<u>DEP</u>			<u>Other Instructions</u>	390
B21C	<u>DCTP</u>			<u>Other Instructions</u>	390
B21D	<u>MAD</u>	Multiply and Add Long		<u>Arithmetic Instructions</u>	390
B21E	<u>MUN</u>			<u>Other Instructions</u>	390

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B21F	<u>STCAP</u>			<u>Other Instructions</u>	390
B220	<u>SERVC</u>			<u>Other Instructions</u>	390
B221	<u>IPTE</u>	Invalidate Page Table Entry	RRF	<u>Privileged Instructions</u>	390
B222	<u>IPM</u>	Insert Program Mask	RRE	<u>Other Instructions</u>	390
B223	<u>IVSK</u>	Insert Virtual Storage Key	RRE	<u>Privileged Instructions</u>	390
B224	<u>IAC</u>	Insert Address Space Control	RRE	<u>Privileged Instructions</u>	390
B225	<u>SSAR</u>	Set Secondary ASN	RRE	<u>Privileged Instructions</u>	390
B226	<u>EPAR</u>	Extract Primary ASN	RRE	<u>Privileged Instructions</u>	390
B227	<u>ESAR</u>	Extract Secondary ASN	RRE	<u>Privileged Instructions</u>	390
B228	<u>PT</u>	Program Transfer	RRE	<u>Privileged Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B229	<u>ISKE</u>	Insert Storage Key Extended	RRE	<u>Privileged Instructions</u>	390
B22A	<u>RRBE</u>	Reset Storage Key Extended	RRE	<u>Privileged Instructions</u>	390
B22B	<u>SSKE</u>	Set Storage Key Extended	RRE	<u>Privileged Instructions</u>	390
B22C	<u>TB</u>	Test Block	RRE	<u>Privileged Instructions</u>	390
B22D	<u>DXR</u>	Divide Extended	RRE	<u>Data Transfer Instructions</u>	390
B22E	<u>PGIN</u>	Page In	RRE	<u>Privileged Instructions</u>	390
B22F	<u>PGOUT</u>	Page Out	RRE	<u>Privileged Instructions</u>	390
B230	<u>CSCH</u>	Clear SubChannel	S	<u>Privileged Instructions</u>	390
B231	<u>HSCH</u>	Halt SubChannel	S	<u>Privileged Instructions</u>	390
B232	<u>MSCH</u>	Modify SubChannel	S	<u>Privileged Instructions</u>	390

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B233	<u>SSCH</u>	Start SubChannel	S	<u>Privileged Instructions</u>	390
B234	<u>STSCH</u>	Store SubChannel	S	<u>Privileged Instructions</u>	390
B235	<u>TSCH</u>	Test SubChannel	S	<u>Privileged Instructions</u>	390
B236	<u>TPI</u>	Test Pending Interruption	S	<u>Privileged Instructions</u>	390
B237	<u>SAL</u>	Set Address Limit	S	<u>Privileged Instructions</u>	390
B238	<u>RSCH</u>	Resume SubChannel	S	<u>Privileged Instructions</u>	390
B239	<u>STCRW</u>	Store Channel Report Word	S	<u>Privileged Instructions</u>	390
B23A	<u>STCPS</u>	Store Channel Path Status	S	<u>Privileged Instructions</u>	390
B23B	<u>RCHP</u>	Reset Channel Path	S	<u>Privileged Instructions</u>	390
B23C	<u>SCHM</u>	Set Channel Monitor	S	<u>Privileged Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B23D	<u>STZP</u>			<u>Other Instructions</u>	390
B23E	<u>SZP</u>			<u>Other Instructions</u>	390
B23F	<u>TPZI</u>			<u>Other Instructions</u>	390
B240	<u>BAKR</u>	Branch and Stack	RRE	<u>Data Transfer Instructions</u>	390
B241	<u>CKSM</u>	Checksum	RRE	<u>Data Transfer Instructions</u>	390
B242		Add FRR	RRE	<u>Other Instructions</u>	390
B243	<u>MADS</u>			<u>Other Instructions</u>	390
B244	<u>SQDR</u>	Square Root Long	RRE	<u>Arithmetic Instructions</u>	390
B245	<u>SQER</u>	Square Root Short	RRE	<u>Arithmetic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B246	<u>STURA</u>	STore Using Real Address	RRE	<u>Privileged Instructions</u>	390
B247	<u>MSTA</u>	Modify Stacked state	RRE	<u>Control Flow Instructions</u>	390
B248	<u>PALB</u>	Purge ALB	RRE	<u>Privileged Instructions</u>	390
B249	<u>EREG</u>	Extract Stacked Registers	RRE	<u>Data Transfer Instructions</u>	390
B24A	<u>ESTA</u>	Extract Stacked State	RRE	<u>Control Flow Instructions</u>	390
B24B	<u>LURA</u>	Load Using Real Address	RRE	<u>Privileged Instructions</u>	390
B24C	<u>TAR</u>	Test Access	RRE	<u>Control Flow Instructions</u>	390
B24D	<u>CPYA</u>	Copy Access	RRE	<u>Other Instructions</u>	390
B24E	<u>SAR</u>	Set Access	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B24F	<u>EAR</u>	Extract Access	RRE	<u>Data Transfer Instructions</u>	390
B250	<u>CSP</u>	Compare and Swap and Purge	RRE	<u>Control Flow Instructions</u>	390
B252	<u>MSR</u>	Multiply Single	RRE	<u>Data Transfer Instructions</u>	390
B254	<u>MVPG</u>	Move Page	RRE	<u>Privileged Instructions</u>	390
B255	<u>MVST</u>	Move String	RRE	<u>Data Transfer Instructions</u>	390
B257	<u>CUSE</u>	Compare Until Substring Equal	RRE	<u>Logic Instructions</u>	390
B258	<u>BSG</u>	Branch in Subspace Group	RRE	<u>Branch Instructions</u>	390
B259	<u>IESBE</u>		RRE	<u>Other Instructions</u>	390
B25A	<u>BSA</u>	Branch and Set Authority	RRE	<u>Branch Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B25B		Asynchronous Page Facility	RRE	Other Instructions	390
B25C		Asynchronous Page Facility	RRE	Other Instructions	390
B25D	CLST	Compare Logical String	RRE	Logic Instructions	390
B25E	SRST	Search String	RRE	Control Flow Instructions	390
B260		Coupling Facility	RRE	Other Instructions	390
B261		Coupling Facility	RRE	Other Instructions	390
B263	CMPSC	Compression Call	RRE	Other Instructions	390
B264		Coupling Facility	RRE	Other Instructions	390
B266		Coupling Facility	RRE	Other Instructions	390
B267		Coupling Facility	RRE	Other Instructions	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B269		Cryptographic Facility	RRE	Other Instructions	390
B26A		Cryptographic Facility	RRE	Other Instructions	390
B26B		Cryptographic Facility	RRE	Other Instructions	390
B26C		Cryptographic Facility	RRE	Other Instructions	390
B26D		Cryptographic Facility	RRE	Other Instructions	390
B26E		Cryptographic Facility	RRE	Other Instructions	390
B26F		Cryptographic Facility	RRE	Other Instructions	390
B272		Coupling Facility	RRE	Other Instructions	390
B276	XSCH	Cancel SubChannel	S	Other Instructions	390
B277	RP	Resume Program	S	Privileged Instructions	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B278	<u>STCKE</u>	Store Clock Extended	S	<u>Data Transfer Instructions</u>	390
B279	<u>SACE</u>	Set Address Space Control Fast	S	<u>Control Flow Instructions</u>	390
B27A		Coupling Facility	RRE	<u>Other Instructions</u>	390
B27B		Coupling Facility	RRE	<u>Other Instructions</u>	390
B27C	<u>STCKF</u>	Store Clock Fast	S	<u>Other Instructions</u>	390
B27D	<u>STSI</u>	Store System Information	S	<u>Privileged Instructions</u>	390
B27E		Coupling Facility	RRE	<u>Other Instructions</u>	390
B27F		Coupling Facility	RRE	<u>Other Instructions</u>	390
B299	<u>SRNM</u>	Set Rounding Mode	S	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B29C	<u>STFPC</u>	Store FPC	S	<u>Data Transfer Instructions</u>	390
B29D	<u>LFPC</u>	Load FPC	S	<u>Data Transfer Instructions</u>	390
B2A5	<u>TRE</u>	Translate Extended	RRE	<u>Data Transfer Instructions</u>	390
B2A6	<u>CU21</u>	Convert UTF-16 to UTF-8	RRF-c	<u>Data Transfer Instructions</u>	390
B2A6	<u>CUUTF</u>	Convert Unicode to UTF-8	RRF-c	<u>Data Transfer Instructions</u>	390
B2A7	<u>CU12</u>	Convert UTF-8 to UTF-16	RRF-c	<u>Data Transfer Instructions</u>	390
B2A7	<u>CUTFU</u>	Convert UTF-8 to Unicode	RRF-c	<u>Data Transfer Instructions</u>	390
B2AA		Dequeue CAM	RRE	<u>Other Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B2AB		Process CAM Queue	RRE	Other Instructions	390
B2AC		Enqueue CAM	RRE	Other Instructions	390
B2B1	<u>STFL</u>	Store Facility List	S	<u>Privileged Instructions</u>	390
B2B2	<u>LPSWE</u>	Load PSW Extended	S	<u>Privileged Instructions</u>	390
B2B8	<u>SRNMB</u>	Set Rounding Mode	S	<u>Data Transfer Instructions</u>	390
B2B9	<u>SRNMT</u>	Set Decimal Rounding Mode	S	<u>Other Instructions</u>	390
B2BD	<u>LFAS</u>	Load FPC and Signal	S	<u>Other Instructions</u>	390
B2F6		Coupling Facility	RRE	<u>Other Instructions</u>	390
B2F8	<u>TEND</u>	Transaction END	S	<u>Control Flow Instructions</u>	Z
B2FC	<u>TABORT</u>	Transaction ABORT	S	<u>Control Flow Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B2FF	<u>TRAP4</u>	Trap	S	<u>Control Flow Instructions</u>	390
B300	<u>LPEBR</u>	Load Positive Short	RRE	<u>Data Transfer Instructions</u>	390
B301	<u>LNEBR</u>	Load Negative Short	RRE	<u>Data Transfer Instructions</u>	390
B302	<u>LTEBR</u>	Load and Test Short	RRE	<u>Data Transfer Instructions</u>	390
B303	<u>LCEBR</u>	Load Complement Short	RRE	<u>Data Transfer Instructions</u>	390
B304	<u>LDEBR</u>	Load Lengthened Short/Long	RRE	<u>Data Transfer Instructions</u>	390
B305	<u>LXDBR</u>	Load Lengthened Long/Extended	RRE	<u>Data Transfer Instructions</u>	390
B306	<u>LDEBR</u>	Load Lengthened Short/Extended	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B307	<u>MXDBR</u>	Multiply Long/Extended	RRE	<u>Arithmetic Instructions</u>	390
B308	<u>KEBR</u>	Compare and Signal Short	RRE	<u>Logic Instructions</u>	390
B309	<u>CEBR</u>	Compare Short	RRE	<u>Logic Instructions</u>	390
B30A	<u>AEBR</u>	Add Short	RRE	<u>Arithmetic Instructions</u>	390
B30B	<u>SEBR</u>	Subtract Short	RRE	<u>Arithmetic Instructions</u>	390
B30C	<u>MDEBR</u>	Multiply Short/Long	RRE	<u>Arithmetic Instructions</u>	390
B30D	<u>DEBR</u>	Divide Short	RRE	<u>Arithmetic Instructions</u>	390
B30E	<u>MAEBR</u>	Multiply and Add Short	RRE	<u>Arithmetic Instructions</u>	390
B30F	<u>MSEBR</u>	Multiply and Subtract Short	RRE	<u>Arithmetic Instructions</u>	390
B310	<u>LPDBR</u>	Load Positive Long	RRE	<u>Data Transfer Instructions</u>	390

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Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B311	<u>LNDBR</u>	Load Negative Long	RRE	<u>Data Transfer Instructions</u>	390
B312	<u>LTDBR</u>	Load and test Long	RRE	<u>Data Transfer Instructions</u>	390
B313	<u>LCDBR</u>	Load Complement Long	RRE	<u>Data Transfer Instructions</u>	390
B314	<u>SQEBR</u>	Square Root Short	RRE	<u>Arithmetic Instructions</u>	390
B315	<u>SQDBR</u>	Square Root Long	RRE	<u>Arithmetic Instructions</u>	390
B316	<u>SQXBR</u>	Square Root Extended	RRE	<u>Arithmetic Instructions</u>	390
B317	<u>MEEBR</u>	Multiply Short	RRE	<u>Arithmetic Instructions</u>	390
B318	<u>KDBR</u>	Compare and Signal Long	RRE	<u>Logic Instructions</u>	390
B319	<u>CDBR</u>	Compare Long	RRE	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B31A	<u>ADBR</u>	Add Long	RRE	<u>Arithmetic Instructions</u>	390
B31B	<u>SDBR</u>	Subtract Long	RRE	<u>Arithmetic Instructions</u>	390
B31C	<u>MDBR</u>	Multiply Long	RRE	<u>Arithmetic Instructions</u>	390
B31D	<u>DDBR</u>	Divide Long	RRE	<u>Arithmetic Instructions</u>	390
B31E	<u>MADBR</u>	Multiply and Add Long	RRE	<u>Arithmetic Instructions</u>	390
B31F	<u>MSDBR</u>	Multiply and Subtract Long	RRE	<u>Arithmetic Instructions</u>	390
B324	<u>LDER</u>	Load Lengthened Short/Long	RRE	<u>Data Transfer Instructions</u>	390
B325	<u>LXDR</u>	Load Lengthened Long/Extended	RRE	<u>Data Transfer Instructions</u>	390
B326	<u>LXER</u>	Load Lengthened Short/Extended	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B32E	<u>MAER</u>	Multiply and Add Short	RRF	<u>Arithmetic Instructions</u>	390
B32F	<u>MSER</u>	Multiply and Subtract Short	RRF	<u>Arithmetic Instructions</u>	390
B336	<u>SQXR</u>	Square Root Extended	RRE	<u>Arithmetic Instructions</u>	390
B337	<u>MEER</u>	Multiply (Short*Short to Short)	RRE	<u>Arithmetic Instructions</u>	390
B338	<u>MAYLR</u>	Multiply and Add Unnormalized (Long>Ext. Low)	RRD	<u>Arithmetic Instructions</u>	Z
B339	<u>MYLR</u>	Multiply Unnormalized (Long>Ext. Low)	RRD	<u>Arithmetic Instructions</u>	Z
B33A	<u>MAYR</u>	Multiply and Add Unnormalized (Long>Extended)	RRD	<u>Arithmetic Instructions</u>	Z
B33B	<u>MYR</u>	Multiply Unnormalized (Long>Extended)	RRD	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B33C	<u>MAYHR</u>	Multiply and Add Unnormalized (Long>Ext. High)	RRD	<u>Arithmetic Instructions</u>	Z
B33D	<u>MYHR</u>	Multiply Unnormalized (Long>Ext. High)	RRD	<u>Arithmetic Instructions</u>	Z
B33E	<u>MADR</u>	Multiply and Add Long	RRF	<u>Arithmetic Instructions</u>	390
B33F	<u>MSDR</u>	Multiply and Subtract Long	RRF	<u>Arithmetic Instructions</u>	390
B340	<u>LPXBR</u>	Load Positive Extended	RRE	<u>Data Transfer Instructions</u>	390
B341	<u>LNXBR</u>	Load Negative Extended	RRE	<u>Data Transfer Instructions</u>	390
B342	<u>LTXBR</u>	Load and Test Extended	RRE	<u>Data Transfer Instructions</u>	390
B343	<u>LCXBR</u>	Load Complement Extended	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B344	<u>LEDBR</u>	Load Rounded Long/Short	RRE	<u>Data Transfer Instructions</u>	390
B344	<u>LEDBRA</u>	Load Rounded Long/Short	RRF-e	<u>Data Transfer Instructions</u>	Z
B345	<u>LDXBR</u>	Load Rounded Extended/Long	RRE	<u>Data Transfer Instructions</u>	390
B345	<u>LDXBRA</u>	Load Rounded Extended/Long	RRF-e	<u>Data Transfer Instructions</u>	Z
B346	<u>LEXBR</u>	Load Rounded Extended/Short	RRE	<u>Data Transfer Instructions</u>	390
B346	<u>LEXBRA</u>	Load Rounded Extended/Short	RRF-e	<u>Data Transfer Instructions</u>	Z
B347	<u>FIXBR</u>	Load FP Integer Extended	RRF-e	<u>Data Transfer Instructions</u>	390
B348	<u>KXBR</u>	Compare and Signal Extended	RRE	<u>Logic Instructions</u>	390

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B349	<u>CXBR</u>	Compare Extended	RRE	<u>Logic Instructions</u>	390
B34A	<u>AXBR</u>	Add Extended	RRE	<u>Arithmetic Instructions</u>	390
B34B	<u>SXBR</u>	Subtract Extended	RRE	<u>Arithmetic Instructions</u>	390
B34C	<u>MXBR</u>	Multiply Extended	RRE	<u>Arithmetic Instructions</u>	390
B34D	<u>DXBR</u>	Divide Extended	RRE	<u>Arithmetic Instructions</u>	390
B350	<u>TBEDR</u>	Convert Short to Long	RRF	<u>Data Transfer Instructions</u>	390
B351	<u>TBDR</u>	Convert Long	RRF	<u>Data Transfer Instructions</u>	390
B353	<u>DIEBR</u>	Divide to Integer Short	RRF	<u>Arithmetic Instructions</u>	390
B357	<u>FIEBR</u>	Load FP Integer Short	RRF-e	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B357	<u>FIEBRA</u>	Load FP Integer Short	RRF-e	<u>Data Transfer Instructions</u>	Z
B358	<u>THDER</u>	Convert Short to Long	RRE	<u>Data Transfer Instructions</u>	390
B359	<u>THDR</u>	Convert Long	RRE	<u>Data Transfer Instructions</u>	390
B35B	<u>DIDBR</u>	Divide to Integer Long	RRF	<u>Arithmetic Instructions</u>	390
B35F	<u>FIDBR</u>	Load FP Integer Long	RRF-e	<u>Data Transfer Instructions</u>	390
B35F	<u>FIDBRA</u>	Load FP Integer Long	RRF-e	<u>Data Transfer Instructions</u>	Z
B360	<u>LPXR</u>	Load Positive Extended	RRE	<u>Data Transfer Instructions</u>	390
B361	<u>LNXR</u>	Load Negative Extended	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B362	<u>LTXR</u>	Load and Test Extended	RRE	<u>Data Transfer Instructions</u>	390
B363	<u>LCXR</u>	Load Complement Extended	RRE	<u>Data Transfer Instructions</u>	390
B365	<u>LXR</u>	Load Extended	RRE	<u>Data Transfer Instructions</u>	390
B366	<u>LEXR</u>	Load Rounded Extended/Short	RRE	<u>Data Transfer Instructions</u>	390
B367	<u>FIXR</u>	Load FP Integer Extended	RRF-e	<u>Data Transfer Instructions</u>	390
B367	<u>FIXRA</u>	Load FP Integer Extended	RRF-e	<u>Data Transfer Instructions</u>	Z
B369	<u>CXR</u>	Compare Extended	RRE	<u>Logic Instructions</u>	390
B370	<u>LPDFR</u>	Load Positive (Long)	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B371	<u>LNDFR</u>	Load Negative (Long)	RRE	<u>Data Transfer Instructions</u>	390
B372	<u>CPSDR</u>	Copy Sign (Long)	RRF	<u>Other Instructions</u>	390
B373	<u>LCDFR</u>	Load Complement (Long)	RRE	<u>Data Transfer Instructions</u>	390
B374	<u>LZER</u>	Load Zero (Short)	RRE	<u>Data Transfer Instructions</u>	390
B375	<u>LZDR</u>	Load Zero (Long)	RRE	<u>Data Transfer Instructions</u>	390
B376	<u>LZXR</u>	Load Zero (Extended)	RRE	<u>Data Transfer Instructions</u>	390
B377	<u>FIER</u>	Load FP Integer (Short)	RRE	<u>Data Transfer Instructions</u>	390
B37F	<u>FIDR</u>	Load FP Integer (Long)	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B384	<u>SFPC</u>	Set FPC	RRE	<u>Other Instructions</u>	390
B385	<u>SFASR</u>	Set FPC and Signal	RRE	<u>Other Instructions</u>	390
B38C	<u>EFPC</u>	Extract FPC	RRE	<u>Other Instructions</u>	390
B390	<u>CELBRA</u>	Convert from Logical (32/Short)	RRF-e	<u>Other Instructions</u>	Z
B391	<u>CDLBRA</u>	Convert from Logical (32/Long)	RRF-e	<u>Other Instructions</u>	Z
B392	<u>CXLBRA</u>	Convert from Logical (32/Extended)	RRF-e	<u>Other Instructions</u>	Z
B394	<u>CEFBR</u>	Convert from Fixed (32/Short)	RRE	<u>Other Instructions</u>	390
B394	<u>CEFBRA</u>	Convert from Fixed (32/Short)	RRF-e	<u>Other Instructions</u>	Z
B395	<u>CDFBR</u>	Convert from Fixed (32/Long)	RRE	<u>Other Instructions</u>	390
B395	<u>CDFBRA</u>	Convert from Fixed (32/Long)	RRF-e	<u>Other Instructions</u>	Z

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B396	<u>CXFBR</u>	Convert from Fixed (32/Extended)	RRE	<u>Other Instructions</u>	390
B396	<u>CXF BRA</u>	Convert from Fixed (32/Extended)	RRF-e	<u>Other Instructions</u>	Z
B398	<u>CFEBR</u>	Convert to Fixed (32/Short)	RRF-e	<u>Other Instructions</u>	390
B398	<u>CFEB RA</u>	Convert to Fixed (32/Short)	RRF-e	<u>Other Instructions</u>	Z
B399	<u>CFDBR</u>	Convert to Fixed (32/Long)	RRF-e	<u>Other Instructions</u>	390
B399	<u>CFDB RA</u>	Convert to Fixed (32/Long)	RRF-e	<u>Other Instructions</u>	Z
B39A	<u>CFXBR</u>	Convert to Fixed (32/Extended)	RRF-e	<u>Other Instructions</u>	390
B39A	<u>CFXB RA</u>	Convert to Fixed (32/Extended)	RRF-e	<u>Other Instructions</u>	Z
B39C	<u>CLFEBR</u>	Convert to Logical (32/Short)	RRF-e	<u>Other Instructions</u>	Z
B39D	<u>CLFD BR</u>	Convert to Logical (32/Long)	RRF-e	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B39E	<u>CLFXBR</u>	Convert to Logical (32/Extended)	RRF-e	<u>Other Instructions</u>	Z
B3A0	<u>CELBRA</u>	Convert from Logical (64/Short)	RRF-e	<u>Other Instructions</u>	Z
B3A1	<u>CDLBRA</u>	Convert from Logical (64/Long)	RRF-e	<u>Other Instructions</u>	Z
B3A2	<u>CXLBRA</u>	Convert from Logical (64/Exteded)	RRF-e	<u>Other Instructions</u>	Z
B3A4	<u>CEGBR</u>	Convert from Fixed (64/Short)	RRE	<u>Other Instructions</u>	Z
B3A4	<u>CEGBRA</u>	Convert from Fixed (64/Short)	RRF-e	<u>Other Instructions</u>	Z
B3A5	<u>CDGBR</u>	Convert from Fixed (64/Long)	RRE	<u>Other Instructions</u>	Z
B3A5	<u>CDGBRA</u>	Convert from Fixed (64/Long)	RRF-e	<u>Other Instructions</u>	Z
B3A6	<u>CXGBR</u>	Convert from Fixed (64/Exteded)	RRE	<u>Other Instructions</u>	Z
B3A6	<u>CXGBRA</u>	Convert from Fixed (64/Exteded)	RRF-e	<u>Other Instructions</u>	Z

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3A8	<u>CGEBR</u>	Convert to Fixed (64/Short)	RRF-e	<u>Other Instructions</u>	Z
B3A8	<u>CGEBRA</u>	Convert to Fixed (64/Short)	RRF-e	<u>Other Instructions</u>	Z
B3A9	<u>CGDBR</u>	Convert to Fixed (64/Long)	RRF-e	<u>Other Instructions</u>	Z
B3A9	<u>CGDBRA</u>	Convert to Fixed (64/Long)	RRF-e	<u>Other Instructions</u>	Z
B3AA	<u>CGXBR</u>	Convert to Fixed (64/Extended)	RRF-e	<u>Other Instructions</u>	Z
B3AA	<u>CGXBRA</u>	Convert to Fixed (64/Extended)	RRF-e	<u>Other Instructions</u>	Z
B3AC	<u>CLGEBR</u>	Convert to Logical (64/Short)	RRF-e	<u>Other Instructions</u>	Z
B3AD	<u>CLGDBR</u>	Convert to Logical (64/Long)	RRF-e	<u>Other Instructions</u>	Z
B3AE	<u>CLGXBR</u>	Convert to Logical (64/Extended)	RRF-e	<u>Other Instructions</u>	Z
B3B4	<u>CEFR</u>	Convert from Fixed (32/Short)	RRE	<u>Other Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3B5	<u>CDFR</u>	Convert from Fixed (32/Long)	RRE	<u>Other Instructions</u>	390
B3B6	<u>CXFR</u>	Convert from Fixed (32/Extended)	RRE	<u>Other Instructions</u>	390
B3B8	<u>CFER</u>	Convert to Fixed (Short/32)	RRF	<u>Other Instructions</u>	390
B3B9	<u>CFDR</u>	Convert to Fixed (Long/32)	RRF	<u>Other Instructions</u>	390
B3BA	<u>CFXR</u>	Convert to Fixed (Extended/32)	RRF	<u>Other Instructions</u>	390
B3C1	<u>LDGR</u>	Load FPR from GPR (Long)	RXY	<u>Data Transfer Instructions</u>	390
B3C4	<u>CEGR</u>	Convert from Fixed (64/Short)	RRE	<u>Other Instructions</u>	Z
B3C5	<u>CDGR</u>	Convert from Fixed (64/Long)	RRE	<u>Other Instructions</u>	Z
B3C6	<u>CXGR</u>	Convert from Fixed (64/Extended)	RRE	<u>Other Instructions</u>	Z
B3C8	<u>CGER</u>	Convert to Fixed (Short/64)	RRF	<u>Other Instructions</u>	Z

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3C9	<u>CGDR</u>	Convert to Fixed (Long/64)	RRF	<u>Other Instructions</u>	Z
B3CA	<u>CGXR</u>	Convert to Fixed (Extended/64)	RRF	<u>Other Instructions</u>	Z
B3CD	<u>LGDR</u>	Load GPR from FPR (Long)	RXY	<u>Data Transfer Instructions</u>	390
B3D0	<u>MDTR</u>	Multiply (Long)	RRR	<u>Arithmetic Instructions</u>	390
B3D0	<u>MDTRA</u>	Multiply (Long)	RRF-a	<u>Arithmetic Instructions</u>	Z
B3D1	<u>DDTR</u>	Divide (Long)	RRF-a	<u>Arithmetic Instructions</u>	390
B3D2	<u>ADTR</u>	Add (Long)	RRF-a	<u>Arithmetic Instructions</u>	390
B3D2	<u>ADTRA</u>	Add (Long)	RRF-a	<u>Arithmetic Instructions</u>	Z
B3D3	<u>SDTR</u>	Subtract (Long)	RRF-a	<u>Arithmetic Instructions</u>	390
B3D3	<u>SDTRA</u>	Subtract (Long)	RRF-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3D4	<u>LDETR</u>	Load Lengthened (Short/Long)	RRF-d	<u>Data Transfer Instructions</u>	390
B3D5	<u>LEDTR</u>	Load Rounded (Long/Short)	RRF-e	<u>Data Transfer Instructions</u>	390
B3D6	<u>LTDTR</u>	Load and Test (Long)	RRE	<u>Data Transfer Instructions</u>	390
B3D7	<u>FIDTR</u>	Load Floating-Point Integer (Long)	RRF-e	<u>Data Transfer Instructions</u>	390
B3D8	<u>MXTR</u>	Multiply (Extended)	RRF-a	<u>Arithmetic Instructions</u>	390
B3D8	<u>MXTRA</u>	Multiply (Extended)	RRF-a	<u>Arithmetic Instructions</u>	Z
B3D9	<u>DXTR</u>	Divide (Extended)	RRF-a	<u>Arithmetic Instructions</u>	390
B3DA	<u>AXTR</u>	Add (Extended)	RRF-a	<u>Arithmetic Instructions</u>	390
B3DA	<u>AXTRA</u>	Add (Extended)	RRF-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3DB	<u>SXT</u>	Subtract (Extended)	RRF-a	<u>Arithmetic Instructions</u>	390
B3DB	<u>SXTA</u>	Subtract (Extended)	RRF-a	<u>Arithmetic Instructions</u>	Z
B3DC	<u>LXDTR</u>	Load Lengthened (Long/Extended)	RRF	<u>Data Transfer Instructions</u>	390
B3DD	<u>LDXTR</u>	Load Rounded (Extended/Long)	RRF	<u>Data Transfer Instructions</u>	390
B3DE	<u>LTXTR</u>	Load and Test (Extended)	RRE	<u>Data Transfer Instructions</u>	390
B3DF	<u>FIXTR</u>	Load Floating-Point Integer (Extended)	RRF	<u>Data Transfer Instructions</u>	390
B3E0	<u>KDTR</u>	Compare and Signal (Long)	RRE	<u>Logic Instructions</u>	390
B3E1	<u>CGDTR</u>	Convert to Fixed (Long/64)	RRF-e	<u>Other Instructions</u>	Z
B3E1	<u>CGDTRA</u>	Convert to Fixed (Long/64)	RRF-e	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3E2	<u>CUDTR</u>	Convert to 64b U.Packed (Long)	RRF	<u>Other Instructions</u>	390
B3E3	<u>CSDTR</u>	Convert to 64b S.Packed (Long)	RRF	<u>Other Instructions</u>	390
B3E4	<u>CDTR</u>	Compare (Long)	RRE	<u>Logic Instructions</u>	390
B3E5	<u>EEDTR</u>	Extract Biased Exponent (Long)	RRE	<u>Other Instructions</u>	390
B3E7	<u>ESDTR</u>	Extract Significance (Long)	RRE	<u>Other Instructions</u>	390
B3E8	<u>KXTR</u>	Compare and Signal (Extended)	RRE	<u>Logic Instructions</u>	390
B3E9	<u>CGXTR</u>	Convert to Fixed (Extended/64)	RRF-e	<u>Other Instructions</u>	Z
B3E9	<u>CGXTRA</u>	Convert to Fixed (Extended/64)	RRF-e	<u>Other Instructions</u>	Z
B3EA	<u>CUXTR</u>	Convert to 128b U.Packed (Extended)	RRF	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3EB	<u>CSXTR</u>	Convert to 128b S.Packed (Extended)	RRF	<u>Other Instructions</u>	Z
B3EC	<u>CXTR</u>	Compare (Extended)	RRE	<u>Logic Instructions</u>	390
B3ED	<u>EEXTR</u>	Extract Biased Exponent (Extended)	RRE	<u>Other Instructions</u>	Z
B3EF	<u>ESXTR</u>	Extract Significance (Extended)	RRE	<u>Other Instructions</u>	Z
B3F1	<u>CDGTR</u>	Convert from Fixed (64/Long)	RRE	<u>Other Instructions</u>	Z
B3F1	<u>CDGTRA</u>	Convert from Fixed (64/Long)	RRE	<u>Other Instructions</u>	Z
B3F2	<u>CUSTR</u>	Convert from 64b U.Packed (Long)	RRE	<u>Other Instructions</u>	390
B3F3	<u>CDSTR</u>	Convert from 64b S.Packed (Long)	RRE	<u>Other Instructions</u>	390
B3F4	<u>CEDTR</u>	Compare Biased Exponent (Long)	RRE	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3F5	<u>QADTR</u>	Quantize (Long)	RRF-b	<u>Other Instructions</u>	390
B3F6	<u>IEDTR</u>	Insert Biased Exponent (Long)	RRF-b	<u>Other Instructions</u>	390
B3F7	<u>RRDTR</u>	Reround (Long)	RRF-b	<u>Other Instructions</u>	390
B3F9	<u>CXGTR</u>	Convert from Fixed (64/Extended)	RRE	<u>Other Instructions</u>	Z
B3F9	<u>CXGTRA</u>	Convert from Fixed (64/Extended)	RRE	<u>Other Instructions</u>	Z
B3FA	<u>CXUTR</u>	Convert from 128b U.Packed (Extended)	RRE	<u>Other Instructions</u>	Z
B3FB	<u>CXSTR</u>	Convert from 128b S.Packed (Extended)	RRE	<u>Other Instructions</u>	Z
B3FC	<u>CEXTR</u>	Compare Biased Exponent (Extended)	RRE	<u>Logic Instructions</u>	Z
B3FD	<u>QAXTR</u>	Quantize (Extended)	RRF-b	<u>Other Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B3FE	<u>IEXTR</u>	Insert Biased Exponent (Extended)	RRF-b	<u>Other Instructions</u>	390
B3FF	<u>RRXTR</u>	Reround (Extended)	RRF-b	<u>Other Instructions</u>	390
B6	<u>STCTL</u>	Store ConTroL	RS	<u>Privileged Instructions</u>	370
B7	<u>LCTL</u>	Load ConTroL	RS	<u>Privileged Instructions</u>	370
B8	<u>LMC</u>	Load Multiple Control	RS	<u>Privileged Instructions</u>	390
B900	<u>LPGR</u>	Load Positive Register (64 bit)		<u>Data Transfer Instructions</u>	Z
B901	<u>LNGR</u>	Load Negative Register (64 bit)		<u>Data Transfer Instructions</u>	Z
B902	<u>LTGR</u>	Load and Test Register (64 bit)		<u>Data Transfer Instructions</u>	Z
B903	<u>LCGR</u>	Load and Complement Register (64 bit)	RRE	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B904	<u>LGR</u>	Load Register (64 bit)	RRE	<u>Data Transfer Instructions</u>	Z
B905	<u>LURAG</u>	Load Using Real Address (64 bit)	RRE	<u>Privileged Instructions</u>	Z
B906	<u>LGBR</u>	Load Byte (8/64)	RRE	<u>Data Transfer Instructions</u>	Z
B908	<u>AGR</u>	Add (64)	RRE	<u>Arithmetic Instructions</u>	Z
B909	<u>SGR</u>	Subtract (64)	RRE	<u>Arithmetic Instructions</u>	Z
B90A	<u>ALGR</u>	Add Logical (64)	RRE	<u>Arithmetic Instructions</u>	Z
B90B	<u>SLGR</u>	Subtract Logical (64)	RRE	<u>Arithmetic Instructions</u>	Z
B90C	<u>MSGR</u>	Multiply Single (64)	RRE	<u>Arithmetic Instructions</u>	Z
B90D	<u>DSGR</u>	Divide Single (64)	RRE	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B90E	<u>EREGG</u>	Extract Stacked Registers (64)	RRE	<u>Data Transfer Instructions</u>	Z
B90F	<u>LRVGR</u>	Load Reserved (64)	RRE	<u>Data Transfer Instructions</u>	Z
B910	<u>LPGFR</u>	Load Positive (32/64)	RRE	<u>Data Transfer Instructions</u>	Z
B911	<u>LNGFR</u>	Load Negative (32/64)	RRE	<u>Data Transfer Instructions</u>	Z
B912	<u>LTGFR</u>	Load And Test (32/64)	RRE	<u>Data Transfer Instructions</u>	Z
B913	<u>LCGFR</u>	Load Complement (32/64)	RRE	<u>Data Transfer Instructions</u>	Z
B914	<u>LGFR</u>	Load (32/64)	RRE	<u>Data Transfer Instructions</u>	Z
B916	<u>LLGFR</u>	Load Logical (32/64)	RRE	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B917	<u>LLGTR</u>	Load Logical Thirty One Bits (31/64)	RRE	<u>Data Transfer Instructions</u>	Z
B918	<u>AGFR</u>	Add (32/64)	RRE	<u>Arithmetic Instructions</u>	Z
B919	<u>SGFR</u>	Subtract (32/64)	RRE	<u>Arithmetic Instructions</u>	Z
B91A	<u>ALGFR</u>	Add Logical (32/64)	RRE	<u>Arithmetic Instructions</u>	Z
B91B	<u>SLGFR</u>	Subtract Logical (32/64)	RRE	<u>Arithmetic Instructions</u>	Z
B91C	<u>MSGFR</u>	Multiply Single (32/64)	RRE	<u>Arithmetic Instructions</u>	Z
B91D	<u>DSGFR</u>	Divide Single (32/64)	RRE	<u>Arithmetic Instructions</u>	Z
B91F	<u>LRVR</u>	Load Reversed (32)	RRE	<u>Data Transfer Instructions</u>	390
B920	<u>CGR</u>	Compare (64)	RRE	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B921	<u>CLGR</u>	Compare Logical (64)	RRE	<u>Logic Instructions</u>	Z
B925	<u>STURG</u>	Store Using Real Address	RRE	<u>Privileged Instructions</u>	390
B926	<u>LBR</u>	Load Byte (8/32)	RRE	<u>Data Transfer Instructions</u>	390
B927	<u>LHR</u>	Load Halfword (32<16)	RRE	<u>Data Transfer Instructions</u>	Z
B928	<u>PCKMO</u>	Perform Cryptographic Key Mgmt Operations	RRE	<u>Privileged Instructions</u>	Z
B929	<u>KMA</u>	cipher Message with Authentication	RRF-b	<u>Other Instructions</u>	Z
B92A	<u>KMF</u>	cipher Message with cipher Feedback	RRE	<u>Other Instructions</u>	Z
B92B	<u>KMO</u>	cipher Message with Output feedback	RRE	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B92C	<u>PCC</u>	Perform Cryptographic Computation	RRE	<u>Other Instructions</u>	Z
B92D	<u>KMCTR</u>	cipher Message with CounTeR	RRF-b	<u>Other Instructions</u>	Z
B92E	<u>KM</u>	cipher Message	RRE	<u>Other Instructions</u>	Z
B92F	<u>KMC</u>	cipher Message with Chaining	RRE	<u>Other Instructions</u>	Z
B930	<u>CGFR</u>	Compare (32/64)	RRE	<u>Logic Instructions</u>	Z
B931	<u>CLGFR</u>	Compare Logical (32/64)	RRE	<u>Logic Instructions</u>	Z
B938	<u>SORTL</u>	Sort List	RRE	<u>Other Instructions</u>	Z
B939	<u>DFLTCC</u>	deflate conversion call	RRF-a	<u>Other Instructions</u>	Z
B93A	<u>KDSA</u>	compute digital signature authentication	RRE	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B93C	<u>PRNO</u>	perform random number operation	RRE	<u>Other Instructions</u>	Z
B93E	<u>KIMD</u>	compute intermediate message digest	RRE	<u>Other Instructions</u>	Z
B93F	<u>KLMD</u>	compute last message digest	RRE	<u>Other Instructions</u>	Z
B941	<u>CFDTR</u>	Convert to fixed (Long Dfp to 32)	RRF-e	<u>Other Instructions</u>	Z
B942	<u>CLGDTR</u>	Convert to logical (Long Dfp to 64)	RRF-e	<u>Other Instructions</u>	Z
B943	<u>CLFDTR</u>	Convert to logical (Long Dfp to 32)	RRF-e	<u>Other Instructions</u>	Z
B946	<u>BCTGR</u>	Branch on Count (64)	RRE	<u>Branch Instructions</u>	Z
B949	<u>CFXTR</u>	Convert to Fixed (eXtended Dfp to 32)	RRF-e	<u>Other Instructions</u>	Z
B94A	<u>CLGXTR</u>	Convert to Logical (eXtended Dfp to 64)	RRF-e	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B94B	<u>CLFXTR</u>	Convert to Logical (eXtended Dfp to 32)	RRF-e	<u>Other Instructions</u>	Z
B951	<u>CDFTR</u>	Convert from fixed (32 to Long Dfp)	RRE	<u>Other Instructions</u>	Z
B952	<u>CDLGTR</u>	Convert from Logical (64 to Long Dfp)	RRF-e	<u>Other Instructions</u>	Z
B953	<u>CDLFTR</u>	Convert from Logical (32 to Long Dfp)	RRF-e	<u>Other Instructions</u>	Z
B959	<u>CXFTR</u>	Convert from Fixed (32 to eXtended Dfp)	RRE	<u>Other Instructions</u>	Z
B95A	<u>CXLGTR</u>	Convert from Logical (64 to eXtended Dfp)	RRF-e	<u>Other Instructions</u>	Z
B95B	<u>CXLFTR</u>	Convert from Logical (32 to eXtended Dfp)	RRF-e	<u>Other Instructions</u>	Z
B960	<u>CGRT</u>	Compare and Trap (64)	RRF-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B960-2	<u>CRTH</u>	Compare and Trap on High (32)	RRF-c	<u>Logic Instructions</u>	Z
B960-4	<u>CTRL</u>	Compare and Trap on Low (32)	RRF-c	<u>Logic Instructions</u>	Z
B960-7	<u>CRTE</u>	Compare and Trap on Equal(32)	RRF-c	<u>Logic Instructions</u>	Z
B960-8	<u>CRTNE</u>	Compare and Trap on Not Equal (32)	RRF-c	<u>Logic Instructions</u>	Z
B960-A	<u>CRTNL</u>	Compare and Trap on Not Low (32)	RRF-c	<u>Logic Instructions</u>	Z
B960-C	<u>CRTNH</u>	Compare and Trap on Not High (32)	RRF-c	<u>Logic Instructions</u>	Z
B961	<u>CLGRT</u>	Compare Logical and Trap (64)	RRF	<u>Logic Instructions</u>	Z
B964	<u>NNGRK</u>	Nand (64)	RRF-a	<u>Other Instructions</u>	Z
B965	<u>OCGRK</u>	Or with Complement (64)	RRF-a	<u>Other Instructions</u>	Z
B966	<u>NOGRK</u>	Nor (64)	RRF-a	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B967	<u>NXGRK</u>	Not eXclusive or (64)	RRF-a	<u>Other Instructions</u>	Z
B972	<u>CRT</u>	Compare and Trap (32)	RRF-c	<u>Logic Instructions</u>	Z
B972-2	<u>CRTH</u>	Compare and Trap on High (32)	RRF-c	<u>Logic Instructions</u>	Z
B972-4	<u>CRTL</u>	Compare and Trap on Low (32)	RRF-c	<u>Logic Instructions</u>	Z
B972-7	<u>CRTE</u>	Compare and Trap on Equal(32)	RRF-c	<u>Logic Instructions</u>	Z
B972-8	<u>CRTNE</u>	Compare and Trap on Not Equal (32)	RRF-c	<u>Logic Instructions</u>	Z
B972-A	<u>CRTNL</u>	Compare and Trap on Not Low (32)	RRF-c	<u>Logic Instructions</u>	Z
B972-C	<u>CRTNH</u>	Compare and Trap on Not High (32)	RRF-c	<u>Logic Instructions</u>	Z
B973	<u>CLRT</u>	Compare Logical and Trap (32)	RRF-c	<u>Logic Instructions</u>	Z
B973-2	<u>CLRTH</u>	Compare Logical and Trap on High (32)	RRF-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B973-4	<u>CLRTL</u>	Compare Logical and Trap on Low (32)	RRF-c	<u>Logic Instructions</u>	Z
B973-7	<u>CLRTE</u>	Compare Logical and Trap on Equal(32)	RRF-c	<u>Logic Instructions</u>	Z
B973-8	<u>CLRTNE</u>	Compare Logical and Trap on Not Equal (32)	RRF-c	<u>Logic Instructions</u>	Z
B973-A	<u>CLRTNL</u>	Compare Logical and Trap on Not Low (32)	RRF-c	<u>Logic Instructions</u>	Z
B973-C	<u>CLRTNH</u>	Compare Logical and Trap on Not High (32)	RRF-c	<u>Logic Instructions</u>	Z
B974	<u>NNRK</u>	Nand (32)	RRF-a	<u>Other Instructions</u>	Z
B975	<u>OCRK</u>	Or with Complement (32)	RRF-a	<u>Other Instructions</u>	Z
B976	<u>NORK</u>	Nor (32)	RRF-a	<u>Other Instructions</u>	Z
B977	<u>NXRK</u>	Not eXclusive or (32)	RRF-a	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B980	<u>NGR</u>	aNd (64)	RRE	<u>Arithmetic Instructions</u>	Z
B981	<u>OGR</u>	Or (64)	RRE	<u>Arithmetic Instructions</u>	Z
B982	<u>XGR</u>	eXclusive or (64)	RRE	<u>Arithmetic Instructions</u>	Z
B984	<u>LLGCR</u>	Load Logical Character (8/64)	RRE	<u>Data Transfer Instructions</u>	Z
B985	<u>LLGHR</u>	Load Logical Halfword (16/64)	RRE	<u>Data Transfer Instructions</u>	Z
B986	<u>MLGR</u>	Multiply Logical (64/128)	RRE	<u>Arithmetic Instructions</u>	Z
B987	<u>DLGR</u>	Divide Logical (128/64)	RRE	<u>Arithmetic Instructions</u>	Z
B988	<u>ALCGR</u>	Add Logical with Carry (64)	RRE	<u>Arithmetic Instructions</u>	Z
B989	<u>SLBGR</u>	Subtract Logical with Borrow (64)	RRE	<u>Arithmetic Instructions</u>	Z

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B98D	<u>EPSW</u>	Extract PSW	RRE	<u>Other Instructions</u>	390
B98E	<u>IDTE</u>	Invalidate DAT Table Entry	RRF-b	<u>Privileged Instructions</u>	Z
B98F	<u>CRDTE</u>	Compare and Replace DAT Table Entry	RRF-b	<u>Privileged Instructions</u>	Z
B990	<u>TRTT</u>	Translate Two To Two	RRF-c	<u>Data Transfer Instructions</u>	390
B991	<u>TRTO</u>	Translate Two To One	RRF-c	<u>Data Transfer Instructions</u>	390
B992	<u>TROT</u>	Translate One To Two	RRF-c	<u>Data Transfer Instructions</u>	390
B993	<u>TROO</u>	Translate One To One	RRF-c	<u>Data Transfer Instructions</u>	390
B994	<u>LLCR</u>	Load Logical Character (8/32)	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B995	<u>LLHR</u>	Load Logical Halfword (16/32)	RRE	<u>Data Transfer Instructions</u>	390
B996	<u>MLR</u>	Multiply Logical (32/64)	RRE	<u>Arithmetic Instructions</u>	Z
B997	<u>DLR</u>	Divide Logical (64/32)	RRE	<u>Arithmetic Instructions</u>	Z
B998	<u>ALCR</u>	Add Logical with Carry	RRE	<u>Arithmetic Instructions</u>	390
B999	<u>SLBR</u>	Subtract Logical with Borrow	RRE	<u>Arithmetic Instructions</u>	390
B99A	<u>EPAIR</u>	Extract Primary ASN and Instance	RRE	<u>Privileged Instructions</u>	Z
B99B	<u>ESAIR</u>	Extract Secondary ASN and Instance	RRE	<u>Privileged Instructions</u>	Z
B99D	<u>ESEA</u>	Extract and Set Extended Authority	RRE	<u>Privileged Instructions</u>	390
B99E	<u>PTI</u>	Program Transfer with Instance	RRE	<u>Privileged Instructions</u>	Z
B99F	<u>SSAIR</u>	Set Secondary ASN and Instance	RRE	<u>Privileged Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B9A1	<u>TPEI</u>	Test Pending External Interruption	RRE	<u>Privileged Instructions</u>	Z
B9A2	<u>PTF</u>	Perform Topology Function	RRE	<u>Privileged Instructions</u>	Z
B9AA	<u>LPTEA</u>	Load Page Table Entry Address	RRF-b	<u>Privileged Instructions</u>	Z
B9AC	<u>IRBM</u>	Insert Reference Bits Multiple	RRE	<u>Control Flow Instructions</u>	Z
B9AE	<u>RRBM</u>	Reset Reference Bits Multiple	RRE	<u>Privileged Instructions</u>	Z
B9AF	<u>PFME</u>	Perform Frame Management Function	RRE	<u>Privileged Instructions</u>	Z
B9B0	<u>CU14</u>	Convert UTF-8 to UTF-32	RRF-c	<u>Data Transfer Instructions</u>	390
B9B1	<u>CU24</u>	Convert UTF-16 to UTF-32	RRF-c	<u>Data Transfer Instructions</u>	390
B9B2	<u>CU41</u>	Convert UTF-32 to UTF-8	RRE	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B9B3	<u>CU42</u>	Convert UTF-32 to UTF-16	RRE	<u>Data Transfer Instructions</u>	390
B9BD	<u>TRTE</u>	TTranslate and Test Reverse Extended	RRF-c	<u>Data Transfer Instructions</u>	390
B9BE	<u>SRSTU</u>	Search String Unicode	RRE	<u>Logic Instructions</u>	Z
B9BF	<u>TRTE</u>	TTranslate and Test Extended	RRF-c	<u>Data Transfer Instructions</u>	390
B9C0	<u>SELFHR</u>	SELect High (32)	RRF-a	<u>Other Instructions</u>	Z
B9C8	<u>AHHHR</u>	Add High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9C9	<u>SHHHR</u>	Subtract High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9CA	<u>ALHHHR</u>	Add Logical High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9CB	<u>SLHHHR</u>	Subtract Logical High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B9CD	<u>CHHR</u>	Compare High (32)	RRE	<u>Logic Instructions</u>	Z
B9CF	<u>CLHHR</u>	Compare Logical High (32)	RRE	<u>Logic Instructions</u>	Z
B9D8	<u>AHHLR</u>	Add High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9D9	<u>SHHLR</u>	Subtract High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9DA	<u>ALHHLR</u>	Add Logical High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9DB	<u>SLHHLR</u>	Subtract Logical High (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9DD	<u>CHLR</u>	Compare High (32)	RRE	<u>Logic Instructions</u>	Z
B9DF	<u>CLHLR</u>	Compare Logical High (32)	RRE	<u>Logic Instructions</u>	Z
B9E0	<u>LOCFHR</u>	Load High on Condition (32)	RRF-c	<u>Other Instructions</u>	Z
B9E1	<u>POPCNT</u>	POPulation CouNT	RRF-c	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B9E2	<u>LOCGR</u>	Load on Condition (64)	RRF-c	<u>Other Instructions</u>	Z
B9E3	<u>SELGR</u>	SElect (64)	RRF-a	<u>Logic Instructions</u>	Z
B9E4	<u>NGRK</u>	aNd (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9E5	<u>NCGRK</u>	aNd with Complement (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9E6	<u>OGRK</u>	OR (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9E7	<u>XGRK</u>	eXclusive or (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9E8	<u>AGRK</u>	Add (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9E9	<u>SGRK</u>	Subtract (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9EA	<u>ALGRK</u>	Add Logical (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9EB	<u>SLGRK</u>	Subtract Logical (64)	RRF-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B9EC	<u>MGRK</u>	Multiply (128<64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9ED	<u>MSGRKC</u>	Multiply Single (64)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9F0	<u>SELR</u>	SElect (32)	RRF-a	<u>Logic Instructions</u>	Z
B9F2	<u>LOCR</u>	Load On Condition (32)	RRF-c	<u>Data Transfer Instructions</u>	Z
B9F4	<u>NRK</u>	aNd (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9F5	<u>NCRK</u>	aNd with Complement (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9F6	<u>ORK</u>	OR (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9F7	<u>XRK</u>	eXclusive or (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9F8	<u>ARK</u>	Add (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9F9	<u>SRK</u>	Subtract (32)	RRF-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
B9FA	<u>ALRK</u>	Add Logical (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9FB	<u>SLRK</u>	Subtract Logical (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
B9FD	<u>MSRKC</u>	Multiply Single (32)	RRF-a	<u>Arithmetic Instructions</u>	Z
BA	<u>CS</u>	Compare and Swap	RS	<u>Logic Instructions</u>	370
BB	<u>CDS</u>	Compare Double and Swap	RS	<u>Logic Instructions</u>	370
BD	<u>CLM</u>	Compare Logical Chars. under Mask	RS	<u>Logic Instructions</u>	370
BE	<u>STCM</u>	Store Characters under Mask	RS	<u>Data Transfer Instructions</u>	370
BF	<u>ICM</u>	Insert Characters under Mask	RS	<u>Data Transfer Instructions</u>	370
C00	<u>LARL</u>	Load Address Relative Long	RIL	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C01	<u>LGFI</u>	Load Immediate (32/64)	RIL	<u>Data Transfer Instructions</u>	Z
C04	<u>BRCL</u>	Branch Relative on Condition Long	RIL	<u>Branch Instructions</u>	390
C04	<u>JCL</u>	Jump on Condition Long	RIL	<u>Branch Instructions</u>	390
C04-0	<u>BRUL</u>	No Operation	RIL	<u>Branch Instructions</u>	390
C04-0	<u>JLNOP</u>	No Operation	RIL	<u>Branch Instructions</u>	390
C04-1	<u>BROL</u>	Branch Relative Long on Overflow	RIL	<u>Branch Instructions</u>	390
C04-1	<u>JLO</u>	Jump Long on Overflow	RIL	<u>Branch Instructions</u>	390
C04-2	<u>BRHL</u>	Branch Relative Long on High	RIL	<u>Branch Instructions</u>	390
C04-2	<u>JLH</u>	Jump Long on High	RIL	<u>Branch Instructions</u>	390
C04-2	<u>BRPL</u>	Branch Relative Long on Plus	RIL	<u>Branch Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C04-2	<u>JLP</u>	Jump Long on Plus	RIL	Branch Instructions	390
C04-4	<u>BRLL</u>	Branch Relative Long on Low	RIL	Branch Instructions	390
C04-4	<u>JLL</u>	Jump Long on Low	RIL	Branch Instructions	390
C04-4	<u>BRML</u>	Branch Relative Long on Minus	RIL	Branch Instructions	390
C04-4	<u>JLM</u>	Jump Long on Minus	RIL	Branch Instructions	390
C04-7	<u>BRNEL</u>	Branch Relative Long on Not Equal	RIL	Branch Instructions	390
C04-7	<u>JLNE</u>	Jump Long on Not Equal	RIL	Branch Instructions	390
C04-7	<u>BRNZL</u>	Branch Relative Long on Not Zero	RIL	Branch Instructions	390
C04-7	<u>JLNZ</u>	Jump Long on Not Zero	RIL	Branch Instructions	390
C04-8	<u>BREL</u>	Branch Relative Long on Equal	RIL	Branch Instructions	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C04-8	<u>JLEQ</u>	Jump Long on Equal	RIL	Branch Instructions	390
C04-8	<u>BRZL</u>	Branch Relative Long on Zero	RIL	Branch Instructions	390
C04-8	<u>JLZ</u>	Jump Long on Zero	RIL	Branch Instructions	390
C04-B	<u>BRLL</u>	Branch Relative Long on Not Low	RIL	Branch Instructions	390
C04-B	<u>JLL</u>	Jump Long on Not Low	RIL	Branch Instructions	390
C04-B	<u>BRNML</u>	Branch Relative Long on Not Minus	RIL	Branch Instructions	390
C04-B	<u>JLNM</u>	Jump Long on Not Minus	RIL	Branch Instructions	390
C04-D	<u>BRNHL</u>	Branch Relative Long on Not High	RIL	Branch Instructions	390
C04-D	<u>JLNH</u>	Jump Long on Not High	RIL	Branch Instructions	390
C04-D	<u>BRNPL</u>	Branch Relative Long on Not Plus	RIL	Branch Instructions	390

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C04-D	<u>JLNP</u>	Jump Long on Not Plus	RIL	Branch Instructions	390
C04-E	<u>BRNOL</u>	Branch Relative Long on Not Overflow	RIL	Branch Instructions	390
C04-E	<u>JLNO</u>	Jump Long on Not Overflow	RIL	Branch Instructions	390
C04-F	<u>BRUL</u>	Unconditional Branch Relative Long	RIL	Branch Instructions	390
C04-F	<u>JLU</u>	Unconditional Jump Long	RIL	Branch Instructions	390
C05	<u>BRASL</u>	Branch Relative and Save Long	RIL	Branch Instructions	390
C06	<u>XIHF</u>	eXclusive Or Immediate (high)	RIL	Arithmetic Instructions	390
C07	<u>XILF</u>	eXclusive Or Immediate (low)	RIL	Arithmetic Instructions	390
C08	<u>IIHF</u>	Insert Immediate (high)	RIL	Data Transfer Instructions	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C09	<u>IILF</u>	Insert Immediate (low)	RIL	<u>Data Transfer Instructions</u>	390
C0A	<u>NIHF</u>	aNd Immediate (high)	RIL	<u>Arithmetic Instructions</u>	390
C0B	<u>NILF</u>	aNd Immediate (low)	RIL	<u>Arithmetic Instructions</u>	390
C0C	<u>OIHF</u>	Or Immediate (high)	RIL	<u>Arithmetic Instructions</u>	390
C0D	<u>OILF</u>	Or Immediate (low)	RIL	<u>Arithmetic Instructions</u>	390
C0E	<u>LLIHE</u>	Load Logical Immediate (high)	RIL	<u>Data Transfer Instructions</u>	390
C0F	<u>LLILF</u>	Load Logical Immediate (low)	RIL	<u>Data Transfer Instructions</u>	390
C20	<u>MSGFI</u>	Multiply Single Immediate (32/64)	RIL	<u>Arithmetic Instructions</u>	Z
C21	<u>MSFI</u>	Multiply Single Immediate (32)	RIL	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C24	<u>SLGFI</u>	Subtract Logical Immediate (32/64)	RIL	<u>Arithmetic Instructions</u>	Z
C25	<u>SLFI</u>	Subtract Logical Immediate (32)	RIL	<u>Arithmetic Instructions</u>	Z
C28	<u>AGFI</u>	Add Immediate (32/64)	RIL	<u>Arithmetic Instructions</u>	Z
C29	<u>AIFI</u>	Add Immediate (32)	RIL	<u>Arithmetic Instructions</u>	Z
C2A	<u>ALGFI</u>	Add Logical Immediate (32/64)	RIL	<u>Arithmetic Instructions</u>	Z
C2B	<u>ALFI</u>	Add Logical Immediate (32)	RIL	<u>Arithmetic Instructions</u>	Z
C2C	<u>CGFI</u>	Compare Immediate (32/64)	RIL	<u>Logic Instructions</u>	Z
C2D	<u>CFI</u>	Compare Immediate (32)	RIL	<u>Logic Instructions</u>	Z
C2E	<u>CLGFI</u>	Compare Logical Immediate (32/64)	RIL	<u>Logic Instructions</u>	Z
C2F	<u>CLFI</u>	Compare Logical Immediate (32)	RIL	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C42	<u>LLHRL</u>	Load Logical Halfword Relative Long (16/32)	RIL	<u>Data Transfer Instructions</u>	390
C44	<u>LGHRL</u>	Load Halfword Relative Long (16/64)	RIL	<u>Data Transfer Instructions</u>	Z
C45	<u>LHRL</u>	Load Halfword Relative Long (16/32)	RIL	<u>Data Transfer Instructions</u>	Z
C46	<u>LLGHL</u>	Load Logical Halfword Relative Long (16/64)	RIL	<u>Data Transfer Instructions</u>	Z
C47	<u>STHRL</u>	STore Halfword Relative Long	RIL	<u>Data Transfer Instructions</u>	Z
C48	<u>LGRL</u>	Load Relative Long (64)	RIL	<u>Data Transfer Instructions</u>	Z
C4B	<u>STGRL</u>	STore Relative Long (64)	RIL	<u>Data Transfer Instructions</u>	Z
C4C	<u>LGFLR</u>	Load Relative Long (32/64)	RIL	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C4D	<u>LRL</u>	Load Relative Long (32)	RIL	<u>Data Transfer Instructions</u>	Z
C4E	<u>LLGFRL</u>	Load Logical Relative Long (32/64)	RIL	<u>Data Transfer Instructions</u>	Z
C4F	<u>STRL</u>	Store Relative Long (32)	RIL	<u>Data Transfer Instructions</u>	390
C60	<u>EXRL</u>	Execute Relative Long	RIL	<u>Control Flow Instructions</u>	390
C62	<u>PFDR</u>	Prefetch Data Relative Long	RIL	<u>Data Transfer Instructions</u>	390
C64	<u>CGHRL</u>	Compare Halfword Relative Long (16/64)	RIL	<u>Logic Instructions</u>	Z
C65	<u>CHRL</u>	Compare Halfword Relative Long (16/32)	RIL	<u>Logic Instructions</u>	390
C66	<u>CLGHRL</u>	Compare Logical Relative Long (16/64)	RIL	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C67	<u>CLHRL</u>	Compare Logical Relative Long (16/32)	RIL	<u>Logic Instructions</u>	390
C68	<u>CGRL</u>	Compare Relative Long (64)	RIL	<u>Logic Instructions</u>	Z
C6A	<u>CLGRL</u>	Compare Logical Relative Long (64)	RIL	<u>Logic Instructions</u>	Z
C6C	<u>CGFRL</u>	Compare Logical Relative Long (32/64)	RIL	<u>Logic Instructions</u>	Z
C6D	<u>CRL</u>	Compare Relative Long (32)	RIL	<u>Logic Instructions</u>	390
C6E	<u>CLGFRL</u>	Compare Logical Relative Long (32/64)	RIL	<u>Logic Instructions</u>	Z
C6F	<u>CLRL</u>	Compare Logical Relative Long (32)	RIL	<u>Logic Instructions</u>	390
C80	<u>MVCOS</u>	MoVe Characters with Optional Specifications	SSF	<u>Control Flow Instructions</u>	390
C61	<u>ECTG</u>	Extract Cpu Time	SSF	<u>Other Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
C62	<u>CSST</u>	Compare and Swap and STore	SSF	<u>Logic Instructions</u>	390
C7	<u>BPP</u>	Branch Prediction Preload	SMI	<u>Branch Instructions</u>	Z
C84	<u>LPD</u>	Load Pair Disjoint (32)	SSF	<u>Data Transfer Instructions</u>	Z
C85	<u>LPDG</u>	Load Pair Disjoint (64)	SSF	<u>Data Transfer Instructions</u>	Z
CC6	<u>BRCTH</u>	Branch Relative on CounT High (32)	RIL-b	<u>Branch Instructions</u>	Z
CC8	<u>AIH</u>	Add Immediate High (32)	RIL-a	<u>Arithmetic Instructions</u>	Z
CCA	<u>ALSIH</u>	Add Logical with Signed Immediate High (32)	RIL-a	<u>Arithmetic Instructions</u>	Z
CCB	<u>ALSIHN</u>	Add Logical with Signed Immediate High (32)	RIL-a	<u>Other Instructions</u>	Z
CCD	<u>CIH</u>	Compare Immediate High (32)	RIL-a	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
CCF	<u>CLIH</u>	Compare Logical Immediate High (32)	RIL-a	<u>Logic Instructions</u>	Z
DD	<u>TRTR</u>	TTranslate and Test Reverse	SS-a	<u>Data Transfer Instructions</u>	390
D1	<u>MVN</u>	MoVe Numeric	SS-a	<u>Data Transfer Instructions</u>	360
D2	<u>MVC</u>	MoVe Character	SS-a	<u>Data Transfer Instructions</u>	360
D3	<u>MVZ</u>	MoVe Zone	SS-a	<u>Data Transfer Instructions</u>	360
D4	<u>NC</u>	aNd Character	SS-a	<u>Data Transfer Instructions</u>	360
D5	<u>CLC</u>	Compare Logical Character	SS-a	<u>Logic Instructions</u>	360
D6	<u>OC</u>	Or Character	SS-a	<u>Data Transfer Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
D7	<u>XC</u>	eXclusive-or Character	SS-a	<u>Data Transfer Instructions</u>	360
D9	<u>MVCK</u>	Move Character with Key	SS-d	<u>Control Flow Instructions</u>	370
DA	<u>MVCP</u>	Move Character to Primary	SS-d	<u>Control Flow Instructions</u>	370
DB	<u>MVCS</u>	Move Character to Secondary	SS-d	<u>Control Flow Instructions</u>	370
DC	<u>TR</u>	TRanslate	SS-a	<u>Data Transfer Instructions</u>	360
DD	<u>TRT</u>	TRanslate and Test	SS-a	<u>Data Transfer Instructions</u>	360
DE	<u>ED</u>	EDit	SS-a	<u>Data Transfer Instructions</u>	360
DF	<u>EDMK</u>	EDit and Mark	SS-a	<u>Data Transfer Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E1	<u>PKU</u>	PacK (Unicode)	SS-f	<u>Data Transfer Instructions</u>	390
E2	<u>UNPKU</u>	UNPacK (Unicode)	SS-a	<u>Data Transfer Instructions</u>	390
E302	<u>LTG</u>	Load and Test (64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E303	<u>LRAG</u>	Load Real Address (64)	RXY-a	<u>Other Instructions</u>	390
E304	<u>LG</u>	Load (64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E306	<u>CVBY</u>	ConVert to Binary (32)	RXY-a	<u>Data Transfer Instructions</u>	390
E308	<u>AG</u>	Add (64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E309	<u>SG</u>	Subtract (64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E30A	<u>ALG</u>	Add Logical (64)	RXY-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E30B	<u>SLG</u>	Subtract Logical (64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E30C	<u>MSG</u>	Multiply single (64)	RXY-a	<u>Arithmetic Instructions</u>	390
E30D	<u>DSG</u>	Divide single (64)	RXY-a	<u>Arithmetic Instructions</u>	390
E30E	<u>CVBG</u>	ConVert to Binary (64)	RXY-a	<u>Data Transfer Instructions</u>	390
E30F	<u>LRVG</u>	Load ReVersed (64)	RXY-a	<u>Data Transfer Instructions</u>	390
E312	<u>LT</u>	Load and Test (32)	RXY-a	<u>Data Transfer Instructions</u>	390
E313	<u>LRAY</u>	Load Real Address (32)	RXY-a	<u>Other Instructions</u>	390
E314	<u>LGF</u>	Load Fullword (32/64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E315	<u>LGH</u>	Load Halfword (64)	RXY-a	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E316	<u>LLGF</u>	Load Logical (32/64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E317	<u>LLGT</u>	Load Logical Thirty One Bits	RXY-a	<u>Data Transfer Instructions</u>	Z
E318	<u>AGF</u>	Add (32/64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E319	<u>SGF</u>	Subtract (32/64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E31A	<u>ALGF</u>	Add Logical (32/64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E31B	<u>SLGF</u>	Subtract Logical (32/64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E31C	<u>MSGF</u>	Multiply Single (32/64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E31D	<u>DSGF</u>	Divide Single (32/64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E31E	<u>LRV</u>	Load Reversed (32)	RXY-a	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E31F	<u>LRVH</u>	Load Reversed (16)	RXY-a	<u>Data Transfer Instructions</u>	390
E320	<u>CG</u>	Compare (64)	RXY-a	<u>Logic Instructions</u>	Z
E321	<u>CLG</u>	Compare Logical (64)	RXY-a	<u>Logic Instructions</u>	Z
E324	<u>STG</u>	Store (64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E325	<u>NTSTG</u>	NonTransactional STore (64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E326	<u>CVDY</u>	Convert to Decimal (32)	RXY-a	<u>Data Transfer Instructions</u>	Z
E32A	<u>LZRG</u>	Load and Zero Rightmost Byte (64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E32E	<u>CVDG</u>	Convert to Decimal (64)	RXY-a	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E32F	<u>STRVG</u>	SToRe ReVersed (64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E330	<u>CGF</u>	Compare Fullword (32/64)	RXY-a	<u>Logic Instructions</u>	Z
E331	<u>CLGF</u>	Compare Logical (32/64)	RXY-a	<u>Logic Instructions</u>	Z
E332	<u>LTGF</u>	Load and Test (32/64)	RXY-a	<u>Logic Instructions</u>	Z
E334	<u>CGH</u>	Compare Halfword (16/64)	RXY-a	<u>Logic Instructions</u>	Z
E336	<u>PFD</u>	PreFetch Data	RXY-b	<u>Data Transfer Instructions</u>	390
E338	<u>AGH</u>	Add Halfword (64<16)	RXY-a	<u>Other Instructions</u>	Z
E339	<u>SGH</u>	Subtract Halfword (64<16)	RXY-a	<u>Other Instructions</u>	Z
E33A	<u>LLZRGF</u>	Load Logical and Zero Rightmost Byte (64<32)	RXY-a	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E33B	<u>LZRF</u>	Load and Zero Rightmost Byte (32)	RXY-a	<u>Other Instructions</u>	Z
E33C	<u>MGH</u>	Multiply Halfword (64<16)	RXY-a	<u>Other Instructions</u>	Z
E33E	<u>STRV</u>	STore Reversed (32)	RXY-a	<u>Data Transfer Instructions</u>	390
E33F	<u>STRVH</u>	STore Reversed (16)	RXY-a	<u>Data Transfer Instructions</u>	390
E346	<u>BCTG</u>	Branch on Count (64)	RXY-a	<u>Branch Instructions</u>	Z
E347	<u>BIC</u>	Branch Indirect on Condition	RXY-b	<u>Other Instructions</u>	Z
E347-1	<u>BIO</u>	Branch Indirect on Overflow	RXY-b	<u>Other Instructions</u>	Z
E347-2	<u>BIP</u>	Branch Indirect on Plus	RXY-b	<u>Other Instructions</u>	Z
E347-2	<u>BIH</u>	Branch Indirect on High	RXY-b	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E347-4	<u>BIM</u>	Branch Indirect on Minus	RXY-b	<u>Other Instructions</u>	Z
E347-4	<u>BIL</u>	Branch Indirect on Low	RXY-b	<u>Other Instructions</u>	Z
E347-7	<u>BINZ</u>	Branch Indirect on Not Zero	RXY-b	<u>Other Instructions</u>	Z
E347-7	<u>BINE</u>	Branch Indirect on Not Equal	RXY-b	<u>Other Instructions</u>	Z
E347-8	<u>BIZ</u>	Branch Indirect on Zero	RXY-b	<u>Other Instructions</u>	Z
E347-8	<u>BIE</u>	Branch Indirect on Equal	RXY-b	<u>Other Instructions</u>	Z
E347-B	<u>BINM</u>	Branch Indirect on Not Minus	RXY-b	<u>Other Instructions</u>	Z
E347-B	<u>BINL</u>	Branch Indirect on Not Low	RXY-b	<u>Other Instructions</u>	Z
E347-D	<u>BINP</u>	Branch Indirect on Not Plus	RXY-b	<u>Other Instructions</u>	Z
E347-D	<u>BINH</u>	Branch Indirect on Not High	RXY-b	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E347-E	<u>BINO</u>	Branch Indirect on No Overflow	RXY-b	<u>Other Instructions</u>	Z
E347-F	<u>BI</u>	Branch Indirect	RXY-b	<u>Other Instructions</u>	Z
E348	<u>LLGFSG</u>	Load Logical and Shift Guarded (64<32)	RXY-a	<u>Other Instructions</u>	Z
E349	<u>STGSC</u>	STore Guarded Storage Controls	RXY-a	<u>Other Instructions</u>	Z
E34C	<u>LGG</u>	Load Guarded (64)	RXY-a	<u>Other Instructions</u>	Z
E34D	<u>LGSC</u>	Load Guarded Storage Controls	RXY-a	<u>Other Instructions</u>	Z
E350	<u>STY</u>	Store (32)	RXY-a	<u>Data Transfer Instructions</u>	Z
E351	<u>MSY</u>	Multiply Single (32)	RXY-a	<u>Arithmetic Instructions</u>	Z
E353	<u>MSC</u>	Multiply Single (32)	RXY-a	<u>Other Instructions</u>	Z

Opção de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E354	<u>NY</u>	aNd (32)	RXY-a	Arithmetic Instructions	Z
E355	<u>CLY</u>	Compare Logical (32)	RXY-a	Logic Instructions	Z
E356	<u>OY</u>	Or (32)	RXY-a	Arithmetic Instructions	Z
E357	<u>XY</u>	eXclusive or (32)	RXY-a	Arithmetic Instructions	Z
E358	<u>LY</u>	Load (32)	RXY-a	Data Transfer Instructions	Z
E359	<u>CY</u>	Compare (32)	RXY-a	Logic Instructions	Z
E35A	<u>AY</u>	Add (32)	RXY-a	Arithmetic Instructions	Z
E35B	<u>SY</u>	Subtract (32)	RXY-a	Arithmetic Instructions	Z
E35C	<u>MFY</u>	Multiply (32/64)	RXY-a	Arithmetic Instructions	Z
E35E	<u>ALY</u>	Add Logical (32)	RXY-a	Arithmetic Instructions	Z

Opco de (Hex)	Mnemon ic	Description	Instructi on Format	Instructio n Class	Instructio n Set Architect ure
E35F	<u>SLY</u>	Subtract Logical (32)	RXY-a	<u>Arithmetic Instructions</u>	Z
E370	<u>STHY</u>	STore Halfword	RXY-a	<u>Data Transfer Instructions</u>	Z
E371	<u>LAY</u>	Load Address	RXY-a	<u>Data Transfer Instructions</u>	390
E372	<u>STCY</u>	STore Character	RXY-a	<u>Data Transfer Instructions</u>	Z
E373	<u>ICY</u>	Insert Character	RXY-a	<u>Data Transfer Instructions</u>	Z
E375	<u>LAEY</u>	Load Address Extended	RXY-a	<u>Data Transfer Instructions</u>	390
E376	<u>LB</u>	Load Byte (8/32)	RXY-a	<u>Data Transfer Instructions</u>	390
E377	<u>LGB</u>	Load Byte (8/64)	RXY-a	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E378	<u>LHY</u>	Load Halfword (32)	RXY-a	<u>Data Transfer Instructions</u>	Z
E379	<u>CHY</u>	Compare Halfword (16/32)	RXY-a	<u>Logic Instructions</u>	Z
E37A	<u>AHY</u>	Add Halfword	RXY-a	<u>Arithmetic Instructions</u>	Z
E37B	<u>SHY</u>	Subtract Halfword	RXY-a	<u>Arithmetic Instructions</u>	Z
E37C	<u>MHY</u>	Multiply Halfword (32)	RXY-a	<u>Arithmetic Instructions</u>	Z
E380	<u>NG</u>	aNd (64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E381	<u>OG</u>	Or (64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E382	<u>XG</u>	eXclusive or (64 bit)	RXY-a	<u>Arithmetic Instructions</u>	Z
E383	<u>MSGC</u>	Multiply Single (64)	RXY-a	<u>Other Instructions</u>	Z
E384	<u>MG</u>	Multiply (128<64)	RXY-a	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E385	<u>LGAT</u>	Load and Trap (64)	RXY-a	<u>Other Instructions</u>	Z
E386	<u>MLG</u>	Multiply Logical (64/128)	RXY-a	<u>Arithmetic Instructions</u>	Z
E387	<u>DLG</u>	Divide Logical (128/64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E388	<u>ALCG</u>	Add Logical with Carry (64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E389	<u>SLBG</u>	Subtract Logical with Borrow (64)	RXY-a	<u>Arithmetic Instructions</u>	Z
E38E	<u>STPQ</u>	STore Pair to Quadword	RXY-a	<u>Data Transfer Instructions</u>	Z
E38F	<u>LPQ</u>	Load Pair from Quadword	RXY-a	<u>Data Transfer Instructions</u>	Z
E390	<u>LLGC</u>	Load Logical Character (8/64)	RXY-a	<u>Data Transfer Instructions</u>	Z
E391	<u>LLGH</u>	Load Logical Halfword (16/64)	RXY-a	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E394	<u>LLC</u>	Load Logical Character (32)	RXY-a	<u>Data Transfer Instructions</u>	390
E395	<u>LLH</u>	Load Logical Halfword (16/32)	RXY-a	<u>Data Transfer Instructions</u>	390
E396	<u>ML</u>	Multiply Logical (32/64)	RXY-a	<u>Arithmetic Instructions</u>	390
E397	<u>DL</u>	Divide Logical (64/32)	RXY-a	<u>Arithmetic Instructions</u>	390
E398	<u>ALC</u>	Add Logical with Carry (32)	RXY-a	<u>Arithmetic Instructions</u>	390
E399	<u>SLB</u>	Subtract Logical with Borrow (32)	RXY-a	<u>Arithmetic Instructions</u>	390
E39C	<u>LLGTAT</u>	Load Logical Thirty one bits and Trap (64<31)	RXY-a	<u>Other Instructions</u>	Z
E39D	<u>LLGFAT</u>	Load Logical and Trap (64<32)	RXY-a	<u>Other Instructions</u>	Z
E39F	<u>LAT</u>	Load and Trap (32<32)	RXY-a	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E3C0	<u>LBH</u>	Load BYTE High (32<8)	RXY-a	<u>Other Instructions</u>	Z
E3C2	<u>LLCH</u>	Load Logical Character High (32<8)	RXY-a	<u>Other Instructions</u>	Z
E3C3	<u>STCH</u>	STore Character High (8)	RXY-a	<u>Other Instructions</u>	Z
E3C4	<u>LHH</u>	Load Halfword High (32<16)	RXY-a	<u>Other Instructions</u>	Z
E3C6	<u>LLHH</u>	Load Logical Halfword High (32<16)	RXY-a	<u>Other Instructions</u>	Z
E3C7	<u>STHH</u>	STore Halfword High (16)	RXY-a	<u>Other Instructions</u>	Z
E3C8	<u>LFHAT</u>	Load High and Trap (32<32)	RXY-a	<u>Other Instructions</u>	Z
E3CA	<u>LFH</u>	Load High (32)	RXY-a	<u>Other Instructions</u>	Z
E3CB	<u>STFH</u>	STore High (32)	RXY-a	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E3CD	<u>CHF</u>	Compare High (32)	RXY-a	<u>Logic Instructions</u>	Z
E3CF	<u>CLHF</u>	Compare Logical High (32)	RXY-a	<u>Logic Instructions</u>	Z
E4--		Vector Instructions	RRE	370 and 390 Only <u>Other Instructions</u>	370
E400	<u>VLI</u>	Vector Load Indirect	RRE	370 and 390 Only <u>Data Transfer Instructions</u>	370
E401	<u>VSTI</u>	Vector STore Indirect	RRE	370 and 390 Only <u>Data Transfer Instructions</u>	370
E410	<u>VLID</u>	Vector Load Indirect Double	RRE	370 and 390 Only <u>Data Transfer Instructions</u>	370
E401	<u>VSTID</u>	Vector Store Indirect Double	RRE	370 and 390 Only <u>Data Transfer Instructions</u>	370
E424	<u>VSRL</u>	Vector Shift Right single Logical	RRE	370 and 390 Only <u>Shift</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
				<u>and Rotate Instructions</u>	
E425	<u>VSL</u>	Vector Shift Left single Logical	RRE	370 and 390 Only <u>Shift and Rotate Instructions</u>	370
E428	<u>VLBIX</u>	Vector Load Bit IndeX	RRE	370 and 390 Only <u>Data Transfer Instructions</u>	370
E500	<u>LASP</u>	Load Address Space Parameters	SSE	<u>Privileged Instructions</u>	370
E501	<u>TPROT</u>	Test PROTection	SSE	<u>Privileged Instructions</u>	370
E502		Fix Page	SS	MVS Assist <u>Other Instructions</u>	370
E502	<u>STRAG</u>	STore Real Address Grande	SSE	<u>Privileged Instructions</u>	370
E503		SVC Assist		MVS Assist <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E504		Obtain Local Lock		MVS Assist Other Instructions	370
E505		Release Local Lock		MVS Assist Other Instructions	370
E506		Obtain CMS Lock		MVS Assist Other Instructions	370
E507		Release CMS Lock		MVS Assist Other Instructions	370
E508		Trace SVC Interruption		MVS Assist Other Instructions	370
E509		Trace Program Interruption		MVS Assist Other Instructions	370
E50A		Trace Initial SRB Dispatch		MVS Assist Other Instructions	370
E50A	MVCRL	MOVE Right to Left	SSE	Data Transfer Instructions	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E50B		Trace I/O Interruption		MVS Assist Other Instructions	370
E50C		Trace Task Dispatch		MVS Assist Other Instructions	370
E50D		Trace SVC Return		MVS Assist Other Instructions	370
E50E	MVCSK	Move Characters with Source Key	SSE	Control Flow Instructions	370
E50F	MVCBK	Move Characters with Dest. Key	SSE	Control Flow Instructions	370
E518	DPFET	Divide Packed Fetch		Other Instructions	370
E544	MVHHI	Move Halfword from Halfword Immediate	SIL	Other Instructions	Z
E548	MVGHI	Move Grande from Halfword Immediate	SIL	Other Instructions	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E54C	<u>MVHI</u>	Move fullword from Halfword Immediate	SIL	<u>Other Instructions</u>	Z
E554	<u>CHHSI</u>	Compare Halfword with Halfword Signed Imm.	SIL	<u>Logic Instructions</u>	Z
E555	<u>CLHHSI</u>	Comp. Log. Halfword w/Halfword Signed Imm.	SIL	<u>Logic Instructions</u>	Z
E558	<u>CGHSI</u>	Comp. Grande w/Halfword Signed Imm.	SIL	<u>Logic Instructions</u>	Z
E559	<u>CLGHSI</u>	Compare Log. Grande w/Halfword Imm.	SIL	<u>Logic Instructions</u>	Z
E55C	<u>CHSI</u>	Compare Halfword Signed Imm.	SIL	<u>Logic Instructions</u>	Z
E55D	<u>CLFHSI</u>	Compare Log. Fullword w/Halfword Signed Imm.	SIL	<u>Logic Instructions</u>	Z
E560	<u>TBEGIN</u>	Transaction BEGIN	SIL	<u>Control Flow Instructions</u>	Z

Opco de (Hex)	Mnemon ic	Description	Instructi on Format	Instructio n Class	Instructio n Set Architect ure
E561	<u>TBEGINC</u>	Transaction BEGIN Constrained	SIL	<u>Control Flow Instructions</u>	Z
E600		Get Free Storage Space		VM Assist <u>Other Instructions</u>	370
E601		Return Free Storage Space		VM Assist <u>Other Instructions</u>	370
E601	<u>VLEBRH</u>	Vector Load Byte Reversed Element (16)	VRX	<u>Data Transfer Instructions</u>	Z
E602		Lock Page		VM Assist <u>Other Instructions</u>	370
E602	<u>VLEBRG</u>	Vector Load Byte Reversed Element (64)	VRX	<u>Data Transfer Instructions</u>	Z
E603		Unlock Page		VM Assist <u>Other Instructions</u>	370
E603	<u>VLEBRF</u>	Vector Load Byte Reversed Element (32)	VRX	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E604		Decode Subsequent CCW Commands		VM Assist Other Instructions	370
E604	<u>VLLEBRZ</u>	Vector Load Byte Reversed Element and Zero	VRX	<u>Data Transfer Instructions</u>	Z
E605		Free CCW Storage		VM Assist Other Instructions	370
E605	<u>VLBRREP</u>	Vector Load Byte Reversed Element and REPlicate	VRX	<u>Data Transfer Instructions</u>	Z
E606		Locate Virtual I/O Control Blocks		VM Assist Other Instructions	370
E606	<u>VLBR</u>	Vector Load Byte Reversed Elements	VRX	<u>Data Transfer Instructions</u>	Z
E607		Dispatch a Block or Virtual Machine		VM Assist Other Instructions	370
E607	<u>VLER</u>	Vector Load Elements Reversed	VRX	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E608		Test Page Status		VM Assist Other Instructions	370
E609		Test Page Status and Lock		VM Assist Other Instructions	370
E609	VSTEBRH	Vector STore Byte Reversed Element (16)	VRX	Data Transfer Instructions	Z
E60A		Invalidate Segment Table		VM Assist Other Instructions	370
E60A	VSTEBRG	Vector STore Byte Reversed Element (64)	VRX	Data Transfer Instructions	Z
E60B		Invalidate Page Table		VM Assist Other Instructions	370
E60B	VSTEBRF	Vector STore Byte Reversed Element (32)	VRX	Data Transfer Instructions	Z
E60C		Decode First CCW Command		VM Assist Other Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E60D		Main Entry to Dispatcher		VM Assist Other Instructions	370
E60E		Locate Real I/O Control Blocks		VM Assist Other Instructions	370
E60E	VSTBR	Vector STore Byte Reversed Elements	VRX	Data Transfer Instructions	Z
E60F		Common CCW Command Processing		VM Assist Other Instructions	370
E60F	VSTER	Vector STore Elements Reversed	VRX	Data Transfer Instructions	Z
E610		Untranslate CCW		VM Assist Other Instructions	370
E611		Dispatch a Block or Virtual Machine		VM Assist Other Instructions	370
E612		Store ECPS:VM/370 Identification		VM Assist Other Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E613		Locate Changed Shared Page		VM Assist Other Instructions	370
E614		Get Free Storage Space (FRETX)		VM Assist Other Instructions	370
E615		Return Free Storage Space (FRETX)		VM Assist Other Instructions	370
E616		Preferred Machine Assist		VM Assist Other Instructions	370
E634	<u>VPKZ</u>	Vector Pack Zoned	VSI	<u>Data Transfer Instructions</u>	Z
E635	<u>VLRL</u>	Vector Load Rightmost with Length	VSI	<u>Data Transfer Instructions</u>	Z
E637	<u>VLRLR</u>	Vector Load Rightmost with Length	VRS-d	<u>Data Transfer Instructions</u>	Z
E63C	<u>VUPKZ</u>	Vector UnPack ZONED	VSI	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E63D	<u>VSTRL</u>	Vector STore Rightmost with Length	VSI	<u>Data Transfer Instructions</u>	Z
E63F	<u>VSTRLR</u>	Vector STore Rightmost with Length	VRS-d	<u>Data Transfer Instructions</u>	Z
E649	<u>VLIP</u>	Vector Load Immediate Decimal	VRI-h	<u>Data Transfer Instructions</u>	Z
E650	<u>VCVB</u>	Vector Convert to Binary	VRR-i	<u>Arithmetic Instructions</u>	Z
E652	<u>VCVBG</u>	Vector Convert to Binary	VRR-i	<u>Arithmetic Instructions</u>	Z
E658	<u>VCVD</u>	Vector Convert to Decimal	VRI-i	<u>Arithmetic Instructions</u>	Z
E659	<u>VSRP</u>	Vector Shift and Round Decimal	VRI-g	<u>Shift and Rotate Instructions</u>	Z
E65A	<u>VCVDG</u>	Vector Convert to Decimal	VRI-i	<u>Arithmetic Instructions</u>	Z
E65B	<u>VPSOP</u>	Vector Perform Sign OPperation Decimal	VRI-g	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E65F	<u>VTP</u>	Vector Test Decimal	VRR-g	<u>Logic Instructions</u>	Z
E671	<u>VAP</u>	Vector Add Decimal	VRI-f	<u>Arithmetic Instructions</u>	Z
E673	<u>VSP</u>	Vector Subtract Decimal	VRI-f	<u>Arithmetic Instructions</u>	Z
E677	<u>VCP</u>	Vector Compare Decimal	VRR-h	<u>Logic Instructions</u>	Z
E678	<u>VMP</u>	Vector Multiply Decimal	VRI-f	<u>Arithmetic Instructions</u>	Z
E679	<u>VMSP</u>	Vector Multiply and Shift Decimal	VRI-f	<u>Arithmetic Instructions</u>	Z
E67A	<u>VDP</u>	Vector Divide Decimal	VRI-f	<u>Arithmetic Instructions</u>	Z
E67B	<u>VRP</u>	Vector Remainder Decimal	VRI-f	<u>Arithmetic Instructions</u>	Z
E67E	<u>VSDP</u>	Vector Shift and Divide Decimal	VRI-f	<u>Arithmetic Instructions</u>	Z
E700	<u>VLEB</u>	Vector Load Element (8)	VRX	<u>Data Transfer Instructions</u>	Z

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E701	<u>VLEH</u>	Vector Load Element (16)	VRX	Data Transfer Instructions	Z
E702		SVC Handler without Trace		VS1 Assist Other Instructions	370
E702	<u>VLEG</u>	Vector Load Element (64)	VRX	Data Transfer Instructions	Z
E703		SVC Handler with Trace		VS1 Assist Other Instructions	370
E703	<u>VLEF</u>	Vector Load Element (32)	VRX	Data Transfer Instructions	Z
E704		Resume Page Measurement		VS1 Assist Other Instructions	370
E704	<u>VLLEZ</u>	Vector Load Logical Element and Zero	VRX	Data Transfer Instructions	Z
E705		Resume Short Term Unfix		VS1 Assist Other Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E705	<u>VLREP</u>	Vector Load and Replicate	VRX	<u>Data Transfer Instructions</u>	Z
E706	<u>VL</u>	Vector Load	VRX	<u>Data Transfer Instructions</u>	Z
E707		Dispatcher		VS1 Assist <u>Other Instructions</u>	370
E707	<u>VLBB</u>	Vector Load to Block Boundary	VRX	<u>Data Transfer Instructions</u>	Z
E708		SIO Trace		VS1 Assist <u>Other Instructions</u>	370
E708	<u>VSTEB</u>	Vector SToRe Element (8)	VRX	<u>Data Transfer Instructions</u>	Z
E709		Task Switch Trace		VS1 Assist <u>Other Instructions</u>	370
E709	<u>VSTEH</u>	Vector SToRe Element (16)	VRX	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E70A		I/O Interrupt Trace		VS1 Assist <u>Other Instructions</u>	370
E70A	<u>VSTEG</u>	Vector STore Element (64)	VRX	<u>Data Transfer Instructions</u>	Z
E70B		Store ECPS:VS2 Level		VS1 Assist <u>Other Instructions</u>	370
E70B	<u>VSTEF</u>	Vector STore Element (32)	VRX	<u>Data Transfer Instructions</u>	Z
E70C		Set Direct Translate Limit		VS1 Assist <u>Other Instructions</u>	370
E70E	<u>VST</u>	Vector STore	VRX	<u>Data Transfer Instructions</u>	Z
E710		PCB EnQueue LIFO		VS1 Assist <u>Other Instructions</u>	370
E712	<u>VGEG</u>	Vector Gather Element (64)	VRV	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E713	<u>VGEF</u>	Vector Gather Element (32)	VRV	<u>Other Instructions</u>	Z
E71A	<u>VSCEG</u>	Vector Scatter Element (64)	VRV	<u>Other Instructions</u>	Z
E71B	<u>VSCEF</u>	Vector Scatter Element (32)	VRV	<u>Other Instructions</u>	Z
E720		PCB EnQueue FIFO		VS1 Assist <u>Other Instructions</u>	370
E721	<u>VLGV</u>	Vector Load GR from VR Element	VRS-c	<u>Data Transfer Instructions</u>	Z
E722	<u>VLVG</u>	Vector Load VR Element from GR	VRS-b	<u>Data Transfer Instructions</u>	Z
E727	<u>LCBB</u>	Load Count to Block Boundary	RXE	<u>Other Instructions</u>	Z
E730		Double Threaded Dequeue		VS1 Assist <u>Other Instructions</u>	370
E730	<u>VESL</u>	Vector Element Shift Left	VRS-a	<u>Shift and Rotate Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E733	<u>VERLL</u>	Vector Element Rotate Left Logical	VRS-a	<u>Shift and Rotate Instructions</u>	Z
E736	<u>VLM</u>	Vector Load Multiple	VRS-a	<u>Data Transfer Instructions</u>	Z
E737	<u>VLL</u>	Vector Load with Length	VRS-b	<u>Data Transfer Instructions</u>	Z
E738	<u>VESRL</u>	Vector Element Shift Right Logical	VRS-a	<u>Shift and Rotate Instructions</u>	Z
E73A	<u>VESRA</u>	Vector Element Shift Right Arithmetic	VRS-a	<u>Shift and Rotate Instructions</u>	Z
E73E	<u>VSTM</u>	Vector STore Multiple	VRS-a	<u>Data Transfer Instructions</u>	Z
E73F	<u>VSTL</u>	Vector STore with Length	VRS-b	<u>Data Transfer Instructions</u>	Z
E740		Get APCBE		VS1 Assist <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E740	<u>VLEIB</u>	Vector Load Element Immediate (8)	VRI-a	<u>Data Transfer Instructions</u>	Z
E741	<u>VLEIH</u>	Vector Load Element Immediate (16)	VRI-a	<u>Data Transfer Instructions</u>	Z
E742	<u>VLEIG</u>	Vector Load Element Immediate (64)	VRI-a	<u>Data Transfer Instructions</u>	Z
E743	<u>VLEIF</u>	Vector Load Element Immediate (32)	VRI-a	<u>Data Transfer Instructions</u>	Z
E744	<u>VGBM</u>	Vector Generate Byte Mask	VRI-a	<u>Other Instructions</u>	Z
E745	<u>VREPI</u>	Vector REPlicate Immediate	VRI-a	<u>Data Transfer Instructions</u>	Z
E746	<u>VGM</u>	Vector Generate Mask	VRI-b	<u>Other Instructions</u>	Z
E74A	<u>VFTCI</u>	Vector FP Test data Class Immediate	VRI-e	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E74D	<u>VREP</u>	Vector REPlicate	VRI-c	<u>Data Transfer Instructions</u>	Z
E750		Return APCBE		VS1 Assist <u>Other Instructions</u>	370
E750	<u>VPOPCT</u>	Vector POPulation Count	VRR-a	<u>Other Instructions</u>	Z
E752	<u>VCTZ</u>	Vector Count Trailing Zeros	VRR-a	<u>Arithmetic Instructions</u>	Z
E753	<u>VCLZ</u>	Vector Count Leading Zeros	VRR-a	<u>Arithmetic Instructions</u>	Z
E756	<u>VLR</u>	Vector Load	VRR-a	<u>Data Transfer Instructions</u>	Z
E758		Find Gotten Queue Element		VS1 Assist <u>Other Instructions</u>	370
E75C	<u>VISTR</u>	Vector ISolate STRing	VRR-a	<u>Other Instructions</u>	Z
E75F	<u>VSEG</u>	Vector Sign Extend to Doubleword	VRR-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E760		Dequeue Top APCBE		VS1 Assist Other Instructions	370
E760	VMRL	Vector MeRge Low	VRR-c	Other Instructions	Z
E761	VMRH	Vector MeRge High	VRR-c	Other Instructions	Z
E762	VLVGP	Vector Load VR from GRS disjoint	VRR-f	Data Transfer Instructions	Z
E764	VSUM	Vector SUM across word	VRR-c	Arithmetic Instructions	Z
E765	VSUMG	Vector SUM across Doubleword	VRR-c	Arithmetic Instructions	Z
E766	VCKSM	Vector ChecKSuM	VRR-c	Arithmetic Instructions	Z
E767	VSUMQ	Vector SUM across Quadword	VRR-c	Arithmetic Instructions	Z
E768		SMF Storage Monitor		VS1 Assist Other Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E768	<u>VN</u>	Vector aNd	VRR-c	Arithmetic Instructions	Z
E769	<u>VNC</u>	Vector aNd with Complement	VRR-c	Arithmetic Instructions	Z
E76A	<u>VO</u>	Vector Or	VRR-c	Arithmetic Instructions	Z
E76B	<u>VNO</u>	Vector NOR	VRR-c	Arithmetic Instructions	Z
E76C	<u>VNX</u>	Vector Not eXclusive OR	VRR-c	Arithmetic Instructions	Z
E76D	<u>VX</u>	Vector eXclusive OR	VRR-c	Arithmetic Instructions	Z
E76E	<u>VNN</u>	Vector NaNd	VRR-c	Arithmetic Instructions	Z
E76F	<u>VOC</u>	Vector OR with Complement	VRR-c	Arithmetic Instructions	Z
E770		Enqueue RSPTE		VS1 Assist Other Instructions	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E770	<u>VESLV</u>	Vector Element Shift Left	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E772	<u>VERIM</u>	Vector Element Rotate and Insert under Mask	VRI-d	<u>Shift and Rotate Instructions</u>	Z
E773	<u>VERLLV</u>	Vector Element Rotate Left Logical	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E774	<u>VSL</u>	Vector Shift Left	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E775	<u>VSLB</u>	Vector Shift Left by Byte	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E777	<u>VSLDB</u>	Vector Shift Left DOUBLE by Byte	VRI-d	<u>Shift and Rotate Instructions</u>	Z
E778		GETMAIN PPA		VS1 Assist <u>Other Instructions</u>	370
E778	<u>VESRLV</u>	Vector Element Shift Right Logical	VRR-c	<u>Shift and Rotate Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E77A	<u>VESRAV</u>	Vector Element Shift Right Arithmetic	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E77C	<u>VSRL</u>	Vector Shift Right Logical	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E77D	<u>VSRLB</u>	Vector Shift Right Logical by Byte	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E77E	<u>VSRA</u>	Vector Shift Right Arithmetic	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E77F	<u>VSRAB</u>	Vector Shift Right Arithmetic by Byte	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E780		Enqueue RSpte to Bottom		VS1 Assist <u>Other Instructions</u>	370
E780	<u>VFEE</u>	Vector Find Element Equal	VRR-b	<u>Other Instructions</u>	Z
E781	<u>VFENE</u>	Vector Find Element Not Equal	VRR-b	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E782	<u>VFAE</u>	Vector Find Any Element Equal	VRR-b	<u>Other Instructions</u>	Z
E784	<u>VPDI</u>	Vector Permute Doubleword Immediate	VRR-c	<u>Other Instructions</u>	Z
E785	<u>VBPERM</u>	Vector BIT PERMute	VRR-c	<u>Shift and Rotate Instructions</u>	Z
E786	<u>VSLD</u>	Vector Shift Left Double by bit	VRI-d	<u>Shift and Rotate Instructions</u>	Z
E787	<u>VSRD</u>	Vector Shift Right Double by bit	VRI-d	<u>Shift and Rotate Instructions</u>	Z
E788		GETMAIN PPA on Page Boundary		VS1 Assist <u>Other Instructions</u>	370
E78A	<u>VSTRC</u>	Vector String Range Compare	VRR-d	<u>Logic Instructions</u>	Z
E78B	<u>VSTRS</u>	Vector String Search	VRR-d	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E78C	<u>VPERM</u>	Vector PERMute	VRR-e	<u>Shift and Rotate Instructions</u>	Z
E78D	<u>VSEL</u>	Vector SElect	VRR-e	<u>Other Instructions</u>	Z
E78E	<u>VFMS</u>	Vector FP Multiply and Subtract	VRR-e	<u>Arithmetic Instructions</u>	Z
E78F	<u>VFMA</u>	Vector FP Multiply and Add	VRR-e	<u>Arithmetic Instructions</u>	Z
E790		Dequeue Specific RSPTE		VS1 Assist <u>Other Instructions</u>	370
E794	<u>VPK</u>	Vector Pack	VRR-c	<u>Arithmetic Instructions</u>	Z
E795	<u>VPKLS</u>	Vector Pack Logical Saturate	VRR-b	<u>Arithmetic Instructions</u>	Z
E797	<u>VPKS</u>	Vector Pack Saturate	VRR-b	<u>Arithmetic Instructions</u>	Z
E798		FREEMAIN PQA		VS1 Assist <u>Other Instructions</u>	370

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E79E	<u>VFNMS</u>	Vector FP Negative Multiply and Subtract	VRR-e	<u>Arithmetic Instructions</u>	Z
E79F	<u>VFNMA</u>	Vector FP Negative Multiply and Add	VRR-e	<u>Arithmetic Instructions</u>	Z
E7A0		Dequeue First RSPTE		VS1 Assist <u>Other Instructions</u>	370
E7A1	<u>VMLH</u>	Vector Multiply Logical High	VRR-c	<u>Arithmetic Instructions</u>	Z
E7A2	<u>VML</u>	Vector Multiply Low	VRR-c	<u>Arithmetic Instructions</u>	Z
E7A3	<u>VMH</u>	Vector Multiply High	VRR-c	<u>Arithmetic Instructions</u>	Z
E7A4	<u>VMLE</u>	Vector Multiply Logical Even	VRR-c	<u>Arithmetic Instructions</u>	Z
E7A5	<u>VMLO</u>	Vector Multiply Logical Odd	VRR-c	<u>Arithmetic Instructions</u>	Z
E7A6	<u>VME</u>	Vector Multiply EVen	VRR-c	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7A7	<u>VMO</u>	Vector Multiply Odd	VRR-c	<u>Arithmetic Instructions</u>	Z
E7A8		FREEMAIN in Partition		VS1 Assist <u>Other Instructions</u>	370
E7A9	<u>VMALH</u>	Vector Multiply AND Add Logical High	VRR-d	<u>Arithmetic Instructions</u>	Z
E7AA	<u>VMAL</u>	Vector Multiply AND Add Low	VRR-d	<u>Arithmetic Instructions</u>	Z
E7AB	<u>VMAH</u>	Vector Multiply AND Add High	VRR-d	<u>Arithmetic Instructions</u>	Z
E7AC	<u>VMALE</u>	Vector Multiply AND Add Logical Even	VRR-d	<u>Arithmetic Instructions</u>	Z
E7AD	<u>VMALO</u>	Vector Multiply AND Add Logical Odd	VRR-d	<u>Arithmetic Instructions</u>	Z
E7AE	<u>VMAE</u>	Vector Multiply AND Add Even	VRR-d	<u>Arithmetic Instructions</u>	Z
E7AF	<u>VMAO</u>	Vector Multiply AND Add Odd	VRR-d	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7B0		Invalidate Virtual Page		VS1 Assist Other Instructions	370
E7B4	<u>VGFM</u>	Vector Galois Field Multiply sum	VRR-c	Arithmetic Instructions	Z
E7B8		Save GETMAIN/FREEM AIN Status		VS1 Assist Other Instructions	370
E7B8	<u>VMSL</u>	Vector Multiply Sum Logical	VRR-d	Arithmetic Instructions	Z
E7B9	<u>VACCC</u>	Vector Add with Carry Compute Carry	VRR-d	Arithmetic Instructions	Z
E7BB	<u>VAC</u>	Vector Add with Carry	VRR-d	Arithmetic Instructions	Z
E7BC	<u>VGFMA</u>	Vector Galois Field Multiply sum and Accumulate	VRR-d	Arithmetic Instructions	Z
E7BD	<u>VSBCBI</u>	Vector Subtract with Borrow Compute Borrow Indication	VRR-d	Arithmetic Instructions	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7BF	<u>VSBI</u>	Vector Subtract with Borrow Indication	VRR-d	<u>Arithmetic Instructions</u>	Z
E7C0		Short Term Unfix		VS1 Assist <u>Other Instructions</u>	370
E7C0	<u>VCLFP</u>	Vector FP Convert to Logical	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C0	<u>VCLGD</u>	Vector FP Convert to Logical 64-bit	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C1	<u>VCFPL</u>	Vector FP Convert from Logical	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C1	<u>VCDLG</u>	Vector FP Convert from Logical 64-bit	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C2	<u>VCSFP</u>	Vector FP Convert to Fixed	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C2	<u>VCGD</u>	Vector FP Convert to Fixed 64-bit	VRR-a	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemon ic	Description	Instructi on Format	Instructio n Class	Instructio n Set Architect ure
E7C3	<u>VCFPS</u>	Vector FP Convert from Fixed	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C3	<u>VCDG</u>	Vector FP Convert from Fixed 64-bit	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C4	<u>VFLL</u>	Vector FP Load Lengthened	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C5	<u>VFLR</u>	Vector FP Load Rounded	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C7	<u>VFI</u>	Vector Load FP Integer	VRR-a	<u>Data Transfer Instructions</u>	Z
E7C8		Restore GETMAIN/FREEM AIN Status		VS1 Assist <u>Other Instructions</u>	370
E7CA	<u>WFK</u>	Vector FP Compare and Signal Scalar	VRR-a	<u>Logic Instructions</u>	Z
E7CB	<u>WFC</u>	Vector FP Compare Scalar	VRR-a	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7CC	<u>VPSO</u>	Vector FP Perform Sign Operation	VRR-a	<u>Arithmetic Instructions</u>	Z
E7CE	<u>VFSQ</u>	Vector FP SQuare root	VRR-a	<u>Arithmetic Instructions</u>	Z
E7D4	<u>VUPLL</u>	Vector UnPack Logical Low	VRR-a	<u>Arithmetic Instructions</u>	Z
E7D5	<u>VUPLH</u>	Vector UnPack Logical High	VRR-a	<u>Arithmetic Instructions</u>	Z
E7D6	<u>VUPL</u>	Vector UnPack Low	VRR-a	<u>Arithmetic Instructions</u>	Z
E7D7	<u>VUPH</u>	Vector UnPack High	VRR-a	<u>Arithmetic Instructions</u>	Z
E7D8		GETMAIN PQA		VS1 Assist <u>Other Instructions</u>	370
E7D8	<u>VTM</u>	Vector Test under Mask	VRR-a	<u>Logic Instructions</u>	Z
E7D9	<u>VECL</u>	Vector Element Compare Logical	VRR-a	<u>Logic Instructions</u>	Z
E7DB	<u>VEC</u>	Vector Element Compare	VRR-a	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7DE	<u>VLC</u>	Vector Load Complement	VRR-a	<u>Data Transfer Instructions</u>	Z
E7DF	<u>VLP</u>	Vector Load Positive	VRR-a	<u>Data Transfer Instructions</u>	Z
E7E0		Page Measurement		VS1 Assist <u>Other Instructions</u>	370
E7E2	<u>VFS</u>	Vector FP Subtract	VRR-c	<u>Arithmetic Instructions</u>	Z
E7E3	<u>VFA</u>	Vector FP Add	VRR-c	<u>Arithmetic Instructions</u>	Z
E7E5	<u>VFD</u>	Vector FP Divide	VRR-c	<u>Arithmetic Instructions</u>	Z
E7E7	<u>VFM</u>	Vector FP Multiply	VRR-c	<u>Arithmetic Instructions</u>	Z
E7E8		Resume Group1 Suboperation		VS1 Assist <u>Other Instructions</u>	370
E7E8	<u>VFCE</u>	Vector FP Compare Equal	VRR-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7EA	<u>VFCHE</u>	Vector FP Compare High or Equal	VRR-c	<u>Logic Instructions</u>	Z
E7EB	<u>VFCH</u>	Vector FP Compare High	VRR-c	<u>Logic Instructions</u>	Z
E7EE	<u>VFMIN</u>	Vector FP Minimum	VRR-c	<u>Logic Instructions</u>	Z
E7EF	<u>VFMAX</u>	Vector FP Maximum	VRR-c	<u>Logic Instructions</u>	Z
E7F0		Short Term Fix		VS1 Assist <u>Other Instructions</u>	370
E7F0	<u>VAVGL</u>	Vector AVerage Logical	VRR-c	<u>Arithmetic Instructions</u>	Z
E7F1	<u>VACC</u>	Vector Add Compute Carry	VRR-c	<u>Arithmetic Instructions</u>	Z
E7F2	<u>VAVG</u>	Vector AVerage	VRR-c	<u>Arithmetic Instructions</u>	Z
E7F3	<u>VA</u>	Vector Add	VRR-c	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7F5	<u>VSCBI</u>	Vector Subtract Compute Borrow Indication	VRR-c	<u>Arithmetic Instructions</u>	Z
E7F7	<u>VS</u>	Vector Subtract	VRR-c	<u>Arithmetic Instructions</u>	Z
E7F8		Resume Group2 Suboperation		VS1 Assist <u>Other Instructions</u>	370
E7F8	<u>VCEQ</u>	Vector Compare EQUAL	VRR-b	<u>Logic Instructions</u>	Z
E7F9	<u>VCHL</u>	Vector Compare High Logical	VRR-b	<u>Logic Instructions</u>	Z
E7FB	<u>VCH</u>	Vector Compare High	VRR-b	<u>Logic Instructions</u>	Z
E7FC	<u>VMNL</u>	Vector Minimum Logical	VRR-c	<u>Logic Instructions</u>	Z
E7FD	<u>VMXL</u>	Vector Maximum Logical	VRR-c	<u>Logic Instructions</u>	Z
E7FE	<u>VMN</u>	Vector Minimum	VRR-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E7FF	<u>VMX</u>	Vector Maximum	VRR-c	<u>Logic Instructions</u>	Z
E8	<u>MVCIN</u>	MoVe Characters Inverse	SS	<u>Data Transfer Instructions</u>	370
E9	<u>PKA</u>	Pack Ascii	SS	<u>Data Transfer Instructions</u>	390
EA	<u>UNPKA</u>	UnPack Ascii	SS	<u>Data Transfer Instructions</u>	370
EA00	<u>DIL</u>		SS	<u>Other Instructions</u>	390
EA01	<u>BDIL</u>		SS	<u>Other Instructions</u>	390
EA04	<u>ANUM</u>		SS	<u>Other Instructions</u>	390
EA05	<u>COMP</u>		SS	<u>Other Instructions</u>	390
EA08	<u>MCPU</u>		SS	<u>Other Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EA09	<u>MIO</u>		SS	<u>Other Instructions</u>	390
EA0C	<u>BIFLAG</u>		SS	<u>Other Instructions</u>	390
EA0D	<u>MULDIV</u>		SS	<u>Other Instructions</u>	390
EB04	<u>LMG</u>	Load Multiple Grande	RSY-a	<u>Data Transfer Instructions</u>	Z
EB0A	<u>SRAG</u>	Shift Right single Arith. Grande	RSY-a	<u>Shift and Rotate Instructions</u>	Z
EB0B	<u>SLAG</u>	Shift Left single Arith. Grande	RSY-a	<u>Shift and Rotate Instructions</u>	Z
EB0C	<u>SRLG</u>	Shift Right single Log. Grande	RSY-a	<u>Shift and Rotate Instructions</u>	Z
EB0D	<u>SLLG</u>	Shift Left single Log. Grande	RSY-a	<u>Shift and Rotate Instructions</u>	Z
EB0F	<u>TRACG</u>	TRACe Grande	RSY-a	<u>Privileged Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EB14	<u>CSY</u>	Compare and Swap (32)	RSY-a	<u>Logic Instructions</u>	Z
EB1C	<u>RLLG</u>	Rotate Left single Log. Grande	RSY-a	<u>Shift and Rotate Instructions</u>	Z
EB1D	<u>RLL</u>	Rotate Left single Logical (32)	RSY-a	<u>Shift and Rotate Instructions</u>	Z
EB20	<u>CLMH</u>	Comp. Log. chars under Mask High	RSY-b	<u>Logic Instructions</u>	Z
EB21	<u>CLMY</u>	Comp. Log. chars under Mask Yonder	RSY-b	<u>Logic Instructions</u>	Z
EB23	<u>CLT</u>	Comp. Log. and Trap	RSY-b	<u>Logic Instructions</u>	390
EB23-2	<u>CLTH</u>	Comp. Log. and Trap on High	RSY-b	<u>Logic Instructions</u>	390
EB23-4	<u>CLTL</u>	Comp. Log. and Trap on Low	RSY-b	<u>Logic Instructions</u>	390
EB23-7	<u>CLTNE</u>	Comp. Log. and Trap on Not Equal	RSY-b	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EB23-8	<u>CLTE</u>	Comp. Log. and Trap on Equal	RSY-b	<u>Logic Instructions</u>	390
EB23-B	<u>CLTNL</u>	Comp. Log. and Trap on Not Low	RSY-b	<u>Logic Instructions</u>	390
EB23-D	<u>CLTNH</u>	Comp. Log. and Trap on Not High	RSY-b	<u>Logic Instructions</u>	390
EB24	<u>STMG</u>	Store Multiple Grande	RSY-a	<u>Data Transfer Instructions</u>	Z
EB25	<u>STCTG</u>	STore ConTrol (64)	RSY-a	<u>Privileged Instructions</u>	Z
EB26	<u>STMH</u>	STore Multiple High	RSY-a	<u>Data Transfer Instructions</u>	Z
EB2B	<u>CLT</u>	Comp. Log. and Trap (64)	RSY-b	<u>Logic Instructions</u>	390
EB2C	<u>STCMH</u>	STore Characters under Mask (High)	RSY-b	<u>Data Transfer Instructions</u>	Z
EB2D	<u>STCMY</u>	STore Characters under Mask (Low)	RSY-b	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EB2F	<u>LCTLG</u>	Load Control (64)	RSY-a	<u>Privileged Instructions</u>	Z
EB30	<u>CSG</u>	Compare and Swap (64)	RSY-a	<u>Logic Instructions</u>	Z
EB31	<u>CDSY</u>	Compare Double and Swap (32)	RSY-a	<u>Logic Instructions</u>	Z
EB3E	<u>CDSG</u>	Compare Double and Swap (64)	RSY-a	<u>Logic Instructions</u>	Z
EB44	<u>BXHG</u>	Branch on indeX High (64)	RSY-a	<u>Branch Instructions</u>	Z
EB45	<u>BXLEG</u>	Branch on indeX Low or Equal (64)	RSY-a	<u>Branch Instructions</u>	Z
EB4C	<u>ECAG</u>	Extract CPU Attribute (Extr. Cache Attribute)	RSY-a	<u>Other Instructions</u>	Z
EB51	<u>TMY</u>	Test under Mask	SIY	<u>Logic Instructions</u>	Z
EB52	<u>MVIY</u>	MoVe Immediate	SIY	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EB54	<u>NIY</u>	aNd Immediate	SIY	<u>Data Transfer Instructions</u>	Z
EB55	<u>CLIY</u>	Compare Logical Immediate	SIY	<u>Logic Instructions</u>	Z
EB56	<u>OIY</u>	Or Immediate	SIY	<u>Data Transfer Instructions</u>	Z
EB57	<u>XIY</u>	eXclusive or Immediate	SIY	<u>Data Transfer Instructions</u>	Z
EB6A	<u>ASI</u>	Add Immediate (8/32)	SIY	<u>Arithmetic Instructions</u>	Z
EB6E	<u>ALSI</u>	Add Logical with Signed Immediate (8/32)	SIY	<u>Arithmetic Instructions</u>	Z
EB7A	<u>AGSI</u>	Add Immediate (8/64)	SIY	<u>Arithmetic Instructions</u>	Z
EB7E	<u>ALGSI</u>	Add Logical with Signed Immediate (8/64)	SIY	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EB80	<u>ICMH</u>	Insert Characters under Mask High	RSY-b	<u>Data Transfer Instructions</u>	390
EB81	<u>ICMY</u>	Insert Characters under Mask	RSY-b	<u>Data Transfer Instructions</u>	390
EB8E	<u>MVCLU</u>	MoVe Character Long (Unicode)	RSY-a	<u>Data Transfer Instructions</u>	390
EB8F	<u>CLCLU</u>	Compare Logical Character Long (Unicode)	RSY-a	<u>Logic Instructions</u>	390
EB96	<u>LMH</u>	Load Multiple High	RSY-a	<u>Data Transfer Instructions</u>	390
EB98	<u>LMY</u>	Load Multiple Yonder	RSY-a	<u>Data Transfer Instructions</u>	390
EB9A	<u>LAMY</u>	Load Access Multiple	RSY-a	<u>Data Transfer Instructions</u>	Z
EBC0	<u>TP</u>	Test Packed Decimal	RSL-a	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EBDC	<u>SRAK</u>	Shift Right sing. Arith. Keeping Source data	RSY-a	<u>Data Transfer Instructions</u>	390
EBDD	<u>SLAK</u>	Shift Left sing. Arith. Keeping Source data	RSY-a	<u>Data Transfer Instructions</u>	390
EBDE	<u>SRLK</u>	Shift Right sing. Logical Keeping Source data	RSY-a	<u>Data Transfer Instructions</u>	390
EBDF	<u>SRLK</u>	Shift Left sing. Logical Keeping Source data	RSY-a	<u>Data Transfer Instructions</u>	390
EBE0	<u>LOCFH</u>	Load High on Condition (32)	RSY-b	<u>Other Instructions</u>	Z
EBE1	<u>STOCFH</u>	STore High on Condition	RSY-b	<u>Other Instructions</u>	Z
EBE2	<u>LOCG</u>	LOad on Condition Grande	RSY-b	<u>Data Transfer Instructions</u>	Z
EBE3	<u>STOCG</u>	STore on Condition (64)	RSY-b	<u>Data Transfer Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
E8E4	<u>LANG</u>	Load and aNd (64)	RSY-a	<u>Arithmetic Instructions</u>	Z
E8E6	<u>LAOG</u>	Load and OR (64)	RSY-a	<u>Arithmetic Instructions</u>	Z
E8E7	<u>LAXG</u>	Load and eXclusive or (64)	RSY-a	<u>Arithmetic Instructions</u>	Z
E8E8	<u>LAAG</u>	Load and Add (64)	RSY-a	<u>Arithmetic Instructions</u>	Z
E8EA	<u>LAALG</u>	Load and Add Logical (64)	RSY-a	<u>Arithmetic Instructions</u>	Z
E8F2	<u>LOC</u>	Load on Condition (32)	RSY-b	<u>Data Transfer Instructions</u>	Z
E8F3	<u>STOC</u>	STore on Condition (32)	RSY-b	<u>Data Transfer Instructions</u>	Z
E8F4	<u>LAN</u>	Load and aNd (32)	RSY-a	<u>Arithmetic Instructions</u>	Z
E8F6	<u>LAO</u>	Load and OR (32)	RSY-a	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EBF7	<u>LAX</u>	Load and eXclusive or (32)	RSY-a	<u>Arithmetic Instructions</u>	Z
EBF8	<u>LAA</u>	Load and Add (32)	RSY-a	<u>Arithmetic Instructions</u>	Z
EBFA	<u>LAAL</u>	Load and Add Logical (32)	RSY-a	<u>Arithmetic Instructions</u>	Z
EC42	<u>LOCHI</u>	Load Halfword Immediate on Condition (32<16)	RIE-g	<u>Data Transfer Instructions</u>	Z
EC44	<u>BRXHG</u>	Branch Relative on indeX High	RIE-e	<u>Branch Instructions</u>	Z
EC45	<u>BRXLG</u>	Branch Relative on indeX Low	RIE-e	<u>Branch Instructions</u>	Z
EC46	<u>LOCGHI</u>	Load Halfword Immediate on Condition (64<16)	RIE-g	<u>Data Transfer Instructions</u>	Z
EC4E	<u>LOCHHI</u>	Load Halfword High Immediate on Condition (32<16)	RIE-g	<u>Data Transfer Instructions</u>	Z
EC51	<u>RISBLG</u>	Rotate then Insert Selected Bits Low (64)	RIE-f	<u>Shift and Rotate Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC54	<u>RNSBG</u>	Rotate then aNd Selected Bits	RIE-f	<u>Shift and Rotate Instructions</u>	Z
EC55	<u>RISBG</u>	Rotate then Insert Selected Bits	RIE-f	<u>Shift and Rotate Instructions</u>	Z
EC56	<u>ROSBG</u>	Rotate then Or Selected Bits	RIE-f	<u>Shift and Rotate Instructions</u>	Z
EC57	<u>RXSBG</u>	Rotate then eXclusive OR Selected Bits	RIE-f	<u>Shift and Rotate Instructions</u>	Z
EC59	<u>RISBGN</u>	Rotate then Insert Selected Bits (64)	RIE-f	<u>Other Instructions</u>	Z
EC5D	<u>RISBHG</u>	Rotate then Insert Selected Bits High (64)	RIE-f	<u>Other Instructions</u>	Z
EC64	<u>CGRJ</u>	Compare and Branch Relative (64)	RIE-b	<u>Logic Instructions</u>	Z
EC64-2	<u>CGRJH</u>	Compare and Branch Relative on High (64)	RIE-b	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC64-4	<u>CGRJL</u>	Compare and Branch Relative on Low (64)	RIE-b	<u>Logic Instructions</u>	Z
EC64-7	<u>CGRJNE</u>	Compare and Branch Relative on Not Equal (64)	RIE-b	<u>Logic Instructions</u>	Z
EC64-8	<u>CGRJE</u>	Compare and Branch Relative on Equal (64)	RIE-b	<u>Logic Instructions</u>	Z
EC64-A	<u>CGRJNL</u>	Compare and Branch Relative on Not Low (64)	RIE-b	<u>Logic Instructions</u>	Z
EC64-C	<u>CGRJNH</u>	Compare and Branch Relative on Not High (64)	RIE-b	<u>Logic Instructions</u>	Z
EC65	<u>CLGRJ</u>	Compare Logical and Branch Relative (64)	RIE-b	<u>Logic Instructions</u>	Z
EC65-2	<u>CLGRJH</u>	Compare Logical and Branch Relative on High (64)	RIE-b	<u>Logic Instructions</u>	Z
EC65-4	<u>CLGRJL</u>	Compare Logical and Branch	RIE-b	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
		Relative on Low (64)			
EC65-7	<u>CLGRJNE</u>	Compare Logical and Branch Relative on Not Equal (64)	RIE-b	<u>Logic Instructions</u>	Z
EC65-8	<u>CLGRJE</u>	Compare Logical and Branch Relative on Equal (64)	RIE-b	<u>Logic Instructions</u>	Z
EC65-A	<u>CLGRJNL</u>	Compare Logical and Branch Relative on Not Low (64)	RIE-b	<u>Logic Instructions</u>	Z
EC65-C	<u>CLGRJNH</u>	Compare Logical and Branch Relative on Not High (64)	RIE-b	<u>Logic Instructions</u>	Z
EC70	<u>CGIT</u>	Compare Immediate and Trap (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC70-2	<u>CGITH</u>	Compare Immediate and Trap on High (16/64)	RIE-a	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC70-4	<u>CGITL</u>	Compare Immediate and Trap on Low (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC70-7	<u>CGITNE</u>	Compare Immediate and Trap on Not Equal (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC70-8	<u>CGITE</u>	Compare Immediate and Trap on Equal (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC70-A	<u>CGITNL</u>	Compare Immediate and Trap on Not Low (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC70-C	<u>CGITNH</u>	Compare Immediate and Trap on Not High (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC71	<u>CLGIT</u>	Compare Logical Immediate and Trap (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC71-2	<u>CLGITH</u>	Compare Logical Immediate and Trap on High (16/64)	RIE-a	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC71-4	<u>CLGITL</u>	Compare Logical Immediate and Trap on Low (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC71-7	<u>CLGITNE</u>	Compare Logical Immediate and Trap on Not Equal (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC71-8	<u>CLGITE</u>	Compare Logical Immediate and Trap on Equal (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC71-A	<u>CLGITNL</u>	Compare Logical Immediate and Trap on Not Low (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC71-C	<u>CLGITNH</u>	Compare Logical Immediate and Trap on Not High (16/64)	RIE-a	<u>Logic Instructions</u>	Z
EC72	<u>CIT</u>	Compare Immediate and Trap (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC72-2	<u>CITH</u>	Compare Immediate and Trap on High (16/32)	RIE-a	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC72-4	<u>CITL</u>	Compare Immediate and Trap on Low (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC72-7	<u>CITNE</u>	Compare Immediate and Trap on Not Equal (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC72-8	<u>CITE</u>	Compare Immediate and Trap on Equal (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC72-A	<u>CITNL</u>	Compare Immediate and Trap on Not Low (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC72-C	<u>CITNH</u>	Compare Immediate and Trap on Not High (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC73	<u>CLFIT</u>	Compare Logical Immediate and Trap (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC73-2	<u>CLFITH</u>	Compare Logical Immediate and Trap on High (16/32)	RIE-a	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC73-4	<u>CLFITL</u>	Compare Logical Immediate and Trap on Low (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC73-7	<u>CLFITNE</u>	Compare Logical Immediate and Trap on Not Equal (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC73-8	<u>CLFITE</u>	Compare Logical Immediate and Trap on Equal (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC73-A	<u>CLFITNL</u>	Compare Logical Immediate and Trap on Not Low (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC73-C	<u>CLFITNH</u>	Compare Logical Immediate and Trap on Not High (16/32)	RIE-a	<u>Logic Instructions</u>	Z
EC76	<u>CRJ</u>	Compare and Branch Relative (32)	RIE-b	<u>Logic Instructions</u>	Z
EC76-2	<u>CRJH</u>	Compare and Branch Relative on High (32)	RIE-b	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC76-4	<u>CRJL</u>	Compare and Branch Relative on Low (32)	RIE-b	<u>Logic Instructions</u>	Z
EC76-7	<u>CRJNE</u>	Compare and Branch Relative on Not Equal (32)	RIE-b	<u>Logic Instructions</u>	Z
EC76-8	<u>CRJE</u>	Compare and Branch Relative on Equal (32)	RIE-b	<u>Logic Instructions</u>	Z
EC76-A	<u>CRJNL</u>	Compare and Branch Relative on Not Low (32)	RIE-b	<u>Logic Instructions</u>	Z
EC76-C	<u>CRJNH</u>	Compare and Branch Relative on Not High (32)	RIE-b	<u>Logic Instructions</u>	Z
EC77	<u>CLRJ</u>	Compare Logical and Branch Relative (32)	RIE-b	<u>Logic Instructions</u>	Z
EC77-2	<u>CLRJH</u>	Compare Logical and Branch Relative on High (32)	RIE-b	<u>Logic Instructions</u>	Z
EC77-4	<u>CLRJL</u>	Compare Logical and Branch	RIE-b	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
		Relative on Low (32)			
EC77-7	<u>CLRJNE</u>	Compare Logical and Branch Relative on Not Equal (32)	RIE-b	<u>Logic Instructions</u>	Z
EC77-8	<u>CLRJE</u>	Compare Logical and Branch Relative on Equal (32)	RIE-b	<u>Logic Instructions</u>	Z
EC77-A	<u>CLRJNL</u>	Compare Logical and Branch Relative on Not Low (32)	RIE-b	<u>Logic Instructions</u>	Z
EC77-C	<u>CLRJNH</u>	Compare Logical and Branch Relative on Not High (32)	RIE-b	<u>Logic Instructions</u>	Z
EC7C	<u>CGIJ</u>	Compare Immediate and Branch Relative (8/64)	RIE-c	<u>Logic Instructions</u>	Z
EC7C-2	<u>CGIJH</u>	Compare Immediate and Branch Relative (a High)	RIE-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC7C-4	<u>CGIJL</u>	Compare Immediate and Branch Relative (a Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7C-7	<u>CGIJNE</u>	Compare Immediate and Branch Relative Not Equal	RIE-c	<u>Logic Instructions</u>	Z
EC7C-8	<u>CGIJE</u>	Compare Immediate and Branch Relative (a Equal b)	RIE-c	<u>Logic Instructions</u>	Z
EC7C-A	<u>CGIJNL</u>	Compare Immediate and Branch Relative (a Not Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7C-C	<u>CGIJNH</u>	Compare Immediate and Branch Relative Not High	RIE-c	<u>Logic Instructions</u>	Z
EC7D	<u>CLGIJ</u>	Compare Log.Immed. and Branch Relative (8/64)	RIE-c	<u>Logic Instructions</u>	Z
EC7D-2	<u>CLGIJH</u>	Compare Log.Immed. and	RIE-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
		Branch Relative (a High)			
EC7D-4	<u>CLGIJL</u>	Compare Log.Immed. and Branch Relative (a Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7D-7	<u>CLGIJNE</u>	Compare Log.Immed. and Branch Relative Not Equal	RIE-c	<u>Logic Instructions</u>	Z
EC7D-8	<u>CLGIJE</u>	Compare Log.Immed. and Branch Relative (a Equal b)	RIE-c	<u>Logic Instructions</u>	Z
EC7D-A	<u>CLGIJNL</u>	Compare Log.Immed. and Branch Relative (a Not Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7D-C	<u>CLGIJNH</u>	Compare Log.Immed. and Branch Relative Not High	RIE-c	<u>Logic Instructions</u>	Z
EC7E	<u>CIJ</u>	Compare Immediate and Branch Relative (8/32)	RIE-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EC7E-2	<u>CIJH</u>	Compare Immediate and Branch Relative (a High)	RIE-c	<u>Logic Instructions</u>	Z
EC7E-4	<u>CIJL</u>	Compare Immediate and Branch Relative (a Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7E-7	<u>CIJNE</u>	Compare Immediate and Branch Relative Not Equal	RIE-c	<u>Logic Instructions</u>	Z
EC7E-8	<u>CIJE</u>	Compare Immediate and Branch Relative (a Equal b)	RIE-c	<u>Logic Instructions</u>	Z
EC7E-A	<u>CIJNL</u>	Compare Immediate and Branch Relative (a Not Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7E-C	<u>CIJNH</u>	Compare Immediate and Branch Relative Not High	RIE-c	<u>Logic Instructions</u>	Z
EC7F	<u>CLIJ</u>	Compare Log.Immed. and	RIE-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
		Branch Relative (8/32)			
EC7F-2	<u>CLIJH</u>	Compare Log.Immed. and Branch Relative (a High)	RIE-c	<u>Logic Instructions</u>	Z
EC7F-4	<u>CLIJL</u>	Compare Log.Immed. and Branch Relative (a Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7F-7	<u>CLIJNE</u>	Compare Log.Immed. and Branch Relative Not Equal	RIE-c	<u>Logic Instructions</u>	Z
EC7F-8	<u>CLIKE</u>	Compare Log.Immed. and Branch Relative (a Equal b)	RIE-c	<u>Logic Instructions</u>	Z
EC7F-A	<u>CLIJNL</u>	Compare Log.Immed. and Branch Relative (a Not Low)	RIE-c	<u>Logic Instructions</u>	Z
EC7F-C	<u>CLIJNH</u>	Compare Log.Immed. and Branch Relative Not High	RIE-c	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ECD8	<u>AHIK</u>	Add Immediate (32<16)	RIE-d	<u>Other Instructions</u>	Z
ECD9	<u>AGHIK</u>	Add Immediate (64<16)	RIE-d	<u>Other Instructions</u>	Z
ECDA	<u>ALHSIK</u>	Add Logical with Signed Immediate (32<16)	RIE-d	<u>Other Instructions</u>	Z
ECDB	<u>ALGHSIK</u>	Add Logical with Signed Immediate (64<16)	RIE-d	<u>Other Instructions</u>	Z
ECE4	<u>CGRB</u>	Compare and Branch (64)	RRS	<u>Logic Instructions</u>	390
ECE4-2	<u>CGRBH</u>	Compare and Branch on High (64)	RRS	<u>Logic Instructions</u>	390
ECE4-4	<u>CGRBL</u>	Compare and Branch on Low (64)	RRS	<u>Logic Instructions</u>	390
ECE4-7	<u>CGRBNE</u>	Compare and Branch on Not Equal (64)	RRS	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ECE4-8	<u>CGRBE</u>	Compare and Branch on Equal (64)	RRS	<u>Logic Instructions</u>	390
ECE4-A	<u>CGRBNL</u>	Compare and Branch on Not Low (64)	RRS	<u>Logic Instructions</u>	390
ECE4-C	<u>CGRBNH</u>	Compare and Branch on Not High (64)	RRS	<u>Logic Instructions</u>	390
ECE5	<u>CLGRB</u>	Compare Logical and Branch (64)	RRS	<u>Logic Instructions</u>	390
ECE5-2	<u>CLGRBH</u>	Compare Logical and Branch on High (64)	RRS	<u>Logic Instructions</u>	390
ECE5-4	<u>CLGRBL</u>	Compare Logical and Branch on Low (64)	RRS	<u>Logic Instructions</u>	390
ECE5-7	<u>CLGRBNE</u>	Compare Logical and Branch on Not Equal (64)	RRS	<u>Logic Instructions</u>	390
ECE5-8	<u>CLGRBE</u>	Compare Logical and Branch on Equal (64)	RRS	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ECE5-A	<u>CLGRBNL</u>	Compare Logical and Branch on Not Low (64)	RRS	<u>Logic Instructions</u>	390
ECE5-C	<u>CLGRBNH</u>	Compare Logical and Branch on Not High (64)	RRS	<u>Logic Instructions</u>	390
ECF6	<u>CRB</u>	Compare and Branch (32)	RRS	<u>Logic Instructions</u>	390
ECF6-2	<u>CRBH</u>	Compare and Branch (32) on High	RRS	<u>Logic Instructions</u>	390
ECF6-4	<u>CRBL</u>	Compare and Branch (32) on Low	RRS	<u>Logic Instructions</u>	390
ECF6-7	<u>CRBNE</u>	Compare and Branch (32) on Not Equal	RRS	<u>Logic Instructions</u>	390
ECF6-8	<u>CRBE</u>	Compare and Branch (32) on Equal	RRS	<u>Logic Instructions</u>	390
ECF6-A	<u>CRBNL</u>	Compare and Branch (32) on Not Low	RRS	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ECF6-E	<u>CRBNH</u>	Compare and Branch (32) on Not High	RRS	<u>Logic Instructions</u>	390
ECF7	<u>CLRB</u>	Compare Logical and Branch (32)	RRS	<u>Logic Instructions</u>	390
ECF7-2	<u>CLRBH</u>	Compare Logical and Branch (32) on High	RRS	<u>Logic Instructions</u>	390
ECF7-4	<u>CLRBL</u>	Compare Logical and Branch (32) on Low	RRS	<u>Logic Instructions</u>	390
ECF7-7	<u>CLRBNE</u>	Compare Logical and Branch (32) on Not Equal	RRS	<u>Logic Instructions</u>	390
ECF7-8	<u>CLRBE</u>	Compare Logical and Branch (32) on Equal	RRS	<u>Logic Instructions</u>	390
ECF7-A	<u>CLRBNL</u>	Compare Logical and Branch (32) on Not Low	RRS	<u>Logic Instructions</u>	390
ECF7-C	<u>CLRBNH</u>	Compare Logical and Branch (32) on Not High	RRS	<u>Logic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ECFC	<u>CGIB</u>	Compare Immediate and Branch (8/64)	RIS	<u>Logic Instructions</u>	Z
ECFC-2	<u>CGIBH</u>	Compare Immediate and Branch (a High)	RIS	<u>Logic Instructions</u>	Z
ECFC-4	<u>CGIBL</u>	Compare Immediate and Branch (a Low)	RIS	<u>Logic Instructions</u>	Z
ECFC-7	<u>CGIBNE</u>	Compare Immediate and Branch Not Equal	RIS	<u>Logic Instructions</u>	Z
ECFC-8	<u>CGIBE</u>	Compare Immediate and Branch (a Equal b)	RIS	<u>Logic Instructions</u>	Z
ECFC-A	<u>CGIBNL</u>	Compare Immediate and Branch (a Not Low)	RIS	<u>Logic Instructions</u>	Z
ECFC-C	<u>CGIBNH</u>	Compare Immediate and Branch Not High	RIS	<u>Logic Instructions</u>	Z
ECFE	<u>CIB</u>	Compare Immediate and Branch (8/32)	RIS	<u>Logic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ECFE-2	<u>CIBH</u>	Compare Immediate and Branch (a High)	RIS	<u>Logic Instructions</u>	Z
ECFE-4	<u>CIBL</u>	Compare Immediate and Branch (a Low)	RIS	<u>Logic Instructions</u>	Z
ECFE-7	<u>CIBNE</u>	Compare Immediate and Branch Not Equal	RIS	<u>Logic Instructions</u>	Z
ECFE-8	<u>CIBE</u>	Compare Immediate and Branch (a Equal b)	RIS	<u>Logic Instructions</u>	Z
ECFE-A	<u>CIBNL</u>	Compare Immediate and Branch (a Not Low)	RIS	<u>Logic Instructions</u>	Z
ECFE-C	<u>CIBNH</u>	Compare Immediate and Branch Not High	RIS	<u>Logic Instructions</u>	Z
ED04	<u>LDEB</u>	Load Lengthened (Short/Long)	RXE	<u>Data Transfer Instructions</u>	390
ED05	<u>LXDB</u>	Load Lengthened (Long/Extended)	RXE	<u>Data Transfer Instructions</u>	390

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ED06	<u>LXEB</u>	Load Lengthened (Short/Extended)	RXE	<u>Data Transfer Instructions</u>	390
ED07	<u>MXDB</u>	Multiply (Long/Extended)	RXE	<u>Arithmetic Instructions</u>	390
ED08	<u>KEB</u>	Compare and Sign (Short)	RXE	<u>Logic Instructions</u>	390
ED09	<u>CEB</u>	Compare (Short)	RXE	<u>Logic Instructions</u>	390
ED0A	<u>AEB</u>	Add (Short)	RXE	<u>Arithmetic Instructions</u>	390
ED0B	<u>SEB</u>	Subtract (Short)	RXE	<u>Arithmetic Instructions</u>	390
ED0C	<u>MDEB</u>	Multiply (Short)	RXE	<u>Arithmetic Instructions</u>	390
ED0D	<u>DEB</u>	Divide (Short)	RXE	<u>Arithmetic Instructions</u>	390
ED0E	<u>MAEB</u>	Multiply and Add (Short)	RXF	<u>Arithmetic Instructions</u>	390
ED0F	<u>MSEB</u>	Multiply and Subtract (Short)	RXF	<u>Arithmetic Instructions</u>	390

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Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ED10	<u>TCEB</u>	Test Data Class (Short)	RXE	<u>Logic Instructions</u>	390
ED11	<u>TCDB</u>	Test Data Class (Long)	RXE	<u>Logic Instructions</u>	390
ED12	<u>TCXB</u>	Test Data Class (Extended)	RXE	<u>Logic Instructions</u>	390
ED14	<u>SQEB</u>	Square Root (Short BFP)	RXE	<u>Arithmetic Instructions</u>	390
ED15	<u>SQDB</u>	Square Root (Long BFP)	RXE	<u>Arithmetic Instructions</u>	390
ED17	<u>MEEB</u>	Multiply	RXE	<u>Arithmetic Instructions</u>	390
ED18	<u>KDB</u>	Compare and Sign (Long)	RXE	<u>Logic Instructions</u>	390
ED19	<u>CDB</u>	Compare (Long)	RXE	<u>Logic Instructions</u>	390
ED1A	<u>ADB</u>	Add (Long)	RXE	<u>Arithmetic Instructions</u>	390
ED1B	<u>SDB</u>	Subtract (Long)	RXE	<u>Arithmetic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ED1C	<u>MDB</u>	Multiply (Long)	RXE	<u>Arithmetic Instructions</u>	390
ED1D	<u>DDB</u>	Divide (Long)	RXE	<u>Arithmetic Instructions</u>	390
ED1E	<u>MADB</u>	Multiply and Add (Long)	RXF	<u>Arithmetic Instructions</u>	390
ED1F	<u>MSDB</u>	Multiply and Subtract (Long)	RXF	<u>Arithmetic Instructions</u>	390
ED24	<u>LDE</u>	Load Lengthened (Short/Long)	RXE	<u>Arithmetic Instructions</u>	390
ED25	<u>LXD</u>	Load Lengthened (Long/Extended)	RXE	<u>Arithmetic Instructions</u>	390
ED26	<u>LXE</u>	Load Lengthened (Short/Extended)	RXE	<u>Arithmetic Instructions</u>	390
ED2E	<u>MAE</u>	Multiply and Add (Short)	RXF	<u>Arithmetic Instructions</u>	390
ED2F	<u>MSE</u>	Multiply and Subtract (Short)	RXF	<u>Arithmetic Instructions</u>	390
ED34	<u>SQE</u>	Square Root (Short)	RXE	<u>Arithmetic Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ED35	<u>SQD</u>	Square Root (Long)	RXE	<u>Arithmetic Instructions</u>	390
ED37	<u>MEE</u>	Multiply (Short*Short to Short)	RXE	<u>Arithmetic Instructions</u>	390
ED38	<u>MAYL</u>	Multiply and Add Unnormalized (Long>Ext. Low)	RXF	<u>Arithmetic Instructions</u>	Z
ED39	<u>MYL</u>	Multiply Unnormalized (Long>Ext. Low)	RXF	<u>Arithmetic Instructions</u>	Z
ED3A	<u>MAY</u>	Multiply and Add Unnormalized (Long>Extended)	RXF	<u>Arithmetic Instructions</u>	Z
ED3B	<u>MY</u>	Multiply Unnormalized (Long>Extended)	RXF	<u>Arithmetic Instructions</u>	Z
ED3C	<u>MAYH</u>	Multiply and Add Unnormalized (Long>Ext. High)	RXF	<u>Arithmetic Instructions</u>	Z
ED3D	<u>MYH</u>	Multiply Unnormalized (Long>Ext. High)	RXF	<u>Arithmetic Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ED3E	<u>MAD</u>	Multiply and Add (Long)	RXF	<u>Arithmetic Instructions</u>	390
ED3F	<u>MSD</u>	Multiply and Subtract (Long)	RXF	<u>Arithmetic Instructions</u>	390
ED40	<u>SLDT</u>	Shift Significand Left (Long)	RXF	<u>Shift and Rotate Instructions</u>	390
ED41	<u>SRDT</u>	Shift Significand Right (Long)	RXF	<u>Shift and Rotate Instructions</u>	390
ED48	<u>SLXT</u>	Shift Significand Left (Extended)	RXF	<u>Shift and Rotate Instructions</u>	390
ED49	<u>SRXT</u>	Shift Significand Right (Extended)	RXF	<u>Shift and Rotate Instructions</u>	390
ED50	<u>TDCET</u>	Test Data Class (short DFP)	RXE	<u>Other Instructions</u>	Z
ED51	<u>TDGET</u>	Test Data Group (short DFP)	RXE	<u>Other Instructions</u>	Z
ED54	<u>TDCDT</u>	Test Data Class (long DFP)	RXE	<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
ED55	<u>TDGDT</u>	Test Data Group (long DFP)	RXE	<u>Other Instructions</u>	Z
ED58	<u>TDCXT</u>	Test Data Class (extended DFP)	RXE	<u>Other Instructions</u>	Z
ED59	<u>TDGXT</u>	Test Data Group (extended DFP)	RXE	<u>Other Instructions</u>	Z
ED64	<u>LEY</u>	Load	RXY-a	<u>Data Transfer Instructions</u>	390
ED65	<u>LDY</u>	Load Double	RXY-a	<u>Data Transfer Instructions</u>	390
ED66	<u>STEY</u>	Store	RXY-a	<u>Data Transfer Instructions</u>	390
ED67	<u>STDY</u>	Store Double	RXY-a	<u>Data Transfer Instructions</u>	390
EDA8	<u>CZDT</u>	Convert to Zoned (Long/Zoned)	RSL-b	<u>Other Instructions</u>	390
EDA9	<u>CZXT</u>	Convert to Zoned (Extended/Zoned)	RSL-b	<u>Other Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
EDAA	<u>CDZT</u>	Convert from Zoned (Zoned/Long)	RSL-b	<u>Other Instructions</u>	390
EDAB	<u>CXZT</u>	Convert from Zoned (Zoned/Extended)	RSL-b	<u>Other Instructions</u>	390
EDAC	<u>CPDT</u>	Convert to PACKED (from long DFP)	RSL-b	<u>Other Instructions</u>	Z
EDAD	<u>CPXT</u>	Convert to PACKED (from extended DFP)	RSL-b	<u>Other Instructions</u>	Z
EDAE	<u>CDPT</u>	Convert from PACKED (to long DFP)	RSL-b	<u>Other Instructions</u>	Z
EDAF	<u>CXPT</u>	Convert from PACKED (to extended DFP)	RSL-b	<u>Other Instructions</u>	Z
EE	<u>PLO</u>	Perform Locked Operation	SS-e	<u>Data Transfer Instructions</u>	390
EF	<u>LMD</u>	Load Multiple Disjoint	SS-e	<u>Data Transfer Instructions</u>	390

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
F0	<u>SRP</u>	Shift and Round Packed	SS-c	<u>Shift and Rotate Instructions</u>	360
F1	<u>MVO</u>	Move with Offset	SS-b	<u>Data Transfer Instructions</u>	360
F2	<u>PACK</u>	PACK	SS-b	<u>Arithmetic Instructions</u>	360
F3	<u>UNPK</u>	UNPack	SS-b	<u>Arithmetic Instructions</u>	360
F8	<u>ZAP</u>	Zero and Add Packed	SS-b	<u>Arithmetic Instructions</u>	360
F9	<u>CP</u>	Compare Packed	SS-b	<u>Logic Instructions</u>	360
FA	<u>AP</u>	Add Packed	SS-b	<u>Arithmetic Instructions</u>	360
FB	<u>SP</u>	Subtract Packed	SS-b	<u>Arithmetic Instructions</u>	360
FC	<u>MP</u>	Multiply Packed	SS-b	<u>Arithmetic Instructions</u>	360

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
FD	<u>DP</u>	Divide Packed	SS-b	Arithmetic Instructions	360
	<u>LBEAR</u>			Other Instructions	Z
	<u>LFI</u>			Other Instructions	Z
	<u>LLGFI</u>			Other Instructions	Z
	<u>LPSWEY</u>			Other Instructions	Z
	<u>NNPA</u>			Other Instructions	Z
	<u>QPACI</u>			Other Instructions	Z
	<u>RDP</u>			Other Instructions	Z
	<u>SLLHH</u>			Other Instructions	Z
	<u>SLLHL</u>			Other Instructions	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
	<u>SLLLH</u>			<u>Other Instructions</u>	Z
	<u>SRLHH</u>			<u>Other Instructions</u>	Z
	<u>SRLHL</u>			<u>Other Instructions</u>	Z
	<u>SRLLH</u>			<u>Other Instructions</u>	Z
	<u>STBEAR</u>			<u>Other Instructions</u>	Z
	<u>VCFN</u>			<u>Other Instructions</u>	Z
	<u>VCLFNH</u>			<u>Other Instructions</u>	Z
	<u>VCLFNL</u>			<u>Other Instructions</u>	Z
	<u>VCLZDP</u>			<u>Other Instructions</u>	Z
	<u>VCNF</u>			<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemonic	Description	Instruction Format	Instruction Class	Instruction Set Architecture
	<u>VCRNF</u>			<u>Other Instructions</u>	Z
	<u>VCSPH</u>			<u>Other Instructions</u>	Z
	<u>VPKZR</u>			<u>Other Instructions</u>	Z
	<u>VSCHDP</u>			<u>Other Instructions</u>	Z
	<u>VSCHP</u>			<u>Other Instructions</u>	Z
	<u>VSCHSP</u>			<u>Other Instructions</u>	Z
	<u>VSCHXP</u>			<u>Other Instructions</u>	Z
	<u>VSCSHP</u>			<u>Other Instructions</u>	Z
	<u>VSRPR</u>			<u>Other Instructions</u>	Z
	<u>VUPKZH</u>			<u>Other Instructions</u>	Z

Opco de (Hex)	Mnemon ic	Description	Instructi on Format	Instructio n Class	Instructio n Set Architect ure
	<u>VUPKZL</u>			<u>Other Instructions</u>	Z