



PIC18 CONFIGURATION SETTINGS ADDENDUM

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Configuration Settings

This addendum lists the configuration settings available for each of the PIC18 devices for use with MPLAB® C18's `#pragma config` directive and MPASM™ assembler's `CONFIG` directive.

PIC18C242

Code Protect:

CP = ON	Enabled
CP = OFF	Disabled

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18C252

Code Protect:

CP = ON	Enabled
CP = OFF	Disabled

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18C442

Code Protect:

CP = ON	Enabled
CP = OFF	Disabled

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18C452

Code Protect:

CP = ON	Enabled
CP = OFF	Disabled

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18C601**Oscillator Selection:**

OSC = LP	LP Oscillator
OSC = EC	EC Oscillator
OSC = HS	HS Oscillator
OSC = RC	RC Oscillator

Power-up Timer:

PWRT = ON	Enable
PWRT = OFF	Disable

External Bus Data Width:

BW = 8	8-bit External Bus mode
BW = 16	16-bit External Bus mode

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Timer Postscale Selection:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Full/Underflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18C658

Code Protect:

CP = ON	Enabled
CP = OFF	Disabled

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18C801

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = EC	EC Oscillator
OSC = HS	HS Oscillator
OSC = RC	RC Oscillator

Power-up Timer:

PWRT = ON	Enable
PWRT = OFF	Disable

External Bus Data Width:

BW = 8	8-bit External Bus mode
BW = 16	16-bit External Bus mode

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Timer Postscale Selection:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Full/Underflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18C858

Code Protect:

CP = ON	Enabled
CP = OFF	Disabled

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

PIC18F1220

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Full/Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F1230

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

FLTA MUX Bit:

FLTAMX = RA7	Multiplexed with RA7
FLTAMX = RA5	Multiplexed with RA5

T1OSC MUX bit:

T1OSCMX = LOW	T1OSC pins reside on RB2 and RB3
T1OSCMX = HIGH	T1OSC pins reside on RA6 and RA7

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Overflow Reset Enable Bit:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Dedicated In-Circuit Port Enable Bit:

ENICPORT = OFF	Disabled
ENICPORT = ON	Enabled

Boot Block Size Select Bits:

BBSIZ = BB256	256 W Boot Block Size
BBSIZ = BB512	512 W Boot Block Size

Extended Instruction Set Enable bit:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F1231**Oscillator Selection:**

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

FLTA MUX Bit:

FLTAMX = RA7	Multiplexed with RA7
FLTAMX = RA5	Multiplexed with RA5

T1OSC MUX bit:

T1OSCMX = LOW	T1OSC pins reside on RB2 and RB3
T1OSCMX = HIGH	T1OSC pins reside on RA6 and RA7

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Overflow Reset Enable Bit:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Dedicated In-Circuit Port Enable Bit:

ENICPORT = OFF	Disabled
ENICPORT = ON	Enabled

Boot Block Size Select Bits:

BBSIZ = BB256	256 W Boot Block Size
BBSIZ = BB512	512 W Boot Block Size

Extended Instruction Set Enable bit:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F1320

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Full/Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F1330

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

FLTA MUX Bit:

FLTAMX = RA7	Multiplexed with RA7
FLTAMX = RA5	Multiplexed with RA5

T1OSC MUX bit:

T1OSCMX = LOW	T1OSC pins reside on RB2 and RB3
T1OSCMX = HIGH	T1OSC pins reside on RA6 and RA7

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Overflow Reset Enable Bit:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Dedicated In-Circuit Port Enable Bit:

ENICPORT = OFF	Disabled
ENICPORT = ON	Enabled

Boot Block Size Select Bits:

BBSIZ = BB256	256 W Boot Block Size
BBSIZ = BB512	512 W Boot Block Size
BBSIZ = BB1K	1 KW Boot Block Size

Extended Instruction Set Enable bit:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F1331

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

FLTA MUX Bit:

FLTAMX = RA7	Multiplexed with RA7
FLTAMX = RA5	Multiplexed with RA5

T1OSC MUX bit:

T1OSCMX = LOW	T1OSC pins reside on RB2 and RB3
T1OSCMX = HIGH	T1OSC pins reside on RA6 and RA7

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Overflow Reset Enable Bit:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Dedicated In-Circuit Port Enable Bit:

ENICPORT = OFF	Disabled
ENICPORT = ON	Enabled

Boot Block Size Select Bits:

BBSIZ = BB256	256 W Boot Block Size
BBSIZ = BB512	512 W Boot Block Size
BBSIZ = BB1K	1 KW Boot Block Size

Extended Instruction Set Enable bit:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2220

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

PORTB A/D Enable:

PBAD = DIG	Digital
PBAD = ANA	Analog

CCP2 Pin Function:

CCP2MX = B3	RB3
CCP2MX = OFF	RB3
CCP2MX = C1	RC1
CCP2MX = ON	RC1

Stack Full/Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2221

Oscillator Selection bits:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO2	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO1	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = DIG	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ANA	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = RB3	CCP2 input/output is multiplexed with RB3
CCP2MX = RC1	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB256	256 Word
BBSIZ = BB512	512 Word

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 code-protected
CP0 = OFF	Block 0 not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 code-protected
CP1 = OFF	Block 1 not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block code-protected
CPB = OFF	Boot block not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 write-protected
WRT0 = OFF	Block 0 not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 write-protected
WRT1 = OFF	Block 1 not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block write-protected
WRTB = OFF	Boot block not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block protected from table reads executed in other blocks
EBTRB = OFF	Boot block not protected from table reads executed in other blocks

PIC18F2320

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

PORTB A/D Enable:

PBAD = DIG	Digital
PBAD = ANA	Analog

CCP2 Pin Function:

CCP2MX = B3	RB3
CCP2MX = OFF	RB3
CCP2MX = C1	RC1
CCP2MX = ON	RC1

Stack Full/Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2321

Oscillator Selection bits:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO2	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO1	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = DIG	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ANA	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = RB3	CCP2 input/output is multiplexed with RB3
CCP2MX = RC1	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB256	256 Word
BBSIZ = BB512	512 Word
BBSIZ = BB1K	1024 Word

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 code-protected
CP0 = OFF	Block 0 not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 code-protected
CP1 = OFF	Block 1 not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block code-protected
CPB = OFF	Boot block not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 write-protected
WRT0 = OFF	Block 0 not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 write-protected
WRT1 = OFF	Block 1 not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block write-protected
WRTB = OFF	Boot block not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block protected from table reads executed in other blocks
EBTRB = OFF	Boot block not protected from table reads executed in other blocks

PIC18F2331**Oscillator Selection:**

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC2	External RC, RA6 is CLKOUT
OSC = EC	EC, RA6 is CLKOUT
OSC = ECIO	EC, RA6 is I/O
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	External RC, RA6 is I/O
OSC = IRCIO	Internal RC, RA6 & RA7 are I/O
OSC = IRC	Internal RC, RA6 is CLKOUT, RA7 is I/O
OSC = RC1	External RC, RA6 is CLKOUT
OSC = RC	External RC, RA6 is CLKOUT

Fail-Safe Clock Monitor Enable:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch-Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRTEN = ON	Enabled
PWRTEN = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDTEN = OFF	Disabled
WDTEN = ON	Enabled

Watchdog Timer Enable Window:

WINEN = ON	Enabled
WINEN = OFF	Disabled

Watchdog Postscaler:

WDPS = 1	1:1
WDPS = 2	1:2
WDPS = 4	1:4
WDPS = 8	1:8
WDPS = 16	1:16
WDPS = 32	1:32
WDPS = 64	1:64
WDPS = 128	1:128
WDPS = 256	1:256
WDPS = 512	1:512
WDPS = 1024	1:1024
WDPS = 2048	1:2048
WDPS = 4096	1:4096
WDPS = 8192	1:8192
WDPS = 16384	1:16384
WDPS = 32768	1:32768

Timer1 Oscillator MUX:

T1OSCMX = OFF	Active
T1OSCMX = ON	Inactive

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2410**Oscillator Selection bits:**

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks

PIC18F242

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2420

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F2423

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTB	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFh) write-protected
WRTB = OFF	Boot block (000000-0007FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F2431

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC2	External RC, RA6 is CLKOUT
OSC = EC	EC, RA6 is CLKOUT
OSC = ECIO	EC, RA6 is I/O
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	External RC, RA6 is I/O
OSC = IRCIO	Internal RC, RA6 & RA7 are I/O
OSC = IRC	Internal RC, RA6 is CLKOUT, RA7 is I/O
OSC = RC1	External RC, RA6 is CLKOUT
OSC = RC	External RC, RA6 is CLKOUT

Fail-Safe Clock Monitor Enable:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch-Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRTEN = ON	Enabled
PWRTEN = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDTEN = OFF	Disabled
WDTEN = ON	Enabled

Watchdog Timer Enable Window:

WINEN = ON	Enabled
WINEN = OFF	Disabled

Watchdog Postscaler:

WDPS = 1	1:1
WDPS = 2	1:2
WDPS = 4	1:4
WDPS = 8	1:8
WDPS = 16	1:16
WDPS = 32	1:32
WDPS = 64	1:64
WDPS = 128	1:128
WDPS = 256	1:256
WDPS = 512	1:512
WDPS = 1024	1:1024
WDPS = 2048	1:2048
WDPS = 4096	1:4096
WDPS = 8192	1:8192
WDPS = 16384	1:16384
WDPS = 32768	1:32768

Timer1 Oscillator MUX:

T1OSCMX = OFF	Active
T1OSCMX = ON	Inactive

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2439

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2450

96 MHz PLL Prescaler:

PLLDIV = 1	No divide (4 MHz input)
PLLDIV = 2	Divide by 2 (8 MHz input)
PLLDIV = 3	Divide by 3 (12 MHz input)
PLLDIV = 4	Divide by 4 (16 MHz input)
PLLDIV = 5	Divide by 5 (20 MHz input)
PLLDIV = 6	Divide by 6 (24 MHz input)
PLLDIV = 10	Divide by 10 (40 MHz input)
PLLDIV = 12	Divide by 12 (48 MHz input)

CPU System Clock Postscaler:

CPUDIV = OSC1_PLL2	[OSC1/OSC2 Src: /1][96 MHz PLL Src: /2]
CPUDIV = OSC2_PLL3	[OSC1/OSC2 Src: /2][96 MHz PLL Src: /3]
CPUDIV = OSC3_PLL4	[OSC1/OSC2 Src: /3][96 MHz PLL Src: /4]
CPUDIV = OSC4_PLL6	[OSC1/OSC2 Src: /4][96 MHz PLL Src: /6]

Full-Speed USB Clock Source Selection:

USBDIV = 1	Clock source from OSC1/OSC2
USBDIV = 2	Clock source from 96 MHz PLL/2

Oscillator Selection bits:

FOSC = XT_XT	XT oscillator, XT used by USB
FOSC = XTPLL_XT	XT oscillator, PLL enabled, XT used by USB
FOSC = ECIO_EC	External clock, port function on RA6, EC used by USB
FOSC = EC_EC	External clock, CLKOUT on RA6, EC used by USB
FOSC = ECPLLIO_EC	External clock, PLL enabled, port function on RA6, EC used by USB
FOSC = ECPLL_EC	External clock, PLL enabled, CLKOUT on RA6, EC used by USB
FOSC = INTOSCIO_EC	Internal oscillator, port function on RA6, EC used by USB
FOSC = INTOSC_EC	Internal oscillator, CLKOUT on RA6, EC used by USB
FOSC = INTOSC_XT	Internal oscillator, XT used by USB
FOSC = INTOSC_HS	Internal oscillator, HS used by USB
FOSC = HS	HS oscillator, HS used by USB
FOSC = HSPLL_HS	HS oscillator, PLL enabled, HS used by USB

Fail-Safe Clock Monitor:

FCMEM = OFF	Disabled
FCMEM = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SOFT	Controlled by SBOREN
BOR = ON_ACTIVE	Enabled when the device is not in Sleep, SBOREN bit is disabled
BOR = ON	Enabled, SBOREN bit is disabled

Brown-out Voltage:

BORV = 46	4.6V
BORV = 43	4.3V
BORV = 28	2.8V
BORV = 21	2.1V

USB Voltage Regulator Enable:

VREGEN = OFF	Disabled
VREGEN = ON	Enabled

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator Enable:

LPT1OSC = OFF	Timer1 oscillator configured for high power
LPT1OSC = ON	Timer1 oscillator configured for low power

PORTB A/D Enable:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input on Reset

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Boot Block Size Select Bit:

BBSIZ = BB2K	2KW Boot Block Size
BBSIZ = BB1K	1KW Boot Block Size

Dedicated In-Circuit Debug/Programming Enable:

ICPRT = OFF	Disabled
ICPRT = ON	Enabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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PLL Prescaler Selection bits:

PLLDIV = 1	No prescale (4 MHz oscillator input drives PLL directly)
PLLDIV = 2	Divide by 2 (8 MHz oscillator input)
PLLDIV = 3	Divide by 3 (12 MHz oscillator input)
PLLDIV = 4	Divide by 4 (16 MHz oscillator input)
PLLDIV = 5	Divide by 5 (20 MHz oscillator input)
PLLDIV = 6	Divide by 6 (24 MHz oscillator input)
PLLDIV = 10	Divide by 10 (40 MHz oscillator input)
PLLDIV = 12	Divide by 12 (48 MHz oscillator input)

CPU System Clock Postscaler:

CPUDIV = OSC1_PLL2	[OSC1/OSC2 Src: /1][96 MHz PLL Src: /2]
CPUDIV = OSC2_PLL3	[OSC1/OSC2 Src: /2][96 MHz PLL Src: /3]
CPUDIV = OSC3_PLL4	[OSC1/OSC2 Src: /3][96 MHz PLL Src: /4]
CPUDIV = OSC4_PLL6	[OSC1/OSC2 Src: /4][96 MHz PLL Src: /6]

USB Clock Selection bit (used in Full Speed USB mode only; UCFG:FSEN = 1):

USBDIV = 1	USB clock source comes directly from the primary oscillator block with no postscale
USBDIV = 2	USB clock source comes from the 96 MHz PLL divided by 2

Oscillator Selection bits:

FOSC = XT_XT	XT oscillator, XT used by USB
FOSC = XTPLL_XT	XT oscillator, PLL enabled, XT used by USB
FOSC = ECIO_EC	External clock, port function on RA6, EC used by USB
FOSC = EC_EC	External clock, CLKOUT on RA6, EC used by USB
FOSC = ECPLLIO_EC	External clock, PLL enabled, port function on RA6, EC used by USB
FOSC = ECPLL_EC	External clock, PLL enabled, CLKOUT on RA6, EC used by USB
FOSC = INTOSCIO_EC	Internal oscillator, port function on RA6, EC used by USB
FOSC = INTOSC_EC	Internal oscillator, CLKOUT on RA6, EC used by USB
FOSC = INTOSC_XT	Internal oscillator, XT used by USB
FOSC = INTOSC_HS	Internal oscillator, HS used by USB
FOSC = HS	HS oscillator, HS used by USB
FOSC = HSPLL_HS	HS oscillator, PLL enabled, HS used by USB

Fail-Safe Clock Monitor Enable bit:

FCMEM = OFF	Fail-Safe Clock Monitor disabled
FCMEM = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = ON_ACTIVE	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

USB Voltage Regulator Enable bit:

VREGEN = OFF	USB voltage regulator disabled
VREGEN = ON	USB voltage regulator enabled

Watchdog Timer Enable bit:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RB3
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFh) code-protected
CPB = OFF	Boot block (000000-0007FFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Configuration registers (300000-3000FFh) write-protected
WRTB = OFF	Configuration registers (300000-3000FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Boot block (000000-0007FFh) write-protected
WRTC = OFF	Boot block (000000-0007FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F248

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2480

Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLKO function on OSC2

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

CCP2 MUX bit:

CCP2MX = ALTERNATE	CCP2 is multiplexed with RB3
CCP2MX = DEFAULT	CCP2 is multiplexed with RC1

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFh) code-protected
CPB = OFF	Boot block (000000-0007FFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFh) write-protected
WRTB = OFF	Boot block (000000-0007FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-003FFFh) code-protected
CP0 = OFF	Block 0 (000800-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks

PIC18F252

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTB	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F2525

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO6	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO6	RC-OSC2 as RA6
OSC = INTIO67	INTRC-OSC2 as RA6, OSC1 as RA7
OSC = INTIO7	INTRC-OSC2 as Clock Out, OSC1 as RA7

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	SBOREN Enabled
BOREN = NOSLP	Enabled except Sleep, SBOREN Disabled
BOREN = SBORDIS	Enabled, SBOREN Disabled

Brown-out Voltage:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

T1 Oscillator Enable:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

PORTB A/D Enable:

PBADEN = OFF	PORTB<4:0> digital on Reset
PBADEN = ON	PORTB<4:0> analog on Reset

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

XINST Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2539

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2550

PLL Prescaler Selection bits:

PLLDIV = 1	No prescale (4 MHz oscillator input drives PLL directly)
PLLDIV = 2	Divide by 2 (8 MHz oscillator input)
PLLDIV = 3	Divide by 3 (12 MHz oscillator input)
PLLDIV = 4	Divide by 4 (16 MHz oscillator input)
PLLDIV = 5	Divide by 5 (20 MHz oscillator input)
PLLDIV = 6	Divide by 6 (24 MHz oscillator input)
PLLDIV = 10	Divide by 10 (40 MHz oscillator input)
PLLDIV = 12	Divide by 12 (48 MHz oscillator input)

CPU System Clock Postscaler:

CPUDIV = OSC1_PLL2	[OSC1/OSC2 Src: /1][96 MHz PLL Src: /2]
CPUDIV = OSC2_PLL3	[OSC1/OSC2 Src: /2][96 MHz PLL Src: /3]
CPUDIV = OSC3_PLL4	[OSC1/OSC2 Src: /3][96 MHz PLL Src: /4]
CPUDIV = OSC4_PLL6	[OSC1/OSC2 Src: /4][96 MHz PLL Src: /6]

USB Clock Selection bit (used in Full Speed USB mode only; UCFG:FSEN = 1):

USBDIV = 1	USB clock source comes directly from the primary oscillator block with no postscale
USBDIV = 2	USB clock source comes from the 96 MHz PLL divided by 2

Oscillator Selection bits:

FOSC = XT_XT	XT oscillator, XT used by USB
FOSC = XTPLL_XT	XT oscillator, PLL enabled, XT used by USB
FOSC = ECIO_EC	External clock, port function on RA6, EC used by USB
FOSC = EC_EC	External clock, CLKOUT on RA6, EC used by USB
FOSC = ECPLLIO_EC	External clock, PLL enabled, port function on RA6, EC used by USB
FOSC = ECPLL_EC	External clock, PLL enabled, CLKOUT on RA6, EC used by USB
FOSC = INTOSCIO_EC	Internal oscillator, port function on RA6, EC used by USB
FOSC = INTOSC_EC	Internal oscillator, CLKOUT on RA6, EC used by USB
FOSC = INTOSC_XT	Internal oscillator, XT used by USB
FOSC = INTOSC_HS	Internal oscillator, HS used by USB
FOSC = HS	HS oscillator, HS used by USB
FOSC = HSPLL_HS	HS oscillator, PLL enabled, HS used by USB

Fail-Safe Clock Monitor Enable bit:

FCMEM = OFF	Fail-Safe Clock Monitor disabled
FCMEM = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = ON_ACTIVE	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

USB Voltage Regulator Enable bit:

VREGEN = OFF	USB voltage regulator disabled
VREGEN = ON	USB voltage regulator enabled

Watchdog Timer Enable bit:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RB3
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Configuration registers (300000-3000FFh) write-protected
WRTB = OFF	Configuration registers (300000-3000FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Boot block (000000-0007FFh) write-protected
WRTC = OFF	Boot block (000000-0007FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks

PIC18F258

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2580

Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F2585**Oscillator Selection bits:**

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block
BBSIZ = 4096	4K words (8K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSC-CON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLKO function on OSC2

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

CCP2 MUX bit:

CCP2MX = ALTERNATE	CCP2 is multiplexed with RB3
CCP2MX = DEFAULT	CCP2 is multiplexed with RC1

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Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO6	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO6	RC-OSC2 as RA6
OSC = INTIO67	INTRC-OSC2 as RA6, OSC1 as RA7
OSC = INTIO7	INTRC-OSC2 as Clock Out, OSC1 as RA7

Fail Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power Up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown Out Reset:

BOREN = OFF	Disabled
BOREN = ON	SBOREN Enabled
BOREN = NOSLP	Enabled except SLEEP, SBOREN Disabled
BOREN = SBORDIS	Enabled, SBOREN Disabled

Brown Out Voltage:

BORV = 46	3.0V
BORV = 43	2.7V
BORV = 28	2.2V
BORV = 21	1.8

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

T1 Oscillator Enable:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

Port B A/D Enable:

PBADEN = OFF	Port B<4:0> digital on RESET
PBADEN = ON	Port B<4:0> analog on RESET

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

XINST Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-003FFFh) code-protected
CP0 = OFF	Block 0 (000800-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFh) code-protected
CPB = OFF	Boot block (000000-0007FFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFh) write-protected
WRTB = OFF	Boot block (000000-0007FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

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Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO6	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO6	RC-OSC2 as RA6
OSC = INTIO67	INTRC-OSC2 as RA6, OSC1 as RA7
OSC = INTIO7	INTRC-OSC2 as Clock Out, OSC1 as RA7

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	SBOREN Enabled
BOREN = NOSLP	Enabled except Sleep, SBOREN Disabled
BOREN = SBORDIS	Enabled, SBOREN Disabled

Brown-out Voltage:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

T1 Oscillator Enable:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

PORTB A/D Enable:

PBADEN = OFF	PORTB<4:0> digital on Reset
PBADEN = ON	PORTB<4:0> analog on Reset

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

XINST Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block
BBSIZ = 4096	4K words (8K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = SBORENCTRL	Controlled by SBOREN
BOREN = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOREN = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block
BBSIZ = 4096	4K words (8K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Code Protection Block 4:

CP4 = ON	Enabled
CP4 = OFF	Disabled

Code Protection Block 5:

CP5 = ON	Enabled
CP5 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Write Protection Block 4:

WRT4 = ON	Enabled
WRT4 = OFF	Disabled

Write Protection Block 5:

WRT5 = ON	Enabled
WRT5 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Table Read Protection Block 4:

EBTR4 = ON	Enabled
EBTR4 = OFF	Disabled

Table Read Protection Block 5:

EBTR5 = ON	Enabled
EBTR5 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4220

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

PORTB A/D Enable:

PBAD = DIG	Digital
PBAD = ANA	Analog

CCP2 Pin Function:

CCP2MX = B3	RB3
CCP2MX = OFF	RB3
CCP2MX = C1	RC1
CCP2MX = ON	RC1

Stack Full/Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4221

Oscillator Selection bits:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO2	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO1	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = DIG	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ANA	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = RB3	CCP2 input/output is multiplexed with RB3
CCP2MX = RC1	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Dedicated In-Circuit Debug/Programming Port (ICPORT) Enable bit:

ICPORT = OFF	ICPORT disabled
ICPORT = ON	ICPORT enabled

Boot Block Size Select bits:

BBSIZ = BB256	256 Word
BBSIZ = BB512	512 Word

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 code-protected
CP0 = OFF	Block 0 not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 code-protected
CP1 = OFF	Block 1 not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block code-protected
CPB = OFF	Boot block not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 write-protected
WRT0 = OFF	Block 0 not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 write-protected
WRT1 = OFF	Block 1 not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block write-protected
WRTB = OFF	Boot block not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block protected from table reads executed in other blocks
EBTRB = OFF	Boot block not protected from table reads executed in other blocks

PIC18F4320

Oscillator Selection:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = EC	External Clock on OSC1, OSC2 as FOSC/4
OSC = ECIO	External Clock on OSC1, OSC2 as RA6
OSC = HSPLL	HS + PLL
OSC = RCIO	External RC on OSC1, OSC2 as RA6
OSC = INTIO2	Internal RC, OSC1 as RA7, OSC2 as RA6
OSC = INTIO1	Internal RC, OSC1 as RA7, OSC2 as FOSC/4
OSC = RC	External RC on OSC1, OSC2 as FOSC/4

Fail-Safe Clock Monitor:

FSCM = OFF	Fail-Safe Clock Monitor disabled
FSCM = ON	Fail-Safe Clock Monitor enabled

Internal External Switch Over mode:

IESO = OFF	Internal External Switch Over mode disabled
IESO = ON	Internal External Switch Over mode enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

PORTB A/D Enable:

PBAD = DIG	Digital
PBAD = ANA	Analog

CCP2 Pin Function:

CCP2MX = B3	RB3
CCP2MX = OFF	RB3
CCP2MX = C1	RC1
CCP2MX = ON	RC1

Stack Full/Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4321

Oscillator Selection bits:

OSC = LP	LP Oscillator
OSC = XT	XT Oscillator
OSC = HS	HS Oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO2	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO1	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = DIG	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ANA	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = RB3	CCP2 input/output is multiplexed with RB3
CCP2MX = RC1	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Dedicated In-Circuit Debug/Programming Port (ICPORT) Enable bit:

ICPORT = OFF	ICPORT disabled
ICPORT = ON	ICPORT enabled

Boot Block Size Select bits:

BBSIZ = BB256	256 Word
BBSIZ = BB512	512 Word
BBSIZ = BB1K	1024 Word

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 code-protected
CP0 = OFF	Block 0 not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 code-protected
CP1 = OFF	Block 1 not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block code-protected
CPB = OFF	Boot block not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 write-protected
WRT0 = OFF	Block 0 not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 write-protected
WRT1 = OFF	Block 1 not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block write-protected
WRTB = OFF	Boot block not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block protected from table reads executed in other blocks
EBTRB = OFF	Boot block not protected from table reads executed in other blocks

PIC18F4331

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC2	External RC, RA6 is CLKOUT
OSC = EC	EC, RA6 is CLKOUT
OSC = ECIO	EC, RA6 is I/O
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	External RC, RA6 is I/O
OSC = IRCIO	Internal RC, RA6 & RA7 are I/O
OSC = IRC	Internal RC, RA6 is CLKOUT, RA7 is I/O
OSC = RC1	External RC, RA6 is CLKOUT
OSC = RC	External RC, RA6 is CLKOUT

Fail-Safe Clock Monitor Enable:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch-Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRTEN = ON	Enabled
PWRTEN = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDTEN = OFF	Disabled
WDTEN = ON	Enabled

Watchdog Timer Enable Window:

WINEN = ON	Enabled
WINEN = OFF	Disabled

Watchdog Postscaler:

WDPS = 1	1:1
WDPS = 2	1:2
WDPS = 4	1:4
WDPS = 8	1:8
WDPS = 16	1:16
WDPS = 32	1:32
WDPS = 64	1:64
WDPS = 128	1:128
WDPS = 256	1:256
WDPS = 512	1:512
WDPS = 1024	1:1024
WDPS = 2048	1:2048
WDPS = 4096	1:4096
WDPS = 8192	1:8192
WDPS = 16384	1:16384
WDPS = 32768	1:32768

Timer1 Oscillator MUX:

T1OSCMX = OFF	Active
T1OSCMX = ON	Inactive

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

External clock MUX bit:

EXCLKMX = RD0	Multiplexed with RD0
EXCLKMX = RC3	Multiplexed with RC3

PWM4 MUX bit:

PWM4MX = RD5	Multiplexed with RD5
PWM4MX = RB5	Multiplexed with RB5

SSP I/O MUX bit:

SSPMX = RD1	SDO output is multiplexed with RD1
SSPMX = RC7	SDO output is multiplexed with RC7

FLTA MUX bit:

FLTAMX = RD4	Multiplexed with RD4
FLTAMX = RC1	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4410

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks

PIC18F442

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4420**Oscillator Selection bits:**

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F4423

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTB	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFh) write-protected
WRTB = OFF	Boot block (000000-0007FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F4431

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC2	External RC, RA6 is CLKOUT
OSC = EC	EC, RA6 is CLKOUT
OSC = ECIO	EC, RA6 is I/O
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	External RC, RA6 is I/O
OSC = IRCIO	Internal RC, RA6 & RA7 are I/O
OSC = IRC	Internal RC, RA6 is CLKOUT, RA7 is I/O
OSC = RC1	External RC, RA6 is CLKOUT
OSC = RC	External RC, RA6 is CLKOUT

Fail-Safe Clock Monitor Enable:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch-Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRTEN = ON	Enabled
PWRTEN = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDTEN = OFF	Disabled
WDTEN = ON	Enabled

Watchdog Timer Enable Window:

WINEN = ON	Enabled
WINEN = OFF	Disabled

Watchdog Postscaler:

WDPS = 1	1:1
WDPS = 2	1:2
WDPS = 4	1:4
WDPS = 8	1:8
WDPS = 16	1:16
WDPS = 32	1:32
WDPS = 64	1:64
WDPS = 128	1:128
WDPS = 256	1:256
WDPS = 512	1:512
WDPS = 1024	1:1024
WDPS = 2048	1:2048
WDPS = 4096	1:4096
WDPS = 8192	1:8192
WDPS = 16384	1:16384
WDPS = 32768	1:32768

Timer1 Oscillator MUX:

T1OSCMX = OFF	Active
T1OSCMX = ON	Inactive

High-Side Transistors Polarity:

HPOL = LOW	Active low
HPOL = HIGH	Active high

Low-Side Transistors Polarity:

LPOL = LOW	Active low
LPOL = HIGH	Active high

PWM output pins Reset state control:

PWMPIN = ON	Enabled
PWMPIN = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

External clock MUX bit:

EXCLKMX = RD0	Multiplexed with RD0
EXCLKMX = RC3	Multiplexed with RC3

PWM4 MUX bit:

PWM4MX = RD5	Multiplexed with RD5
PWM4MX = RB5	Multiplexed with RB5

SSP I/O MUX bit:

SSPMX = RD1	SDO output is multiplexed with RD1
SSPMX = RC7	SD0 output is multiplexed with RC7

FLTA MUX bit:

FLTAMX = RD4	Multiplexed with RD4
FLTAMX = RC1	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4439

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4450

96 MHz PLL Prescaler:

PLLDIV = 1	No divide (4 MHz input)
PLLDIV = 2	Divide by 2 (8 MHz input)
PLLDIV = 3	Divide by 3 (12 MHz input)
PLLDIV = 4	Divide by 4 (16 MHz input)
PLLDIV = 5	Divide by 5 (20 MHz input)
PLLDIV = 6	Divide by 6 (24 MHz input)
PLLDIV = 10	Divide by 10 (40 MHz input)
PLLDIV = 12	Divide by 12 (48 MHz input)

CPU System Clock Postscaler:

CPUDIV = OSC1_PLL2	[OSC1/OSC2 Src: /1][96 MHz PLL Src: /2]
CPUDIV = OSC2_PLL3	[OSC1/OSC2 Src: /2][96 MHz PLL Src: /3]
CPUDIV = OSC3_PLL4	[OSC1/OSC2 Src: /3][96 MHz PLL Src: /4]
CPUDIV = OSC4_PLL6	[OSC1/OSC2 Src: /4][96 MHz PLL Src: /6]

Full-Speed USB Clock Source Selection:

USBDIV = 1	Clock source from OSC1/OSC2
USBDIV = 2	Clock source from 96 MHz PLL/2

Oscillator Selection bits:

FOSC = XT_XT	XT oscillator, XT used by USB
FOSC = XTPLL_XT	XT oscillator, PLL enabled, XT used by USB
FOSC = ECIO_EC	External clock, port function on RA6, EC used by USB
FOSC = EC_EC	External clock, CLKOUT on RA6, EC used by USB
FOSC = ECPLLIO_EC	External clock, PLL enabled, port function on RA6, EC used by USB
FOSC = ECPLL_EC	External clock, PLL enabled, CLKOUT on RA6, EC used by USB
FOSC = INTOSCIO_EC	Internal oscillator, port function on RA6, EC used by USB
FOSC = INTOSC_EC	Internal oscillator, CLKOUT on RA6, EC used by USB
FOSC = INTOSC_XT	Internal oscillator, XT used by USB
FOSC = INTOSC_HS	Internal oscillator, HS used by USB
FOSC = HS	HS oscillator, HS used by USB
FOSC = HSPLL_HS	HS oscillator, PLL enabled, HS used by USB

Fail-Safe Clock Monitor:

FCMEM = OFF	Disabled
FCMEM = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SOFT	Controlled by SBOREN
BOR = ON_ACTIVE	Enabled when the device is not in Sleep, SBOREN bit is disabled
BOR = ON	Enabled, SBOREN bit is disabled

Brown-out Voltage:

BORV = 46	4.6V
BORV = 43	4.3V
BORV = 28	2.8V
BORV = 21	2.1V

USB Voltage Regulator Enable:

VREGEN = OFF	Disabled
VREGEN = ON	Enabled

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator Enable:

LPT1OSC = OFF	Timer1 oscillator configured for high power
LPT1OSC = ON	Timer1 oscillator configured for low power

PORTB A/D Enable:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input on Reset

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Boot Block Size Select Bit:

BBSIZ = BB2K	2KW Boot Block Size
BBSIZ = BB1K	1KW Boot Block Size

Dedicated In-Circuit Debug/Programming Enable:

ICPRT = OFF	Disabled
ICPRT = ON	Enabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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PLL Prescaler Selection bits:

PLLDIV = 1	No prescale (4 MHz oscillator input drives PLL directly)
PLLDIV = 2	Divide by 2 (8 MHz oscillator input)
PLLDIV = 3	Divide by 3 (12 MHz oscillator input)
PLLDIV = 4	Divide by 4 (16 MHz oscillator input)
PLLDIV = 5	Divide by 5 (20 MHz oscillator input)
PLLDIV = 6	Divide by 6 (24 MHz oscillator input)
PLLDIV = 10	Divide by 10 (40 MHz oscillator input)
PLLDIV = 12	Divide by 12 (48 MHz oscillator input)

CPU System Clock Postscaler:

CPUDIV = OSC1_PLL2	[OSC1/OSC2 Src: /1][96 MHz PLL Src: /2]
CPUDIV = OSC2_PLL3	[OSC1/OSC2 Src: /2][96 MHz PLL Src: /3]
CPUDIV = OSC3_PLL4	[OSC1/OSC2 Src: /3][96 MHz PLL Src: /4]
CPUDIV = OSC4_PLL6	[OSC1/OSC2 Src: /4][96 MHz PLL Src: /6]

USB Clock Selection bit (used in Full Speed USB mode only; UCFG:FSEN = 1):

USBDIV = 1	USB clock source comes directly from the primary oscillator block with no postscale
USBDIV = 2	USB clock source comes from the 96 MHz PLL divided by 2

Oscillator Selection bits:

FOSC = XT_XT	XT oscillator, XT used by USB
FOSC = XTPLL_XT	XT oscillator, PLL enabled, XT used by USB
FOSC = ECIO_EC	External clock, port function on RA6, EC used by USB
FOSC = EC_EC	External clock, CLKOUT on RA6, EC used by USB
FOSC = ECPLLIO_EC	External clock, PLL enabled, port function on RA6, EC used by USB
FOSC = ECPLL_EC	External clock, PLL enabled, CLKOUT on RA6, EC used by USB
FOSC = INTOSCIO_EC	Internal oscillator, port function on RA6, EC used by USB
FOSC = INTOSC_EC	Internal oscillator, CLKOUT on RA6, EC used by USB
FOSC = INTOSC_XT	Internal oscillator, XT used by USB
FOSC = INTOSC_HS	Internal oscillator, HS used by USB
FOSC = HS	HS oscillator, HS used by USB
FOSC = HSPLL_HS	HS oscillator, PLL enabled, HS used by USB

Fail-Safe Clock Monitor Enable bit:

FCMEM = OFF	Fail-Safe Clock Monitor disabled
FCMEM = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = ON_ACTIVE	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

USB Voltage Regulator Enable bit:

VREGEN = OFF	USB voltage regulator disabled
VREGEN = ON	USB voltage regulator enabled

Watchdog Timer Enable bit:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RB3
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Dedicated In-Circuit Debug/Programming Port (ICPORT) Enable bit:

ICPRT = OFF	ICPORT disabled
ICPRT = ON	ICPORT enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Configuration registers (300000-3000FFFh) write-protected
WRTB = OFF	Configuration registers (300000-3000FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Boot block (000000-0007FFFh) write-protected
WRTC = OFF	Boot block (000000-0007FFFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F448

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4480

Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F44J10**Background Debugger Enable bit:**

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLKO function on OSC2

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

CCP2 MUX bit:

CCP2MX = ALTERNATE	CCP2 is multiplexed with RB3
CCP2MX = DEFAULT	CCP2 is multiplexed with RC1

PIC18F4510

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-003FFFh) code-protected
CP0 = OFF	Block 0 (000800-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks

PIC18F452

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disable (RB3)
CCP2MUX = ON	Enable (RC1)

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4520

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F4523

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTB	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFFh) code-protected
CPB = OFF	Boot block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFFh) write-protected
WRTB = OFF	Boot block (000000-0007FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F4525

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO6	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO6	RC-OSC2 as RA6
OSC = INTIO67	INTRC-OSC2 as RA6, OSC1 as RA7
OSC = INTIO7	INTRC-OSC2 as Clock Out, OSC1 as RA7

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	SBOREN Enabled
BOREN = NOSLP	Enabled except Sleep, SBOREN Disabled
BOREN = SBORDIS	Enabled, SBOREN Disabled

Brown-out Voltage:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

T1 Oscillator Enable:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

PORTB A/D Enable:

PBADEN = OFF	PORTB<4:0> digital on Reset
PBADEN = ON	PORTB<4:0> analog on Reset

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

XINST Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4539

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4550

PLL Prescaler Selection bits:

PLLDIV = 1	No prescale (4 MHz oscillator input drives PLL directly)
PLLDIV = 2	Divide by 2 (8 MHz oscillator input)
PLLDIV = 3	Divide by 3 (12 MHz oscillator input)
PLLDIV = 4	Divide by 4 (16 MHz oscillator input)
PLLDIV = 5	Divide by 5 (20 MHz oscillator input)
PLLDIV = 6	Divide by 6 (24 MHz oscillator input)
PLLDIV = 10	Divide by 10 (40 MHz oscillator input)
PLLDIV = 12	Divide by 12 (48 MHz oscillator input)

CPU System Clock Postscaler:

CPUDIV = OSC1_PLL2	[OSC1/OSC2 Src: /1][96 MHz PLL Src: /2]
CPUDIV = OSC2_PLL3	[OSC1/OSC2 Src: /2][96 MHz PLL Src: /3]
CPUDIV = OSC3_PLL4	[OSC1/OSC2 Src: /3][96 MHz PLL Src: /4]
CPUDIV = OSC4_PLL6	[OSC1/OSC2 Src: /4][96 MHz PLL Src: /6]

USB Clock Selection bit (used in Full Speed USB mode only; UCFG:FSEN = 1):

USBDIV = 1	USB clock source comes directly from the primary oscillator block with no postscale
USBDIV = 2	USB clock source comes from the 96 MHz PLL divided by 2

Oscillator Selection bits:

FOSC = XT_XT	XT oscillator, XT used by USB
FOSC = XTPLL_XT	XT oscillator, PLL enabled, XT used by USB
FOSC = ECIO_EC	External clock, port function on RA6, EC used by USB
FOSC = EC_EC	External clock, CLKOUT on RA6, EC used by USB
FOSC = ECPLLIO_EC	External clock, PLL enabled, port function on RA6, EC used by USB
FOSC = ECPLL_EC	External clock, PLL enabled, CLKOUT on RA6, EC used by USB
FOSC = INTOSCIO_EC	Internal oscillator, port function on RA6, EC used by USB
FOSC = INTOSC_EC	Internal oscillator, CLKOUT on RA6, EC used by USB
FOSC = INTOSC_XT	Internal oscillator, XT used by USB
FOSC = INTOSC_HS	Internal oscillator, HS used by USB
FOSC = HS	HS oscillator, HS used by USB
FOSC = HSPLL_HS	HS oscillator, PLL enabled, HS used by USB

Fail-Safe Clock Monitor Enable bit:

FCMEM = OFF	Fail-Safe Clock Monitor disabled
FCMEM = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOR = OFF	Brown-out Reset disabled in hardware and software
BOR = SOFT	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOR = ON_ACTIVE	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOR = ON	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

USB Voltage Regulator Enable bit:

VREGEN = OFF	USB voltage regulator disabled
VREGEN = ON	USB voltage regulator enabled

Watchdog Timer Enable bit:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RB3
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Dedicated In-Circuit Debug/Programming Port (ICPORT) Enable bit:

ICPRT = OFF	ICPORT disabled
ICPRT = ON	ICPORT enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-001FFFh) code-protected
CP0 = OFF	Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (002000-003FFFh) code-protected
CP1 = OFF	Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (004000-005FFFh) code-protected
CP2 = OFF	Block 2 (004000-005FFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFh) code-protected
CPB = OFF	Boot block (000000-0007FFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Configuration registers (300000-3000FFh) write-protected
WRTB = OFF	Configuration registers (300000-3000FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Boot block (000000-0007FFh) write-protected
WRTC = OFF	Boot block (000000-0007FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks

PIC18F458

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4580

Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Enhanced Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block
BBSIZ = 4096	4K words (8K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSC-CON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK0 function on OSC2

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

CCP2 MUX bit:

CCP2MX = ALTERNATE	CCP2 is multiplexed with RB3
CCP2MX = DEFAULT	CCP2 is multiplexed with RC1

PIC18F45K20

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO6	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO6	RC-OSC2 as RA6
OSC = INTIO67	INTRC-OSC2 as RA6, OSC1 as RA7
OSC = INTIO7	INTRC-OSC2 as Clock Out, OSC1 as RA7

Fail Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power Up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown Out Reset:

BOREN = OFF	Disabled
BOREN = ON	SBOREN Enabled
BOREN = NOSLP	Enabled except SLEEP, SBOREN Disabled
BOREN = SBORDIS	Enabled, SBOREN Disabled

Brown Out Voltage:

BORV = 46	3.0V
BORV = 43	2.7V
BORV = 28	2.2V
BORV = 21	1.8

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

T1 Oscillator Enable:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

Port B A/D Enable:

PBADEN = OFF	Port B<4:0> digital on RESET
PBADEN = ON	Port B<4:0> analog on RESET

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

XINST Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4610**Oscillator Selection bits:**

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	MCLR pin enabled; RE3 input pin disabled
MCLRE = ON	RE3 input pin enabled; MCLR disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800-003FFFh) code-protected
CP0 = OFF	Block 0 (000800-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot block (000000-0007FFh) code-protected
CPB = OFF	Boot block (000000-0007FFh) not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFh) write-protected
WRTB = OFF	Boot block (000000-0007FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFh) not protected from table reads executed in other blocks

PIC18F4620

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO6	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO6	RC-OSC2 as RA6
OSC = INTIO67	INTRC-OSC2 as RA6, OSC1 as RA7
OSC = INTIO7	INTRC-OSC2 as Clock Out, OSC1 as RA7

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = ON	SBOREN Enabled
BOREN = NOSLP	Enabled except Sleep, SBOREN Disabled
BOREN = SBORDIS	Enabled, SBOREN Disabled

Brown-out Voltage:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

T1 Oscillator Enable:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

PORTB A/D Enable:

PBADEN = OFF	PORTB<4:0> digital on Reset
PBADEN = ON	PORTB<4:0> analog on Reset

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

XINST Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F4680

Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMENB = OFF	Disabled
FCMENB = ON	Enabled

Internal External Osc. Switch:

IESOB = OFF	Disabled
IESOB = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = SBORENCTRL	Controlled by SBOREN
BOR = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOR = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Timer1 Low Power Oscillator Disabled
LPT1OSC = ON	Timer1 Low Power Oscillator Active

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Enhanced Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block
BBSIZ = 4096	4K words (8K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	External RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	External RC with OSC2 as RA6
OSC = IRCIO67	Internal RC with OSC2 as RA6 and OSC1 as RA7
OSC = IRCIO7	Internal RC with OSC1 as RA7 and OSC2 as divide by 4 clock out
OSC = ERC1	External RC with OSC2 as divide by 4 clock out
OSC = ERC	External RC with OSC2 as divide by 4 clock out

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal External Osc. Switch:

IESO = OFF	Disabled
IESO = ON	Enabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOREN = OFF	Disabled
BOREN = SBORENCTRL	Controlled by SBOREN
BOREN = BOACTIVE	Enabled whenever Part is Active - SBOREN Disabled
BOREN = BOHW	Enabled in HW, SBOREN Disabled

Brown-out Voltage:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

Low Power Timer1 Oscillator:

LPT1OSC = OFF	Disabled
LPT1OSC = ON	Enabled

PORTB Pins Configured for A/D:

PBADEN = OFF	PORTB<4> and PORTB<1:0> Configured as Digital I/O Pins on Reset
PBADEN = ON	PORTB<4> and PORTB<1:0> Configured as Analog Pins on Reset

BackGround Debug:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Enhanced Instruction Set CPU:

XINST = OFF	Disabled
XINST = ON	Enabled

Boot Block Size:

BBSIZ = 1024	1K words (2K bytes) Boot Block
BBSIZ = 2048	2K words (4K bytes) Boot Block
BBSIZ = 4096	4K words (8K bytes) Boot Block

Low Voltage Programming:

LVP = OFF	Disabled
LVP = ON	Enabled

Stack Overflow/Underflow Reset:

STVREN = OFF	Disabled
STVREN = ON	Enabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Code Protection Block 4:

CP4 = ON	Enabled
CP4 = OFF	Disabled

Code Protection Block 5:

CP5 = ON	Enabled
CP5 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Write Protection Block 4:

WRT4 = ON	Enabled
WRT4 = OFF	Disabled

Write Protection Block 5:

WRT5 = ON	Enabled
WRT5 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Table Read Protection Block 4:

EBTR4 = ON	Enabled
EBTR4 = OFF	Disabled

Table Read Protection Block 5:

EBTR5 = ON	Enabled
EBTR5 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTE	CCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block code-protected
CP = OFF	Program memory block not code-protected

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown Out Voltage:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block (000000-003FFFh) code-protected
CP = OFF	Program memory block (000000-003FFFh) not code-protected

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTE	CCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block code-protected
CP = OFF	Program memory block not code-protected

PIC18F6490

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown Out Voltage:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block (000000-003FFFh) code-protected
CP = OFF	Program memory block (000000-003FFFh) not code-protected

PIC18F64J90**Background Debugger Enable bit:**

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

PIC18F6520

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC-OSC2 as Clock Out
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Uses RE7
CCP2MUX = RE7	Uses RE7
CCP2MUX = ON	Uses RC1
CCP2MUX = RC1	Uses RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F6525

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6
OSC = ECIOPLL	EC-OSC2 as RA6 and PLL
OSC = ECIOSWPLL	EC-OSC2 as RA6 and SW PLL
OSC = HSSWPLL	HS with SW PLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3 or RE7
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F6527

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTE	ECCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFFh) code-protected
CPB = OFF	Boot Block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

PIC18F6585

Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	RC with OSC2 as RA6
OSC = ECIOPLL	EC with OSC2 as RA6 and HW enabled 4xPLL
OSC = ECIO SWPLL	EC with OSC2 as RA6 and SW enabled 4xPLL
OSC = HSSWPLL	HS with SW enabled 4xPLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RE7
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

PIC18F6620

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disabled
CCP2MUX = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6
OSC = ECIOPLL	EC-OSC2 as RA6 and PLL
OSC = ECIOSWPLL	EC-OSC2 as RA6 and SW PLL
OSC = HSSWPLL	HS with SW PLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3 or RE7
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTE	ECCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFFh) code-protected
CPB = OFF	Boot Block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTE	ECCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Code Protection bit Block 4:

CP4 = ON	Block 4 (010000-013FFFh) code-protected
CP4 = OFF	Block 4 (010000-013FFFh) not code-protected

Code Protection bit Block 5:

CP5 = ON	Block 5 (014000-017FFFh) code-protected
CP5 = OFF	Block 5 (014000-017FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFFh) code-protected
CPB = OFF	Boot Block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Write Protection bit Block 4:

WRT4 = ON	Block 4 (010000-013FFFh) write-protected
WRT4 = OFF	Block 4 (010000-013FFFh) not write-protected

Write Protection bit Block 5:

WRT5 = ON	Block 5 (014000-017FFFh) write-protected
WRT5 = OFF	Block 5 (014000-017FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 4:

EBTR4 = ON	Block 4 (010000-013FFFh) protected from table reads executed in other blocks
EBTR4 = OFF	Block 4 (010000-013FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 5:

EBTR5 = ON	Block 5 (014000-017FFFh) protected from table reads executed in other blocks
EBTR5 = OFF	Block 5 (014000-017FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	RC with OSC2 as RA6
OSC = ECIOPLL	EC with OSC2 as RA6 and HW enabled 4xPLL
OSC = ECIOPLL	EC with OSC2 as RA6 and SW enabled 4xPLL
OSC = HSSWPLL	HS with SW enabled 4xPLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RE7
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSC-CON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
FOSC2 = ON	FOSC<1:0> selects system clock for OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, Software Controlled PLL
FOSC = EC	External Clock
FOSC = ECPLL	External Clock, Software Controlled PLL

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

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Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
FOSC2 = ON	FOSC<1:0> selects system clock for OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, Software Controlled PLL
FOSC = EC	External Clock
FOSC = ECPLL	External Clock, Software Controlled PLL

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

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Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

CCP2 MUX:

CCP2MUX = OFF	Disabled
CCP2MUX = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Code Protection Block 4:

CP4 = ON	Enabled
CP4 = OFF	Disabled

Code Protection Block 5:

CP5 = ON	Enabled
CP5 = OFF	Disabled

Code Protection Block 6:

CP6 = ON	Enabled
CP6 = OFF	Disabled

Code Protection Block 7:

CP7 = ON	Enabled
CP7 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Write Protection Block 4:

WRT4 = ON	Enabled
WRT4 = OFF	Disabled

Write Protection Block 5:

WRT5 = ON	Enabled
WRT5 = OFF	Disabled

Write Protection Block 6:

WRT6 = ON	Enabled
WRT6 = OFF	Disabled

Write Protection Block 7:

WRT7 = ON	Enabled
WRT7 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Table Read Protection Block 4:

EBTR4 = ON	Enabled
EBTR4 = OFF	Disabled

Table Read Protection Block 5:

EBTR5 = ON	Enabled
EBTR5 = OFF	Disabled

Table Read Protection Block 6:

EBTR6 = ON	Enabled
EBTR6 = OFF	Disabled

Table Read Protection Block 7:

EBTR7 = ON	Enabled
EBTR7 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTE	ECCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Code Protection bit Block 4:

CP4 = ON	Block 4 (010000-013FFFh) code-protected
CP4 = OFF	Block 4 (010000-013FFFh) not code-protected

Code Protection bit Block 5:

CP5 = ON	Block 5 (014000-017FFFh) code-protected
CP5 = OFF	Block 5 (014000-017FFFh) not code-protected

Code Protection bit Block 6:

CP6 = ON	Block 6 (01BFFF-018000h) code-protected
CP6 = OFF	Block 6 (01BFFF-018000h) not code-protected

Code Protection bit Block 7:

CP7 = ON	Block 7 (01C000-01FFFFh) code-protected
CP7 = OFF	Block 7 (01C000-01FFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFh) code-protected
CPB = OFF	Boot Block (000000-0007FFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Write Protection bit Block 4:

WRT4 = ON	Block 4 (010000-013FFFh) write-protected
WRT4 = OFF	Block 4 (010000-013FFFh) not write-protected

Write Protection bit Block 5:

WRT5 = ON	Block 5 (014000-017FFFh) write-protected
WRT5 = OFF	Block 5 (014000-017FFFh) not write-protected

Write Protection bit Block 6:

WRT6 = ON	Block 6 (01BFFF-018000h) write-protected
WRT6 = OFF	Block 6 (01BFFF-018000h) not write-protected

Write Protection bit Block 7:

WRT7 = ON	Block 7 (01C000-01FFFFh) write-protected
WRT7 = OFF	Block 7 (01C000-01FFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 4:

EBTR4 = ON	Block 4 (010000-013FFFh) protected from table reads executed in other blocks
EBTR4 = OFF	Block 4 (010000-013FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 5:

EBTR5 = ON	Block 5 (014000-017FFFh) protected from table reads executed in other blocks
EBTR5 = OFF	Block 5 (014000-017FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 6:

EBTR6 = ON	Block 6 (018000-01BFFFh) protected from table reads executed in other blocks
EBTR6 = OFF	Block 6 (018000-01BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 7:

EBTR7 = ON	Block 7 (01C000-01FFFFh) protected from table reads executed in other blocks
EBTR7 = OFF	Block 7 (01C000-01FFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
FOSC2 = ON	FOSC<1:0> selects system clock for OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, Software Controlled PLL
FOSC = EC	External Clock
FOSC = ECPLL	External Clock, Software Controlled PLL

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Data Memory Mode Select bits:

PM = EM	Extended Microcontroller mode
PM = MPB	Microprocessor with Boot Block mode
PM = MP	Microprocessor mode
PM = MC	Microcontroller mode

External Bus Data Width Select bit:

BW = 8	8-bit External Bus Data Width
BW = 16	16-bit External Bus Data Width

External Bus Data Wait Enable bit:

WAIT = ON	Wait programmed by WAIT1 and WAIT0 bits of MEMCOM register (MEMCOM<5:4>)
WAIT = OFF	Wait selections unavailable, device will not wait

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 is multiplexed with RB3 in Extended Microcontroller, Microprocessor or Microprocessor with Boot Block mode. Or with RE7 in Microcontroller mode.
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block code-protected
CP = OFF	Program memory block not code-protected

Table Read Protection bit:

EBTR = ON	Internal program memory block protected from table reads executed from external memory block
EBTR = OFF	Internal program memory block not protected from table reads executed from external memory block

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown Out Voltage:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block (000000-003FFFh) code-protected
CP = OFF	Program memory block (000000-003FFFh) not code-protected

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Configuration Settings

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Data Memory Mode Select bits:

PM = EM	Extended Microcontroller mode
PM = MPB	Microprocessor with Boot Block mode
PM = MP	Microprocessor mode
PM = MC	Microcontroller mode

External Bus Data Width Select bit:

BW = 8	8-bit External Bus Data Width
BW = 16	16-bit External Bus Data Width

External Bus Data Wait Enable bit:

WAIT = ON	Wait programmed by WAIT1 and WAIT0 bits of MEMCOM register (MEMCOM<5:4>)
WAIT = OFF	Wait selections unavailable, device will not wait

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 is multiplexed with RB3 in Extended Microcontroller, Microprocessor or Microprocessor with Boot Block mode. Or with RE7 in Microcontroller mode.
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block code-protected
CP = OFF	Program memory block not code-protected

Table Read Protection bit:

EBTR = ON	Internal program memory block protected from table reads executed from external memory block
EBTR = OFF	Internal program memory block not protected from table reads executed from external memory block

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (clock frequency = 4 x FOSC1)
OSC = RCIO	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Oscillator Switchover mode disabled
IESO = ON	Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown Out Voltage:

BORV = 0	Maximum Setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum Setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer 1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RE7
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit:

CP = ON	Program memory block (000000-003FFFh) code-protected
CP = OFF	Program memory block (000000-003FFFh) not code-protected

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLK0 function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC-OSC2 as Clock Out
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Processor Mode Selection:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

CCP2 MUX:

CCP2MUX = OFF	Uses RE7
CCP2MUX = RE7	Uses RE7
CCP2MUX = ON	Uses RC1
CCP2MUX = RC1	Uses RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F8525

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6
OSC = ECIOPLL	EC-OSC2 as RA6 and PLL
OSC = ECIOPLL	EC-OSC2 as RA6 and SW PLL
OSC = HSSWPLL	HS with SW PLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Mode Selection:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

ECCP MUX:

ECCPMX = PORTH	Multiplexed with RH7:4
ECCPMX = PORTE	Multiplexed with RE6:3

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3 or RE7
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F8527**Oscillator Selection bits:**

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Data Memory Mode Select bits:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

Address Bus Width Select bits:

ADDRBW = ADDR8BIT	8-bit Address Bus
ADDRBW = ADDR12BIT	12-bit Address Bus
ADDRBW = ADDR16BIT	16-bit Address Bus
ADDRBW = ADDR20BIT	20-bit Address Bus

Data Bus Width Select bit:

DATABW = DATA8BIT	8-bit External Bus mode
DATABW = DATA16BIT	16-bit External Bus mode

External Bus Data Wait Enable bit:

WAIT = ON	Wait selections for table reads and table writes are determined by the WAIT1:WAIT0 bits
WAIT = OFF	Wait selections are unavailable for table reads and table writes

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

ECCP MUX bit:

ECCPMX = PORTH	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RH7, RH6, RH5 and RH4 respectively
ECCPMX = PORTE	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RE6, RE5, RE4 and RE3 respectively

CCP2 MUX bit:

CCP2MX = PORTBE	ECCP2 is multiplexed with RB3 in Extended Microcontroller, Microprocessor or Microprocessor with Boot Block mode. Or with RE7 in Microcontroller mode.
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFFh) code-protected
CPB = OFF	Boot Block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	RC with OSC2 as RA6
OSC = ECIOPLL	EC with OSC2 as RA6 and HW enabled 4xPLL
OSC = ECIOPLL	EC with OSC2 as RA6 and SW enabled 4xPLL
OSC = HSSWPLL	HS with SW enabled 4xPLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Mode Selection:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RE7
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

External Bus Wait Enable bit:

WAIT = ON	Wait states for operations on external memory bus enabled
WAIT = OFF	Wait states for operations on external memory bus disabled

Data Bus Width Select bit:

BW = 8	8-bit external bus mode
BW = 16	16-bit external bus mode

Processor Mode Selection:

MODE = MM	Microcontroller mode - External bus disabled
MODE = XM12	Extended Microcontroller mode, 12-bit Address mode
MODE = XM16	Extended Microcontroller mode, 16-bit Address mode
MODE = XM20	Extended Microcontroller mode, 20-bit Address mode

External Address Bus Shift Enable bit:

EASHFT = OFF	Address shifting disabled, address on external bus reflects the PC value
EASHFT = ON	Address shifting enabled, address on external bus is offset to start at 000000h

ECCPx MUX bit:

ECCPMX = ALTERNATE	ECCP1 outputs (P1B/P1C) are multiplexed with RH7 and RH6; ECCP3 outputs (P3B/P3C) are multiplexed with RH5 and RH4
ECCPMX = DEFAULT	ECCP1 outputs (P1B/P1C) are multiplexed with RE6 and RE5; ECCP3 outputs (P3B/P3C) are multiplexed with RE4 and RE3

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

PIC18F85J15**Background Debugger Enable bit:**

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

External Bus Wait Enable bit:

WAIT = ON	Wait states for operations on external memory bus enabled
WAIT = OFF	Wait states for operations on external memory bus disabled

Data Bus Width Select bit:

BW = 8	8-bit external bus mode
BW = 16	16-bit external bus mode

Processor Mode Selection:

MODE = MM	Microcontroller mode - External bus disabled
MODE = XM12	Extended Microcontroller mode, 12-bit Address mode
MODE = XM16	Extended Microcontroller mode, 16-bit Address mode
MODE = XM20	Extended Microcontroller mode, 20-bit Address mode

External Address Bus Shift Enable bit:

EASHFT = OFF	Address shifting disabled, address on external bus reflects the PC value
EASHFT = ON	Address shifting enabled, address on external bus is offset to start at 000000h

ECCPx MUX bit:

ECCPMX = ALTERNATE	ECCP1 outputs (P1B/P1C) are multiplexed with RH7 and RH6; ECCP3 outputs (P3B/P3C) are multiplexed with RH5 and RH4
ECCPMX = DEFAULT	ECCP1 outputs (P1B/P1C) are multiplexed with RE6 and RE5; ECCP3 outputs (P3B/P3C) are multiplexed with RE4 and RE3

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

PIC18F85J90**Background Debugger Enable bit:**

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Processor Mode Selection:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

CCP2 MUX:

CCP2MUX = OFF	Disabled
CCP2MUX = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F8621

Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6
OSC = ECIOPLL	EC-OSC2 as RA6 and PLL
OSC = ECIOSWPLL	EC-OSC2 as RA6 and SW PLL
OSC = HSSWPLL	HS with SW PLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Mode Selection:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

ECCP MUX:

ECCPMX = PORTH	Multiplexed with RH7:4
ECCPMX = PORTE	Multiplexed with RE6:3

CCP2 MUX:

CCP2MX = PORTBE	Multiplexed with RB3 or RE7
CCP2MX = PORTC	Multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

PIC18F8622**Oscillator Selection bits:**

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Data Memory Mode Select bits:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

Address Bus Width Select bits:

ADDRBW = ADDR8BIT	8-bit Address Bus
ADDRBW = ADDR12BIT	12-bit Address Bus
ADDRBW = ADDR16BIT	16-bit Address Bus
ADDRBW = ADDR20BIT	20-bit Address Bus

Data Bus Width Select bit:

DATABW = DATA8BIT	8-bit External Bus mode
DATABW = DATA16BIT	16-bit External Bus mode

External Bus Data Wait Enable bit:

WAIT = ON	Wait selections for table reads and table writes are determined by the WAIT1:WAIT0 bits
WAIT = OFF	Wait selections are unavailable for table reads and table writes

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

ECCP MUX bit:

ECCPMX = PORTH	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RH7, RH6, RH5 and RH4 respectively
ECCPMX = PORTE	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RE6, RE5, RE4 and RE3 respectively

CCP2 MUX bit:

CCP2MX = PORTBE	ECCP2 is multiplexed with RB3 in Extended Microcontroller, Microprocessor or Microprocessor with Boot Block mode. Or with RE7 in Microcontroller mode.
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFFh) code-protected
CPB = OFF	Boot Block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Data Memory Mode Select bits:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

Address Bus Width Select bits:

ADDRBW = ADDR8BIT	8-bit Address Bus
ADDRBW = ADDR12BIT	12-bit Address Bus
ADDRBW = ADDR16BIT	16-bit Address Bus
ADDRBW = ADDR20BIT	20-bit Address Bus

Data Bus Width Select bit:

DATABW = DATA8BIT	8-bit External Bus mode
DATABW = DATA16BIT	16-bit External Bus mode

External Bus Data Wait Enable bit:

WAIT = ON	Wait selections for table reads and table writes are determined by the WAIT1:WAIT0 bits
WAIT = OFF	Wait selections are unavailable for table reads and table writes

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

ECCP MUX bit:

ECCPMX = PORTH	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RH7, RH6, RH5 and RH4 respectively
ECCPMX = PORTE	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RE6, RE5, RE4 and RE3 respectively

CCP2 MUX bit:

CCP2MX = PORTBE	ECCP2 is multiplexed with RB3 in Extended Microcontroller, Microprocessor or Microprocessor with Boot Block mode. Or with RE7 in Microcontroller mode.
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Code Protection bit Block 4:

CP4 = ON	Block 4 (010000-013FFFh) code-protected
CP4 = OFF	Block 4 (010000-013FFFh) not code-protected

Code Protection bit Block 5:

CP5 = ON	Block 5 (014000-017FFFh) code-protected
CP5 = OFF	Block 5 (014000-017FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFFh) code-protected
CPB = OFF	Boot Block (000000-0007FFFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Write Protection bit Block 4:

WRT4 = ON	Block 4 (010000-013FFFh) write-protected
WRT4 = OFF	Block 4 (010000-013FFFh) not write-protected

Write Protection bit Block 5:

WRT5 = ON	Block 5 (014000-017FFFh) write-protected
WRT5 = OFF	Block 5 (014000-017FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 4:

EBTR4 = ON	Block 4 (010000-013FFFh) protected from table reads executed in other blocks
EBTR4 = OFF	Block 4 (010000-013FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 5:

EBTR5 = ON	Block 5 (014000-017FFFh) protected from table reads executed in other blocks
EBTR5 = OFF	Block 5 (014000-017FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

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Oscillator Selection bits:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC with OSC2 as divide by 4 clock out
OSC = EC	EC with OSC2 as divide by 4 clock out
OSC = ECIO	EC with OSC2 as RA6
OSC = HSPLL	HS with HW enabled 4xPLL
OSC = RCIO	RC with OSC2 as RA6
OSC = ECIOPLL	EC with OSC2 as RA6 and HW enabled 4xPLL
OSC = ECIOSWPLL	EC with OSC2 as RA6 and SW enabled 4xPLL
OSC = HSSWPLL	HS with SW enabled 4xPLL

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 20	2.0V

Watchdog Timer:

WDT = OFF	HW Disabled - SW Controlled
WDT = ON	HW Enabled - SW Disabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Mode Selection:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

MCLR Enable:

MCLRE = OFF	Disabled
MCLRE = ON	Enabled

CCP2 MUX bit:

CCP2MX = OFF	CCP2 input/output is multiplexed with RE7
CCP2MX = ON	CCP2 input/output is multiplexed with RC1

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

External Bus Wait Enable bit:

WAIT = ON	Wait states for operations on external memory bus enabled
WAIT = OFF	Wait states for operations on external memory bus disabled

Data Bus Width Select bit:

BW = 8	8-bit external bus mode
BW = 16	16-bit external bus mode

Processor Mode Selection:

MODE = MM	Microcontroller mode - External bus disabled
MODE = XM12	Extended Microcontroller mode, 12-bit Address mode
MODE = XM16	Extended Microcontroller mode, 16-bit Address mode
MODE = XM20	Extended Microcontroller mode, 20-bit Address mode

External Address Bus Shift Enable bit:

EASHFT = OFF	Address shifting disabled, address on external bus reflects the PC value
EASHFT = ON	Address shifting enabled, address on external bus is offset to start at 000000h

ECCPx MUX bit:

ECCPMX = ALTERNATE	ECCP1 outputs (P1B/P1C) are multiplexed with RH7 and RH6; ECCP3 outputs (P3B/P3C) are multiplexed with RH5 and RH4
ECCPMX = DEFAULT	ECCP1 outputs (P1B/P1C) are multiplexed with RE6 and RE5; ECCP3 outputs (P3B/P3C) are multiplexed with RE4 and RE3

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

External Bus Wait Enable bit:

WAIT = ON	Wait states for operations on external memory bus enabled
WAIT = OFF	Wait states for operations on external memory bus disabled

Data Bus Width Select bit:

BW = 8	8-bit external bus mode
BW = 16	16-bit external bus mode

Processor Mode Selection:

MODE = MM	Microcontroller mode - External bus disabled
MODE = XM12	Extended Microcontroller mode, 12-bit Address mode
MODE = XM16	Extended Microcontroller mode, 16-bit Address mode
MODE = XM20	Extended Microcontroller mode, 20-bit Address mode

External Address Bus Shift Enable bit:

EASHFT = OFF	Address shifting disabled, address on external bus reflects the PC value
EASHFT = ON	Address shifting enabled, address on external bus is offset to start at 000000h

ECCPx MUX bit:

ECCPMX = ALTERNATE	ECCP1 outputs (P1B/P1C) are multiplexed with RH7 and RH6; ECCP3 outputs (P3B/P3C) are multiplexed with RH5 and RH4
ECCPMX = DEFAULT	ECCP1 outputs (P1B/P1C) are multiplexed with RE6 and RE5; ECCP3 outputs (P3B/P3C) are multiplexed with RE4 and RE3

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

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Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
FOSC2 = ON	FOSC<1:0> selects system clock for OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, Software Controlled PLL
FOSC = EC	External Clock
FOSC = ECPLL	External Clock, Software Controlled PLL

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

ECCP MUX:

ECCPMX = OFF	Disabled
ECCPMX = ON	Enabled

CCP2 MUX:

CCP2MX = OFF	Disabled
CCP2MX = ON	Enabled

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Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
FOSC2 = ON	FOSC<1:0> selects system clock for OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, Software Controlled PLL
FOSC = EC	External Clock
FOSC = ECPLL	External Clock, Software Controlled PLL

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

ECCP MUX:

ECCPMX = OFF	Disabled
ECCPMX = ON	Enabled

CCP2 MUX:

CCP2MX = OFF	Disabled
CCP2MX = ON	Enabled

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Oscillator Selection:

OSC = LP	LP
OSC = XT	XT
OSC = HS	HS
OSC = RC	RC
OSC = EC	EC-OSC2 as Clock Out
OSC = ECIO	EC-OSC2 as RA6
OSC = HSPLL	HS-PLL Enabled
OSC = RCIO	RC-OSC2 as RA6

Osc. Switch Enable:

OSCS = ON	Enabled
OSCS = OFF	Disabled

Power-up Timer:

PWRT = ON	Enabled
PWRT = OFF	Disabled

Brown-out Reset:

BOR = OFF	Disabled
BOR = ON	Enabled

Brown-out Voltage:

BORV = 45	4.5V
BORV = 42	4.2V
BORV = 27	2.7V
BORV = 25	2.5V

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128

Processor Mode Selection:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

CCP2 MUX:

CCP2MUX = OFF	Disabled
CCP2MUX = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Low Voltage ICSP:

LVP = OFF	Disabled
LVP = ON	Enabled

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Code Protection Block 0:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Code Protection Block 1:

CP1 = ON	Enabled
CP1 = OFF	Disabled

Code Protection Block 2:

CP2 = ON	Enabled
CP2 = OFF	Disabled

Code Protection Block 3:

CP3 = ON	Enabled
CP3 = OFF	Disabled

Code Protection Block 4:

CP4 = ON	Enabled
CP4 = OFF	Disabled

Code Protection Block 5:

CP5 = ON	Enabled
CP5 = OFF	Disabled

Code Protection Block 6:

CP6 = ON	Enabled
CP6 = OFF	Disabled

Code Protection Block 7:

CP7 = ON	Enabled
CP7 = OFF	Disabled

Boot Block Code Protection:

CPB = ON	Enabled
CPB = OFF	Disabled

Data EEPROM Code Protection:

CPD = ON	Enabled
CPD = OFF	Disabled

Write Protection Block 0:

WRT0 = ON	Enabled
WRT0 = OFF	Disabled

Write Protection Block 1:

WRT1 = ON	Enabled
WRT1 = OFF	Disabled

Write Protection Block 2:

WRT2 = ON	Enabled
WRT2 = OFF	Disabled

Write Protection Block 3:

WRT3 = ON	Enabled
WRT3 = OFF	Disabled

Write Protection Block 4:

WRT4 = ON	Enabled
WRT4 = OFF	Disabled

Write Protection Block 5:

WRT5 = ON	Enabled
WRT5 = OFF	Disabled

Write Protection Block 6:

WRT6 = ON	Enabled
WRT6 = OFF	Disabled

Write Protection Block 7:

WRT7 = ON	Enabled
WRT7 = OFF	Disabled

Boot Block Write Protection:

WRTB = ON	Enabled
WRTB = OFF	Disabled

Configuration Register Write Protection:

WRTC = ON	Enabled
WRTC = OFF	Disabled

Data EEPROM Write Protection:

WRTD = ON	Enabled
WRTD = OFF	Disabled

Table Read Protection Block 0:

EBTR0 = ON	Enabled
EBTR0 = OFF	Disabled

Table Read Protection Block 1:

EBTR1 = ON	Enabled
EBTR1 = OFF	Disabled

Table Read Protection Block 2:

EBTR2 = ON	Enabled
EBTR2 = OFF	Disabled

Table Read Protection Block 3:

EBTR3 = ON	Enabled
EBTR3 = OFF	Disabled

Table Read Protection Block 4:

EBTR4 = ON	Enabled
EBTR4 = OFF	Disabled

Table Read Protection Block 5:

EBTR5 = ON	Enabled
EBTR5 = OFF	Disabled

Table Read Protection Block 6:

EBTR6 = ON	Enabled
EBTR6 = OFF	Disabled

Table Read Protection Block 7:

EBTR7 = ON	Enabled
EBTR7 = OFF	Disabled

Boot Block Table Read Protection:

EBTRB = ON	Enabled
EBTRB = OFF	Disabled

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Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECIO6	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Processor Data Memory Mode Select bits:

MODE = EM	Extended Microcontroller mode
MODE = MPB	Microprocessor with Boot Block mode
MODE = MP	Microprocessor mode
MODE = MC	Microcontroller mode

Address Bus Width Select bits:

ADDRBW = ADDR8BIT	8-bit Address Bus
ADDRBW = ADDR12BIT	12-bit Address Bus
ADDRBW = ADDR16BIT	16-bit Address Bus
ADDRBW = ADDR20BIT	20-bit Address Bus

Data Bus Width Select bit:

DATABW = DATA8BIT	8-bit External Bus mode
DATABW = DATA16BIT	16-bit External Bus mode

External Bus Data Wait Enable bit:

WAIT = ON	Wait selections for table reads and table writes are determined by the WAIT1:WAIT0 bits
WAIT = OFF	Wait selections are unavailable for table reads and table writes

MCLR Pin Enable bit:

MCLRE = OFF	RG5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RG5 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

ECCP MUX bit:

ECCPMX = PORTH	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RH7, RH6, RH5 and RH4 respectively
ECCPMX = PORTE	ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RE6, RE5, RE4 and RE3 respectively

CCP2 MUX bit:

CCP2MX = PORTBE	ECCP2 is multiplexed with RB3 in Extended Microcontroller, Microprocessor or Microprocessor with Boot Block mode. Or with RE7 in Microcontroller mode.
CCP2MX = PORTC	ECCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Boot Block Size Select bits:

BBSIZ = BB2K	1K word (2 Kbytes) Boot Block size
BBSIZ = BB4K	2K words (4 Kbytes) Boot Block size
BBSIZ = BB8K	4K words (8 Kbytes) Boot Block size

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

Code Protection bit Block 0:

CP0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) code-protected
CP0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON	Block 1 (004000-007FFFh) code-protected
CP1 = OFF	Block 1 (004000-007FFFh) not code-protected

Code Protection bit Block 2:

CP2 = ON	Block 2 (008000-00BFFFh) code-protected
CP2 = OFF	Block 2 (008000-00BFFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON	Block 3 (00C000-00FFFFh) code-protected
CP3 = OFF	Block 3 (00C000-00FFFFh) not code-protected

Code Protection bit Block 4:

CP4 = ON	Block 4 (010000-013FFFFh) code-protected
CP4 = OFF	Block 4 (010000-013FFFFh) not code-protected

Code Protection bit Block 5:

CP5 = ON	Block 5 (014000-017FFFFh) code-protected
CP5 = OFF	Block 5 (014000-017FFFFh) not code-protected

Code Protection bit Block 6:

CP6 = ON	Block 6 (01BFFF-018000h) code-protected
CP6 = OFF	Block 6 (01BFFF-018000h) not code-protected

Code Protection bit Block 7:

CP7 = ON	Block 7 (01C000-01FFFFh) code-protected
CP7 = OFF	Block 7 (01C000-01FFFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON	Boot Block (000000-0007FFh) code-protected
CPB = OFF	Boot Block (000000-0007FFh) not code-protected

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800, 001000 or 002000-003FFFFh) write-protected
WRT0 = OFF	Block 0 (000800, 001000 or 002000-003FFFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (004000-007FFFFh) write-protected
WRT1 = OFF	Block 1 (004000-007FFFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (008000-00BFFFFh) write-protected
WRT2 = OFF	Block 2 (008000-00BFFFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (00C000-00FFFFh) write-protected
WRT3 = OFF	Block 3 (00C000-00FFFFh) not write-protected

Write Protection bit Block 4:

WRT4 = ON	Block 4 (010000-013FFFFh) write-protected
WRT4 = OFF	Block 4 (010000-013FFFFh) not write-protected

Write Protection bit Block 5:

WRT5 = ON	Block 5 (014000-017FFFFh) write-protected
WRT5 = OFF	Block 5 (014000-017FFFFh) not write-protected

Write Protection bit Block 6:

WRT6 = ON	Block 6 (01BFFF-018000h) write-protected
WRT6 = OFF	Block 6 (01BFFF-018000h) not write-protected

Write Protection bit Block 7:

WRT7 = ON	Block 7 (01C000-01FFFFh) write-protected
WRT7 = OFF	Block 7 (01C000-01FFFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) write-protected
WRTB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTD = ON	Data EEPROM write-protected
WRTD = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800, 001000 or 002000-003FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800, 001000 or 002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (004000-007FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (004000-007FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (008000-00BFFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (008000-00BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (00C000-00FFFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (00C000-00FFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 4:

EBTR4 = ON	Block 4 (010000-013FFFh) protected from table reads executed in other blocks
EBTR4 = OFF	Block 4 (010000-013FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 5:

EBTR5 = ON	Block 5 (014000-017FFFh) protected from table reads executed in other blocks
EBTR5 = OFF	Block 5 (014000-017FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 6:

EBTR6 = ON	Block 6 (018000-01BFFFh) protected from table reads executed in other blocks
EBTR6 = OFF	Block 6 (018000-01BFFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 7:

EBTR7 = ON	Block 7 (01C000-01FFFFh) protected from table reads executed in other blocks
EBTR7 = OFF	Block 7 (01C000-01FFFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot Block (000000-007FFF, 000FFF or 001FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot Block (000000-007FFF, 000FFF or 001FFFh) not protected from table reads executed in other blocks

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Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Stack Overflow/Underflow Reset Enable bit:

STVREN = OFF	Reset on stack overflow/underflow disabled
STVREN = ON	Reset on stack overflow/underflow enabled

Watchdog Timer Enable bit:

WDTEN = OFF	WDT disabled (control is placed on SWDTEN bit)
WDTEN = ON	WDT enabled

Code Protection bit:

CP0 = ON	Program memory is code-protected
CP0 = OFF	Program memory is not code-protected

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit:

IESO = OFF	Two-Speed Start-up disabled
IESO = ON	Two-Speed Start-up enabled

Default/Reset System Clock Select bit:

FOSC2 = OFF	INTRC enabled as system clock when OSCCON<1:0> = 00
FOSC2 = ON	Clock selected by FOSC1:FOSC0 as system clock is enabled when OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, PLL enabled and under software control
FOSC = EC	EC oscillator, CLKO function on OSC2
FOSC = ECPLL	EC oscillator, PLL enabled and under software control, CLK function on OSC2

Watchdog Timer Postscaler Select bits:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

External Bus Wait Enable bit:

WAIT = ON	Wait states for operations on external memory bus enabled
WAIT = OFF	Wait states for operations on external memory bus disabled

Data Bus Width Select bit:

BW = 8	8-bit external bus mode
BW = 16	16-bit external bus mode

Processor Mode Selection:

MODE = MM	Microcontroller mode - External bus disabled
MODE = XM12	Extended Microcontroller mode, 12-bit Address mode
MODE = XM16	Extended Microcontroller mode, 16-bit Address mode
MODE = XM20	Extended Microcontroller mode, 20-bit Address mode

External Address Bus Shift Enable bit:

EASHFT = OFF	Address shifting disabled, address on external bus reflects the PC value
EASHFT = ON	Address shifting enabled, address on external bus is offset to start at 000000h

ECCPx MUX bit:

ECCPMX = ALTERNATE	ECCP1 outputs (P1B/P1C) are multiplexed with RH7 and RH6; ECCP3 outputs (P3B/P3C) are multiplexed with RH5 and RH4
ECCPMX = DEFAULT	ECCP1 outputs (P1B/P1C) are multiplexed with RE6 and RE5; ECCP3 outputs (P3B/P3C) are multiplexed with RE4 and RE3

ECCP2 MUX bit:

CCP2MX = ALTERNATE	ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode
CCP2MX = DEFAULT	ECCP2/P2A is multiplexed with RC1

PIC18F87J60

Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
FOSC2 = ON	FOSC<1:0> selects system clock for OSCCON<1:0> = 00

Oscillator Selection bits:

FOSC = HS	HS oscillator
FOSC = HSPLL	HS oscillator, Software Controlled PLL
FOSC = EC	External Clock
FOSC = ECPLL	External Clock, Software Controlled PLL

Watchdog Postscaler:

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

ECCP MUX:

ECCPMX = OFF	Disabled
ECCPMX = ON	Enabled

CCP2 MUX:

CCP2MX = OFF	Disabled
CCP2MX = ON	Enabled

PIC18F96J60**Background Debugger Enable:**

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

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IESO = OFF	Disabled
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WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

External Bus Data Wait:

WAIT = ON	Enabled
WAIT = OFF	Disabled

Data Bus Width Select:

BW = 8	8-bit external bus
BW = 16	16-bit external bus

Processor Mode Selection:

MODE = MM	Microcontroller mode - External bus disabled
MODE = XM12	Extended Microcontroller mode - 12-bit Address mode
MODE = XM16	Extended Microcontroller mode - 16-bit Address mode
MODE = XM20	Extended Microcontroller mode - 20-bit Address mode

External Address Bus Shift Enable:

EASHFT = OFF	External bus reflects PC value
EASHFT = ON	External bus starts at 000000h

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

ECCP MUX:

ECCPMX = OFF	Disabled
ECCPMX = ON	Enabled

CCP2 MUX:

CCP2MX = OFF	Disabled
CCP2MX = ON	Enabled

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Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
FOSC2 = ON	FOSC<1:0> selects system clock for OSCCON<1:0> = 00

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MODE = XM20	Extended Microcontroller mode - 20-bit Address mode

External Address Bus Shift Enable:

EASHFT = OFF	External bus reflects PC value
EASHFT = ON	External bus starts at 000000h

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

ECCP MUX:

ECCPMX = OFF	Disabled
ECCPMX = ON	Enabled

CCP2 MUX:

CCP2MX = OFF	Disabled
CCP2MX = ON	Enabled

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Background Debugger Enable:

DEBUG = ON	Enabled
DEBUG = OFF	Disabled

Extended Instruction Set Enable:

XINST = OFF	Disabled
XINST = ON	Enabled

Stack Overflow Reset:

STVR = OFF	Disabled
STVR = ON	Enabled

Watchdog Timer:

WDT = OFF	Disabled
WDT = ON	Enabled

Code Protection:

CP0 = ON	Enabled
CP0 = OFF	Disabled

Fail-Safe Clock Monitor:

FCMEN = OFF	Disabled
FCMEN = ON	Enabled

Internal/External Switch Over:

IESO = OFF	Disabled
IESO = ON	Enabled

Default/Reset System Clock Select Bit:

FOSC2 = OFF	INTRC as system clock when OSCCON<1:0> = 00
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WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048
WDTPS = 4096	1:4096
WDTPS = 8192	1:8192
WDTPS = 16384	1:16384
WDTPS = 32768	1:32768

External Bus Data Wait:

WAIT = ON	Enabled
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External Address Bus Shift Enable:

EASHFT = OFF	External bus reflects PC value
EASHFT = ON	External bus starts at 000000h

Ethernet LED Enable:

ETHLED = OFF	Disabled
ETHLED = ON	Enabled

ECCP MUX:

ECCPMX = OFF	Disabled
ECCPMX = ON	Enabled

CCP2 MUX:

CCP2MX = OFF	Disabled
CCP2MX = ON	Enabled

NOTES:



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