Design and Implementation of FPGA Based 32 Bit Floating Point Processor for DSP Application.

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***Abstract*— The floating point arithmetic operations have discovered applications in the various different fields for the necessities for requirments high precision operation because of its incredible dynamic range, high accuracy and fast arithmetic operations. High accuracy is needed for the design and research of the floating point processing units. With the expanding necessities for the floating point operations for the fast high speed data signal processing and the logical operation, the requirements for the high-speed hardware floating point arithmetic units have turned out to be increasingly requesting.**

This paper deals with the design and implementation of the 32-bit floating point Processor with MAC unit for signal processing application. The Linear convolution and Circular convolution of signals is verified. The necessary code is written in the language Verilog. Xilinx 14.7 suite is used for software development and then implementation on Spartan 6 board. The designed DSP has instructions set and consists of 32-bit ALU, 32-bit X 32-bit parallel multiplier for single-cycle MAC operation, 2 addressing modes, 31 auxiliary register arithmetic units.

Keywords—DSP, MAC, FPU, ALU, IEEE754, CPU, RAM, ROM.

I. INTRODUCTION

The Digital Signal Processor (DSP) plays very important role in day-to-day life. In today's life the importance of DSP processor goes increasing. The intelligence of the word transmitting analog based system to digital based system to fast handling and processing.

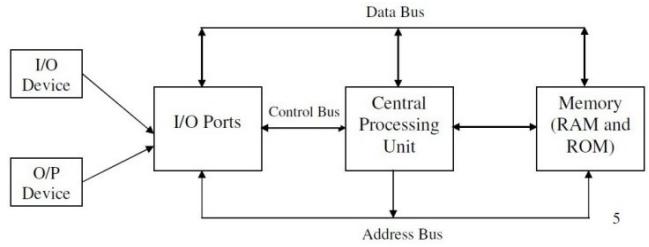
In this paper design, synthesis and implementation of 32 bit IEEE 754 standard Floating Point DSP processor. It has a complete instruction set, program memory and data memory, general purpose registers and a simple Arithmetic & Logical Unit with single precision floating point arithmetic operations like addition, subtraction, multiplication and division.

Figure 1 (a) shows a block diagram of simple processor system. The three major parts of a processor are the memory, the CPU and the I/O ports.

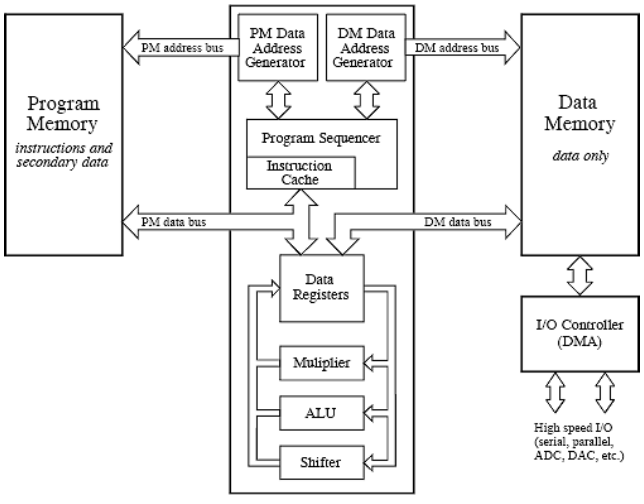
Memory Section The memory section usually consists of ROM and RAM. Memory is used to store instruction sequence or program which computer will execute. Memory is also used to store data to be processed by computer or data resulting from the processing.

CPU Section The central processing unit or CPU contains the control circuitry, an ALU, some registers andan address program counter. To execute a program, the CPU sends out to memory the address of the location of the code for the first instruction to be executed. The CPU also sends out a memory enable signal. The instruction code comes to the CPU from memory and gets decoded and executed. After each operation the program counter increments to the address the location of the next instruction or data stored in memory.

Input-Output Ports The third part of the processor is the interface of the processor with the outside world. This interface is often called input-output ports. An input port allows data from a keyboard or some other data to be taken into the processor under CPU control. An output port is used to send a data to some output devices.



(a)



(b)

Fig.1 Basic block diagram of simple processor (ref 15)

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II. PROPOSED WORK

A. ALU

Arithmetic Logical Unit plays an important role indigital signal processor. The Arithmetic Logic Unit is essentially the heart of a CPU. ALU having generally two inputs one is Operand and second is Opcode. Opcode is nothing but select lines given to ALU.

The operations will be controlled by select lines. Generally two types of operations are performed arithmetic and logical operations. In this processor which operation will be perform is selected by three select lines bit no 23-21 which will shown in table below table 1.

TABLE I. LOGICAL FUNCTIONS

Sr. No.	Logical Functions	
	ALU Control	*Function*
1.	000	Multiplication
2.	001	Addition
3.	010	Subtraction
4.	011	Division
5.	100	AND
6.	101	OR
7.	110	XOR
8.	111	NOT

B. Shifter

The shifter block in DSP processor plays an important block in floating-point operations where it holds the block exponent value. In this shifter the exponent part of the IEEE 754 Floating point number are normalized. The normalization is a processor nothing that the number represent one number after the decimal point. In this rotorby the shifting of the number by left or right by that operation we are normalizing the number for further calculations. The shifter provides a complete set of shifting functions for a 32-bit input values and 32-bit output values. These include arithmetic shift, logical shift and normalization. In this shifter the main role is normalization of a number is followed by shifting.

C. MAC

MAC is one of the most important component of the digital signal processor. In this MAC unit the multiplication and addition both operations are performs. In computing and especially digital signal processing, the multiply–accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known asa multiplier–accumulator MAC unit below fig 2.shows the basic MAC unit structure.

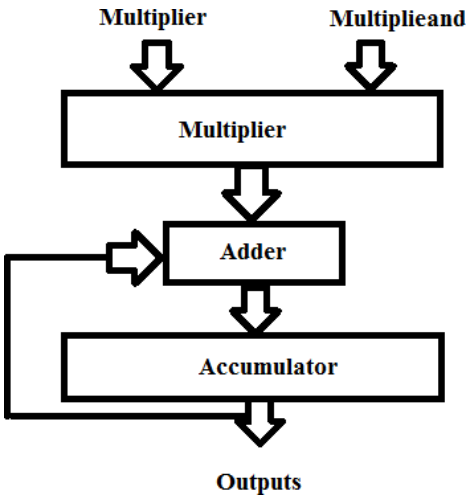

Fig. 2. MAC Unit

D. IEEE 754Standerd

IEEE754 standard is a technical standard established by IEEE and the most widely used standard for floating-point computation, followed by many hardware (CPU and FPU) and software implementations [3]. IEEE 754 Standard for Floating-Point calculations. This standard defines binary representation for floating-point numbers of varying precision, giving specific examples of the binary32 (or single precision) format table no 2 below shows 32 bit floating point standard.

TABLE II. FLOATING POINT STANDARD

IEEE 754 Standard single precision			
Sign	*Exponent*	*Mantissa*	*Bias*
1(31)	8(30-23)	23(22-00)	127

E. Instruction set

All the instructions are 32 bits long and instruction is represented in hex format. There are instructions that have been implemented in the design. According to their purposes, the instructions can be divided into groups which are illustrated in table 3.

TABLE III. INSTRUCTION SET

Instruction set		
Processing Unit	*Operation*	*Instruction*
CPU	Arithmetic	ADD SUB MUL DIV
	Logical	AND OR XOR NOT
	Shifter	
DSP Processing Unit	MAC	

A 32-bit instruction is encoded as follows. The most significant 8 bits represents the opcode (bit 31–bit 24).The next 3 bits represent for select lines for which the ALU operation (bit 23–bit 21), next 4-bit represents the second source register (bit 19- 16 bit) and the next 4-bit represents first source register (bit 15–bit 12) respectively. Next bits are not used. It is not necessary that all the bits will be used in every instruction. When a new instruction is fetched from the instruction memory, for example an arithmetic operation -

ADD R1, R2

This will be encoded in the instruction memory in the following

format : h56212900

5 6 1 2 2 9 0 0
0101 0110 0010 0001 0010 1001 0000 0000

When this instruction comes to the controller and register file, the controller will interpret the opcode bits and will find that this is an add operation. The controller will output the corresponding control signals that set up the correct path for this operation. The register file will output the stored value for these corresponding registers. These data will be used as the source for the specified operations.

F. Convolution

In this proposed system the application of digital signal processor such as Linear convolution and Circular convolution of signals are verified.

Convolution is a mathematical way of combining two signal and form a third signal. It is a single most important part in the digital signal processing. Convolution is fundamental and important operation on signal processing and the Multiply and accumulator (MAC) operation is widely used in convolution. Convolution between of an input signal x[n] with a system having impulse response h[n] is given as,

$$x[n] \times h[n] = \sum_{k=-\infty}^{\infty} x[k]\,h[n-k]$$

III. PERFORMANCE ANALYSIS AND DISCUSSION

In this system convolution of two signals are evaluated on the terminal window tab, which as follows x[k]=251,302 and h[k]=4,-2 this two signals are stored in RAM.

The 32 bit DSP processor contain MAC unit and ALU, based on 32-bit floating point IEEE 754 standard, which was simulated and synthesized on Xilinx 14.7. , Where fig. no. 3 shows the device utilization summary. Where is obtained that Number of slice register utilization is 6% , number of slice LUT's is 33% utilization ,number used as logic 33% utilization , number of slice LUT's utilization is 65% , fig. no. 4 shows the power consumption of this system. The total power consumption is 0.016W. fig. no. 5 shows top level model , fig. no. 6 shows RTL schematic of proposed system. By comparing with previous system this system is power consumption and memory consumption device because of that the hardware required is less.

The design is able to achieve best power consumption over the past work in the same field.

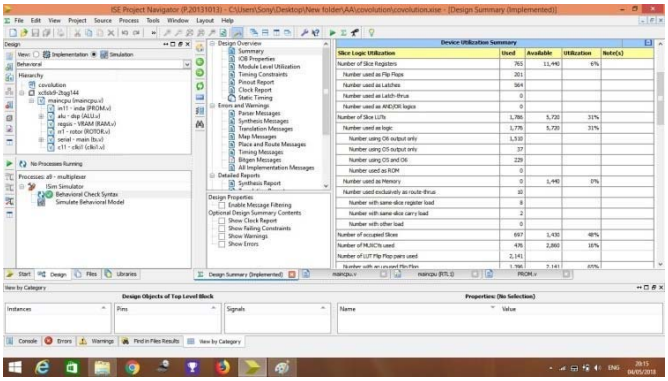

Fig. 3. Device utilization summary

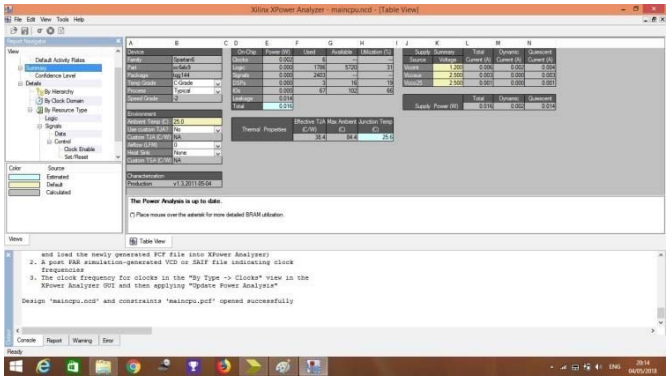

Fig. 4. Power consumption

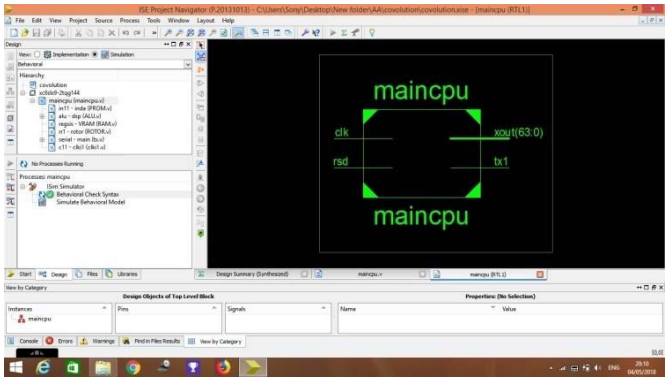

Fig. 5. Top level schematic view

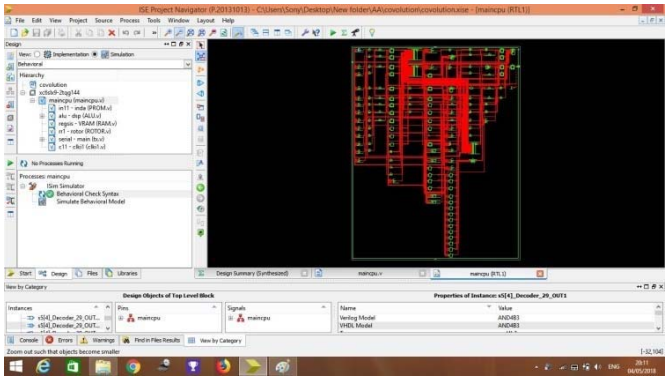

Fig. 6. RTL Schematic

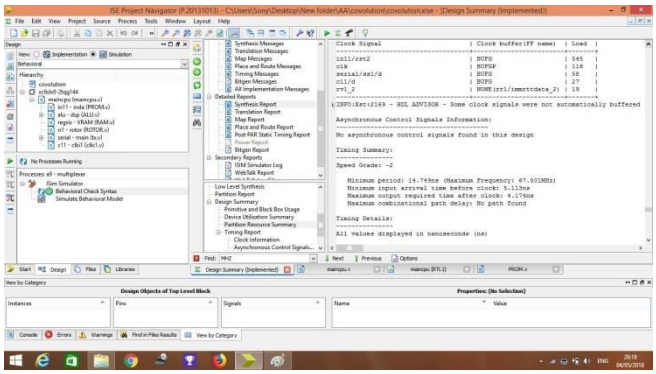

Fig. 7. Maximum Frequency

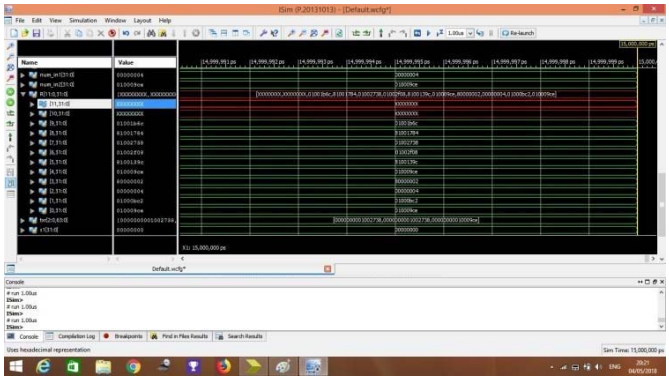

Fig. 8. Timing diagram of convolution

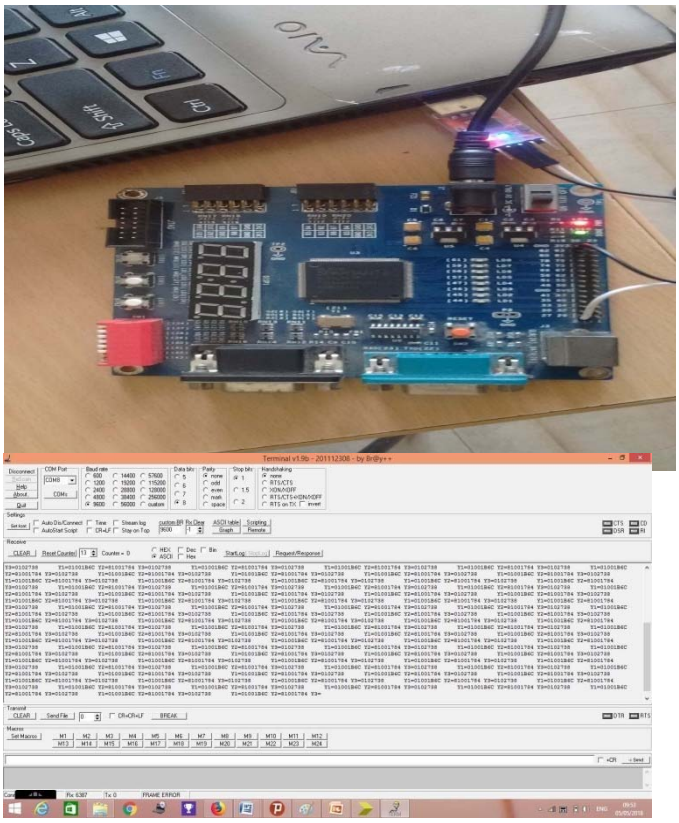

Fig. 10. Output on terminal window

IV. Conclusion

Single precision floating point unit digital signal processor MAC unit is designed and implemented using Xilinx 14.7 in this paper. The designed MAC unit conforms to IEEE 754 single precision floating point standard and designed is verified using fpu test bench.

The design has been able to achieve low power over the past work in the same field. The time and power required for this system is low. Because of its processing fast speed and hardware requirement is reduced, thereby reducing power consumption and delay. This architecture has become indispensable and increasingly important in many applications like signal processing, graphics and medical.

V. Future Scope

Digital signal processor plays important role in Digital communication and a day-to-day life the use of it and importance is increases. For better operations and fast handling processing are required for various applications. In future by using this processor we can implement different a various application of signal processing.

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