DOSonCHIP™

CD17B10

Memory Card Interface with File System

General Description

The DOSonCHIP™ CD17B10 provides an interface to industry standard removable memory cards, including microSDHC, microSD, miniSDHC, miniSD, SDHC, SD, and MMC cards. Both a physical interface and file system interface are included on the CD17B10. Simple file commands along with user data are sent to the CD17B10 over either of its UART, SPI, or I²C/SMBbus†. These file commands are used to navigate the file system directory, read data, or write data to the memory card using the industry standard FAT file system format, which is directly compatible with PC's, digital media players, digital cameras, etc.

Features

- UART / SPI / I²C/SMBus† to microSDHC / microSD / miniSDHC / miniSD / SDHC / SD / MMC memory card interface
- Hot swap of memory card
- FAT16 / FAT32 file system compatible
- Minimal external components
- Real Time Clock with file time-stamping
- 4 simultaneous open files
- 2.7V – 3.3V operation
- 5V tolerant I/O
- 5mA typical operating current
- 0.1µA typical shutdown current
- In System Upgradable
- Small PCB real estate: 4mm x 4mm
- Simplified PCB layout
- -40 to +85 °C Temperature Range
- RoHS compliant

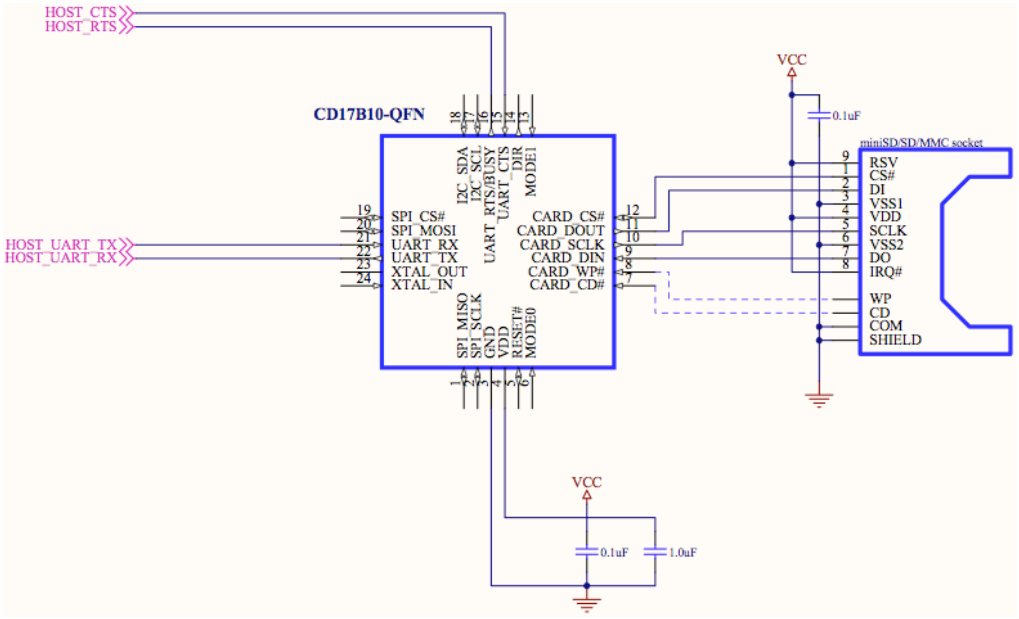
Packages

- 24-pin QFN
- 32-pin QFP

Applications

- Portable Consumer Electronics
- Mobile Handsets
- Digital Audio/Video Players
- Digital Cameras
- Laptop and Palm Computers
- Media Players
- Scientific Data Loggers

Typical Application Circuit



Typical Application Circuit (UART interface)

Table of Contents

1. System Overview

CD17B10 devices are fully integrated memory card controllers with a high-level file system stack. The CD17B10 devices contain a complete host serial interface to memory card physical interface. Reading and writing PC compatible files from/to widely available memory cards is executed using simple commands while retaining complete PC compatibility. Also included is the optional real-time clock (RTC) for keeping the current date and time and for time-stamping files. Finally, in-system firmware updating is available to provide new capabilities and future optimizations.

The host communications interface consists of either: UART, SPI, or I^2C/SMBus† serial interface. This interface accepts commands and data from the host and responds with status and data appropriately. Please see the DOSonCHIP host source code for command protocol and syntax.

The memory card physical layer interface is compatible with industry standard Secure Digital (SD) cards, Secure Digital High Capacity (SDHC) cards, and the Multi-Memory cards (MMC). The physical interface provides hot-swapping of memory cards and is designed to provide a simple PCB layout.

The file system stack is based upon the PC compatible FAT file system. Both FAT16 and FAT32 standards are supported. Reading, writing, and file/folder management is provided along with clock and interface option settings. Please see the DOSonCHIP host source code for the available commands.

The optional real-time clock (RTC) provides time keeping with date and leap year correction. This function is useful for tracking the last time a file was modified or created. The date and time is also available to the host for standard time-keeping functionality. This option is contingent with adding an external watch crystal.

The CD17B10 devices allow for in-system firmware upgrading. This allows future-proofing as well as the ability to add new and customized firmware capabilities.

2. Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		-55	–	125	°C
Storage Temperature		-65	–	150	°C
Voltage on any I/O pin or RESET# with respect to GND		-0.3	–	5.8	V
Voltage on VDD with respect to GND		-0.3	–	4.2	V
Maximum Total current through VDD and GND		–	–	500	mA
Maximim output current sunk by RESET# or any I/O pin		–	–	100	mA

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. DC Electrical Characteristics

Table 3-1: Global DC Electrical Characteristics

-40 to +85 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		VRST[1]	3.0	3.6	V
Supply Current: Active	VDD = 2.7V	–	5.0	–	mA
Supply Current Inactive		–	3.2	–	mA
Supply Current Shutdown		–	0.1	–	µA
Supply RAM Data Retention Voltage		–	1.5	–	V
Specified Operating Temperature Range	Industrial	-40	–	+85	°C
Notes: 1. Given in Table 2-1.					

Table 3-2: Reset Electrical Characteristics

-40 to +85 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
RESET# Output Low Voltage	IOL = 8.5 mA, VDD = 2.7 to 3.6 V	–	–	0.6	V
RESET# Input High Voltage		0.7 x VDD	–	–	V
RESET# Input Low Voltage		–	–	0.3 x VDD	V
RESET# Input Pullup Current	RESET# = 0.0V	–	25	40	µA
VDD Monitor Threshold (VRST)		2.40	2.55	2.70	V
Minimum RESET# Low Time to Generate a System Reset		15	–	–	µs
VDD Ramp Time	VDD = 0 to VDD = 2.7V	–	–	1	ms

Table 3-3: Port I/O DC Electrical Characteristics

VDD = 2.7 to 3.6 V, -40 to +85 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage	IOH = -3 mA, Port I/O push-pull	VDD - 0.7	–	–	V
	IOH = -10 μA, Port I./O push-pull	VDD - 0.1	–	–	
	IOH = -10 mA, Port I./O push-pull	–	VDD – 0.8	–	
Output Low Voltage	IOL = 8.5 mA	–	–	0.6	V
	IOL = 10 μA	–	–	0.1	
	IOL = 8.5 mA	–	1.0	–	
Input High Voltage		2.0	–	–	V
Input Low Voltage		–	–	0.8	V
Input Leakage Current	VIN = 0 V	–	25	40	μA

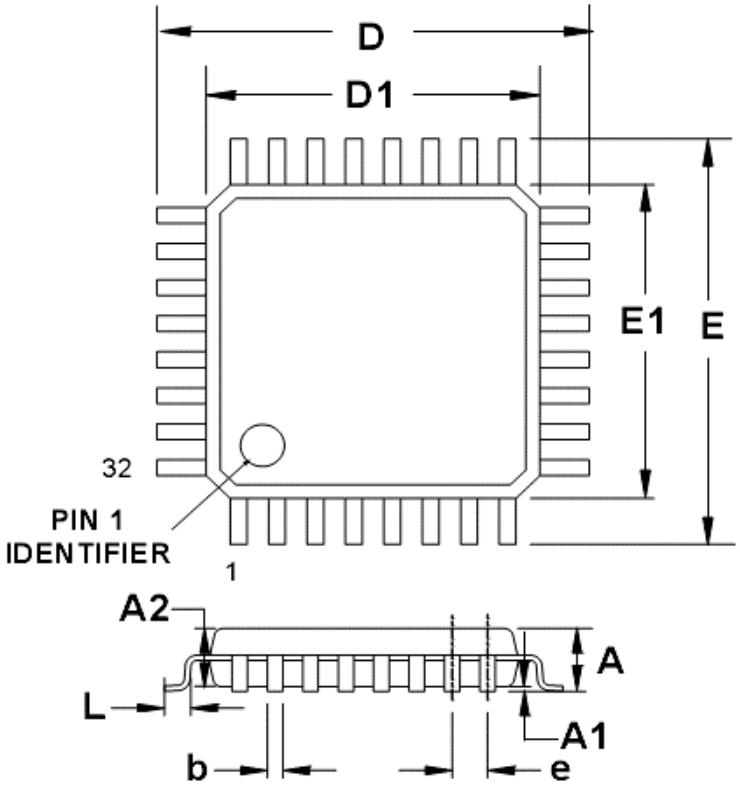
4. Pinout and Package Definitions

Table 4-1: Pin Definitions

Name	Pin Numbers		Type	Description
	QFP	QFN		
VDD	4	4	Power	Power Supply Voltage.
GND	3	3	Power	Ground.
RESET#	5	5	D I/O	Device Reset. External Reset input and open drain output of internal power-on reset & VDD Brownout Reset. Drive low for at least 10µs to manually reset device.
MODE0	6	6	D I	Device Com Port Select 0. Used in conjunction with MODE1 pin. See rest of datasheet for details.
SPI_SCLK	2	2	D I	SPI Slave Port Clock Input.
SPI_MISO	1	1	D O	SPI Slave Port Data Output.
XTAL_IN	32	24	A In	External Clock Input. Connect to watch crystal for Real Time Clock function; otherwise leave unconnected or connect to Ground.
XTAL_OUT	31	23	A Out	External Clock Output. Connect to crystal for Real Time Clock function; otherwise do not connect.
UART_TX	30	22	D O	Asynchronous Transmitter Output.
UART_RX	29	21	D I	Asynchronous Transmitter Input.
SPI_MOSI	28	20	D I	SPI Slave Port Data Input.
SPI_CS#	27	19	D I	SPI Slave Port Chip Select.
I2C_SDA	26	18	D I/OC	I^2C /SMBus Slave Port Data.
I2C_SCL	25	17	D I/OC	I^2C /SMBus Slave Port Clock.
UART_RTS/BUSY	24	16	D O	Request To Send Output /Busy Output.
UART_CTS	23	15	D I	Clear To Send Input.

Name	Pin Numbers		Type	Description
	QFP	QFN		
DIR	22	14	D I	Direction. Used to indicate data direction for host-chip communications.
MODE1	21	13	D I	Device Com Port Select 1. Used in conjunction with MODE0 pin. See rest of datasheet for details.
RSVD1	20	–		Reserved Pin 1. Do not connect
RSVD2	19	–		Reserved Pin 2. Do not connect
CARD_CS#	18	12	D I	Memory Card Select/Detect.
CARD_DOUT	17	11	D O	Memory Card Data Output.
CARD_SCK	16	10	D O	Memory Card Clock Output.
CARD_DIN	15	9	D I/O	Memory Card Data Input.
CARD_WP	14	8	D O	Memory Card Write Protect Input. Connected to Memory Card Socket. Optional.
CARD_CD#	13	7	D I	Memory Card Detect Input. Connected to Memory Card Socket. Optional.
RSVD3	12	–		Reserved Pin 3. Do not connect.
RSVD4	11	–		Reserved Pin 4. Do not connect.
RSVD5	7	–		Reserved Pin 5. Do not connect.
RSVD6	8	–		Reserved Pin 6. Do not connect.
RSVD7	9	–		Reserved Pin 7. Do not connect.
RSVD8	10	–		Reserved Pin 8. Do not connect.

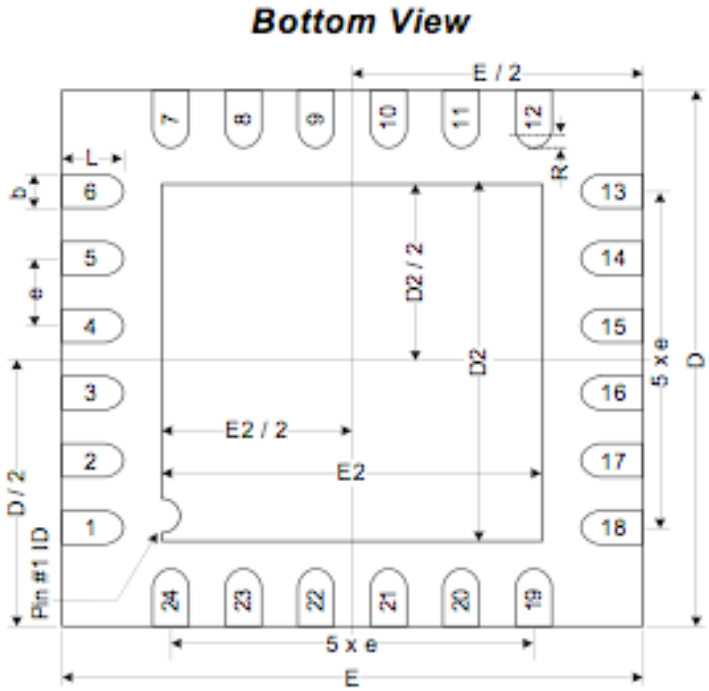
Table 4-2: QFP Package Dimensions



Package Dimensions

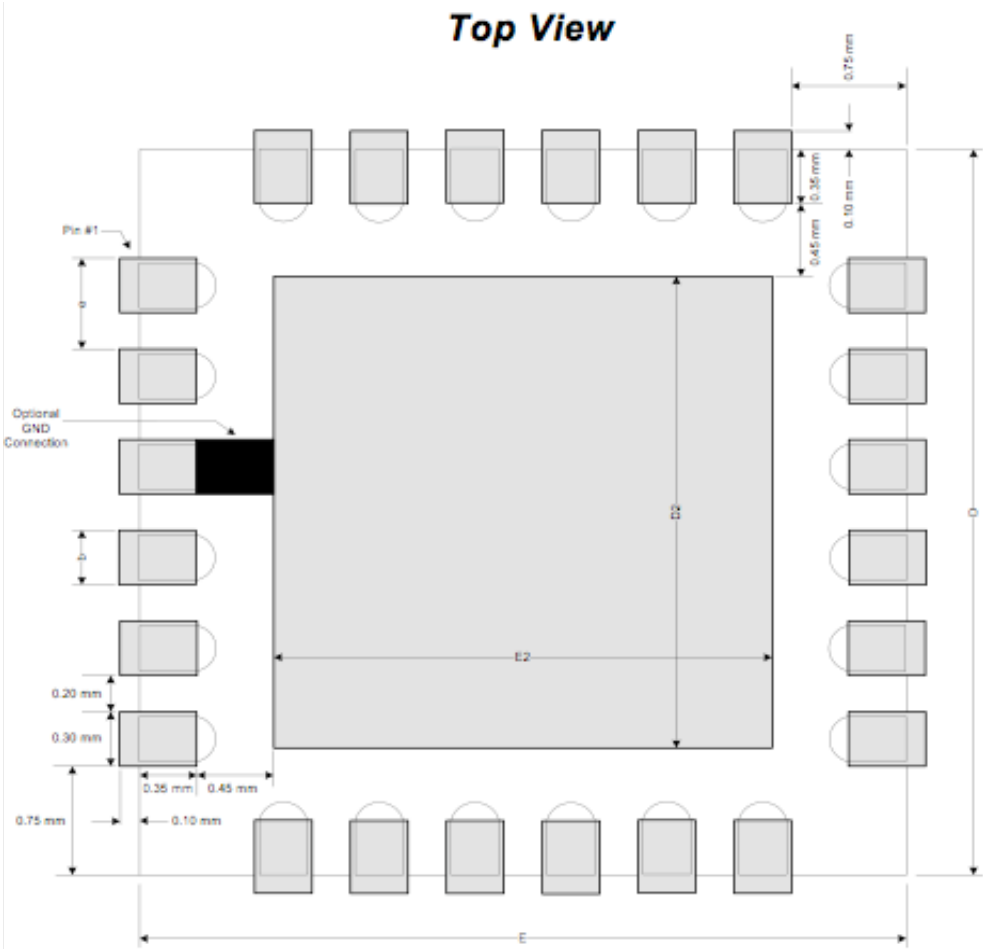
	MM		
	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	-	9.00	-
D1	-	7.00	-
e	-	0.80	-
E	-	9.00	-
E1	-	7.00	-
L	0.45	0.60	0.75

Table 4-3: QFN Package Dimensions



	MM		
	MIN	**TYP**	**MAX**
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	—	0.50	—
A3	—	0.25	—
b	0.18	0.25	0.30
D	—	4.00	—
D2	2.50	2.60	2.70
E	—	4.00	—
E2	2.50	2.60	2.70
e	—	0.50	—
L	0.35	0.40	0.45
N	—	24	—
ND	—	6	—
NE	—	6	—
R	0.09	—	—

Table 4-4: QFN Landing Diagram



5. Reset & Power-Up Configuration

The RESET# pin is an open-drain bidirectional pin that provides input for an external reset and an output to signal an internal reset. The internal resets consist of a power-on reset and a power-fail reset. The three reset sources are connected in a "wired OR" configuration.

5.1. Power-on Reset

During power-up, the RESET# line will be held low until a short delay after VDD settles above VRST.

Note that if the VDD Ramp Time (see Table 3-2) is greater than 1ms then an external voltage supervisor must be used to prevent possible corruption of the firmware memory. In the event the firmware memory becomes corrupt, the CD17B10 may become unstable/unusable and it may no longer be possible to perform In System Updates.

5.2. Power-fail Reset

Whenever VDD drops below VRST, whether due to a power transition or power irregularity, the CD17B10 will go into reset and drive the RESET# line low until a short delay after VDD settles above VRST.

5.3. External Reset

The RESET# signal pin can be driven low to reset the CD17B10. If the external driving signal has a high state, then a series resistor should be used to prevent a short condition when the RESET# line outputs a low state. See Table 3-2 for the minimum time that RESET# must be held low.

5.4. Pin States During Reset

During any reset event and while the RESET# line is low, the CD17B10's remaining signal pins are placed in a high impedance state with weak pull-up resistors.

5.5. Reset Wake-up

If at any time the CD17B10 is placed in Shutdown to minimize power consumption, it can only be woken-up by a reset event.

5.6. Reset Firmware Integrity Verification

Immediately after a hardware reset, the Bootloader firmware (version 1.1) is executed and performs an integrity check to verify there is no corruption of the firmware flash. If there is any corruption, the in-system update will automatically commence to update the firmware (see section 8.2).

6. Communication Ports

6.1. Host Ports

There are three physical communication ports that can be used to interface to the CD17B10:

Table 6-1: Physical Communication Ports

Physical Port	Bootloader 1.x	Firmware 1.x	Firmware 2.x
UART	Supported	Supported	Supported
SPI	Not Supported	Supported	Supported
I^2C/SMBus	Not Supported	Not Supported	Planned

Only one Host Port can be used at a time and is selected at reset using the MODE0 and MODE1 pins. The state of the MODEx pins must be maintained during operation of the CD17B10. If a change is required during operation, make sure the CD17B10 has completed any pending operations, all files are closed, then change the MODEx pins and generate a reset event (see Section 5).

A change in either or both of the MODEx pins at any other time may lead to unpredictable results including the possibility of lost application data.

Use the following table to select the desired Host Port:

Table 6-2: Communication Port Selection via MODEx Pins

MODE0	MODE1	Host Port
Open/VCC	Open/VCC	UART
Open/VCC	GND	SPI (slave)
GND	Open/VCC	Start Bootloader
GND	GND	I^2C/SMBus address 0

6.2. UART

The UART, or Universal Asynchronous Receiver & Transmitter, provides asynchronous digital serial communications with the host. The UART physical interface consists of the following signal pins:

- UART_RX : Commands & data sent from host to the DOSonCHIP device.
- UART_TX : Commands & data sent from the DOSonCHIP device to the host.
- UART_CTS : Handshake signal from the host to the DOSonCHIP device. This signal is set to logical 1 (high) by the host to prevent the DOSonCHIP device from sending bytes to the host. This signal is optional for Firmware 2.x and if not used it must be tied to ground (low). This signal should be used by the Bootloader when updating firmware.
- UART_RTS : Handshake signal from the DOSonCHIP device to the host. It is set to logical 0 (low) when the DOSonCHIP device is ready to accept data from the host. This signal is optional for Firmware 2.x and asserts when a packet transfer is ready and stays asserted until the packet transfer is complete. The Bootloader uses this signal for individual byte transfers.

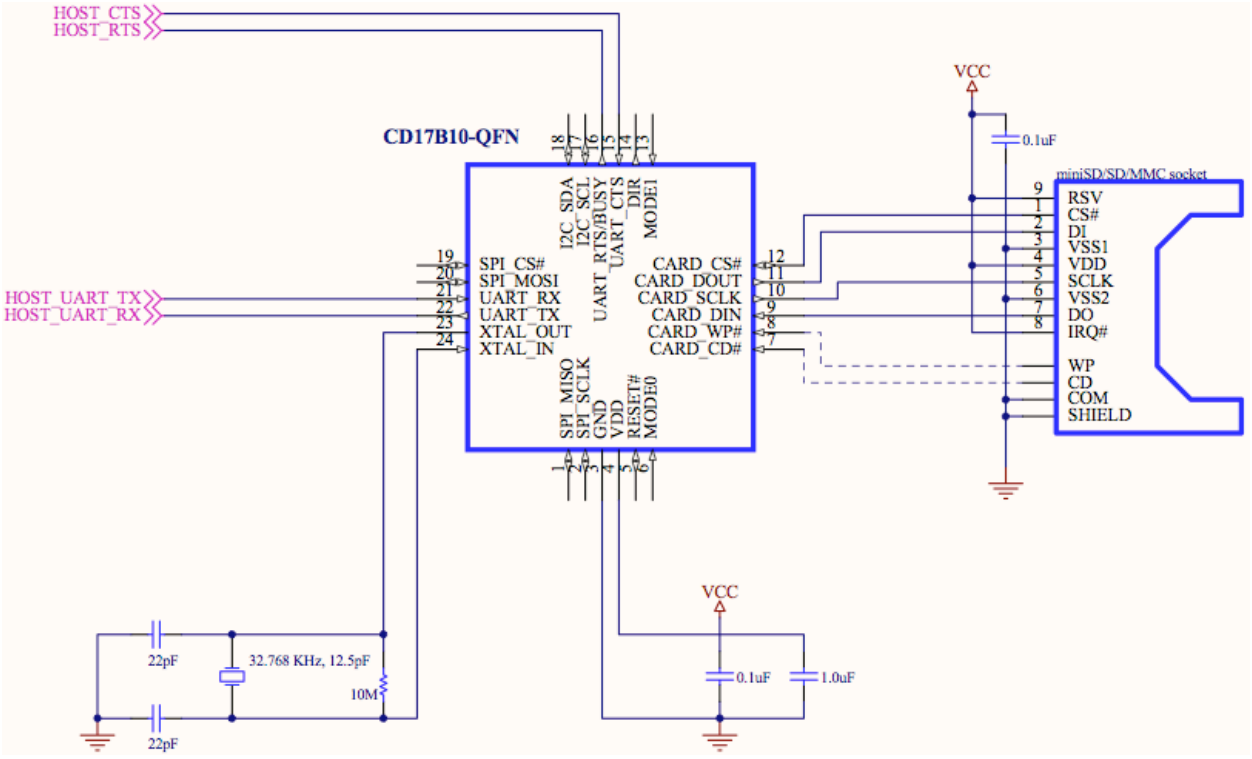
Baud Rate

The baud rate is selected after the device comes out of reset and the UART or Bootloader is selected via the MODEx pins. The DOSonCHIP device baud rate is set using autobaud detection. 2 consecutive carriage returns (<CR>) are required to set the baud rate. The first carriage return sets the baud rate and the second carriage return is used to confirm that the baud rate is correct. The DOSonCHIP device will wait until two consecutive error free carriage return's are received at the same baud rate before sending the ready prompt. Please see the DOSonCHIP host source code for UART baud rate initialization.

The allowable baud rates are:

- 1200
- 2400
- 9600
- 28800
- 38400
- 57600
- 115200
- 230400

Figure 6-1: Application Circuit with UART interface and Real Time Clock



6.3. SPI

The SPI, or Serial Peripheral Interface, provides slave synchronous serial communications with the host. The SPI physical interface consists of the following signal pins:

- SPI_MOSI : Commands & data sent from host to the DOSonCHIP device.
- SPI_MISO : Commands & data sent from the DOSonCHIP device to the host.
- SPI_CLK : Synchronous clock signal from host.
- SPI_CS# : SPI port select signal from host. When this set to logical 1 (high), the SPI port will be disabled and SPI_MISO will be placed in a high impedence state. When there is a transition from logical 1 (high) to logical 0 (low), it resets the DOSonCHIP bit counter; therefore, it should not be tied to logical 0 (low) as a default since noise on the SPI_CLK line could offset the DOSonCHIP bit counter for all subsequent byte transfers.
- BUSY : Handshake from the DOSonCHIP device to the host. It is set to logical 0 (low) when the DOSonCHIP is ready to accept data from the host. This signal is optional for Firmware 2.x and asserts when a packet transfer is ready and stays asserted until the packet transfer is complete.
- DIR : Firmware 1.x only: data direction indicator line from the DOSonCHIP device to the host. It is set to logical 1 (high) to indicate the DOSonCHIP device is in a mode to accept data from the host. It is set at logical 0 (low) to indicate the DOSonCHIP device is in a mode to send data to the host. It is not used for Firmware 2.x.

Figure 6-2: Application Circuit with SPI interface (without Real Time Clock)

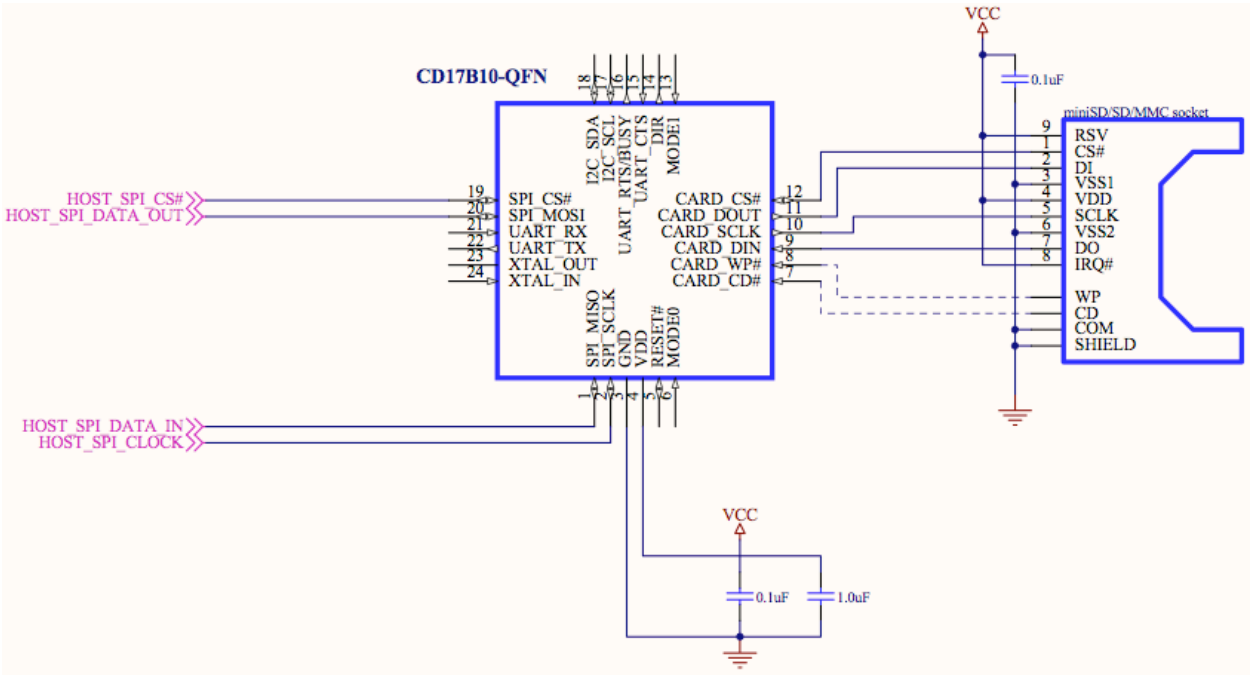


Figure 6-3: SPI Slave Timing

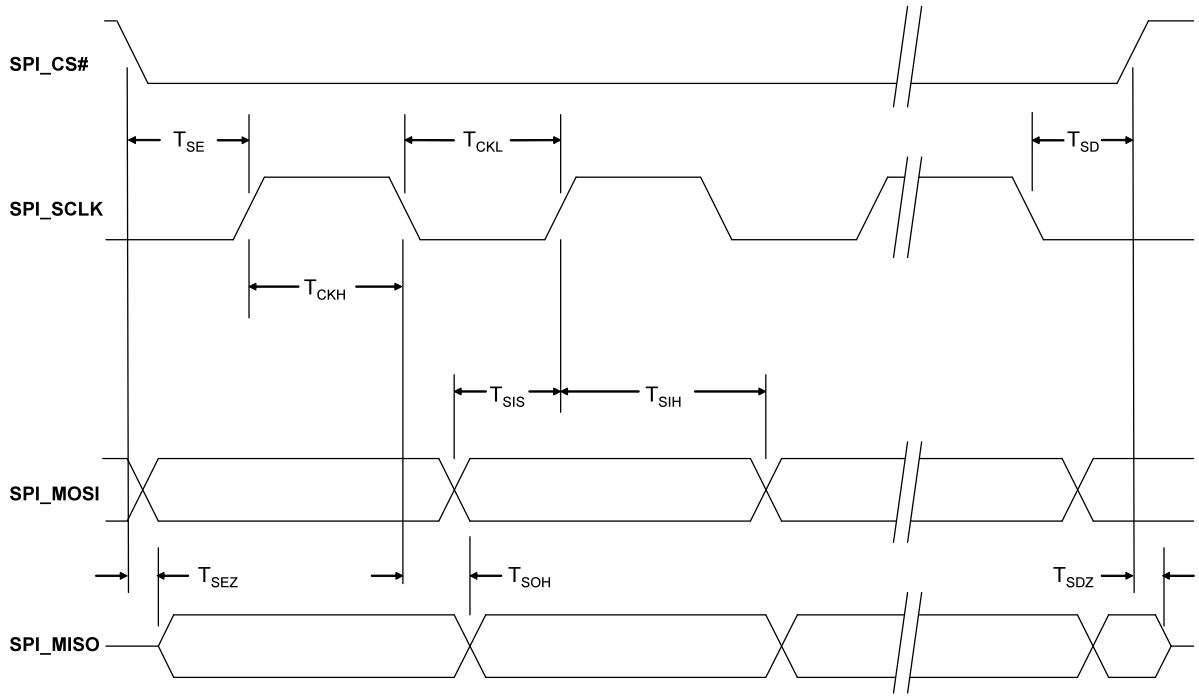


Table 6-3: SPI Timing Parameter Table

Parameter	Description	Min	Max	Units
F_{CK}	SPI_CLK frequency Firmware = 1.x Firmware = 2.x	 0 0	 1.5 2.4	MHz
T_{CK}	SPI_SCLK period	$1/F_{CK(MAX)}$	–	ns
T_{SE}	SPI_CS# Falling to First SPI_SCLK Edge	0.2 x $T_{CK(MIN)}$	–	ns
T_{SD}	Last SPI_SCLK Edge to SPI_CS# Rising	0.2 x $T_{CK(MIN)}$	–	ns
T_{SEZ}	SPI_CS# Falling to SPI_MISO Valid	–	0.4 x $T_{CK(MIN)}$	ns
T_{SDZ}	SPI_CS# Rising to SPI_MISO High-Z	–	0.4 x $T_{CK(MIN)}$	ns
T_{CKH}	SPI_SCLK High Time	0.5 x $T_{CK(MIN)}$	–	ns
T_{CKL}	SPI_SCLK Low Time	0.5 x $T_{CK(MIN)}$	–	ns
T_{SIS}	SPI_MOSI Valid to SPI_SCLK Sample Edge	0.2 x $T_{CK(MIN)}$	–	ns
T_{SIH}	SPI_SCLK Sample Edge to SPI_MOSI Change	0.2 x $T_{CK(MIN)}$	–	ns
T_{SOH}	SPI_SCLK Shift Edge to SPI-MISO Change	–	0.4 x $T_{CK(MIN)}$	ns
T_{SLH}	Last SPI_SCLK Edge to SPI-MISO Change (Clock Phase 1 only)	0.6 x $T_{CK(MIN)}$	0.8 x $T_{CK(MIN)}$	ns

6.4. I²C/SMBus†

The I²C/SMBus provides synchronous serial communications with the host. It is compatible with the I²C serial bus and compliant with System Management Bus Specification, version 1.1. It functions in slave mode only (host is master). The I²C/SMBus physical interface consists of the following signal pins:

- I2C_SDA : bidirectional slave port data line between host & DOSonCHIP device
- I2C_SCL : bidirectional slave port clock line between host & DOSonCHIP device

The maximum clock speed is 2.4MHz.

The maximum rise and fall times must not exceed 300ns and 1000ns, respectively.

DOSonCHIP may temporarily hold the I2C_SCL line low to extend the clock low period (per I2C and SMBus specifications). This depends upon the firmware and host clock speed.

7. Real Time Clock (RTC)

The Real Time Clock is an optional feature that provides the current date & time.

7.1. Hardware Configuration

The RTC requires a 32.768 KHz, 50% duty cycle clock to function. This can be provided with a common watch crystal.

7.1.1. External Crystal

Connect a tuning-fork crystal of 32.768 KHz with a recommended load capacitance of 12.5 pF as shown in Figure 6-1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal.

7.1.2. No Clock/Disable RTC

If the RTC function is not needed, then either leave XTAL_IN and XTAL_OUT unconnected or connect the XTAL_IN pin to GND and leave the XTAL_OUT pin unconnected.

7.2. Setting the Date & Time

When the RTC is disabled, the set time & date will remain static. This is useful for time stamping files with a specific date & time.

See the DOSonCHIP host source code for date and time commands.

7.3. Resetting of the Date & Time

The set date and time will be reset if either of the following conditions occur:

- The CD17B10 is placed into Shutdown mode (via host command), or
- The CD17B10 is reset.

8. In-System Updates

The DOSonCHIP device can be updated with new firmware.
Firmware updating takes place over the UART interface using Ward Christensen's 1977 public domain XModem transfer protocol as documented in:

[1] "XModem / YModem Protocol Reference" by Chuck Forsberg [1988-10-14]
[2] http://www.commonsoftinc.com/Babylon_Cpp/Documentation/Res/KRefFrame.htm

The following procedure uses Windows XP HyperTerminal to upload new firmware from 1.x to 2.x (and uses hardware handshaking).
Follow similar guidelines for additional firmware updates:

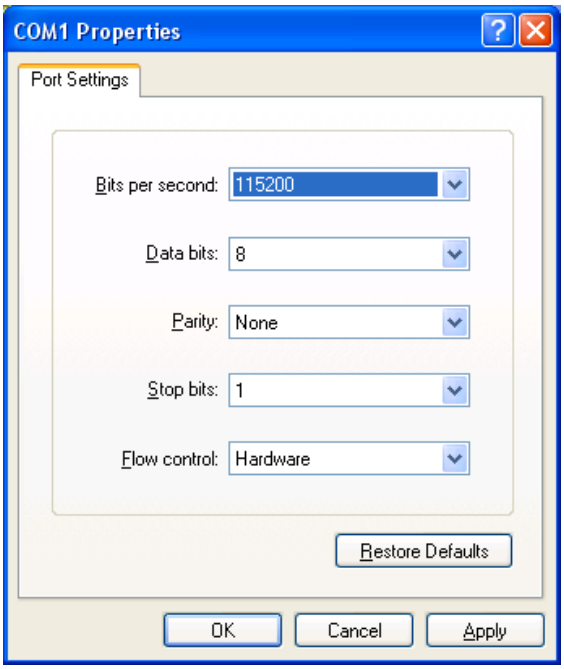
8.1. Windows HyperTerminal Setup

1. Launch HyperTerminal on the PC (Start>All Programs>Accessories<Communications>HyperTerminal).

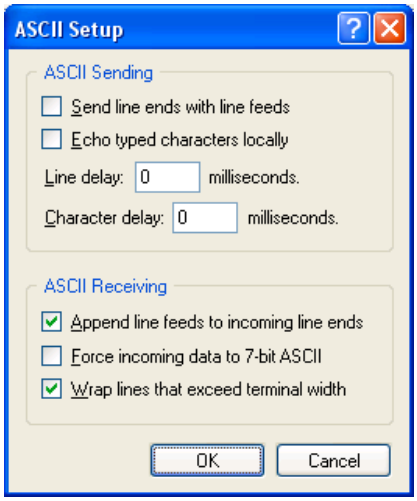
2. At the "New Connection" prompt, choose a profile name for this connection:

3. Choose your RS-232 serial connection COM port at the next prompt:

4. At the next prompt, choose the serial port speed (see section 6.2 for allowable serial speeds), and choose the settings as shown:

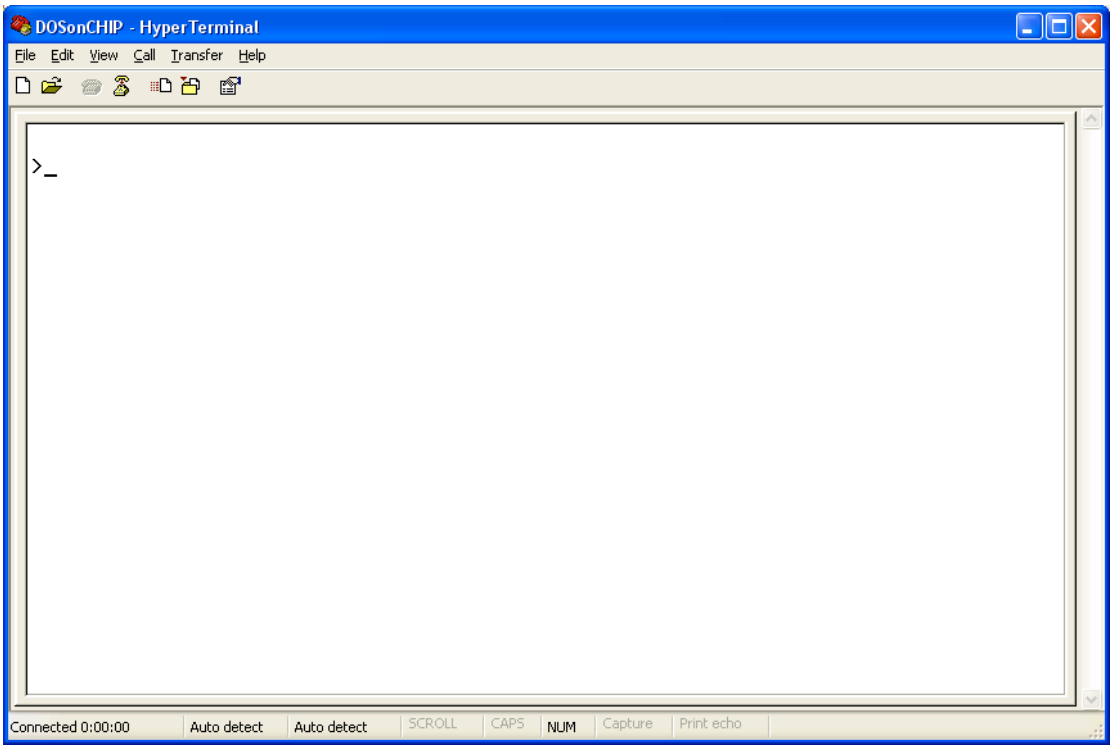


5. Firmware 1.x ONLY: On the menu bar, select "File>Properties" and click on the "Settings" tab and select the "ASCII Setup…" button. Then choose the settings as shown:



Make sure you press "OK" for both the "ASCII Setup" prompt AND the previous prompt for the settings to take effect.

6. Firmware 1.xx ONLY: On the PC's keyboard, press the "Enter/Return" button a minimum of two consecutive times until you see a returned character (do not press return after receiving the character). This step communicates and sets the serial baud rate with on the CD17B10. For firmware 1.x, you should see the ">" character:

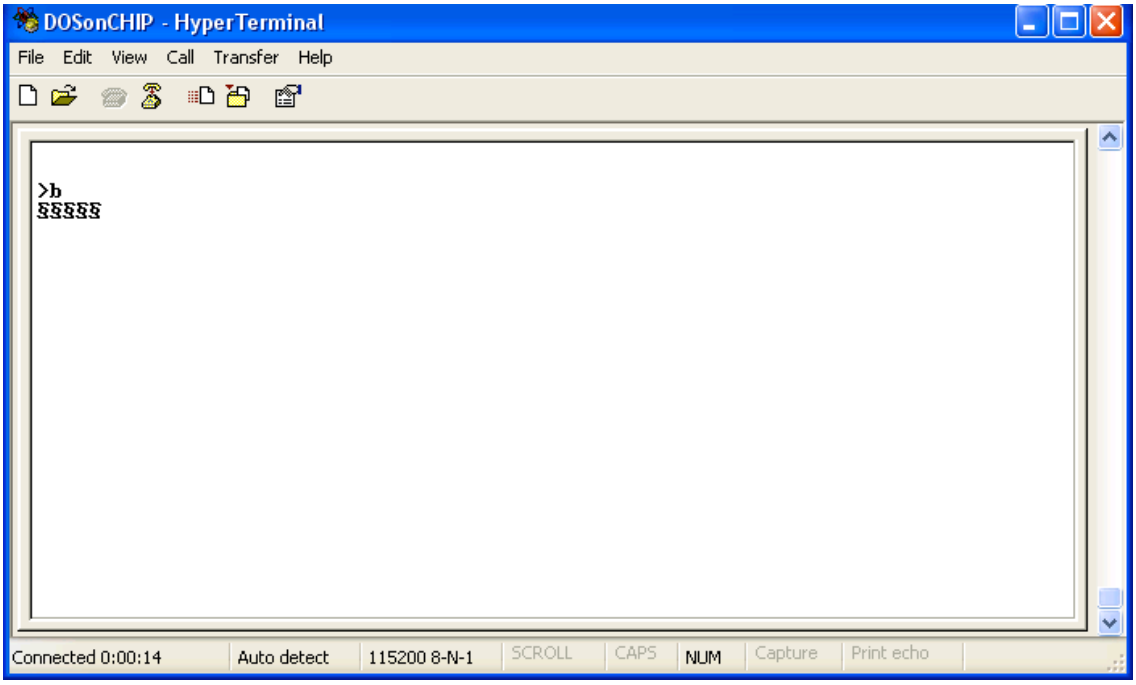


7. Continue to the next section (File Transfer).

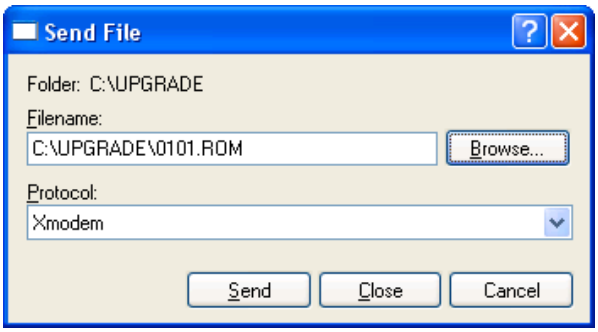
8.2. File Transfer

1. There are 2 ways to manually initiate the Bootloader
   - PREFERRED: Set appropriate pins and reset the device (see Section 6.1), or
   - Use the DOSonCHIP command. For firmware 1.x, type "b" and hit Enter/Return key. For firmware 2.xx, type "BBBBB" (note do NOT press Enter/Return key). NOTE: for firmware 2.xx, there have been issues with failure to complete Xmodem download using Hyperterminal. If this happens, use the preferred/previous method to invoke the bootloader.

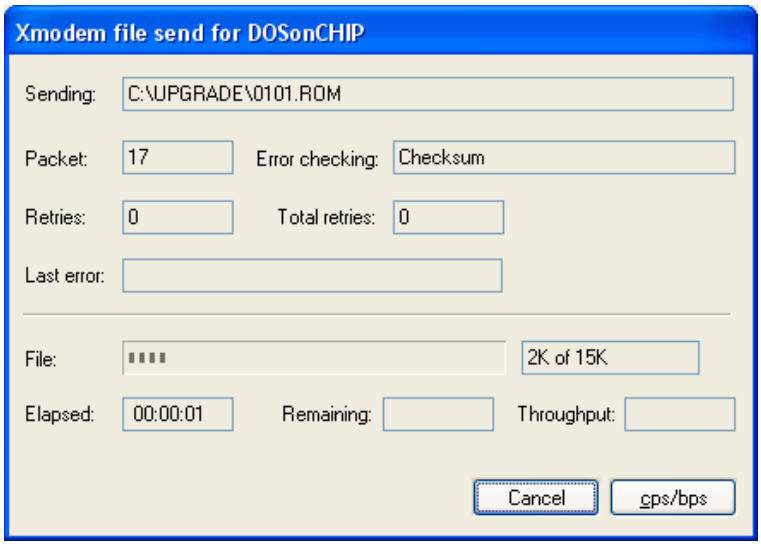
2. Enter two carriage return's (press the Enter/Return key twice) to complete the CD17B10's autobaud detection. There should be a new '§' symbol being shown about every second.



3. Select Transfer>Send File… on the Menu Bar and at the Send File prompt, select the firmware upgrade file (.ROM file), select the Xmodem protocol and press the "Send" button



4. The "Xmodem file send" progress display should show the uploading process



5. After the file transfer completes and there are no errors, the new firmware will be executed. Enter two <CR>'s (press the Enter key twice) to complete the CD17B10's autobaud detection.

9. Ordering Information

Part Number	Supply Voltage	Temperature Range	Package	Packing
CD17B10-QFP	2.7V to 3.3V	Industrial	QFP32	Bulk
CD17B10-QFN	2.7V to 3.3V	Industrial	QFN24	Bulk

- Industrial Temperature Range: -40 to +85 °C
- Tape & Reel packing upon request with volume minimums

10. Document Change List

Revision	Date	Comments
0.8	4/1/2006	Initial Distribution.
1.0	3/14/2008	Changed title & added firmware support table (6.1). Fixed error (6.2). Updated SPI timing parameters (6.3). Updated spec (6.4). Added RTC date & time clock reset (7.3). Added reference to User Guide (8). Updated schematics. Updated table & figure references. Updated company contact information. Removed "Preliminary" status. Updated copyright.
1.1	4/19/2008	Updated Table 3-2 formatting. Updated reference to Table 3-2 (5.1 & 5.3). Updated 5.1.
2.0	10/31/2008	Changed chip reference from CD17Bxx to CD17B10. Updated Document for Firmware 2.x. Updated reference for SDHC cards. Added Table 4-2 (QFP package dimensions). Added Table 4-3 (QFN package dimensions). Added Table 4-4 (QFN landing diagram). Updated UART & SPI signal pin definitions. Added baud rate description to UART definition. Replaced reference to DOSonCHIP User Guide with DOSonCHIP host source code. Added MODEx for Bootloader. Updated Packing Order information. Updated In-System Updates. Updated Contact Information.
2.1	12/25/2008	Updated Schematics to include extra decoupling capacitor
2.1.1	02/20/2009	Updated 7.1.1. Updated copyright. Updated bootloader description.
2.1.2	03/20/2009	Updated 6.2 & 6.3 with respect to the UART_RTS/BUSY functional description.
2.1.3	03/21/2009	Added section 5.6
2.1.4	04/07/2009	Fixed error in Table 6-3 (SPI Timing Parameter Table)

11. Contact Information

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†Planned feature (I²C/SMBbus compatibility) not currently available.