EECS 418 Final Report
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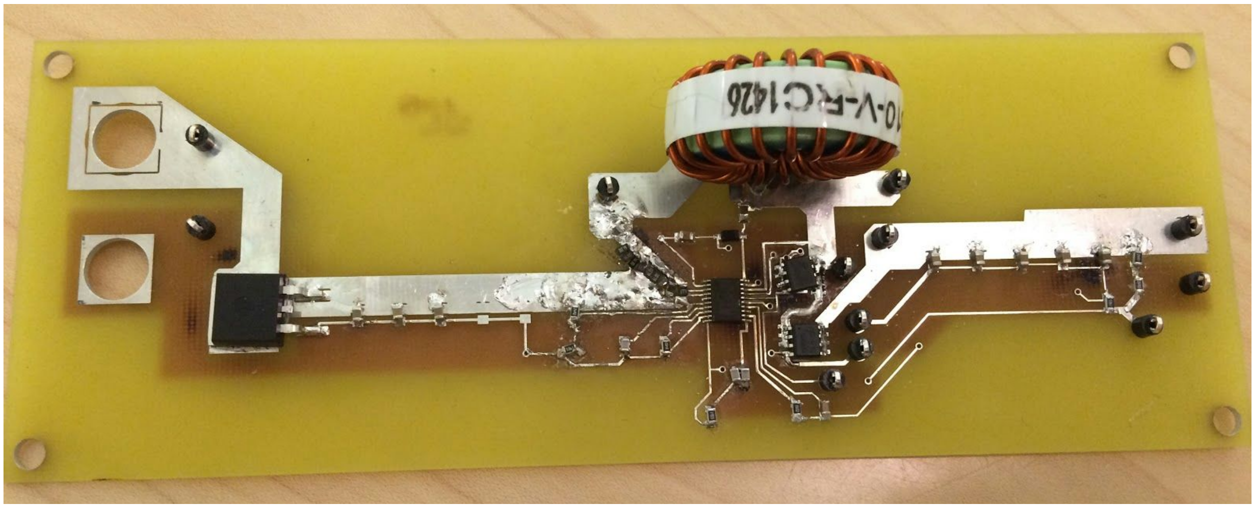


Figure 1: Final Working Boost Converter

Problems Encountered
The first problem we encountered before we even started testing was that we forgot a couple parts we needed for our board. One was C_{res}, which was meant to be 0.47μF. Upon looking up this part on the datasheet to see if we could use something else we had as a replacement, the datasheet said 0.47μF is just a typical value used and something a little larger can be used. We had extra 0.68μF capacitors so we used one of those in place of the 0.47μF. The other missing component was the 50kΩ resistor for the feedback, but we just used two 25kΩ resistors in series instead (essentially the same).

The first problem we encountered while testing our first board was that the current was being limited. In other words, we were getting a steady 12 V output voltage with minimal ripple, but our current was only at 50mA. After talking with Aaron, we discovered our error to be using a physical surface mount resistor on our board. The solution he suggested was just to use the electronic load and remove the 6Ω surface mount resistor we were using. In Figure 1, the fifth output capacitor is placed where the 6Ω load used to be.

The next problem was that when we used the electronic load for a constant resistance load of 6Ω, one of our MOSFETs would overheat and start smoking. We decided that we must be putting too much current/power through that MOSFET. In order to avoid this, we started at a load resistance much higher than 6Ω (100Ω to be exact) and then would step down the resistance from there. We also increased our output capacitance from five 10μF capacitors (50μF) to two 10μF and three 22μF capacitors (86μF) and added a sense resistor in parallel, upon suggestion from Aaron.

Similar to the previous issue we were having, while stepping down the load resistance, we discovered that our circuit stopped working after decreasing past a certain resistance. At this point, we also noticed quite a bit of ripple in the waveforms we were seeing, so we added two more 4.7μF capacitors at the input. To solve the issue with the circuit shutting off after dropping below a certain load resistance value, Aaron suggested that we change our values for R_{comp} and C_{comp} because the problem was likely due to the controller. After testing a few combinations of R_{comp} and C_{comp} based on the relationship between the two outlined in the controller's datasheet, the best output resulted from an R_{comp} of 5.36kΩ, instead of 70kΩ, and C_{comp} of 44nF, instead of 1nF. We also noticed that changing the value of C_{comp} affected the output much more than the value of R_{comp}.

After all of these changes, we were still only able to step down to 9Ω or 10Ω (results varied with each trial). In order to get to 9Ω or 10Ω in the first place, we had to continue adding sense resistors in parallel. We got up to six parallel sense resistors, three 18mΩ and three 6mΩ resistors, before we couldn't fit anymore than that. We tried adding more (see Figure 1), but the last three didn't end up getting electrically connected. However, each time we added another resistor, we got closer and closer to our desired value of 6Ω and 4A. This leads us to believe that we could have met design specifications if we had a smaller (in value, not size) sense resistor because our controller still gave us a perfect average output voltage of 12.0V with a ripple within design specifications and drawing close to exactly 6V. So, the only thing that was missing was the current, which was being limited by the sense resistance, which was why we could not reach the desired output power of 24W.

Additionally, our reverse battery protection did not work during the in-lab demonstration, but we determined that all we needed to do was replace the PMOS with a new one in order to get the reverse protection working (see Figure 2 below).

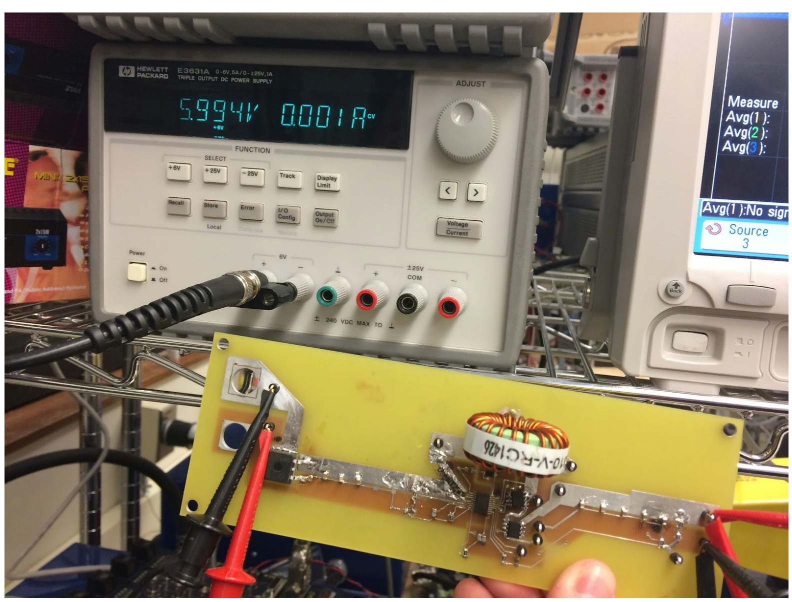


Figure 2: Proof of Reverse Battery Protection Implementation

Changed Components

R_{UV1}	12.5kΩ ⇒ 5.36kΩ
R_{UV2}	50kΩ ⇒ 24.9kΩ
R_{comp}	70kΩ ⇒ 5.36kΩ
R_{slope}	1222kΩ ⇒ 16kΩ
R_{sense}	18mΩ ⇒ 3 // 18mΩ, 3 // 6mΩ = 1.2 mΩ
R_{load}	6Ω ⇒ electronic load 10Ω
C_{comp}	1nF ⇒ 2 x 22nF
C_{res}	.47μF ⇒ .68μF
C_{in}	4.7μF ⇒ 3 x 4.7μF
C_{out}	47μF ⇒ 2 x 10u + 3 x 22μF
L	220μH ⇒ 56μH

New Component Analysis

$$\Delta i_L = \frac{D(V_{in} - I_L R_{sens} - V_{M1})}{2 f_s L} = \frac{0.5284(6-4.241\cdot 0.0012 - 0.5284\cdot 4.241\cdot 11.5\times 10^{-9})}{2\cdot 481\times 10^3\cdot 56\times 10^{-6}} = 58.8mA$$

$$\Delta v = \frac{DV}{2 f_s RC} = \frac{0.5284\cdot 12}{2\cdot 481\times 10^3\cdot 10\cdot 86\times 10^{-6}} = 7.66mV$$

$$P_{L,\,cond} = \tfrac{1}{2} I_{max}^2 R_{dc} = \tfrac{1}{2} 4.300^2 \cdot 0.017 = 0.157W$$

$$P_{C,\,esr} = \tfrac{1}{2} ESR \cdot I_{Cmax}^2 = \tfrac{1}{2} 0.0005013 \cdot 0.0588^2 = 86.7\mu W$$

$$P_{NMOS,\,cond} = D(I_L^2 + \tfrac{1}{3}\Delta i_L^2) R_{ds(on)} = 0.5284(4.241^2 + \tfrac{1}{3}.0588^2)0.0088 = 83.6mW$$

$$P_{NMOS,\,rr} = (V_M^{off} I_M^{on} t_{rr} + V_M^{off} Q_{rr}) f_s$$

$$= (0.5284 \cdot 4.241 \cdot 11.5 \times 10^{-9} \cdot 4.241 \cdot 11.5 \times 10^{-9} + 0.5284 \cdot 4.241 \cdot 11.5 \times 10^{-9} \cdot 12.5 \times 10^{-9}) \cdot 481 \times 10^3$$

$$= 0.76nW$$

$$P_{NMOS,\,sw} = \tfrac{1}{2}(V_M^{off} I_M^{on} t_{on} + V_M^{off} I_M^{on} t_{off}) f_s$$

$$= \tfrac{1}{2}(0.5284 \cdot 4.241 \cdot 11.5 \times 10^{-9} \cdot 4.241 \cdot 5 \times 10^{-9} + 0.5284 \cdot 4.241 \cdot 11.5 \times 10^{-9} \cdot 4.241 \cdot 17 \times 10^{-9}) \cdot 481 \times 10^3$$

$$= 0.58nW$$

$$P_{Rsense} = I_L^2 R_{sense} = 4.241^2 \cdot 0.0012 = 21.6mW$$

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{24}{24 + 0.346} = 98.6\%$$

Test Results

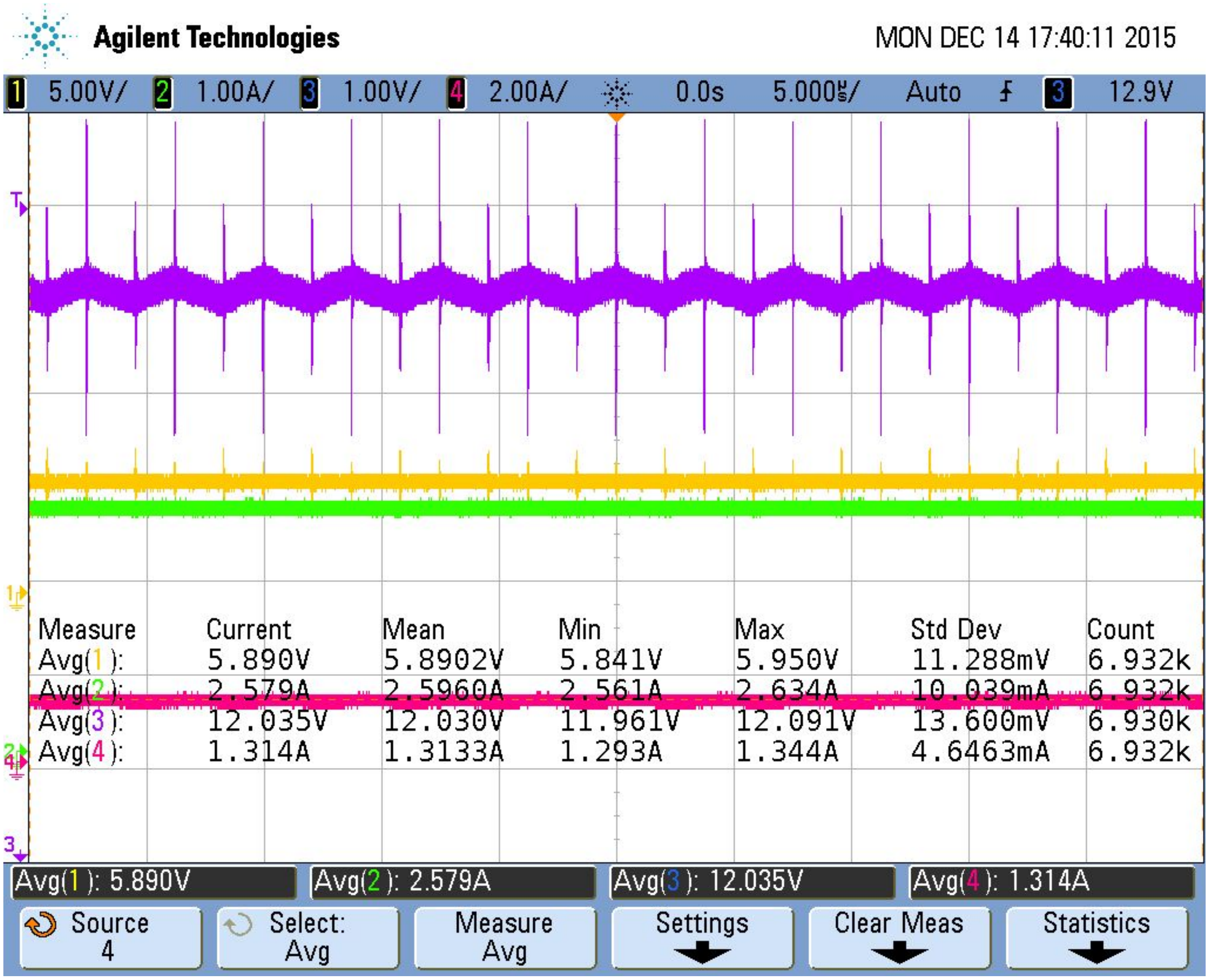


Figure 3: Output and Input Current/Voltage Plot

Figure 3 shows our final results relating to the design criteria. The resistive load is set to 10Ω, with an input voltage of nearly 6V. We observe an output voltage ripple (the standard deviation) of roughly 13mV , or roughly 0.1% of the output voltage. Output current ripple was roughly 4.64mA, or 0.3% of the output current. As mentioned before, our design meets the project criteria of allowing less than 10% and 5% output voltage and current ripple, respectively.

Using the data from Figure 3, we also calculated an efficiency of 97% from measuring the input and output currents with the Hall effect sensors, although during the in-lab demonstration, the output current was measured on the electronic load and this was measured to be slightly lower, resulting in an efficiency of 93% during the in-lab demonstration. Both of these efficiencies hit the project criteria of achieving a power efficiency at least 85%. However, due to the sense resistor issue mentioned before, we could not draw the required current to hit the 24W power criteria. Thus, we only managed to draw a roughly 65% of the current(both input and output) required to match 24W. As mentioned earlier, we believe we would have been able to fix this if we had a smaller sense resistor, which, if we had more time in between orders for testing, we may have been able to discover in time for the second parts order. Using the data from Figure 3, we calculated that our converter uses 15.2W and 15.8W for output and input power, respectively.

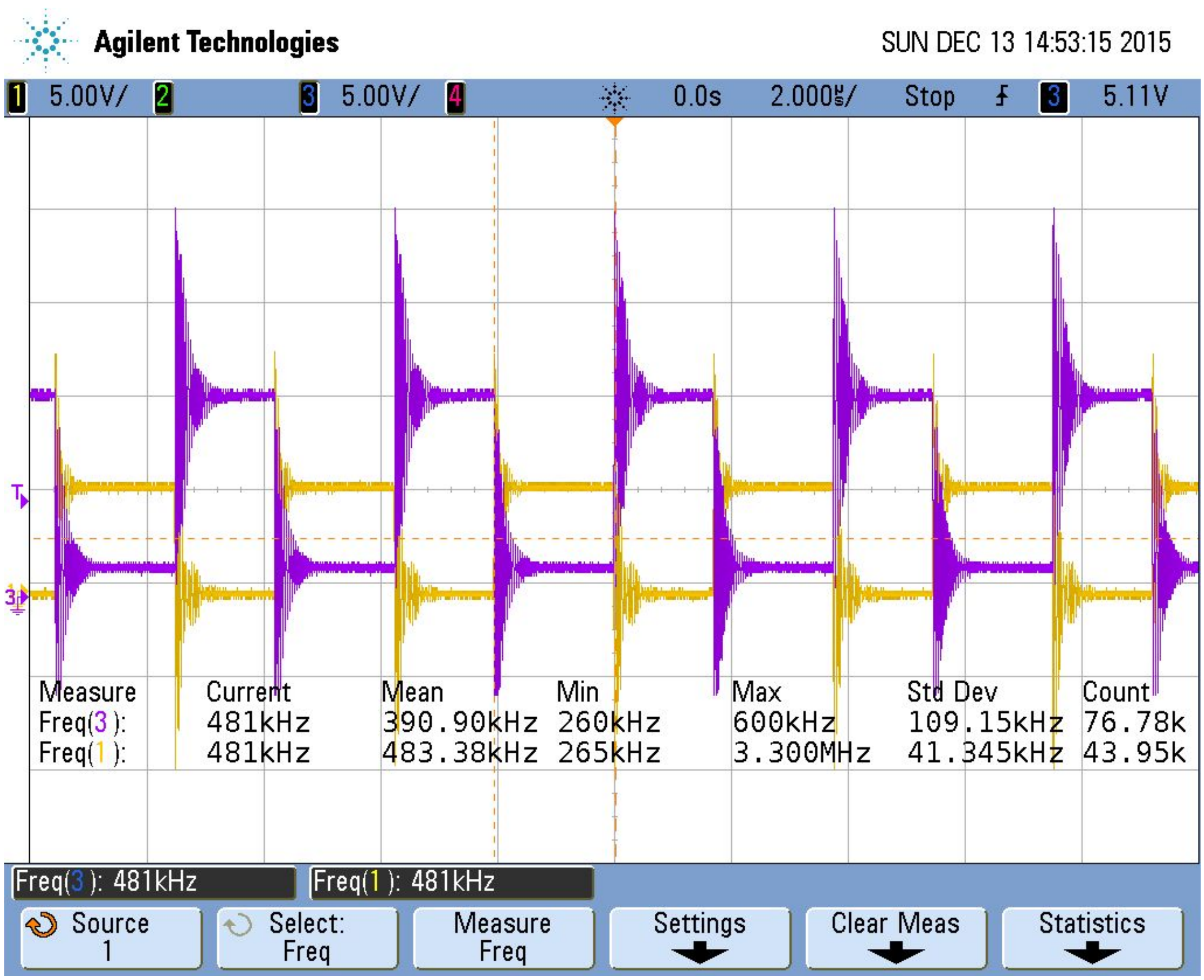


Figure 4: MOSFET Switching Plot

Our design utilized synchronous rectification to further enhance our projected efficiency. Figure 4 shows the gate waveform for both the MOSFETS. The waveforms are inverted, as expected, for our circuit to function. The frequency measured was well above the project criteria of a switching frequency greater than 200kHz. The average frequency for both MOSFETs ranged from 390kHz to 483kHz.

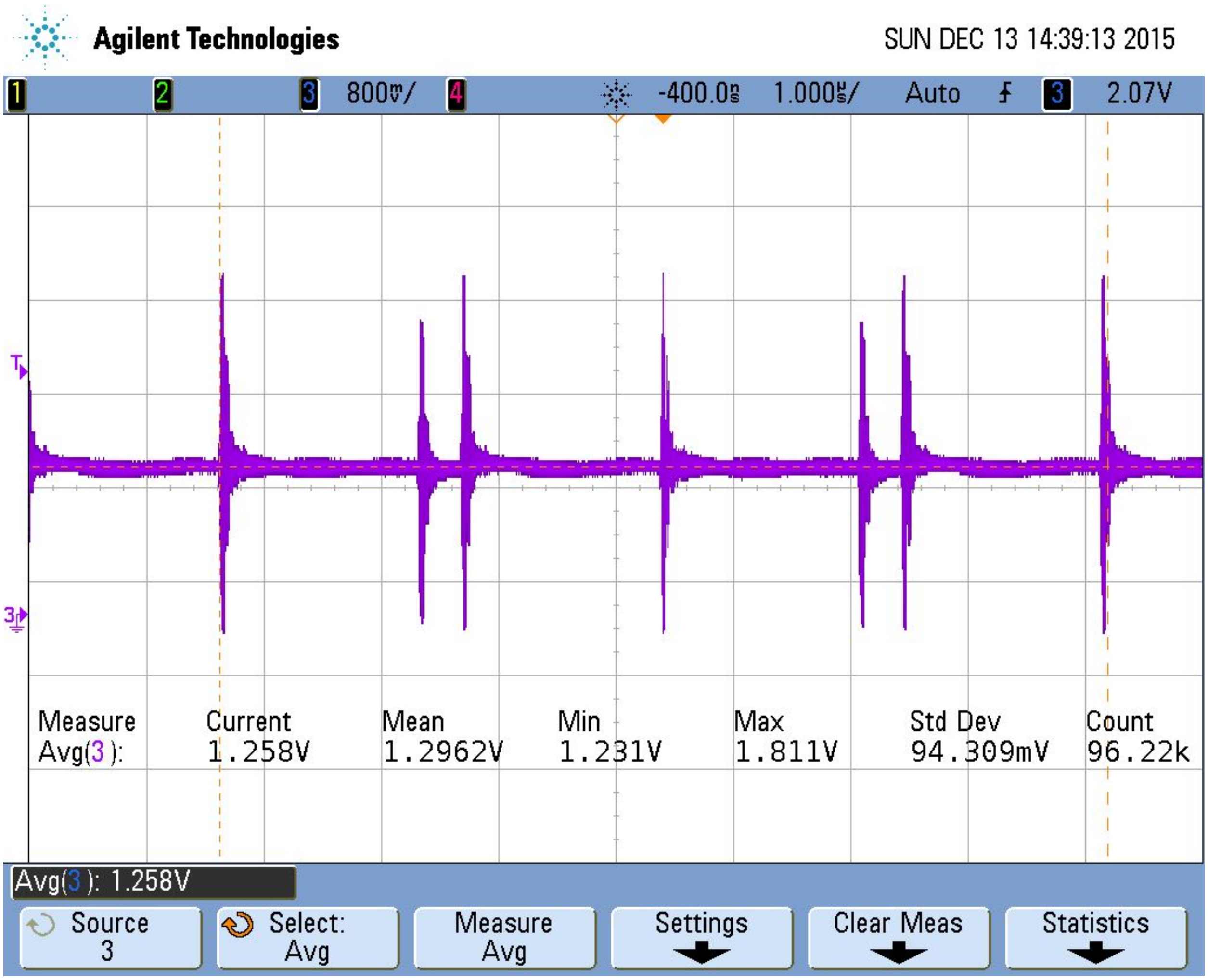


Figure 5: Feedback Voltage Plot

To utilize a voltage control loop, our controller required a feedback voltage of 1.2V. By using a voltage divider on our expected output voltage of 12V, we determined a 1:9 ratio for the resistors. Our feedback voltage, as shown in Figure 5, was a good measure to see if our circuit was working correctly.

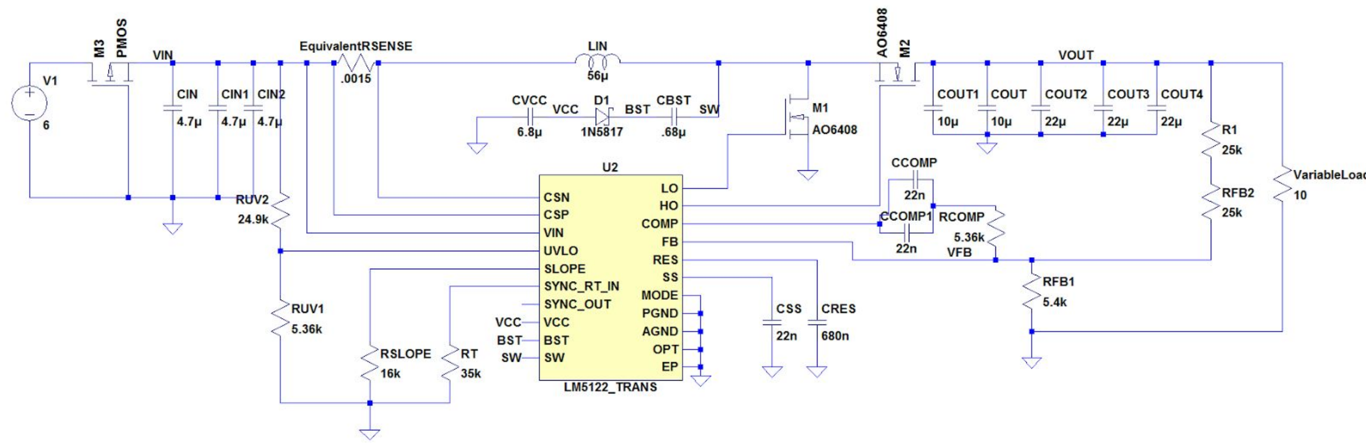
Figure 6: Proof of Mode Switching Circuit Implementation

We were also able to implement the optional Mode Switching functionality. As seen in Figure 6, our converter essentially shuts down when we drop to 5V or lower.

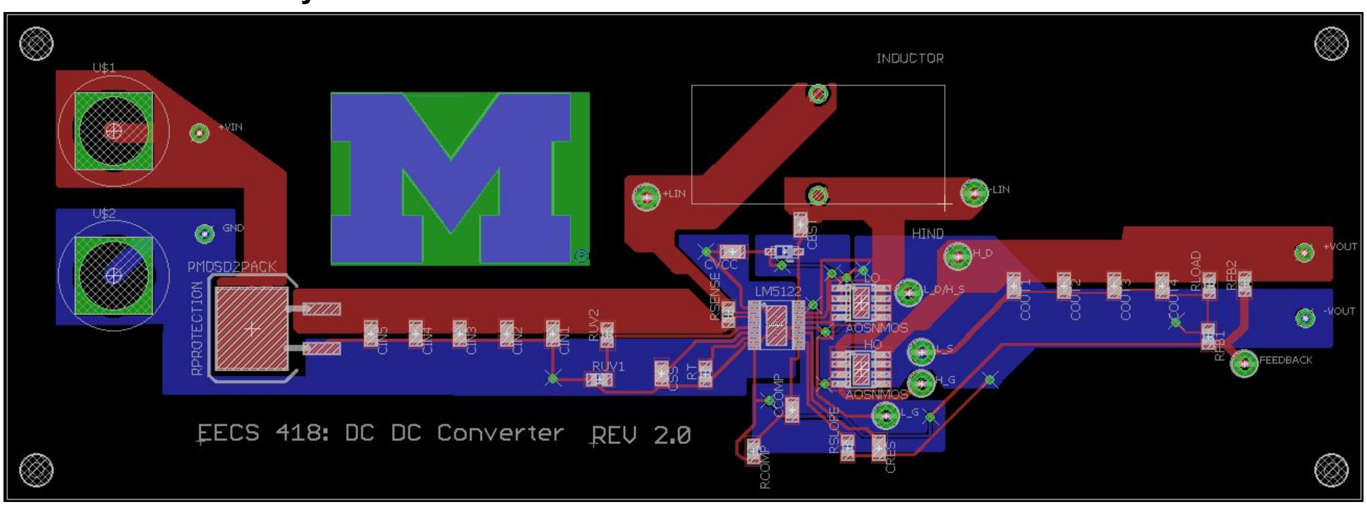
Conclusion

We were able to achieve the majority of the project criteria. 6V input was successfully boosted to 12V. Power efficiency was, at its highest point, 97%. We tested our circuit under different load resistances to find the sweet spot of our design. We were able to maximize our current draw by decreasing the sense resistor value. Adding sense resistors in parallel solved our issue and were now able to draw more current, thus reaching higher output power. The values of other components were then adjusted accordingly to account for a new effective sense resistor value. Further decreasing the sense resistance value would have allowed us to reach 6Ω load, drawing close to 2A and reaching the power criteria for the design. If time allowed, we could revise our board once more to fulfill all design criteria for the project.

Final/Revised Schematic



Final/Revised PCB Layout



Digikey Cart (Single Board)

http://www.digikey.com/short/t02p0r