Jose Eduardo Barcenas

josebar@umich.edu • 940 389 8319

Education

University of Michigan — Ann Arbor, MI
Masters of Science in Engineering, Electrical Engineering — Expected Graduation: December 2015
Solid State Electronics and Nanotechnology Focus — GPA: 3.55/4.00
Relevant Courses: Thin Film Devices and Circuits, Power Semiconductor Devices, Solid State Device Laboratory

University of North Texas — Denton , TX
Bachelor of Science in Computer Engineering; Minor in Mathematics — May 2014
Cum Laude, Outstanding Undergraduate Student in Computer Engineering for 2014-2015 — GPA: 3.72/4.00
Relevant Courses: Numerical Analysis, Solid State Physics, VLSI Design

Technical Expertise

Systems: Windows, Linux, Mac OS X
Languages: C++, C, VHDL, Verilog-A, Python, Visual Basic for Applications, SQL
Applications: JMP, Microsoft Office, Matlab, LabVIEW, Cadence Virtuoso, PSpice, Synopsys TCAD, Silvaco TCAD

Work Experience

Intel - Thermal and Power Validation Metrology Intern [May 2015 - August 2015]
• Assessed repeatability, stability and measurement accuracy of thermal power systems across multiple product segments/platforms
• Setup thermal power system experiments in a lab setting. Fully Integrated Voltage Regulator(FIVR) and System on a Chip parts were tested
• Automate data collection and analysis using JMP and Python scripts

NSF International - Engineering Intern [January 2015 - April 2015]
• Wrote Visual Basic for Excel scripts to update automotive parts database from multiple sources
• Generate accuracy check reports of database created from multiple sources
• Audited OEM certification part reports from technicians for website listing

VCE - Cloud Practice Technical Intern [May 2014 - August 2014]
• Maintain and Organize the Internal Wiki for the Cloud Practice group
• Monitor usage and utilization of Cloud Environment Lab
• Assist with creation of the software release certification matrix document for the Cloud Accelerator Service

Texas Instruments – Software Engineering Intern [May 2013 – August 2013]
• Validate Android DSSComp(Display SubSystem Composition architecture) on Android Kernel 3.8 using a test suite on a next generation "Jacinto 6" infotainment processor developed by Texas Instruments
• Update Design Specification Document for Android DSSComp
• Add new test cases to the test suite

Course Projects and Research

EECS 423, Solid State Device Laboratory:
Silicon Wafer Fabrication [Fall 2014]
Fabricated and tested polycrystalline Si gate, n-channel enhancement Si Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and related devices in the Lurie Nanofabrication Facility. Fabrication technology includes lithography, etching, deposition, oxidation, diffusion, and annealing.

EECS 512, Thin Film Devices and Circuits:
Report on Active Pixel Sensors for X-ray Imaging[Fall 2013 – Spring 2014]
Explore X-ray digital imaging techniques, focusing on Active Pixel Sensors(APS) arrays. Thin film transistor circuit architecture explored along with operation and properties at the circuit level. Noise and Quantum Efficiency metrics of APS compared to Passive Pixel Sensor arrays were also explored.

EECS 521, Solid State Devices:
Sentaurus Simulation for Junctionless Transistor [Spring 2015]
Design a double gate n-channel junctionless transistor to maintain Drain Induced Barrier Lowering less than 50mV/V and subthreshold slope below 70mV/dec. Gate length, oxide thickness and doping levels were optimized to achieve the design goals.