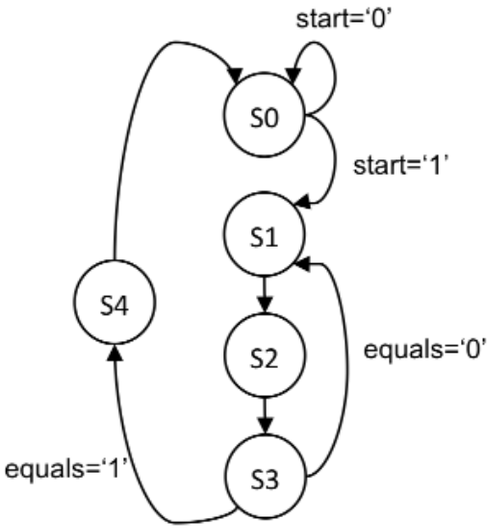
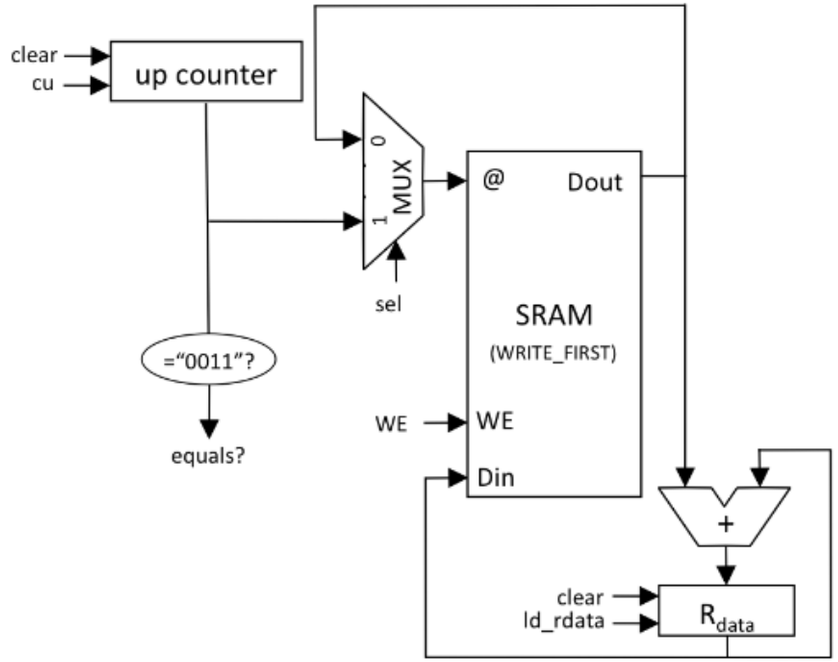
- Complete the chronogram corresponding to the following system and indicate the final content of the memory. The system inputs are `start`, `clk` and `rst`, the output is end. The rest of the signals are internal signals according to the attached table.
- The memory is synchronous for reading/writing and is of type WRITE_FIRST.





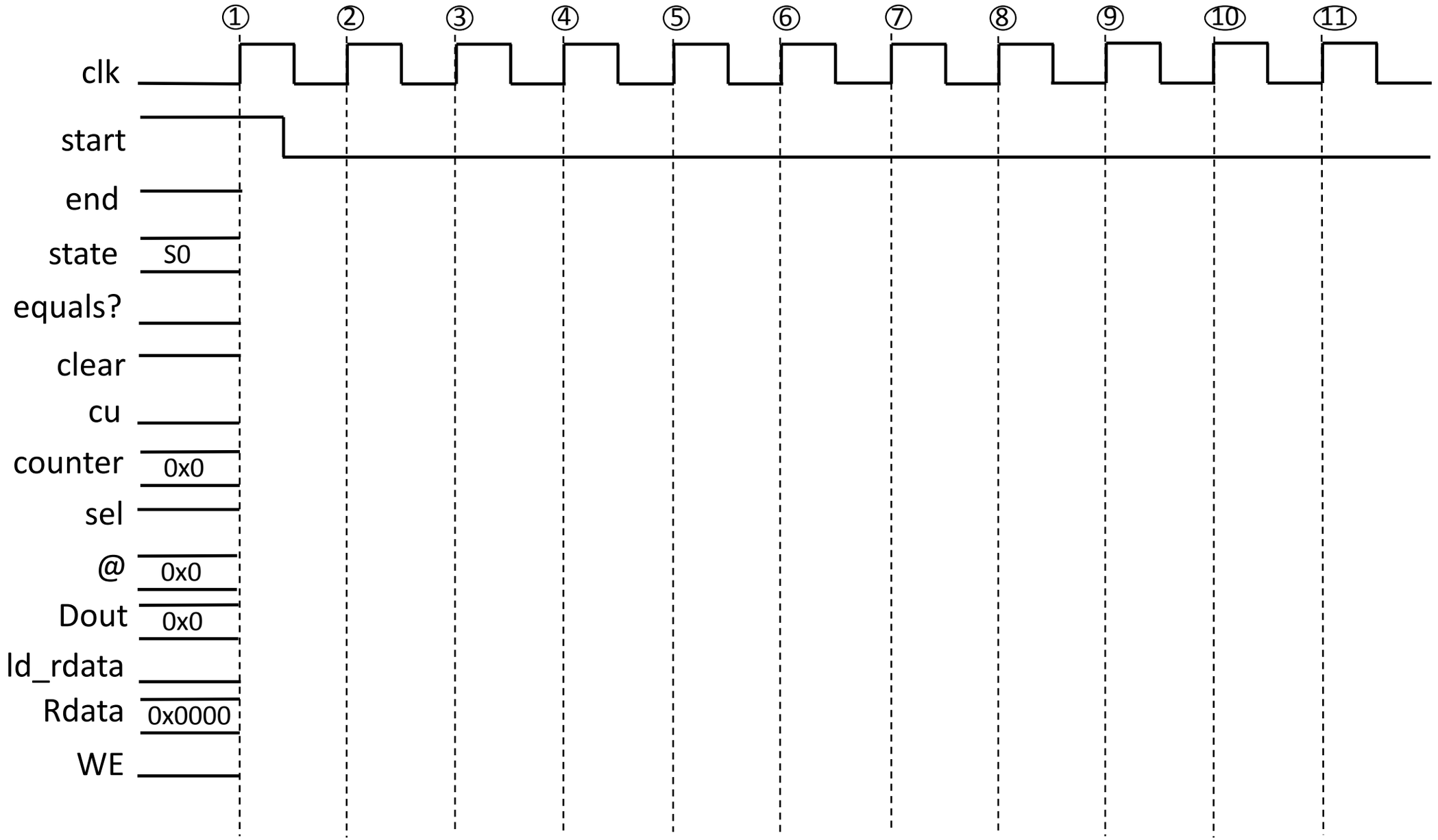
SRAM Data

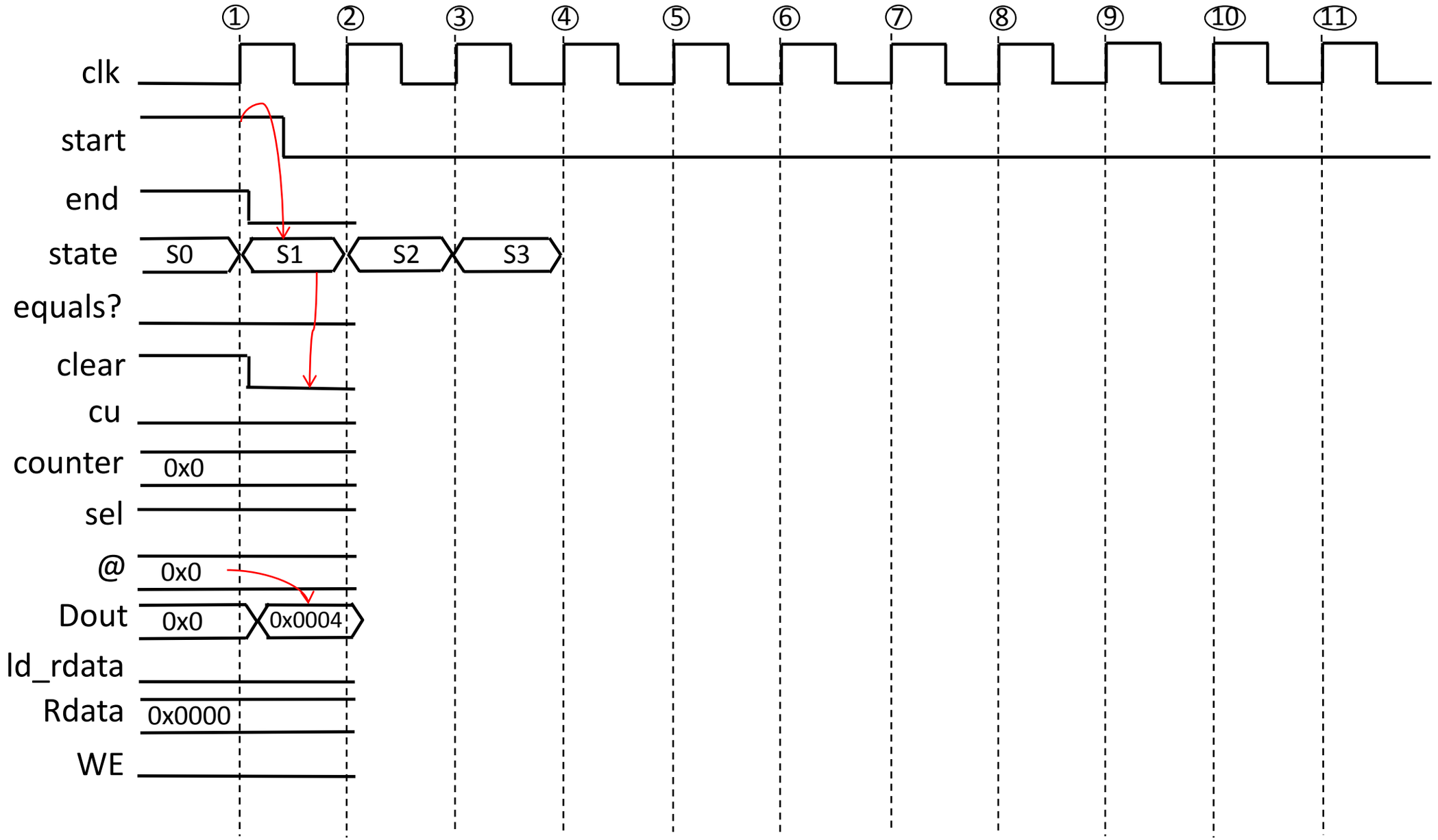
Dirección	Dato
0x00	0x0004
0x01	0x0005
0x02	0x0006
0x03	0xBEEF
0x04	0x1010
0x05	0x0202
0x06	0x3131

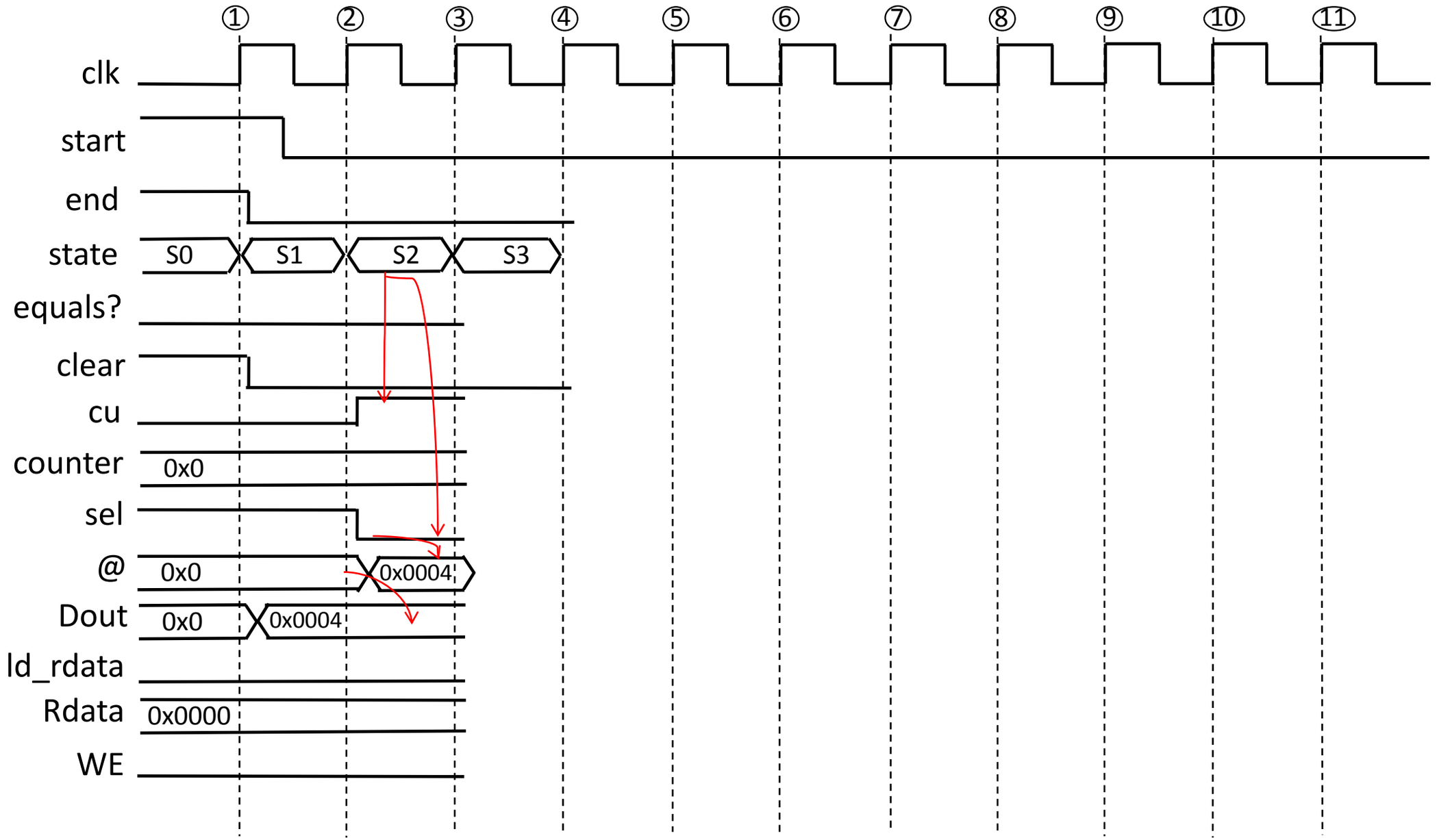
FSM Outputs

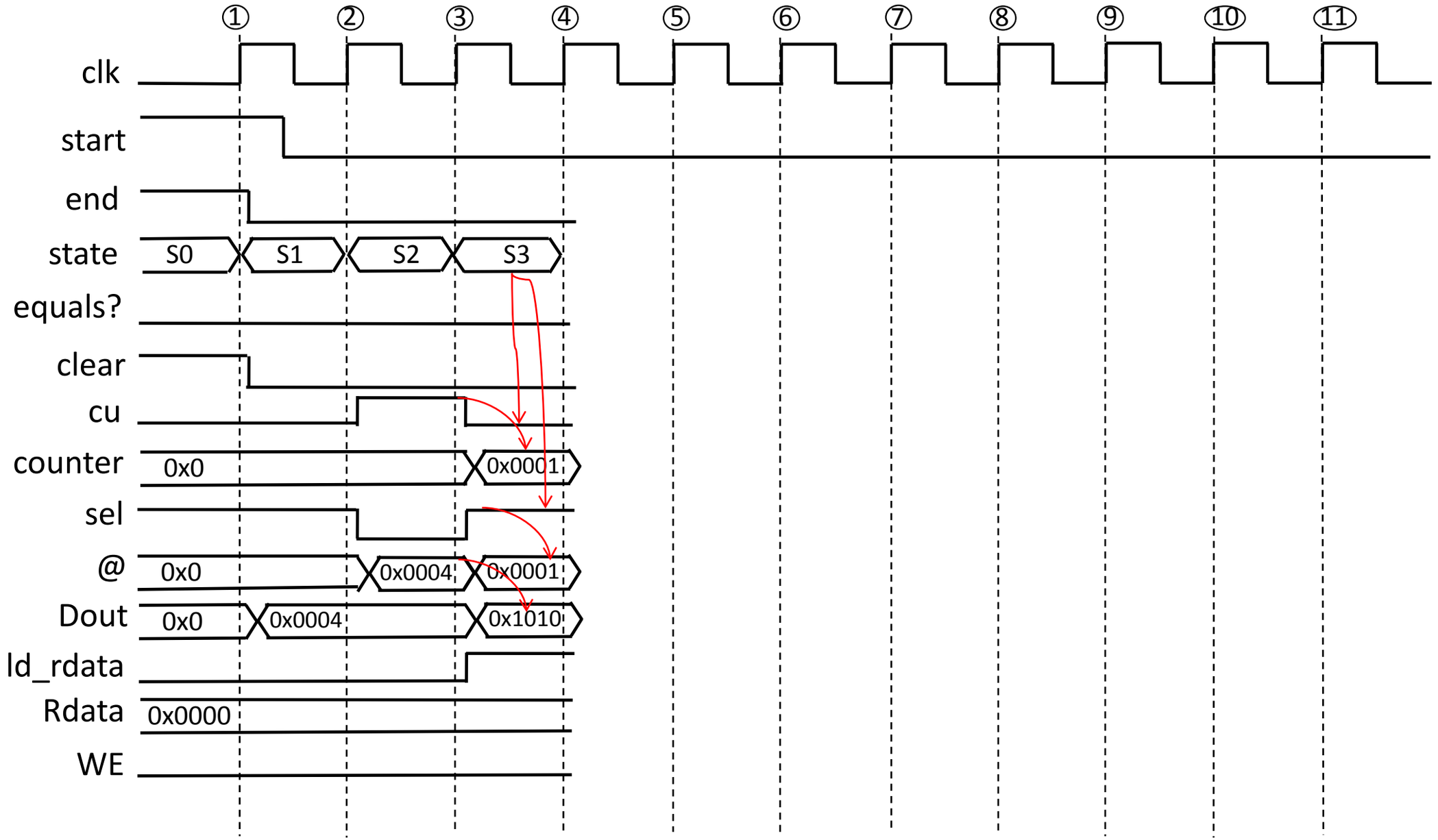
Estado	clear	cu	sel	ld_rdata	WE	end
S0	1	0	1	0	0	1
S1	0	0	1	0	0	0
S2	0	1	0	0	0	0
S3	0	0	1	1	0	0
S4	0	0	1	0	1	0

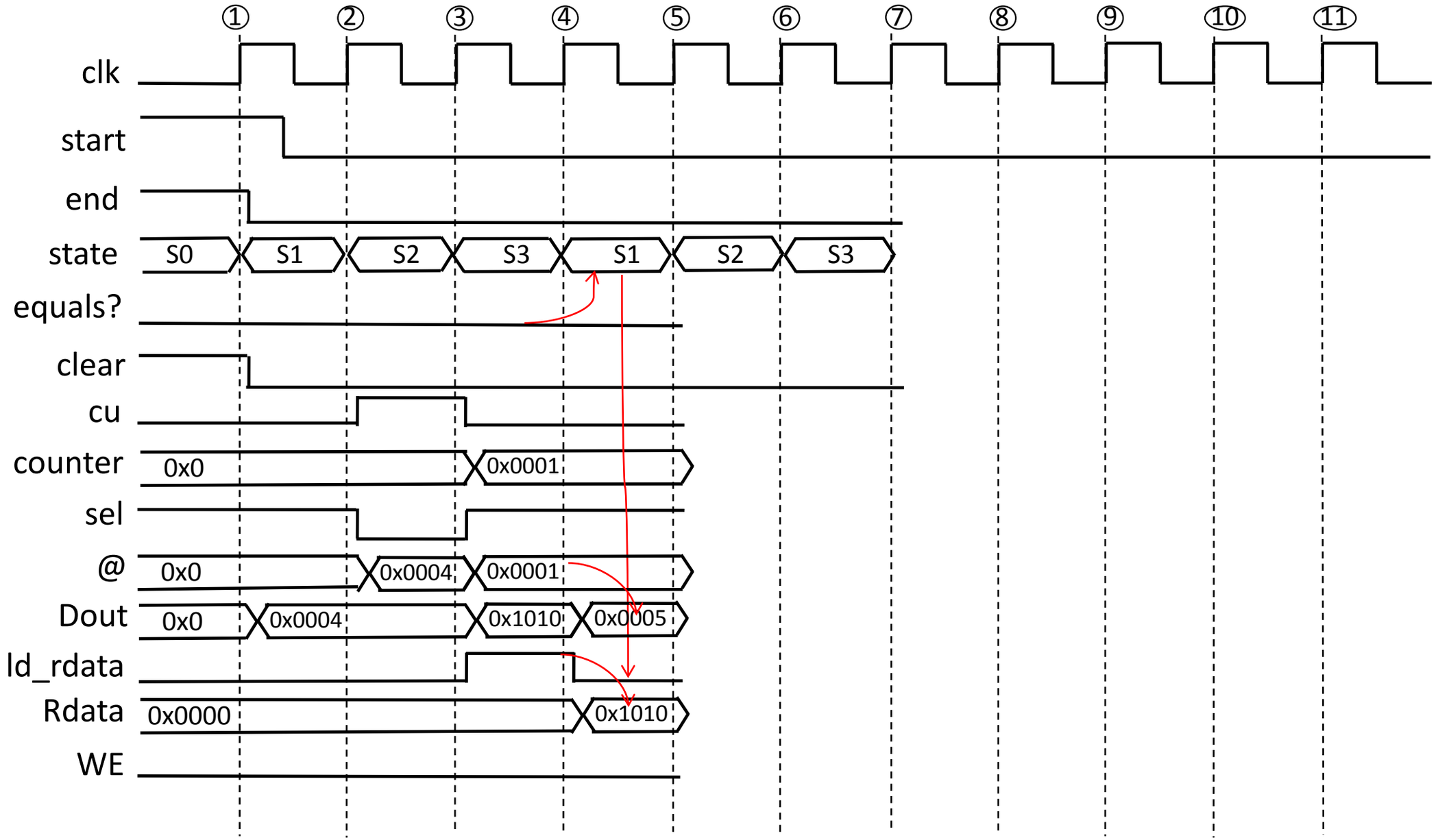
- The counter module is ascending, 8b wide, has the signal `cu` as count enable and the `clear` signal loads a 0 synchronously.

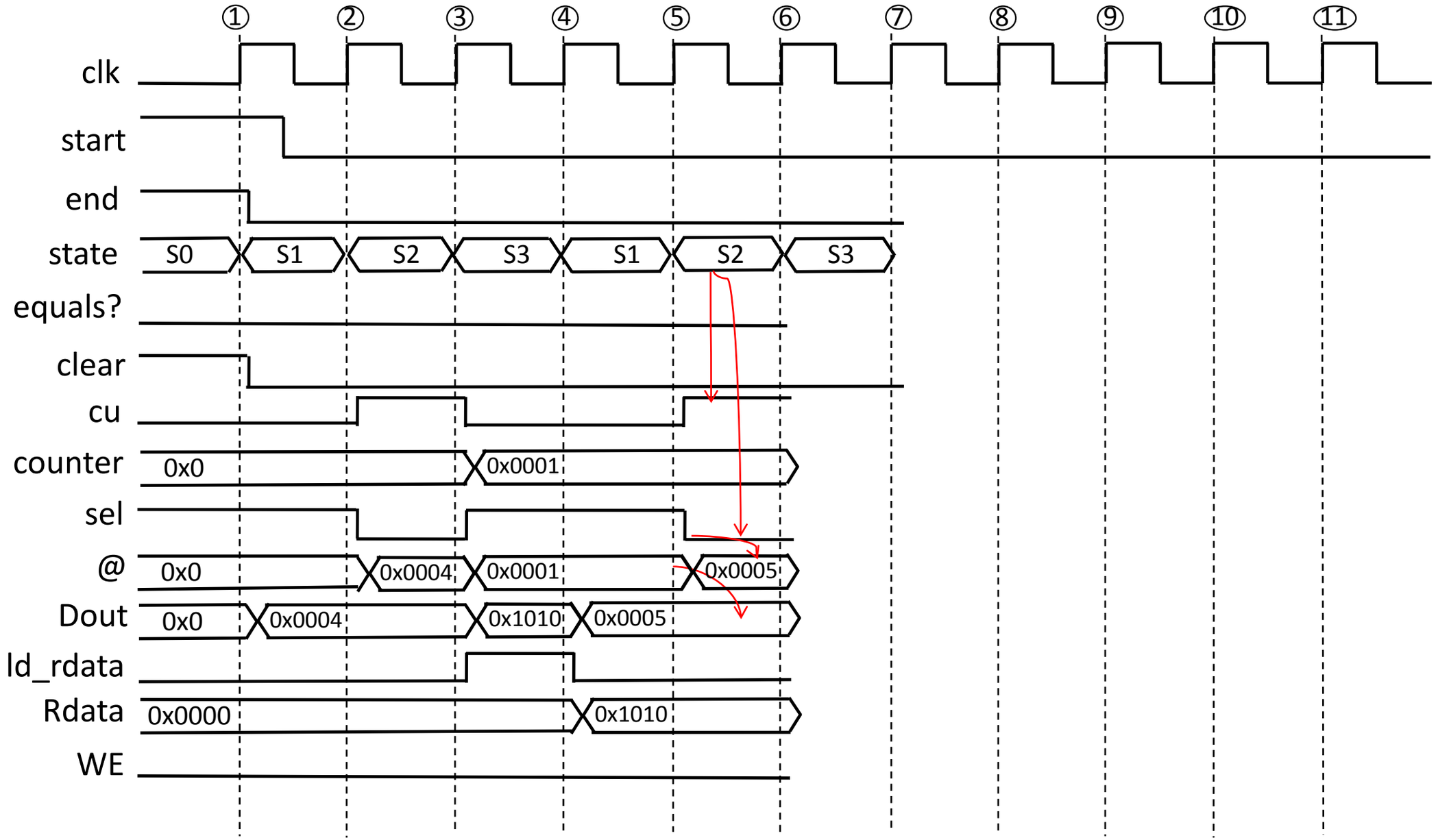

①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
equals?
clear
cu
counter
0x0
sel
@
0x0
Dout
0x0
ld_rdata
Rdata
0x0000
WE

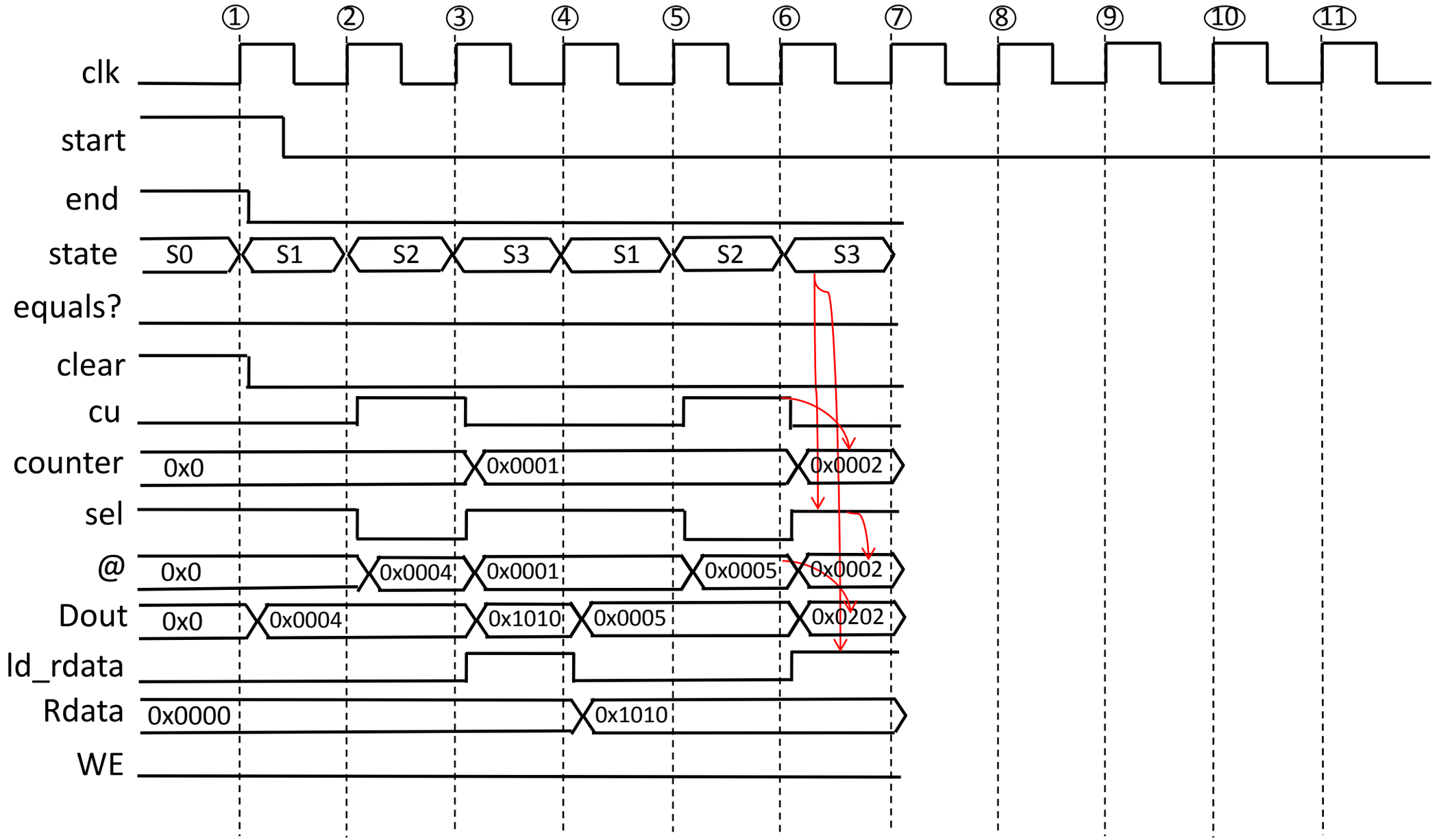

①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
equals?
clear
cu
counter
0x0
sel
@
0x0
Dout
0x0
0x0004
ld_rdata
Rdata
0x0000
WE

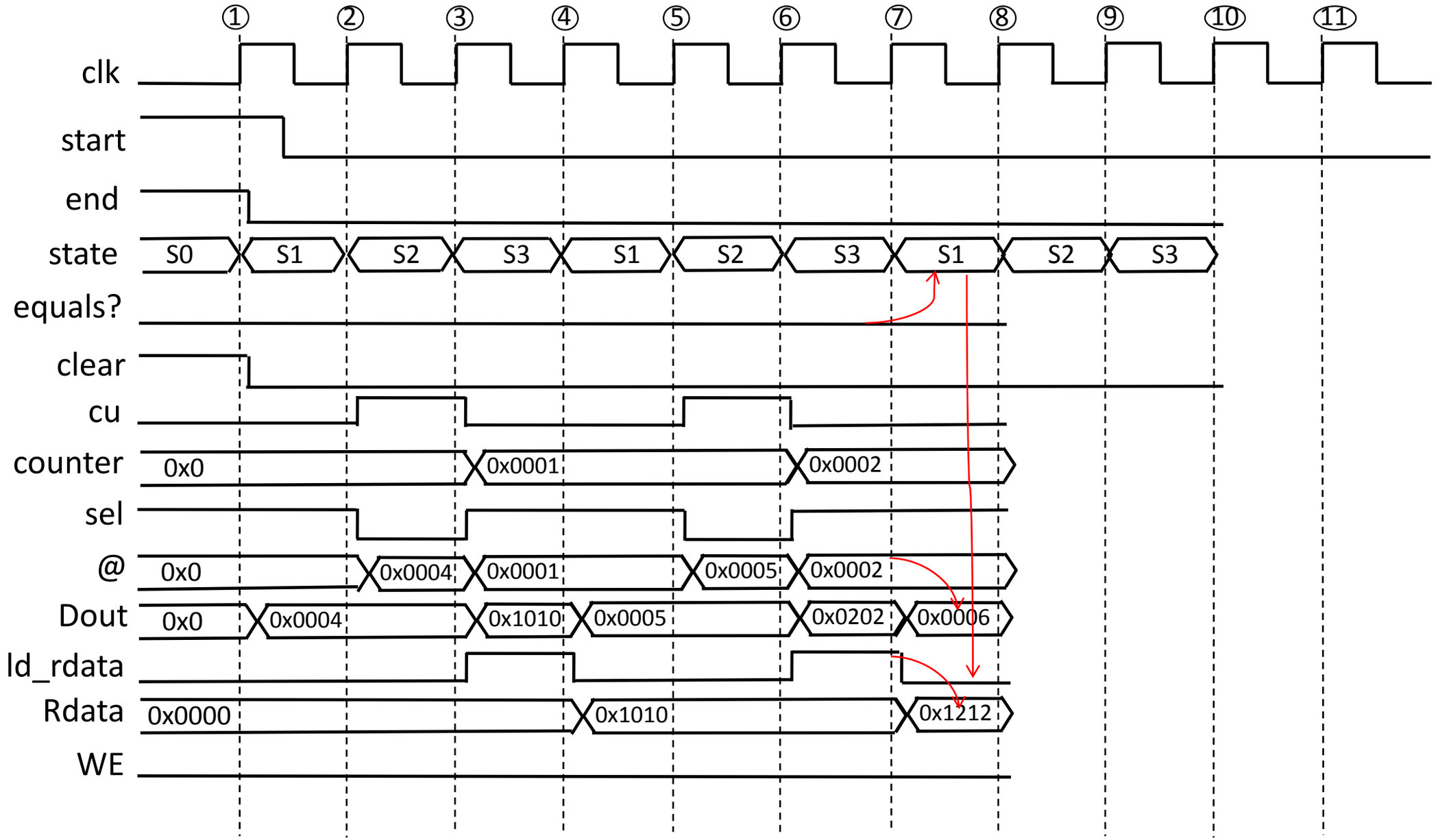

①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
equals?
clear
cu
counter
0x0
sel
@
0x0
0x0004
Dout
0x0
0x0004
ld_rdata
Rdata
0x0000
WE

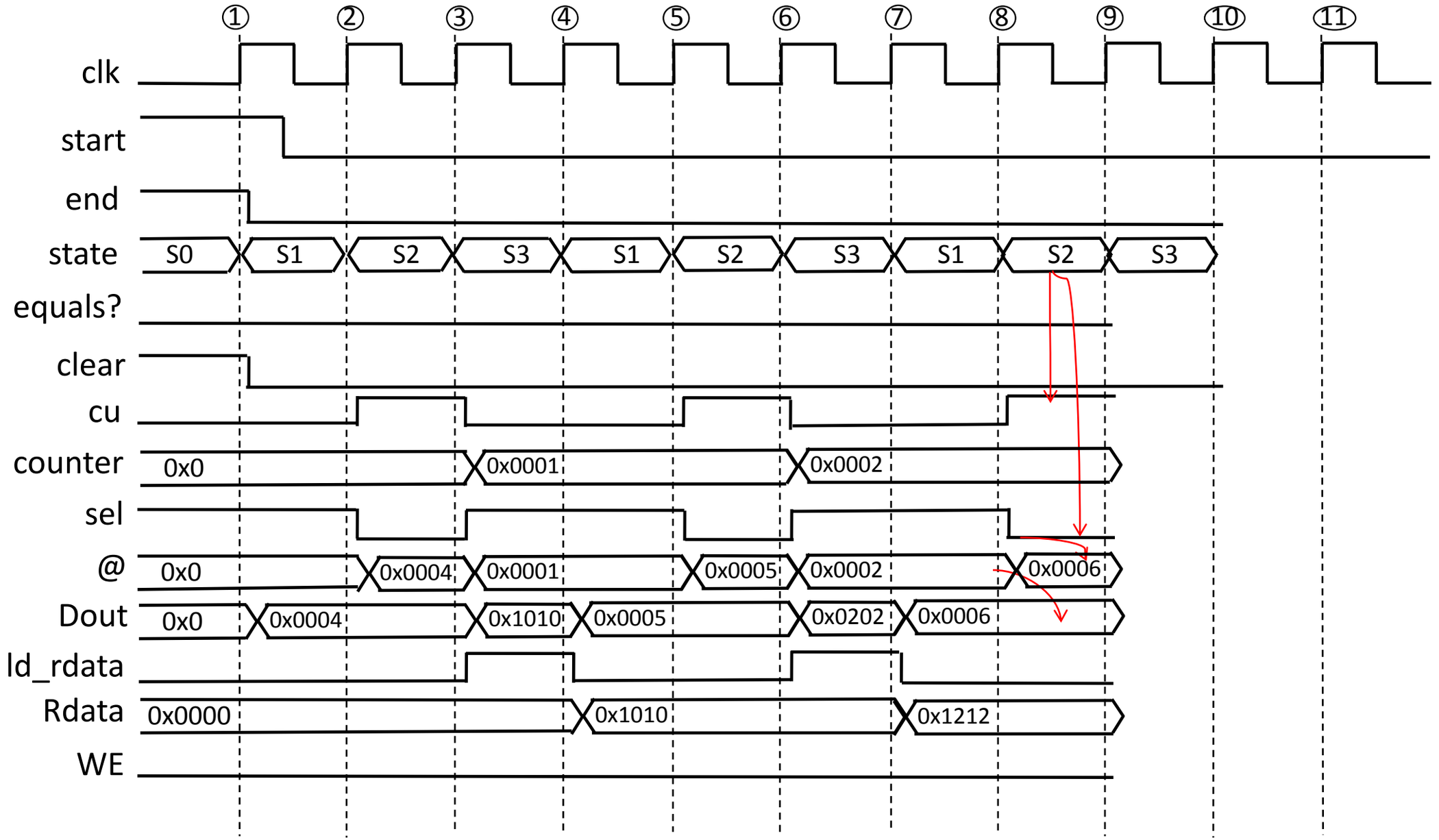

①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
equals?
clear
cu
counter
0x0
0x0001
sel
@
0x0
0x0004
0x0001
Dout
0x0
0x0004
0x1010
ld_rdata
Rdata
0x0000
WE


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
equals?
clear
cu
counter
0x0
0x0001
sel
@
0x0
0x0004
0x0001
Dout
0x0
0x0004
0x1010
0x0005
ld_rdata
Rdata
0x0000
0x1010
WE


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
equals?
clear
cu
counter
0x0
0x0001
sel
@
0x0
0x0004
0x0001
0x0005
Dout
0x0
0x0004
0x1010
0x0005
ld_rdata
Rdata
0x0000
0x1010
WE


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
equals?
clear
cu
counter
0x0
0x0001
0x0002
sel
@
0x0
0x0004
0x0001
0x0005
0x0002
Dout
0x0
0x0004
0x1010
0x0005
0x0202
ld_rdata
Rdata
0x0000
0x1010
WE


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
S1
S2
S3
equals?
clear
cu
counter
0x0
0x0001
0x0002
sel
@
0x0
0x0004
0x0001
0x0005
0x0002
Dout
0x0
0x0004
0x1010
0x0005
0x0202
0x0006
ld_rdata
Rdata
0x0000
0x1010
0x1212
WE


①
②
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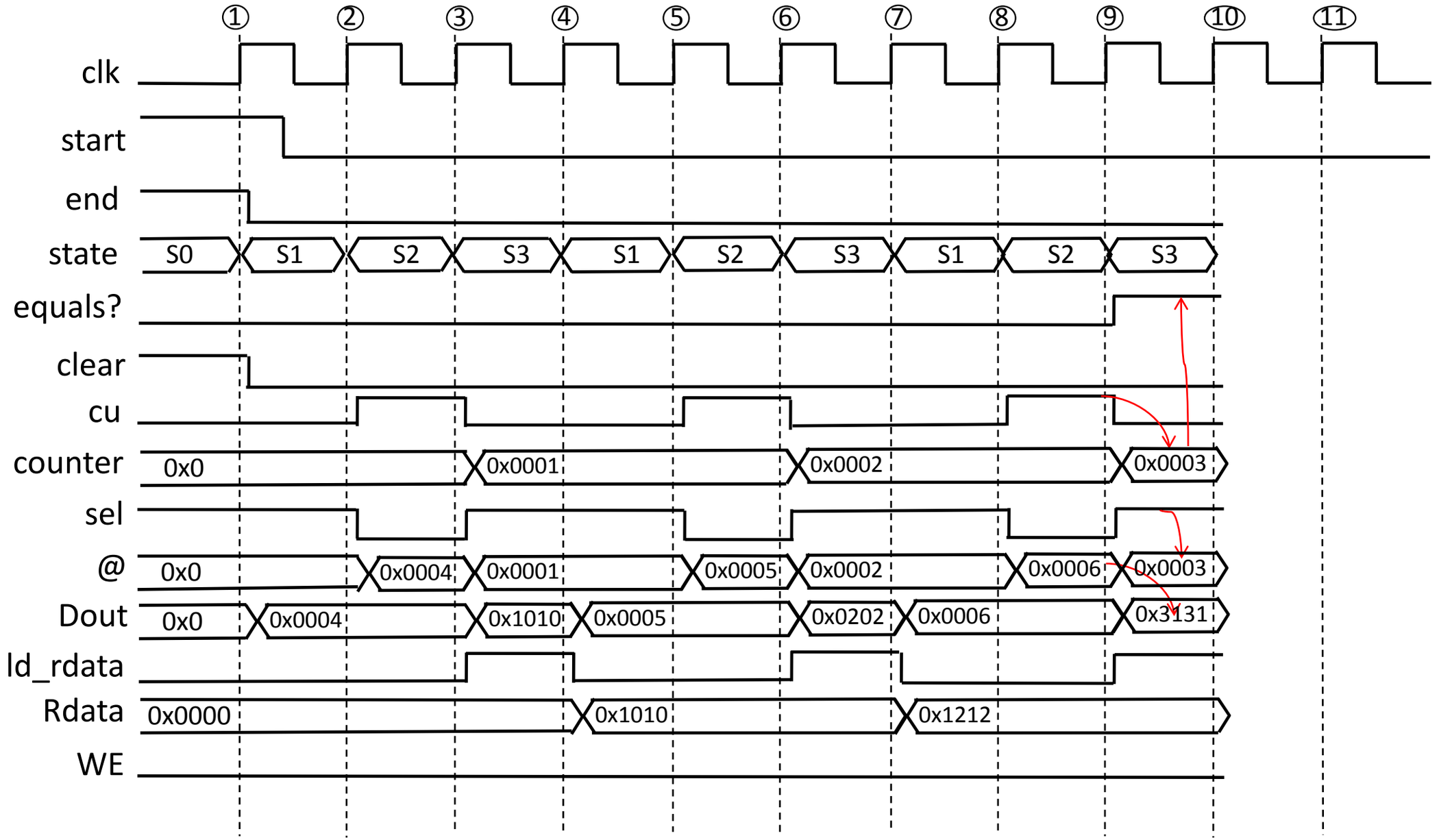
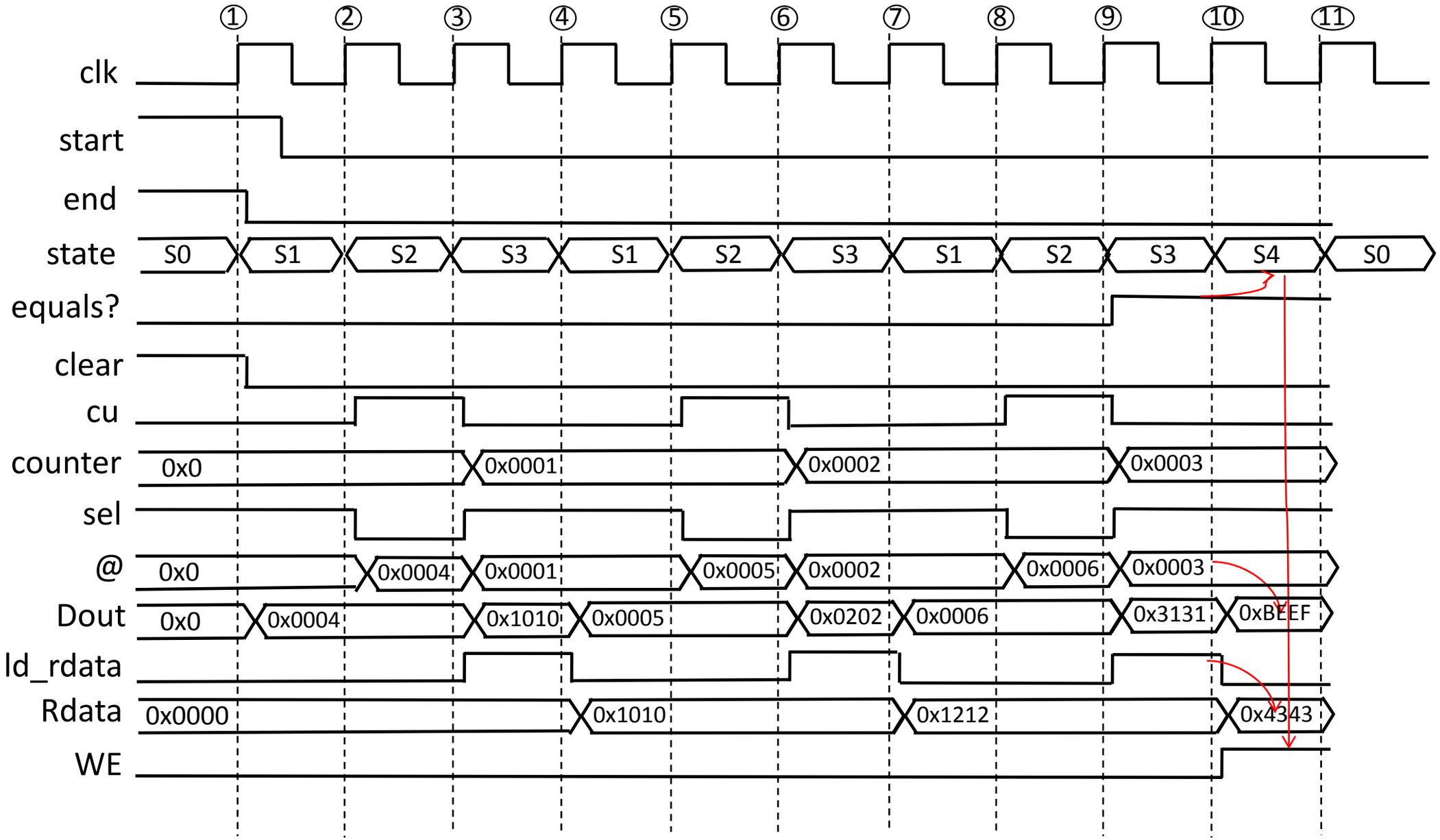
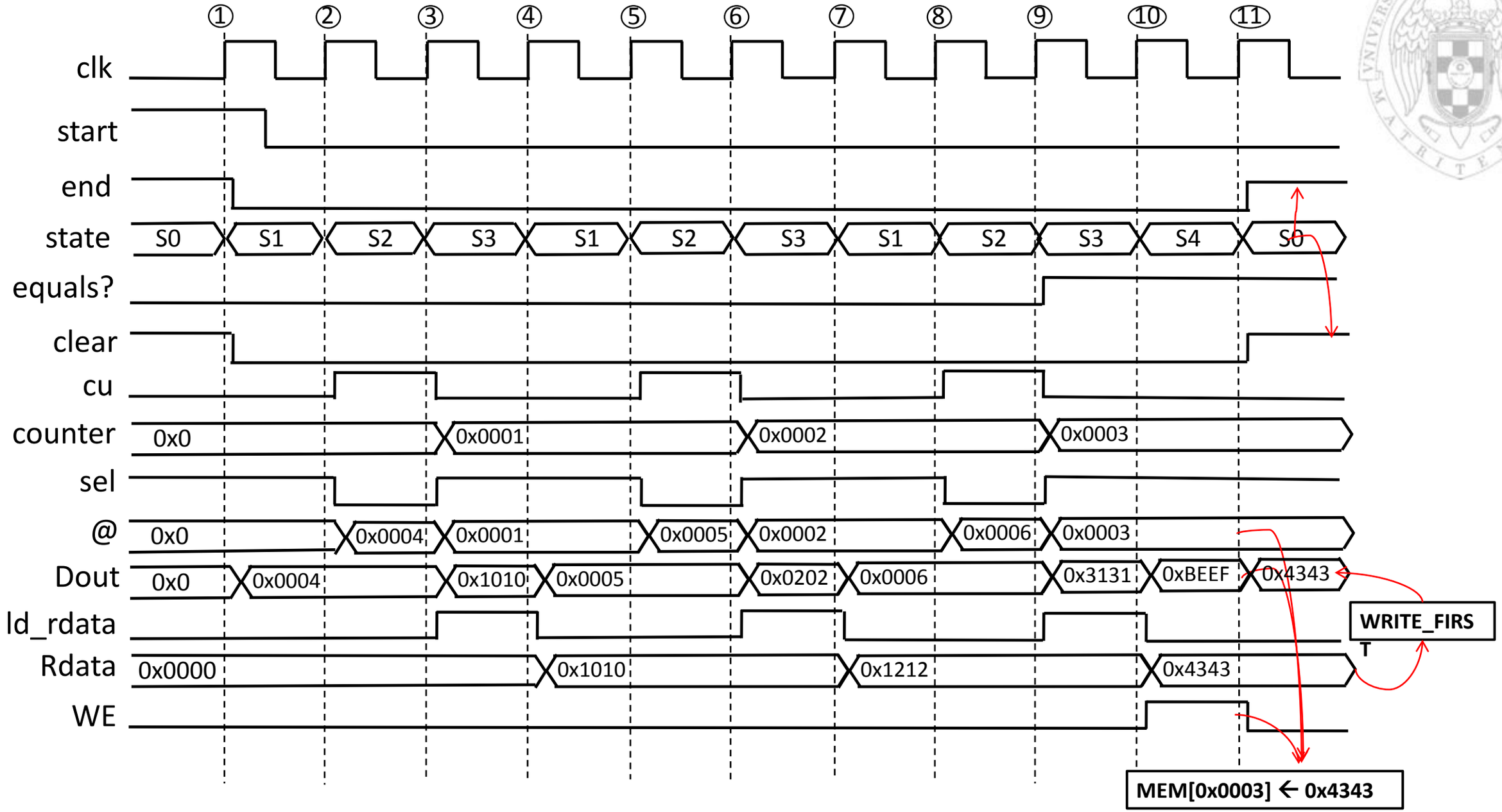
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
S1
S2
S3
equals?
clear
cu
counter
0x0
0x0001
0x0002
sel
@
0x0
0x0004
0x0001
0x0005
0x0002
0x0006
Dout
0x0
0x0004
0x1010
0x0005
0x0202
0x0006
ld_rdata
Rdata
0x0000
0x1010
0x1212
WE

TOC


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
S1
S2
S3
equals?
clear
cu
counter
0x0
0x0001
0x0002
0x0003
sel
@
0x0
0x0004
0x0001
0x0005
0x0002
0x0006
0x0003
Dout
0x0
0x0004
0x1010
0x0005
0x0202
0x0006
0x3131
ld_rdata
Rdata
0x0000
0x1010
0x1212
WE


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
S1
S2
S3
S4
S0
equals?
clear
cu
counter
0x0
0x0001
0x0002
0x0003
sel
@
0x0
0x0004
0x0001
0x0005
0x0002
0x0006
0x0003
Dout
0x0
0x0004
0x1010
0x0005
0x0202
0x0006
0x3131
0xBEEF
ld_rdata
Rdata
0x0000
0x1010
0x1212
0x4343
WE


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
⑪
clk
start
end
state
S0
S1
S2
S3
S1
S2
S3
S1
S2
S3
S4
S0
equals?
clear
cu
counter
0x0
0x0001
0x0002
0x0003
sel
@
0x0
0x0004
0x0001
0x0005
0x0002
0x0006
0x0003
Dout
0x0
0x0004
0x1010
0x0005
0x0202
0x0006
0x3131
0xBEEF
0x4343
ld_rdata
Rdata
0x0000
0x1010
0x1212
0x4343
WE
WRITE_FIRST
MEM[0x0003] ← 0x4343