High-Frequency Signal Interconnection Optimization Using Wirebond and GCPW Transmission Line in HFSS

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1 Design Specifications

- Use 25 µm diameter Au wirebonding
- Minimum wire bond loop height: 75 µm
- Package substrate minimum L/S: 30 µm / 30 µm
- Minimum via radius: 30 µm, pad radius: 50 µm
- Minimum clearance from die edge to wirebond pad: 180 µm

1.1 Transmission Line Design

To build a reliable signal interconnect, the design incorporated vertical vias to route the signal from the bottom of the package to the top, followed by a grounded coplanar waveguide (GCPW) transmission line of characteristic impedance of 50 Ω. This target was critical for minimizing reflection. The TX Line tool was used to ensure the trace configuration achieves 50 Ω impedance. Initial parameters:

- Signal width: 60 µm
- Package height (to the first layer): 18 µm
- Spacing to ground: 60 µm
- Ground via radius: 35 µm, pitch: 100 µm
- Via pad radius: 50 µm

To improve grounding, multiple vertical ground layers were added inside the package, connected with densely spaced vias.

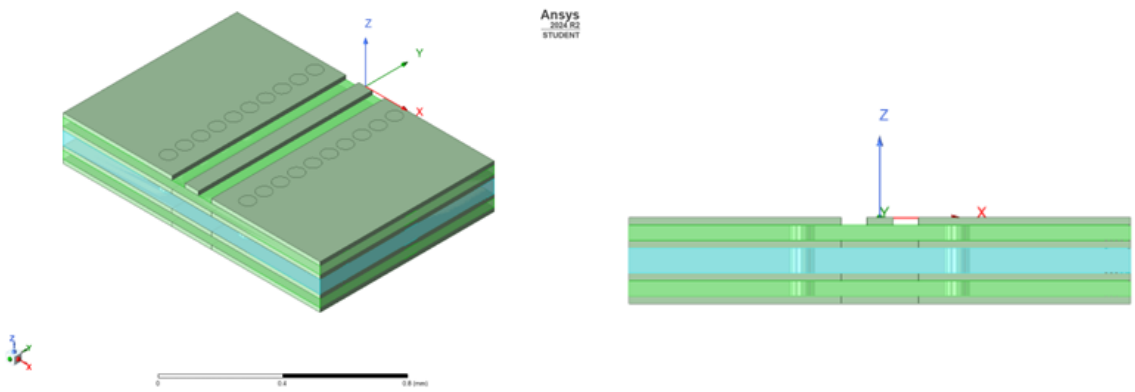

Figure 1: First Image depicts the geometry of the Transmission Line. Second image depicts the Cross-sectional view of GCPW transmission line

The layout shown includes the matched transmission line on the package substrate. Its width and spacing were chosen to work with the calculated parameters.

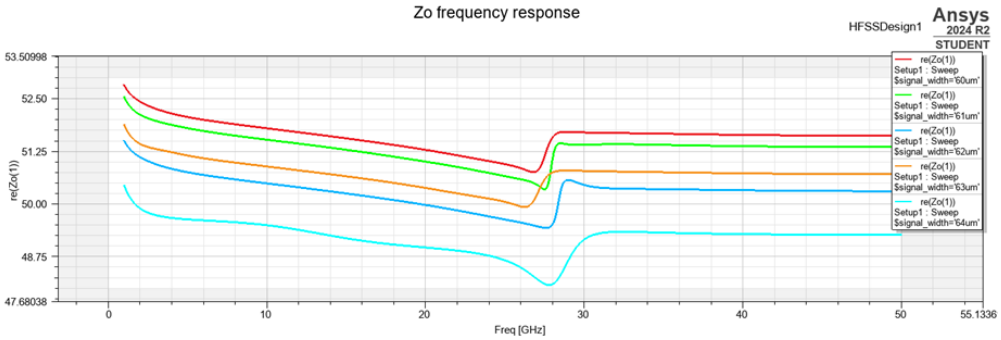

Figure 2: The impedance analysis shows excellent agreement with the 50 Ω goal over a wide frequency range using widths from 60 microns to 64 microns.(target: 50 Ω)

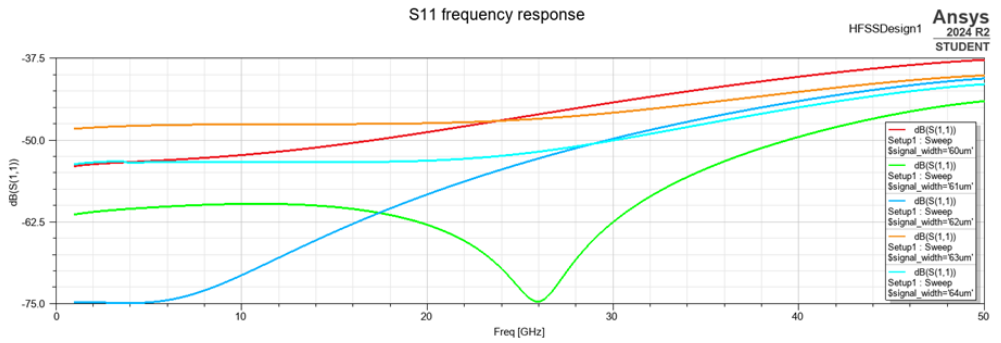

Figure 3: S_{11} parameter of transmission line: sub -37.5 dB

As shown, the GCPW structure alone exhibits nearly perfect matching, with S11 dropping below -37.5 dB at the desired high frequency.

1.2 Initial Vertical Interconnection

A single wirebond was used to bridge the signal from the die to the top trace, with minimized height and distance to reduce self-inductance. The wirebond diameter, which is the primary parameter to adjust inductance, was not modified in the simulation creating a challenge with the low radius for the signal to reach the Die. Additionally, three Through-Package Vias where used to connect the bottom pads to the top traces and the corresponding ground plates.

Although initially simple, when connecting to the transmission line and the PCB, the reflection power increase was drastic at high frequencies.

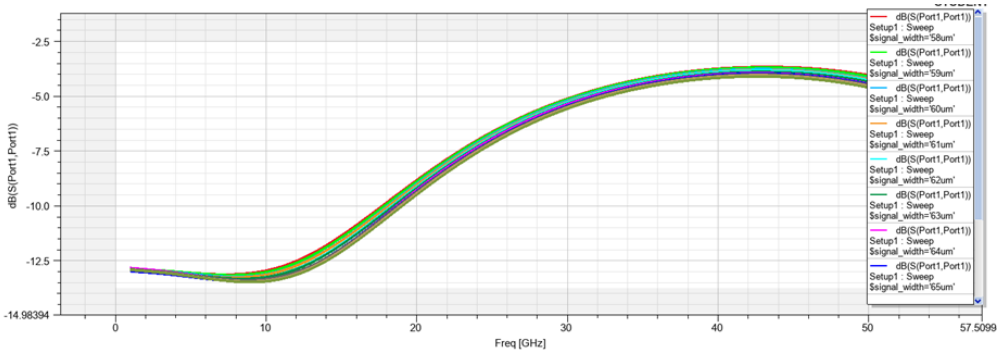

Figure 4: S_{11} of full path of Transmission Line with single wirebond, width ranges from 55-68 microns

Reflection reached $-3\,\text{dB}$ at $45\,\text{GHz}$, meaning more than 50% of the signal was being reflected. This level of mismatch is unacceptable for high-frequency operation.

The following limitations were identified:

- High wirebond inductance from using a single bond
- Impedance discontinuity due to mismatched PCB's, TPV's, signal trace's and wirebond interconnect's cross-sectional areas.
- Poor ground connectivity due to small, sparse vias.

1.3 Final Product

Improvements implemented:

- Signal width increased to $200\,\mu\text{m}$ to achieve a closer width to the PCB's signal trace ($300\,\mu\text{m}$)to assimilate the PCB's characteristic impedance.
- 5 parallel wirebonds used to reduce inductance.
- Signal vias increased to $200\,\mu\text{m}$ diameter with $300\,\mu\text{m}$ pads to reduce self inductance and reduce trace discontinuity.

- Ground vias enlarged and densely packed to enlarge the ground connection coverage and improve fencing.

The width and spacing were carefully tuned because the characteristic impedance of a transmission line is fully dependent on the physical properties and dimensions of the component.

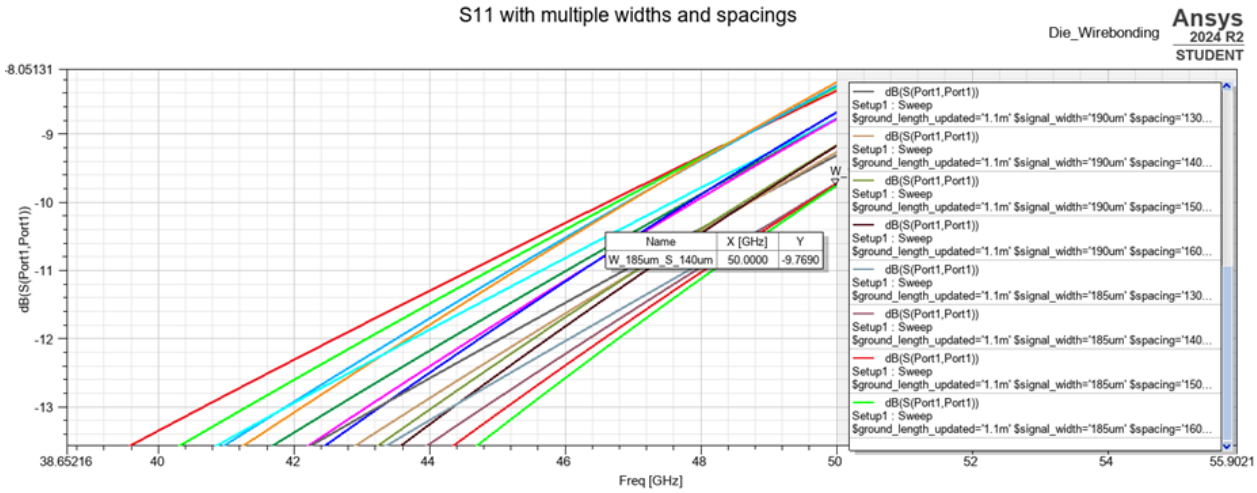

Figure 5: S11 is one of the closest to -10dB at 140 µm spacing and 185 µm width. The difference in using 140 µm (green) and 150 µm spacing (red) was subtle, 150 µm was kept.

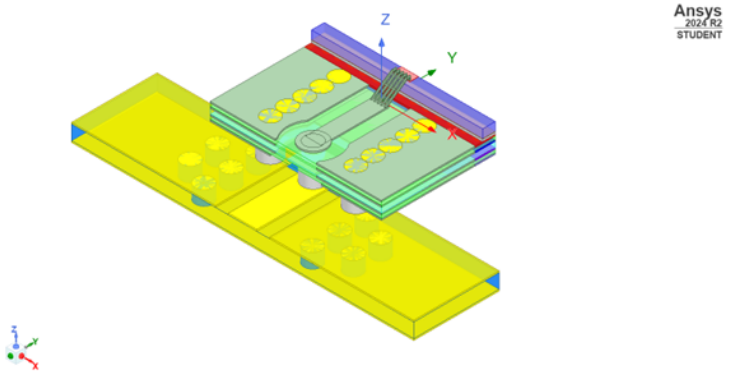

Figure 6: Final design layout

This final layout integrates optimized transmission line dimensions, dense ground stitching, and multi-wirebond structure.

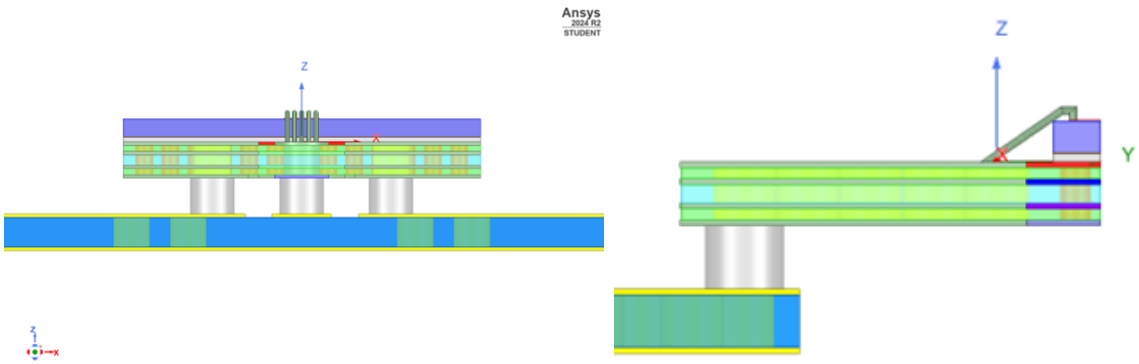

Figure 7: First Image depicts the geometry of the Transmission Line. Second image depicts the Cross-sectional view of GCPW transmission line

Following several simulation refinements, the final interconnect structure was evaluated using HFSS with full 3D modeling of the wirebond, GCPW transmission line, via arrays, and dielectric stack. This setup accurately captured high-frequency parasitics and discontinuities.

The final geometry was selected to minimize parasitic inductance and ensure impedance continuity:

- Signal trace width: 185 µm
- Trace length: 793 µm
- Signal-to-ground spacing: 150 µm
- Vias radii: 100 µm
- Signal via pad radius: 150 µm

The 185 µm trace was centered to align with five 25 µm gold wirebonds, spaced 0.4 µm apart. This ensured symmetrical current distribution, reduced inductive mismatch, and preserved EM field symmetry.

S-Parameter Performance

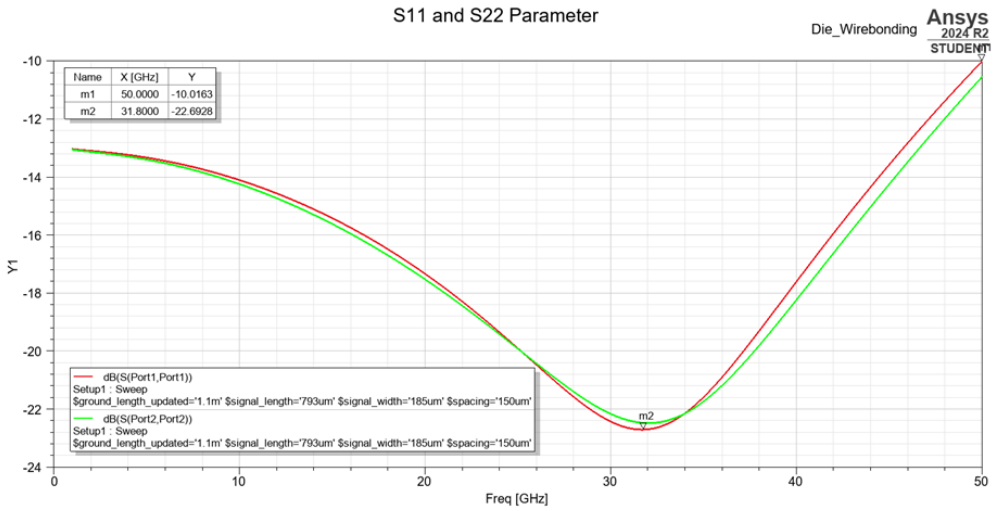

Figure 8: Simulated S_{11} and S_{22} parameters of final optimized structure

Figure 24 shows both S_{11} and S_{22} below the $-10\,\text{dB}$ threshold across the full frequency range. At 50 GHz, reflection remains low, with a minimum near $-22\,\text{dB}$ at 30 GHz, keeping reflections under 10%.

2 Conclusion

This project successfully demonstrated a low-reflection, high-frequency signal interconnection between a PCB and bare die using a grounded coplanar waveguide (GCPW) and optimized gold wirebonding. The final design achieved S_{11} and S_{22} below $-10\,\text{dB}$ up to 50 GHz sharp.

Key improvements included matching the signal width to the PCB trace, using five parallel 25 µm gold wirebonds, increasing via sizes, and tightening via spacing to enhance the return path. A 185 µm trace aligned with the wirebond layout minimized discontinuity, while the enlarged vias reduced parasitic inductance.

These changes significantly lowered high-frequency reflections, with simulation confirming strong field confinement and impedance continuity. The approach highlights how detailed layout optimization and EM modeling can enable robust mmWave packaging with minimal signal degradation.