OV7630 SINGLE-CHIP CMOS VGA COLOR DIGITAL CAMERA
OV7130 SINGLE-CHIP CMOS VGA B&W DIGITAL CAMERA

Description

The OV7630 (color) and OV7130 (black and white) CMOS Image sensors are single-chip video/imaging camera devices designed to provide a high level of functionality in a single, small-footprint package. The devices incorporate a 640 x 480 image array capable of operating at up to 30 frames per second. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions including exposure control, gamma, gain, white balance, color matrix, color saturation, hue control, windowing, and more, are programmable through the serial SCCB interface. The device can be programmed to provide image output in different 8-bit formats.

Features

- 326,688 pixels, 1/4" lens, VGA/QVGA format
- Progressive scan
- 8-bit Data output formats - YCrCb 4:2:2 ITU-656, GRB 4:2:2 & RGB Raw Data
- Wide dynamic range, anti-blooming, zero smearing
- Electronic exposure/gain/white balance control
- Image Controls - brightness, contrast, gamma, saturation, sharpness, windowing, hue, etc.
- Internal & external synchronization
- Line exposure option
- 3.3-Volt operation, low power dissipation
  - < 25 mA active power at 30FPS
  - < 10 μA in power-down mode
- Built in Gamma correction (0.45/0.55/1.00)
- SCCB programmable:
  - Color saturation, brightness, hue, white balance, exposure time, gain, etc.

Ordering Information

Product	Package	Description
OV7630	**28 LCC 0.450 in^2**	**COLOR, VGA, Digital, SCCB interface**
OV7130	**28 LCC 0.450 in^2**	**VGA, Digital, SCCB interface**

Applications

. Picture Phones
. Cell Phones
. Toys
. PC Multimedia
. PDA
. Digital Still Camera

Key Specifications

Array Element(VGA) (QVGA)	640x480 (320x240)
Pixel Size	5.6μm x 5.6μm
Image Area	3.6mm x 2.7mm
Max Frames/Sec	Up to 60 FPS for QVGA
Electronics Exposure	Up to 648:1 (for selected FPS)
Scan Mode	Progressive or Interlace
Gamma Correction	0.45/0.55/1.0
Min. Illumination (3000K)	OV7630 < 5 lux @ f1.2 OV7130 < 0.8 lux @ f1.2
S/N Ratio	> 48 dB (AGC off, Gamma=1)
FPN	< 0.03% V_{PP}
Dark Current	< 1.9nA/cm^2
Dynamic Range	> 72 dB
Power Supply	3.0–3.6VDC
Power Requirements	< 25mA Active < 10μA Standby
Package	28pin LCC

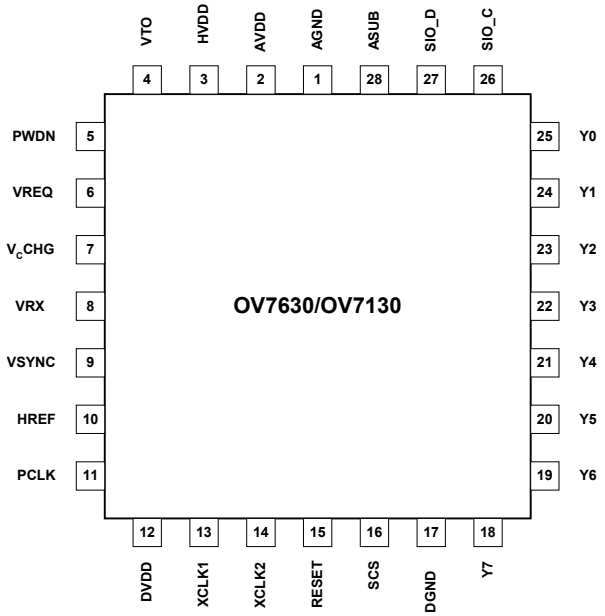

Figure 1. OV7630/OV7130 Pin Diagram

OmniVision Technologies, Inc. 930 Thompson Place Sunnyvale, CA 94085 U.S.A.
Tel: (408) 733-3030 Fax: (408) 733-3061
e-mail: info@ovt.com
Website: http://www.ovt.com

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Pin Description

Table 1. Pin Description

Pin No.	Name	Pin Type	Function/Description
01	AGND	P	Analog ground
02	AVDD	P	Analog power supply (+3.3VDC)
03	HVDD	V_{REF} (4V)	Charge-pump voltage. Connect to ground through 10μF capacitor.
04	VTO	O	Luminance composite signal output (black/white in NTSC standard).
05	PWDN	Function (Default=0)	Power-down mode selection. "0" – Normal mode. "1" – Power-down mode.
06	VREQ	V_{REF} (1.5V)	Array reference. Connect to ground through 0.1μF capacitor.
07	V_CCHG	V_{REF} (2.7V)	Internal voltage reference. Connect to ground through 1μF capacitor.
08	VRX	VREF(2.7V)	Internal voltage reference. Connect to ground through 1μF capacitor
09	VSYNC	O	Vertical sync output.
10	HREF	O	HREF output.
11	PCLK	O	PCLK (pixel clock) output.
12	DVDD	P	Digital power supply (+3.3VDC)
13	XCLK1	I	Crystal clock input
14	XCLK2	O	Crystal clock output
15	RESET	Function (Default=0)	Chip reset, active high
16	SCS	Function (Default=0)	SCCB-enable selection. "0" – Selects internal register setting control and enables SCCB interface. "1" – Disables register interface and all registers keep previous value.
17	DGND	P	Digital ground
18	Y7	O	Bit 7 of Y video component output.
19	Y6	O	Bit 6 of Y video component output.
20	Y5	O	Bit 5 of Y video component output.
21	Y4	O	Bit 4 of Y video component output.
22	Y3	O	Bit 3 of Y video component output.
23	Y2	O	Bit 2 of Y video component output.
24	Y1	O	Bit 1 of Y video component output.
25	Y0	O	Bit 0 of Y video component output.
26	SIO-C	I	SCCB serial interface clock input.
27	SIO-D	I/O	SCCB serial interface data input and output.
28	ASUB	P	Analog substrate ground.

Legend: (I=Input), (O=Output), (I/O=Bi-directional), (P=Power)

Electrical and Mechanical Characteristics

Table 2. General Characteristics

Descriptions	Min	Max	Units
Operating temperature (guaranteed performance)	0	40	°C
Operating temperature (chip functional)	-10	70	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 3. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Min	Typ	Max	Units
Supply					
V_{DD1}	Supply voltage (DEVDD, ADVDD, AVDD, SVDD, DVDD, DOVDD)	3.0	3.3	3.6	V
I_{DD2}	Supply current (V_{DD}=3V, @30Hz frame rate without digital I/O loading.		15		mA
I_{DD3}	Standby supply current		10	15	µA
Digital Inputs					
V_{IL}	Input voltage LOW	0.8		0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	PF
Digital Outputs (standard loading 25pF, 1.2KΩ to 3V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB Input					
V_{IL}	SIO-C and SIO-D (V_{DD2}=5V)	-0.5		1.5	V
V_{IH}	SIO-C and SIO-D (V_{DD2}=5V)	3.0	3.3	V_{DD}+0.5	V
V_{IL}	SIO-C and SIO-D (V_{DD2}=3V)	-0.5	0	1	V
V_{IH}	SIO-C and SIO-D (V_{DD2}=3V)	2.5	3	V_{DD}+0.5	V

Table 4. AC Characteristics (T_A=25°C, V_{DD}=3V)

Symbol	Descriptions	Min	Typ	Max	Units
RGB/YCrCb Output					
I_{SO}	Maximum sourcing current		15		mA
V_Y	DC level at zero signal Y_{PP} 100% amplitude (without sync) Sync amplitude		0.4 0.7 0.4		V
ADC Parameters					
B	Analog bandwidth				MHz
Φ_{DIFF}					
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB

Table 5. Timing Characteristics

Symbol	Descriptions	Min	Typ	Max	Units
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1, XCLK2)	10	20	40	MHz
t_r, t_f	Clock input rise/fall time			5	ns
	Clock input duty cycle	45	50	55	%
SCCB Timing (400Kbit/s)					
t_{BUF}	Bus free time between STOP and START	1.3			ms
$t_{HD:SAT}$	SIO-D change after START status	0.6			µs
t_{LOW}	SIO-D low period	1.3			µs
t_{HIGH}	SIO-D high period	0.6			µs
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:DAT}$	Data setup time	0.1			µs
$t_{SU:STP}$	Setup time for STOP status	0.6			µs
Digital Timing					
t_{PCLK}	PCLK cycle time	37			ns
t_r, t_f	PCLK rise/fall time			5	ns
t_{PDD}	PCLK to data valid			5	ns
t_{PHD}	PCLK to HREF delay	0	5	10	ns

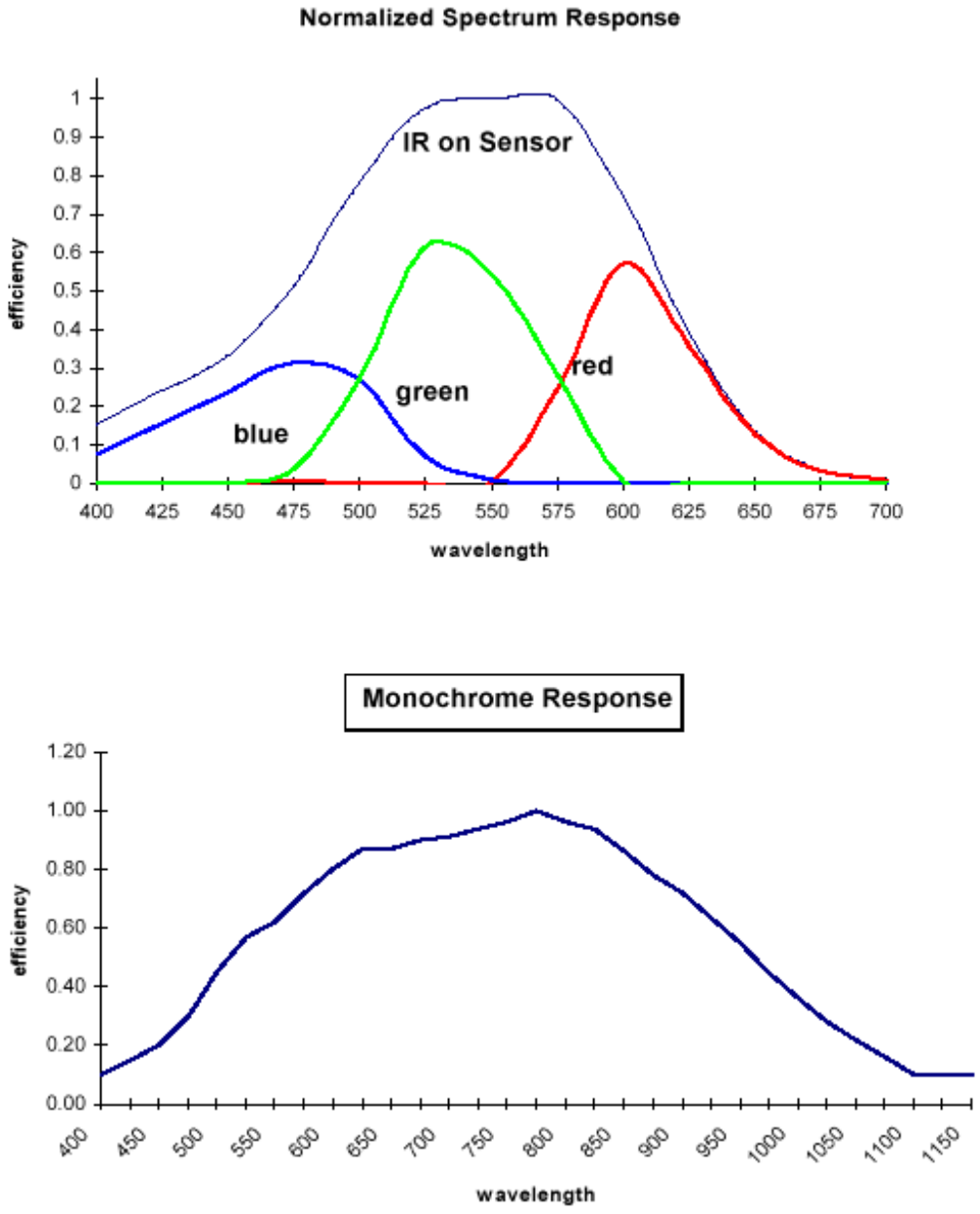


Figure 2. OV7630/7130 Light Response

Function Description

Overview

Referring to Figure 3 below, the OV7630/OV7130 sensor includes a 664 x 492 resolution image array, an analog signal processor, dual 8-bit A/D converters, analog video multiplexer, digital data formatter, video port, SCCB interface, registers, and digital controls that include timing block, exposure control, black level control, and white balance.

The OV7630/OV7130 sensor is a 0.25" CMOS imaging device. The sensor contains approximately 326,688 pixels (664x492). Its design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme. The color filter of the sensor consists of a primary color RG/GB array arranged in line-alternating fashion.

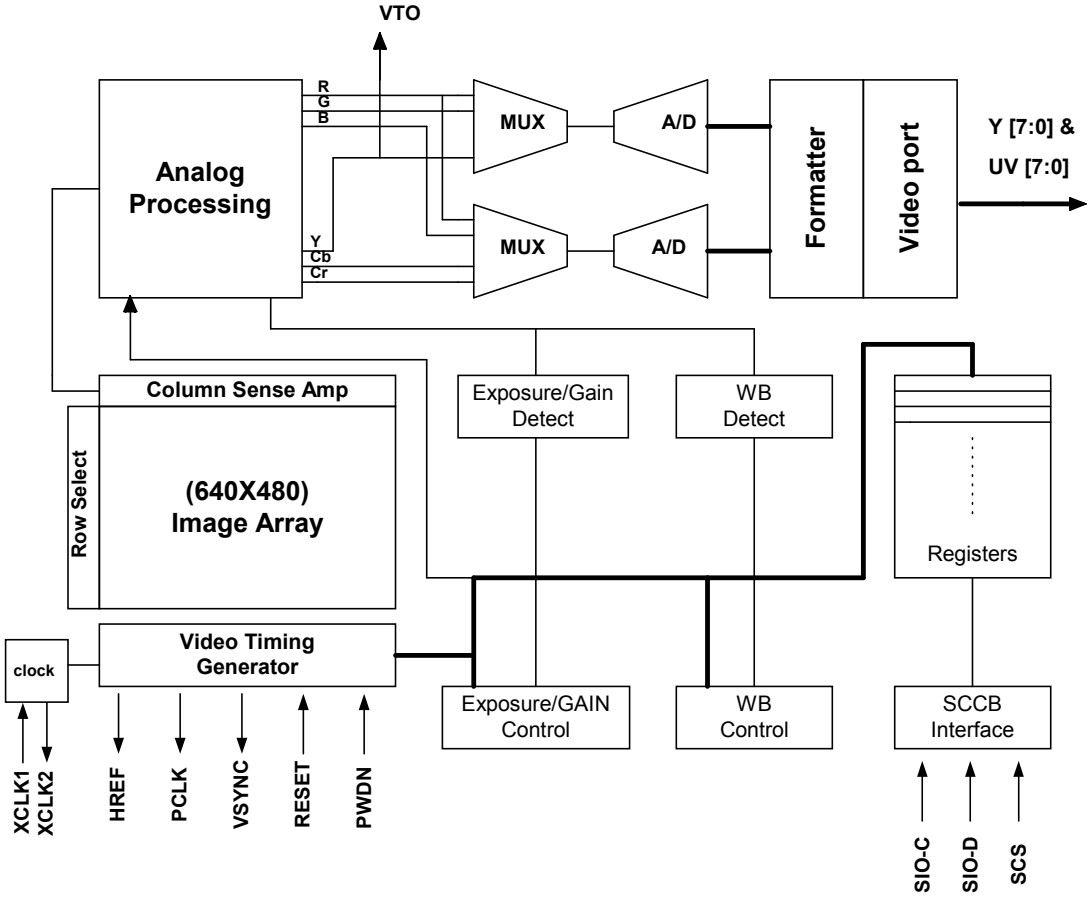


Figure 3. OV7630/OV7130 CMOS Image Sensor Block Diagram

Analog Processor Circuits

Overview

The image is captured by the 664 x 492 pixel image array and routed to the analog processing section where the majority of signal processing occurs. This block contains the circuitry that performs color separation, color correction, automatic gain control (AGC), gamma correction, color balance, black level calibration, "knee" smoothing, aperture correction, controls for picture luminance and chrominance, and hue control for color. The analog video signals are based on the following formula:

Y = 0.59G + 0.31R + 0.11B
U = B – Y
V = R – Y
Where R,G,B are the equivalent color components in each pixel.

YCrCb format is also supported, based on the formula below:

Y = 0.59G + 0.31R + 0.11B
Cr = 0.713 (R – Y)
Cb = 0.564 (B – Y)

The YCrCb/RGB data signal from the analog processing section is fed to two on-chip 10-bit analog-to-digital (A/D) converters: one for the Y/RG channel and one shared by the CrCb/BG channels. The converted data stream is further conditioned in the digital formatter. The processed signal is delivered to the digital video port through the video multiplexer which routes the user-selected 8-, or 4-bit video data to the correct output pins.

The on-chip 10-bit A/D operates at up to 12 MHz, and is fully synchronous to the pixel rate. Actual conversion rate is related to the frame rate. A/D black-level calibration circuitry ensures:

- The black level of Y/RGB is normalized to a value of 16
- The peak white level is limited to 240
- CrCb black level is 128
- CrCb Peak/bottom is 240/16
- RGB raw data output range is 16/240
  (Note: Values 0 and 255 are reserved for sync flag)

Image Processing

The algorithm used for the electronic exposure control is based on the brightness of the full image. The exposure is optimized for a "normal" scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the automatic exposure control (AEC) white/black ratio may be adjusted to suit the needs of the application.

Additional on-chip functions include:

- AGC that provides a gain boost of up to 24dB
- White balance control that enables setting of proper color temperature and can be programmed for automatic or manual operation.
- Separate saturation, brightness, hue, and sharpness adjustments allow for further fine-tuning of the picture quality and characteristics.

The OV7630/OV7130 image sensor also provides control over the White Balance ratio for increasing/decreasing the image field Red/Blue component ratio. The sensor provides a default setting that may be sufficient for many applications.

Windowing

The windowing feature of the OV7630/OV7130 image sensors allows user-definable window sizing as required by the application. Window size setting (in pixels) ranges from 2 x 2 to 640 x 480, and can be positioned anywhere inside the 662 x 492 boundary. Note that modifying window size and/or position does not change frame or data rate. The OV7630 imager alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical region. The default output window is 640 x 480.

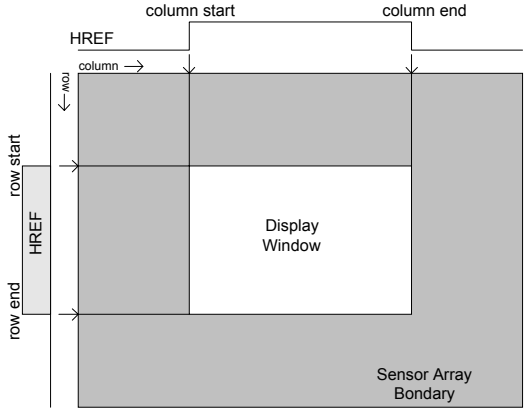


Figure 4. Windowing

QVGA Format

A QVGA mode is available for applications where higher resolution image capture is not required. Default resolution is 320 x 240 pixels. The entire array is subsampled for maximal image quality. Only half of the pixel rate is required when programmed in this mode.

Video Output

The video output port of the OV7630/OV7130 image sensors provides a number of output format/standard options to suit many different application requirements. Table 6, Digital

Output Format indicates the output formats available. These formats are user-programmable through the SCCB interface.

The OV7630/OV7130 imager supports output formats in the following configurations:

YUV Output

The OV7630/7130 supports ITU-656 YUV output format.

8-bit 4:2:2

The OV7630/OV7130 imager provides VSYNC, HREF, and PCLK, as standard output video timing signals.

ITU-656

In RGB raw data ITU-656 modes, the OV7630/OV7130 imager asserts SAV (Start of Active Video) and EAV (End of Active Video) to indicate the beginning and the ending of HREF window. As a result, SAV and EAV change with the active pixel window. 8-bit RGB raw data is also available without SAV and EAV encoding.

The OV7630/OV7130 imager offers flexibility in YUV output format. The device may be programmed as standard YUV 4:2:2. The device may also be configured to "swap" the U V sequence. When swapped, the 8-bit configuration becomes:

- V Y U Y···

Another swap format available in the 8-bit configuration is the Y/UV sequence swap:

- Y U Y V···

For YUV output, please refer to Tables 6-10, and Figure 5.

RGB Raw Data Output

The OV7630/7130 also supports two RGB raw data output formats.

RGB progressive scan mode

The OV7630/7130 outputs each line twice for each frame. Each horizontal SYNC outputs two lines of data. See Table 11 for details. The output clock rate will be double the rate of the pixel clock. The sequence for the output is BGRG···

Single Line Output

The OV7630/7130 supports single-line output, also known as one-line format. The sequence is BGBG for even lines and GRGR for odd lines. This format exactly matches the Bayer pattern color filter in the sensor array.

For RGB output, The OV7630/OV7130 imager also offers some format swaps:

- The device may be configured to "swap" the BR sequence. Which means the sequence is R G B G··· rather than BGRG ···
- Another swap format available is the Y/UV sequence can be swapped which means the sequence is GBGR···

The OV7630/OV7130 imager supports 8 bit 4:2:2 format for YUV and RGB RAW output formats in the following configurations. See Figure 5. , Pixel Data Bus (YUV Output) for further details):

- *8-bit data mode*

(In this mode, video information is output in Cb Y Cr Y order using the Y port only and running at twice the pixel rate. (See Table 7. 4:2:2 8-bit Format.)

B/W output

The single-chip camera can be configured for use as a black and white image device. The vertical resolution is higher than in color mode. Video data output is provided at the Y port.

The MSB and LSB of Y/UV or RGB output can be reversed. Y7 is MSB and Y0 is LSB in the default setting. Y7 becomes LSB and Y0 becomes MSB in the reverse order configuration. Y2-Y6 is also reversed appropriately.

For RGB formats please refer to Tables 2,7and Figure 6.

Table 6. Digital Output Format

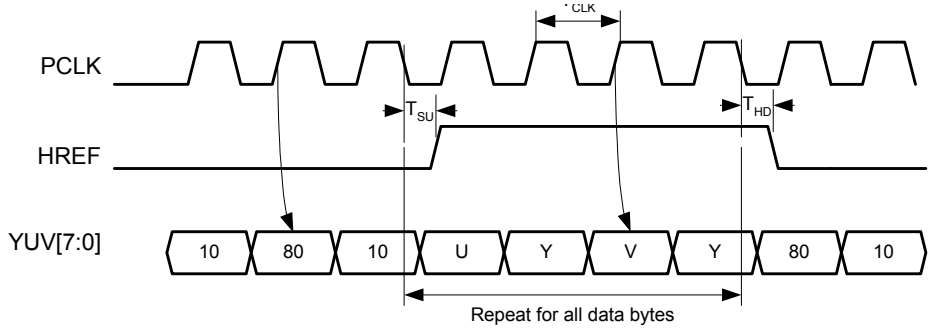
Resolution	Pixel Clock	640 x 480	320 x 240
YUV	8-bit	Y	Y
	ITU-656	Y	Y
RGB	8-bit	Y	Y
	ITU-656[1]	Y	Y
	Single-line	Y	Y
Y/UV swap[2]	YUV[3]	Y	Y
	RGB[4]	Y	Y
U/V swap	8-bit	Y	Y
Single Line	8-bit	Y	
MSB/LSB swap		Y	Y

Note:

- *("Y" indicates mode/combination is supported by OV7630/OV7130)*
- Output is 8-bit in RGB ITU-656 format. SAV and EAV are inserted at the beginning and ending of HREF, which synchronizes the acquisition of VSYNC and HSYNC. 8-bit data bus configuration (without VSYNC and CHSYNC) can provide timing and data in this format.
- Y/UV swap is valid in 8-bit format only. Y channel output sequence is Y U Y V ···
- U/V swap means neighbor row B R output sequence swaps in RGB format. Refer to RGB raw data output format for further details.

Table 7. 4:2:2 8-bit Format

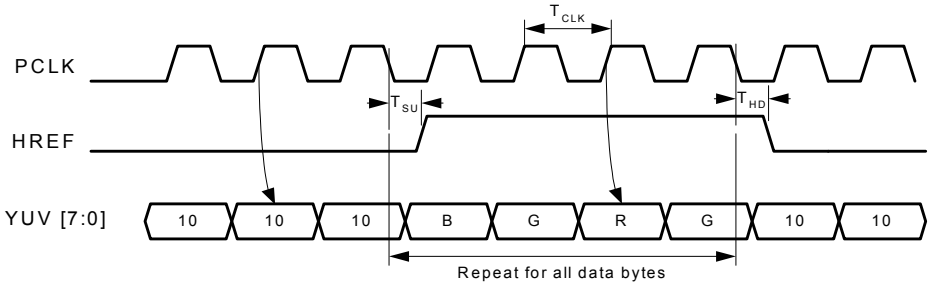
Data Bus	Pixel Byte Sequence							
Y7	U7	Y7	V7	Y7	U7	Y7	V7	
Y6	U6	Y6	V6	Y6	U6	Y6	V6	
Y5	U5	Y5	V5	Y5	U5	Y5	V5	
Y4	U4	Y4	V4	Y4	U4	Y4	V4	
Y3	U3	Y3	V3	Y3	U3	Y3	V3	
Y2	U2	Y2	V2	Y2	U2	Y2	V2	
Y1	U1	Y1	V1	Y1	U1	Y1	V1	
Y0	U0	Y0	V0	Y0	U0	Y0	V0	
Y Frame	0		1		2		3	
UV Frame	0 1				2 3			



Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

Note: *T_{CLK} is pixel clock period.. T_{CLK}=37ns for 8-bit output if the system clock is 27MHz . T_{SU} is the setup time of HREF. The maximum is 10ns. T_{HD} is the hold time of HREF. The maximum is 10ns.*

Figure 5. Pixel Data Bus (YUV Output)



Pixel Data 8-bit Timing
(PCLK rising edge latches data bus)

Note: *T_{CLK} is pixel clock period.. T_{CLK}=74ns for 8-bit output if the system clock is 27MHz . T_{SU} is the setup time of HREF. The maximum is 10ns. T_{HD} is the hold time of HREF. The maximum is 10ns.*

Figure 6. Pixel Data Bus (RGB Output)

The default U/UV channel output port relation before an MSB/LSB swap:

Table 8. Default Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The relation after an MSB/LSB swap changes to:

Table 9. Swapped MSB/LSB Output Sequence

	MSB							LSB
Output port	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Internal output data	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7

Table 10. QVGA Digital Output Format (YUV beginning of line)

Pixel #	1	2	3	4	5	6	7	8
Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
UV	U0, V0	U1, V1	U2, V2	U3, V3	U4, V4	U5, V5	U6, V6	U7, V7

- Y channel output U2Y2V3 Y3U6 Y6V7 Y7 U10Y10 V11Y11 ···
- Every other (total 320) pixel and every other line (total 240 lines) is output in each frame.

Table 11. RGB Data Format

The pixel pattern is as following:

R\C	1	2	3	4	···	641	642	643	644
1	$B_{1,1}$	$G_{1,2}$	$B_{1,3}$	$G_{1,4}$		$B_{1,641}$	$G_{1,642}$	$B_{1,643}$	$G_{1,644}$
2	$G_{2,1}$	$R_{2,2}$	$G_{2,3}$	$R_{2,4}$		$G_{2,641}$	$R_{2,642}$	$G_{2,643}$	$R_{2,644}$
3	$B_{3,1}$	$G_{3,2}$	$B_{3,3}$	$G_{3,4}$		$B_{3,641}$	$G_{3,642}$	$B_{3,643}$	$G_{3,644}$
4	$G_{4,1}$	$R_{4,2}$	$G_{4,3}$	$R_{4,4}$		$G_{4,641}$	$R_{4,642}$	$G_{4,643}$	$R_{4,644}$
491	$B_{491,1}$	$G_{491,2}$	$B_{491,3}$	$G_{491,4}$		$B_{491,641}$	$G_{491,642}$	$B_{491,643}$	$G_{491,644}$
492	$G_{492,1}$	$R_{492,2}$	$G_{492,3}$	$R_{492,4}$		$G_{492,641}$	$R_{492,642}$	$G_{492,643}$	$R_{492,644}$

- RGB full resolution progressive scan mode. (Total 492 HREFs)
  - 1st HREF Y channel output unstable data
  - 2nd HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{13}G_{23}$ R_{24} G_{14}···
  - 3rd HREF Y channel output B_{31} G_{21} R_{22} G_{32} B_{33} G_{23} R_{24} G_{34} ···
  - Every line of data is output twice for each frame.
  - PCLK is double
- RGB QVGA resolution progressive scan mode. (Total 246 HREFs)
  - 1st HREF Y channel output $B_{11}G_{21}$ R_{22} G_{12} $B_{15}G_{25}$ R_{26} G_{16}···
  - 2nd HREF Y channel output $B_{31}G_{41}$ R_{42} G_{32} $B_{35}G_{45}$ R_{46} G_{36}···
  - 3rd HREF Y channel output B_{51} G_{61} R_{62} G_{52} B_{55} G_{65} R_{66} G_{56} ···
  - Every line of data is output once for each frame.
  - Max frame rate is 60f/s
- RGB full resolution raw data one line format. (Total 492 HREFs)
  - 1st HREF Y channel output B_{11} G_{12} B_{13} G_{14} ···
  - 2nd HREF Y channel output G_{21} R_{22} G_{23} R_{24} ···
  - 3rd HREF Y channel output B_{31} G_{32} B_{33} G_{34} ···
  - PCLK rising edge latch data bus.
- RGB QVGA resolution raw data one line format. (Total 246 HREFs)
  - 1st HREF Y channel output B_{11} G_{12} B_{15} G_{16} ···
  - 2nd HREF Y channel output G_{21} R_{22} G_{25} R_{26} ···
  - 3rd HREF Y channel output B_{51} G_{52} B_{55} G_{56} ···
  - 3rd HREF Y channel output G_{61} R_{62} G_{65} R_{66} ···
  - PCLK rising edge latch data bus.

Frame Exposure Mode

OV7630/OV7130 supports frame exposure mode by set register 1F[6} to high. PWDN is asserted by an external master device to set exposure time at this mode. The pixel array is quickly pre-charged when PWDN is set to "1". OV7630/OV7130 captures the image in the time period when PWDN remains high. The video data stream is delivered to output port in a line-by-line manner after PWDN switches to "0".

It should be noted that PWDN must remain high long enough to ensure the entire image array has been pre-charged.

Reset

OV7630/7130 includes a RESET pin (pin 15) that forces a complete hardware reset when it is pulled high (VCC). OV7630/7130 clears all registers and resets to their default values when a hardware reset occurs. Reset can also be initiated through the SCCB interface.

Power Down Mode

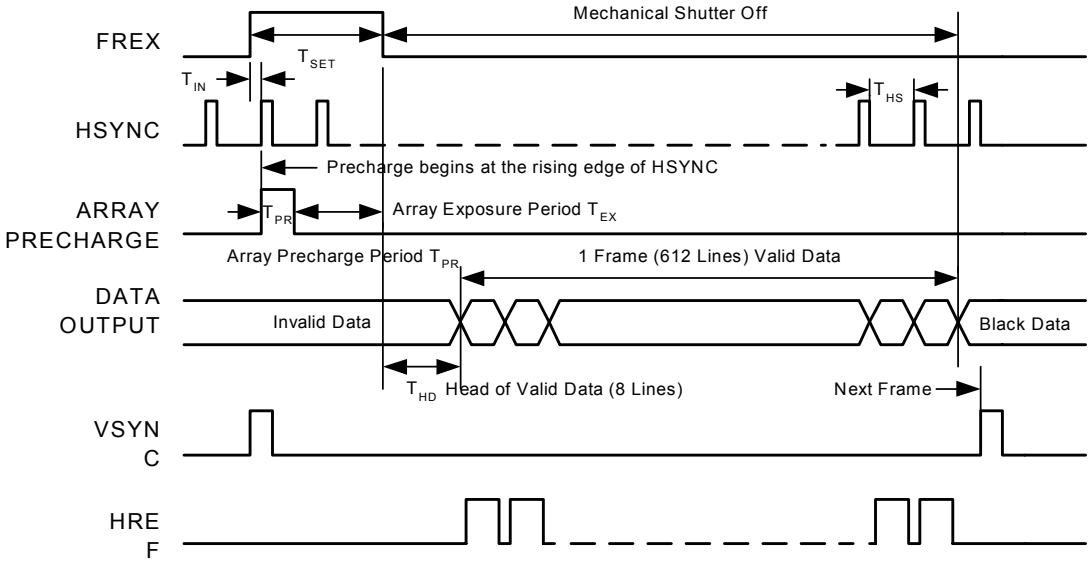
Two methods are available to place OV7630 into power-down mode: hardware power-down and SCCB software power-down. All internal register settings remain unchanged when OV7630/7130 is in the power-down mode.

To initiate hardware power-down, the PWDN pin (pin 5) must be tied to high (+3.3VDC). When this occurs, the OV7630 internal device clock is halted and all internal counters are reset. The current draw is less than 10μA in this standby mode.

Executing a software power-down through the SCCB interface suspends internal circuit activity, but does not halt the device clock. The current requirements drop to less than 1mA in this mode.

Configure OV7630/OV7130

The on-chip SCCB register programming capability provides a flexible and comprehensive method of configuring OV6640. The SCCB interface provides access to all of the device's programmable internal registers.



Note:

- *T_{PR}=612 x 4 x T_{CLK} or T_{PR}=858xT_{clk} depends on mode selecton. T_{CLK} is internal pixel period. T_{CLK}=74ns if the system clock is 27MHz . T_{CLK} will increase with the clock divider CLK[5:0].*
- *T_{EX} is array exposure time which is decided by external master device.*
- *T_{IN} is uncertain time due to the using of HSYNC rising edge to synchronize FREX. T_{IN} < T_{HS}.*
- *There are 8 lines data output before valid data after FREX=0. T_{HD}=4 THS. Valid data is output when HREF=1.*
- *T_{SET}=T_{IN} + T_{PR} + T_{EX}. T_{SET} > T_{PR} + T_{IN}. The exposure time setting resolution is T_{HS} (one line) due to the uncertainty of T_{IN}.*

Figure 7. Frame Exposure Timing

Register Set

The table below provides a list and description of available SCCB registers contained in the OV7630/7130 image sensor.

Table 12. SCCB Registers

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
00	GAIN	00	RW	AGC gain control GC[7:6] – Unimplemented. GC[5:0] – The current gain setting. *This register is updated automatically if AGC is enabled. The internal controller stores the optimal gain value in this register. The current value is stored in this register if AGC is not enabled.*
01	BLUE	80	RW	Blue gain control BLU[7:0] – blue channel gain balance value. "FFh" is highest and "00h" is lowest ***Note:*** *This function is not available on the OV7130 image sensor.*
02	RED	80	RW	Red gain control RED[7:0] – red channel balance value. "FFh" is highest and "00h" is lowest ***Note:*** *This function is not available on the OV7130 image sensor.*
03	SAT	80	RW	Color saturation control SAT[7:4] – Saturation adjustment. "F0h" is highest and "00h" is lowest. SAT[3:0] – Unimplemented. ***Note:*** *This function is not available on the OV7130 image sensor.*
04	HUE	10	RW	Color hue control HUE[7:6] – Unimplemented. HUE[5] – Enable HUE control HUE[4:0] – HUE control, range -30°~30°
05	CNT	20	RW	Contrast control CNT[7:6] – Unimplemented. CNT[5] – Enable contrast control CNT[4:0] – Contrast control, range 0.6 ~ 1.6
06	BRT	80	RW	Brightness control BRT[7:0] – Brightness adjustment. "FFh" is highest and "00h" is lowest.
07-09	Rsvd 07-09	××	–	Reserved
0A	PID	76	R	Product ID number read only
0B	VER	30	R	Product version number, read only
0C	ABLU	20	RW	White balance background: Blue channel ABLU[7:6] – Rsvd ABLU[5:0] - White balance blue ratio adjustment, "3Fh" is most blue. ***Note:*** *This function is not available on the OV7130 image sensor.*
0D	ARED	20	RW	White balance background: Red channel ARED[7:6] – Rsvd ARED[4:0] - White balance red ratio adjustment, "3Fh" is most red. ***Note:*** *This function is not available on the OV7130 image sensor.*
0E-0F	Rsvd 0E-0F	Xx	-	Reserved
10	AEC	41	RW	Automatic exposure control. MSB [9:2], LSB [1:0] in COMO [1:0] AEC[9:0] - Set exposure time $T_{EX} = T_{LINE} \times AEC[9:0]$

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
11	CLKRC	00	RW	Clock rate control CLKRC[7:6] – Sync output polarity selection "00" – HSYNC=Neg, CHSYNC=Neg, VSYNC=Pos "01" – HSYNC=Neg, CHSYNC=Neg, VSYNC=Neg "10" – HSYNC=Pos, CHSYNC=Neg, VSYNC=Pos "11" – HSYNC=Pos, CHSYNC=Pos, VSYNC=Pos CLKRC[5:0] – Clock pre-scalar CLK = (MAIN_CLOCK / ((CLKRC[5:0] + 1) × 2)) / n Where n=1 if register [15], COMD[5] is set to "1" and n=2 otherwise.
12	COMA	24	RW	Common control A COMA[7] – SRST, "1" initiates soft reset. All registers are set to default values and chip is reset to known state and resumes normal operation. COMA[6] – MIRR, "1" selects mirror image COMA[5] – AGCEN, "1" enables AGC, COMA[4] – Digital output format, "1" Y U Y V Y U Y V other than UYVYUYVY COMA[3] – Select video data output: "1" - select RGB, "0" - select YCrCb COMA[2] – Auto white balance "1" - Enable AWB, "0" - Disable AWB COMA[1] – Color bar test pattern: "1" - Enable color bar test pattern COMA[0] – ADC BLC method : "1" – precise, "0" more stable but less precise ***Note:*** *COMA[3] is not programmable on the OV7130 image sensor.*
13	COMB	21	RW	Common control B COMB[7] – Use 24MHz clock other than 27MHz to generate 30f/s frame rate if "1". COMB[6] – Banding filter option. "1" – Main clock is 13.5Mhz/12Mhz. COMB[5] - Reserved COMB[4] – "1" - enable digital output in ITU-656 format COMB[3] – CHSYNC output. "0" - horizontal sync, "1" - composite sync. Only effective when Reg[71] <5> high. COMB[2] – "1" – Tri-state Y and UV bus. "0" - enable both bus COMB[1] – "1" – Enables AGC when set to "1". COMB[0] – "1" – Enables AEC when set to "1". ***Note:*** *COMB[5] is not programmable on the OV7130 image sensor.*
14	COMC	04	RW	Common control C COMC[7] – AWB threshold selection. "1" - More stable and less accurate, "0" – more accurate but less stable. COMC[6] – Reserved COMC[5] – QVGA digital output format selection. "1" - 320x240; "0" - 640x 480. COMC[4] – Field/Frame vertical sync output in VSYNC port selection: "1" - frame sync, only ODD field vertical sync; "0" - field vertical sync, effect in Interlaced mode COMC[3] – HREF polarity selection: "0" - HREF positive effective, "1" - HREF negative. COMC[2] – gamma selection: "1" - RGB Gamma on ; "0" - RGB gamma is 1. COMC[1:0] – reserved

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
15	COMD	01	RW	Common Control D COMD[7] – Output will be full range as 00 ~ FF. Otherwise 00 and FF reserved and flag bits. COMD[6] – PCLK polarity selection. “0” - OV7630/OV7130 output data at PCLK falling edge and data bus will be stable at PCLK rising edge; “1” - rising edge output data and stable at PCLK falling edge. COMD[5:4] – AWB step selection. This will has effect on stability and speed of AWB. “00”, 1 bit each step, total 256 steps. “10”, 2 bits each step, total 128 steps. “01” & “11”, 4 bits each step, total 64 steps. COMD[3] – Fast AEC step selection. “1” big step, “0” small step. Only effective COMD[2] high. COMD[2] – Fast AEC mode. The step is determined by COMD[3]. COMD[1] – Reserved COMD[0] – U V digital output sequence exchange control. 1 - U Y V Y ···; 0 - V Y U Y ···. ***Note:*** *COMD[0] is not programmable on the OV7130 image sensor.*
16	FSD	03	RW	Field slot division FSD[7:2] – Field interval selection. It has functional in EVEN and ODD mode defined by FSD[1:0]. It is disabled in OFF and FRAME mode. The purpose of FSD[7:2] is to divide the video signal into programmed number of time slots, and allows HREF to be active only one field in every FSD[7:2] fields. It does not affect the video data or pixel rate. FSD[7:2]=1 outputs one field every field. FSD[7:2]=2 outputs one field every two fields. All other fields output black reference. FSD[1:0] – field mode selection. Each frame consists of two fields: Odd and Even, FSD[1:0] define the assertion of HREF in relation to the two fields. “00” – OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register 13) “01” – Interlace mode: ODD mode; HREF is asserted in odd field only. Progressive mode: HREF is asserted in frame according FD[7:2] “10” – Interlace mode: EVEN mode; HREF is asserted in even field only. Progressive mode: HREF is asserted in frame according FD[7:2]. “11” – FRAME mode; HREF is asserted in both odd field and even field. FSD[7:2] disabled.
17	HREFST	2D	RW	Horizontal HREF start HS[7:0] – selects the starting point of HREF window, each LSB represents four pixels for VGA resolution mode, two pixels for QVGA resolution mode, one pixel for QQVGA mode. This value is set based on an internal column counter. The default value corresponds to 640 horizontal windows. Maximum window size is 662. HS[7:0] should be less than HE[7:0].
18	HREFEND	CD	RW	Horizontal HREF end HE[7:0] – selects the ending point of HREF window, each LSB represents four pixels for full resolution and two pixels for QVGA resolution, one pixel for QQVGA mode. This value is set based on an internal column counter. The default value corresponds to the last available pixel. HE[7:0] should be larger than HS[7:0].
19	VSTRT	06	RW	Vertical line start VS[7:0] – selects the starting row of vertical window, in full resolution mode, each LSB represents 2 scan line in one field for Interlaced Scan Mode, 4 scan line in one frame for Progressive Scan Mode. In QVGA mode, each LSB represents 1 scan line in one field for Interlaced Mode, 2 scan line in one frame for Progressive Scan Mode. See window description below. Min. is [02], max. is [98] and should less than VE[7:0].

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
1A	VEND	F6	RW	Vertical line end VE[7:0] – selects the ending row of vertical window, in full resolution mode, each LSB represents 1 scan line in one field for Interlaced Scan Mode, 2 scan line in one frame for Progressive Scan Mode. In QVGA mode, each LSB represents 1 scan line in one field for interlaced Mode, 2 scan line in one frame for Progressive Scan Mode. See window description below. Min. is [03], max. is [98] and should be larger than VS[7:0].
1B	PSHFT	00	RW	Pixel shift PS[7:0] – to provide a way to fine tune the output timing of the pixel data relative to that of HREF, it physically shifts the video data output time late in unit of pixel clock. This function is different from changing the size of the window as defined by HS[7:0] and HE[7:0] in registers 17 and 18. It just delays the output pixels relative tp HREF and does not change the window size. The highest number is “FF” and the maximum shift number is delay 256 pixels.
1C	MIDH	7F	R	Manufacture ID byte: High MIDH[7:0] – read only, always returns “7F” as manufacturer’s ID no.
1D	MIDL	A2	R	Manufacture ID byte: Low MIDL[7:0] – read only, always returns “A2” as manufacturer’s ID no.
1E	OPTL	00	RW	Reserved
1F	SOFT	00	RW	Soft reset option for array. SOFT[7] Frame exposure reset method option. “1” Whole array reset at the same time. “0” Line reset. Only effective when SOFT[6] high SOFT[6] Frame exposure option. SOFT[5] The gap of AEC/AGC when exposure time less than 8 lines. “1” large gap. SOFT[4:1] Reserved SOFT[0] Array soft reset.
20	COME	80	RW	Common control E COME[7] – Reserved COME[6] – Field/Frame luminance average value caculationg enable. Value is stored in Reg. [7C], AVG [7:0]. COME[5] – Reserved. COME[4] – “1” Aperture correction enable. Correction strength and threshold value will be decided by COMF[7] ~ COMF[4]. COME[3] – AWB smart mode enable. 1 – do not count pixels that their luminance level are not in the range defined in register [66]. 0 - count all pixels to get AWB result. Valid only when COMB[0]=1 and COMA[2]=1. COME[2] – Enable AWB manual adjustable in auto mode. COME[1] – AWB fast/slow mode selection. “1” - AWB is always fast mode, that is register [01] and [02] is changed every field. “0” AWB is slow mode, [01] and [02] change every 16/ 64 field decided by COMK[1]. When AWB enable, COMA[2]=1, AWB is working as fast mode until it reaches stable, than as slow mode. COME[0] – Digital output driver capability increase selection: “1” Double digital output driver current; “0” low output driver current status. ***Note:*** *COME[3] and COME[1] are not programmable on the OV7130 image sensor.*
21	YOFF	80	RW	Y channel offset adjustment YOFF[7] – Offset adjustment direction 0 - Add Y[6:0]; 1 -Subtract Y[6:0]. YOFF[6:0] –Y channel digital output offset adjustment. Range: +127 ~ -127. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through SCCB has no effect. COMG[2]=1, Y channel offset adjustment will use the stored value which can be changed through SCCB. This register has no effect to ADC output data if COMF[1]=0. If output RGB raw data, this register will adjust G channel data.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
22	UOFF	80	RW	U Channel offset adjustment UOFF[7] – Offset adjustment direction: 0 - Add U[6:0]; 1 - Subtract U[6:0]. UOFF[6:0] – U channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through SCCB has no effect. COMG[2]=1, U channel offset adjustment will use the stored value which can be changed through SCCB. This register has no effect to ADC output data if COMF[1]=1. If output RGB raw data, this register will adjust B channel data. ***Note:*** *This function is not available on the OV7130 image sensor.*
23	CLKC	DE	RW	Oscillator circuit and common mode control CLKC[7:6] – Select different crystal circuit power level (“11” = minimum). CLKC[5] – ADC current control, “1” – half current, “0” full current. CLKC[4] – Optical black level register update option. “1” automatically update OPBLC[7:0] (1E[7:0]), which is the optical black level; “0” disable this function and OPBL[7:0] no use. CLKC[3:2] – Reserved. CLKC[1] – QVGA format clock option. Only in QVGA one line mode. Not recommend to change it by users. CLKC[0] – Data output every other two line. QVGA one line mode only.
24	AEW	10	RW	Automatic exposure control: Bright pixel ratio adjustment AEW[7:0] – Used as calculate bright pixel ratio. OV7630/OV7130 AEC algorithm is count whole field bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is on the range of the ratio defined by the register [24] and [25], image stable. This register is used to define bright pixel ratio, default is 25%, each LSB represent step: 1.3% for interlace and 0.7% for progressive scan. Change range is: [01] ~ [9A]; Increase AEW[7:0] will increase bright pixel ratio. For same light condition, the image brightness will increase if AEW[7:0] increase. ***Note:*** *AEW[7:0] must combine with register [25] AEB[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] > [9A].*
25	AEB	8A	RW	Automatic Exposure Control: Black pixel ratio adjustment AEB[7:0] – used as calculate black pixel ratio. OV7630/OV7130 AEC algorithm is count whole field/ frame bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is in the range of the ratio defined by the register [24] and [25], image stable. This register is used to define black pixel ratio, default is 75%, each LSB represent step: 1.3% for interlace and 0.7 for progressive scan. Change range is: [01] ~ [9A]; Increase AEB[7:0] will increase black pixel ratio. For same light condition, the image brightness will decrease if AEB[7:0] increase. ***Note:*** *AEB[7:0] must e combined with register [24] AEW[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] > [9A].*
26	COMF	A2	RW	Common control F COMF[7:6] – Aperture correction threshold selection. Range is 1% to 6.4% of difference of neighbor pixel luminance. COMF[5:4] – Aperture correction strength selection. Range is 0 to 200% of difference of neighbor pixel luminance. COMF[3] – Reserved. COMF[2] – Digital data MSB/LSB swap. “1” LSB→bit7, MSB→bit0; “0” normal. COMF[1] – “1” digital offset adjustment enable. “0” disable. COMF[0] – “1” Output first 4/8 line black level before valid data output according Interlace/Progressive scan mode. HREF number will increase 4/8 lines relatively. “0” no black level output.

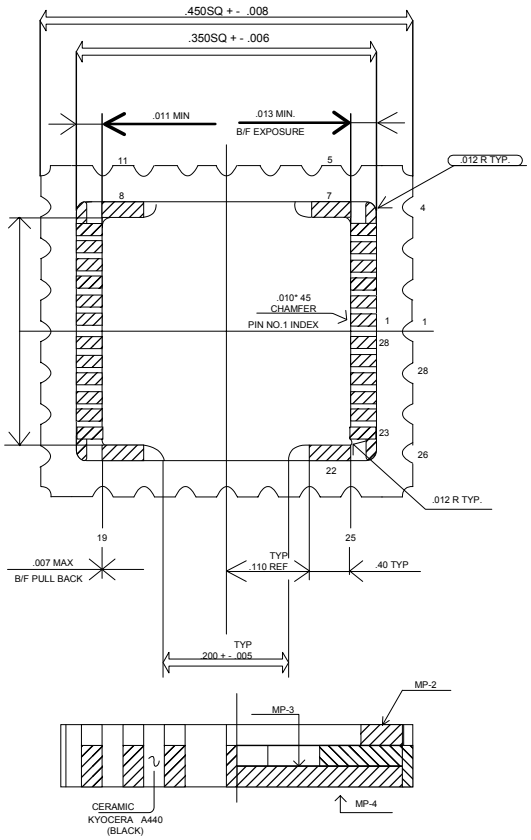
Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
27	COMG	E2	RW	Common control G COMG[7] – reserved. COMG[6] – Enable band gap reference for array other than diode reference. COMG[5] – Reserved. COMG[4] – By pass RGB matrix which is used to cancel the cross talk of color filter. COMG[3] – Enable ADC black level calibration offset define by register [78]~[7A]. COMG[2] – "1" digital offset adjustment manually mode enable. Digital data will be add/subtract a value defined by register [21], [22] and [2E], the contents are programmed through SCCB. "0" - digital data will be added/subtract a value defined by register [21], [22] and [2E], which are update by internal circuit. Effective only when COMF[1] high. COMG[1] – Digital output full range selection. OV7630/OV7130 default output data range is [10] - [F0]. The output range changes to [01] - [FE] with signal overshoot and undershoot level if COMG[1]=1. COMG[0] – Reserved.
28	COMH	00	RW	Common control H COMH[7] – "1" selects one-line RGB raw data output format, "0" selects normal two-line RGB raw data output. COMH[6] – "1" enable black/white mode. The vertical resolution will be higher than color mode when the imager works as BW mode. OV7630/OV7130 outputs data from Y port. COMB[4] will be set to "0". "0" normal color mode. COMH[5] – Progressive scan mode selection. "0" – Interlace, "1" Progressive. COMH[4] – Freeze AEC/AGC value, effective only at COMB[0]=1. "1" - register [00] and [10] will not be updated and hold latest value. "0" - AEC/AGC normal working status. COMH[3] – Reserved. COMH[2] – Reserved. COMH[1] – Gain control bit. "1" channel gain increases 3dB. "0" no change to the channel gain. COMH[0] – Reserved
29	COMI	34	RW	Common control I COMI[7] – Reserved. COMI[6] – Double clock rate 2X option. COMI[5:4] – Reserved. COMI[3] – Central 1/4 image area rather whole image used to calculate AEC/AGC. "0" use whole image area to calculate AEC/AGC. COMI[2] – Reserved. COMI[1:0] – Version flag. For version A, value is [00], these two bits are read only.
2A	FRARH	00	RW	Frame rate adjust high FRARH[7] – Frame rate adjustment enable bit. "1" Enable. FRARH[6:5] – Highest 2 bit of frame rate adjust control byte. FRARH[4] – UV delay 2 pixels if this bit high. FRARH[3] –Y brightness adjustment by manual. Effective only COMF[1]="1". FRARH[2] – Reserved. FRARH[1] – "1" When in Frame exposure mode, only One frame data output. FRARH[0] – Use internal average of luminance to determine the AEC/AGC rather than comparator counter.
2B	FRARL	00	RW	Frame rate adjust low FRARL[7:0] – Frame rate adjust control byte. Frame rate adjustment resolution is 0.12%. Control byte is 10 bit. Every LSB equal decrease frame rate 0.12%. Range is 0.12% - 112%.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
2C	EXBK	88	RW	Auto brightness ratio control EXBK[7:4] Ratio for auto brightness control. Range 0.06% ~ 3.85% EXBK[3:0] Ratio for auto brightness control. Range 0.06% ~ 3.85%. If the pixel that lower than reference level percentage is larger than EXBK[7:4]+EXBK[3:0], the brightness determined by reg[6] will decrease. If this percentage is less than EXBK[3:0], the brightness will increase. If this percentage is between EXBK[3:0] and EXBK[7:4]+EXBK[3:0], auto brightness will be stable.
2D	COMJ	81	RW	Common control J COMJ[7] – AEC update rate selection. “1” AEC update every 2 or 4 fields. “0” update every 1 field. COMJ[6] – QVGA format option. “1” Only odd field array data output and the read format is as interlaced, max frame rate is 60f/s. “0” every field array data output and the data is dropped every other line at digital format output, max frame rate is 30f/s. COMJ[5] – Reserved. COMJ[4] – Enable auto black expanding mode. COMJ[3] – Reserved COMJ[2] – Band filter enable. This bit enables a different exposure algorithm to cut light band induced by fluorescent light. COMJ[1:0] – Reserved.
2E	VCOFF	2C	RW	V channel offset adjustment VCOFF[7] – Offset adjustment direction: “0” = Add V[6:0]; “1” = Subtract V[6:0]. VCOFF[6:0] – V channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write to this register through SCCB has no effect. If COMG[2] =1, V channel offset adjustment will use the stored value which can be changed through SCCB. Only effective when COMF[1] =0. If output RGB raw data, this register will adjust R channel data. ***Note:*** *This function is not available on the OV7130 image sensor.*
2F	REF1	31	RW	REF1[7] – Internal doubler enable. REF1[6:0] -- Internal voltage reference control
30	REF2	38	RW	Internal voltage reference and current control. Not recommend user to change the value.
31	ARRAY	00	RW	Array work mode selection. Not recommend user to change the value.
32	DBL	06	RW	Double drive current control DBL[7:4] - double drive current control. Each bit represents 1x current drive capability. DBL[3:0] - Reserved.
33	BGP	08	RW	Band gap reference control. BGP[7] – Enable band gap reference function BGP[6:0] – Band gap reference adjustment control.
34~4B	Rsvd34 – 4B	xx	-	Reserved
4C	MEDC	00	RW	Medium filter option control MEDC[7] – AWB step and range x1.5 when this register is “1”. MEDC[6] – Reserved. MEDC[5] – Medium filter for RGB channel. MEDC[4] – Medium filter for Y channel controlled by AGC[5:0]. MEDC[3] – Reserved. MEDC[2:0] – Medium filter for Y channel component R/G/B controlled by manual respectively.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
4D	ADDC	00	RW	ADC converter option control ADDC[7:4] – reserved ADDC[3:2]—UV delay selection. “00” – no delay. “01” – no delay. “10” – 2tp delay. “11” 4tp delay. ADDC[1:0] Reserved.
4E—5F	Rsvd 4E—5F	××	-	Reserved
60	SPCA	00	RW	Signal process control A SPCA[7] – Channel 1.5x preamplifier gain enable. SPCA[6] – Analog half current selection. SPCA[5] – Gev/God switch instead of average for G in RGB and UV channel. SPCA[4] – Gev/God switch instead of average for Y channel in YUV mode SPCA[3:2] – Red channel preamplifier gain selection. “00” –1x, “01” –1.2x, “10” –1.4x, “11”-1.6x. SPCA[1:0] – Blue channel preamplifier gain selection. Same as above.
61	SPCB	80	RW	Signal process control B SPCB[7] – AGC/AEC feedback loop using Y channel. When RGB output must set it to “0”. SPCB[6:4] – Reserved. SPCB[3] – Enable RGB brightness control. SPCB[2] – Brightness control BRT[7:0] range and step half. SPCB[1:0] – Auto brightness reference level. “00” – 0IRE, “01” – 6IRE, “10” 10IRE, “11” 20IRE.
62~64	Rsvd 62—64	××	RW	RGB and Y gamma curve control. Not recommend to change the value for user.
65	SPCC	02	RW	Signal process control C SPCC[7:0] – Reserved for internal use.
66	AWBC	55	RW	AWB process control. AWBC[7:6] – Selectable highest luminance level to be available in AWB control. Pixels that value is larger than this threshold is excluded for AWB. AWBC[5:4] – Selectable lowest luminance level to be available in AWB control. Pixels that value is less than this threshold is excluded for AWB. Effective only when COME[3]=1 in AWBC[7:4]. AWBC[3:2] – Selectable U level to be available in AWB control. AWBC[1:0] – Selectable V level to be available in AWB control. Effective only when COMM[7]=1 in AWBC[3:0].
67	YMXB	01	RW	YUV matrix control. YMXB[7:6] – UV coefficient selection, u=B-Y, v=R-Y “00” - U=u. V=v. “01” – U=0.938u, V=0.838v “10” – U=0.563u, V=0.613v “11” – U=0.5u, V=0.877v YMXB[5] – Reserved. YMXB[4] – UV signal with 3 points average. YMXB[3:2] – Y delay selection. 0tp to 3tp. YMXB[1:0] – Reserved.
68	ARL	AC	RW	AEC/AGC reference level ARL[7:5] – Voltage reference selection (Higher voltage = brighter final stable image) “000” = Lowest reference level “111” = Highest reference level ARL[4:0] – Reserved

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
69	ADRC	42	RW	ADC reference adjustment and control bit ADRC[7:4] – ADC control bit. Not recommend to change the value. ADRC[3] – ADC range selection. “0” full range ADC is equal to about 0.6V analog level. “1” full rage ADC is equal to about 0.9V analog level. ADRC[2:0] – ADC reference control. This control will have effect on ADC signal range. Not recommend user to change the value
6A-6E	Rvsd 69-6E	xx	-	Reserved.
6F	EOC	00	RW	Even odd noise compensation. EOC[7] – Disable analog output at pin GYYO. EOC[6:5] – Reserved. EOC[4] – Sign of even/odd noise compensation. EOC[3:0] – Even/odd noise compensation value. Range 6.4 bits.
70	COMK	01	RW	Common mode control K COMK[7] – Enable one line output for optical black. COMK[6] – Output port drive current 2x larger option. COMK[5] – Aperture correction option. COMK[4:3] – Reserved. COMK[2] – Double Aperture correction strength. COMK[1] – 4x stable time less when in AWB slow mode. “1” AWB updates every 64 fields/frame. “0” AWB updates every 16 fields/frames. COMK[0] – Reserved.
71	COMJ	00	RW	Common control J COMJ[7] – Auto brightness update rate selection. “1” slow, “0” fast. COMJ[6] – PCLK output gated by HREF. COMJ[5] – Change CHSYNC output port to HREF. COMJ[4] – Reserved COMJ[3:2] – Highest 2 bit for HSYNC rising edge shift control. See register [72]. COMJ[1:0] – Highest 2 bit for HSYNC falling edge shift control. See register [73].
72	HSDY	10	RW	Horizontal SYNC rising edge shift COMJ[3:2], HSDY[7:0], HSYNC rising edge shift control. Range 000 to 35A, must be less than HEDY, step is 1 pixel.
73	HEDY	50	RW	Horizontal SYNC falling edge shift COMJ[1:0]&HEDY[7:0], HSYNC falling edge shift control. Range 000 to 35A, must be larger than HSDY, step is 1 pixel.
74	COMM	20	RW	Common mode control M COMM[7] – Enable UV smart AWB which threshold controlled by COMG[5]. COMM[6:5] – AGC maximum gain boost control. “00” – 6db, “01” – 12db, “10” – 6db, “11” – 18db COMM[4:0] – Reserved. COMM[3] – AEC update rate option. “1” 64/128/256 fields depend COMM[2:0]. “0” 32/64/128 fields depend COMM[2:0]. Effective only COMM[4]=1. COMM[2:0] – AEC update rate option. “100” every 32/64 fields according COMM[3]. “010” 64/128 fields according COMM[3]. “001” every 128/256 fields according COMM[3]. Other value is not valid.
75	COMN	02	RW	Common mode control N COMN[7] – Enables vertical flip. COMN[6:4] – Reserved for internal test mode. COMN[3] – Drop one field/frame when exposure line change is bigger than a fixed number. COMN[2] – Enable exposure go down to less than 1/120” in smooth AEC mode. COMN[1:0] – Reserved.

Sub-address (hex)	Register	Default (hex)	Read/ Write	Descriptions
76	COMO	01	RW	Common mode control O COMO[7] – Tri state output bus in power down mode when high. COMO[6] – Reserved. COMO[5] – Software power down mode. COMO[4] – Reserved. COMO[3] – Reserved COMO[2] – Tri-state all timing output except data line. COMO[1:0] – AEC LSBs [1:0].
77	AEGR	F3	RW	AEC/AGC fast mode threshold control. AEGR[7:4] – AEC/AGC fast mode high threshold control. Same as AEW[7:0]. AEGR[3:0] – AEC/AGC fast mode low threshold control. Same as AEB[7:0].
78	YBAS	80	RW	Y/G ADC offset YBAS[7:0] – Fixed offset to final Y/G data, range –128 to 128
79	UBAS	80	RW	U/B ADC offset UBAS[7:0] – Fixed offset to final U/B data, range –128 to 128
7A	VBAS	80	RW	V/R ADC offset VBAS[7:0] – Fixed offset to final V/R data, range –128 to 128.
7B	Rsvd 7B	××	-	Reserved
7C	AVG	00	RW	Field/Frame average level storage. Only effective COME[6]=1.
7D	COMP	77	RW	Common mode control P COMP[7] – Optical black line as black level calibration, effective only when . COMP[6] – Optical black line enable. COMP[5:3] – Reserved COMP[2] – VSYC drop option. “1” VSYNC will drop when frame data drop. “0” VSYN always exist. COMP[1:0] – Reserved
7E-7F	Rsvd 7E-7F	××	-	Reserved



Top View

Note:
Die thickness=0.024

Bottom View

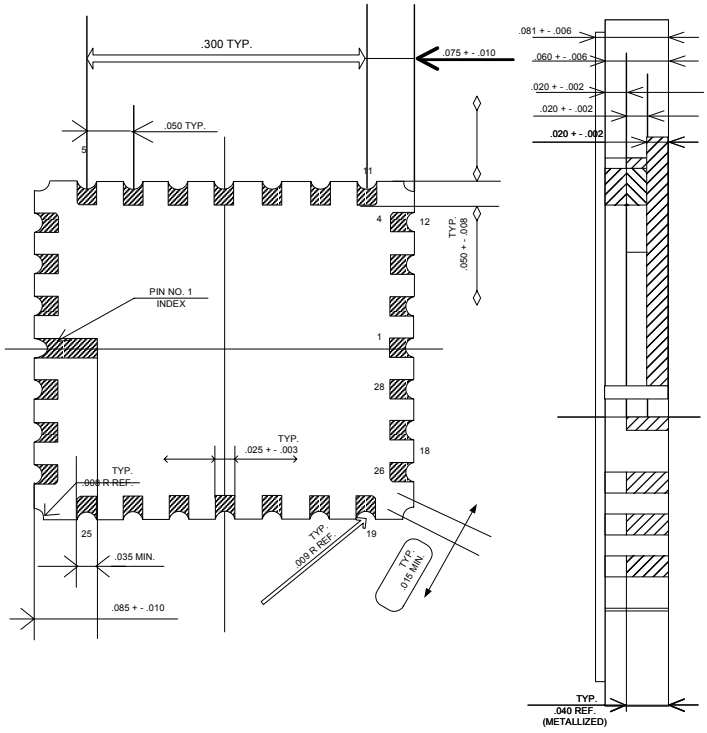


Figure 8. OV7630/OV7130 Package Diagram

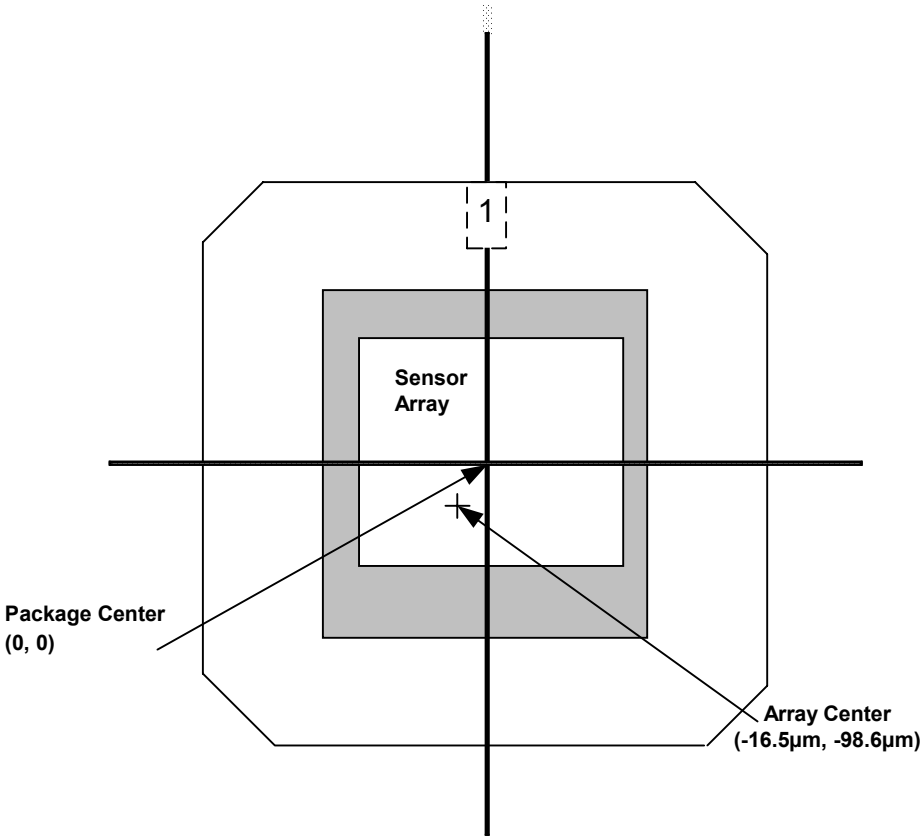


Figure 8. OV7630/7130 Sensor array center location

Note: *Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin one down.*