PC Camera Controller

1. General Description

The SN9C103 is a video/audio single-chip processor to pair with the resolution of VGA or CIF CMOS image sensor. It reads the 9 or 8 bits input raw image data (RGB Bayer pattern) from an image device and outputs through a USB port into the PC. This chip includes three individual digital color gains setting (named R, G, B gains), image compression engine, offset compensation, hardware windowing with random image size selection, panning and scaling functions and audio input interface.

2. Features

- 9-Bit CMOS image raw data input

- Up to 30fps @ CIF, 15fps @VGA for PC mode video

- Provide individual R/G/B digital color gains control

- Provide snapshot function

- Support pixel offset compensation

- Support *IC-media*, *TAS*C 5110/5130, *Hynix 7131D/E/G ,OmniVision, Pixart 106/202,Micron ,NS , CI sensor,* …etc

- Embedded two modes of AE calculation and report

- Built in microphone interface that include pre-amplifier , PGA and ADC

- Built in external EEPROM controller for customer V_ID,P_ID , defect pixel compensation and streaming setting

- Provide internal Up to 26 various P_ID in default setting

- Provide hardware windowing, 1/2, 1/4 scaling function with smooth filter and panning function

- Built in gamma correction and white balance gain circuit

- Support operation mode in image quality/frame rate selection

- USB 1.1 compliance and support suspend mode

- USB 5 endpoints: control, iso-chronous read, bulk read, and bulk write endpoints and audio class interface

- Support video data transfer either in USB iso-chronous or bulk modes

- Up to 9 alternated setting for USB iso-chronous transfer

- 12MHz crystal and 3.3Volt only

- 48 pins LQFP package

3. PIN description

Pin Location	NAME	I/O	Description
Sensor Interface(16 pins)			
4	S_IMG0	B	Sensor image data
3	S_IMG1	B	Sensor image data
2	S_IMG2	B	Sensor image data
1	S_IMG3	B	Sensor image data
46	S_IMG4	B	Sensor image data
45	S_IMG5	B	Sensor image data
44	S_IMG6	B	Sensor image data
43	S_IMG7	B	Sensor image data
42	S_IMG8	B	Sensor image data
12	SDA	B	I2C data
15	SCL	O	I2C clock
10	PCK	B	Sensor pixel clock
41	PWR_DN	O	Power down for sensor
7	S_CLK	O	System clock
9	VSYNC	B	Sensor vsync
8	HSYNC	B	Sensor hsync
Miscellaneous (12 pins)			
32	PID_SEL2	I	Product ID selection
31	PID_SEL1	I	Product ID selection
30	PID_SEL0	I	Product ID selection
29	KEY	I	KEY input
33	RST	I	chip reset
36	GPIO_0	B	General purpose I/O
35	GPIO_1	B	General purpose I/O
34	GPIO_2	B	General purpose I/O
28	TEST	I	test mode
11	LED	O	LED output
USB (4 pins)			
19	TAVSS	P	GND for USB part
18	DN	B	D- for USB
17	DP	B	D+ for USB
16	TAVDD	P	VDD for USB part
PLL & OSC (4 pins)			
40	VDDAP	P	VDD for PLL
39	XIN	I	OSC input

38	XOUT	B	OSC output
37	VSSAP	P	GND for PLL
Audio Input interface (7 pins)			
20	SIN_PREA1	I	Pre-amplifier input
22	SIN_PGA in	I	Programmable gain amplifier input
21	OUT_PREA1	O	Programmable gain amplifier output
27	REF_H	I	Higher level of reference voltage
25	REF_MID	I	Middle level of reference voltage
26	REF_L	I	Lower level of reference voltage

# I : input pin , O : output pin , B : bi-direction pin , P : power pin .

VID[15:0] = 16'h0c45

PID[15:6] = 10'b0110_0000_10 , PID[5:0] = PID_L, totally (3^3 -1) internal PID selected by PID_SEL[2:0]

```
case (PID_SEL)
3'b000:PID_L=6'b00_00_00; //6080      3'b100:PID_L=6'b11_00_00; //60b0      3'bz00:PID_L=6'b10_00_00; //60a0
3'b001:PID_L=6'b00_00_11; //6083      3'b101:PID_L=6'b11_00_11; //60b3      3'bz01:PID_L=6'b10_00_11; //60a3
3'b00z:PID_L=6'b00_00_10; //6082      3'b10z:PID_L=6'b11_00_10; //60b2      3'bz0z:PID_L=6'b10_00_10; //60a2
3'b010:PID_L=6'b00_11_00; //608c      3'b110:PID_L=6'b11_11_00; //60bc      3'bz10:PID_L=6'b10_11_00; //60ac
3'b011:PID_L=6'b00_11_11; //608f      3'b111:EEPROM_EN = 1;                 3'bz11:PID_L=6'b10_11_11; //60af
3'b01z:PID_L=6'b00_11_10; //608e      3'b11z:PID_L=6'b11_11_10; //60be      3'bz1z:PID_L=6'b10_11_10; //60ae
3'b0z0:PID_L=6'b00_10_00; //6088      3'b1z0:PID_L=6'b11_10_00; //60b8      3'bzz0:PID_L=6'b10_10_00; //60a8
3'b0z1:PID_L=6'b00_10_11; //608b      3'b1z1:PID_L=6'b11_10_11; //60bb      3'bzz1:PID_L=6'b10_10_11; //60ab
3'b0zz:PID_L=6'b00_10_10; //608a      3'b1zz:PID_L=6'b11_10_10; //60ba      3'bzzz:PID_L=6'b10_10_10; //60aa
```

4. **Block Diagram and Architecture Description**
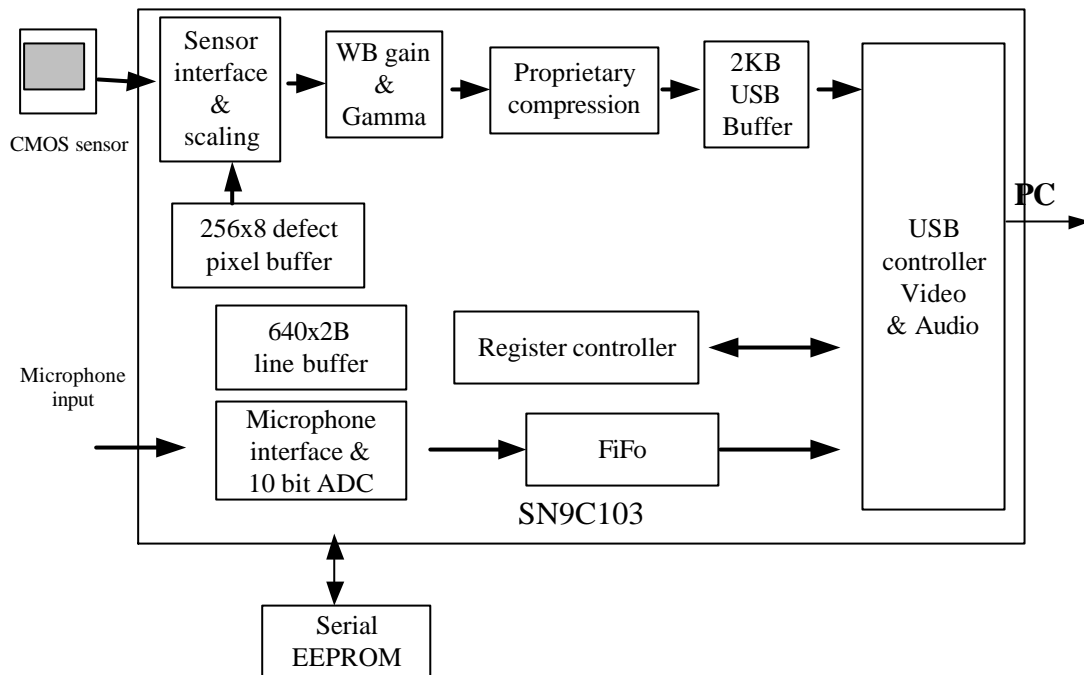
Function block diagram of SN9C103

Electrical Characteristics

DC Operating Condition

a. Absolute maximum ratings:

Symbol	Parameter	Rating	Units
Vcc	Power Supply	-0.3 to 3.6	V
Vin	Input Voltage	-0.3 to Vcc+0.3	V
Vout	Output Voltage	-0.3 to Vcc+0.3	V
Tstg	Storage Temperature	-55 to 150	°C

b. Recommended operating conditions:

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.0	3.3	3.6	V
Vin	Input voltage	0		Vcc	V
Topr	Operating Temperature	0		70	°C

c. DC electrical characteristics:

(Under Recommended Operating Conditions and Vcc=3.0 ~ 3.6V , Tj=0 to +115 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input low voltage	CMOS	-0.3		0.3Vcc	V
Vih	Input high voltage	CMOS	0.7Vcc		Vcc+0.3	V
Vil	Input low voltage	TTL	-0.3		0.8	V
Vih	Input high voltage	TTL	2.0		5.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	uA
Iih	Input high current	no pull-up or pull-down	-1		1	uA
Ioz	Tri-state leakage current		-1		1	uA
Vil	Schmitt input low voltage	CMOS		1.20		V
Vih	Schmitt input high voltage	CMOS		2.10		V
Vol	Output Low voltage	Iol=4mA			0.4	V
Voh	Output high voltage	Ioh=4mA	2.4			V
Cin	Input capacitance			2.8		pF
Cout	Output capacitance			2.7	4.9	pF
Cbid	Bi-directional buffer Capacitance			2.7	4.9	pF

AC Operating Condition

Symbol	Description	Max operation Frequency	Notes
S_CLK	System clock	48MHz	
XIN	Crystal input clock	12 MHz	
SCK	I2C clock frequency	400KHz	

7. Application Circuit

sensor interface
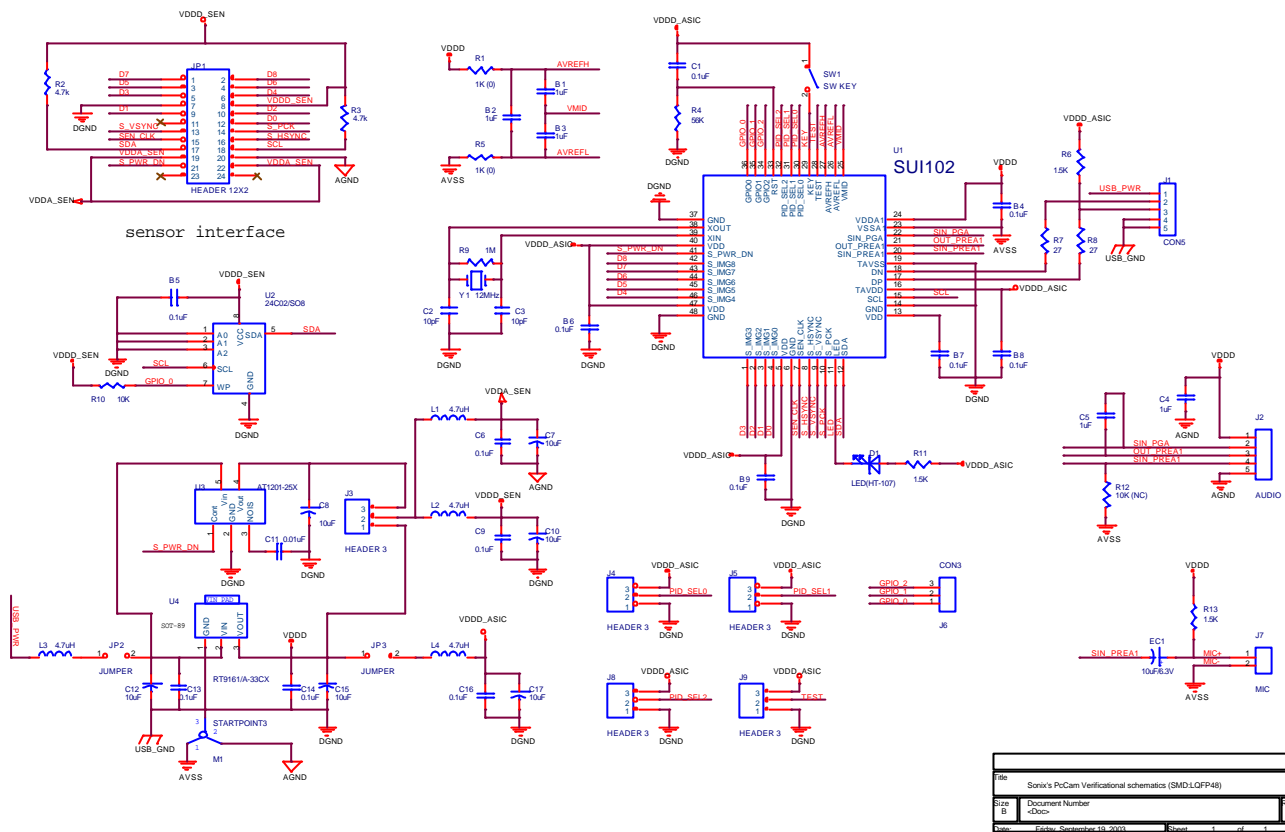
8. Package Dimension

● **48pin LQFP**
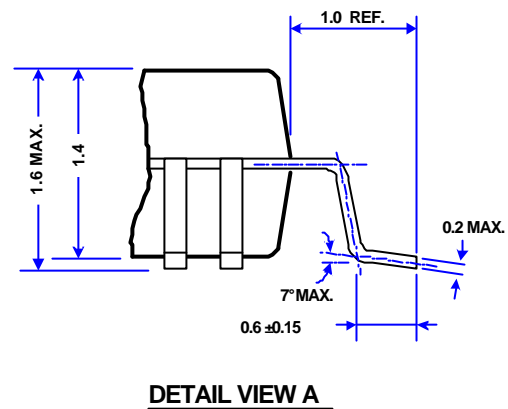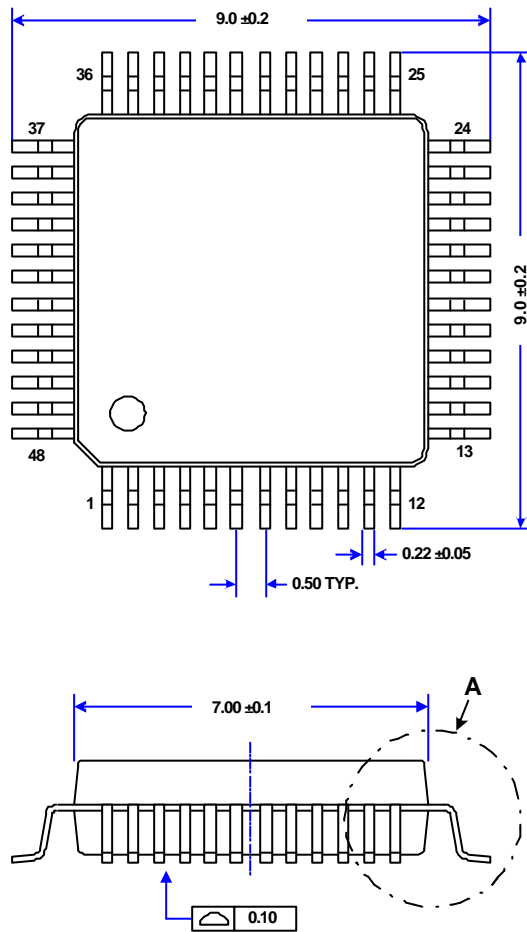
(All dimensions are in Millimeters)