

Circuit Theory and Electronics Fundamentals

T2 Laboratory Report

Group 34

José Bento, N^o 95815
Thomas Childs, N^o 95847
Luís Pacheco, N^o 96425

Aerospace Engineering (MEAer), Técnico, University of Lisbon

April 5, 2021

Contents

1	Introduction	3
2	Theoretical Analysis	4
2.1	Analysis for $t < 0$	4
2.2	Equivalent resistor as seen from the capacitor terminals	5
2.3	Natural solution for V_6	6
2.4	Forced solution for V_6 with $f = 1000Hz$	7
2.5	Final total solution $v_6(t)$	8
2.6	Frequency responses $v_c(f)$, $v_s(f)$ and $v_6(f)$ for frequency range 0.1 Hz to 1 MHz	9
3	Simulation Analysis	11
3.1	Operating Point Analysis for $t < 0$	11
3.2	Operating Point Analysis for $t = 0$	12
3.3	Natural solution for V_6 using transient analysis	13
3.4	Total solution for V_6 using transient analysis	14
3.5	Frequency response in node 6	15
4	Conclusion	16

1 Introduction

The objective of this laboratory assignment is to study a circuit containing a capacitor and a sinusoidal voltage source v_s . The value of this sinusoidal voltage source varies in time according to the following equations:

$$v_s(t) = V_s u(-t) + \sin(2\pi f t) u(t) \quad (1)$$

with

$$u(t) = \begin{cases} 0 & \text{if } t < 0 \\ 1, & \text{if } t \geq 0 \end{cases} \quad (2)$$

In this circuit there is also a linearly dependent voltage and current source. The circuit also contains 7 resistors.

The nodes of the circuit were numbered arbitrarily (from V_0 to V_7), and it was considered that *node 0* was the ground node. The voltage-controlled current source I_b has a linear dependence on Voltage V_b , of constant K_b . The voltage V_b is the voltage drop at the ends of resistor R_3 . The current-controlled voltage source V_d has a linear dependence on current I_d , of constant K_d . The control current I_d is the current that passes through the resistor R_6 . The circuit can be seen in **Figure 1**.

These values for the capacitance, resistors and the constants for the dependent sources were obtained using the Python script provided by the Professor and using the number 95815 as the seed. The seed number can be altered in the top Makefile (line 9). By doing so, all figures and tables will be updated according to the new values.

In Section 2, a theoretical analysis of the circuit is presented. Here the circuit is analysed for $t < 0$ using the nodal analysis and the equivalent resistance R_{eq} as seen from the capacitor terminals is determined. In this section both the natural and forced solutions for V_6 are also determined as well as the frequency responses for V_c , V_s and V_6 . In Section 3, the circuit is analysed by simulation using the program Ngspice. An operating point analysis is used to analyse the circuit when $t < 0$ and another one to determine the time constant. A transient analysis is used to determine the natural and forced responses on node 6. A frequency analysis is also performed on node 6. The conclusions of this study are outlined in Section 4, where the theoretical results obtained in Section 2 are compared to the simulation results obtained in Section 3.

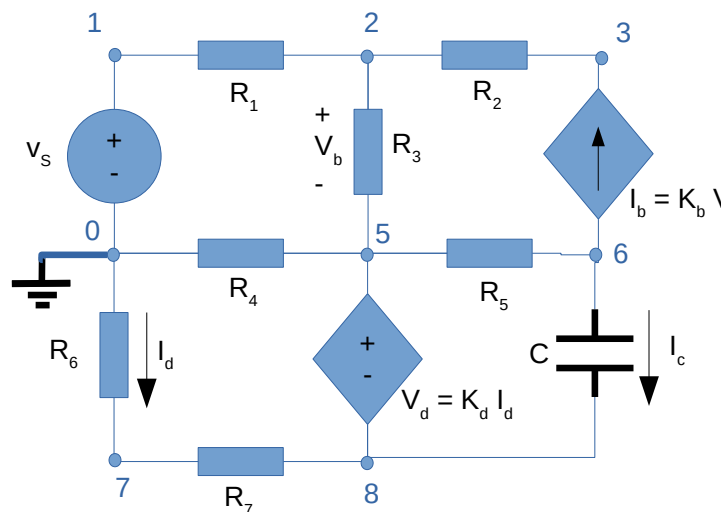


Figure 1: Circuit in study

2 Theoretical Analysis

In this section, the circuit shown in **Figure 2** is analysed theoretically.

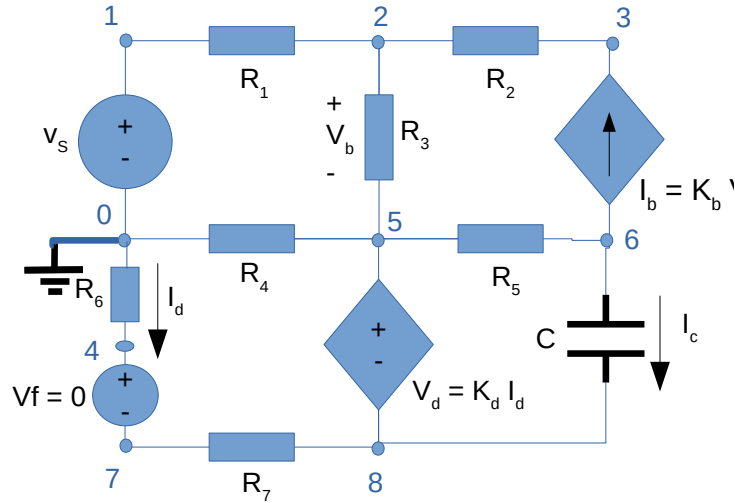


Figure 2: Diagram of the circuit considered for the computations and simulations

2.1 Analysis for $t < 0$

The nodal method is applied to the circuit in order to determine the voltage in all nodes and the current on all branches. The nodal method applies KVL and for $t < 0$ no current passes through the capacitor, and therefore this component behaves like an open circuit.

Name	Node method
Gb	2.658975828540764e-04
@r1	-2.536487650536384e-04
@r2	-2.658975828540766e-04
@r3	1.224881780043733e-05
@r4	1.205310280144243e-03
@r5	2.658975828540764e-04
@r6	-9.516615150906037e-04
@r7	-9.516615150906037e-04
v(0)	0.000000000000
v(1)	5.05481864136
v(2)	4.79370469182
v(3)	4.25819778407
v(4)	-1.93422555001
v(5)	4.83104709336
v(6)	5.66829837233
v(7)	-1.93422555001
v(8)	-2.90523132271

Table 1: A variable that starts with "Ir" and the variable "Gb" are of type *current* and expressed in milliampere (mA); all the other variables that start with a "V" are of the type *voltage* and expressed in Volt (V).

2.2 Equivalent resistor as seen from the capacitor terminals

To compute the equivalent resistance as seen by C the independent source V_c needs to be switched off. We do this by replacing it with a short circuit ($V_s = 0$). We also replace the capacitor with a voltage source $V_x = V_6 - V_8$. We use the V_6 and V_8 from the previous section because the voltage drop at the ends of the capacitor needs to be a continuous function (there can not be an energy spike in the capacitor). With this in mind a nodal analysis is performed in order to determine the current I_x that is supplied by V_x . With this values we can determine R_{eq} ($R_{eq} = V_x/I_x$). All this procedures were required in order to determine the time constant τ ($\tau = R_{eq} * C$). The time constant is crucial to determine the natural and forced solutions for V_6 , which will be done in the next subsections.

Name	Values for aux circuit
@r1	0
@r2	0
@r3	0
@r4	0
@r5	2.722815574850947e-03
@r6	0
@r7	0
v(0)	0.000000000000
v(1)	0.000000000000
v(2)	0.000000000000
v(3)	0.000000000000
v(4)	0.000000000000
v(5)	0.000000000000
v(6)	8.57352969504
v(7)	0.000000000000
v(8)	0.000000000000
Ix	-0.00272281557
Vx	8.57352969504
Req	-3148.773561540000
τ	-3.239206e-03

Table 2: A variable that starts with a "V" is of type *voltage* and expressed in Volt (V). The variable R_{eq} is expressed in Ohm and the variable τ is expressed in seconds

2.3 Natural solution for V_6

The natural solution depends on initial charge (voltage) and on R_{eq} and C and it is computed by removing all independent sources and applying KVL. In Octave to compute the Natural solution the general formula derived in the theoretical classes was used: $V_{6n}(t) = Ae^{\frac{-t}{\tau}}$. In this formula τ is the time constant determined in the previous section and A is a constant that can be determined through the boundry conditions (when $t = 0$, $A = V_x$)

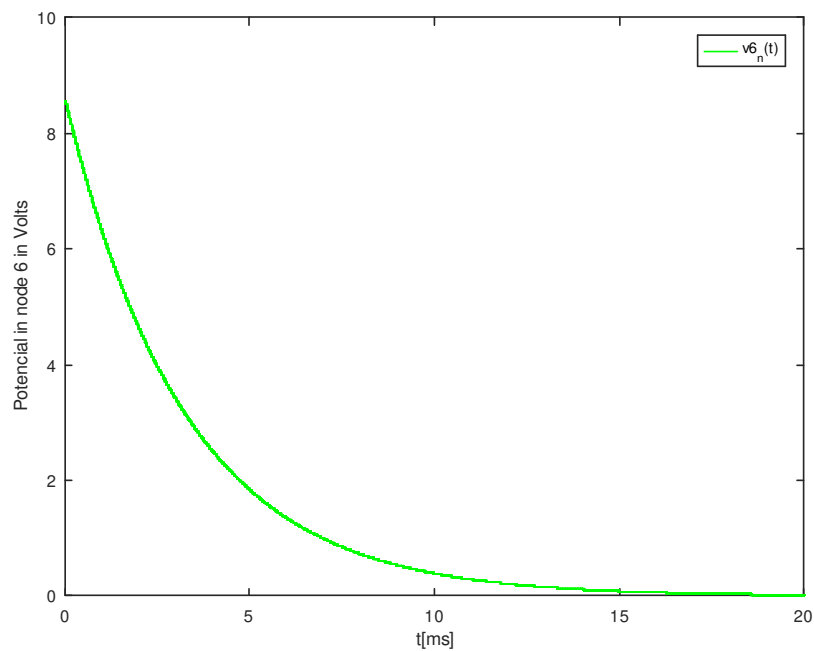


Figure 3: Natural response of V_6 as a function of time in the interval from [0,20] ms

2.4 Forced solution for V_6 with $f = 1000Hz$

In this section the forced solution V_{6f} is determined for the same time interval and for a frequency of 1KHz. To do this a nodal analysis was used but instead of resistances and capacitances, impedances were used. It was also considered that the magnitude of the phaser of the voltage source V_s was 1 ($V_s = 1$). By taking all these steps the phaser voltages in all nodes were determined. The complex amplitudes of the phasers are presented in **Table 3**

Name	Complex amplitude voltage
V0	0
V1	1
V2	9.483435572940677e-01
V3	8.424036718612813e-01
V4	3.826498411208256e-01
V5	9.557310432127906e-01
V6	5.766840995881649e-01
V7	3.826498411208256e-01
V8	5.747449174416580e-01

Table 3: Complex amplitudes in all nodes *****quais são as unidades da amplitude V ou m?*****

2.5 Final total solution $v_6(t)$

In this section the final total solution V_6 for a frequency of 1KHz is determined by superimposing the natural and forced solutions determined in previous sections ($V_6=V_{n6}+V_{6f}$) In **Figure: 4** the voltage of the independent font V_{st} and the voltage of V_6 were plotted for the time interval of $[-5,20]$ ms.

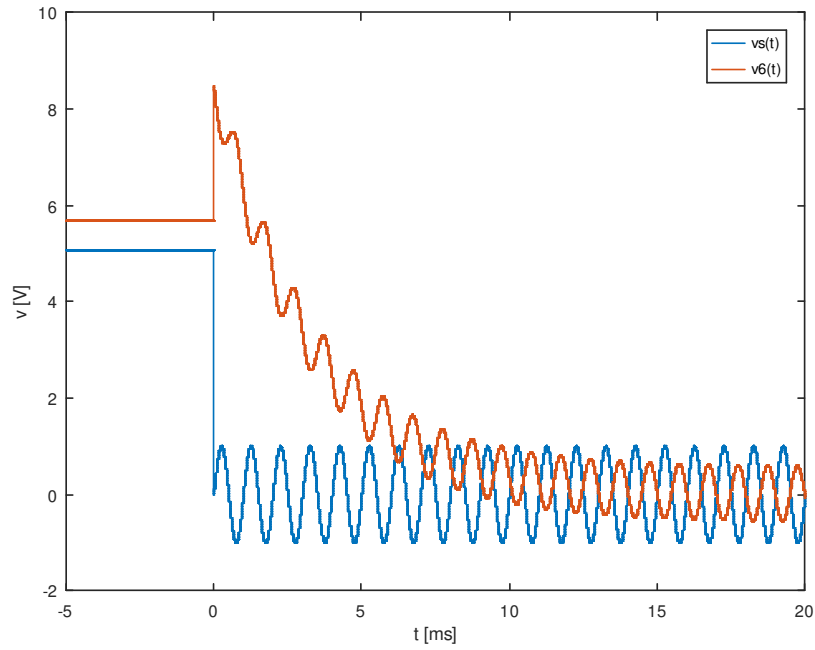


Figure 4: Voltage of $V_6(t)$ and $V_{st}(t)$ as functions of time from $[-5,20]$ ms

2.6 Frequency responses $v_c(f)$, $v_s(f)$ and $v_6(f)$ for frequency range 0.1 Hz to 1 MHz

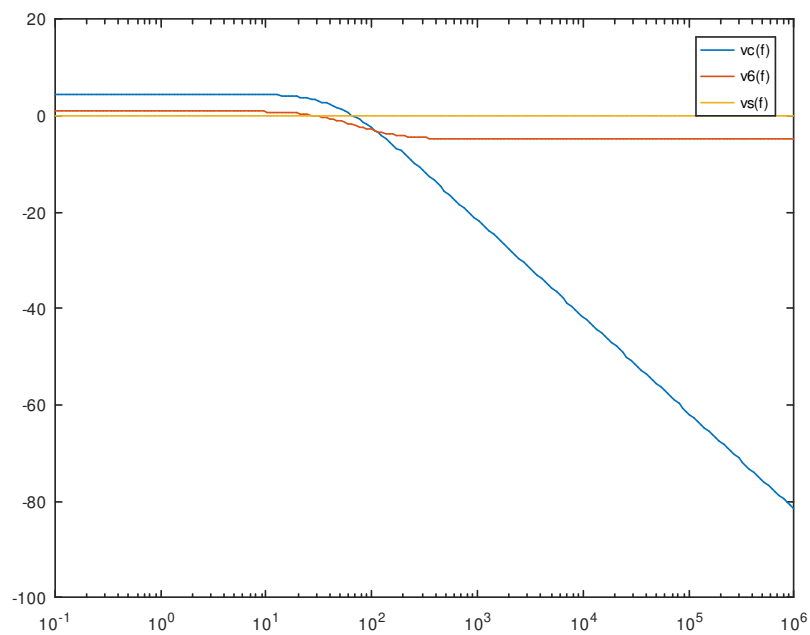


Figure 5: point 6: Graph for amplitude frequency response of V_c , V_6 and V_s for frequencies ranging from 0.1Hz to 1MHz

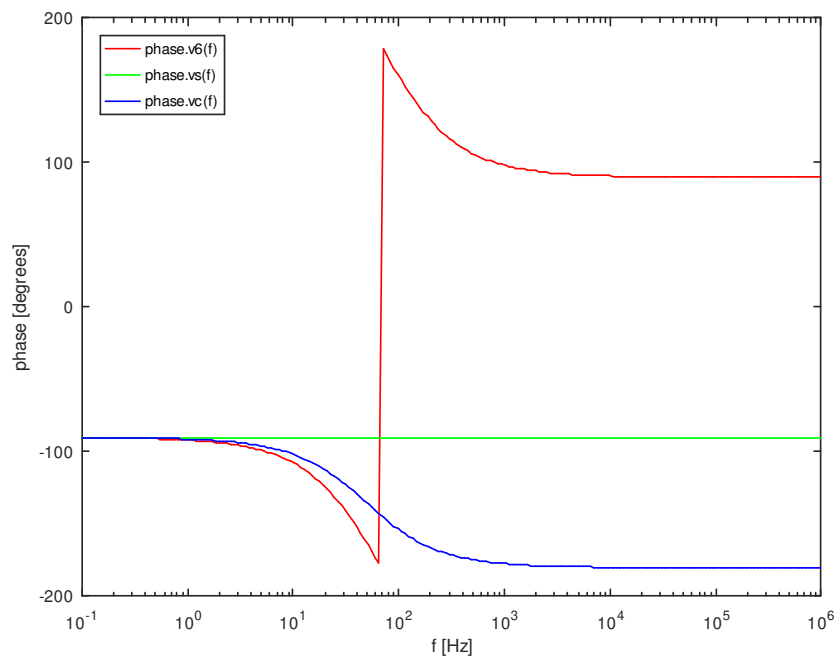


Figure 6: point 6: Graph for phase frequency response of V_c , V_6 and V_s for frequencies ranging from 0.1Hz to 1MHz

3 Simulation Analysis

In this section we will describe the steps needed to simulate this circuit using the software Ngspice. Three types of analysis will be performed: Operating Point analysis, Transient analysis and Frequency analysis.

The following steps in the simulations are to be conducted:

- for $t < 0$ (operating point only, in order to obtain the voltages in all nodes and the currents in all branches);
- operating point for $V_s(0) = 0$, replacing the capacitor with a voltage source $V_x = V_6 - V_8$, where V_6 and V_8 are the voltages in nodes 6 and 8 as obtained in the previous step (this step is necessary given that we must compute the boundary conditions that guarantee continuity in the capacitor's discharge - such may imply that the boundary conditions differ from those computed for $t_1(0)$);
- simulate the natural response of the circuit (using the boundary conditions $V(6)$ and $V(8)$ as obtained previously) using a transient analysis;
- repeating the third step, using V_s as given in **Figure 7** and $f = 1\text{kHz}$ in order to simulate for the total response on node 6
- simulate the frequency response in node 6 for a frequency range 0.1 Hz to 1MHz.

$$v_s(t) = V_s u(-t) + \sin(2\pi f t) u(t)$$

$$u(t) = \begin{cases} 0, & t < 0 \\ 1, & t \geq 0 \end{cases}$$

Figure 7: Time step conditions

3.1 Operating Point Analysis for $t < 0$

There was a need to create a "fictional" voltage source, between node 7 and resistor 6 (providing 0V to the circuit in order not to alter the behaviour of the rest of the circuit) so as to be able to define the dependency for the current-controlled voltage source V_d . This has no specific reason to be, other than the particularities of the Ngspice software. The circuit and nodes used for the simulation can be seen in **Figure 2**.

Table 4 shows the simulated operating point results for the circuit under analysis for $t < 0$.

Name	Value [mA or V]
@c[i]	0.000000e+00
@gb[i]	-2.65897e-04
@r1[i]	2.536486e-04
@r2[i]	2.658975e-04
@r3[i]	-1.22488e-05
@r4[i]	-1.20531e-03
@r5[i]	-2.65897e-04
@r6[i]	9.516617e-04
@r7[i]	9.516617e-04
v(1)	5.054819e+00
v(2)	4.793705e+00
v(3)	4.258199e+00
v(4)	-1.93423e+00
v(5)	4.831048e+00
v(6)	5.668299e+00
v(7)	-1.93423e+00
v(8)	-2.90523e+00

Table 4: Step 1: Operating point for t_0 . A variable preceded by @ is of type *current* and expressed in miliAmpere; other variables are of type *voltage* and expressed in Volt.

3.2 Operating Point Analysis for $t = 0$

Name	Value [mA or V and Ohm]
@gb[i]	6.332294e-18
@r1[i]	-6.04059e-18
@r2[i]	-6.33229e-18
@r3[i]	2.917029e-19
@r4[i]	-1.32956e-18
@r5[i]	-2.72282e-03
@r6[i]	8.673617e-19
@r7[i]	1.320008e-20
v(1)	0.000000e+00
v(2)	6.218372e-15
v(3)	1.897135e-14
v(4)	-1.76289e-15
v(5)	5.329071e-15
v(6)	8.573530e+00
v(7)	-1.76289e-15
v(8)	-1.77636e-15
Ix	-2.72282e-03
Vx	8.573530e+00
Req	-3.14877e+03

Table 5: Step 2: Operating point for $v_s(0) = 0$, with the capacitor replaced by a voltage source $V_x = V(6) - V(8)$ with these as obtained in the last step. A variable preceded by @ is of type *current* and expressed in miliAmpere; variables are of type *voltage* and expressed in Volt. The equivalent resistance is in Ohms

3.3 Natural solution for V_6 using transient analysis

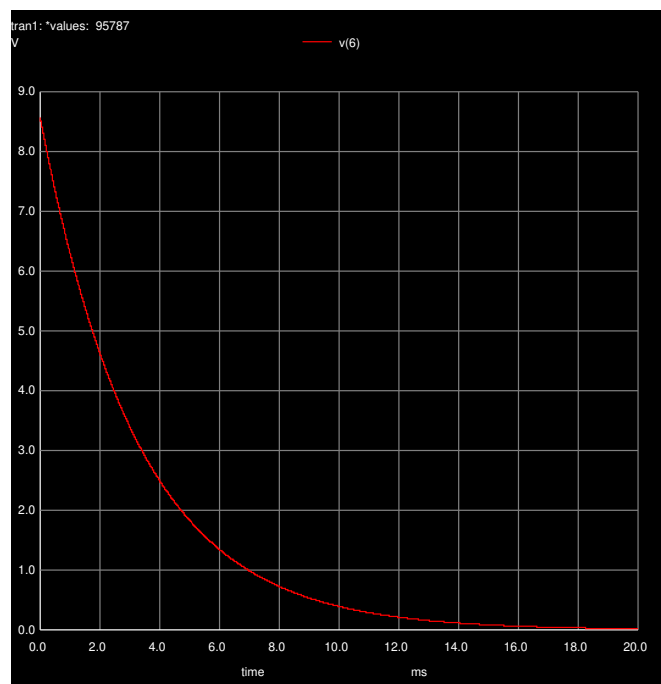


Figure 8: estudo transiente

3.4 Total solution for V_6 using transient analysis

3.5 Frequency response in node 6

4 Conclusion

In this laboratory assignment the objective of analysing a circuit containing a capacitor and a sinusoidal voltage source v_s that varies in time has been achieved .

Static analyses have been performed both theoretically, using the Octave maths tool, and by circuit simulation, using the Ngspice tool. Not only did the theoretical results obtained using different methods agree perfectly, they also matched the simulation results precisely.

The reason for this perfect match is the fact that this is a straightforward circuit containing only linear components - this implies, as pointed out in the theory classes, that the theoretical and simulation models cannot differ. For more complex components and circuits, the theoretical and simulation models could differ (given the greater complexity of the models implemented by the simulator Ngspice, when compared to those studied in the theoretical classes); however, that is not the case for this particular circuit.