TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

T2 Laboratory Report

Group 34

José Bento, Nº 95815
Thomas Childs, Nº 95847
Luís Pacheco, Nº 96425

Aerospace Engineering (MEAer), Técnico, University of Lisbon

April 5, 2021

Contents

1 Introduction

The objective of this laboratory assignment is to study a circuit containing a capacitor and a sinusoidal voltage source v_s.The value of this sinusoidal voltage source varies in time acording to the following equations:

$$v_s(t) = V_s u(-t) + sin(2\pi f t)u(t) \tag{1}$$

with

$$u(t) = \begin{cases} 0 & \text{if } t < 0 \\ 1, & \text{if } t \geq 0 \end{cases} \tag{2}$$

In this circuit there is also a linearly dependent voltage and current source. The circuit also contains 7 resistors.

The nodes of the circuit were numbered arbitrarily (from V_0 to V_7), and it was considered that *node 0* was the ground node. The voltage-controlled current source I_b has a linear dependence on Voltage V_b, of constant K_b. The voltage V_b is the voltage drop at the ends of resistor R_3. The current-controlled voltage source V_d has a linear dependece on current I_d, of constant K_d. The control current I_d is the current that passes through the resistor R_6. The circuit can be seen in **Figure 1**.

These values for the capacitance, resistors and the constants for the dependent sources were obtained using the Python script provided by the Professor and using the number 95815 as the seed.The seed number can be altered in **********. By doing so, all figures and tables will be updated acording to the new values.

In Section 2, a theoretical analysis of the circuit is presented.Here the circuit is analises for $t < 0$ using the nodal analysis and the equivalent resistence R_{eq} as seen from the capacitor terminals is determined. In this section both the natural and forced solutions for V_6 are also determined as well as the frequency responses for V_c, V_s and V_6. In Section 3, the circuit is analysed by simulation using the program Ngspice. A operating point analysis is used to analyse the circuit when $t < 0$ and to determine the time constant **********Acho que é por isto que se faz o ponto 2 da simulation analysis*******.A transient analysis is used to determine the natural and forced responses on node 6.A frequency analysis is also performed on node 6. The conclusions of this study are outlined in Section 4 , where the theorical results obtained in Section 2 are compared to the simulation results obtained in Section 3.

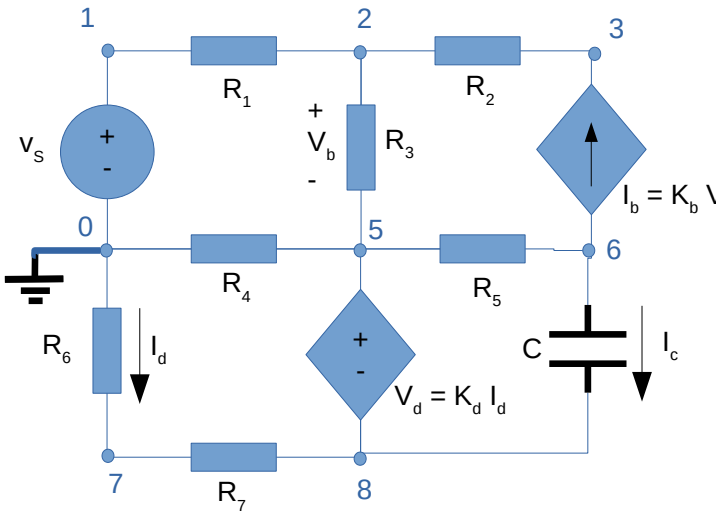

Figure 1: Circuit in study

2 Theoretical Analysis

In this section, the circuit shown in **Figure 2** is analysed theoretically.

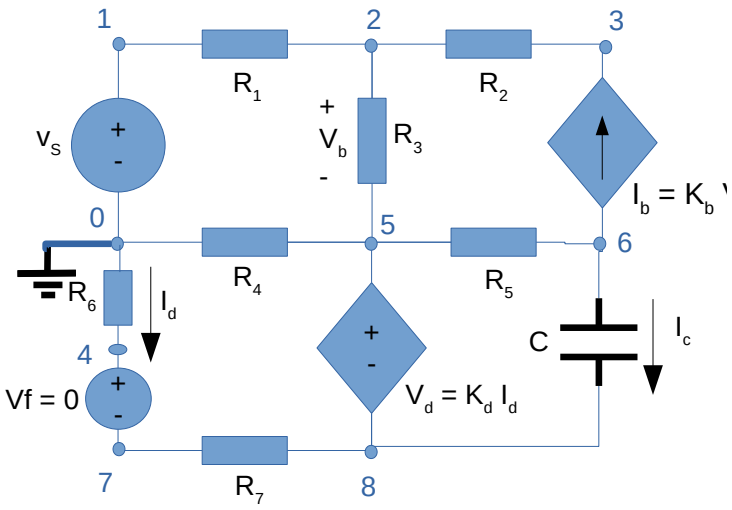

Figure 2: Diagram of the circuit considered for the computations and simulations

2.1 Analysis for $t < 0$

The nodal method is aplied to the circuit in order to determine the voltage in all nodes and the current on all branches . The nodal method aplies KVL and for $t < 0$ no current passes through the capacitor, and therefore this component behaves like an open circuit.******* sera que é a corrente ou é a voltagem que é nula?********

Name	Node method
V0	0
V1	5.054818641360000
V2	4.793704691824189
V3	4.258197784082119
V4	-1.934225550007436
V5	4.831047093349573
V6	5.668298372306746
V7	-1.934225550007436
V8	-2.905231322705667
Ir1	-2.536487650531725e-01
Ir2	-2.658975828505401e-01
Ir3	1.224881779736725e-02
Ir4	1.205310280142027
Ir5	2.658975828505403e-01
Ir6	-9.516615150888543e-01
Ir7	-9.516615150888547e-01
Gb	2.658975828505403e-01

Table 1: A variable that starts with "Ir" and the variable "Gb" are of type *current* and expressed in milliampere (mA); all the other variables that start with a "V" are of the type *voltage* and expressed in Volt (V).

2.2 Equivalent resistor as seen from the capacitor terminals

To compute the equivalent resistance as seen by C the independent source V_c needs to be switched off. We do this by replacing it with a short circuit ($V_s = 0$). We also replace the capacitor with a voltage source $V_x = V_6 - v_8$.We use the V_6 and V_8 from the previous section beacause the voltage drop at the ends of the capacitor needs to be a continuous function (there can not be an energy spike in the capacitor). With this in mind a nodal analysis is performed in order to determine the current I_x that is supplied by V_x.With this values we can determine R_{eq} ($R_{eq} = V_x/I_x$). All this procedures were required in order to determine the time constant τ ($\tau = R_eq * C$). The time constant in crucial to determine the natural and forced solutions for V_6, which will be done in the next subsections.

Name	Values for aux circuit
V0	0
V1	0
V2	0
V3	0
V4	0
V5	0
V6	8.573529695010000
V7	0
V8	0
Req	-3.148773561540000
τ	-3.239212e-03

Table 2: A variable preceded by @ is of type *current* and expressed in milliampere (mA); other variables are of type *voltage* and expressed in Volt (V).

Name	Complex amplitude voltage
V0	0
V1	1
V2	9.483435572941628e-01
V3	8.424036718627852e-01
V4	3.826498411201222e-01
V5	9.557310432110339e-01
V6	1.121194149101466
V7	3.826498411201222e-01
V8	5.747449174406016e-01

Table 3: The table for the complex amplitudes in point 4:

3 Simulation Analysis

In this section we will describe the steps needed to simulate this circuit using the software Ngspice.

3.1 Operating Point Analysis

Table 4 shows the simulated operating point results for the circuit under analysis. The current flows considered in the theoretical section were coherent with the polarity implicitly declared when defining the circuit to be simulated in the Ngspice script.

As mentioned previously, in Section 2, we had to create a ”fictional” voltage source, between node 7 and resistor 6 (providing 0V to the circuit in order not to alter the behaviour of the rest of the circuit) so as to be able to define the dependecy for the current-controlled voltage source V_c. This has no specific reason to be, other than the particularities of the Ngspice software. The consequences of adding this additional voltage have already been described (namely the creation of a new node) and dealt with in the previous section - see, for example, equation 2.

The following steps in the simulations are to be conducted:

- for t¡0 (operating point only, in order to obtain the voltages in all nodes and the currents in all branches);
- operating point for $V_s(0) = 0$, replacing the capacitor with a a voltage source Vx = V(6)-V(8), where V(6) and V(8) are the voltages in nodes 6 and 8 as obtained in the previous step (this step is necessary given that we must the compute the boundary conditions that guarantee continuity in the capacitor's discharge - such may imply that the boundary conditions differ from those computed for t¡0);
- for the natural response of the circuit (using the boundary conditions V(6) and V(8) as obtained previously);
- repeating the third step, for the natural and forced response on node 6 with V_s (as given in **Figure 8**) and f = 1kHz.
- for the frequency response in node 6 given these conditions

Name	Value [mA or V]
@c[i]	0.000000e+00
@gb[i]	-2.65897e-04
@r1[i]	2.536486e-04
@r2[i]	2.658975e-04
@r3[i]	-1.22488e-05
@r4[i]	-1.20531e-03
@r5[i]	-2.65897e-04
@r6[i]	9.516617e-04
@r7[i]	9.516617e-04
v(1)	5.054819e+00
v(2)	4.793705e+00
v(3)	4.258199e+00
v(4)	-1.93423e+00
v(5)	4.831048e+00
v(6)	5.668299e+00
v(7)	-1.93423e+00
v(8)	-2.90523e+00

Table 4: Step 1: Operating point for t¡0. A variable preceded by @ is of type *current* and expressed in miliAmpere; other variables are of type *voltage* and expressed in Volt.

4 Conclusion

In this laboratory assignment the objective of analysing a circuit containing independent, linearly dependent voltage and current sources and other linear components (resistors) has been achieved. Static analyses have been performed both theoretically, using the Octave maths tool, and by circuit simulation, using the Ngspice tool. Not only did the theoretical results obtained using different methods agree perfectly, they also matched the simulation results precisely.

The reason for this perfect match is the fact that this is a straightforward circuit containing only linear components - this implies, as pointed out in the theory classes, that the theoretical and simulation models cannot differ. For more complex components and circuits, the theoretical and simulation models could differ (given the greater complexity of the models implemented by the simulator Ngspice, when compared to those studied in the theoretical classes); however, that is not the case for this particular circuit.

This lab assignment has been useful to learn and give us the chance to put into practice our knowledge of the invaluable software tools and automation procedures required for this and other types of work, from Git and Makefile to Octave and the syntax of Ngspice. In more theoretical terms, we have become more at ease with the analysis of linear circuits, and, knowing what we now know, we would have made differente choices regarding the analysis even of this circuit (for example, we probably would have chosen a different node to assign to the Ground potential).

Name	Value [mA or V]
@gb[i]	6.332294e-18
@r1[i]	-6.04059e-18
@r2[i]	-6.33229e-18
@r3[i]	2.917029e-19
@r4[i]	-1.32956e-18
@r5[i]	-2.72282e-03
@r6[i]	8.673617e-19
@r7[i]	1.320008e-20
v(1)	0.000000e+00
v(2)	6.218372e-15
v(3)	1.897135e-14
v(4)	-1.76289e-15
v(5)	5.329071e-15
v(6)	8.573530e+00
v(7)	-1.76289e-15
v(8)	-1.77636e-15
Ix	-2.72282e-03
Vx	8.573530e+00
Req	-3.14877e+03

Table 5: Step 2: Operating point for $v_s(0) = 0$, with the capacitor replaced by a voltage source $V_x = V(6) - V(8)$ with these as obtained in the last step. A variable preceded by @ is of type *current* and expressed in miliAmpere; other variables are of type *voltage* and expressed in Volt.

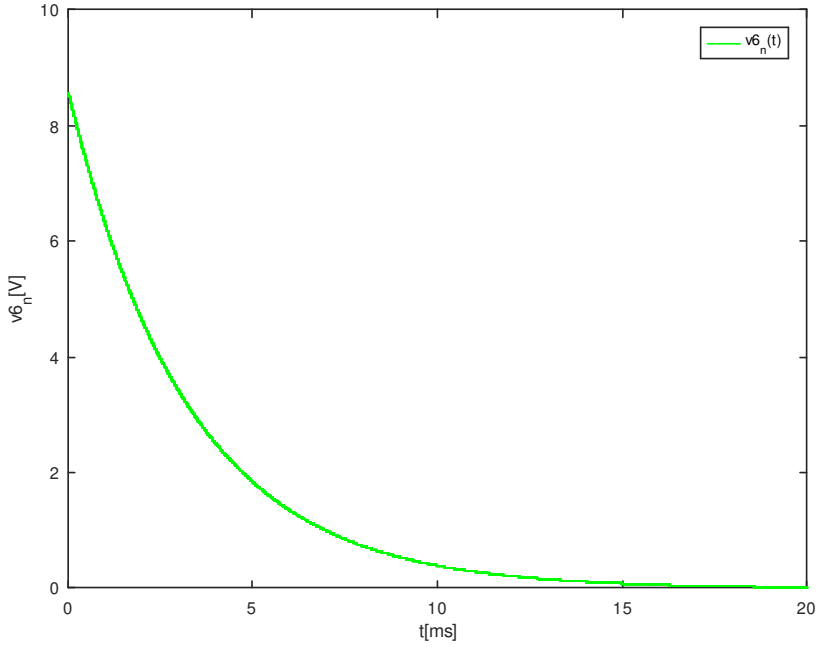

Figure 3: Graph for natural response point 3

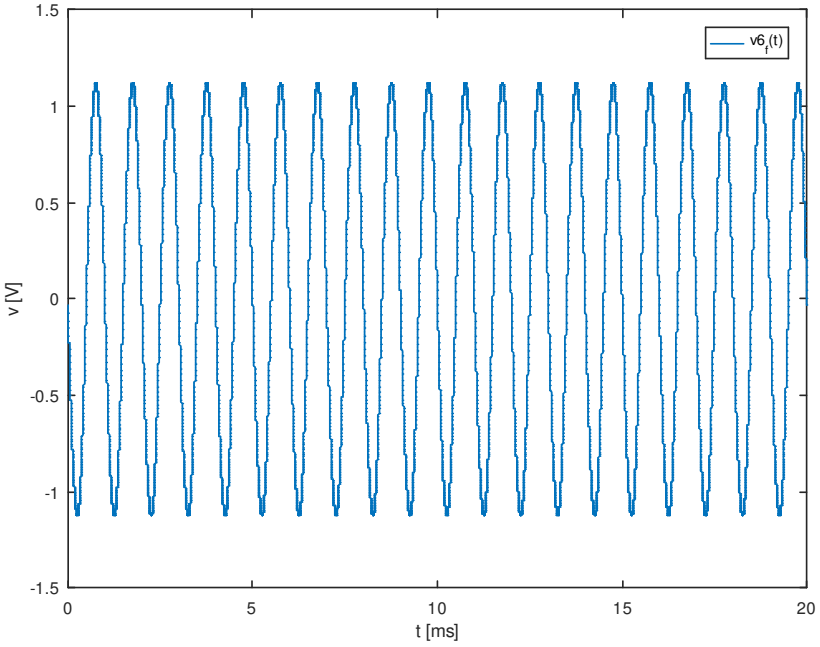

Figure 4: Graph for forced response point 4

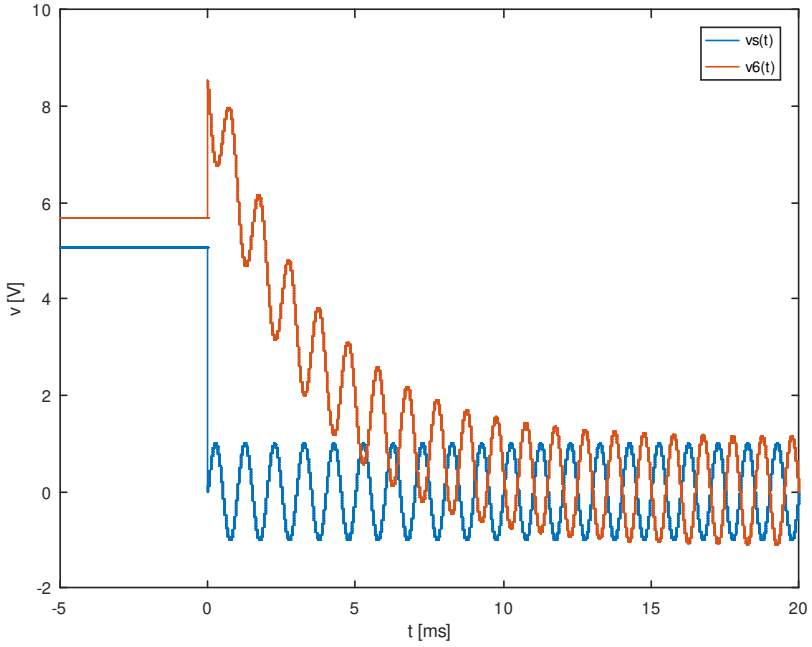

Figure 5: point 5: Graph for time interval from -5 to 20 ms

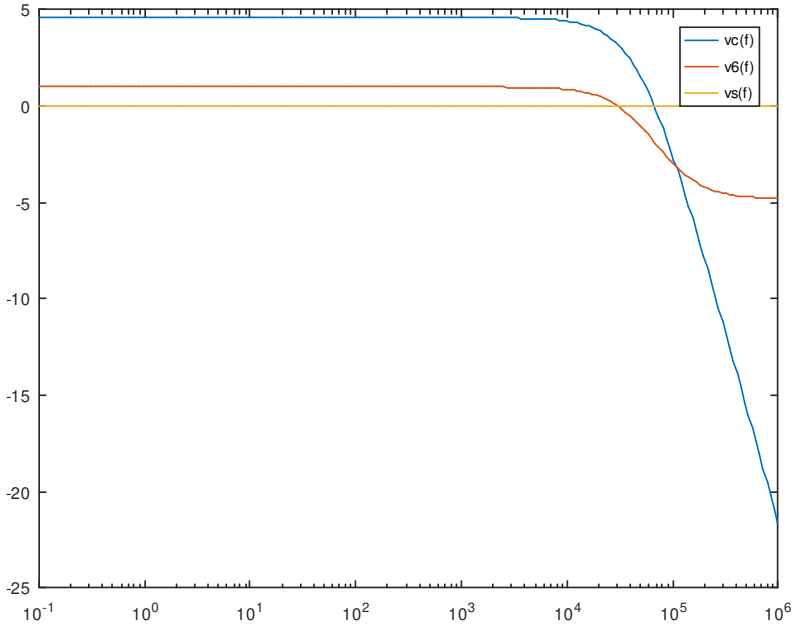

Figure 6: point 6: Graph for amplitude frequency response of Vc, V8 and Vs for frequencies ranging from 0.1Hz to 1MHz

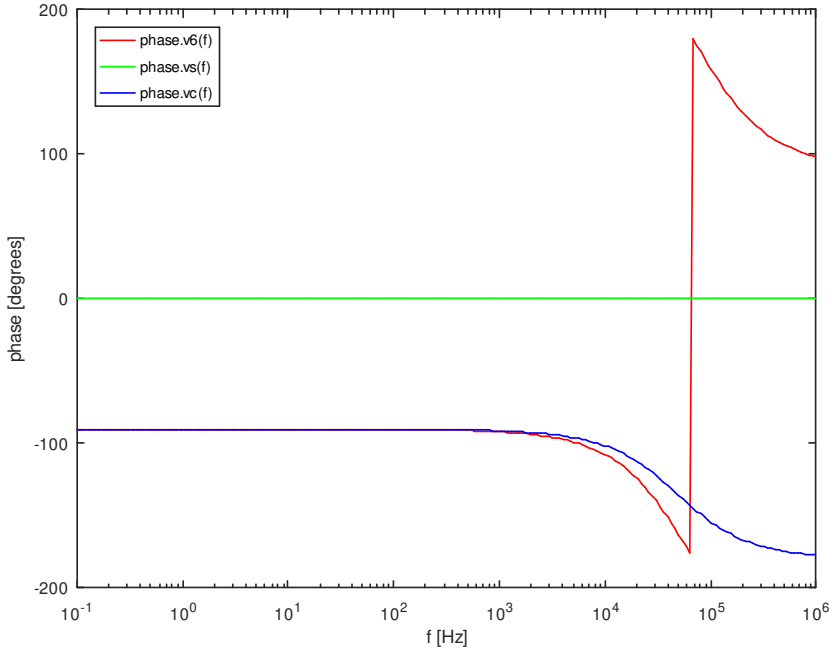

Figure 7: point 6: Graph for phase frequency response of Vc, V6 and Vs for frequencies ranging from 0.1Hz to 1MHz

$$v_s(t) = V_s u(-t) + \sin(2\pi f t) u(t)$$

$$u(t) = \begin{cases} 0, t < 0 \\ 1, t \geq 0 \end{cases}$$

Figure 8: Time step conditions