**Circuit Theory and Electronics Fundamentals**

T3 Laboratory Report

**Group 34**

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May 5, 2021

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# 1 Introduction

The objective of this laboratory assignment was to create a circuit that would transform an input AC voltage of amplitude 230V and frequency of 50 Hz to an output DC voltage of amplitude 12V and frequency 50Hz.To do this an Envelope detector, a Voltage Regulator and a Transformer were used. This last component was not actually modeled in the simulation and theorethical analysis. It was considerared that the transformer would be represented whith an alternated voltage source that would connect to the envelope detector and would reduce the amplitude of the first source in a ratio of n:1.This ration will be decided during the simulation and theorethical analysis.

To determine whether or not the circuit was good when compered to others a merit classification sistem was created. This merit sistem took into account the cost of the components used and the ripple and average amplitude of the output voltage.The merit of the circuit will determined according to the following equation:

$$MERIT = \frac{1}{(cost * (ripple_reg + abs(average_reg - 12) + 1e - 6))}$$ (1)

and the cost of the componets are the following: cost of resistors = 1 monetary unit (MU) per kOhm, cost of capacitors = 1 MU/uF and cost of diodes = 0.1 MU per diode. The voltage source that represents the transformer was not taken into account in the cost.

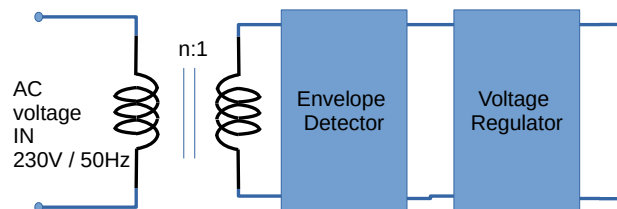The circuit that was implemented can be seen in **Figure 1**.



Figure 1: Circuit in study

In this circuit there is also a linearly dependent voltage and current source. The circuit also contains 7 resistors.

The nodes of the circuit were numbered arbitrarily (from $V_0$ to $V_7$ ), and it was considered that *node 0* was the ground node. The voltage-controlled current source $I_b$ has a linear dependence on Voltage $V_b$, of constant $K_b$. The voltage $V_b$ is the voltage drop at the ends of resistor $R_3$. The current-controlled voltage source $V_d$ has a linear dependece on current $I_d$, of constant $K_d$. The control current $I_d$ is the current that passes through the resistor $R_6$.

In Section 2, a theoretical analysis of the circuit is presented. Here the circuit is analised for $t < 0$ using the nodal analysis and the equivalent resistence $R_{eq}$ as seen from the capacitor terminals is determined. In this section both the natural and forced solutions for $V_6$ are also determined as well as the frequency responses for $V_c, V_s$ and $V_6$. In Section 3, the circuit is analysed by simulation using the program Ngspice. An operating point analysis is used to analyse the circuit when $t < 0$ and another one to determine the time constant.A transient analysis is used to determine the natural and forced responses on node 6. A frequency analysis is also performed on node 6. The conclusions of this study are outlined in Section 4, where the theoretical results obtained in Section 2 are compared to the simulation results obtained in Section 3.

# 2 Theoretical Analysis

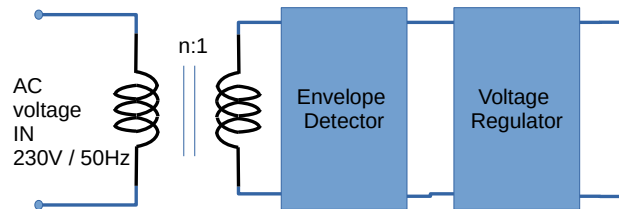In this section, the circuit shown in **Figure 2** is analysed theoretically.



Figure 2: Diagram of the circuit considered for the computations and simulations

## 2.1 Analysis for $t < 0$

The nodal method is aplied to the circuit in order to determine the voltage in all nodes and the current on all branches . The nodal method aplies KVL and for $t < 0$ no current passes through the capacitor, and therefore this component behaves like an open circuit.

# 3 Simulation Analysis

In this section we will describe the steps needed to simulate this circuit using the software Ngspice. Three types of analysis will be performed: Operating Point analysis, Transient analysis ans Frequency analysis.

# 4 Conclusion

In this laboratory assignment the objective of analysing a circuit containing multiple resistances, a capacitor and a sinusoidal voltage source $v_s$ that varies in time has been achieved.

Static, time and frequency analyses have been performed both theoretically, using the Octave maths tool, and by circuit simulation, using the Ngspice tool. The theoretical results obtained match the simulation results quite precisely - one must call attention to the fact that certain values obtained theoretically were precisely zero, whilst im some cases (the boundary conditions simulated for t=0) the corresponding simulated results were of the order of 1e-15 - we considered these results to be effectively zero, given they were multiple orders of magnitude inferior to the remaining nominal values and aproximately of the magnitude of the floating point precision for the numerical representation types used.

The reason for this overall satisfactory match is the fact that this is a relatively straightforward circuit, containing only one capacitor, besides linear components - as such, any differences will be related to the model used in ngspice for the capacitor, and in particular for the transient boundary condition analysis. For more complex components and circuits, the theoretical and simulation models could differ more (given the greater complexity of the models implemented by the simulator Ngspice, as well as the interactions between these, when compared to those studied in the theoretical classes).