TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

T3 Laboratory Report

Group 34

José Bento, Nº 95815
Thomas Childs, Nº 95847
Luís Pacheco, Nº 96425

Aerospace Engineering (MEAer), Técnico, University of Lisbon

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1 Introduction

The objective of this laboratory assignment was to create a circuit that would transform an input AC voltage of amplitude 230V and frequency of 50 Hz to an output DC voltage of amplitude 12V and frequency 50Hz.To do this an Envelope detector, a Voltage Regulator and a Transformer were used. This last component was not actually modeled in the simulation and theorethical analysis. It was considerared that the transformer would be represented whith an alternated voltage source that would connect to the envelope detector and would reduce the amplitude of the first source in a ratio of n:1.This ratio will be decided during the simulation and theorethical analysis.

To determine whether or not the circuit was good when compared to others a merit classification sistem was created. This merit sistem took into account the cost of the components used and the ripple and average amplitude of the output voltage.The merit of the circuit will determined according to the following equation:

$$MERIT = \frac{1}{cost * (ripple_reg + abs(average_reg - 12) + 1e - 6)} \tag{1}$$

and the cost of the componets are the following: cost of resistors = 1 monetary unit (MU) per kOhm, cost of capacitors = 1 MU/uF and cost of diodes = 0.1 MU per diode. The voltage source that represents the transformer was not taken into account in the cost.

The circuit that was implemented can be seen in **Figure 1**.

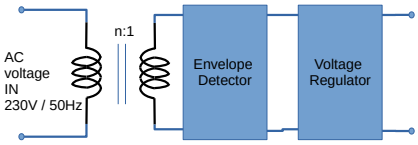

Figure 1: Circuit in study

In Section 2, a theoretical analysis of the circuit is presented. Here the circuit is analised using suitbale theorethicals models for the diodes in order to predict the output of the Envelope Detector and Voltage Regulator circuits. The output DC level and the voltage ripple are calculated and the plots for the voltages at the output of the Envelope Detector and Voltage Regulator circuits are presented, as well as the plot for the diference between the output of the regulator with 12. In Section 3, the circuit is analysed by simulation using the program Ngspice.In Ngspice de default model for the diode was used. The AC/DC converter was simulated for 10 periods and the voltage average and ripple were mesured using built in functions of the program.The same plots produced in the theoretical analysis were made in this section by simultaion.The conclusions of this study are outlined in Section 4, where the theoretical results obtained in Section 2 are compared to the simulation results obtained in Section 3.

2 Theoretical Analysis

In this section, the circuit shown in **Figure 2** is analysed theoretically.

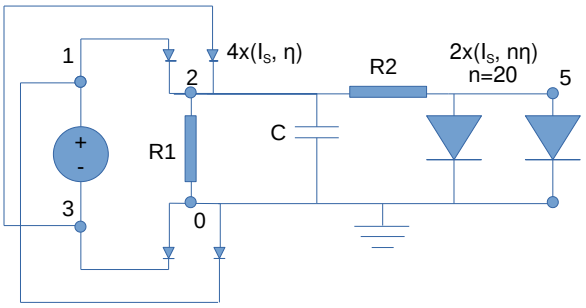

Figure 2: Diagram of the circuit considered for the computations and simulations

In the Envolope Detector the diode model used has an ideal diode and an voltage source while in the Voltage regulator de Diode model has a ideal diode, a voltage source and a resistor.

The output of the transformer will be the input of our Envelope detector.The Envelope detector circuit is made up of a rectifier and a capacitor.The rectifier is a full-wave bridge rectifier circuit and is composed of 4 diodes and a resistor. The full-wave rectifier was used as oposed of a half-wave rectifier because the full-wave rectifier allows us to reduce the ripple without incrising the time constant which would avoid a big raise in costes. The full-wave rectifier reduces the ripple because the voltage that comes out of the transformer will leave the rectifier oscillating at twice the frequency and with less amplitude, which helps us in our ripple problem.

The output of the Envelope detector

3 Simulation Analysis

In this section we will describe the steps needed to simulate this circuit using the software Ngspice. Three types of analysis will be performed: Operating Point analysis, Transient analysis ans Frequency analysis.

4 Conclusion

In this laboratory assignment the objective of analysing a circuit containing multiple resistances, a capacitor and a sinusoidal voltage source v_s that varies in time has been achieved.

Static, time and frequency analyses have been performed both theoretically, using the Octave maths tool, and by circuit simulation, using the Ngspice tool. The theoretical results obtained match the simulation results quite precisely - one must call attention to the fact that certain values obtained theoretically were precisely zero, whilst im some cases (the boundary conditions simulated for t=0) the corresponding simulated results were of the order of 1e-15 - we considered these results to be effectively zero, given they were multiple orders of magnitude inferior to the remaining nominal values and aproximately of the magnitude of the floating point precision for the numerical representation types used.

The reason for this overall satisfactory match is the fact that this is a relatively straightforward circuit, containing only one capacitor, besides linear components - as such, any differences will be related to the model used in ngspice for the capacitor, and in particular for the transient boundary condition analysis. For more complex components and circuits, the theoretical and simulation models could differ more (given the greater complexity of the models implemented by the simulator Ngspice, as well as the interactions between these, when compared to those studied in the theoretical classes).