TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

T4 Laboratory Report

Group 34

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May 23, 2021

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1 Introduction

The objective of this laboratory assignment was to create an audio amplifier circuit. The audio amplifier would recieve an audio input of 10mV (maximum) and would connect to an 8 Ohm speaker. The source would have an 100 Ohm impedance and the circuit would be supplied with 12 volts by a DC source (Vcc).

A good voltage amplifier has to have an high gain (A_V) (as we want to amplify), a high input impedance (Z_i) and a low output impedance (Z_o) (so as not to degrade the input and output voltages, respectively). In order to meet this criteria the audio amplifier circuit will have two stages: the gain stage and the output stage, as this seemed like the best way to combine the good and not so good properties of each of the amplifier circuits studied in class.

In the gain stage a common emitter amplifier with degeneration was used because it allows us to have a high Z_i and a high gain A_V. Unfortunately it has a high Z_o as well, which will degrade the output signal. This problem will have to be fixed in the next stage. In this stage an NPN transistor was used.

In the output stage a commom collector amplifier was used because it allows us to maintain the high gain A_V from the previous stage whilst having a low Z_o. This stage is able to maintain the high gain because its high input impedance connects to the lower output impedance (but still an high one) of the previous stage and the gain in this section is ≈ 1. In this stage a PNP transistor was used.

To determine the quality of the audio amplifier, when compared to others, a merit classification system was created. This merit system took into account the cost of the components used, as well as the voltage gain, the cut off frequency and the bandwidth. The merit of the circuit will determined according to the following equation:

$$MERIT = \frac{VoltageGain * Bandwidth}{Cost * LowerCutOffFrequency} \tag{1}$$

and the cost of the components are the following: cost of resistors = 1 monetary unit (MU) per kOhm, cost of capacitors = 1 MU/uF and cost of transistors = 0.1 MU per diode.

The general layout of the circuit that was implemented can be seen in **Figure 1**. In the next sections the actual architecture implemented for each stage will be analyzed in greater detail.

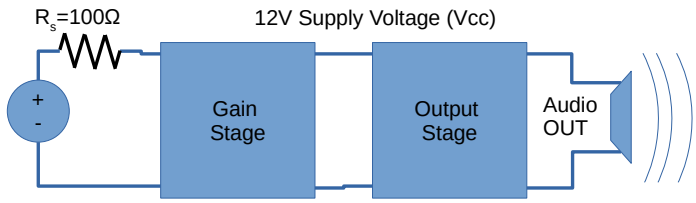

Figure 1: Circuit in study

In Section 2, a theoretical analysis of the circuit is presented. Here the circuit is analised using the suitable OP (to ensure the transistors are in the Forward Active Region) and incremental theoretical models studied in the class, in order to predict the gain and the input and output impedances for each of the stages. In Section 3, the circuit is analysed by simulation

using the program Ngspice. In Ngspice the Philips BJT'S model BC557A (PNP) and BC547A (NPN) for the transistors were used. The input and output impedances, the lower and upper 3dB cut off frequencies (the difference between them is the bandwidth), as well as the gain, were computed by simulation. The conclusions of this study are outlined in Section 4, where the theoretical results obtained in Section 2 are compared to the simulation results obtained in Section 3.

2 Theoretical Analysis

In this section, the circuit shown in **Figure 3** is analysed theoretically.

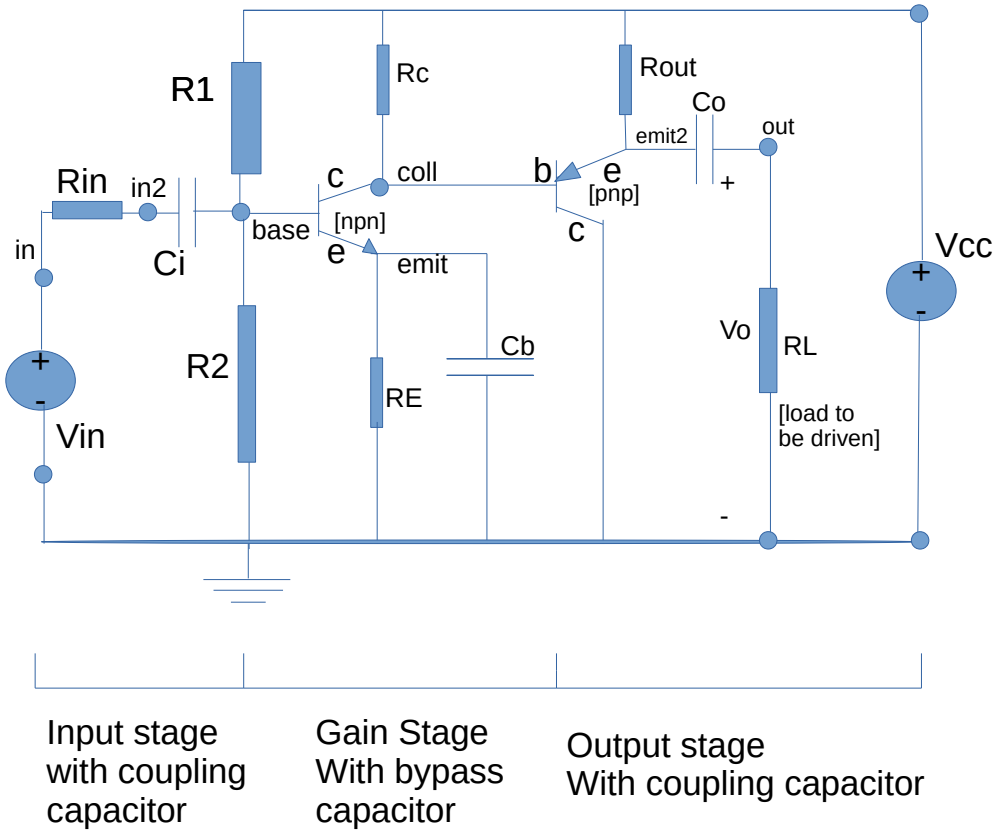

Figure 2: Diagram of the circuit considered for the computations and simulations.

As explained before, in the previous section, the audio amplifier is composed of two stages. In the first stage (the gain stage) the primary objective is to amplify the voltage input signal. To do so this section will have a high gain. This stage also has a high input impedance which avoids the degradation of the input signal. The downside of this stage is its high output impedance that makes it difficult to connect to a speaker without having the signal degrade in the exit. That is why there is an output stage. This stage will have a low output impedance which is very good because it allows us to connect to the speaker while minimizing signal degradation. When we connect the two stages the signal does not degrade very much beacuse the output stage input impedance is higher than the output impedance of the gain stage, meaning no signal degradation in the transtion between stages. In the output stage the gain is very close to one, meaning than there will be no amplification nor attenuation of the signal.

The main purpose of the bypass capacitor C_E in the gain stage is to avoid a gain loss through resistor R_E and the main purpose of resistor R_E is to stabilize the temperature effect. In the DC the temperature effect is most important while in AC the gain is. Therefore there needs to be an equilibrium. This components were placed in parallel in order to achive this

equilibrium. For lower frequencies (DC) capacitor C_E behaves like an open circuit and the current goes through resistor R_E, stabilizing the temperature effect. For higher frequencies (AC) the capacitor is a short circuit and therefore it is used to bypass the resistor R_E, avoiding lowering the gain.

In the following table is the operating point analysis, both for the theoretical analysis (right) and the Ngspice simulation (left), in order to make a side-by-side comparison. This also includes a flag (last row) that ensures that both BJTs are in the Forward Active Region - if everything is ok, the flag should read "ok". If any (or both) of the transistor are not in this region, the flag should read "bad". The condition considered was, for the NPN transistor: $V_{CE} > V_{BE} <=> V_C > V_B$ and for the PNP transistor: $V_{EC} > V_{EB} <=> V_C < V_B$

Node Voltage	Simulation	Theoretical	Units
Vbase	1.3841	1.3841	V
Vcoll	8.6547	8.6547	V
Vemit	0.6855	0.6855	V
Vemit2	9.3974	9.3974	V
Vin	0.0000	0.0000	V
Vin2	0.0000	0.0000	V
Vout	0.0000	0.0000	V
Vvcc	12.0000	12.0000	V
FAR?	ok	ok	V

The circuit used to compute the cutoff frequencies and the gain, theoretically, was the following incremental model (which includes the coupling capacitors given that these are the limiting factors in terms of the lower cutoff frequency). For the upper cutoff frequency it is a little bit more complex given that this is due to the parasitic capacitances of the transistor, which are part of the Ngspice model, but were not considered in the theory:

The gain of the audio amplifier, the upper and lower cut off frequency, the bandwidth and the input and output impedances as well as the merit are presented in the following table, both for the theoretical analysis (right) and the Ngspice simulation (left), in order to make a side-by-side comparison.

Parameter	Simulation	Theoretical	Units
Zi_{total}	766.402	640.49	Ohm
Zo_{total}	4.49605	2.9364	Ohm
Zi_{gain}	-	640.49	Ohm
Zo_{gain}	-	477.05	Ohm
Zi_{output}	-	15013.9	Ohm
Zo_{output}	-	0.93273	Ohm
Cost	8116	8116	MU
uco	3106930.000	0.000	Hz
lco	7.924	42.970	Hz
Bandwidth	3106922.076	0.000	Hz
Gainv(out)	56.041	107.220	[adimensional]
MERIT	2707.5208	0.0000	gold medals

The only difference is in the ripple value, given the Von parameter for the thoeretical model was derived from the simulation results - this accounts for the perfect fit between the simulated and predicted average output voltages. As such, the merit figures differ given the ripple value

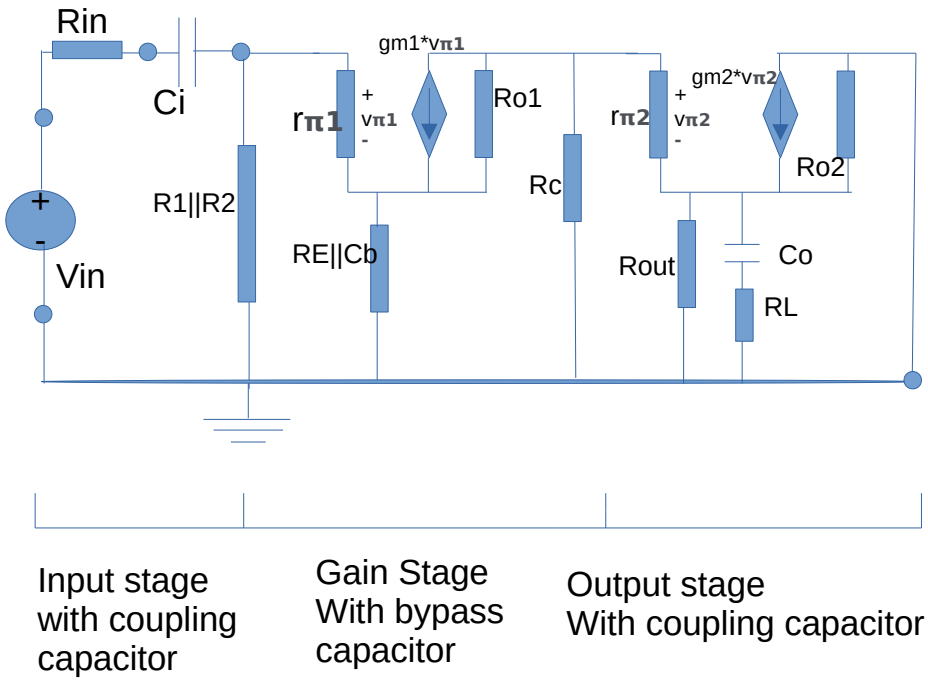

Figure 3: Diagram of the incremental model considered for the gain and frequency response computations.

is found in denominator - this means that, despite the ripple deviation being in the order of microvolts, this deviation is amplified in the merit formula. In adition, the precision of octave and ngspice floating point is different, which may account for part of the differences found. But more importantly, the difference obtained was mainly due to the fact that the models used for the diodes in the theorethical analysis differ from those used by Ngspice. The diode model used by Ngspice is way more complex than the one implemented theoretically.

The next figures present the plots required, resulting solely from the theoretical analysis.

2.1 Output of the voltage regulator circuit, compared with the output sinusoidal voltage of the transformer and the envelope detector voltage

Figure 4: Output of the voltage regulator circuit (yellow), compared with the output sinusoidal voltage of the transformer (blue) and the envelope detector voltage (red)

2.2 Output of the Envelope Detector (acting on the output of the full-wave rectifier)

Figure 5: Output of the Envelope Detector (acting on the output of the full-wave rectifier)

Figure 6: Output of the voltage regulator circuit, so as to visualize the ripple effect in greater detail

Figure 7: (v_O – 12) (output AC component + DC deviation)

3 Simulation Analysis

The circuit used to simulate the output impedance of the amplifier as a whole was the one that can be found in the following figure. The intermediate input and output impedances for the differente stages were not simulated.

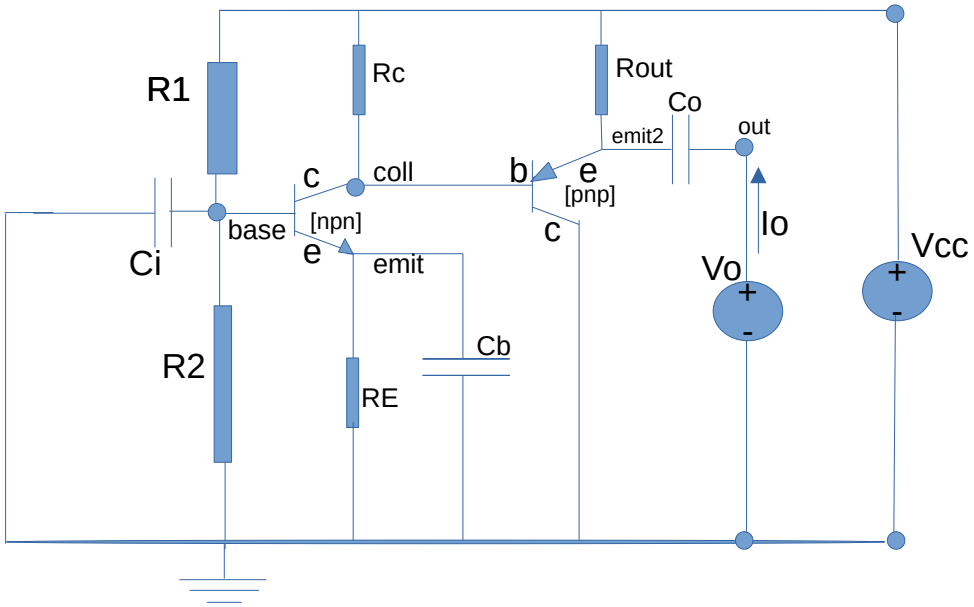

Figure 8: Diagram of the circuit considered for the simulation of the output impedance of the amplifier .

In this section we will describe the steps needed to simulate this circuit using the software Ngspice. Essentially, we only need to perform transient analysis.

The following steps in the simulations were conducted:

- describing the circuit architecture in the Ngspice script;
- simulating the AC/DC converter for 10 periods (200 ms, given the source frequency of 50 Hz); given the initial transient period, corresponding to the charge/discharge of the Capacitors up to operating point conditions, we considered a time period between 1400ms and 1600ms, to avoid having our average and ripple values contaminated by this transient initial period, beginning at t=0ms.
- measuring the output voltage ripple using Ngpice's min and max functions: ripple(v_O) = max(v_O) - min(v_O)
- plotting the voltages at the output of the Envelope Detector and Voltage Regulator circuits

- plotting (v_O – 12) (output AC component + DC deviation)
- recursively automating the parameter generation data with a different octave script, so as to only alter the parameters in one file and simultaneously run the simulation and the theoretical analysis for comparison
- automate the result evaluation process, in order to automatically generate the merit, given the parameters used (relating to cost) as input and the simulation results.
- trying to optimize the the parameters for a maximum merit. This was done by choosing values for the envelope detector (a quick analysis suggested the ideal combination would have equal numerical values for the capacitance and for the resistor in this segment of the circuit), in order to minimize ripple and cost, followed by fine-tuning the output voltage to 12V by tweaking the parameters n and Voltage Regulator resistor. Multiple iterations of this process were carried out before a ”final configuration” was chosen.

The only significant change implemented regarding the architecture for a converter studied in class (using the full wave rectifier, which seemed, off the bat, to be the best choice), was substituting the series of diodes in the regulator for a parallel of two equal series of 21 diodes, which offered a slight advantage, as this proved to be an inexpensive way to reduce by half the equivalent incremental resistance of the regulator's diodes, and thus minimize the ripple even more. The results of the simulation (left) are repeated here, compared with the corresponding theoretical simulations.

Parameter	**Simulation**	**Theoretical**	**Units**
Zi_{total}	766.402	640.49	Ohm
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3.1 Output of the voltage regulator circuit, compared with the output sinusoidal voltage of the transformer and the envelope detector voltage

Figure 9: Output of the voltage regulator circuit (yellow), compared with the output sinusoidal voltage of the transformer (red) and the envelope detector voltage (blue)

3.2 Output of the Envelope Detector (acting on the output of the full-wave rectifier)

Figure 10: Output of the Envelope Detector (acting on the output of the full-wave rectifier)

Figure 11: Output of the voltage regulator circuit, so as to visualize the ripple effect in greater detail

Figure 12: (v_O – 12) (output AC component + DC deviation) - note the vertical scale is in microVolts

4 Conclusion

In this laboratory assignment, the objective of creating a circuit that transforms an input AC voltage of 230V and frequency 50 Hz to a usable output DC voltage of 12V with minimun cost and ripple has been achieved.

The circuit created was analysed theoretically using the Octave maths tool, and by circuit simulation, using the Ngspice tool. The theoretical results obtained are very close to the simulation results. The slight difference obtained was mainly due to the fact that the models used for the diodes in the theoretical analysis differ from those used by Ngspice. The diode model used by Ngspice is way more complex than the one implemented theoretically. However due to the overall satisfactory match we can say that the theoretical model is acceptable due to its low complexity and its good results. Note that the main deviation occurred in the ripple computation - the predicted ripple was smaller than the actual ripple encountered in the simulations.

For more complex circuits, the theoretical and simulation models could differ even more, given that the greater complexity of the models implemented by the simulator Ngspice, as well as the interactions between these, which will be more noticeble when compared to the results obtained using the simpler models studied in the theoretical classes.

The final value settled on for the Merit was 16.0613 using the Ngsice's results and 23.2915 using Octave's theoretical results. This may seem like a great discrepancy, but is in fact fully explained by the difference in precision between the ngspice floating point numbers and the octave floating point, along with the the different ripple encountered between simulation and theory.