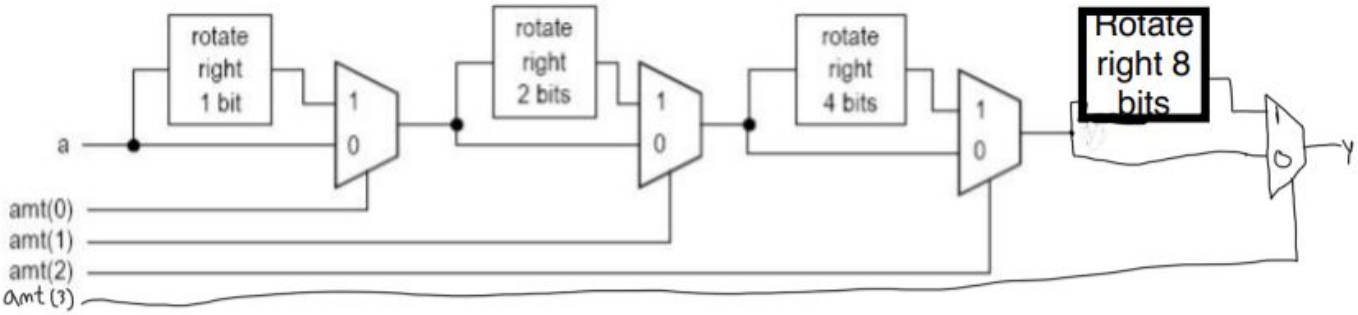
Jose Luis Martinez
Prof: Shahnam Mirzaei, Ph.D.
October 10, 2020
ECE 420

Fall 2020
California State University, Northridge
Department of Electrical and Computer Engineering
Computer Assignment 2: Design of a Combinational Barrel Shifter/Rotator

1.) Expand the idea presented by this block diagram to design a 16 bit rotator and draw the block diagram.



2.) Design a 2x1 multiplexer using simple gates.

Stage 1 Multiplexer Design (Code)

```
1  ----------------------------------------------------------------------------------
2  -- Engineer: Jose Luis Martinez
3  --
4  -- Create Date: 10/10/2020 11:46:32 PM
5  -- Design Name: 16bit Barrel Shifter
6  -- Module Name: stage1MUX - Behavioral
7  -- Project Name: 16bit Barrel Shifter
8  -- Revision 0.01 - File Created
9  --
10 ----------------------------------------------------------------------------------
11
12
13 library IEEE;
14 use IEEE.STD_LOGIC_1164.ALL;
15
16 entity stage1MUX is
17     Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
```

```
18          sel: in STD_LOGIC;
19          r: out STD_LOGIC_VECTOR(15 downto 0));
20      end stage1MUX;
21
22      architecture Behavioral of stage1MUX is
23
24      begin
25
26      r <= (a(0) & a(15 downto 1)) when sel='1' else a;
27
28      end Behavioral;
29
```

Stage 2 Multiplexer Design (Code)

```
1  ----------------------------------------------------------------------------------
2  -- Engineer: Jose Luis Martinez
3  --
4  -- Create Date: 10/10/2020 11:46:32 PM
5  -- Design Name: 16bit Barrel Shifter
6  -- Module Name: stage1MUX - Behavioral
7  -- Project Name: 16bit Barrel Shifter
8  -- Revision 0.01 - File Created
9  --
10 ----------------------------------------------------------------------------------
11
12
13 library IEEE;
14 use IEEE.STD_LOGIC_1164.ALL;
15
16 entity stage1MUX is
17     Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
18            sel: in STD_LOGIC;
19            r: out STD_LOGIC_VECTOR(15 downto 0));
20 end stage1MUX;
21
22 architecture Behavioral of stage1MUX is
23
24 begin
25
26 r <= (a(0) & a(15 downto 1)) when sel='1' else a;
27
28 end Behavioral;
29
```

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Stage 3 Multiplexer Design (Code)

```
1  ----------------------------------------------------------------------------------
2  -- Engineer: Jose Luis Martinez
3  --
4  -- Create Date: 10/10/2020 11:46:32 PM
5  -- Design Name: 16bit Barrel Shifter
6  -- Module Name: stage3MUX - Behavioral
7  -- Project Name: 16bit Barrel Shifter
8  -- Revision 0.01 - File Created
9  --
10 ----------------------------------------------------------------------------------
11
12
13 library IEEE;
14 use IEEE.STD_LOGIC_1164.ALL;
15
16 entity stage3MUX is
17     Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
18            sel: in STD_LOGIC;
19            r: out STD_LOGIC_VECTOR(15 downto 0));
20 end stage3MUX;
21
22 architecture Behavioral of stage3MUX is
23
24 begin
25
26 r <= (a(3 downto 0) & a(15 downto 4)) when sel='1' else a;
27
28 end Behavioral;
29
```

Stage 4 Multiplexer Design (Code)

```
1  ----------------------------------------------------------------------------------
2  -- Engineer: Jose Luis Martinez
3  --
4  -- Create Date: 10/10/2020 11:46:32 PM
5  -- Design Name: 16bit Barrel Shifter
6  -- Module Name: stage4MUX - Behavioral
7  -- Project Name: 16bit Barrel Shifter
8  -- Revision 0.01 - File Created
9  --
10 ----------------------------------------------------------------------------------
11
12
13 library IEEE;
```

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```
14      use IEEE.STD_LOGIC_1164.ALL;
15
16      entity stage4MUX is
17          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
18                 sel: in STD_LOGIC;
19                 r: out STD_LOGIC_VECTOR(15 downto 0));
20      end stage4MUX;
21
22      architecture Behavioral of stage4MUX is
23
24      begin
25
26      r <= (a(7 downto 0) & a(15 downto 8)) when sel='1' else a;
27
28      end Behavioral;
29
```

3.) Instantiate the multiplexer in the top level design as many times as necessary to design a combinational rotator of length 16 bits.

16 Bit Barrel Shifter Design (Code)

```
1       ----------------------------------------------------------------------------------
2       -- Engineer: Jose Luis Martinez
3       --
4       -- Create Date: 10/10/2020 11:46:32 PM
5       -- Design Name: 16bit Barrel Shifter
6       -- Module Name:  Bshifter_16 - Behavioral
7       -- Project Name: 16bit Barrel Shifter
8       -- Revision 0.01 - File Created
9       --
10      ----------------------------------------------------------------------------------
11
12
13
14      library IEEE;
15      use IEEE.STD_LOGIC_1164.ALL;
16      use IEEE.NUMERIC_STD.ALL;
17
18      entity Bshifter_16 is
19          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
20                 amt: in STD_LOGIC_VECTOR(3 downto 0);
21                 y: out STD_LOGIC_VECTOR(15 downto 0));
22      end Bshifter_16;
23
24      architecture Behavioral of Bshifter_16 is
25
26      component stage1MUX is
27          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
28                 sel: in STD_LOGIC;
29                 r: out STD_LOGIC_VECTOR(15 downto 0));
30      end component stage1MUX;
31
32      component stage2MUX is
```

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```
33          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
34                 sel: in STD_LOGIC;
35                 r: out STD_LOGIC_VECTOR(15 downto 0));
36      end component stage2MUX;
37
38      component stage3MUX is
39          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
40                 sel: in STD_LOGIC;
41                 r: out STD_LOGIC_VECTOR(15 downto 0));
42      end component stage3MUX;
43
44      component stage4MUX is
45          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
46                 sel: in STD_LOGIC;
47                 r: out STD_LOGIC_VECTOR(15 downto 0));
48      end component stage4MUX;
49
50      signal a1: std_logic_vector(15 downto 0);
51      signal sel1, sel2, sel3, sel4: std_logic;
52      signal r1, r2, r3, r4: std_logic_vector(15 downto 0);
53
54      begin
55
56      a1 <= a;
57      sel1 <= amt(0);
58      sel2 <= amt(1);
59      sel3 <= amt(2);
60      sel4 <= amt(3);
61
62      stage1: stage1MUX port map (a => a1, sel => sel1, r => r1);
63      stage2: stage2MUX port map (a => r1, sel => sel2, r => r2);
64      stage3: stage3MUX port map (a => r2, sel => sel3, r => r3);
65      stage4: stage4MUX port map (a => r3, sel => sel4, r => r4);
66
67      y <= r4;
68
69      end Behavioral;
70
```

4.) Simulate your design for the correct functionality. Write testbenches for 2x1 multiplexer as well as 16 bit combinational rotator.

Stage 1 Multiplexer Design (Test Bench Code)

```
1   ----------------------------------------------------------------------------------
2   -- Engineer: Jose Luis Martinez
3   --
4   -- Create Date: 10/10/2020 11:46:32 PM
5   -- Design Name: 16bit Barrel Shifter
6   -- Module Name: stage1MUX_tb - Behavioral
7   -- Project Name: 16bit Barrel Shifter
8   -- Revision 0.01 - File Created
9   --
10  ----------------------------------------------------------------------------------
```

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```
13      library IEEE;
14      use IEEE.STD_LOGIC_1164.ALL;
15      use IEEE.NUMERIC_STD.ALL;
16
17      entity stage1MUX_tb is
18      --  Port ( );
19      end stage1MUX_tb;
20
21      architecture Behavioral of stage1MUX_tb is
22
23      signal a_tb: STD_LOGIC_VECTOR(15 downto 0);
24      signal sel_tb: STD_LOGIC;
25      signal r_tb: STD_LOGIC_VECTOR(15 downto 0);
26
27      component stage1MUX is
28          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
29                 sel: in STD_LOGIC;
30                 r: out STD_LOGIC_VECTOR(15 downto 0));
31      end component stage1MUX;
32
33      begin
34
35      stage1MUXsim: stage1MUX port map ( a => a_tb,
36                                         sel => sel_tb,
37                                         r => r_tb);
38
39      process
40      begin
41
42          a_tb <= b"0100_0000_1100_0000";
43          sel_tb <= '0';
44          wait for 125ns;
45
46          a_tb <= b"0100_0000_1100_0000";
47          sel_tb <= '1';
48          wait for 125ns;
49
50          a_tb <= b"0100_1111_0000_0000";
51          sel_tb <= '0';
52          wait for 125ns;
53
54          a_tb <= b"0100_1111_0000_0000";
55          sel_tb <= '1';
56          wait for 125ns;
57
58          a_tb <= b"0100_0000_0000_0001";
59          sel_tb <= '0';
60          wait for 125ns;
```

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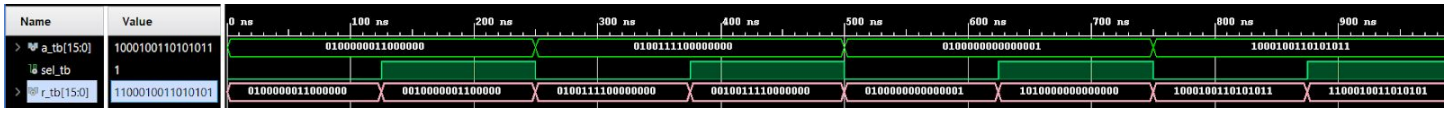
```
61
62      a_tb <= b"0100_0000_0000_0001";
63      sel_tb <= '1';
64      wait for 125ns;
65
66      a_tb <= b"1000_1001_1010_1011";
67      sel_tb <= '0';
68      wait for 125ns;
69
70      a_tb <= b"1000_1001_1010_1011";
71      sel_tb <= '1';
72      wait for 125ns;
73
74      end process;
75
76      end Behavioral;
77
```

Stage 1 Multiplexer Design (Waveforms)



Stage 2 Multiplexer Design (Test Bench Code)

```
1       ----------------------------------------------------------------------------------
2       -- Engineer: Jose Luis Martinez
3       --
4       -- Create Date: 10/10/2020 11:46:32 PM
5       -- Design Name: 16bit Barrel Shifter
6       -- Module Name: stage2MUX_tb - Behavioral
7       -- Project Name: 16bit Barrel Shifter
8       -- Revision 0.01 - File Created
9       --
10      ----------------------------------------------------------------------------------
11
12
13      library IEEE;
14      use IEEE.STD_LOGIC_1164.ALL;
15      use IEEE.NUMERIC_STD.ALL;
16
17      entity stage2MUX_tb is
18      --  Port ( );
19      end stage2MUX_tb;
20
21      architecture Behavioral of stage2MUX_tb is
22
23      signal a_tb: STD_LOGIC_VECTOR(15 downto 0);
24      signal sel_tb: STD_LOGIC;
25      signal r_tb: STD_LOGIC_VECTOR(15 downto 0);
```

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```
26
27      component stage2MUX is
28          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
29                 sel: in STD_LOGIC;
30                 r: out STD_LOGIC_VECTOR(15 downto 0));
31      end component stage2MUX;
32
33      begin
34
35      stage1MUXsim: stage2MUX port map ( a => a_tb,
36                                         sel => sel_tb,
37                                         r => r_tb);
38
39      process
40      begin
41
42          a_tb <= b"0100_0000_1100_0000";
43          sel_tb <= '0';
44          wait for 125ns;
45
46          a_tb <= b"0100_0000_1100_0000";
47          sel_tb <= '1';
48          wait for 125ns;
49
50          a_tb <= b"0100_1111_0000_0000";
51          sel_tb <= '0';
52          wait for 125ns;
53
54          a_tb <= b"0100_1111_0000_0000";
55          sel_tb <= '1';
56          wait for 125ns;
57
58          a_tb <= b"0100_0000_0000_0001";
59          sel_tb <= '0';
60          wait for 125ns;
61
62          a_tb <= b"0100_0000_0000_0001";
63          sel_tb <= '1';
64          wait for 125ns;
65
66          a_tb <= b"1000_1001_1010_1011";
67          sel_tb <= '0';
68          wait for 125ns;
69
70          a_tb <= b"1000_1001_1010_1011";
71          sel_tb <= '1';
72          wait for 125ns;
```

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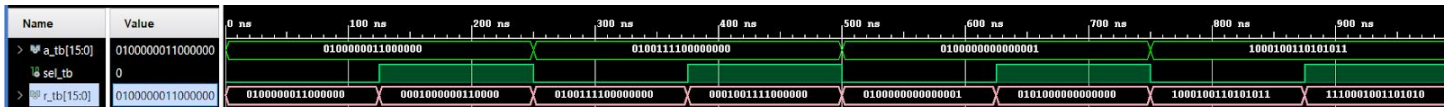
```
73
74      end process;
75
76      end Behavioral;
77
```

Stage 2 Multiplexer Design (Waveforms)



Stage 3 Multiplexer Design (Test Bench Code)

```
1       ----------------------------------------------------------------------------------
2       -- Engineer: Jose Luis Martinez
3       --
4       -- Create Date: 10/10/2020 11:46:32 PM
5       -- Design Name: 16bit Barrel Shifter
6       -- Module Name: stage3Mux_tb - Behavioral
7       -- Project Name: 16bit Barrel Shifter
8       -- Revision 0.01 - File Created
9       --
10      ----------------------------------------------------------------------------------
11
12
13      library IEEE;
14      use IEEE.STD_LOGIC_1164.ALL;
15      use IEEE.NUMERIC_STD.ALL;
16
17      entity stage3Mux_tb is
18      --  Port ( );
19      end stage3Mux_tb;
20
21      architecture Behavioral of stage3Mux_tb is
22
23      signal a_tb: STD_LOGIC_VECTOR(15 downto 0);
24      signal sel_tb: STD_LOGIC;
25      signal r_tb: STD_LOGIC_VECTOR(15 downto 0);
26
27      component stage3Mux is
28          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
29                 sel: in STD_LOGIC;
30                 r: out STD_LOGIC_VECTOR(15 downto 0));
31      end component stage3Mux;
32
33      begin
34
35      stage3MUXsim: stage3Mux port map ( a => a_tb,
36                                         sel => sel_tb,
37                                         r => r_tb);
38
39      process
40      begin
```

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```
41
42      a_tb <= b"0100_0000_1100_0000";
43      sel_tb <= '0';
44      wait for 125ns;
45
46      a_tb <= b"0100_0000_1100_0000";
47      sel_tb <= '1';
48      wait for 125ns;
49
50      a_tb <= b"0100_1111_0000_0000";
51      sel_tb <= '0';
52      wait for 125ns;
53
54      a_tb <= b"0100_1111_0000_0000";
55      sel_tb <= '1';
56      wait for 125ns;
57
58      a_tb <= b"0100_0000_0000_0001";
59      sel_tb <= '0';
60      wait for 125ns;
61
62      a_tb <= b"0100_0000_0000_0001";
63      sel_tb <= '1';
64      wait for 125ns;
65
66      a_tb <= b"1000_1001_1010_1011";
67      sel_tb <= '0';
68      wait for 125ns;
69
70      a_tb <= b"1000_1001_1010_1011";
71      sel_tb <= '1';
72      wait for 125ns;
73
74      end process;
75
76      end Behavioral;
77
```

Stage 3 Multiplexer Design (Waveforms)

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Stage 4 Multiplexer Design (Test Bench Code)

```
1  ----------------------------------------------------------------------------------
2  -- Engineer: Jose Luis Martinez
3  --
4  -- Create Date: 10/10/2020 11:46:32 PM
5  -- Design Name: 16bit Barrel Shifter
6  -- Module Name: stage4MUX_tb - Behavioral
7  -- Project Name: 16bit Barrel Shifter
8  -- Revision 0.01 - File Created
9  --
10 ----------------------------------------------------------------------------------
11
12
13 library IEEE;
14 use IEEE.STD_LOGIC_1164.ALL;
15 use IEEE.NUMERIC_STD.ALL;
16
17 entity stage4MUX_tb is
18 --  Port ( );
19 end stage4MUX_tb;
20
21 architecture Behavioral of stage4MUX_tb is
22
23 signal a_tb: STD_LOGIC_VECTOR(15 downto 0);
24 signal sel_tb: STD_LOGIC;
25 signal r_tb: STD_LOGIC_VECTOR(15 downto 0);
26
27 component stage4MUX is
28     Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
29            sel: in STD_LOGIC;
30            r: out STD_LOGIC_VECTOR(15 downto 0));
31 end component stage4MUX;
32
33 begin
34
35 stage4MUXsim: stage4MUX port map ( a => a_tb,
36                                    sel => sel_tb,
37                                    r => r_tb);
38
39 process
40 begin
41
42     a_tb <= b"0100_0000_1100_0000";
43     sel_tb <= '0';
44     wait for 125ns;
45
46     a_tb <= b"0100_0000_1100_0000";
47     sel_tb <= '1';
48     wait for 125ns;
49
50     a_tb <= b"0100_1111_0000_0000";
51     sel_tb <= '0';
52     wait for 125ns;
53
54     a_tb <= b"0100_1111_0000_0000";
```

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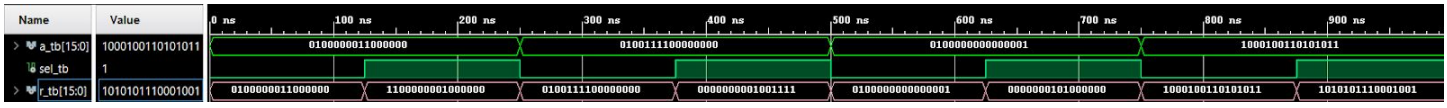
```
55      sel_tb <= '1';
56      wait for 125ns;
57
58      a_tb <= b"0100_0000_0000_0001";
59      sel_tb <= '0';
60      wait for 125ns;
61
62      a_tb <= b"0100_0000_0000_0001";
63      sel_tb <= '1';
64      wait for 125ns;
65
66      a_tb <= b"1000_1001_1010_1011";
67      sel_tb <= '0';
68      wait for 125ns;
69
70      a_tb <= b"1000_1001_1010_1011";
71      sel_tb <= '1';
72      wait for 125ns;
73
74      end process;
75
76      end Behavioral;
77
```

Stage 4 Multiplexer Design (Waveforms)



16 Bit Barrel Shifter Design (Test Bench Code)

```
1       ----------------------------------------------------------------------------------
2       -- Engineer: Jose Luis Martinez
3       --
4       -- Create Date: 10/10/2020 11:46:32 PM
5       -- Design Name: 16bit Barrel Shifter
6       -- Module Name:  Bshifter_16_tb - Behavioral
7       -- Project Name: 16bit Barrel Shifter
8       -- Revision 0.01 - File Created
9       --
10      ----------------------------------------------------------------------------------
11
12
13
14      library IEEE;
15      use IEEE.STD_LOGIC_1164.ALL;
16      use IEEE.NUMERIC_STD.ALL;
17
18
19      entity Bshifter_16_tb is
20      --  Port ( );
21      end Bshifter_16_tb;
22
```

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```
23      architecture Behavioral of Bshifter_16_tb is
24
25      signal a_tb: std_logic_vector(15 downto 0);
26      signal amt_tb: std_logic_vector(3 downto 0);
27      signal y_tb: std_logic_vector(15 downto 0);
28
29      component Bshifter_16 is
30          Port ( a: in STD_LOGIC_VECTOR(15 downto 0);
31                 amt: in STD_LOGIC_VECTOR(3 downto 0);
32                 y: out STD_LOGIC_VECTOR(15 downto 0));
33      end component Bshifter_16;
34
35      begin
36
37      Bshifter_16_SIM: Bshifter_16 port map (a => a_tb,
38                                             amt => amt_tb,
39                                             y => y_tb);
40
41      process
42          begin
43
44          a_tb <= b"0100_1111_0000_1111";
45          amt_tb <= "0001";
46          wait for 250ns;
47
48          amt_tb <= "1001";
49          wait for 250ns;
50
51          amt_tb <= "0110";
52          wait for 250ns;
53
54          amt_tb <= "1111";
55          wait for 250ns;
56
57      end process;
58
59      end Behavioral;
60
```

16 Bit Barrel Shifter Design (Waveforms)