

Spring 2021  
California State University, Northridge  
Department of Electrical & Computer Engineering

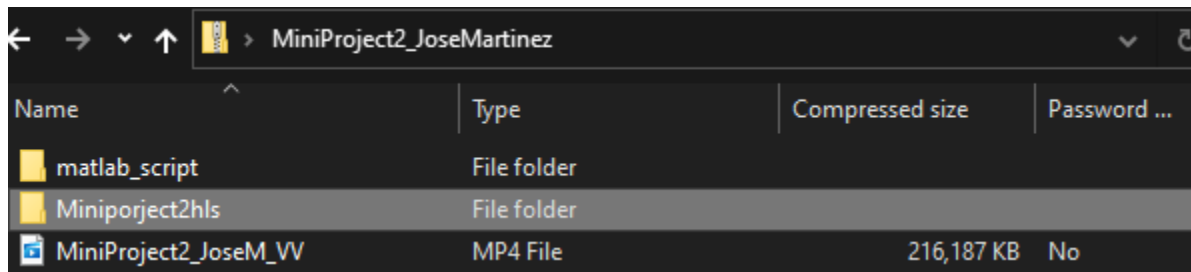


Mini Project 2  
HLS - Image Processing  
May 15, 2021  
ECE 520L

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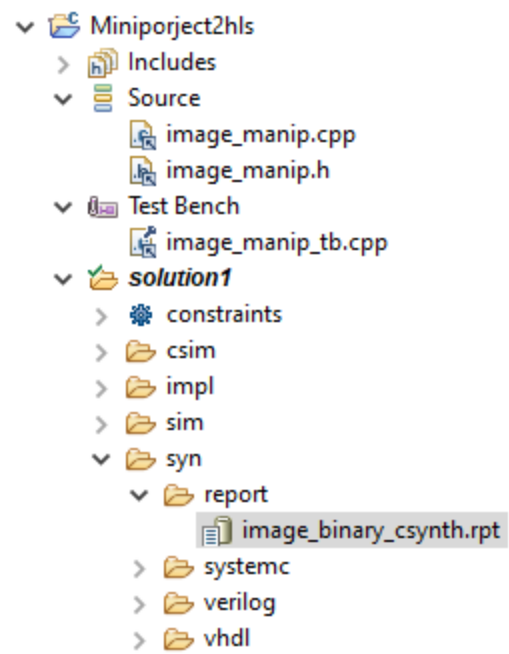
## Mini Project 2: Run Instructions

1. The zipped file will contain the following:
  - a. Vivado HLS Project
    - i. This contains the source project for Mini Project 1.
    - ii. All 6 processes are run at the same time by a top level function calling them each once.
    - iii. There are 5 solutions to accommodate for each of the constraints.
  - b. Matlab Script
    - i. This is used to generate the image into a 100x100 grayscale matrix ready for hls.
    - ii. The same script will also take in matrices generated by HLS and show them as images.
  - c. Verification Video
  - d. Source code **image\_manip.cpp**, **image\_manip.h**, and **image\_manip\_tb.cpp**.
  - e. All images used in this instruction report.
2. This project was created using Vivado HLS 2019.1 and ZYBO was used as the target hardware device. Make sure to extract the folder before starting.
  - a. To open this project, go to Vivado HLS and open the folder Miniporject2hls inside the zipped folder as the project.

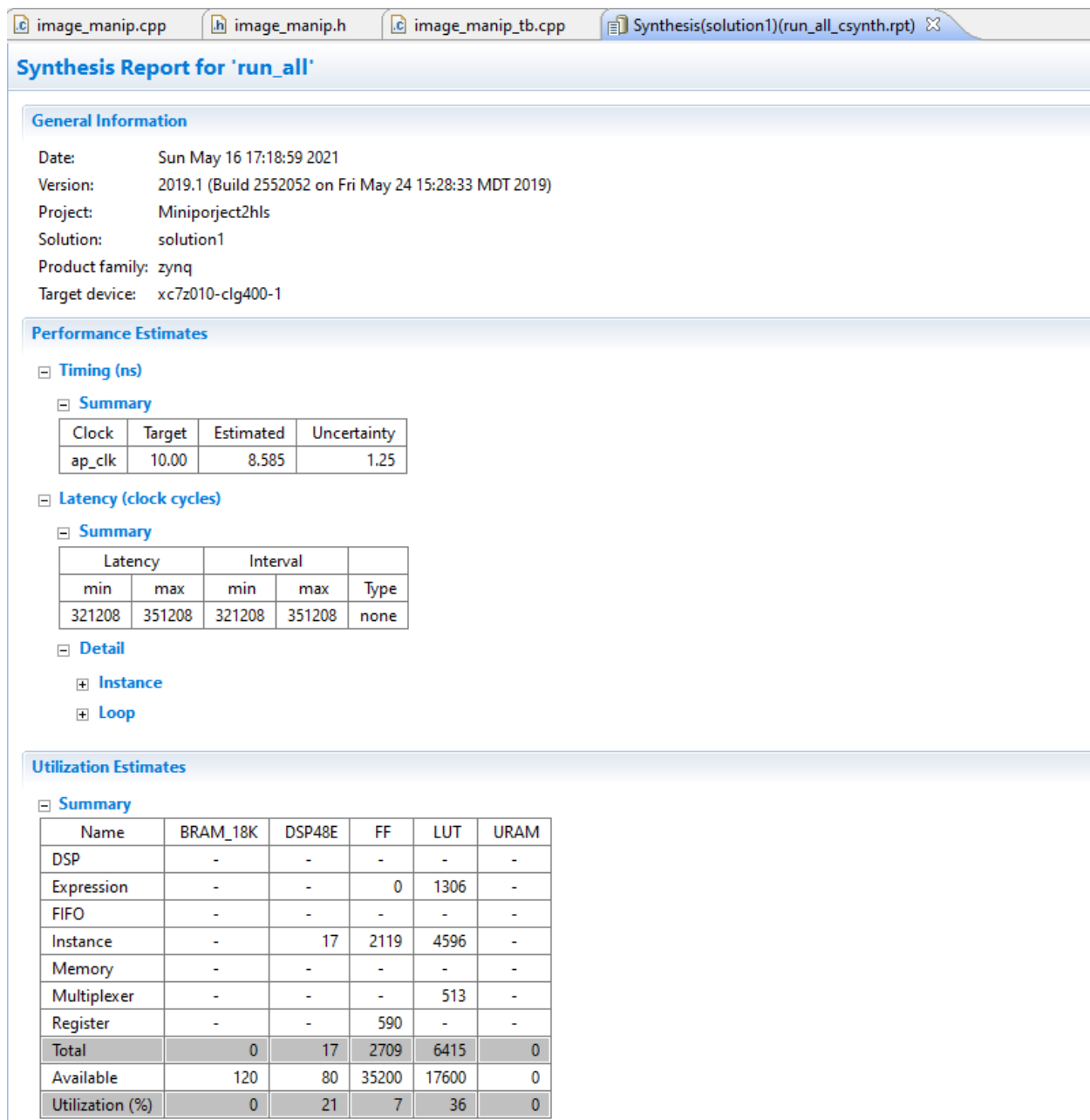


**Fig. 1** Vivado HLS Project Directory

3. Once in Vivado HLS, you can verify anything that was required of this mini project.
  - a. To verify Synthesis go to solution1 → syn → report and open the report found there as shown below.
  - b. To verify the constraints just set the active solution to the one you want to check.

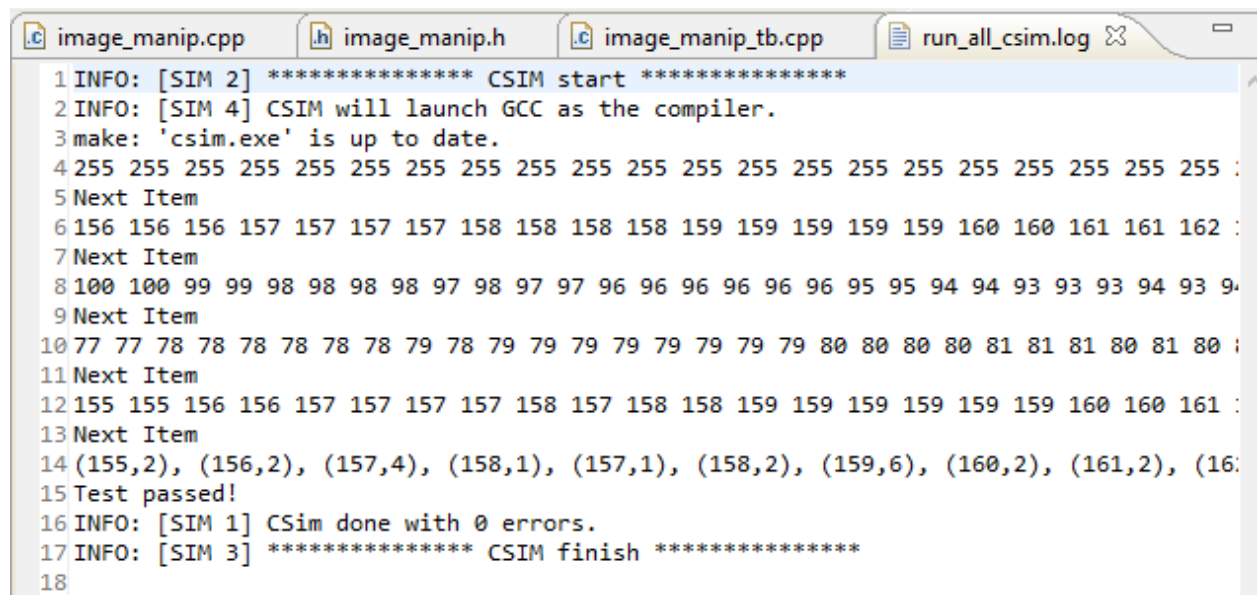


**Fig. 2** Synthesis Report Location



**Fig. 3** Synthesis Report

4. I used Matlab to generate the original input image for me.
  - a. Go to the matlab\_scripts folder and open r\_g.m.
  - b. Run it and you should see a matrix printed out in the console.
  - c. Copy and paste that into the Testbench file in hls.
  - d. Run the C Simulation and you should see a similar output to **Fig. 4**.
  - e. Each row of numbers corresponds to an image except the last one.
  - f. Paste each in the following order: bin\_image, ave\_image, invert\_image, scale\_image, and decomp\_image.
  - g. When you run the mat lab simulation again you should see something like **Fig. 6**.



```
1 INFO: [SIM 2] ***** CSIM start *****
2 INFO: [SIM 4] CSIM will launch GCC as the compiler.
3 make: 'csim.exe' is up to date.
4 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 255 :
5 Next Item
6 156 156 156 157 157 157 157 158 158 158 158 159 159 159 159 160 160 161 161 162 :
7 Next Item
8 100 100 99 99 98 98 98 98 97 98 97 97 96 96 96 96 96 95 95 94 94 93 93 93 94 93 94 :
9 Next Item
10 77 77 78 78 78 78 78 78 79 78 79 79 79 79 79 79 79 80 80 80 80 81 81 81 80 81 80 :
11 Next Item
12 155 155 156 156 157 157 157 157 158 157 158 158 159 159 159 159 160 160 161 161 :
13 Next Item
14 (155,2), (156,2), (157,4), (158,1), (157,1), (158,2), (159,6), (160,2), (161,2), (162,2) :
15 Test passed!
16 INFO: [SIM 1] CSim done with 0 errors.
17 INFO: [SIM 3] ***** CSIM finish *****
18
```

**Fig. 4** C Testbench Results

## Vivado HLS Report Comparison

### All Compared Solutions

[solution1](#): xc7z010-clg400-1

[solution2](#): xc7z010-clg400-1

[solution3](#): xc7z010-clg400-1

[solution5](#): xc7z010-clg400-1

### Performance Estimates

#### Timing (ns)

| Clock  |           | solution1 | solution2 | solution3 | solution5 |
|--------|-----------|-----------|-----------|-----------|-----------|
| ap_clk | Target    | 10.00     | 10.00     | 10.00     | 10.00     |
|        | Estimated | 8.585     | 9.634     | 10.983    | 8.585     |

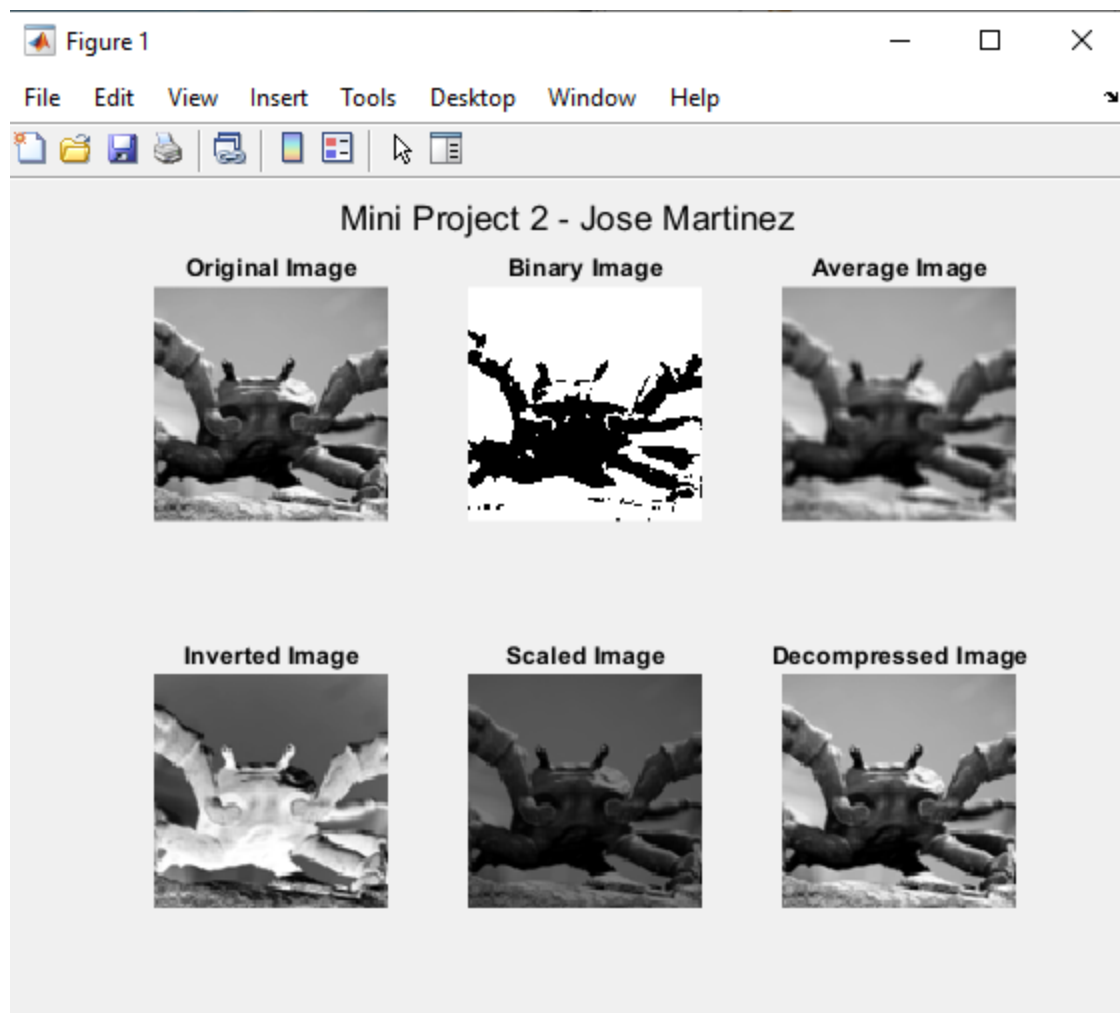
#### Latency (clock cycles)

|          |     | solution1 | solution2 | solution3 | solution5 |
|----------|-----|-----------|-----------|-----------|-----------|
| Latency  | min | 321208    | 120038    | 111817    | 321208    |
|          | max | 351208    | 120038    | 131717    | 351208    |
| Interval | min | 321208    | 120038    | 111817    | 321208    |
|          | max | 351208    | 120038    | 131717    | 351208    |

### Utilization Estimates

|          | solution1 | solution2 | solution3 | solution5 |
|----------|-----------|-----------|-----------|-----------|
| BRAM_18K | 0         | 0         | 0         | 0         |
| DSP48E   | 17        | 19        | 416       | 17        |
| FF       | 2709      | 3016      | 58932     | 2709      |
| LUT      | 6415      | 6695      | 145814    | 6415      |
| URAM     | 0         | 0         | 0         | 0         |

**Fig. 5** Solution Comparison (Solution 4 Could not Synthesize due to load and write errors)



**Fig. 6** Matlab Output