

Spring 2021
California State University, Northridge
Department of Electrical & Computer Engineering



Experiment 2
Using Delays on Primitives
February 8, 2021
ECE 526L

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Introduction

In experiment 2 we were presented with the circuit in **Fig. 1** and given the verilog code to code (**Fig. 3**) to simulate it. We were also given another circuit **Fig. 2** but this time we were to modify the previous code to match the new circuit.

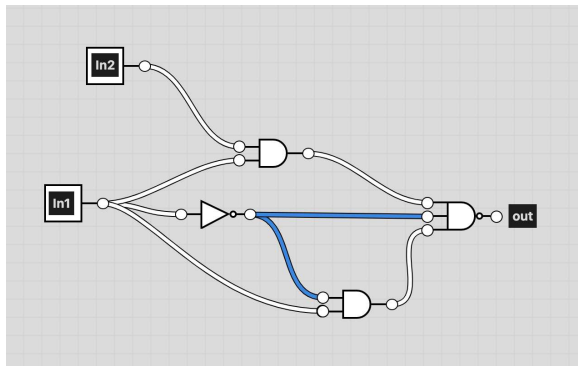


Fig. 1 - Circuit 1

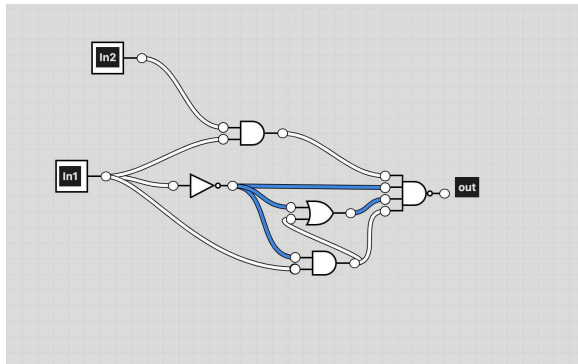


Fig. 2 - Circuit 2

The purpose of this lab is to practice basic verilog syntax and see the difference in the output when applying delays to our primitives.

```
Lab2.v
~/526LSP21/Lab2
Save
Lab2.v x Lab2_tb.v x Lab2_complete.v x

timescale 1 ns / 100 ps

`define PRIMARY_OUT 0 // ns (primary outputs)
`define FAN_OUT_1 0 // ns (one output fanout)
`define FAN_OUT_2 0 // ns (two output fanout)
`define TIME_DELAY_1 0 // ns (one input gates)
`define TIME_DELAY_2 0 // ns (two input gates)
`define TIME_DELAY_3 0 // ns (three input gates)

module Lab2_1 (in1,in2,out1);
    input in1,in2;
    output out1;

    wire NT,A1,A2;

    not #(`TIME_DELAY_1 + `FAN_OUT_2) NOT1(NT,in1);
    and #(`TIME_DELAY_2 + `FAN_OUT_1) AND1(A1,in2,in1);
    and #(`TIME_DELAY_2 + `FAN_OUT_1) AND2(A2,in1,NT);
    nand #(`TIME_DELAY_3 + `PRIMARY_OUT) NAND1(out1,NT,A1,A2);

endmodule

timescale 1 ns / 1 ns

`define MONITOR_STR_1 "%d: in1 = %b, in2 = %b, | out = %b"

module Lab2_1_tb();
    reg in1, in2;
    wire out;
    Lab2_1 UUT(in1,in2,out);

    initial begin
        $monitor(`MONITOR_STR_1, $time, in1, in2, out);
    end

    initial begin
        $vcdpluson; // For graphical viewer (waveforms)
        #15 in1 = 1'b0;
        in2 = 1'b0;
        #15 in1 = 1'b0;
        in2 = 1'b1;
        #15 $finish;
    end
endmodule
```

Fig. 3 - Circuit 1 code

Methodology

Being one of the earlier labs in the semester there were only a few things we had to design. One being changing the code that was given to us for the second circuit. The other being changing the delay values for the second circuit.

Circuit 2 is very similar to the first one except that it has one OR gate and the NAND gate now has 4 inputs instead of 3. So in my code I added a 2 input OR gate and connected its inputs from the signals NT and A2. The NAND gate has one more input added coming from the OR gate I created called OR1.

For the delay of the primitives we had to add delay based on the number of inputs and a delay based on the number of inputs the output was connected to. For NOT1 it has 1 input and its output is connected to 3 inputs hence `#('TIME_DELAY_1 + 'FAN_OUT_3)`. For AND1 it has 2 inputs and its output is connected to 1 input hence `#('TIME_DELAY_2 + 'FAN_OUT_1)`. For AND2 it has 2 inputs and its output is connected to 2 inputs hence `#('TIME_DELAY_2 + 'FAN_OUT_2)`. For OR1 it has 2 inputs and its output is connected to 1 input hence `#('TIME_DELAY_2 + 'FAN_OUT_1)`. For NAND1 it has 4 inputs and its output is connected to primary output hence `#('TIME_DELAY_4 + 'PRIMARY_OUT)`.

Both circuits were simulated with and without delays using Synopsis in a linux virtual machine.

Results

Lab2.v (circuit 1) (No Delay)

```
1  /*****
2  ***
3  *** ECE 526 L Experiment #2          Jose Luis Martinez, Spring, 2021 ***
4  ***
5  *** Lab2
6  ***
7  *****/
8  *** Filename: Lab2.v      Created by Jose Luis Martinez, Febuary 4, 2021 ***
9  ***
10 *****/
11
12 `timescale 1 ns / 100 ps
13
14 `define PRIMARY_OUT    0
15 `define FAN_OUT_1      0
16 `define FAN_OUT_2      0
17 `define TIME_DELAY_1   0
18 `define TIME_DELAY_2   0
19 `define TIME_DELAY_3   0
```

```

20
21 module Lab2_1 (in1, in2, out1);
22     input in1, in2;
23     output out1;
24
25     wire NT, A1, A2;
26
27     not #(`TIME_DELAY_1 + `FAN_OUT_2) NOT1(NT, in1);
28     and #(`TIME_DELAY_2 + `FAN_OUT_1) AND1(A1, in2, in1);
29     and #(`TIME_DELAY_2 + `FAN_OUT_1) AND2(A2, in1, NT);
30     nand #(`TIME_DELAY_3 + `PRIMARY_OUT) NAND1(out1, NT, A1, A2);
31
32 endmodule

```

Lab2.v (circuit 1) (Delay)

```

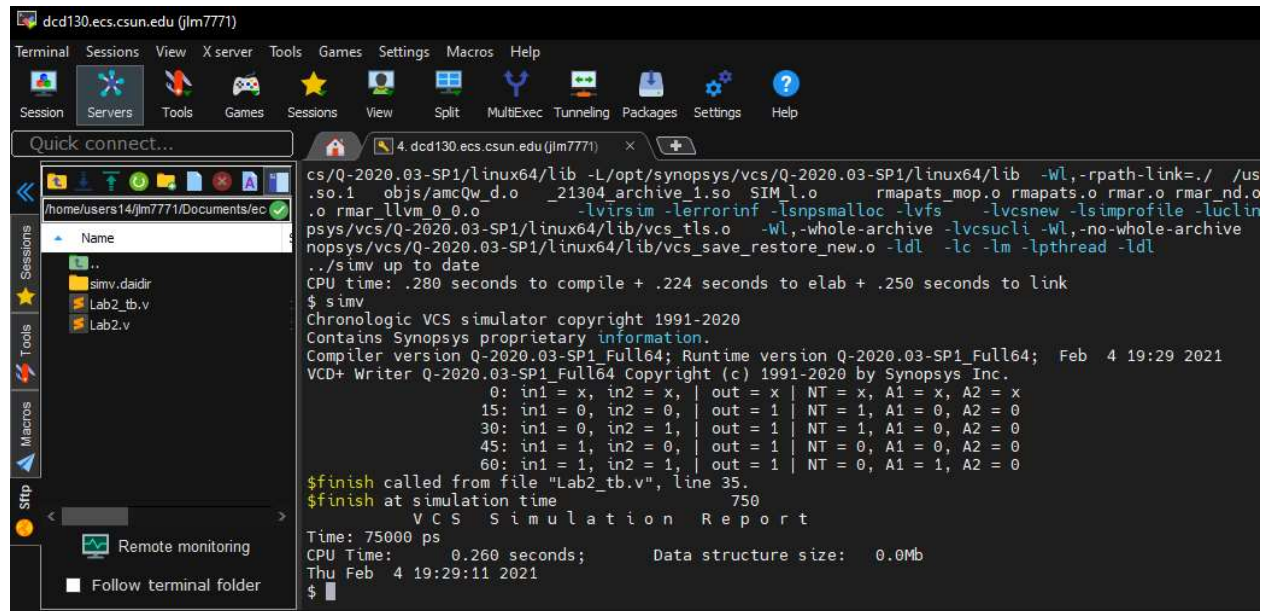
1  /*****
2  ***
3  *** ECE 526 L Experiment #2          Jose Luis Martinez, Spring, 2021 ***
4  ***
5  *** Lab2
6  ***
7  ****
8  *** Filename: Lab2.v      Created by Jose Luis Martinez, Febuary 4, 2021 ***
9  ***
10 *****/
11
12 `timescale 1 ns / 100 ps
13
14 `define PRIMARY_OUT    5
15 `define FAN_OUT_1      0.5
16 `define FAN_OUT_2      1
17 `define TIME_DELAY_1   1
18 `define TIME_DELAY_2   2
19 `define TIME_DELAY_3   3
20
21 module Lab2_1 (in1, in2, out1);
22     input in1, in2;
23     output out1;
24
25     wire NT, A1, A2;
26
27     not #(`TIME_DELAY_1 + `FAN_OUT_2) NOT1(NT, in1);
28     and #(`TIME_DELAY_2 + `FAN_OUT_1) AND1(A1, in2, in1);
29     and #(`TIME_DELAY_2 + `FAN_OUT_1) AND2(A2, in1, NT);
30     nand #(`TIME_DELAY_3 + `PRIMARY_OUT) NAND1(out1, NT, A1, A2);
31
32 endmodule

```

Lab2_tb.v

```
1  /*****
2  ***
3  *** ECE 526 L Experiment #1          Jose Luis Martinez, Spring, 2021 ***
4  ***
5  *** Lab2
6  ***
7  *****/
8  *** Filename: Lab2_tb.v  Created by Jose Luis Martinez, January 29, 2021 ***
9  ***
10 *****/
11
12 `timescale 1 ns / 1 ns
13
14 `define MONITOR_STR_1 "%d: in1 = %b, in2 = %b, | out = %b | NT = %b, A1 = %b, A2 = %b"
15
16 module Lab2_1_tb();
17     reg in1, in2;
18     wire out;
19     Lab2_1 UUT(.in1(in1), .in2(in2), .out1(out));
20
21     initial begin
22         $monitor(`MONITOR_STR_1, $time, in1, in2, out, UUT.NT, UUT.A1, UUT.A2);
23     end
24
25     initial begin
26         $vcdpluson;
27         #15 in1 = 1'b0;
28             in2 = 1'b0;
29         #15 in1 = 1'b0;
30             in2 = 1'b1;
31         #15 in1 = 1'b1;
32             in2 = 1'b0;
33         #15 in1 = 1'b1;
34             in2 = 1'b1;
35         #15 $finish;
36     end
37 endmodule
```

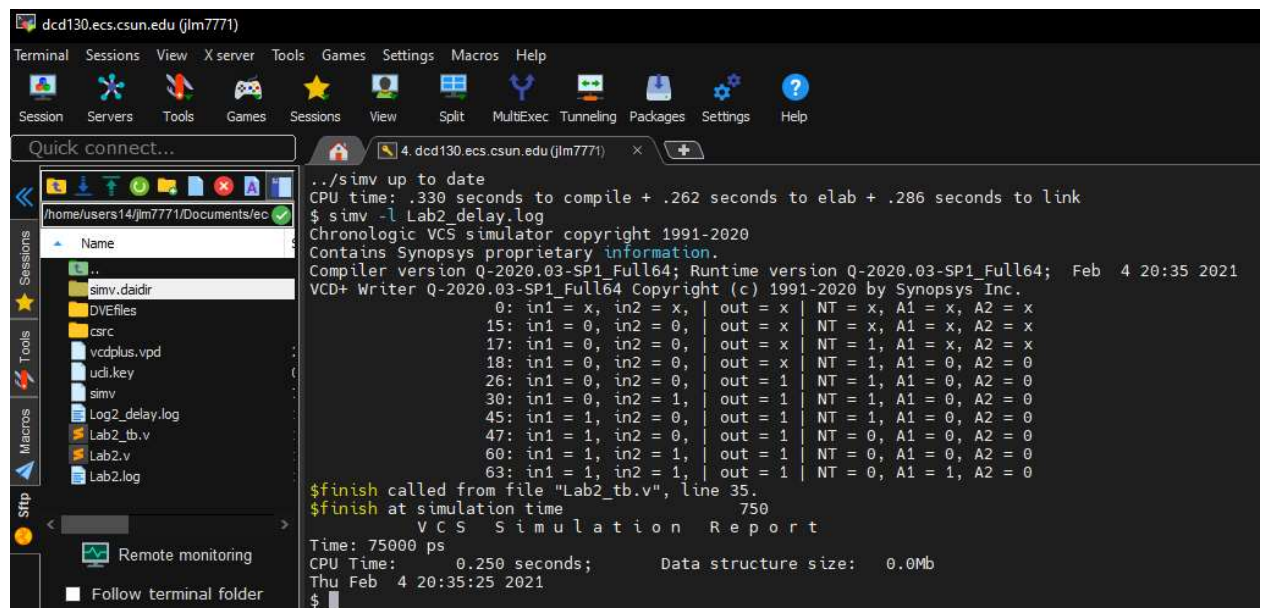

Lab2.log (No Delay)



The screenshot shows a terminal window titled "dcd130.ecs.csun.edu (jlm7771)". The terminal displays the output of a simulation command. The output includes the path to the simulation files, the command to run the simulation, the CPU time taken, and the simulation results. The simulation results show a successful completion of the simulation with no delay.

```
dcd130.ecs.csun.edu (jlm7771)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
/home/users14/jlm7771/Documents/ec
Name
..
simv.daidir
Lab2_tb.v
Lab2.v
Remote monitoring
Follow terminal folder
cs/Q-2020.03-SP1/linux64/lib -L/opt/synopsys/vcs/Q-2020.03-SP1/linux64/lib -Wl,-rpath-link=./ /us
.so.1 objs/amcQw_d.o _21304 archive_1.so SIM_l.o rmapats_mop.o rmapats.o rmar.o rmar_nd.o
.o rmar_llvm_0.o.o -lvrsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -lucln
psys/vcs/Q-2020.03-SP1/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive
nopsys/vcs/Q-2020.03-SP1/linux64/lib/vcs_save_restore_new.o -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .280 seconds to compile + .224 seconds to elab + .250 seconds to link
$ simv
Chronologic VCS simulator copyright 1991-2020
Contains Synopsys proprietary information.
Compiler version Q-2020.03-SP1_Full64; Runtime version Q-2020.03-SP1_Full64; Feb 4 19:29 2021
VCD+ Writer Q-2020.03-SP1_Full64 Copyright (c) 1991-2020 by Synopsys Inc.
0: in1 = x, in2 = x, | out = x | NT = x, A1 = x, A2 = x
15: in1 = 0, in2 = 0, | out = 1 | NT = 1, A1 = 0, A2 = 0
30: in1 = 0, in2 = 1, | out = 1 | NT = 1, A1 = 0, A2 = 0
45: in1 = 1, in2 = 0, | out = 1 | NT = 0, A1 = 0, A2 = 0
60: in1 = 1, in2 = 1, | out = 1 | NT = 0, A1 = 1, A2 = 0
$finish called from file "Lab2_tb.v", line 35.
$finish at simulation time 750
VCS Simulation Report
Time: 75000 ps
CPU Time: 0.260 seconds; Data structure size: 0.0Mb
Thu Feb 4 19:29:11 2021
$
```

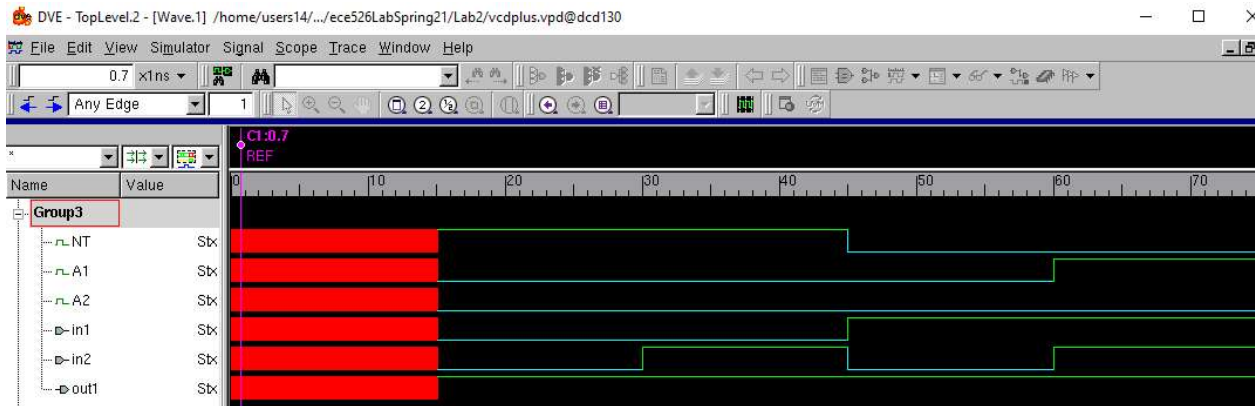
Lab2.log (Delay)



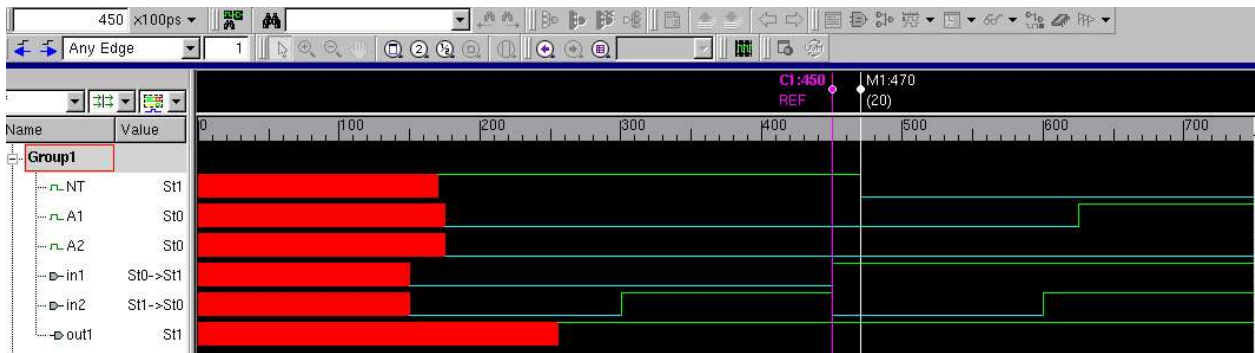
The screenshot shows a terminal window titled "dcd130.ecs.csun.edu (jlm7771)". The terminal displays the output of a simulation command. The output includes the path to the simulation files, the command to run the simulation, the CPU time taken, and the simulation results. The simulation results show a successful completion of the simulation with a delay.

```
dcd130.ecs.csun.edu (jlm7771)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
/home/users14/jlm7771/Documents/ec
Name
..
simv.daidir
DVEFiles
csrc
vcdplus.vpd
udi.key
simv
Log2_delay.log
Lab2_tb.v
Lab2.v
Lab2.log
Remote monitoring
Follow terminal folder
../simv up to date
CPU time: .330 seconds to compile + .262 seconds to elab + .286 seconds to link
$ simv -l Lab2_delay.log
Chronologic VCS simulator copyright 1991-2020
Contains Synopsys proprietary information.
Compiler version Q-2020.03-SP1_Full64; Runtime version Q-2020.03-SP1_Full64; Feb 4 20:35 2021
VCD+ Writer Q-2020.03-SP1_Full64 Copyright (c) 1991-2020 by Synopsys Inc.
0: in1 = x, in2 = x, | out = x | NT = x, A1 = x, A2 = x
15: in1 = 0, in2 = 0, | out = x | NT = x, A1 = x, A2 = x
17: in1 = 0, in2 = 0, | out = x | NT = 1, A1 = x, A2 = x
18: in1 = 0, in2 = 0, | out = x | NT = 1, A1 = 0, A2 = 0
26: in1 = 0, in2 = 0, | out = 1 | NT = 1, A1 = 0, A2 = 0
30: in1 = 0, in2 = 1, | out = 1 | NT = 1, A1 = 0, A2 = 0
45: in1 = 1, in2 = 0, | out = 1 | NT = 1, A1 = 0, A2 = 0
47: in1 = 1, in2 = 0, | out = 1 | NT = 0, A1 = 0, A2 = 0
60: in1 = 1, in2 = 1, | out = 1 | NT = 0, A1 = 0, A2 = 0
63: in1 = 1, in2 = 1, | out = 1 | NT = 0, A1 = 1, A2 = 0
$finish called from file "Lab2_tb.v", line 35.
$finish at simulation time 750
VCS Simulation Report
Time: 75000 ps
CPU Time: 0.250 seconds; Data structure size: 0.0Mb
Thu Feb 4 20:35:25 2021
$
```

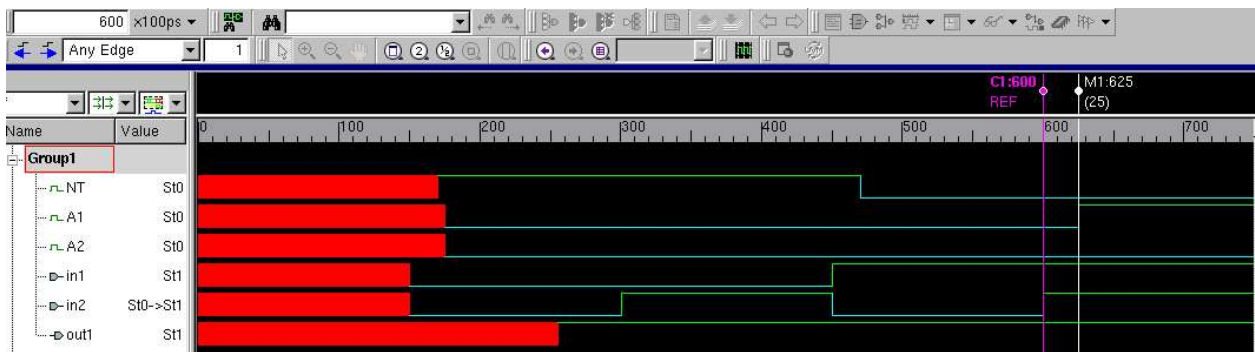
Lab2 Waveforms (Circuit 1) (No Delay)



Lab2 Waveforms (Circuit 1) (Delay) (NOT1 Measurement)



Lab2 Waveforms (Circuit 1) (Delay) (AND1 Measurement)



Lab2_2.v (Circuit 2) (No Delay)

```
1  /*****
2  ***
3  *** ECE 526 L Experiment #2          Jose Luis Martinez, Spring, 2021 ***
4  ***
5  *** Familiarization with Linux and Synopsys VCS          ***
6  ***
7  *****/
8  *** Filename: Lab2.v          Created by Jose Luis Martinez, Febuary 4, 2021 ***
9  ***
10 *****/
11
12 `timescale 1 ns / 100 ps
13
14 `define PRIMARY_OUT    0    // 5
15 `define FAN_OUT_1      0    // 0.5
16 `define FAN_OUT_2      0    // 1
17 `define FAN_OUT_3      0    // 1.5
18 `define TIME_DELAY_1   0    // 1
19 `define TIME_DELAY_2   0    // 2
20 `define TIME_DELAY_3   0    // 3
21 `define TIME_DELAY_4   0    // 4
22
23 module Lab2_2 (in1, in2, out1);
24     input in1, in2;
25     output out1;
26
27     wire NT, A1, A2, OR1;
28
29     not #(`TIME_DELAY_1 + `FAN_OUT_3) NOT1(NT, in1);
30     and #(`TIME_DELAY_2 + `FAN_OUT_1) AND1(A1, in2, in1);
31     and #(`TIME_DELAY_2 + `FAN_OUT_2) AND2(A2, in1, NT);
32     or #(`TIME_DELAY_2 + `FAN_OUT_1) OR1(OR1, NT, A2);
33     nand #(`TIME_DELAY_4 + `PRIMARY_OUT) NAND1(out1, NT, A1, A2, OR1);
34
35 endmodule
```

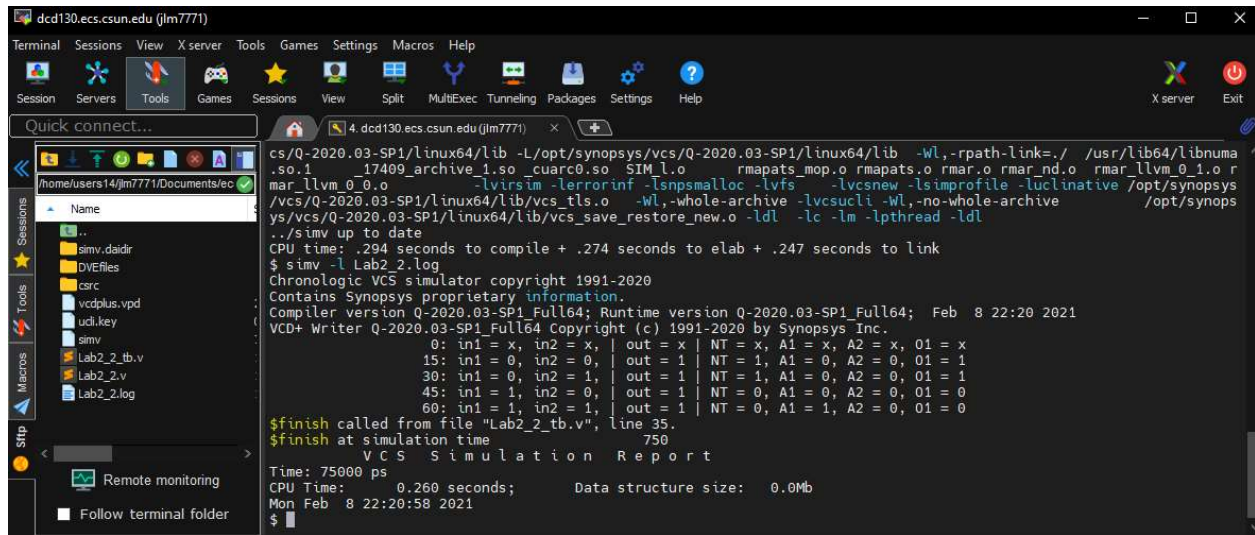

Lab2_2.v (Circuit 2) (Delay)

```
1  /*****
2  ***
3  *** ECE 526 L Experiment #2          Jose Luis Martinez, Spring, 2021 ***
4  ***
5  *** Familiarization with Linux and Synopsys VCS          ***
6  ***
7  *****/
8  *** Filename: Lab2.v      Created by Jose Luis Martinez, Febuary 4, 2021 ***
9  ***
10 *****/
11
12 `timescale 1 ns / 100 ps
13
14 `define PRIMARY_OUT    5    // 5
15 `define FAN_OUT_1      0.5  // 0.5
16 `define FAN_OUT_2      1    // 1
17 `define FAN_OUT_3      1.5  // 1.5
18 `define TIME_DELAY_1   1    // 1
19 `define TIME_DELAY_2   2    // 2
20 `define TIME_DELAY_3   3    // 3
21 `define TIME_DELAY_4   4    // 4
22
23 module Lab2_2 (in1, in2, out1);
24     input in1, in2;
25     output out1;
26
27     wire NT, A1, A2, OR1;
28
29     not #(`TIME_DELAY_1 + `FAN_OUT_3) NOT1(NT, in1);
30     and #(`TIME_DELAY_2 + `FAN_OUT_1) AND1(A1, in2, in1);
31     and #(`TIME_DELAY_2 + `FAN_OUT_2) AND2(A2, in1, NT);
32     or #(`TIME_DELAY_2 + `FAN_OUT_1) OR1(OR1, NT, A2);
33     nand #(`TIME_DELAY_4 + `PRIMARY_OUT) NAND1(out1, NT, A1, A2, OR1);
34
35 endmodule
```

Lab2_2_tb.v

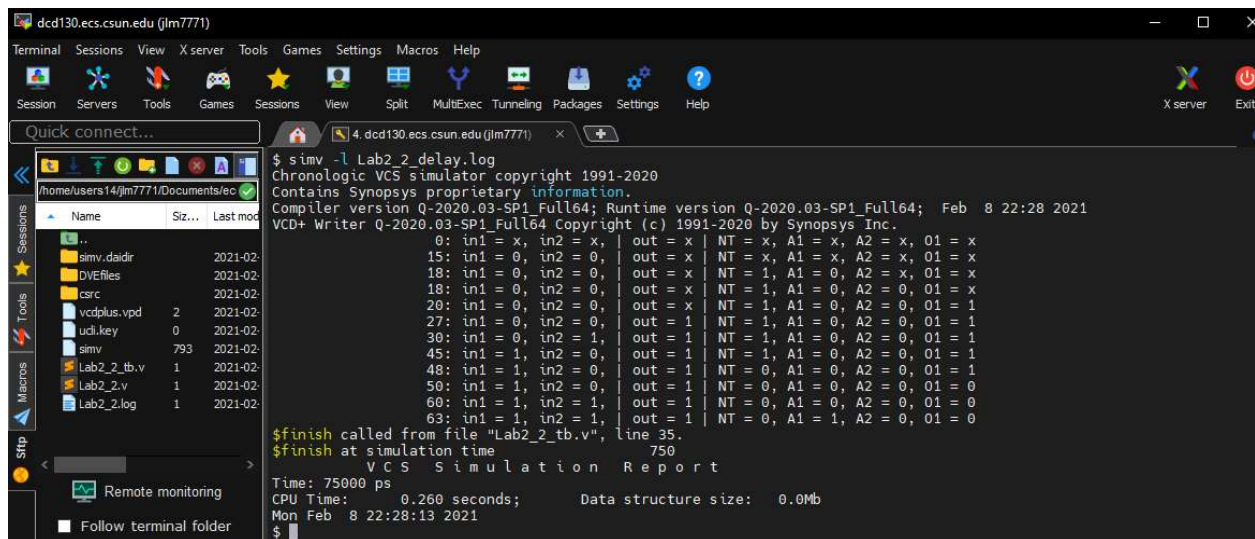
```
1  /*******
2  ***
3  *** ECE 526 L Experiment #2          Jose Luis Martinez, Spring, 2021 ***
4  ***
5  *** Lab2_2                          ***
6  ***
7  *****/
8  *** Filename:Lab2_2tb.v Created by Jose Luis Martinez, January 29, 2021 ***
9  ***
10 *****/
11
12 `timescale 1 ns / 1 ns
13
14 `define MONITOR_STR_1 "%d: in1 = %b, in2 = %b, | out = %b | NT = %b, A1 = %b, A2 = %b, O1 = %b"
15
16 module Lab2_1_tb();
17     reg in1, in2;
18     wire out;
19     Lab2_2 UUT(.in1(in1), .in2(in2), .out1(out));
20
21     initial begin
22         $monitor(`MONITOR_STR_1, $time, in1, in2, out, UUT.NT, UUT.A1, UUT.A2, UUT.O1);
23     end
24
25     initial begin
26         $vcdpluson;
27         #15 in1 = 1'b0;
28             in2 = 1'b0;
29         #15 in1 = 1'b0;
30             in2 = 1'b1;
31         #15 in1 = 1'b1;
32             in2 = 1'b0;
33         #15 in1 = 1'b1;
34             in2 = 1'b1;
35         #15 $finish;
36     end
37 endmodule
```

Lab2_2.log (No Delay)



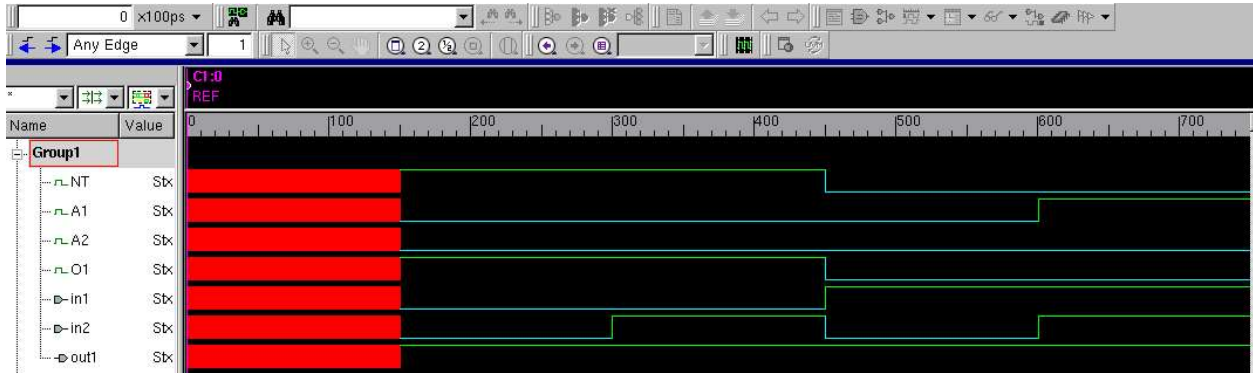
```
cs/Q-2020.03-SP1/linux64/lib -L/opt/synopsys/vcs/Q-2020.03-SP1/linux64/lib -Wl,-rpath-link=/usr/lib64/libnuma
.so.1 _17409_archive_1.so _cuarc0.so SIM l.o rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o r
mar_llvm_0_0.o -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinate /opt/synopsys
/vcs/Q-2020.03-SP1/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive /opt/synops
ys/vcs/Q-2020.03-SP1/linux64/lib/vcs_save_restore_new.o -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .294 seconds to compile + .274 seconds to elab + .247 seconds to link
$ simv -l Lab2_2.log
Chronologic VCS simulator copyright 1991-2020
Contains Synopsys proprietary information.
Compiler version Q-2020.03-SP1_Full64; Runtime version Q-2020.03-SP1_Full64; Feb 8 22:20 2021
VCD+ Writer Q-2020.03-SP1_Full64 Copyright (c) 1991-2020 by Synopsys Inc.
0: in1 = x, in2 = x, out = x | NT = x, A1 = x, A2 = x, O1 = x
15: in1 = 0, in2 = 0, out = 1 | NT = 1, A1 = 0, A2 = 0, O1 = 1
30: in1 = 0, in2 = 1, out = 1 | NT = 1, A1 = 0, A2 = 0, O1 = 1
45: in1 = 1, in2 = 0, out = 1 | NT = 0, A1 = 0, A2 = 0, O1 = 0
60: in1 = 1, in2 = 1, out = 1 | NT = 0, A1 = 1, A2 = 0, O1 = 0
$finish called from file "Lab2_2.tb.v", line 35.
$finish at simulation time 750
VCS Simulation Report
Time: 75000 ps
CPU Time: 0.260 seconds; Data structure size: 0.0Mb
Mon Feb 8 22:20:58 2021
$
```

Lab2_2_delay.log (Delay)

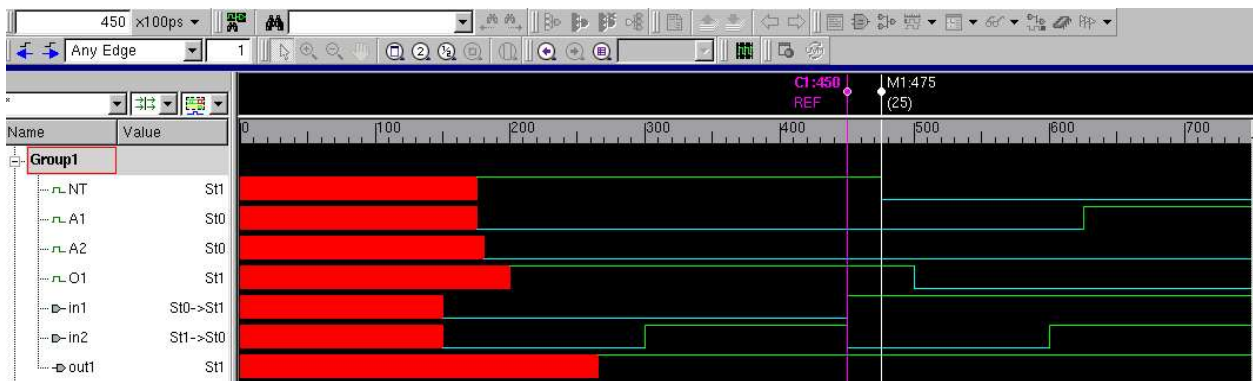


```
$ simv -l Lab2_2_delay.log
Chronologic VCS simulator copyright 1991-2020
Contains Synopsys proprietary information.
Compiler version Q-2020.03-SP1_Full64; Runtime version Q-2020.03-SP1_Full64; Feb 8 22:28 2021
VCD+ Writer Q-2020.03-SP1_Full64 Copyright (c) 1991-2020 by Synopsys Inc.
0: in1 = x, in2 = x, out = x | NT = x, A1 = x, A2 = x, O1 = x
15: in1 = 0, in2 = 0, out = x | NT = x, A1 = x, A2 = x, O1 = x
18: in1 = 0, in2 = 0, out = x | NT = 1, A1 = 0, A2 = x, O1 = x
18: in1 = 0, in2 = 0, out = x | NT = 1, A1 = 0, A2 = 0, O1 = x
20: in1 = 0, in2 = 0, out = x | NT = 1, A1 = 0, A2 = 0, O1 = 1
27: in1 = 0, in2 = 0, out = 1 | NT = 1, A1 = 0, A2 = 0, O1 = 1
30: in1 = 0, in2 = 1, out = 1 | NT = 1, A1 = 0, A2 = 0, O1 = 1
45: in1 = 1, in2 = 0, out = 1 | NT = 1, A1 = 0, A2 = 0, O1 = 1
48: in1 = 1, in2 = 0, out = 1 | NT = 0, A1 = 0, A2 = 0, O1 = 1
50: in1 = 1, in2 = 0, out = 1 | NT = 0, A1 = 0, A2 = 0, O1 = 0
60: in1 = 1, in2 = 1, out = 1 | NT = 0, A1 = 0, A2 = 0, O1 = 0
63: in1 = 1, in2 = 1, out = 1 | NT = 0, A1 = 1, A2 = 0, O1 = 0
$finish called from file "Lab2_2.tb.v", line 35.
$finish at simulation time 750
VCS Simulation Report
Time: 75000 ps
CPU Time: 0.260 seconds; Data structure size: 0.0Mb
Mon Feb 8 22:28:13 2021
$
```

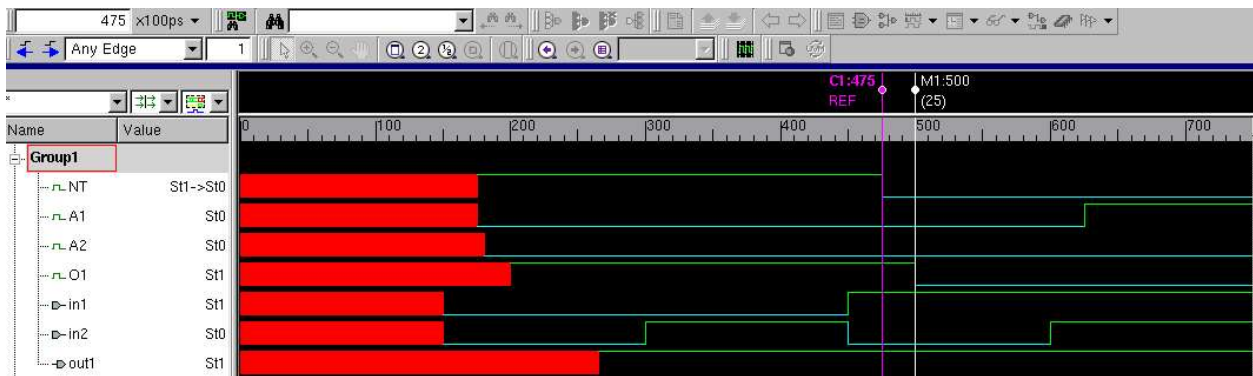
Lab2 Waveforms (Circuit 2) (No Delay)



Lab2 Waveforms (Circuit 2) (Delay) (NOT1 Measured)



Lab2 Waveforms (Circuit 2) (Delay) (OR1 Measured)



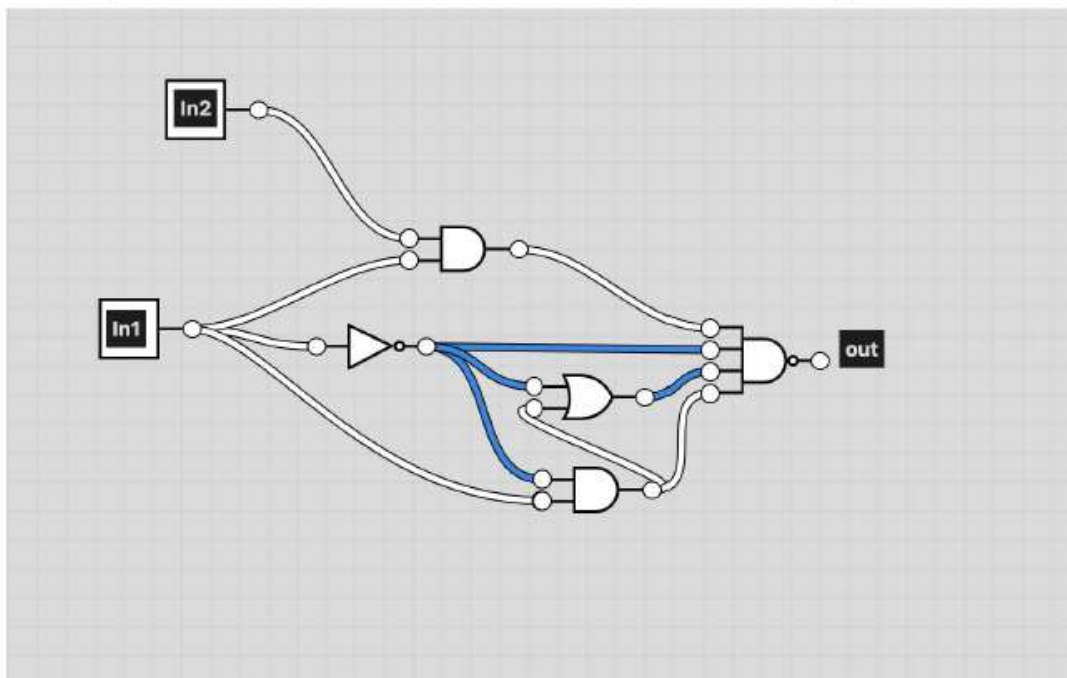
Analysis

From the waveforms and simv output we can verify that the design works as intended. For circuit 1 we can see the signal NT goes to logic level LOW when the signal in1 goes HIGH. The signal A1 goes HIGH when both in1 and in2 are logic level HIGH. However signal A2 never goes HIGH because its inputs are complement of each other and will never be both logic HIGH. Nonetheless our circuit works as intended by the picture given to us. When we add delays to circuit 1, some of our signals take a little bit of time to change. For example, when in1 goes HIGH our NT signal has a 2ns delay before changing to logic level LOW. When in1 and in2 are both logic level HIGH, AND1 has a 2.5ns delay before rising to logic level HIGH. These delays match the delays we assigned them in the verilog file.

For circuit 2 we can see the signal NT goes to logic level LOW when the signal in1 goes HIGH. The signal O1 goes LOW when both A2 and NT are logic level LOW. However, similar to circuit 1, signal A2 never goes HIGH because its inputs are complement of each other and will never be both logic HIGH. Circuit 2 works as intended when no delays are present. When we add delays to circuit 2, some of our signals have a delay before the change to the right value. For example, when in1 goes HIGH our NT signal has a 2.5ns delay before changing to logic level LOW. When both NT and A2 are logic level low, the O1 signal is delayed by 2.5ns before going to logic level LOW. These delays match the delays we assigned them in the verilog file.

Conclusion

In conclusion, I learned how to add delays to the primitive types in verilog and how to measure delays using cursors in the graphing tool. This lab went smoothly and all the results match with what was expected. The logic matched with the pictures given to us and the delays also match with the given timings. So far the labs have been interesting and I hope to learn more in the upcoming experiments.



Lab report question: What's the critical path (longest delay) of this new design?

The delays for the gates we should consider going through are NOT1 = 2.5ns, AND1 = 1.5ns, AND2 = 3ns, and OR1 = 2.5ns. The path that has the highest delay would be the one that travels from in1 -> NOT1 -> AND2 -> OR1 -> NAND1. Taking NAND1's delay of 9ns it will take 17ns for the signal to completely travel the path.

Academic Dishonesty

Submitting any report that is not entirely your own work is a form of academic dishonesty and will not be tolerated. Each and every lab report must include the following statement, signed and dated by the student. Lab reports without the statement will be summarily rejected.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Jose Luis Martinez

Name (signed) Jose Martinez Date 2/8/2021