

A decorative graphic consisting of thin, grey, stylized circuit lines with small circles at the ends, extending horizontally from the left and right sides of the central black box.

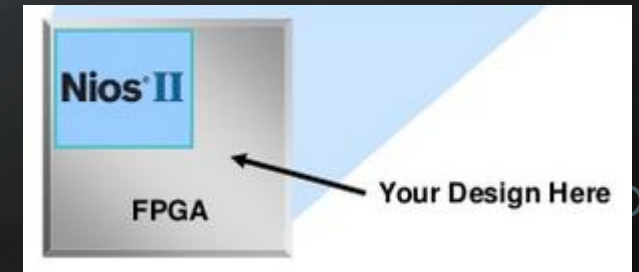
SISTEMAS EMBARCADOS

PROF. JOSENALDE OLIVEIRA

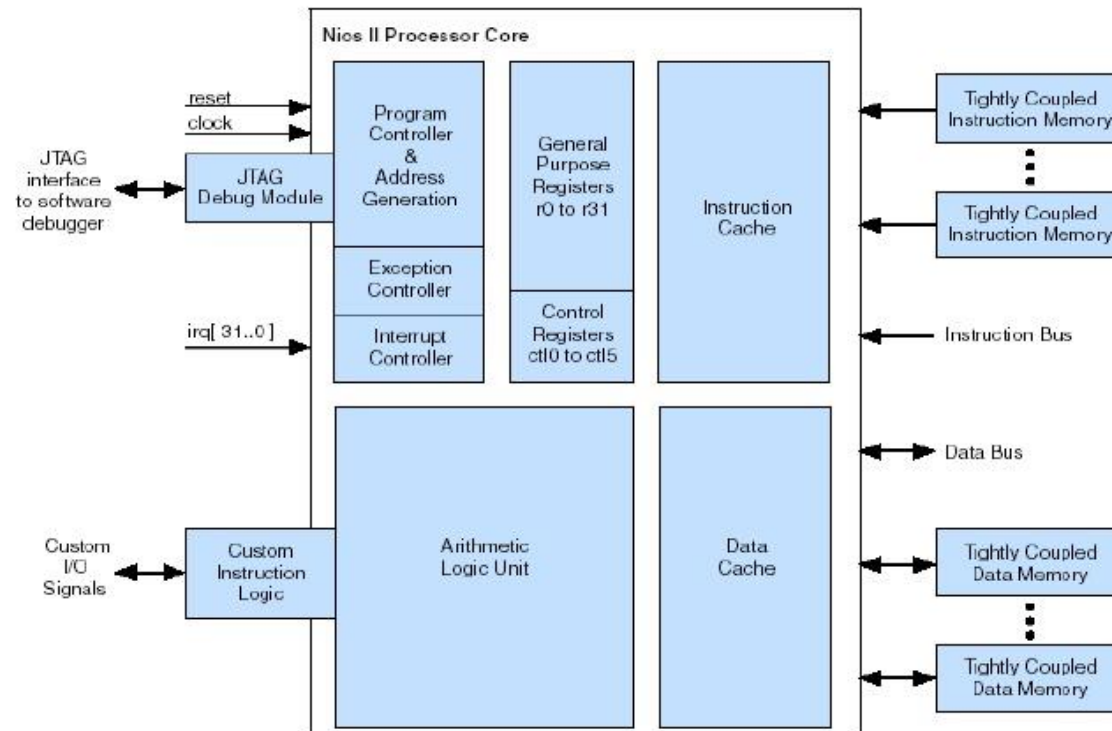
ADS-UFRN

SOFT-PROCESSOR: ALTERA'S NIOSII – NOÇÕES SOC

- Consiste num PROCESSADOR completo, cujos componentes são implementados com a estrutura lógica (blocos, elementos, tabelas etc.) do CI FPGA, daí ser chamado “soft-processor”, portanto, herda a característica REPROGRAMÁVEL do FPGA
- Ou seja, é possível sintetizar uma CPU baseada em FPGA para tarefa X ou Y
- Custom-made ou User-made PROCESSOR (memórias, periféricos, etc.)
- Características NIOSII
 - 32-bit RISC (barramentos de instrução, dados, endereçamento)
 - 32 registradores de uso geral, 32 interrupções externas
 - Multiplicadores/Divisores em hardware (32, 64, 128 bit): acelerar cálculos
 - MMU opcional (para SOs que suportam)



NIOS II Processor Core [3]



15

SOFT-PROCESSOR: ALTERA'S NIOSII

- Desenvolvimento de software em C/C++ no NIOSII Software Build Tools (SBT) integrado ao ECLIPSE
- Permite expandir de 01 CPU à várias CPUs

FAMILIAS NIOSII

Processor Core Variations

	Nios II/f Fast Core	Nios II/s Standard Core	Nios II/e Economy Core
Pipeline	6 stage	5 stage	None
Hardware Multiplier and Barrel Shifter	1 cycle	3 cycle	Emulated in software
Branch Prediction	Dynamic	Static	None
Instruction Cache	Configurable	Configurable	None
Data Cache	Configurable	None	None
Logic Elements (LEs)	1,800 without MMU 3,200 with MMU	1,200	600
Custom Instructions	Up to 256		

DO-254 Certifiable Core Based on Nios II/f Variation (Without MMU)

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ALTERA

[»]

- Fast, standard, economy
- Fast: voltado para o desempenho (maior consumo de espaço no FPGA);
- Standard: equilíbrio entre consumo de lógica e velocidade
- Economy: voltado para a economia de lógica.
- O software compilado é compatível com as 3 variações
- Na versão Economy, não há royalties nem requer licença comercial do Quartus para embarcar nas soluções
- Nas demais, exige licença comercial do Quartus

Nios II Processor Performance (MIPS*)

Device Family	Nios II/f Core
Standard-cell ASIC (~90 nm)	>500
Stratix IV	340
Stratix III	340
Stratix II	250
HardCopy IV	345
HardCopy III	260
Hardcopy II	230
Arria II GX	283
Cyclone IV GX	186
Cyclone III LS	158
Cyclone III	195
Cyclone II	145

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9

* Dhrystones 2.1 benchmark

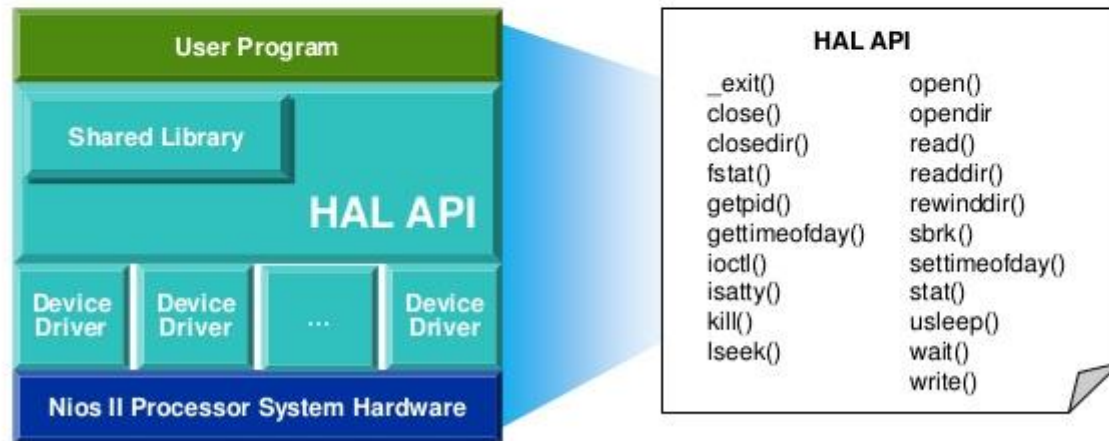


PERFORMANCE

- Core i7 7700K: >33000MIPS
- ATMEGA328P: 8-bit RISC, até 20 MIPS
- [dsPIC33: 100 MIPS 16-bit](#)
- Broadcom BCM2711B0 quad-core A72 (ARMv8-A) 64-bit @ 1.5GHz (Raspberry Pi 4): (748-2037) MIPS

Nios II HAL

- Provides run-time services and device drivers which interface to the hardware
- Allows you to change your hardware without having to change your software code
- Creates a matching custom software BSP automatically when hardware is generated



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32

ALTERA

HARDWARE ABSTRACTION LAYER

- Abstrai HARDWARE para o desenvolvedor

SOFT-PROCESSOR

- BSP (Board Support Package): link software/target (real) hardware

DE2: CYCLONE II EP2C35F672CN6 / DE2-115 (CYCLONE IV EP4CE115F29C7N)

- LINUX EMBARCADO: μ C LINUX / FREE RTOS

- Preparar HARDWARE para receber um SO

- O Nios II se comunica com os periféricos e componentes internos por meio do

Qsys (platform designer), ambiente

para criação de SOPC

(System on a Programmable Chip)

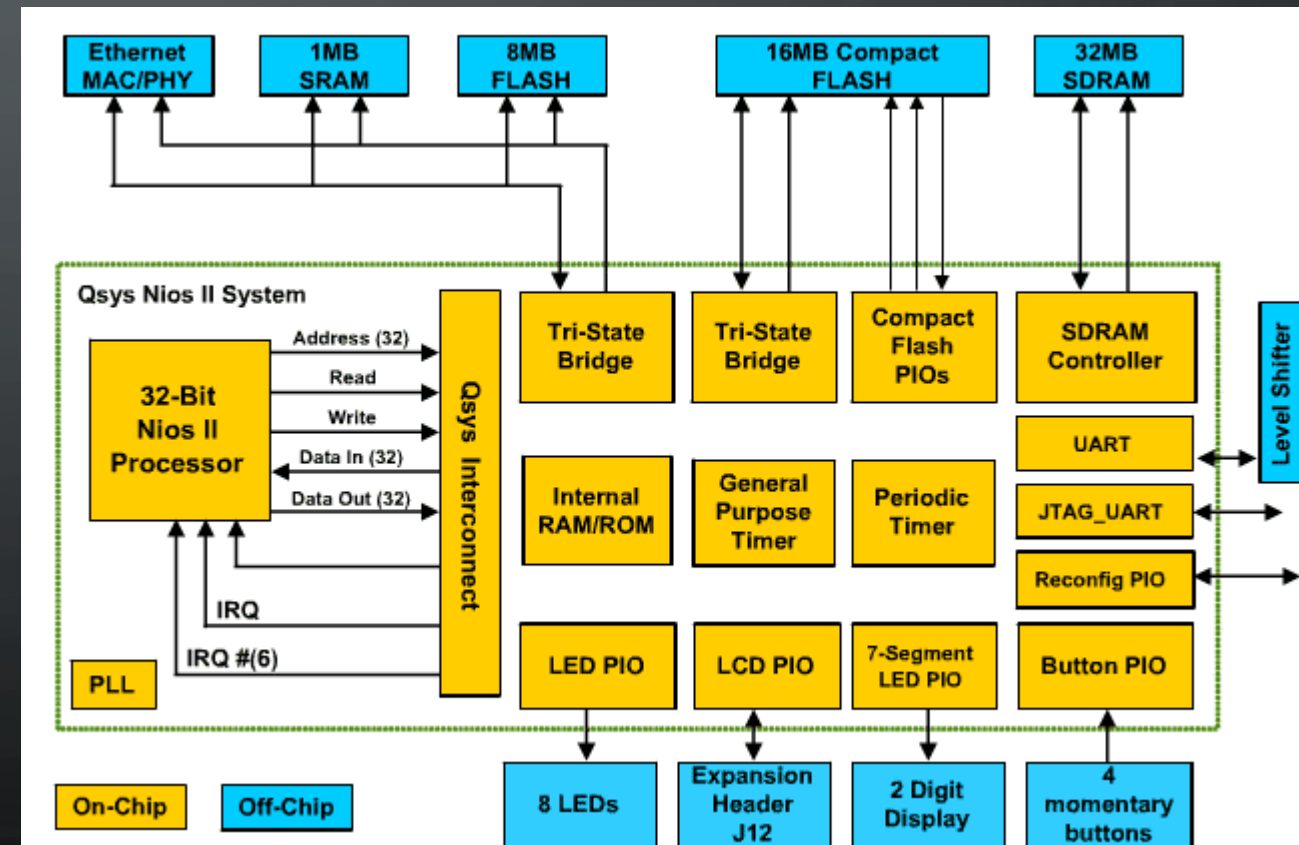
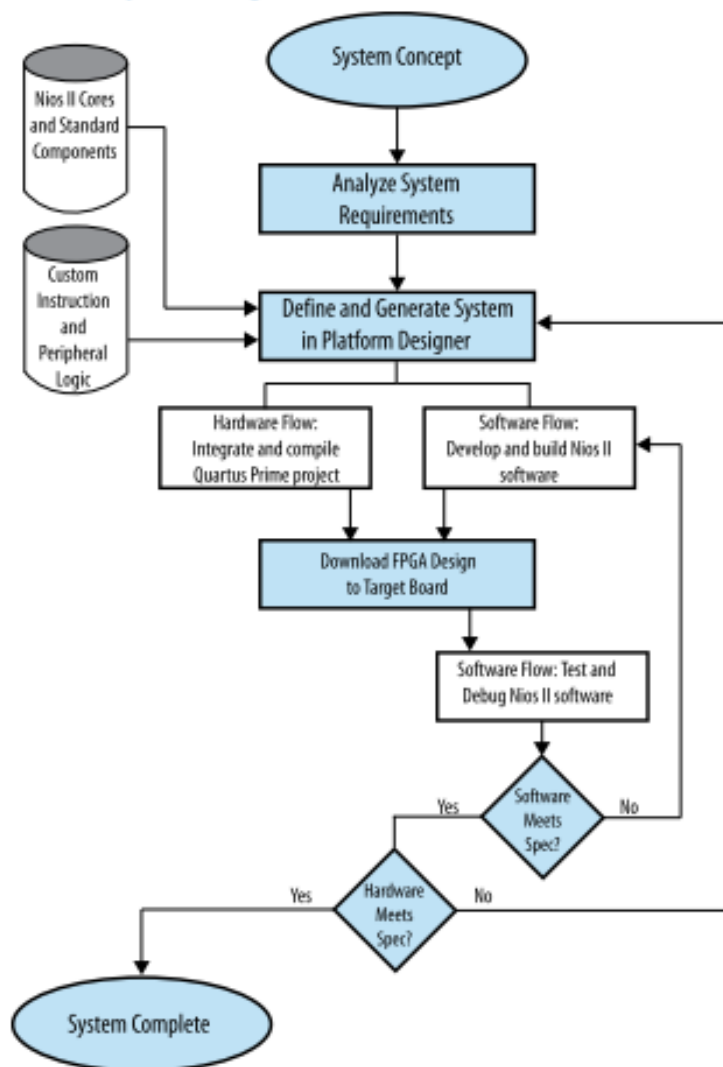


Figure 1. General Nios II System Design Flow

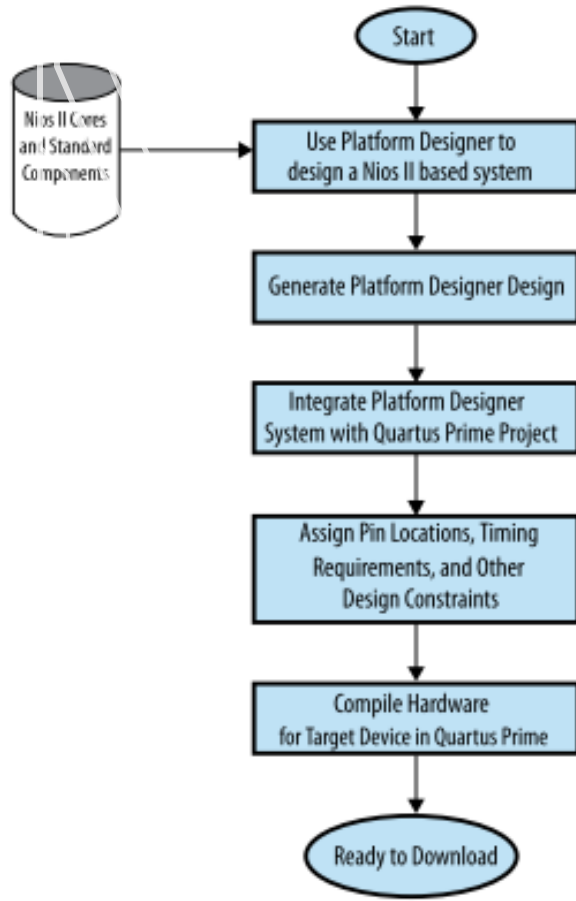


HARDWARE/SOFTWARE CO-DESIGN

Esta placa da Arrow (BeMicro SDK) já tem um design de hardware com todos os dispositivos IO integrados, sendo focada na programação em C para o NiosII, e não tão simples para VHDL, embora possível de posse das pinagens etc. Tem 512 MB LPDDR (Low Power); Cyclone IV (32 MB RAM é suficiente para portar Linux)



Nios II System Hardware Design Flow



HARDWARE DESIGN

1. novo
2. criar Sistema de hardware no qsys (platform designer)
3. gerar Sistema (há opção de criar block symbol file .bsf associado)
4. integrar ao projeto no quartus
5. incluir .qip no projeto
6. atribuir pinos (seja manualmente, seja importando .qsf da placa)
7. compilar

HARDWARE DESIGN

Arquitetura de computadores: o que necessita um computador num CHIP?

a) CPU (a qual necessita de um CLOCK); Memória (neste caso interna); Uma interface de comunicação UART

Platform Designer - niossystem.qsys (C:\system1\niossystem.qsys)

File Edit System Generate View Tools Help

IP Catalog

Project

- New Component...
- System
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Low Power
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - Qsys Interconnect
 - Tri-State Components
 - University Program

Hierarchy

Device Family

niossystem [niossystem.qsys]

- clk
- green_leds
- reset
- clock
 - clk
 - clk_in_reset
 - clk
 - clk_reset
- cpu
 - clk
 - reset
 - data_master
 - instruction_master
 - irq
 - debug_reset_request
 - debug_mem_slave
 - custom_instruction_master
- onchipmemory
 - clk1
 - s1
 - reset1
- jtag_uart
 - clk
 - reset
 - avalon_jtag_slave
 - irq
- green_leds
 - clk
 - reset
 - s1
 - external_connection
- sysid_qsys_0
 - clk
 - reset
 - control_slave

System Contents

System: niossystem Path: clock

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opcode Name
<input checked="" type="checkbox"/>		clock	Clock Source							
<input checked="" type="checkbox"/>		clk_in	Clock Input	clk	exported					
<input checked="" type="checkbox"/>		clk_in_reset	Reset Input	reset						
<input checked="" type="checkbox"/>		clk	Clock Output	Double-click to export	clock					
<input checked="" type="checkbox"/>		clk_reset	Reset Output	Double-click to export						
<input checked="" type="checkbox"/>		cpu	Nios II Processor							
<input checked="" type="checkbox"/>		clk	Clock Input	Double-click to export	clock					
<input checked="" type="checkbox"/>		reset	Reset Input	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		irq	Interrupt Receiver	Double-click to export	[clk]			IRQ 0		
<input checked="" type="checkbox"/>		debug_reset_request	Reset Output	Double-click to export	[clk]			IRQ 31		
<input checked="" type="checkbox"/>		debug_mem_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x8800	0x8fff			
<input checked="" type="checkbox"/>		custom_instruction_master	Custom Instruction Master	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		onchipmemory	On-Chip Memory (RAM or ROM) Intel ...							
<input checked="" type="checkbox"/>		clk1	Clock Input	Double-click to export	clock					
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	0x0000	0x4fae			
<input checked="" type="checkbox"/>		reset1	Reset Input	Double-click to export	[clk1]					
<input checked="" type="checkbox"/>		jtag_uart	JTAG UART Intel FPGA IP							
<input checked="" type="checkbox"/>		clk	Clock Input	Double-click to export	clock					
<input checked="" type="checkbox"/>		reset	Reset Input	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		avalon_jtag_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x8000	0x8007			
<input checked="" type="checkbox"/>		irq	Interrupt Sender	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		green_leds	PIO (Parallel I/O) Intel FPGA IP							
<input checked="" type="checkbox"/>		clk	Clock Input	Double-click to export	clock					
<input checked="" type="checkbox"/>		reset	Reset Input	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x8010	0x801e			
<input checked="" type="checkbox"/>		external_connection	Conduit	Double-click to export						
<input checked="" type="checkbox"/>		sysid_qsys_0	System ID Peripheral Intel FPGA IP							
<input checked="" type="checkbox"/>		clk	Clock Input	Double-click to export	clock					
<input checked="" type="checkbox"/>		reset	Reset Input	Double-click to export	[clk]					
<input checked="" type="checkbox"/>		control_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x8008	0x800e			

Current filter:

Messages

Type	Path	Message
3 Info Messages		
i	niossystem.jtag_uart	JTAG UART IP input clock need to be at least double (2x) the operating frequency of JTAG TCK on board
i	niossystem.sysid_qsys_0	System ID is not assigned automatically. Edit the System ID parameter to provide a unique ID
i	niossystem.sysid_qsys_0	Time stamp will be automatically updated when this component is generated.

0 Errors, 0 Warnings

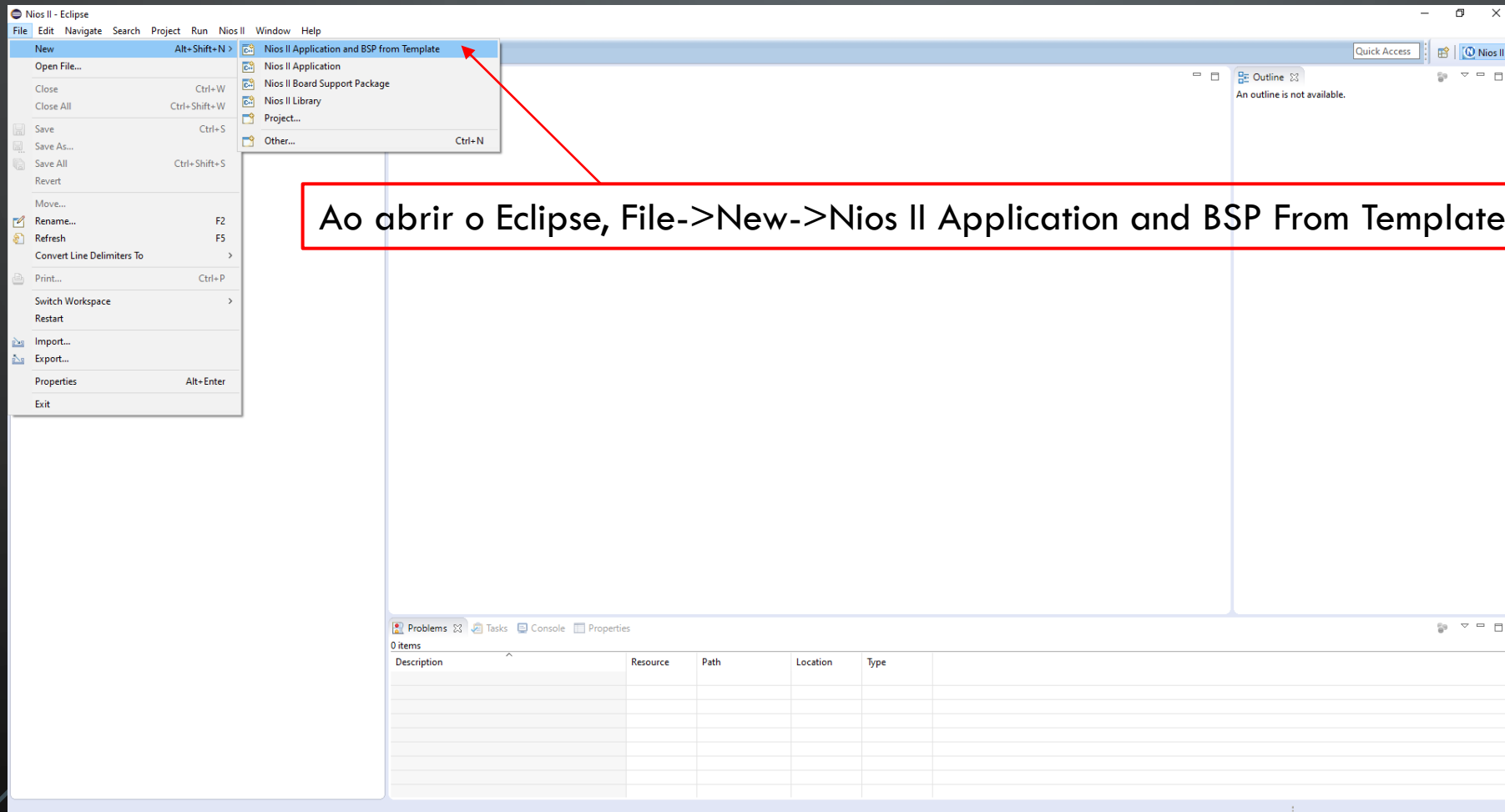
Generate HDL... Finish

Adicionalmente:

- a) PIO (leds)
- b) Chaves
- c) Display
- d) Botões
- e) ID
- f) Timer
- g) SDRAM
- h) SRAM
- i) Ethernet
- j) VGA
- k) Áudio
- l) etc.

SOFTWARE DESIGN

- Uma vez o hardware especificado no platform designer (qsys) e devidamente compilado, desenvolve-se o software em C/C++ que irá rodar na CPU especificada (Nios II)
- O Quartus possui um IDE Eclipse integrado, o qual tem suas versões atualizadas conforme a versão do Quartus!
 - Acessível em **Tools->Nios II Software Build Tools for Eclipse** – O workspace pode ser a pasta principal do projeto



SOFTWARE DESIGN

- Um dos arquivos gerados no QSYS, .sopcinfo, possui a descrição do hardware e identificação da CPU
- O mesmo deve ser informado no campo SOPC Information File name
- Há a opção de criar um projeto em branco (blank Project) ou a partir de templates. Recomenda-se iniciar com um simples template de HELLO WORLD SMALL

The screenshot displays the Nios II Eclipse IDE interface. The 'Nios II Application and BSP from Template' dialog is open, showing the 'Target hardware information' section with 'SOPC Information File name' set to 'C:\system1\niosisystem.sopcinfo' and 'CPU name' set to 'cpu'. The 'Application project' section shows 'Project name' as 'systema'. A file explorer window is open, showing the contents of the 'system1' directory, with 'niosisystem.sopcinfo' selected. A red arrow points from the 'Project name' field in the dialog to the 'systema' text. Another red arrow points from the 'SOPC Information File name' field to the 'niosisystem.sopcinfo' file in the explorer. A red box highlights the text: 'O nome do projeto pode ser por convenção o mesmo do Quartus, mas não é obrigatório'. The console window at the bottom shows the Nios II Software Build Tools output.

Nios II Application and BSP from Template

Nios II Software Examples

Create a new application and board support package based on a software example template

Target hardware information

SOPC Information File name: C:\system1\niosisystem.sopcinfo

CPU name: cpu

Application project

Project name: systema

Abrir

Este Computador > OS (C:) > system1

Nome	Data de modificação	Tipo	Tamanho
.metadata	09/02/2021 13:48	Pasta de arquivos	
.qsys_edit	09/02/2021 13:19	Pasta de arquivos	
db	09/02/2021 13:28	Pasta de arquivos	
incremental_db	09/02/2021 13:19	Pasta de arquivos	
ip_upgrade_port_diff_reports	09/02/2021 13:28	Pasta de arquivos	
niosisystem	09/02/2021 13:28	Pasta de arquivos	
output_files	09/02/2021 13:19	Pasta de arquivos	
RemoteSystemsTempFiles	09/02/2021 13:48	Pasta de arquivos	
niosisystem.sopcinfo	09/02/2021 13:27	Arquivo SOPCINFO	222 KB

Nome: niosisystem.sopcinfo

SOPC Information File (*.sopcinfo)

Abrir **Cancelar**

Problems **Tasks** **Console** **Properties**

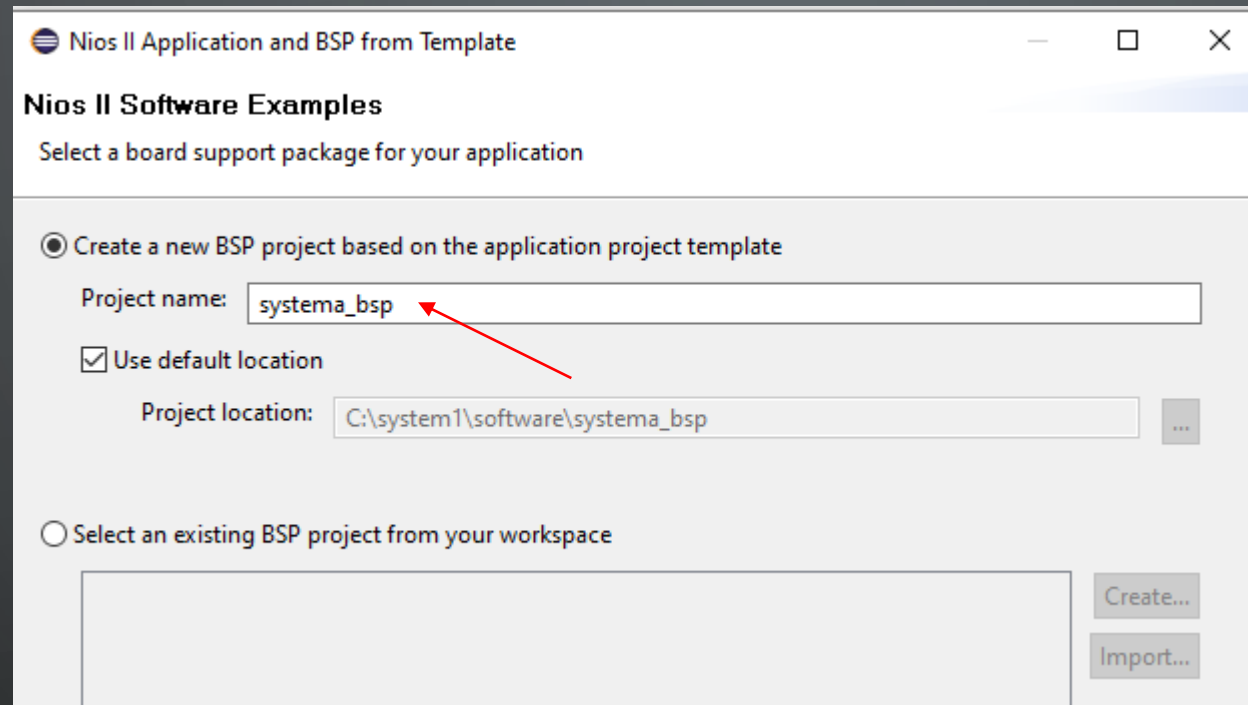
Nios II Software Build Tools

examples, refer to the Design Examples page of the Nios II documentation available with your installation at:
<installation_directory>/nios2eds/documents/index.htm.

Micrium's uC/OS-II can be used free of charge for non-commercial purposes and academic projects only.
This is not open-source software.
Use of the code is subject to the terms of an end-user license agreement, please see the license files included in the BSP project.
</nios2-swexample>

SOFTWARE DESIGN

- Na tela seguinte é solicitado o nome do projeto para criação do BSP; por default é o nome do projeto_bsp



Nios II Application and BSP from Template

Nios II Software Examples

Select a board support package for your application

☒ Create a new BSP project based on the application project template

Project name:

☒ Use default location

Project location: ...

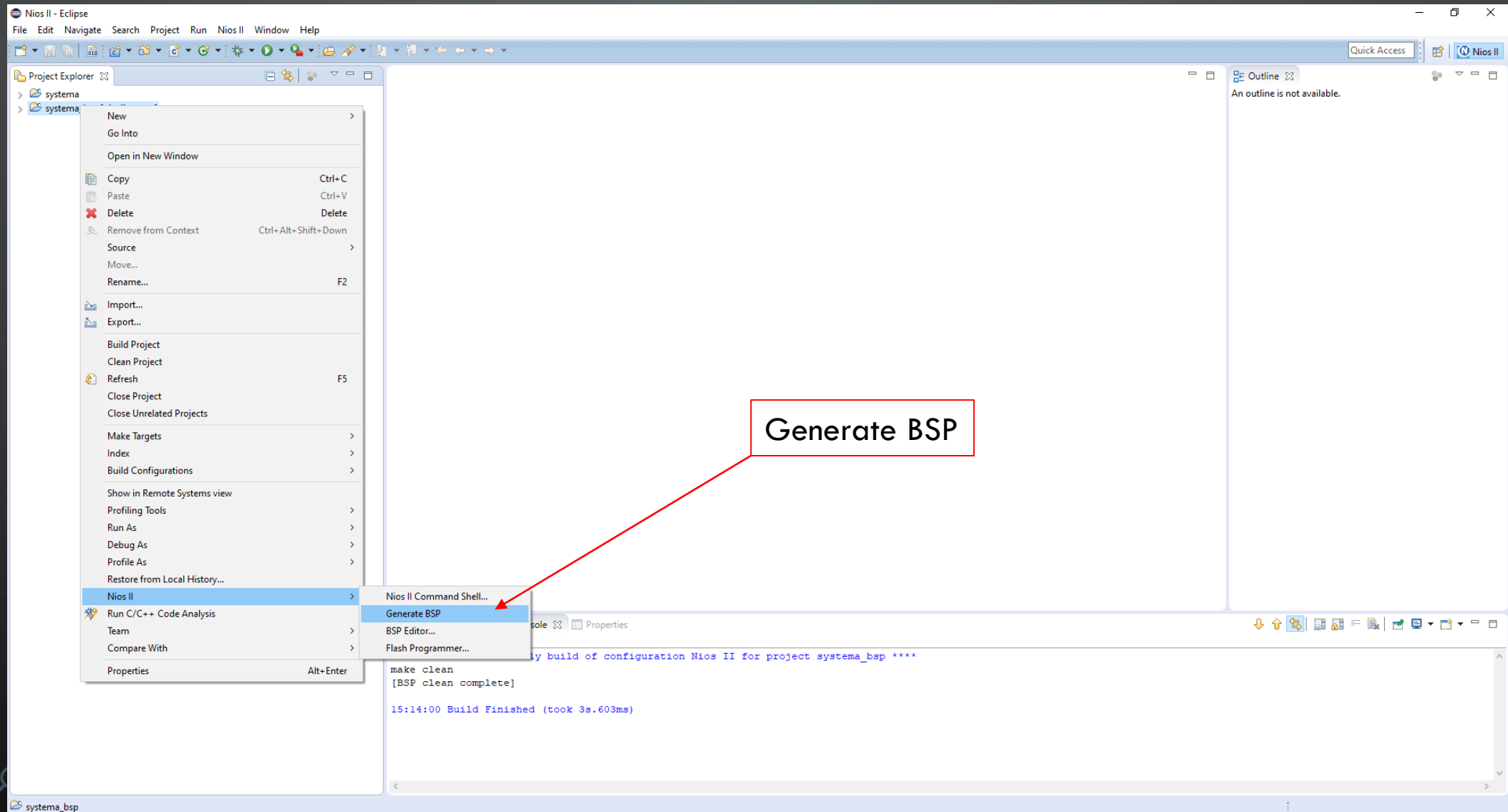
☐ Select an existing BSP project from your workspace

Create...

Import...

SOFTWARE DESIGN

- O próximo passo é clicar com o botão direito do mouse no nome do projeto BSP, opção Nios II->Generate BSP



SOFTWARE DESIGN

- O próximo passo é clicar com o botão direito do mouse no nome do projeto BSP, opção Build Project
- O mesmo deve ser realizado para a pasta do projeto em si (acima do BSP)

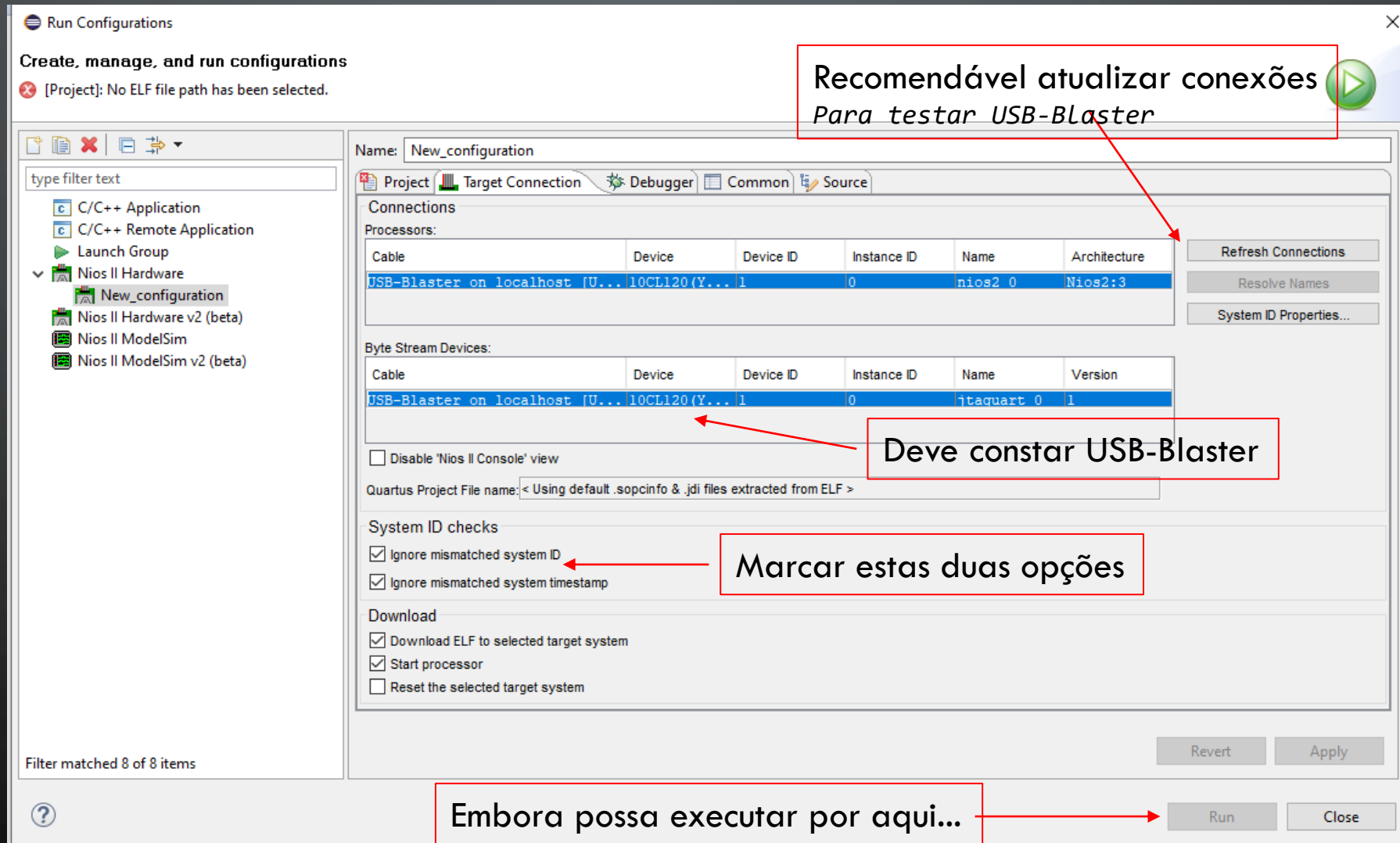
Primeiro projeto no Nios II:
simples Hello World no console
função *alt_putstr*

```
make clean
[BSP clean complete]
15:14:00 Build Finished (took 3s.603ms)
```

```
CTD Build Console [systema]
nios2-elf-insert systema.elf --thread_model hal --cpu_name cpu --qsys true --simulation_enabled false --id 4112 --sidp 0x8008 --timestamp 1612888069 --stderr_dev jtag_uart --st
Info: (systema.elf) 712 Bytes program size (code + initialized data).
Info: 19 KBytes free for stack + heap.
Info: Creating systema.objdump
nios2-elf-objdump --disassemble --syms --all-header --source systema.elf >systema.objdump
[systema build complete]
15:28:28 Build Finished (took 9s.966ms)
```

SOFTWARE DESIGN

- Ao construir (build) o projeto, é criado um arquivo .elf (ELF), o qual será transferido para o soft processor
- Menu Run-> Run Configurations



SOFTWARE DESIGN

- Ao alterar o código .c (ou .cpp se o BSP inclui esta possibilidade), basta clicar com o botão direito no nome do projeto e Ruas as-> Nios II Hardware

