Design Procedure for Two-Stage CMOS Opamp using gm/ID design Methodology in 16 nm FinFET Technology

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***Abstract*—This paper proposes a new procedure for the design of a two-stage (Miller) CMOS operational amplifier in 16 nm FinFET technology based on gm/I_D methodology. Unlike the conventional techniques, the proposed design flow allows the designer to reach the desired Opamp specifications from the first iteration, using pre-generated gm/I_D sizing charts, and without any need to a compact model equation for the FinFET device. The proposed procedure succeeded in describing the behavior of the FinFET device not only in strong inversion region but also in the week and moderate inversion regions. The designed Opamp is verified using 16 nm Predictive Technology Model (PTM-MG) for low-power FinFET (BSIM-CMG, level 72 technology). The results show that the proposed design methodology fulfills the desired Opamp specifications.**

Keywords—FinFET, Opamp design, gm/I_D methodology, Moderate inversion, Week inversion.

I. Introduction

Nowadays, the great market demands drive the semiconductor industry toward smaller size and lower power consumption [1], [2]. System-on-chip designers are in charge of covering the required demands. However, by pushing the manufacture of semiconductors towards sub-20 nm technology, some effects like short-channel effect (SCE) and gate-dielectric leakage cannot be any more neglected. This happens due to the lack of gate over channel control. One solution is the FinFET technology with a 3D structure in which a gate surrounds three sides of a vertical silicon channel (Fin). It leads to enhance the channel control, reduces the leakage current and overcomes the short-channel effect [3], [4]. Unfortunately, the device downscaling is not the only problem for the analog designers, but also challenging of the conventional square-law MOSFET model that cannot any more accurately describe the new devices such as FinFET. To overcome this problem, a new design procedure that describes FinFET behaviour is highly recommended. The needed FinFET procedure has to be survived in all inversion regions (strong, moderate and week inversion regions) in low power consumption applications [5], [6]. Gm/I_D design methodology [7]–[11] is a promising methodology to overcome the drawbacks of the conventional design that is based on square-law. It gives the analog designer a full control and flexibility on the design trade-offs.

This paper is organized as following. Section II describes a systematic design procedure for the two-stage (Miller) Op-amp. Section III illustrates the simulation results of the proposed design procedure in comparison with the desired amplifier specifications and followed by a conclusion in Section IV.

II. Two-stage (Miller) OpAmp Design Procedure

This section provides a guideline for the design flow of a two-stage (Miller) operational amplifier. It gives the dimensions of the FinFETs (fin height, fin thickness, and channel length) as well as the value of the compensation capacitor that satisfies the amplifier specification. The schematic of the two-stage operational amplifier is shown in Fig. 1. Table 1 shows the Op-amp targeted specifications. It is logical to start the design procedure with the noise requirement. At high frequency, the input-referred noise voltage ($S_n(f)$) is given by [12]:

$$S_n(f) = 2\,.\,4kT\,\frac{2}{3}\frac{1}{gm_{1,2}}[1+\frac{gm_{3,4}}{gm_{1,2}}] \quad (1)$$

For a lower noise, we can assume $gm_{3,4} << gm_{1,2}$. So, the transconductance $gm_{1,2}$ can be expressed by (2), and then calculated using the $S_n(f)$ specification.

$$gm_{1,2} = \frac{16}{3}\frac{kT}{S_n(f)} \quad (2)$$

A. The Compensation Capacitance (C_C)

For a specified value of the gain-bandwidth product, the compensation capacitance Cc will be calculated from (3) [13], using the gain-bandwidth product (GBW) specification:

$$GBW_{Hz} = \frac{gm_{1,2}}{2\pi\,C_c} \quad (3)$$

B. Input-pair Design (M1 and M2)

For calculating the aspect ratio of the input pair, first we have to calculate the drain current I_{D1} which is calculated from the specified slew-rate using equation (4) [12].

$$I_{D1} = \frac{SR_I\,.\,C_c}{2} \quad (4)$$

$$A_{V1} = \frac{gm_{1,2}}{gds_{1,2}+gds_{3,4}} \quad (5)$$

Then by choosing a convenient value of the DC-gain for the first stage (A_{V1}), and by assuming that $gds_{1,2}$= $gds_{3,4}$ for simplicity , the value of the transconductance $gds_{1,2}$ could be

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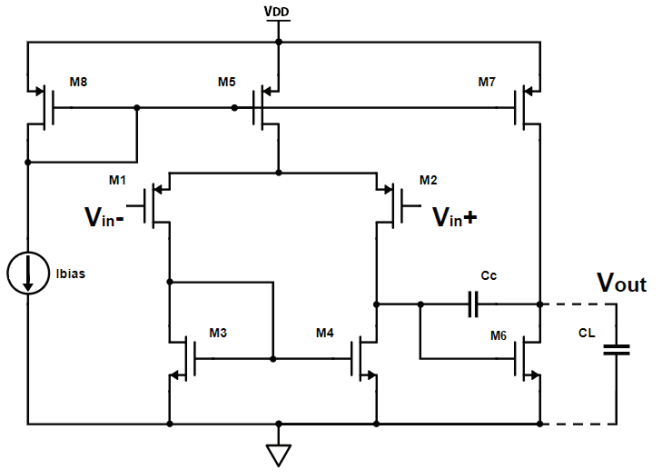


Fig. 1. Schematic of the two-stage (Miller) operational amplifier.

calculated from (5) [13]. The length (L) of the transistors M1 and M2 can be found by finding the intersection point between the pre-calculated values of gm_2/I_{D2} and gm_2/gds_2 on the first PFET sizing chart shown in Fig. 2(a), then the effective width (W) could be found by finding the intersection point between gm_2/I_{D2} and the choosen length curve (from the previous step) on the second sizing chart Fig. 2(b). thus, we found the aspect ratio $(W/L)_{1,2}$ for both M1 and M2. And by using them again on the third sizing chart Fig. 2(c) we could found V_{GS1} that will be used in finding $(W/L)_{3,4}$.

C. Current Mirror Load Design (M3 and M4)

To design the active load of the first stage (M3,4), we will use the pre-designed values for $gds_{3,4}$ and $I_{D3,4}$, and by assuming an arbitrary but large current efficiency $(gm/I_D)_{3,4}$ (this assumption will be checked soon), we could use $(gm/I_D)_{3,4}$ and $(gm/gds)_{3,4}$ on the first NFET sizing chart Fig. 3(a) on which the length $(L_{3,4})$ can be picked easily. $V_{GS3,4}$ will be calculated from the lower common mode input range ($CMIR_{low}$) specification, V_{GS1} and V_{DSat1}. Then the correct $(gm/I_D)_{3,4}$ will be found using $V_{GS3,4}$ and $L_{3,4}$ on the last sizing chart Fig. 3(c), this $(gm/I_D)_{3,4}$ should be firstly checked before finding the effective width (W). So, if the calculated current efficiency of M3,4 is greater than the assumed value, this means a lower gain and then we have to assume a higher current efficiency and recalculate the length $(L_{3,4})$ again, else if it was smaller than the assumed value (this means a higher gain) then it is a convenient $(gm/I_D)_{3,4}$ value. Thus, the effective width $(W_{3,4})$ will be calculated with the aid of the second sizing chart Fig. 3(b).

D. Tail Current Source Design (M5)

To find the aspect ratio of the tail current source we will use the common mode rejection ratio specification (CMRR). the CMRR is given by [13]:

$$CMRR = \frac{A_{vd}}{A_{CM}} = \frac{gm_{1,2}}{gds_{1,2} + gds_{3,4}} \,.\, 2\, gm_{3,4} \,.\, R_{ss} \qquad (6)$$

After calculating the transconductance gds_5 (gds_5=1/Rss), and by knowing I_{D5} ($I_{D5} = 2I_{D1}$) we can find the aspect ratio of M5 $(W/L)_5$ in same manner used before for calculating the aspect ratio of M3 and M4 as illustrated in the design procedure flow chart (Fig. 4).

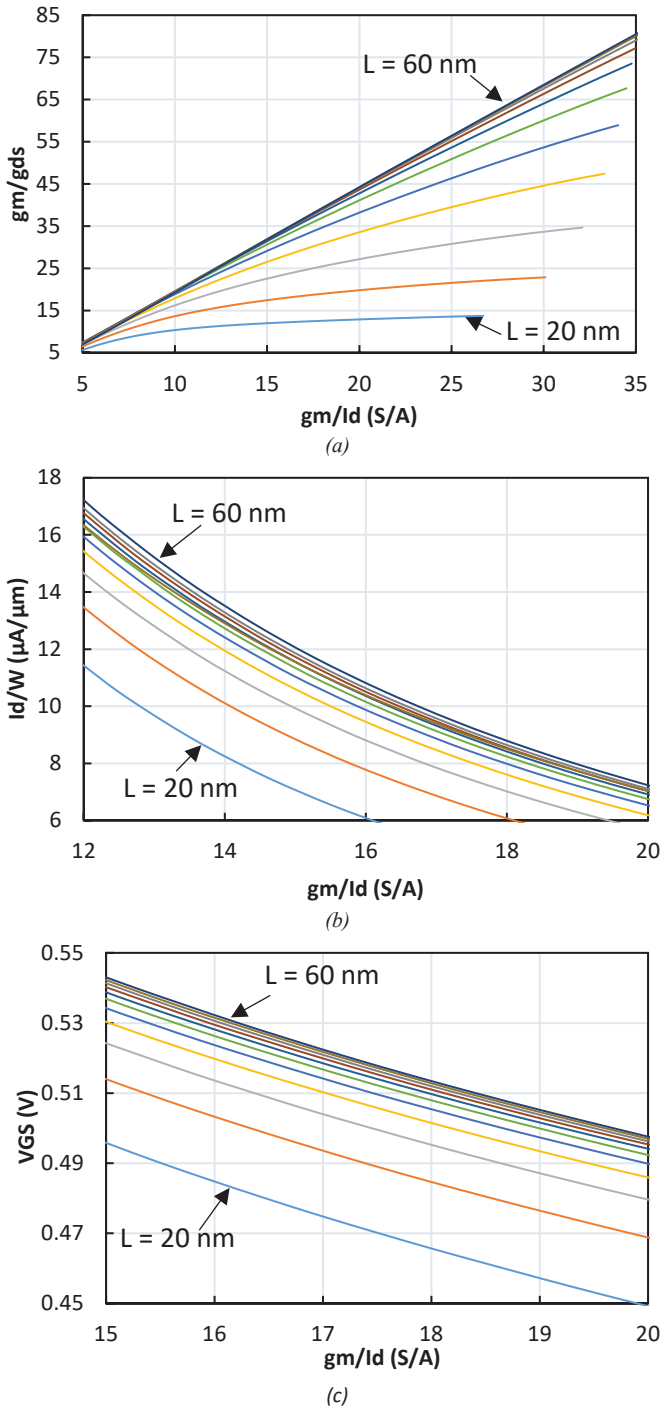


Fig. 2. Sizing charts 1, a PFIT sizing charts vs gm/ID with length as a parametric parameter (By a 4 nm step): (a) intrinsic gain (gm/gds), (b) current density (ID/W), (c) gate-source voltage VGS.

E. The Second Stage Amplifier (M6)

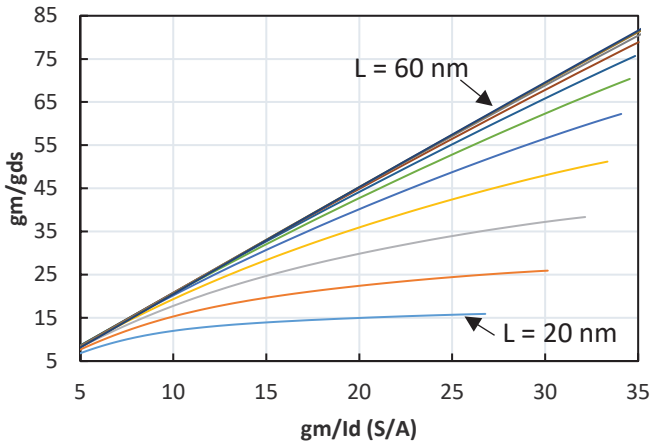
In order to achieve the required slew rate specification, the internal slew-rate (SRI) which is associated with C_C has to be less than or equal the external slew-rate (SRII) which is associated with C_L. The current I_{D6} must be chosen in order to fulfill the required slew rates and power-consumption requirements. So, I_{D6} could be calculated to satisfy the following condition [12]:

$$\frac{I_{D1}}{I_{D6}} \leq \frac{C_C}{2(C_L + C_C)} \qquad (7)$$

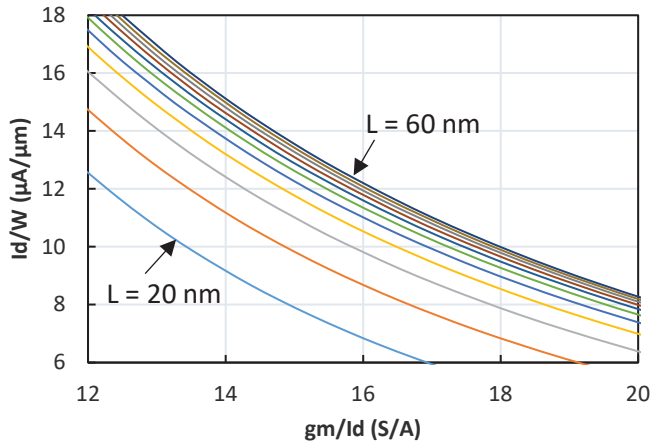
In order to achieve the phase margin given in (8), the second pole (p2) and the first zero (z1) will be represented in terms of gm, C_L and C_C and rewritten in equation (9) [14], so we can calculate gm_6, such that K= $(\frac{gm1/I_{D1}}{gm6/I_{D6}})$. Thus, we have our design knob $(gm/I_D)_6$ for designing M6. So, the aspect ratio $(W/L)_6$ could be found by following the same steps for achieving $(W/L)_{1,2}$.

$$PM° = 90° - \tan^{-1}\left[\frac{GBW}{p2}\right] - \tan^{-1}\left[\frac{GBW}{z1}\right] \quad (8)$$

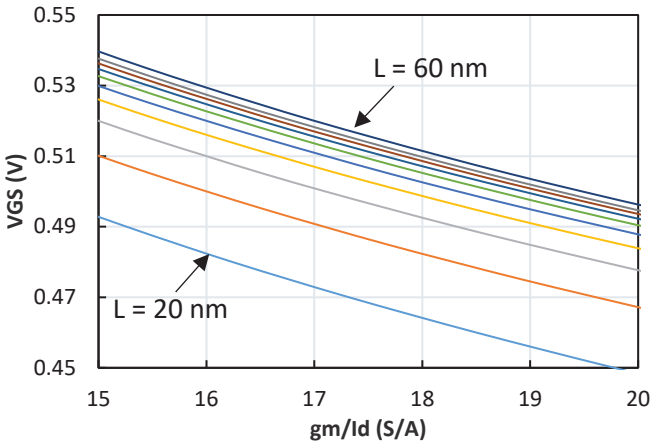
$$PM° = 90° - \tan^{-1}\left[K\frac{I_{D1}}{I_{D6}}\frac{C_L}{C_C}\right] - \tan^{-1}\left[K\frac{I_{D1}}{I_{D6}}\right] \quad (9)$$



(a)



(b)



(c)

Fig. 3. Sizing charts 1, a NFIT sizing charts vs gm/I_D with length as a parametric parameter (By a 4 nm step): (a) intrinsic gain (gm/gds), (b) current density (I_D/W), (c) gate-source voltage V_{GS}.

TABLE 1. SPECIFICATIONS AND SIMULATION RESULTS FOR THE TWO-STAGE (MILLER) OPAMP

Specification	Required	Simulation
Technology	16 nm FinFET	16 nm FinFET
Supply voltage	0.9 V	0.9 V
Load capacitance	5 pF	5 pF
GBW	>= 35 MHz	39.1 MHz
DC gain (Ao)	>= 60 dB	61.3 dB
Phase margin (PM)	>= 60°	60.4°
CM input range – low	<= 0.2 V	0.2 V
CM input range – high	>= 0.5 V	0.5 V
CMRR	70 dB	68 dB
$S_n(f)$	8 nV/√Hz	8.58 nV/√Hz
Slew rate (SR)	15 V/µs	15.4 V/µs

TABLE 2. DESIGN PARAMETERS

	(W/L) µm/nm	H_{Fin} nm	N-Fins	N-Fingers	T_{Fin} nm
$M_{1,2}$	14.28/40	192	6	6	12
$M_{3,4}$	1.95/40	116	4	2	12
M_5	22/40	240	5	9	12
M_6	42/40	254	9	9	12
M_7	88.5/40	240	20	9	12
M_8	18/40	240	4	9	12
CC	1.26 pF				

F. The Second Stage Load (M7) and the copying transistor (M8)

The output transconductance of M7 (gds_7) should have a specific value in order to achieve the required DC voltage gain for the second stage (A_{V2}). Also, for a better mirroring accuracy, the length of the transistor M7 should equal the length of the transistor M5. Therefore, the effective width of M7 is easily found by following the same way of finding $W_{3,4,5}$.

The length of the diode-connected transistor M8 has to be the same as the transistors M5 and M7. For a better mirroring accuracy while copying I_{bias} from M8 to M5 the effective width of M8 should be [15]:

$$W8 \approx \frac{2}{3} W_5 \frac{I_D 8}{I_D 5} \quad (10)$$

III. SIMULATION RESULTS

To justify the proposed procedure, a two-stage CMOS operational amplifier is designed based on gm/I_D methodology and simulated using 16 nm Predictive Technology Model (PTM-MG) for low-power FinFET (BSIM-CMG, level 72 technology) to meet the targeted amplifier specifications shown in Table. 1. The design parameters of the two-stag (Miller) Op-amp shown in Fig. 1 are obtained from the first iteration based on the proposed design procedure shown in Fig. 4. Table 2 shows the calculated Op-amp design parameters.

Fig. 5 shows that the DC-gain and the phase margin are similar to the desired specifications, and the unity gain bandwidth is much better than the targeted one. Also fig. 6 which shows the step response of the designed two-stag (Miller) Op-amp illustrates a very acceptable slew-rate in comparison to the desired specification. Table 1 demonstrates the accuracy of the proposed design procedure in satisfying the required specifications.

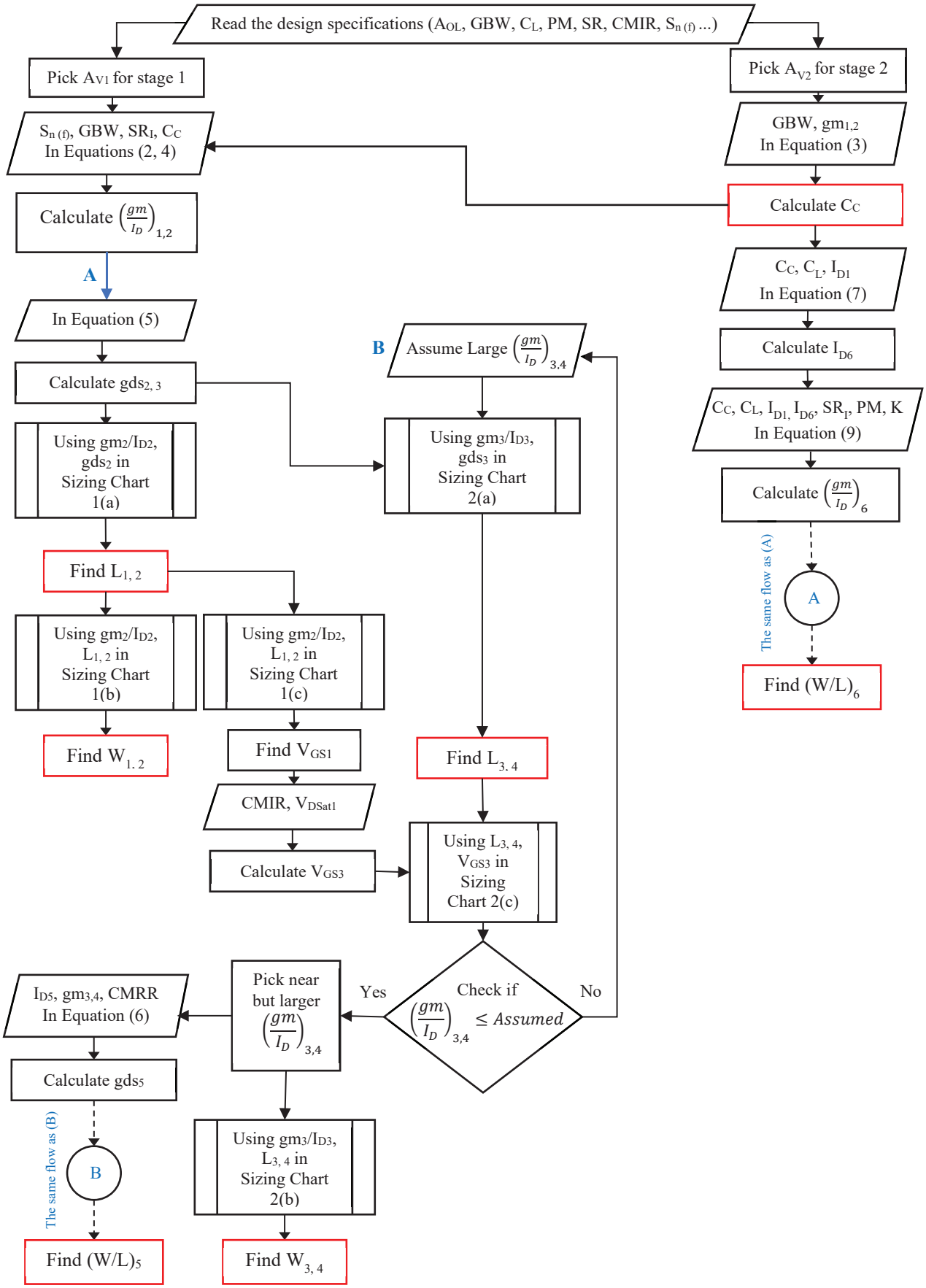


Fig. 4. The proposed design procedure for the two-stage (Miller) opamp.

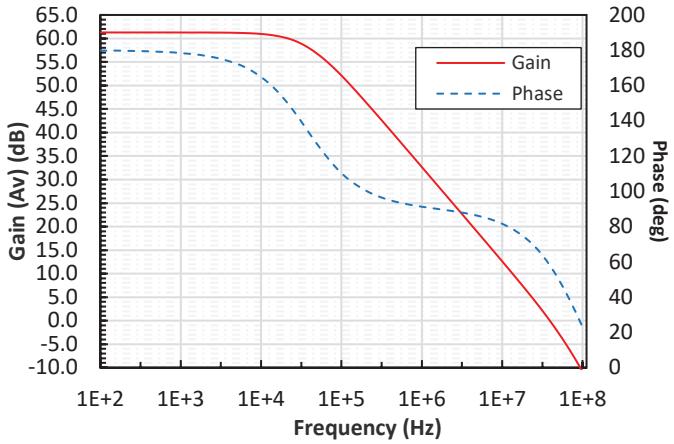


Fig. 5. Loop gain frequency response of the designed two-stage opamp.

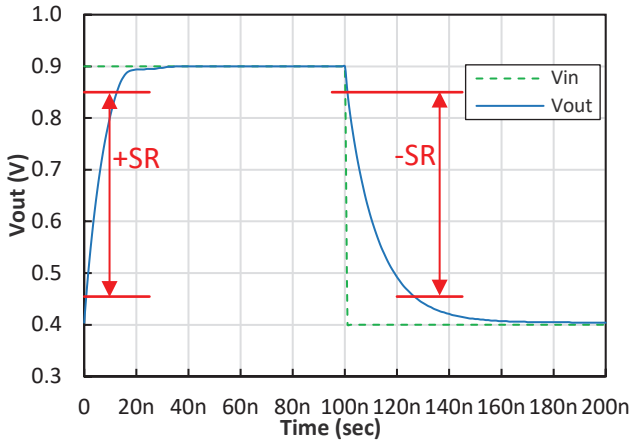


Fig. 6. Step response of the designed two-stage opamp in unity-gain configuration.

IV. Conclusion

This work proposed a procedure that reinforces analog integrated circuit designers with a better tool that gives the availability of compromising between the two-stage operational amplifier figure-of-merits and met the design requirements from the first iteration. A flow-chart that describes all the design steps for each transistor starting from the design specifications ending to the transistors' aspect ratio has been presented. Simulation results of two-stage operational amplifier that confirmed the availability and simplicity of the proposed procedure have been carried.

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