

Design and Implementation of Operational Amplifiers with CMOS 180 nm Technology Node using gm/ID Methodology

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Abstract—This work deals with the design procedures for single stage and two stage operational amplifiers with CMOS 180 nm technology node using gm/ID methodology. The gm/ID methodology is a graphical technique for sizing the transistors to achieve the Figure of Merits and it helps to address the shortcomings of square law. The gm/ID lookup tables are generated for both PMOS and NMOS with CMOS 180 nm technology node in cadence virtuoso tool. The usage of design equations as constraints on the gm/ID lookup tables provide an efficient sizing to satisfy the Figure of Merits. The proposed methodology offers the advantage of reducing transistor sizes. In general, the gm/ID lookup table contains multiple possible values for a given combination of current, gain and gm/ID ratio and proposed methodology chooses the most appropriate value to optimize the transistor's area in the circuit design. This helps achieve the desired gm/ID ratio while minimizing the physical space occupied by the transistor. This reduction in transistor dimensions enables overall area reduction. The proposed methodology helps to improve the Common Mode Rejection Ratio of the single stage and two stage operational amplifier. It also provides an increased differential gain in case of two stage operational amplifier. The design is validated with cadence virtuoso and the results are compared.

Index Terms—operational amplifiers; gm/ID methodology; sizing; Common Mode Rejection Ratio; differential gain; Figure of Merits; CMOS

I. INTRODUCTION

Analog circuit design is crucial in today's world, with operational amplifiers (op-amps) serving as fundamental building blocks for various applications such as filters, converters, rectifiers, and comparators. Op-amps are also used as drivers for analog-to-digital converters. While the square law MOSFET model falls short in describing the behavior of short-channel and moderate/weak inversion devices, the gm/ID methodology addresses these limitations and bridges the gap between manual analysis and simulation. Transistor sizing, a key aspect of analog circuit design, can be achieved using the gm/ID methodology, considering factors like noise efficiency, common-mode gain, and input common-mode range.

Shi et al., [1] proposed a systematic initial sizing method for designing multi-stage op-amps using the gm/ID method.

Design equations are used as constraints for the gm/ID lookup table, enhancing the reliability of sizing calculations and reducing the need for simulation-based corrections. These design equations ensure frequency performance and leverage regular sizing rules for configuring multi-stage op-amps.

Palmisano et al. [2] presented the design of two-stage operational transconductance amplifiers (OTA) using first-order transistor models and design equations optimized to achieve high gain-bandwidth product through frequency compensation techniques. Sabry et al. [3] and Elbadry et al. [4] incorporated design equations as constraints for OTA design.

Konishi et al. [5] focused on designing low-power and high-speed OTAs using the gm/ID lookup table method, considering different operating regions and employing analytical and simulation-based methods to optimize parameters while accounting for second-order effects. Singh et al. [6] and Girardi et al. [7] used the gm/ID lookup table method for designing CMOS folded cascode OTAs. Hillebrand et al. [8] incorporated the gm/ID methodology in a tool that provides information on operating point-dependent degradation caused by Hot Carrier Injection and Negative Bias Temperature Instability. Common-source amplifiers and Miller OTAs are also designed and implemented in Hillebrand et al. [8].

Krishnan et al. [9] presented a comparative study of the gm/ID methodology for low-power applications, offering a systematic procedure to fix transistor sizing and current while achieving gain-bandwidth product specifications through area optimization. Rakús et al. [10] analyzed traditional design techniques for low-voltage analog integrated circuits, differential amplifiers and current mirrors. Hesham et al. [11] implemented the gm/ID technique for a two-stage Miller operational amplifier in FinFET technology, considering low-power features in the design.

Aminzadeh et al. [12] presented a systematic approach that considers short-channel MOS devices in various process and temperature corners, utilizing matrix representations for bias conditions and small-signal parameters to generate generalized gm/ID functions. Efficient frequency compensation techniques

for CMOS three-stage OTAs are discussed in Liu et al. [13] and Marano et al. [14] for folded cascode OTAs with Miller capacitor compensation and feedforward stages, respectively.

Dammak et al. [15], Pinjare et al. [16], Singh et al. [6], Sanabria-Borbon et al. [17], Giustolisi et al. [18], and Shi [1] applied the gm/ID technique to various circuits, including folded cascode amplifier, differential amplifiers, current mirrors, common-source amplifiers, op-amps, and OTAs. Pollissard-Quatremère et al. [19] suggested modifying the

gm/ID technique for advanced short-channel CMOS technologies to expedite the design process and provide accurate transistor sizing. Ou et al. [20] proposed using unit-sized transistors to minimize the impact of small geometry effects on gm/ID-dependent parameters.

This paper focuses on the design of single-stage and two-stage op-amps using the gm/ID methodology and tabulates the Figure of Merits. The amplifier stages, gm/ID methodology, and design process are described in Sections II, III, and IV respectively. Results and discussions are presented in Section V, with the conclusion followed in Section VI.

The following novelties are implemented in this paper,

1. Overall area reduction achieved for the desired specification.
2. Two stage operational amplifier shows improved gain and Common Mode Rejection Ratio (CMRR).

II. AMPLIFIER STAGES

A. Single Stage Operational Amplifier

A single stage operational amplifier is shown in Figure 1. It consists of a regular differential stage. The single stage operational amplifier designed in this paper consists of six transistors and a load capacitance CL. The single stage amplifier is designed as per the specifications and the results are tabulated in Section VI. The Figure of merits such as Differential Gain, Common Mode Gain, Common Mode Rejection Ratio, Gain Bandwidth product, Slew Rate and Phase Margin are considered.

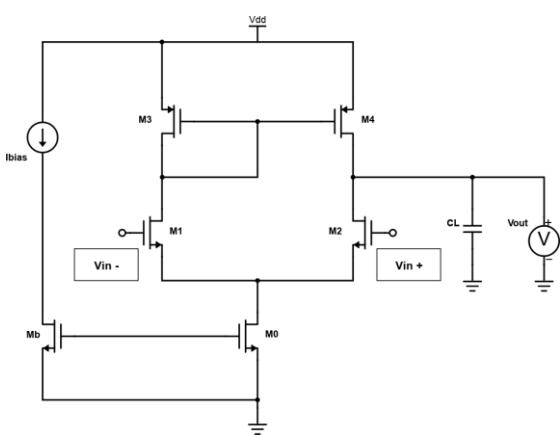


Fig. 1. Single stage operational amplifier

The gm/ID methodology is used to design the widths and lengths of the six transistors and the Figure of Merits

are verified. The gm/ID constraints are obtained with the specifications given in Table I. The design of transistors M1 and M2 involves the Gain Bandwidth Product specification which helps in achieving the gm/ID constraint of transistors M1 and M2. The design of transistors M3, M4 and M0 is obtained by gm/ID method with the help of Input Common Mode Range, Common mode gain and the noise factor. Using the current proportionality, the design of the transistor Mb is obtained from the transistor M0.

B. Two Stage Operational Amplifier

The main advantage for designing the two stage Op Amp is mainly for the gain which combines the gain of first and second stages. The single stage Op Amp which uses a smaller number of transistors for driving the load capacitance has gm/ID design procedures, which can be used to design the first stage of two stage Op Amp. But in two stage operational amplifier, the load capacitance driven by second stage modifies the GBW design equation as follows.

$$GBW = \frac{g_{m1,2}}{2\pi * C_c} \quad (1)$$

The first stage in two stage Op Amp loads with compensation capacitor CC, instead of load capacitance CL. Rewriting the above equation including a gm/ID variable.

$$C_c = \left(\frac{g_m}{I_D} \right)_{1,2} \left(\frac{I_{D1,2}}{2\pi * GBW} \right) \quad (2)$$

Where $g_{m1,2}$ is the transconductance of the differential input pair and $I_{D1,2}$ is the drain current of the same. Note the compensation capacitance C_c is also related to Slew rate. Hence, choosing C_c value is very crucial while designing the Op Amp.

The second order pole makes the direct impact on the high frequency behavior. As per the suggestion provided by Palmisano et al. (2001), it is advisable to use a separation factor.

$$\chi = \frac{P_2}{GBW} > 1 \quad (3)$$

The second dominant pole p2 must be taken care properly while design a two stage Op Amp and it can be denoted as

$$P_2 = \frac{g_{m6}}{2\pi C_L} \quad (4)$$

Where g_{m6} is the transconductance of the transistor M6 of the second stage. Rewriting the above equation as

$$g_{m6} = 2\pi * GBW * C_L * \chi \quad (5)$$

Dividing both sides by the drain current of M_6 , we get

$$\frac{g_{m6}}{I_{D6}} = 2\pi * GBW * \frac{C_L}{I_{D6}} * \chi = \frac{2\pi * GBW}{SR} \quad (6)$$

Where $\frac{I_{D6}}{C_L}$ approximately equal to negative slew rate and SR denotes Slew rate. A two stage operational amplifier with Miller compensation is shown in Figure 2.

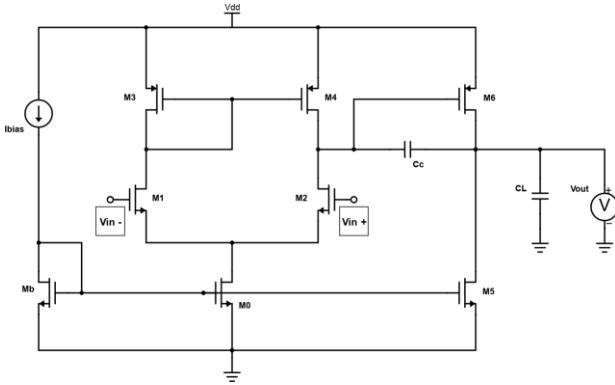


Fig. 2. Two Stage Op Amp with Miller Compensation

III. THE GM/ID METHODOLOGY

The gm/ID denotes ‘transconductance to drain current ratio’ [2]. It is the measure of transconductance of a transistor per unit drain current. The magnitude range of gm/ID gives the inversion level of the transistor. A small gm/ID indicates that the transistor is in strong inversion whereas large gm/ID indicates weak inversion of transistor. The gm/ID curves depends on the process technology which means that the gm/ID curves differ for each process technology.

The gm/ID profile of a technology is a collection of combination of dc curves obtained by dc sweep simulation over a single transistor i.e., either PMOS or NMOS. Typical simulation setting is as follows: Fix the drain to source voltage of the transistor VDS i.e. (say 1/2 or 1/3 of VDD) depending on the number of the transistors in the stage column. Then fix the channel width of the transistor W i.e., say 10um in case of 0.18 um technology.

The curves were obtained by running a dc sweep simulation for a NMOS transistor. The width was fixed at 10 um and length was varied from 0.18um to 1.5um. In this case, we ignored the second order effects to simplify the sizing.

The lookup tables were generated for the parameters such as VGS, VDS, gm and ID respectively.

IV. THE GM/ID CONSTRAINTS

A. Application of gm/ID methodology for first stage

1) *Using ICMR spec to derive gm/ID constraint:* The specification given for ICMR puts voltage constraints on the input MOS transistors at their gate terminals. Here, we gm/ID values measured in correspondence to V_{GS} and V_{DSAT} . Suppose the ICMR specification is given as [$ICMR_{min}, ICMR_{max}$]. In this case, we assume that the differential stage has NMOS input pair as shown in Figure 1. We can derive the design equation as $V_{DSAT\ 0max} = ICMR_{min} - V_{GS1,2}$, in which $V_{GS1,2}$ can be determined using $gm/ID_{1,2}$. On the other hand, $V_{DS3,4min} = ICMR_{max} - V_{THp1,2}$, where threshold voltage $V_{THp1,2}$ can be known from the process technology or by using gm/ID curves. Then, $V_{GS3,4max} = V_{DD} - V_{DS3,4min}$ is useful for finding $V_{GS3,4max}$.

After determining $V_{GS3,4max}$ and $V_{DSAT\ 0max}$, we can find $gm/ID_{3,4min}$ and gm/ID_{0min} respectively. Then proceed to derive the constraints using noise and common mode gain.

2) *Using noise efficiency for gm/ID constraint:* The first stage of Op Amp is considered the primary source for noise. The noise PSD $S_n(f)$ is denoted as follows.

$$S_n(f) = \frac{4kT\gamma_{eff}}{g_m^2} \quad (7)$$

Where $\gamma_{eff} = \gamma_N g_{mN} + \gamma_P g_{mP}$, k is the Boltzmann constant, t is the absolute temperature, γ_{eff} is the effective noise coefficient and γ_N and γ_P are the NMOS and PMOS noise coefficients respectively. We can use the above transfer function for gm/ID procedure. Rewriting the above equation as

$$S_n(f) = \frac{4kT}{g_m N} (\gamma_N + \gamma_P \frac{\frac{g_{mP}}{ID}}{\frac{g_{mN}}{ID}}) \quad (8)$$

3) *Using common mode gain spec for gm/ID constraint:* The common mode gain which is denoted as A_{cm} is approximately denoted as follows.

$$A_{cm} \approx \frac{g_{ds0}}{2g_{m3,4}} \quad (9)$$

Assume that.

$$\frac{g_{ds0}}{2g_{m3,4}} \leq A_{cm,max} \quad (10)$$

Where $A_{cm,max}$ denotes the maximum of A_{cm} . Rewriting the above equation gives

$$\frac{g_{m0}}{2g_{m3,4}} \leq A_{cm,max} \frac{g_{m0}}{g_{ds0}} = A_{cm,max} \cdot A_{M0} \quad (11)$$

Where A_{M0} stands for intrinsic gain of the transistor M_0 . Dividing both sides by $I_{d0} = 2I_{D3,4}$ leads to

$$\left(\frac{g_{m0}}{I_{D0}} \right)_{max} = (A_{cm,max} \cdot A_{M0}) \frac{g_{m3,4}}{I_{D3,4}} \quad (12)$$

Where I_{D0} and $I_{D3,4}$ denote the drain currents of the corresponding transistors. Note that $A_{cm,max}$ can be derived from the CMRR equation.

$$A_{cm,max} = A_d(dB) - CMRR_{min}(dB) \quad (13)$$

Where A_d is the differential gain in dB of the differential stage of the Op amp.

B. Application of gm/ID Methodology for common source stage

The intrinsic gain (A_v) of a single transistor can be found by $A_v = g_m R_{DS}$, Where g_m is the transconductance of the transistor and R_{DS} is the drain to source resistance or output resistance of the transistor.

In case of complementary transistor, the output stage resistance is as follows.

$$R_{o,stg}^{-1} = R_{DS,n}^{-1} + R_{DS,p}^{-1} \quad (14)$$

Where $R_{DS,n}$ and $R_{DS,p}$ indicates the channel resistance of NMOS and PMOS transistors respectively. Suppose the input

signal connected to the gate of NMOS transistor. Then the stage gain is altered as follows.

$$A_{stg} = g_{m,n} \frac{R_{DS,n} R_{DS,p}}{R_{DS,n} + R_{DS,p}} \quad (15)$$

Note that $g_{m,n} R_{DS,n}$ is the intrinsic gain of the input transistor M_n . Increasing the dc gain of a stage and improper sizing and biasing of the complementary transistors in the common source stage may cause imbalance in output resistance of complementary transistors $R_{DS,n}$ and $R_{DS,p}$. By providing balance to the network $R_{DS,n} = R_{DS,p}$, the stage gain becomes

$$A_{stg} = \frac{g_m}{2} \quad (16)$$

i.e., half of the intrinsic gain of the input transistor. Hence, for the initial sizing, the intrinsic gain of the input transistor must be twice of the stage gain. It is noted that the channel length of the transistor can alter the intrinsic gain of the transistor.

By holding all the above discussions and by noting that the biasing currents I_D of the complementary transistors in the same column are equal. The following gain equation holds good.

$$A_{Mp} = A_{Mn} \frac{\frac{g_m}{id_p}}{\frac{g_m}{id_n}} \quad (17)$$

V. PROPOSED METHODOLOGY

A. Sizing steps of single stage operational amplifier using gm/ID methodology

The single stage operational amplifier comprises a CMOS differential stage. The sizing of the amplifier is done based on the gm/ID method and the performance specifications. The proposed methodology, when compared to [1], allows for reduced transistor sizes, enabling the achievement of specifications while effectively decreasing transistor dimensions.

Step1 The current through the symmetric transistors $I_{M1,2}$ and $I_{M3,4}$ is $10 \mu\text{A}$ as per the performance specifications in [1], $I_b=10\mu\text{A}$ and I_{m0} is $20 \mu\text{A}$.

Step2 From the given Gain Bandwidth product, the transconductance of transistors M_1 and M_2 are calculated as $15.7 \mu\text{s}$

$$GBW = \frac{g_{m1,2}}{C_L} \quad (18)$$

Step3 The gm/ID of transistors M_1 and M_2 are calculated from the transconductance of transistors M_1 and M_2 and the current through the symmetric transistors as 15.7 S/A .

$$\left(\frac{g_m}{I_D}\right)_{1,2} = \frac{g_m}{I_{M1}} \quad (19)$$

Step4 The width of the transistors M_1 and M_2 is derived from the intrinsic gain, gm/ID of M_1 and M_2 and the current through the symmetric transistors $I_{M1,2}$. The length of transistors M_1 and M_2 is calculated from the gm/ID lookup table. The intrinsic gain of the transistors is given by the below equation.

$$A_{M1,2} = 2 * gain_{stg} = 80 = 38dB \quad (20)$$

Step5 The minimum gm/ID of transistors M_3 , M_4 which are matched transistors and the transistor M_0 is calculated using the ICMR value given in the performance specification and also from the minimum value of the L dependent curves. The value of $(gm/ID)_{3,4,min}$ is obtained as 8.7 S/A and $(gm/ID)_{0,min}$ is obtained as 9.05 S/A .

Step6 The maximum gm/ID value of transistors M_3 and M_4 is determined from the noise factor equation. The $(gm/ID)_{3,4,max}$ is obtained as 19.3 S/A .

$$\left(\frac{g_m}{I_D}\right)_{ratio} = \frac{s_n(f) * \frac{gmN}{4kT} - Vn}{Vp} \quad (21)$$

$$\left(\frac{g_m}{I_D}\right)_{3,4max} = \left(\frac{g_m}{I_D}\right)_{ratio} * \left(\frac{g_m}{I_D}\right)_{1,2max}^2 \quad (22)$$

$$Vn = Vp = \frac{1}{3} \quad (23)$$

Step7 From the Common mode gain equation, an upper bound of $(gm/ID)_0$ value is obtained. The intrinsic gain A_{M0} is taken as 100 from the feasible values of gain curves and common mode gain is precalculated. The slope is calculated which gives the value of $A_{cm,max} A_{M0}$ as 1.26.

$$\left(\frac{g_m}{I_D}\right)_0 = (A_{cm,max} A_{M0}) * \left(\frac{g_m}{I_D}\right)_{3,4} \quad (24)$$

Step8 From the constraint region $((gm/ID)_{3,4}, (gm/ID)_0)$, a sample value of $(12 \text{ S/A}, 12 \text{ S/A})$ is chosen. The intrinsic gain of transistors M_3 and M_4 is obtained from the gm/ID value of M_3 and M_4 and the gm/ID value of M_1 and M_2 using the equation,

$$AM_p = \frac{gm/ID_p}{gm/ID_n} AM_n \quad (25)$$

Step9 The widths of the transistors M_3 and M_4 are determined from the intrinsic gain of transistors M_3 and M_4 , the gm/ID values of M_3 and M_4 and the symmetric currents $I_{M3,4}$. The length of the transistors M_3 and M_4 is determined from the gm/ID lookup table.

Step10 The sizing of the transistor M_0 is determined using the intrinsic gain $A_{M0} = 100$, current I_{M0} and the gm/ID value of transistor M_0 to calculate the width and L_0 is calculated from the gm/ID lookup table.

Step11 The transistor M_b is sized with the help of current proportionality rule to determine the width where $W_b = \frac{1}{2} W_0$ and the length is same as that of M_0 transistor.

The Specifications of Single Stage Opamp is shown in the Table I. The final sizing result is listed in Table II.

TABLE I
DESIGN SPECIFICATIONS

Design Parameters	Required FOM	
	Single stage opamp	Two stage opamp
Differential Gain	32dB	80dB
Common Mode Gain	-38dB	10dB
CMRR	70dB	70dB
Gain Bandwidth	5MHz	10MHz
Capacitive Load	5pF	5pF
Bias Current	10 uA	20 uA
Slew Rate	4V/us	10V/us
Phase Margin	70deg	60deg
Input Referred Noise (nV/ $\sqrt{\text{Hz}}$)	17.7	17.7

TABLE II
INITIAL SIZING RESULTS OF SINGLE STAGE OPAMP

Width	Design value from [1]	Design value from our proposed method	Length	Design Value from our Proposed method	Design Value from [1]
W1,W2	7.7 um	1.98um	L1,L2	800nm	270nm
W3,W4	7.5 um	1.876um	L3,L4	400nm	270nm
Wb	7.1 um	1.059um	Lb	2um	360nm
W0	14.3 um	2.118um	L0	2um	360nm

B. Sizing steps of two stage operational amplifier using gm/ID methodology

Step1 Provide the necessary stage currents to the circuit as listed in the Table II, i.e., $I_{M0} = 20 \mu\text{A}$ and $I_{MS} = 60\mu\text{A}$ respectively. This step should be based on design requirements and technology availability.

Step2 Divide the total gain 80dB into two stages. The gain can be split evenly or unevenly. Here we split the gain as $\text{Astg1} = 38\text{dB}$ and $\text{Astg2} = 42\text{dB}$.

Step3 Using the gain bandwidth equation $GBW = gm_1 \cdot 2/C_C$, which is mainly useful for gm/ID calculation, we use (2) to find the feasible range of Capacitance C_C , i.e., $C_C \in [0, 5.7] \text{ pF}$ for $gm/ID \in [2, 24] \text{ S/A}$. Hence choosing $C_C = 2\text{pF}$ for the $(gm/ID)_{1,2} = 8.4 \text{ S/A}$.

Step4 Let $AM_{1,2} = 2 * \text{Astg1} = 44\text{dB}$. Remaining steps are same as the design of differential input stage of single stage Op Amp. Hence, go through the sizing steps of design of single stage Op Amp. Choose a higher value of transconductance (gm/ID)_{3,4} as 15 S/A in Step 8 of design of differential input stage of single stage op amp. This helps in achieving higher slew rate.

Step5 Using the equation of second dominant pole.

$$\rho_2 = \frac{g_{m6}}{2\pi C_L} \quad (26)$$

Where g_{m6} is the transconductance of M_6 . We simply ignored the output parasitic capacitance of the first

TABLE III
INITIAL SIZING RESULTS OF TWO STAGE OPAMP

Width	Design value from [1]	Design value from our proposed method	Length	Design Value from [1]	Design Value from our Proposed method
W1,W2	7.7 um	27.5um	L1,L2	2um	2.04nm
W3,W4	7.5 um	6um	L3,L4	400nm	2.5um
W5	42.6 um	9.5um	L5	2um	2.76um
W6	32.2 um	7um	L6	800nm	2.4um
W0,Wb	14.2 um	10um	L0,Lb	2um	2.4um

stage in second dominant pole equation. We also choose $\chi(\text{separationfactor}) = 2$ in order to get $gm/ID_6 = \chi * 2\pi * GBW/ID_6 = 10.4 \text{ S/A}$. By using the lookup table and with $(ID_6, gm/ID_6, AM_6)$ we can choose W_6 and L_6 .

Step6 Apply the gm/ID rule to the biasing current mirror by setting $gm/ID_5 = gm/ID_0$ for the load transistor M_5 of the second stage.

Upon using the equation $AM_p = \frac{gm/ID_p}{gm/ID_n} AM_n$ to calculate AM_5 . By using $(IM_5, gm/ID_5, AM_5)$ we can determine W_5 and L_5 using gm/ID lookup table.

Since most of the equations used here use a lot of approximate calculations, the design of two stage Op Amp so sized would not immediately give rise to good dc gain characteristics that meets the design specification. Especially, the biasing done for the second stage might not result in perfect balancing. Hence, we have to run an ac sweep test.

The Specifications of Two Stage Opamp is shown in the Table I. The final sizing result is listed in Table III.

VI. RESULTS AND DISCUSSION

A. Simulation results of single stage operational amplifier

Based on the initial sizing of single stage operational amplifier using gm/ID methodology, the results are further validated with Cadence Virtuoso as shown in the Table V and found that all the simulated results are approximately matched with given FOM.

B. Simulation results of two stage operational amplifier

Based on the initial sizing of two stage operational amplifier using gm/ID methodology, the simulated dc gain is 88.73 dB higher than 80dB and the GBW has 13 MHZ both exceeds the target but results in reduced common mode gain. The design may use further optimization procedure either manually or using CAD optimization tool. The Simulated results of two stage operational amplifier are shown from Figure 3 to Figure 5 respectively. Compared to the work in [1], the proposed methodology demonstrates superior performance in terms of achieving higher differential mode gain and CMRR. This makes the two-stage operational amplifier well-suited for applications that require high differential gain and CMRR capabilities.

TABLE IV
COMPARISON OF SIMULATED RESULTS OF SINGLE STAGE OPAMP WITH
REFERENCE PAPER [1].

Design Parameters	Required FOM Design	Simulated Results from [1]	Simulated Results from our proposed Method
Differential Gain	32dB	38dB	38dB
Common Mode Gain	-38dB	-23dB	-46.06dB
CMRR	70dB	61dB	76.98dB
Gain Bandwidth	5MHz	5.02MHz	5.12MHz
Slew Rate	4V/us	4.46V/us	4.41V/us
Phase Margin	70deg	90deg	88.89deg
Input Referred noise (nV/ \sqrt{Hz})	17.7	29.5	9.82
THD	-	-	1.06 %
PSRR	-	-	87 dB

TABLE V
COMPARISON OF SIMULATED RESULTS OF TWO STAGE OPAMP WITH [1].

Design Parameters	Required FOM Design	Simulated Results from [1]	Simulated Results from our proposed Method
Differential Gain	80dB	72.8dB	89.7dB
Common Mode Gain	1uV/B	-9dB	-9.4dB
CMRR	70dB	81.8dB	99dB
Gain Bandwidth	10MHz	16.3MHz	13.89MHz
Slew Rate	10V/us	11.9(V/us)	11.4(V/us)
Phase Margin	60deg	47deg	78.1deg
Input Referred noise (nV/ \sqrt{Hz})	17.7	37.9	14.54
THD	-	-	1.93 %
PSRR	-	-	105 dB

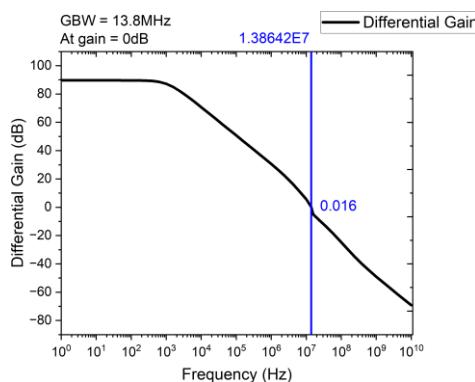


Fig. 3. Differential Mode Gain of Two Stage Opamp

VII. CONCLUSION

The gm/ID methodology is applied to a single stage and a two stage operational amplifier. The results are verified using Cadence Virtuoso and the technology node used is GPDK 180 nm technology. For a single stage operational amplifier, the Common Mode Rejection Ratio achieved is 76.98 dB, compared to the existing work in the literature.

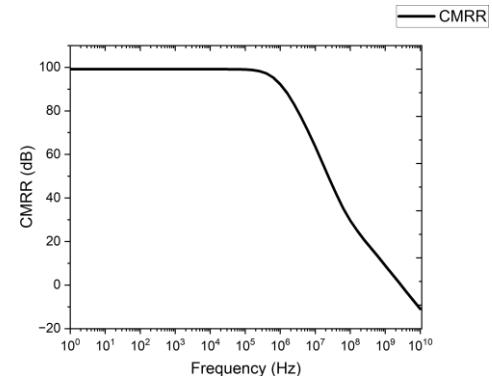


Fig. 4. Common Mode Rejection Ratio of Two Stage Opamp

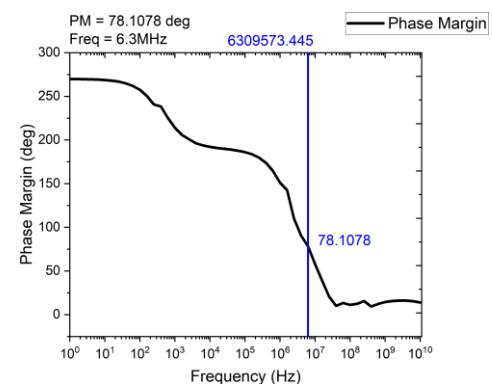


Fig. 5. Phase Margin of Two Stage Opamp.png

The Figure of Merits such as differential gain, common mode gain, Gain Bandwidth Product, Slew Rate and Phase Margin are also considered as metrics and the results are analyzed in comparison with the existing work. With respect to two stage operational amplifier, a high differential gain of 89.7 dB is achieved. The Common Mode Rejection Ratio is improved to 99 dB. The widths and lengths of the transistors are designed to meet the required specifications. The usage of design equations to achieve the gm/ID constraints and the application of gm/ID lookup tables result in an efficient design satisfying the Figure of Merits. The proposed methodology can be extended for other topologies and also for multi stages with the consideration of suitable design equations and gm/ID lookup tables.

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