

8-BIT FLOATING POINT DIVIDER

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Objective :

Two floating point numbers to be divided are given as inputs in IEEE 754 format. Division is done and delivered out in IEEE 754 format.

Abstract Idea :

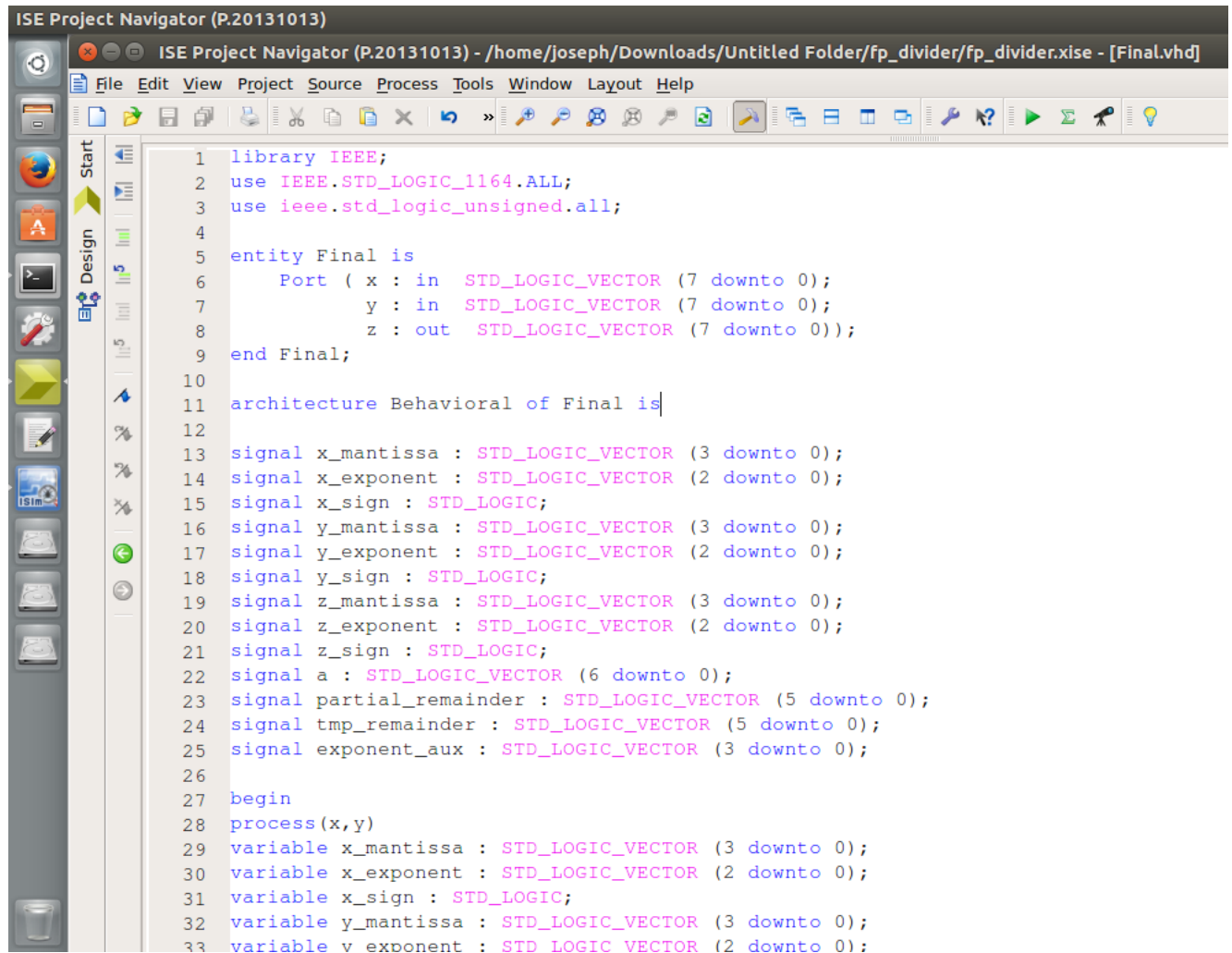
For giving an input in IEEE format refer the below chart. The division is done using iterative method.

Chart for Converting Binary to 8-bit IEEE 754 :

			S	E1	E2	E3	F3	F2	F1	F0									
EXPONENT			C15	C14	C13	C12	C11	C10	C9	C8	.	C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	0	0	0	0	0	0	0	0		0	0	F3	F2	F1	F0	0	0
0	0	1	0	0	0	0	0	0	0	0		0	1	F3	F2	F1	F0	0	0
0	1	0	0	0	0	0	0	0	0	0		1	F3	F2	F1	F0	0	0	0
0	1	1	0	0	0	0	0	0	0	1		F3	F2	F1	F0	0	0	0	0
1	0	0	0	0	0	0	0	1	F3			F2	F1	F0	0	0	0	0	0
1	0	1	0	0	0	0	1	F3	F2			F1	F0	0	0	0	0	0	0
1	1	0	0	0	1	F3	F2	F1				F0	0	0	0	0	0	0	0
1	1	0	0	1	F3	F2	F1	F0				0	0	0	0	0	0	0	0

Figure 1: (S1 E1 E2 E3 F3 F2 F1 F0) is in IEEE format

VHDL Code :

The image is a screenshot of the ISE Project Navigator software interface. The title bar reads "ISE Project Navigator (P.20131013)". The menu bar includes "File", "Edit", "View", "Project", "Source", "Process", "Tools", "Window", "Layout", and "Help". The toolbar contains various icons for file operations, editing, and simulation. On the left, there is a "Start" button and a "Design" pane showing a project hierarchy. The main window displays a VHDL file named "Final.vhd". The code defines an entity "Final" with two input ports "x" and "y" of type "STD_LOGIC_VECTOR (7 downto 0)" and one output port "z" of type "STD_LOGIC_VECTOR (7 downto 0)". The architecture "Behavioral of Final" contains several signal declarations for mantissa, exponent, and sign components of x, y, and z, as well as intermediate signals "a", "partial_remainder", "tmp_remainder", and "exponent_aux". A "begin" block starts with a "process(x,y)" and declares several variables for the same components as the signals.

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use ieee.std_logic_unsigned.all;
4
5 entity Final is
6     Port ( x : in  STD_LOGIC_VECTOR (7 downto 0);
7           y : in  STD_LOGIC_VECTOR (7 downto 0);
8           z : out STD_LOGIC_VECTOR (7 downto 0));
9 end Final;
10
11 architecture Behavioral of Final is
12
13     signal x_mantissa : STD_LOGIC_VECTOR (3 downto 0);
14     signal x_exponent : STD_LOGIC_VECTOR (2 downto 0);
15     signal x_sign : STD_LOGIC;
16     signal y_mantissa : STD_LOGIC_VECTOR (3 downto 0);
17     signal y_exponent : STD_LOGIC_VECTOR (2 downto 0);
18     signal y_sign : STD_LOGIC;
19     signal z_mantissa : STD_LOGIC_VECTOR (3 downto 0);
20     signal z_exponent : STD_LOGIC_VECTOR (2 downto 0);
21     signal z_sign : STD_LOGIC;
22     signal a : STD_LOGIC_VECTOR (6 downto 0);
23     signal partial_remainder : STD_LOGIC_VECTOR (5 downto 0);
24     signal tmp_remainder : STD_LOGIC_VECTOR (5 downto 0);
25     signal exponent_aux : STD_LOGIC_VECTOR (3 downto 0);
26
27 begin
28     process(x,y)
29         variable x_mantissa : STD_LOGIC_VECTOR (3 downto 0);
30         variable x_exponent : STD_LOGIC_VECTOR (2 downto 0);
31         variable x_sign : STD_LOGIC;
32         variable y_mantissa : STD_LOGIC_VECTOR (3 downto 0);
33         variable y_exponent : STD_LOGIC_VECTOR (2 downto 0);
```

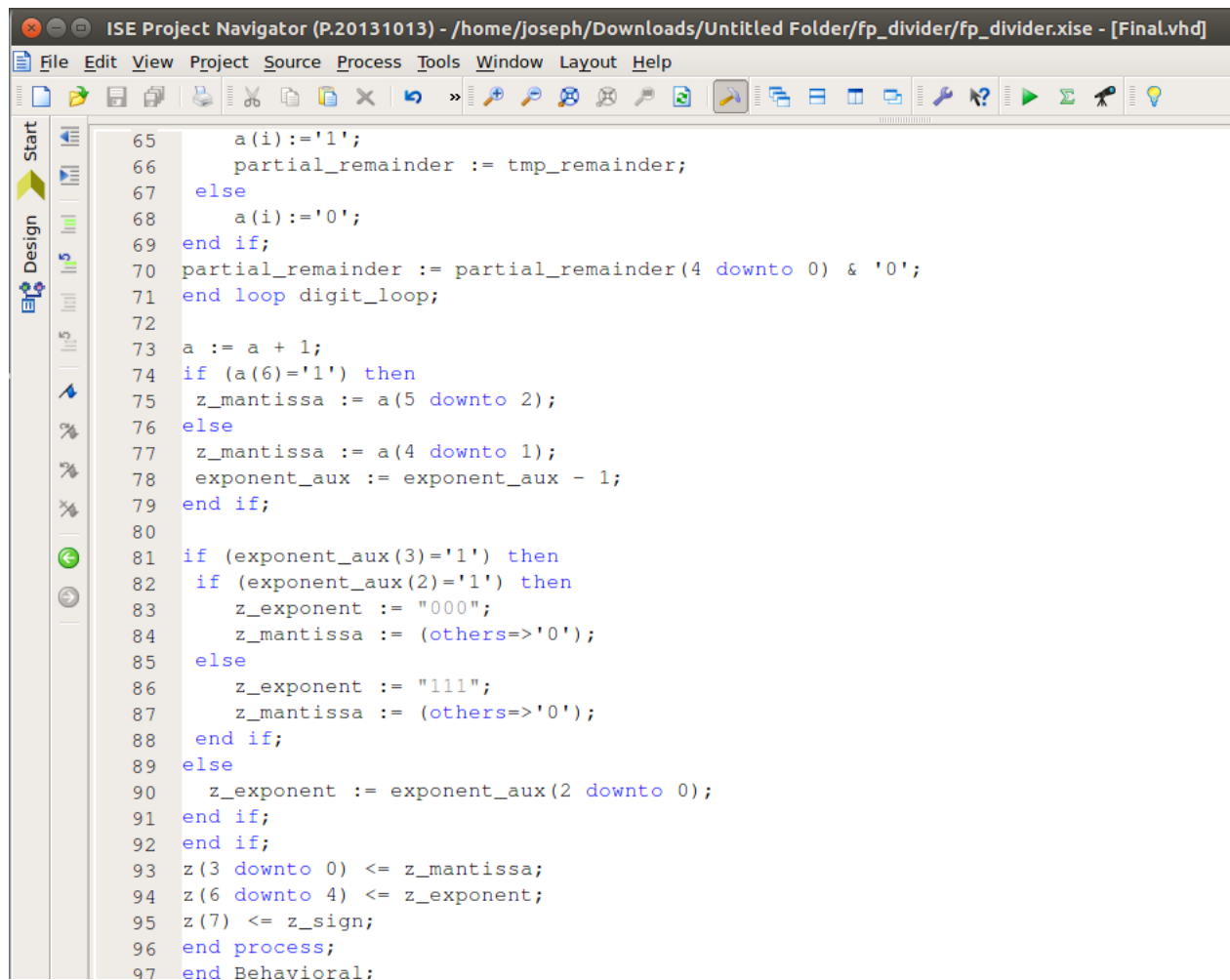
Figure 2: Initializing the inputs, outputs and intermediate signals

```

33 variable y_exponent : STD_LOGIC_VECTOR (2 downto 0);
34 variable y_sign : STD_LOGIC;
35 variable z_mantissa : STD_LOGIC_VECTOR (3 downto 0);
36 variable z_exponent : STD_LOGIC_VECTOR (2 downto 0);
37 variable z_sign : STD_LOGIC;
38 variable a : STD_LOGIC_VECTOR (6 downto 0);
39 variable partial_remainder : STD_LOGIC_VECTOR (5 downto 0);
40 variable tmp_remainder : STD_LOGIC_VECTOR (5 downto 0);
41 variable exponent_aux : STD_LOGIC_VECTOR (3 downto 0);
42
43 begin
44   x_mantissa := x(3 downto 0);
45   x_exponent := x(6 downto 4);
46   x_sign := x(7);
47   y_mantissa := y(3 downto 0);
48   y_exponent := y(6 downto 4);
49   y_sign := y(7);
50   z_sign := x_sign xor y_sign;
51
52   if (y_exponent="111") then
53     z_exponent := "000";
54     z_mantissa := (others=>'0');
55   elsif (y_exponent=0 or x_exponent=7) then
56     z_exponent := "111";
57     z_mantissa := (others=>'0');
58   else
59     exponent_aux := ('0' & x_exponent) - ('0' & y_exponent) + 3;
60     partial_remainder := "01" & x_mantissa;
61
62     digit_loop: for i in 6 downto 0 loop
63       tmp_remainder := partial_remainder - ("01" & y_mantissa);
64       if ( tmp_remainder(5)='0' ) then
65         a(i):='1';

```

Figure 3: Checking for special cases..



```
65     a(i):='1';
66     partial_remainder := tmp_remainder;
67   else
68     a(i):='0';
69   end if;
70   partial_remainder := partial_remainder(4 downto 0) & '0';
71 end loop digit_loop;
72
73 a := a + 1;
74 if (a(6)='1') then
75   z_mantissa := a(5 downto 2);
76 else
77   z_mantissa := a(4 downto 1);
78   exponent_aux := exponent_aux - 1;
79 end if;
80
81 if (exponent_aux(3)='1') then
82   if (exponent_aux(2)='1') then
83     z_exponent := "000";
84     z_mantissa := (others=>'0');
85   else
86     z_exponent := "111";
87     z_mantissa := (others=>'0');
88   end if;
89 else
90   z_exponent := exponent_aux(2 downto 0);
91 end if;
92 end if;
93 z(3 downto 0) <= z_mantissa;
94 z(6 downto 4) <= z_exponent;
95 z(7) <= z_sign;
96 end process;
97 end Behavioral;
```

Figure 4: Key lines of the code for Division...

Design Summary :

Start

Design

Run

Tools

Help

Project

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Process

Tools

Window

Layout

Help

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Figure 5: Final report of the design

Simulation Report :

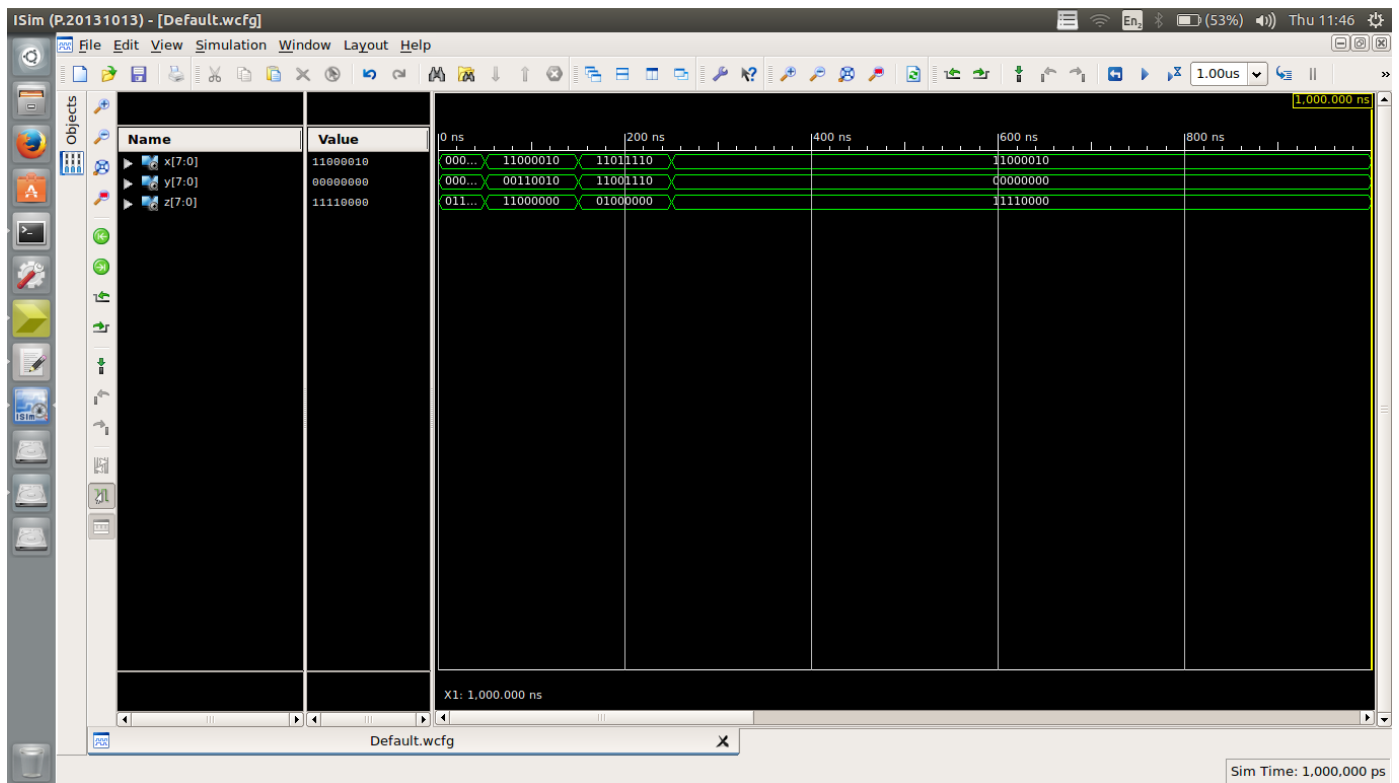


Figure 6: Sample inputs and outputs in signal form

References :

1 edaboard:

<http://www.edaboard.com/forum.php>

2 VHDLguru:

<http://vhdlguru.blogspot.in/>

3 WIKIPEDIA:

https://en.wikipedia.org/wiki/IEEE_floating_point

4 Others:

http://class.ece.iastate.edu/arun/CprE281_F05/ieee754/ie5.html