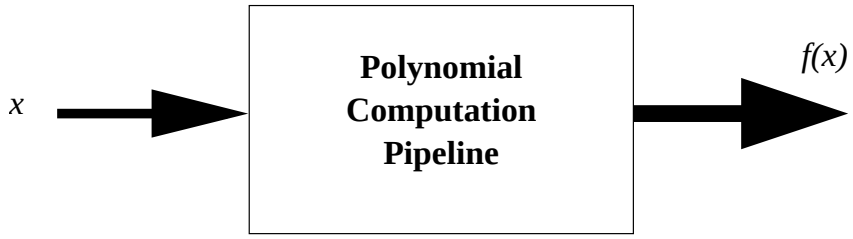
ECE 319 : Digital System Design : Fall 2015

Project IV : Due: Dec 4, 2015.

Design a pipeline processor that will compute a third degree polynomial

$$f(x) = a_3x^3 + a_2x^2 + a_1x + a_0.$$



The specifications of the system are as follows:

- The constants a_0, a_1 , a_2 and a_3 are 4 bit 2's complement numbers ($-7 \leq a_i \leq 7$). They are read into the system on reset.
- The pipeline is applied data at regular intervals. Each input data x is a 4 bit 2's complement number ($-7 \leq x \leq 7$).
- all calculations are done using 2's complement number system.
- The system can use only two *array multipliers* and one *carry propagation adder* of appropriate sizes.
- Under these hardware constraints, the pipeline should have optimum throughput.
- The input and output of the pipeline should be periodic.
- The pipeline should use minimum power.

To test the pipeline, write a test bench to read the data from a file "proj4.dat" and apply it to the pipeline at the right time. The output should come from an output register and should change only when new output is produced. Note that verilog requires that the x values in the file as well as the constants a_0, a_1 , a_2 and a_3 are decimal values of 4 bit binary strings to be used. For example, to apply -3 (which is 1101B in 4-bit 2's complement), one should place value 13 in the file since 13 is the value of the string 1101B.

Your system should have low hardware complexity and should consume as little power as possible.

Use the following templet for your system.

```
module PolyPipe(clock, reset, const3, const2, const1, const0, x, y);
input clock, reset;
input [3:0] const0, const1, const2, const3, x;
output [15:0] y;

reg [3:0] a0, a1, a2, a3;
always @(posedge reset)
  begin
    a0 <= const0;
    a1 <= const1;
    a2 <= const2;
    a3 <= const3;
  end

// rest of your code

endmodule
```

This module can be instantiated in the test bench as

```
module PolyPipe(clock, reset, 2, 13, 11, 0, x, y);
```

The instantiation shown above corresponds to the polynomial

$$2x^3 - 3x^2 - 5x.$$

Use different coefficients to check that you get correct results for all cases.

Submit a report on your design that includes at the minimum:

- Problem statement
- Design approach
- The complete design including datapath sketch and control description.
- verilog description of the design including a properly set-up test bench.
- Simulation result waveforms.
- Any additional design enhancements you might have used to improve the speed or to reduce power.

Name the verilog file proj4.v. Identify yourself clearly in the program header. Upload your files to the coursesite by 11:59 PM, Fri, December 4. Submit your report on Monday, Dec 7th before Noon to my office (PL 402A). Late penalty will be applied to submissions after the due date. Reports will not be accepted after the final exam.