5.8GHz Maximum Gain Amplifier

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***Abstract*—This paper explores and compares the design of two different 5.8 GHz maximum gain amplifiers. Each design aims to achieve maximum gain using different transistors, matching networks, and DC biases. The first design utilizes the NXP BFU725F with a lumped component design for the source and load matching networks as well as an inductor as an RF choke for the DC bias. The second design makes use of the NXP BFU730F with open circuit shunt stubs for the matching networks and quarter wave length transmission lines for the RF choke in the DC bias. Both are designed for fabrication on FR-4 due to cost efficiency. The simulations on Advanced Design Systems uses specifications in order to accurately simulate the substrate. These include the thickness of the substrate at 1.6 mm, the dielectric constant of 4.7, the conductivity of the copper at 5.8×10^7, the thickness of the copper at 35 μm and the dissipation factor, or $tan\delta$, at 0.0127. The two designs are compared and the better design is chosen for fabrication and testing. The BFU730F performed better in simulation, with 2.5 dB higher gain and 6 dB lower reflection, so the layout was simulated and fabricated professionally through PCBway. The fabricated board achieved a gain of 14.11 dB and a -12 dB reflection coefficient.**

I. Introduction

The design of microwave transistor amplifiers is the primary focus of this paper, emphasizing the configuration of an amplifier aimed to provide maximum gain according to the chosen transistor.

A. Stability

In order to begin the design of a quality transistor amplifier, the transistor chosen must have the necessary conditions for stability in the design frequency. Otherwise, it is possible for oscillations to occur when the input or output impedance of the transistor has a $|\Gamma_{in}| > 1$ and $|\Gamma_{out}| > 1$. Therefore, the amplifier is developed for a $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$. When both of these conditions are met, the amplifier can be one of two types of stability — unconditionally stable or conditionally stable [1]. Unconditional stability is met when $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all source impedances and load impedances; meaning $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$. Conditional stability occurs when instead the condition is met for specific values of the source and load impedances.

1) Unconditional Stability Test: The K-Δ test is a simple mathematical test used to show if a device is unconditionally stable or not using (1) and (2).

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{1}$$

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2}$$

Both conditions must be met for the device to be considered unconditionally stable. If either condition is not met, stability circles must be evaluated and drawn on the Smith chart to determine if the values of $|\Gamma_S|$ and $|\Gamma_L|$ are in the stable regions.

B. Maximum Gain

Once the stability of the transistor at the specified frequency has been found, Γ_L and Γ_S can be determined using the transistor's S-parameters. In order to obtain maximum gain, Γ_L must be conjugately matched to Γ_{out} and Γ_S must be conjugately matched to Γ_{in} [1]. Designing the matching networks in this fashion allows for less mismatch at the input and output of the transistor leading to the greatest possible gain. Γ_L and Γ_S can be found using (3) and (4).

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{3}$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{4}$$

The variables B_1, B_2, C_1, and C_2 can be obtained by (5), (6), (7), (8), and (9).

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{5}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{6}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{7}$$

$$C_1 = S_{11} - \Delta S_{22}^* \tag{8}$$

$$C_2 = S_{22} - \Delta S_{11}^* \tag{9}$$

If designing the matching network on the Smith chart, Γ_S and Γ_L must first be plotted and matched backwards to from the center point.

As the amplifier is designed to achieve maximum gain, $G_{T_{max}}$, must be calculated to understand what that value may be using (10). This gain estimation provides an understanding of what the simulated and fabricated amplifier should reach [1].

$$G_{T_{max}} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \tag{10}$$

II. Design with BFU725

Using the NXP BFU725 silicon germanium RF transistor, the first of two amplifier designs uses lumped component matching networks to achieve a maximum transducer gain of 17.7 dB, calculated using 10. Further this design uses an inductor for the RF choke in the DC bias of both the base and collector of the transistor.

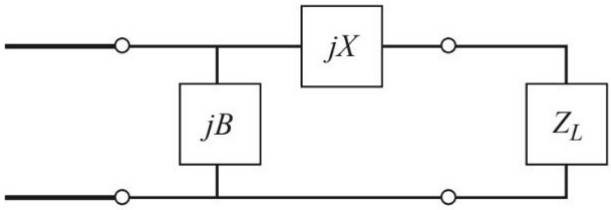

Fig. 1: L-Matching Network Topology

A. Stability and L-Matching Network

Before beginning the design of the matching networks and DC bias, the stability of the transistor at 5.8 GHz was determined using the transistor's S-parameter design file [3] with the values shown in Table I. Through the K-Δ test from (1) and (2), the transistor was found unconditionally stable with a K value of 1.0651 and a Δ value of 0.3871. The established maximum gain, G_{max}, is also found from (10) to be 17.7 dB.

TABLE I: S-Parameters of BFU725 at 5.8 GHz

S_{11}	S_{12}	S_{21}	S_{22}
0.4979∠150.81	0.0699∠29.46	5.949∠39.68	0.1221∠−139.16

Next, the Γ_S and Γ_L were calculated using (3) and (4) respectfully as well as their corresponding source and load impedance values Z_S and Z_L which are used for the L-matching network equations shown in (11) and (12).

$$X = \pm\sqrt{R_L(Z_0 - R_L)} - X_L \tag{11}$$

$$B = \pm\frac{\sqrt{(Z_0 - R_L)/R_L}}{Z_0} \tag{12}$$

These equations correspond to the topology in Fig. (1) which was determined as the correct topology since for both Z_S and Z_L the R_S and R_L values were less than the characteristic impedance of the transmission lines, 50 Ω.

Table II displays the values of the capacitor and inductor used in the source matching network along with the conjugate source impedance value used for (11) and (12). These values are rounding in the final design to a capacitance of 1 pF and inductance of 0.6 nH in order to depict values that can be attained from a manufacturer.

TABLE II: Source Matching Network Component Values

Z_S	$Z_{in} = Z_S^*$	C_S	L_S
7.5215-j10.6030	7.5215+j10.6030	0.946 pF	0.577 nH

Table III contains the values of the capacitor and inductor used in the load matching network as well as the conjugate load impedance values. Similarly, these values are also rounded to a capacitance of 0.6 pF and an inductance of 1.6 nH in order to be able to order them from the manufacturer.

TABLE III: Load Matching Network Component Values

Z_L	$Z_{out} = Z_L^*$	C_L	L_L
21.94 + j38.1137	21.94 - j38.1137	0.62 pF	1.73 nH

B. ADS Simulation

Following the design, the source and load matching networks are implemented in the simulation software Advanced Design Systems (ADS). Prior to the addition of any transmission or microstrip lines, the matching networks are simulated on ADS using the S-parameter file of the BFU725 transistor shown in Fig. 2. These networks on their own output a gain of 17.7 dB, accurately matching the calculated G_{max} value as depicted in Fig. 3 .

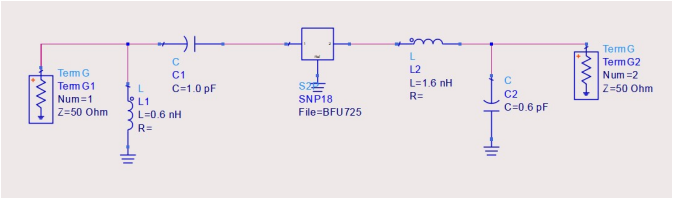

Fig. 2: Source and load impedance L-Matching networks at the input and output of the BFU725 S-parameter file.

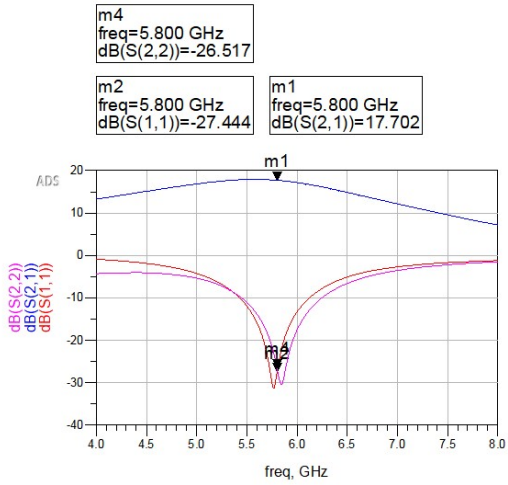

Fig. 3: Source and load impedance L-Matching networks at the input and output of the BFU725 S-parameter file.

Next, ideal transmission lines are included in the design for the solder pads of the transistor, capacitors, inductors, and the SMA connector which is shown in Fig. 4. As displayed in Fig. 5, the gain obtained after the addition of the transmissions lines is 14.6 dB. Along with the transmission lines, the DC bias is added and a transistor spice model is used to verify the input and output currents required to bias the transistor [3]. The BFU725 S-parameter file indicates a base voltage of 0.85 V with the corresponding 93 mA current and a collector voltage of 2 V with a 25 mA current in order to bias the transistor correctly. In order to control the currents into the transistor, resistors were implemented so that during testing small errors of voltage would not affect the transistor. The RF

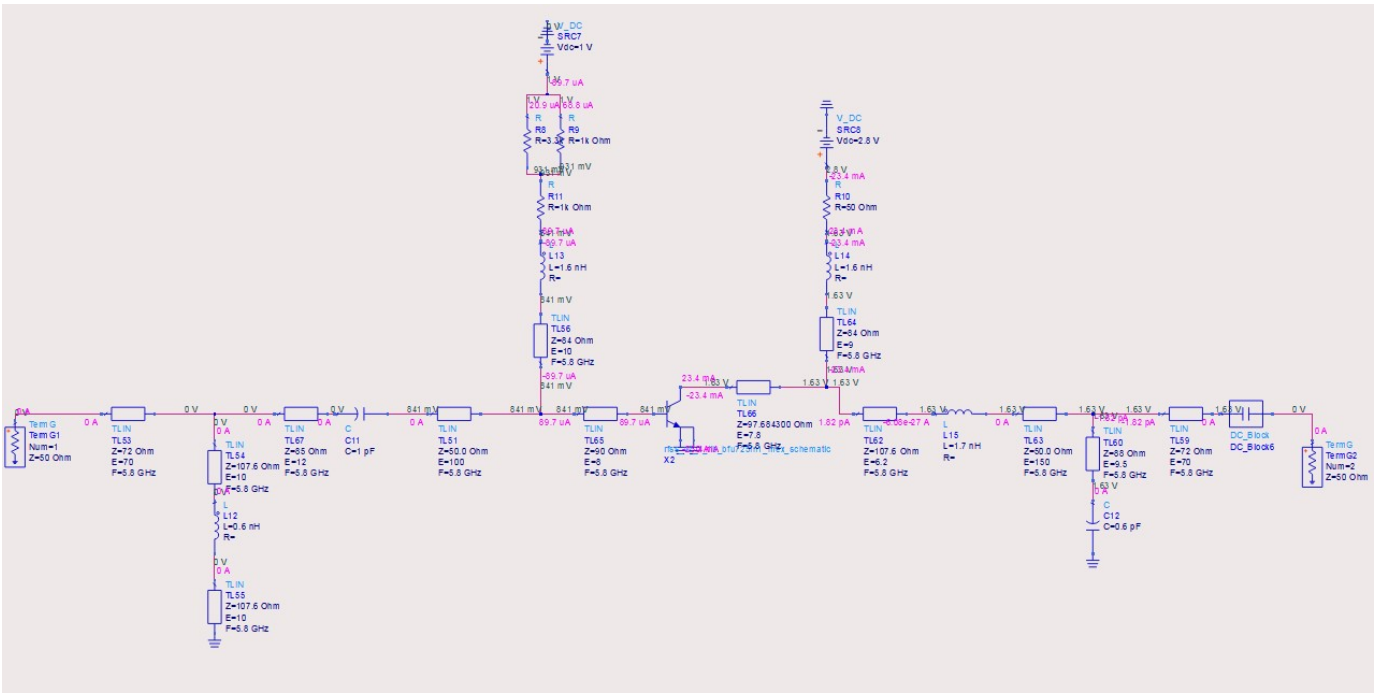

Fig. 4: Source and load impedance L-Matching networks at the input and output of the BFU725 S-parameter file.

choke consists of one inductor with a value of 1.6 nH for each DC bias which resulted in an effective block for the RF.

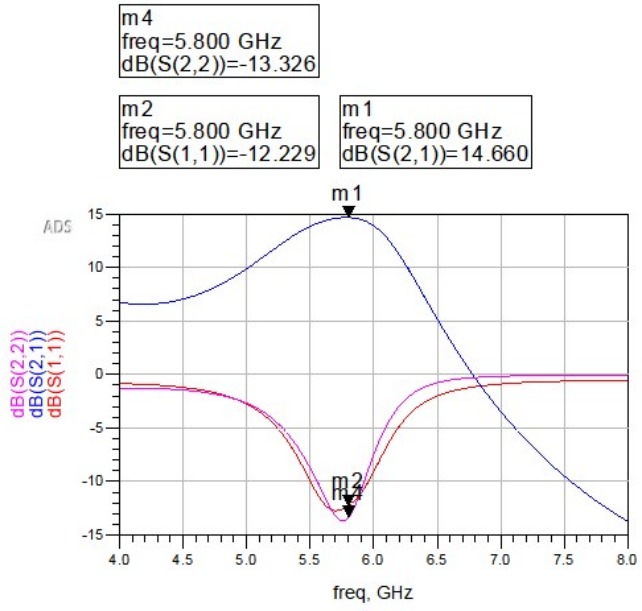

Fig. 5: S-parameters of the simulation depicting a gain of 17.7 dB.

The addition of the ideal transmission lines for the solder pads drastically influences the impedance seen at the input and the outputs. To diminish these affects which would greatly attenuate S_{21} due to a mismatch from the added transmission lines, half wave length 50 Ω lines were included and the values manipulated until the optimal gain was shifted back to the desired frequency.

To further the design, the ideal transmission lines were switched to microstrip lines called MLINs in ADS and displayed in Fig. 7. Using the LineCalc tool, the widths and lengths were determined for each line from the electrical length and characteristic impedance. This final version produced an accurate simulation of the complete amplifier with a final maximum gain of 14.7 dB at 5.8 GHz shown in Fig. 6.

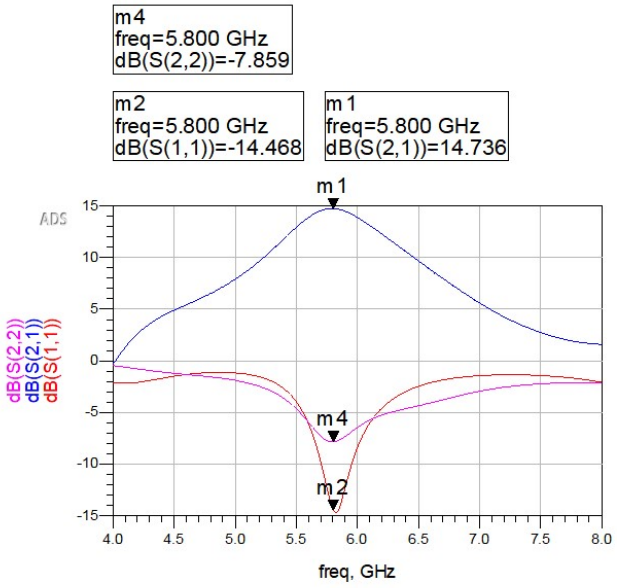

Fig. 6: S-parameters of the maximum gain amplifier with microstrip lines.

C. PCB Layout

Once the design was complete, the amplifier PCB layout is created on ADS as well and depicted in Fig. 8. The PCB consists of three main layers: the first conductor layer, the hole layer for the vias, and the bottom ground conductor layer. Drawing the layout involved using the microstrip line widths and lengths for each trace and leaving the appropriate amount of space between the solder pads of each component. The spacing was determined from the datasheets of each capacitor and inductor models. The trace in the DC bias led to two large pads on which two wires will be soldered and connected to a DC supply. The vias were then drawn on the hole layer to provide a connection to through the substrate to the bottom ground layer. Finally, the second conductor layer is drawn to complete the layers. To prepare the board completely for fabrication, PCBway requires an additional board boundary as well to clearly indicate where the board begins and ends.

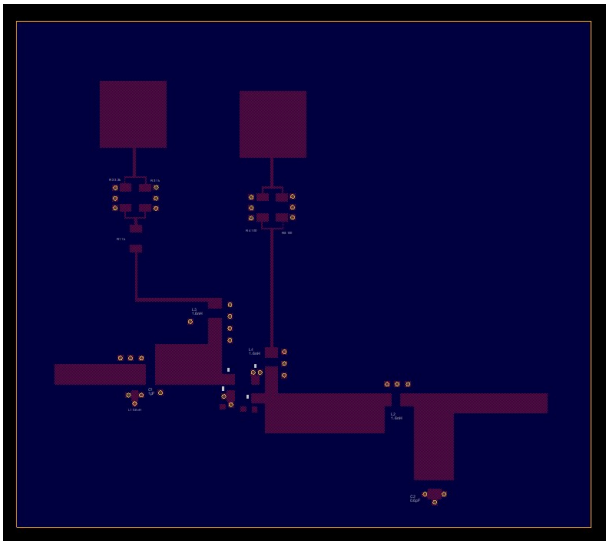

Fig. 8: Maximum Gain Amplifier PCB Layout.

III. Design BFU730

The second amplifier design uses the NXP BFU730F which is a NPN silicon germanium RF transistor. The transistor is biased at 2.5 V and 25 mA [4]. The matching networks and the DC bias RF chokes were designed using open circuit shunt stubs. Before the amplifier was designed, stability was determined at the design frequency 5.8 GHz using the S-parameters of the transistor.

TABLE IV: S-Parameters at 5.8 GHz

S_{11}	S_{12}	S_{21}	S_{22}
$0.422\angle 159.89$	$0.0605\angle 43.83$	$6.699\angle 51.71$	$0.203\angle -66.14$

A. Stability and Matching Network

Using (1) and (2) and Table IV, K is calculated to a value of 1.0876 and Δ to a value of 0.3197 showing that the transistor is unconditionally stable at the desired frequency. Since stability is established, Γ_S and Γ_L was then used to establish the matching networks for the amplifier. Using (3) and (4), Γ_S and Γ_L are found to be $0.7056\angle -160$ and $0.06111\angle 65$ respectively. Once plotted on the Smith chart, the matching networks were designed with respect to λ, the wavelength of the line. The maximum gain achievable with this transistor is found using (10) to be 18.635 dB.

B. ADS Simulation

In ADS, TLIN's are used in order to test the matching networks using ideal transmission lines. These transmission lines typically depict peak performance and degrade once realistic microstrip lines are implemented. The following ideal model was implemented on ADS.

The DC blocks in Fig. 9 are placed for the ADS simulation since DC blocks are attached on the input in output to protect the equipment during testing.

In ADS, λ is 360° so the numbers obtained from the Smith chart are then multiplied by 360 in order to get the correct electrical length in ADS. For the input matching network, the

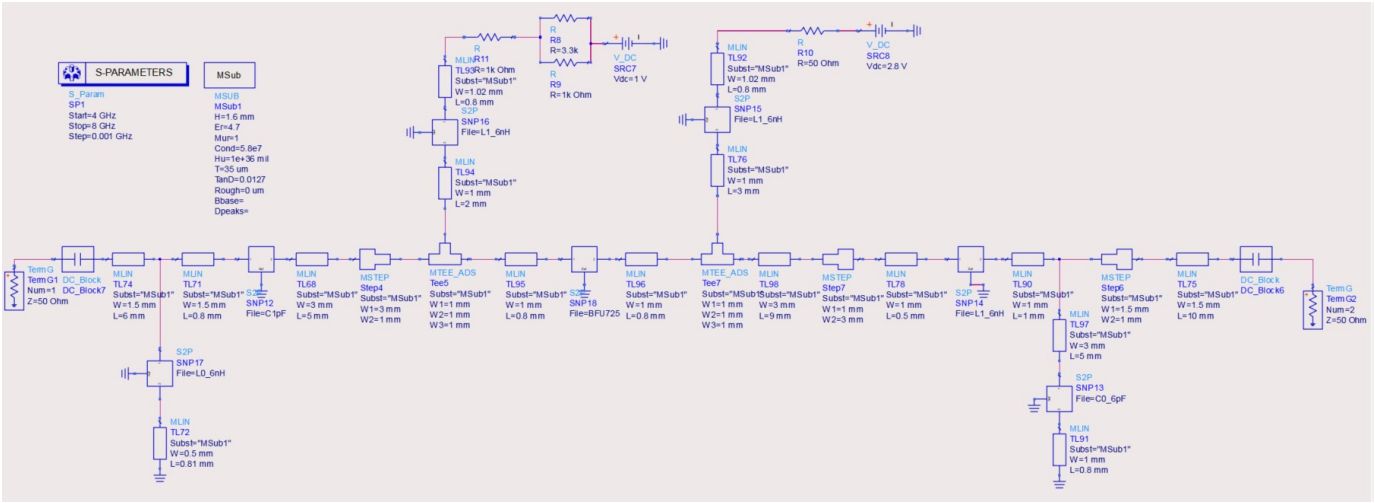

Fig. 7: Maximum gain amplifier utilizing microstrip lines.

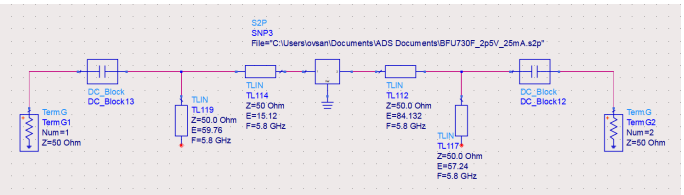

Fig. 9: Schematic made in ADS using TLINs.

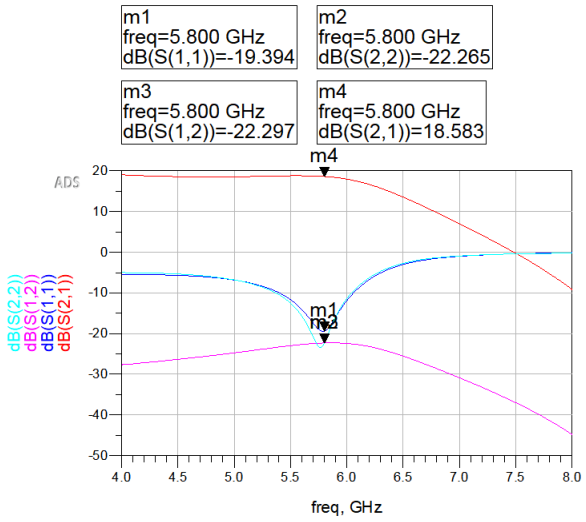

Fig. 10: Schematic made in ADS using TLINs.

open circuit stub is 0.166λ and the series transmission line is 0.042λ. For the output matching network, the open circuit stub is 0.159λ and the series transmission line is 0.2337λ. Those values are then converted to electrical lengths and used for the TLIN values shown in Fig. 9.

The results a clear corrolation with the simulation and the calculated values, as seen in Fig. 10, since they are similar. The calculated maximum gain was 18.635 dB and the simulated maximum gain was 18.583 dB which is nearly identical. Further, the return loss was low for the input and output which was aimed to be as minimum as possible to become more accurate to actual fabrication.

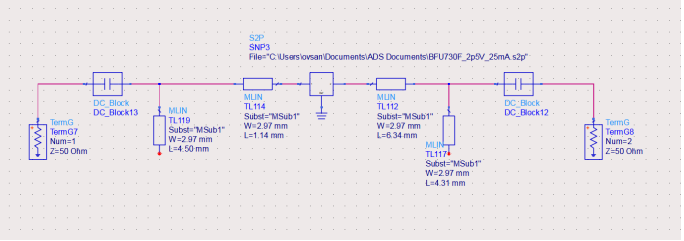

Fig. 11: Schematic in ADS with MLINs instead of TLINs.

In order to transition to microstip lines, called MLINs in ADS, which are more accurate models of transmission lines that take into account of the substrate being used. The tool used to transition from TLINs to MLINs is called LineCalc which is integrated into ADS and allows us to see the specific

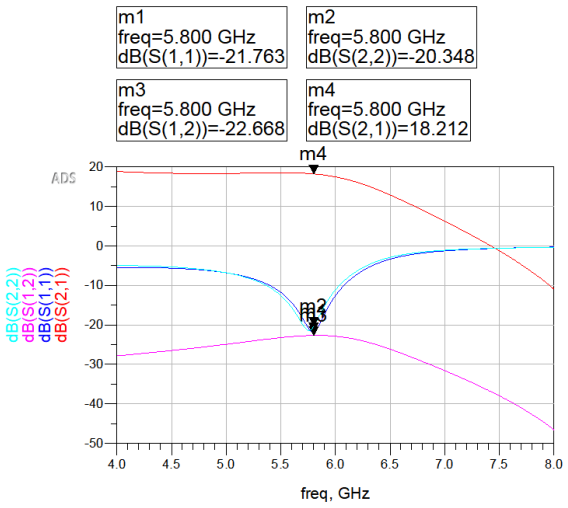

Fig. 12: S-parameter results from MLIN simulation.

width and length the transmission line needs to be in order to match the electrical length the TLINs used. Those values can be seen in the schematic as shown in Fig. 11. The widths are all the same at 2.97586 mm since that gives all the lines a 50 Ω impedance which keeps everything at a standard impedance. The lengths will fluctuate depending on the electrical length needed to conjugately match the transistor. Some of the lengths have been shifted by ± 0.8 dB in order to combat shifts in frequency. Additionally, the gain did decrease as seen in Fig. 12. This is due to the substrate being taken into account and since the design was fabricated using FR-4, which is a lossy board at high frequency, those losses in gain are expected.

Next, aspects of the design were changed to include microstrip lines that would make the simulation as close to fabrication as possible. SMA connectors are needed to be soldered on the input and output. The width of the current lines are too wide, so a taper was used at the input and output to a line with 1.5 mm width and a length of 5 mm. A cross section was added to connect the open circuit stub and the DC biasing to the rest of the amplifier. This accounts for the cross section effects in the simulation but it does have an inherent length so approximately 0.5 mm length is cut from everything the cross section is connected to. Finally, a step must be made for transistor footprint. The footprint of this transistor is 0.675 mm wide which is significantly smaller than the width of transmission line. A taper was also used here originally but it caused significant mismatches so instead a step was used and found to be more successful.

A quarter wavelength open circuit stub was used as an RF choke in order to ensure the RF signal will not interfere with the DC signal. This works since the RF signal will see the quarter wavelength open circuit stub as short and short into the stub while the DC will see it as an open and ignore the stub entirely. This is perfect for the design since it removes the complication of using lumped components to choke the RF signal. Resistors were used to reduce the sensitivity the

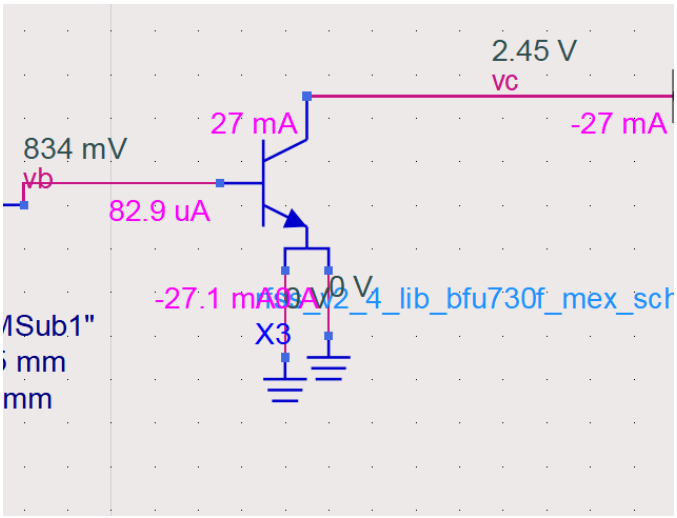

Fig. 13: Implementation of the SPICE model.

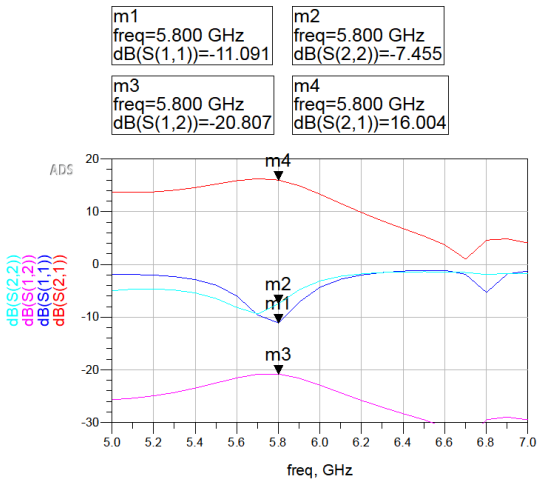

Fig. 14: SPICE model S-parameters.

amplifier has to changes in the DC source. This alleviates a layer of human error with the DC source since it doesn't need to be extremely accurate since small changes don't impact the voltages and currents at the collector and base. A 50 Ω resistor was used for the collector and a 2000 Ω resistor used for the base. The DC source at the base was set to 1 V which gives the 0.834 V and 0.00829 mA needed at the base. The collector DC source was set to 3.8 V which gives the 2.45 V and 27 mA needed for this design as shown in Fig. 13. The DC bias was simulated using a spice model, which isn't as accurate as the S2P file used for the rest of the simulations but since the S2P file ignores DC biasing, the spice model was used to show the currents and voltages measured at each node. This is shown in Fig.14, where the gain and return loss is not as accurate but it shows that there is decent gain at the specified design frequency.

The final schematic can be seen in Fig. 16 along with the

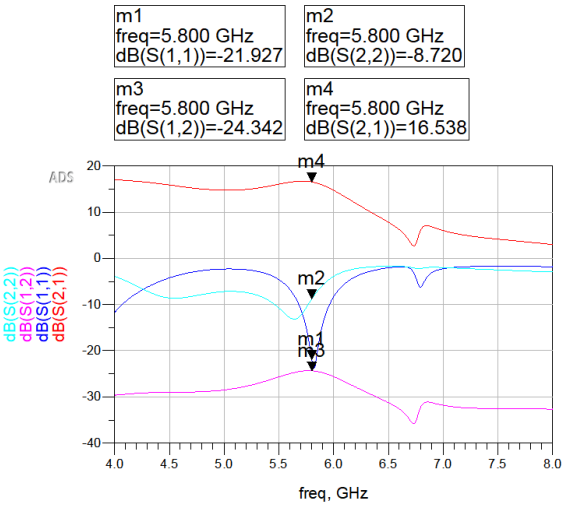

Fig. 15: S-parameter output of the amplifier with microstrip lines.

results in Fig. 15. The final gain is simulated at 16.5 dB with a reflection coefficient of -10 dB. The only concern is the reflection at the output is a bit high but not high enough to warrant a change in design. The losses of gain are potentially due to the tapers and steps used on the FR-4 substrate which is an already lossy board.

C. PCB Layout

The final step in designing the amplifier is generating a layout to get the Gerber files to send to a professional manufacturer. ADS has auto-generation and will generate the parts in the schematic onto the layout. While that doesn't include everything, it does include most of the traces that would be needed for the design. The footprint for the resistors and the transistor must be created manually, but this did not present as much of an issue as the rectangle tool was used and the widths and lengths of the rectangle are as specified by the supplier for the components. Larger DC pads are created where the DC sources are located on the schematic, which allows a wire to be soldered to connect the DC supply. Since the RF choke is blocking all RF signals going through this part of the board, transmission line effects can be ignored, so the resistors and extra traces used here do not affect the RF signal at all.

Vias are also created on the two emitter pins on the transistor which can be seen in Fig. 17. A second conductive layer on the bottom of the board and a board border have also been created as another layer. The vias were given the hole layer, and the design is complete. There is also the purple bottom copper layer that covers the entire bottom of the bottom of the PCB. Finally a white bound boarder is placed for the boundaries and the layout is complete.

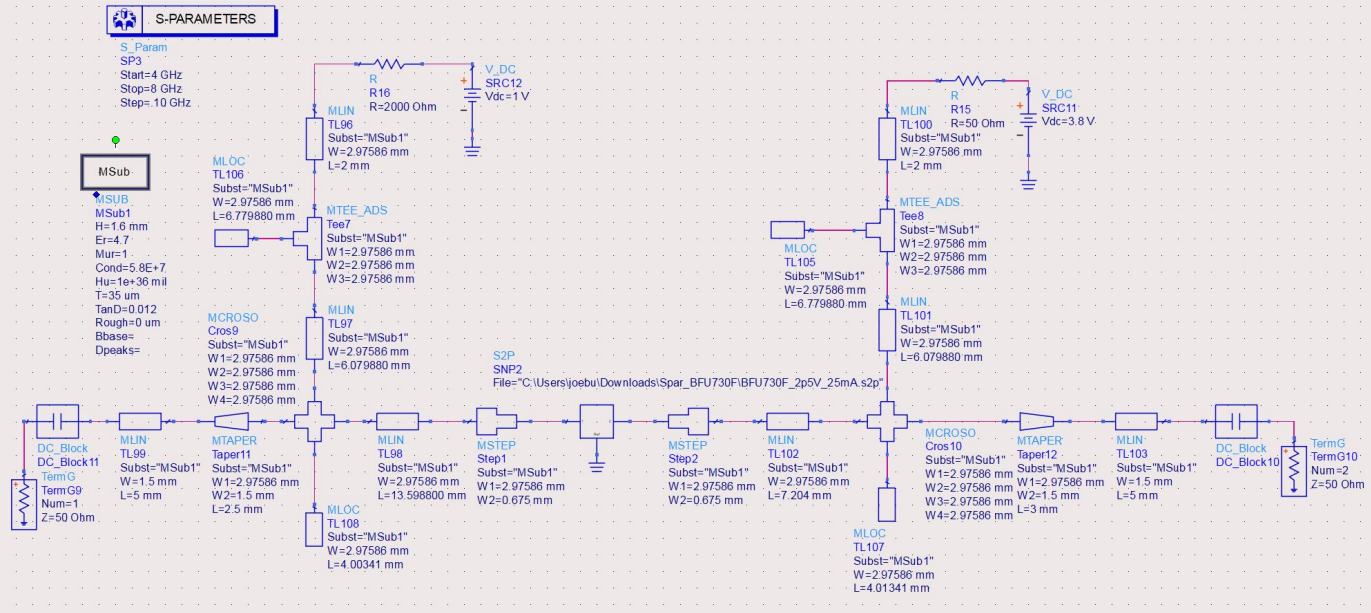

Fig. 16: This is the schematic that is used in the final design for the BFU730F

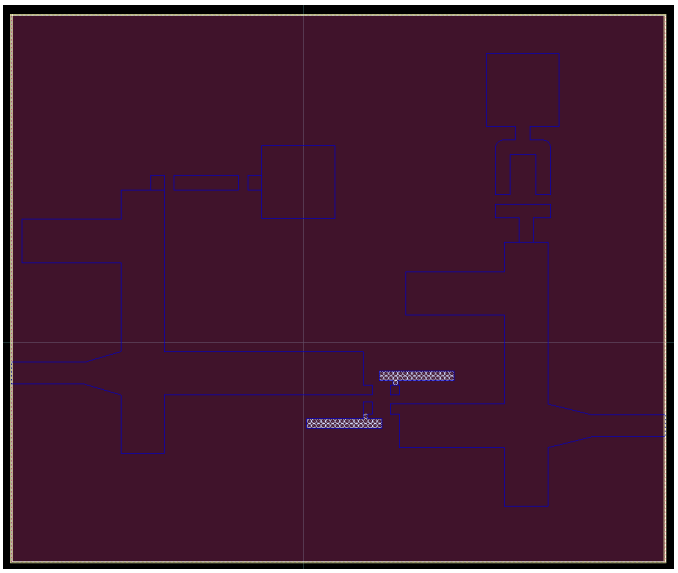

Fig. 17: PCB layout of the amplifier with blue lines as the top copper later and white circles as the vias.

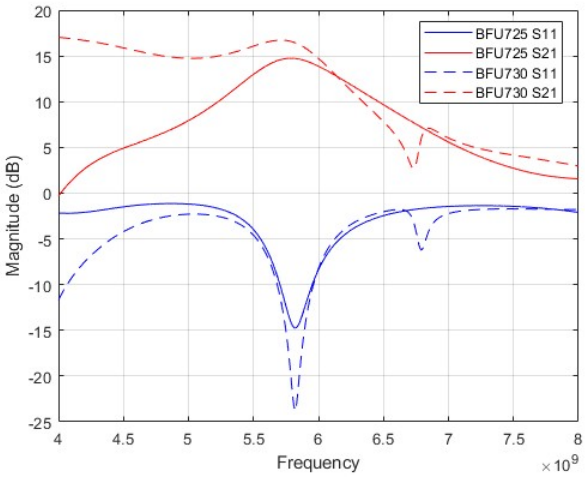

Fig. 18: Gain and reflection coefficients of each design.

IV. Comparison and Fabrication

After both designs have been brought to the point in which they can be sent off to fabrication, a choice is made in which board will get the chance to do so. Fig. 18 shows the difference in gain and the reflection coefficient and the results are as expected. The BFU730F has a higher S21 which results in a higher calculated maximum gain. The BFU730F has a gain of 16.5 dB and a return loss of 21 dB while the BFU725F had a gain of 14.7 dB and a return loss of 14.5 dB. The use of lumped components can also create that difference since there is some amount of loss in the components. The decision is then made to go with the BFU730F design.

Since the BFU730 board was chosen for fabrication, the Gerber files were sent to PCBWAY. PCBWAY is a Chinese PCB fabrication company and within 5 days the board was fabricated and shipped in order to be tested.

The resistors and the transistor were then soldered onto the board and the final result can be shown in Fig. 19. The board was then tested using a Vector Network Analyser to measure the S-parameters which is shown in Fig. 20. While the results are shifted to 5.1 GHz, the gain is great at 14 dB. While it was expected to have 16.5 dB gain, 1 dB is lost at the SMA connectors and the other 1 dB loss can be attributed to a few different educated guesses. The differences can be seen in Fig. 21.

One possibility is that the step transmission lines were not accurately simulated since the location of the step was towards the top or bottom of the transmission lines. Another possibility is the fringing field effects at the input DC bias network. Due

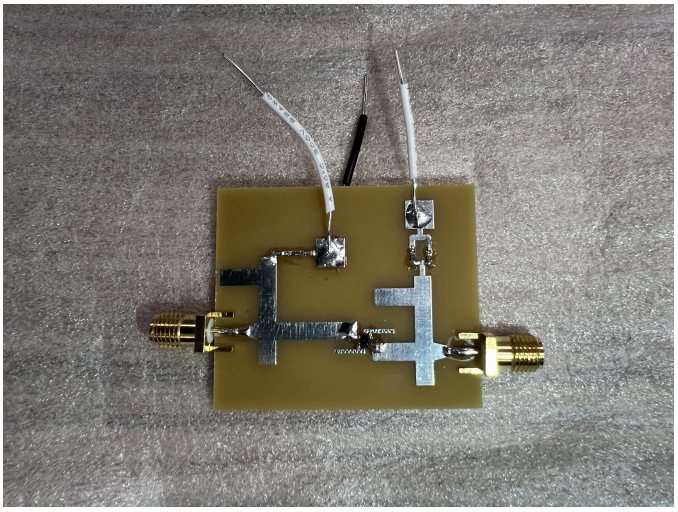

Fig. 19: Fabricated PCB with all components soldered and ready for testing.

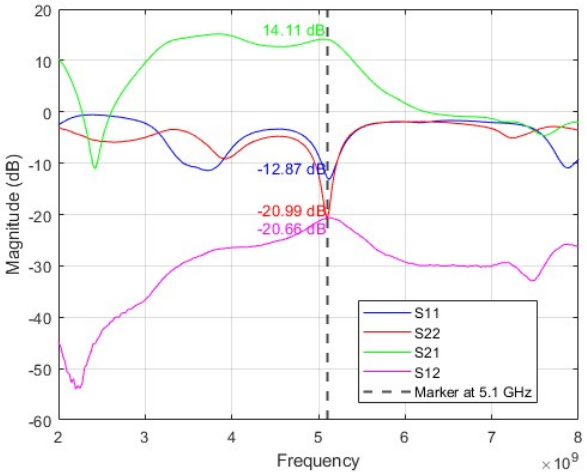

Fig. 20: S-parameters of the fabricated amplifier.

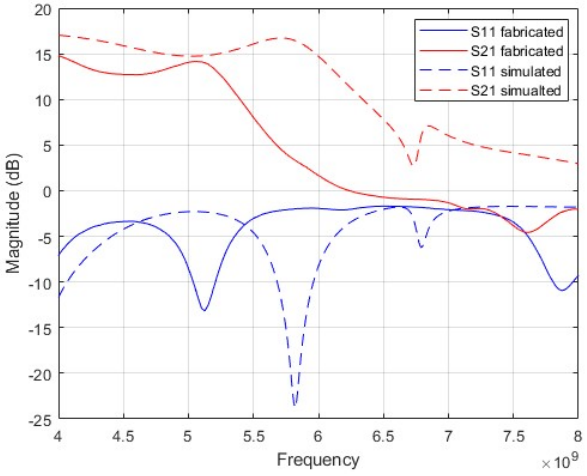

Fig. 21: This graph compares the simulated gain and return loss with the fabricated.

to the open circuit stubs at the edge of the board, the electric fields travel around the substrate through the air and into the bottom conductive plane bypassing the substrate and inducing loss. Now when it comes to the frequency shift, it is most likely a issue with the dielectric constant that was chosen for the design. 4.7 was chosen as that was estimated to be on the higher side as to plan for the worst case scenario but it is possible that isn't accurate to what the boards actually dielectric constant is. Since access to rebuilding and retesting the board was limited, a simulation has been made with a different dielectric constant which can be seen in Fig. 22. While this is quite a high dielectric constant and is not a typical value for FR-4, if the board was designed with this dielectric constant then the fabricated board would have been at the specified frequency.

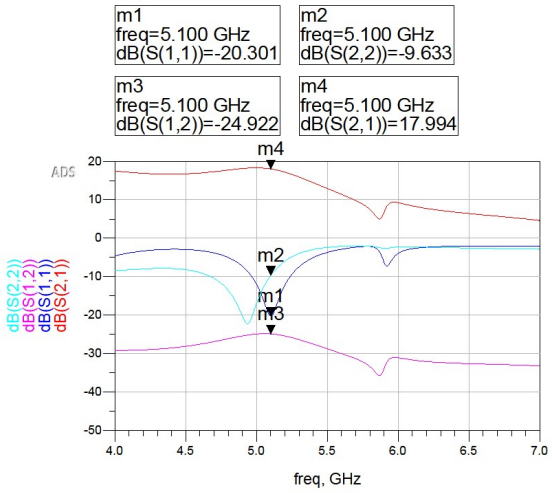

Fig. 22: The S-parameters of the shifted frequency when simulated with a higher dielectric constant.

V. Conclusion

This paper focused on the design of two different 5.8 GHz maximum gain transistor amplifiers to compare the results of each type. The first design used a BFU725 transistor with matching networks created using lumped components. This design achieved a maximum gain of 14.7 dB and a reflection coefficient of-14.5 dB. The second design used a BFU730 transistor with open circuit shunt stub matching networks and observed a gain of 16.5 dB with a reflection coefficient of -21.9 dB. The second design was chosen to be fabricated due to the higher gain and lower reflection coefficient as well as a simpler design due to its lack of lumped components. The vector network analyser was used to test the fabricated amplifier and was found to have a slightly lower gain of 14.11 dB and higher reflection coefficient of -12.87 dB. Further, the measured parameters were found shifted to 5.1 GHz, 700 MHz lower than the design frequency. The board was then re-simulated and found to have a higher relative permittivity of 6.3 instead of the original 4.7.

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