Static Random-Access Memory

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***Abstract*—The SRAM cell that was designed works as intended and each cell can hold a bit which can be read or written over. The design shows how transistor logic works and how a cross coupled inverter can store values as long as it is connected to power. The row and column decoders each use a specific address code in order to select a specific bit or word line. This ensures that the specific cell that is desired to be operated on will be selected. The row decoder and the sense amplifier also show how a clock can be used for power saving and control over parts of the circuit. The sense amplifier also makes sure the bit line stays high or low depending on the input. Overall the design was a success and can be used for further increased bit size. The two bit SRAM that was designed also works as intended and shows how all the parts interact with one another to ensure a working SRAM.**

I. Introduction

RAM is memory used in computers that can perform both read and write operations. To further understand RAM it can be contrasted with read-only memory, (ROM), which can only preform read operations. While ROM is used primarily for mass storage, RAM is used for short term memory for opening files and running applications. There are two types of RAM, static and dynamic, and this report will be focused on how static RAM, or SRAM, works and how it is designed.

In order to design SRAM, a complementary metal-oxide semiconductor, or CMOS, inverter must be used.

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.model MbreakND NMOS
+ Level=1    Gamma= 0   Xj=0
+ Tox=1200n  Phi=.6     Rs=0      Kp=111u  Vto=2.0    Lambda=0.01
+ Rd=0       Cbd=2.0p   Cbs=2.0p  Pb=.8    Cgso=0.1p
+ Cgdo=0.1p  Is=16.64p  N=1

*The default W and L is 30 and 10 um respectively and AD and AS
*should not be included.


.model MbreakPD PMOS
+ Level=1    Gamma= 0   Xj=0
+ Tox=1200n  Phi=.6     Rs=0      Kp=55u   Vto=-1.5   Lambda=0.04
+ Rd=0       Cbd=4.0p   Cbs=4.0p  Pb=.8    Cgso=0.2p
+ Cgdo=0.2p  Is=16.64p  N=1

*The default W and L is 60 and 10 um respectively and AD and AS
*should not be included.
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Fig. 1. This is the CD4007 NMOS and PMOS transistor SPICE models, used in order to specify which transistor models will be used in the PSPICE simulation.

PSPICE will be used to simulate all the designs and the CD4007 transistor model will be used as seen in Fig.1. The sizing of the transistor shows the sizing used only in inverter applications. When transistors are used for other purposes the sizing might be different but will be stated if so.

SRAM contains four different components which are the SRAM cell, the sense amplifier, the column decoder, and the row decoder. Each SRAM cell has the job or storing one bit.

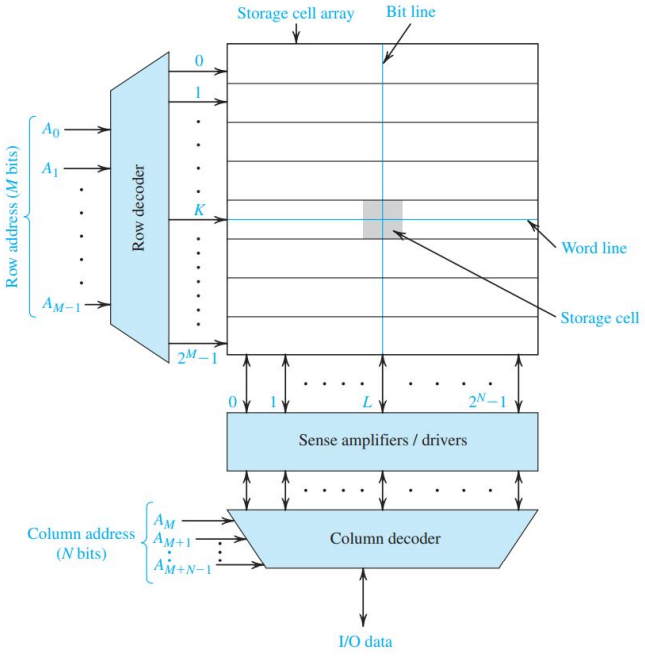

Fig. 2. This is a genral diagram of how SRAM is constructed, showing clearly all four parts and how they are connected in the circuit.

All of the cells are connected via word lines and bit lines. The word lines connect the rows and the bit lines connect the columns. The row decoder and the column decoder uses transistor and Boolean logic to control which bit and word lines are turned on. This allows a specific cell to be selected in order to either read or write a bit on that specific cell. The sense amplifier makes sure that the bit lines are pulled up to V_{DD} or to ground to ensure that the correct value of 0 or 1 is read or written. Since there will be small changes of voltage on the bit line, the sense amplifier will keep the voltages high or low. This construction of SRAM can be shown in Fig. 2 which clearly shows how each part fits in order to effect each cell.

II. SRAM Cell

The SRAM cell is comprised of two cross-coupled inverters, which allow the continuous storing of a bit as long as the cell is receiving power. Two NMOS transistors, called access transistors, are used to access the cell in order to perform read or write operations. The access transistors are controlled using the word line. If that specific word line is selected and turned on, then the access transistors will effect the cell depending on the state of the bit and $\overline{\text{bit}}$ line. Assuming the word line is high or on, the bit lines must both also be high in order to perform a read operation. To perform a write operation, the bit line must be whatever state you are writing. For example,

if it is desired to write a 1, then the bit line must be raised to V_{DD} while the $\overline{\text{bit}}$ line must be set to 0. When writing a 0, the bit line must be set to 0 while the $\overline{\text{bit}}$ must be set to V_{DD}.

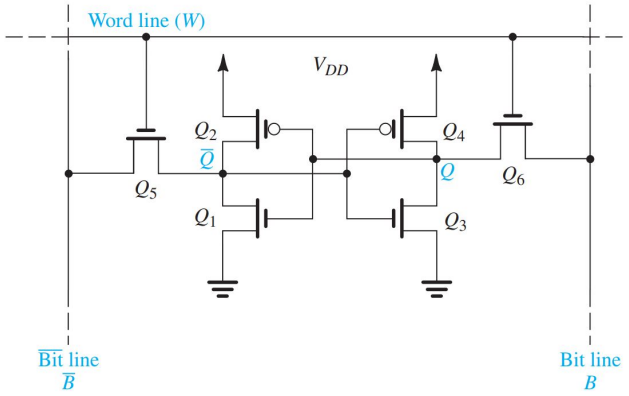

Fig. 3. This is a general diagram of how SRAM is constructed, showing clearly all four parts and how they are connected in the circuit.

A. Transistor Sizing

When sizing the transistors, Fig. 3 will be used to reference which transistor is being talked about. Transistors Q_1, Q_2, Q_3, and Q_4 are part of the cross coupled transistors that make up the cell. Q_1 and Q_3 are NMOS' with a (W/L) of 3 with the width being $30\mu m$ and the length $10\mu m$. While Q_2 and Q_4 are PMOS' with a (W/L) of 6 and the width being $60\mu m$ and the length being $10\mu m$. Finally Q_5 and Q_6 are the access transistors that allow access into the cell. They must be sized differently as the cell will not work as intended if they are size incorrectly.

$$\frac{(W/L)_a}{(W/L)_n} \leq \frac{1}{(1-\frac{V_{tn}}{V_{DD}-V_{tn}})^2} - 1 \qquad (1)$$

For the sizing of these transistors we use (1) to determine the width of the access transistors as the length for all transistors in this design remain the same. Once plugging in all the values to (1), the result comes out to $\leq 2400\mu m$. That means the width of the access transistor must be less than $2400\mu m$ which ends up being quite a large width for a transistor. Since any width less than $2400\mu m$ can be used the design implemented a $60\mu m$ width for the access transistors.

B. SRAM Read Operation

When the SRAM cell is storing a 1, Q as seen in Fig.3 is high. Assume that word line is selected which means the gate for Q_5 and Q_6 are high and whenever performing a read operation, both the bit and $\overline{\text{bit}}$ lines must be high. That means Q_6 is off since v_{GS} is 0 which is less than any v_{tn} possible. Q_6 being off allows the use of an equivalent circuit shown in Fig. 4. Since v_Q is high, that means $v_{\overline{Q}}$ must be low since it is the complement of v_Q. $C_{\overline{B}}$ represents the parasitic capacitance that is formed from all the transistors connected to the $\overline{\text{bit}}$ line. $C_{\overline{Q}}$ represents the parasitic capacitance that is formed from all the transistors in that specific cell. When the $\overline{\text{bit}}$ line is set

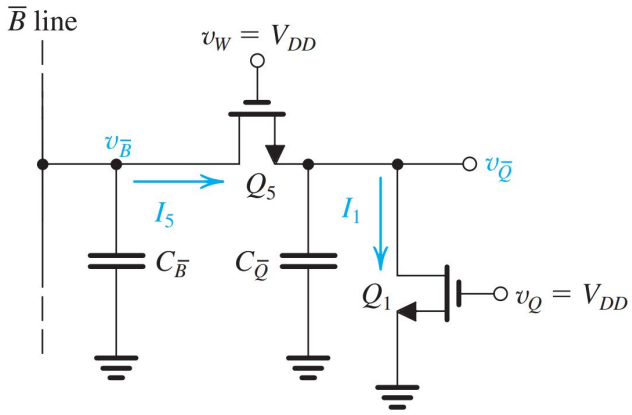

Fig. 4. This is an equivalent circuit for an SRAM cell used when v_Q is high.

high, $C_{\overline{B}}$ charges up to V_{DD}. Then the word line goes high and Q_5 is turned on allowing current I_5 to pass through the transistor charging up $C_{\overline{Q}}$. At a certain point the current will stop flowing into $C_{\overline{Q}}$ and will go into transistor Q_1 and I_5 and I_1 will reach an equilibrium. Since $v_{\overline{B}}$ was discharging it will dip slightly from V_{DD}. When sized correctly $v_{\overline{Q}}$ will never reach passed $V_{DD}/2$ since that will cause the cell to flip from a 1 to a 0. A read 0 operation is extremely similar to a read 1 and the same events occur but takes place on transistors Q_6 and Q_3.

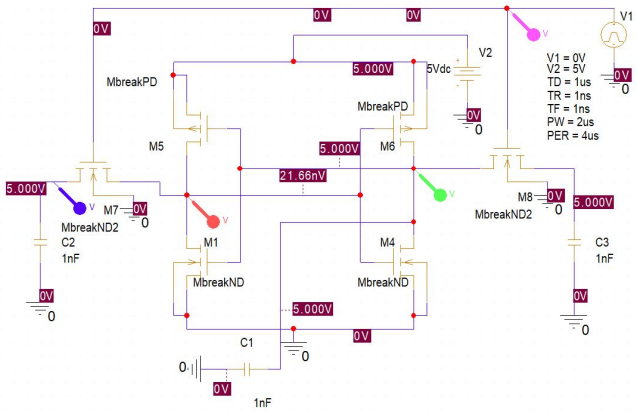

Fig. 5. The SRAM cell designed in PSPICE for a read 1 operation.

The circuit diagram shown in Fig. 5 is a PSPICE simulation of the SRAM cell. Capacitor C1 is used to set Q to a specific voltage. In this case C1 has an initial charge of 5 volts and is setting the SRAM cell to read a 1. C2 and C3 are used similarly to set the bit and $\overline{\text{bit}}$ lines to 5 volts in order to perform the read operations. C2 and C3 also have an initial charge of 5 volts and all of the capacitors have a value of $1nF$ so they discharge at a speed in orfder to see the effect it has to the cell. The word line is controlled using a pulse voltage generator from 0 to 5 volts with a $1\mu s$ time delay. The rise and fall times of the pulse are set to $1ns$ and period is $4\mu s$ long. The pulse width is half of the period at $2\mu s$. It is set this way to see what the cell looks like when the access transistors are off to ensure that the cell is still holding the same bit.

The output of the PSPICE SRAM design can be seen in Fig. 6 and Fig. 7 where Fig. 6 shows the pulse wave controlling the word line so it can be contrasted to Fig. 7, which shows the cell state, in order to see the effect of the word line has on the cell. The graph shows that as expected Q is high and $\overline{\mathrm{Q}}$ is low and that the voltage on the $\overline{\mathrm{bit}}$ line is slowly discharging while the word line is high. This will be fixed once the sense amplifier is connected and can charge the $\overline{\mathrm{bit}}$ line back to V_{DD}. The read 1 operation is a success as it has worked as expected and holds the value that is desired in the cell.

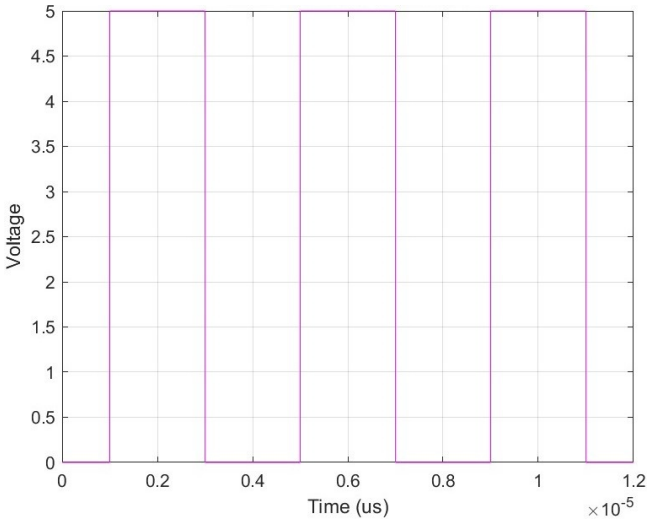

Fig. 6. This graph shows the 5 volt square wave that is turning the word line on and off. It has a 1 microsecond time delay to allow transistors to pre-charge. It has a frequency of 250 kHz.

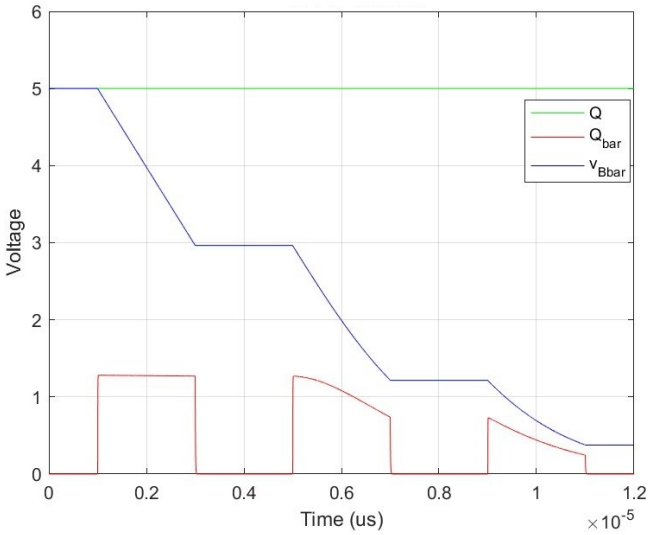

Fig. 7. This graph shows what the read 1 operation looks like in the cell. The $\overline{\mathrm{bit}}$ does not go back to V_{DD} since it is not yet connected to the sense amplifier. In its current state it will discharge continuously as long as the word line is high.

The next operation to look at is the read 0 operation. As seen in Fig. 8 the circuit changes just a little to set the cell to store a 0. The C1 capacitor is now setting $\overline{\mathrm{Q}}$ high so that it can be inverted to set Q to 0. The bit line is also being measured using the blue probe instead of the $\overline{\mathrm{bit}}$ line since the change in voltage will occur in the bit line instead. As expected, Fig. 9 shows Q is low this time and that inversely $\overline{\mathrm{Q}}$ is now high. It can also be seen that the v_B line has the same response that that the $v_{\overline{\mathrm{B}}}$ line had where it slowly discharges and will continue to discharge until the sense amplifier is connected. The same word line graph seen in Fig. 6 can be compared to Fig. 9 in order to see how the word line changes how the cell operates. When the word line is on, the bit line is connected, which raises Q slightly above zero since the voltage from the bit line is still discharging. When the word line is off the bit line is no longer connected to Q since the access transistors cut off which sets Q back to 0.

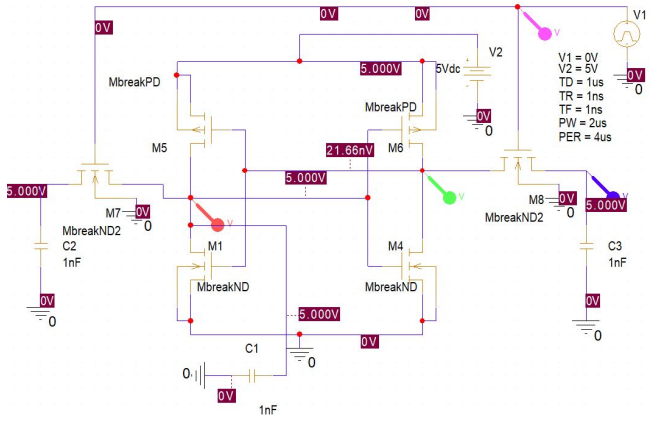

Fig. 8. This is a PSPICE circuit diagram of a SRAM cell that is precharged using C1 to hold a 0 in order to show a read 0 operation.

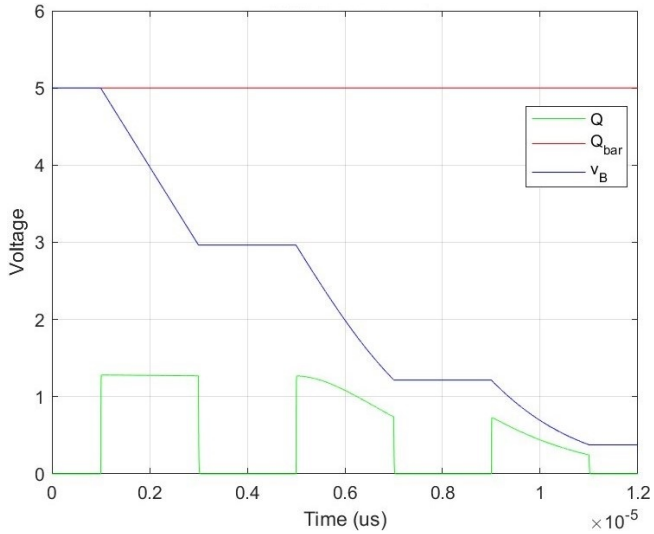

Fig. 9. This graph shows what the read 0 operation looks like in the cell. The bit line does not go back to V_{DD} since it is not yet connected to the sense amplifier. In its current state it will discharge continuously as long as the word line is high.

C. SRAM Write Operation

SRAM writing operation relies on pulling the cell down or up depending on what is being written. As mentioned earlier, the access transistors are designed so that a flip of the cell

cannot occur. $v_{\overline{Q}}$ and v_Q cannot go over 2.5 volts to flip the cell. So in order to flip the cell, $v_{\overline{Q}}$ must be pulled down while v_Q is pulled up or visa versa. For example, for a write 0 operation, $v_{\overline{Q}}$ will be low since v_Q must be high in order to write a 0. So to flip the cell, $v_{\overline{Q}}$ must be pulled up while v_Q is pulled down. The bit line is set to low in order to pull v_Q down and the $\overline{\text{bit}}$ line is pulled up to V_{DD} to pull $v_{\overline{Q}}$ up. This will then flip the cell because the gate voltage of M4 and M6, as seen in Fig. 10, will go above $V_{DD}/2$ which in this design is 2.5 volts. This will then flip the inverter inputs and cause v_Q to be high which will then feedback and make $v_{\overline{Q}}$ low, successfully writing a 0 in that cell.

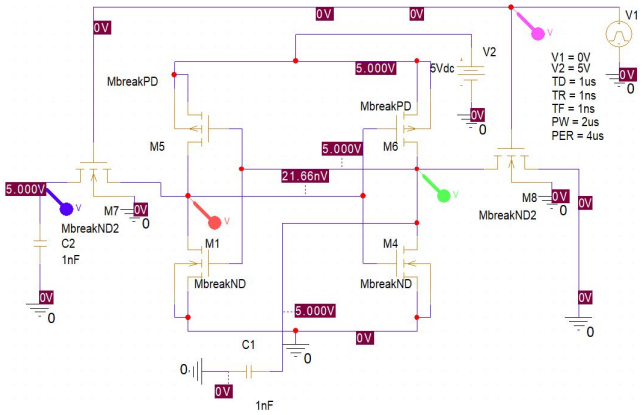

Fig. 10. This is the PSPICE circuit diagram for a write 0 operation. The capacitor C1 is presetting the cell to hold a 1 in order for there be a visible change when writing a 0. C2 represents the $\overline{\text{bit}}$ line with an initial charge of 5 volts to set it high. The bit line is connected to ground to set the line to low.

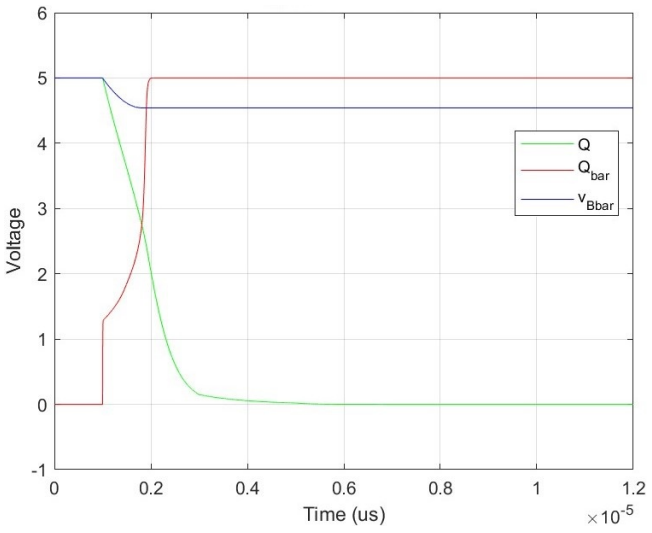

Fig. 11. This is the output waveform of the write 0 circuit. Q is being pulled down to 0 volts while $\overline{\text{Q}}$ is being pulled up to 5 volts and the cell will then hold that charge to keep the 0.

The output waveform, as seen in Fig. 11, clearly shows the write 0 operation. Q is precharged to high which then inverts and sets $\overline{\text{Q}}$ to low. Once the word line is turned on at $1\mu s$, the access transistors turn on and connect the cell to the bit lines which allow the pull up of $\overline{\text{Q}}$ and pull down of Q. $v_{\overline{\text{B}}}$ will discharge to pull $\overline{\text{Q}}$ up and once $\overline{\text{Q}}$ is high then it will stop discharging. Once connected to the sense amplifier it will charge back up to V_{DD}. Even when the word line is off, since it is connected to a pulse signal generator, the correct charge is still held and Q stays low and $\overline{\text{Q}}$ stays high until a change is made. The write 1 operation is also a success with this SRAM cell design. Finally the write 1 operation will be simulated and tested to see if the SRAM design works for all cases.

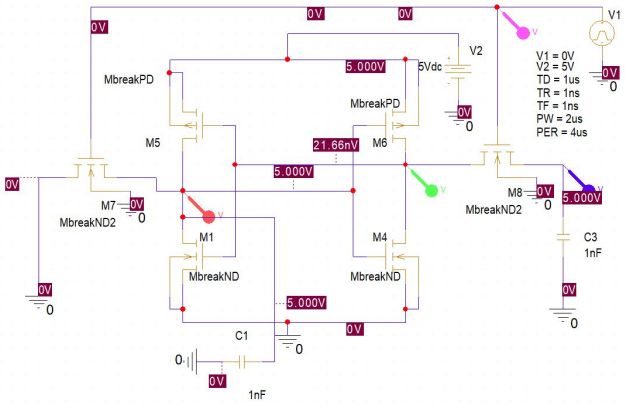

Fig. 12. This is the PSPICE circuit diagram for a write 1 operation. The capacitor C1 is presetting the cell to hold a 0 in order for there be a visible change when writing a 1. C3 represents the bit line with an initial charge of 5 volts to set it high. The $\overline{\text{bit}}$ line is connected to ground to set the line to low.

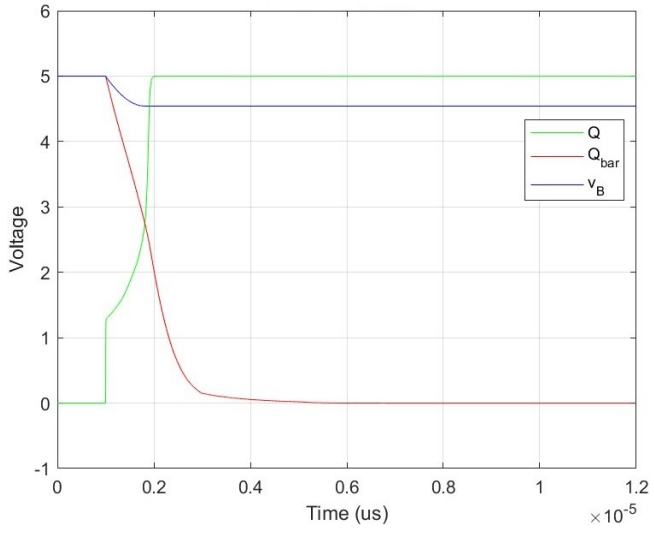

Fig. 13. This is the output waveform of the write 1 circuit. $\overline{\text{Q}}$ is being pulled down to 0 volts while Q is being pulled up to 5 volts and the cell will then hold that charge to keep the 1.

When writing a 1 it is very similar to writing a 0 since it is just the opposite of what was done to write a 0. The cell it precharged to hold a 0 as seen in Fig. 12 and the $\overline{\text{bit}}$ line is now set to ground and the bit line is set with an initial charge of 5 volts. This pulls Q up and $\overline{\text{Q}}$ down in order to flip the cell. The results can be seen in Fig. 13 and shows how Q starts at a low input but is then flipped to a high input demonstrating the success of the design. All four cases have worked as intended and help further show how the cell operates when it is selected.

III. Sense Amplifier

The sense amplifier is very similar to the cell itself but instead of having access transistors, in now has a PMOS above the cell and an NMOS below the cell acting as a clock as seen in Fig. 14. Those transistors allow the sense amplifier to be turned off if need be such as when the cell that is being effected word line is low. This is to save power as there is a sense amplifier or each column of the SRAM. The sense amplifier is used to keep the bit or $\overline{\text{bit}}$ lines charged up to V_{DD} and stops the dicharging from occurring as seen in the earlier diagrams.

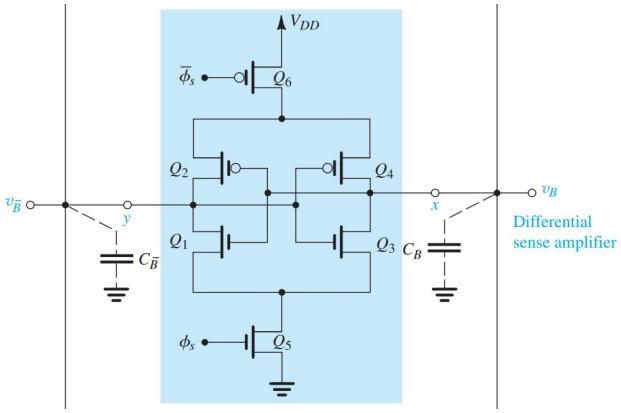

Fig. 14. This is a general circuit diagram for the sense amplifier.

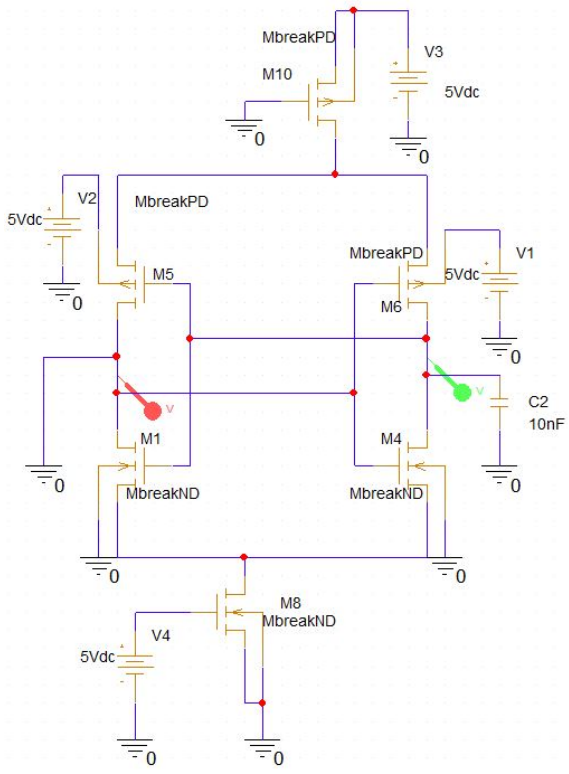

Fig. 15. This is PSPICE circuit diagram showing the sense amplifier when connected to a cell that is writing a 1 as the bit line is high while the $\overline{\text{bit}}$ line is low.

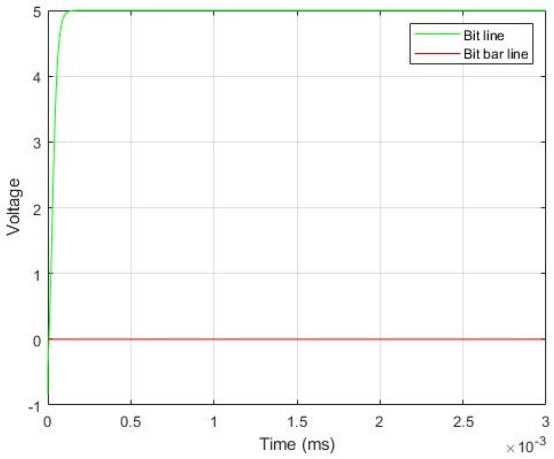

Fig. 16. This is output wave form of the sense amplifier when connected to a write 1 operation.

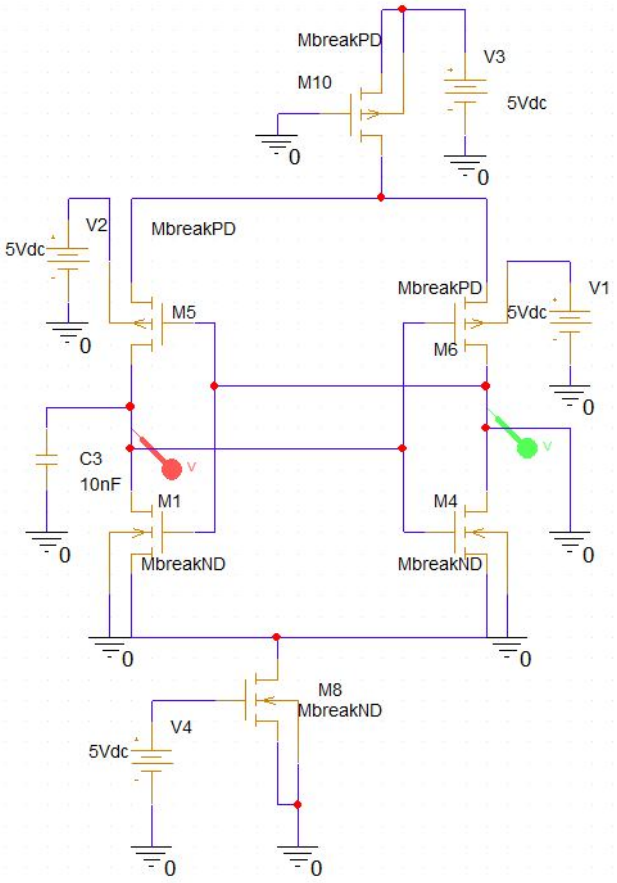

Fig. 17. This is PSPICE circuit diagram showing the sense amplifier when connected to a cell that is writing a 0 as the bit line is low while the $\overline{\text{bit}}$ line is high.

The PSPICE design as seen in Fig. 15 shows a very similar design as the SRAM cell design. The clock is preset to high to show the sense amplifier when it is working and for this case the bit line is high. This is in order to see how the sense amplifier operates while connected to a write 1 operation. C2 is set to have an initial charge of 4.6 volts to emulate the voltage

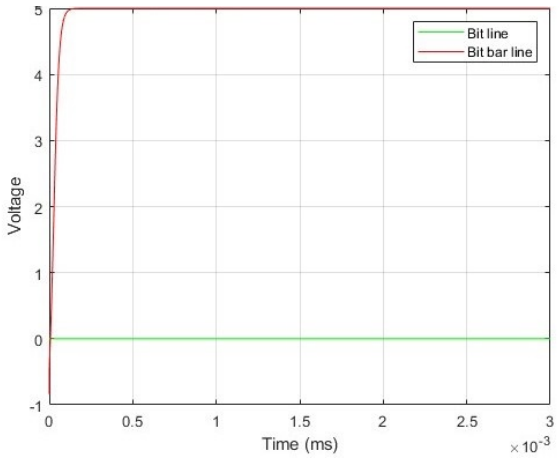

Fig. 18. This is output wave form of the sense amplifier when connected to a write 0 operation.

drop a write operation causes. The sense amplifier will use the feedback loop from the cross coupled inverters in order to pull the high charge of 4.6 volts back to V_{DD}.

With the sense amplifier on and working the bit line is pulled up to 5 volts even tho it was set at 4.6 volts as seen in Fig.16. And the $\overline{\text{bit}}$ line is set to 0 and holds that zero continuously. This shows how the sense amplifier is successful pulling the intended line to V_{DD}.

The PSPICE circuit diagram seen in Fig. 17 shows the opposite case, where the $\overline{\text{bit}}$ line is now set to high and the bit line is set to low. This simulates a sense amplifier connected to a write 0 operation and if working correctly should set the $\overline{\text{bit}}$ line back to V_{DD} in order to get rid of the lines discharge. C3 is also set to 4.6 volts to simulate a voltage drop. This design is also a success as Fig. 18 shows the $\overline{\text{bit}}$ line go high to V_{DD} as the bit line goes low which is exactly what is needed for a write 0 operation. The sense amplifier design is a success.

IV. Column Decoder

The column decoder allows the user to select a bit line depending on an address bit code. The number of bit lines changes depending on the amount of bits the SRAM is designed for. The variable N will be used when describing the number of bits. Since there is a bit and $\overline{\text{bit}}$ line for each cell, the amount of bit lines grows exponentially 2^N power.

The column decoder that will be used is a tree column decoder as seen in Fig. 19 where each A represents one number in an three bit address input. It works so that only one bit line will be selected at a time. For example, if the input was 101, then the three transistors highlighted will turn on and allow a route from the I/O data to the B_5 bit line. Only the combination of all three of those transistors will allow access to the bit line. Even if one or two series transistors are on but the last one is off then current will not flow so it must be a combination of all threee series transistors.

When designing the tree column decoder, the NMOS are sized for three transistors in series meaning the width of all the NMOS's is $10\mu m$ while the length stays the same. The PSPICE circuit diagram as seen in Fig. 20 is designed for a

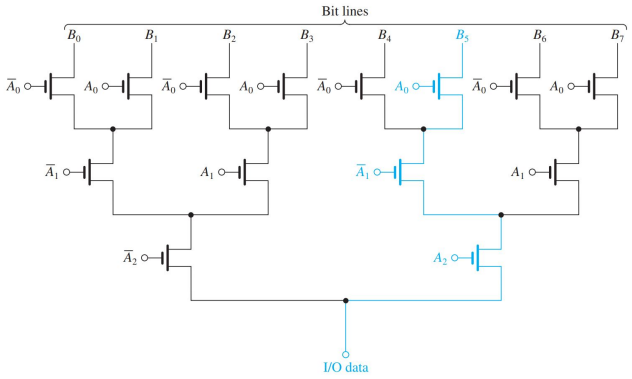

Fig. 19. This is a general diagram of a tree column decoder.

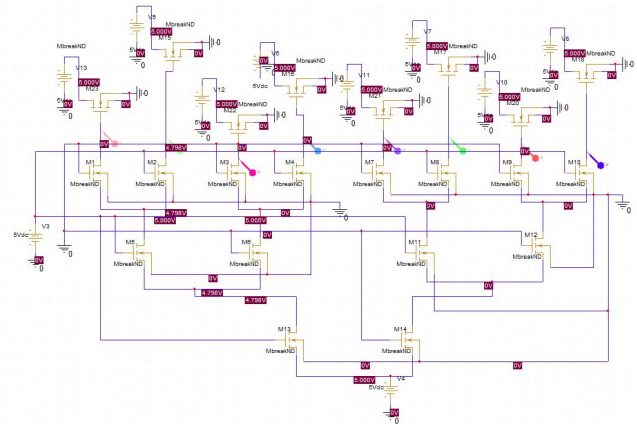

Fig. 20. This is a PSPICE circuit diagram of a column decoder that is set with an 001 bit address code which activates the second bit line.

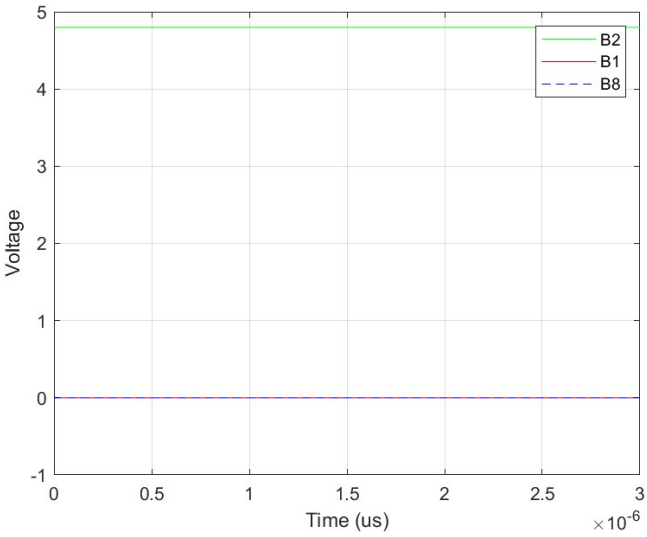

Fig. 21. This is output wave form of the tree column decoder showing how the correct bit line is high and the rest are low. Since the all of the low probes overlap only two are shown.

three bit address code input which requires eight bit lines. The three bit address code is 001 for this case which should have the second bit line be the only one on which is what the circuit is doing as seen by the voltage markers on the diagram. There will be a small voltage drop as seen in Fig. 21 which comes

from the small parasitic capacitance the three transistors in series create. The design is working correctly since only the correct bit line is high while all the others are low. The bit line that is on also corresponds correctly with the bit address code that was inputted into the circuit.

V. Row Decoder

The row decoder is designed to take a bit address code and use it to select the correct corresponding word line to turn on. It does this by using a clock connected to a PMOS transistor that is set low to turn the word lines on and only the row with all other connect NMOS's turned off does the word line stay at V_{DD}. If the NMOS's were turned on, current can then flow through them discharging the wordline. When all the NMOS's are turned off on that specific word line, no current travels through the NMOS's so that the word line stays at V_{DD}. The NMOS's are designed so that each wordline is connect to a specific bit address code.

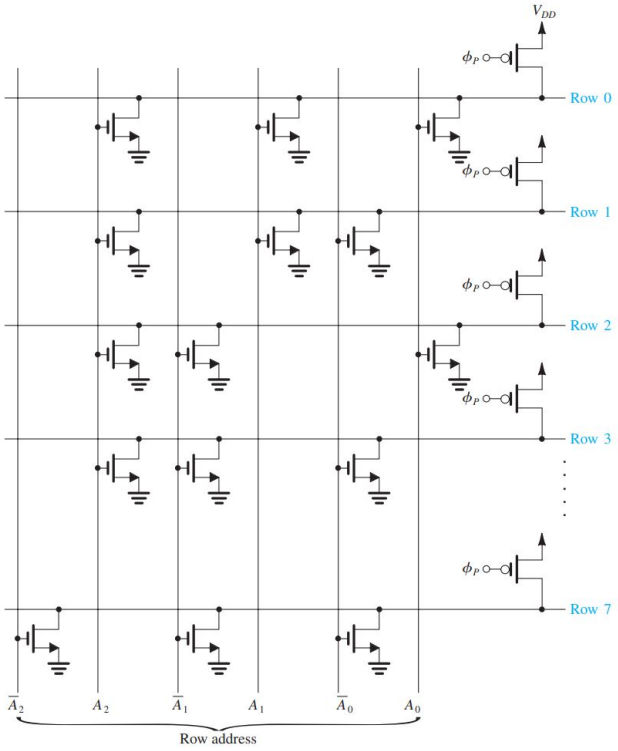

Fig. 22. This is a row decoder diagram to show how the transistors should be placed in order to set a specific word line on.

For example, in Fig. 22 the first word line is set to go high if the bit address input code is set to 000. The second word line is set for but address code 001 and so on. This ensures each word line is set up for a specific bit address code and allows for all codes to be covered. This can also be seen in Fig. 23 which shows the PSPICE circuit diagram which is set up with a 010 bit address code in order set the third word line on. The PSPICE diagram shows and extended version of the diagram given by Fig. 22. This design can work for any three bit address code as long as the clock is low so that the PMOS's are on. The PSPICE design is proven successful by looking at the output waveform in Fig. 24 which shows how the correct word line is high. With both the row and column decoder, a specific cell can now be selected without actually inputting a source to set the word or bit line high. It can now be down without touching the cell and with a specific bit address code.

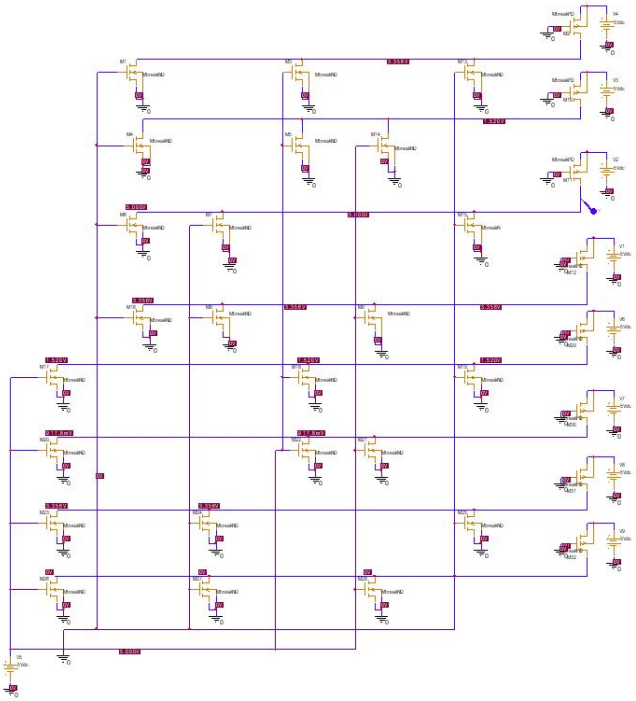

Fig. 23. This is PSPICE circuit diagram of a row decoder designed for a three bit address code input. The bit address code is currently set to 010.

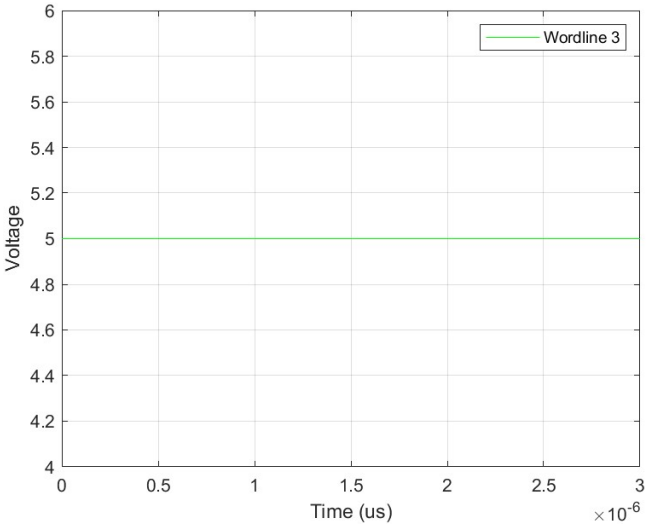

Fig. 24. This is output wave form of the row decoder showing how the third word line is high when a 010 bit address code is inputted.

VI. Final Result

After connecting all parts together, unfortunately it seems impossible to show the whole schematic as it is too large and cannot be show with a clear image in this report. The final

output wave form is shown in Fig. 25. The final design was a 2 bit SRAM and with a bit address code input of 01. The output wave form shows the word line high and a write 1 operation being performed in the top left cell. The design was a success.

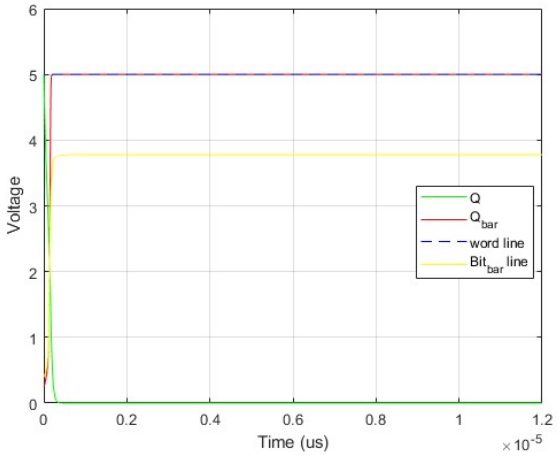

Fig. 25. This is output wave form of the entire SRAM circuit connected while looking specifically at the 01 cell.

VII. Conclusion

In conclusion, all of the designs shown in this report are proven successful and working as intended. The SRAM cell can read and write both a 0 and a 1. The sense amplifier pulls the correct bit line high when a lower voltage is inputted in the bit line. The row decoder selects the correct word line depending on what address code is inputted. The column decoder also selects the correct bit line when the same address code is inputted. This design can be blown up to include many more bits than has been included and all that needs to be done is copy and paste the design in order to account for more bits.

Referances

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, *Microelectronic Circuits*. Oxford University Press, 2021.

[2] B. Jackson, *SRAM Lecture Notes*, 2023

[3] B. Jackson, *DRAM and Sense Amplifiers Lecture Notes*, 2023

[4] B. Jackson, *Row & Column Decoders and ROM Lecture Notes*, 2023