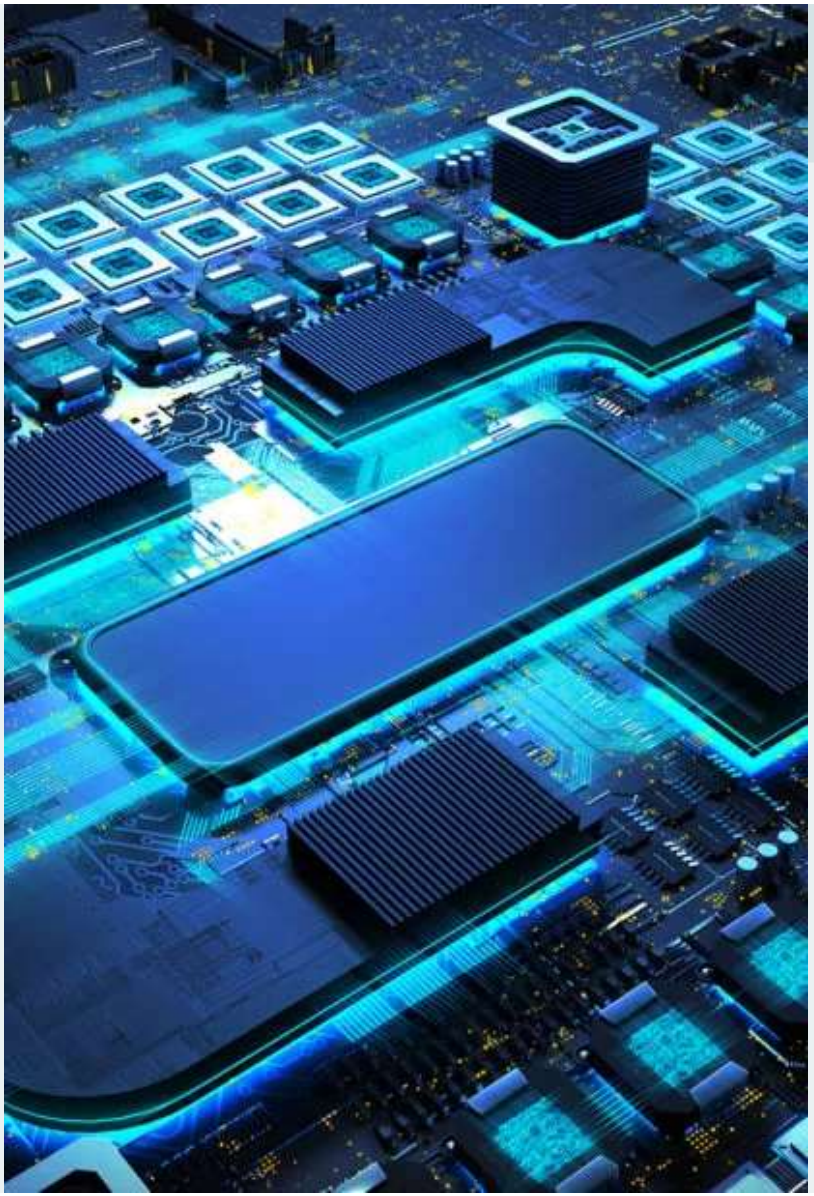
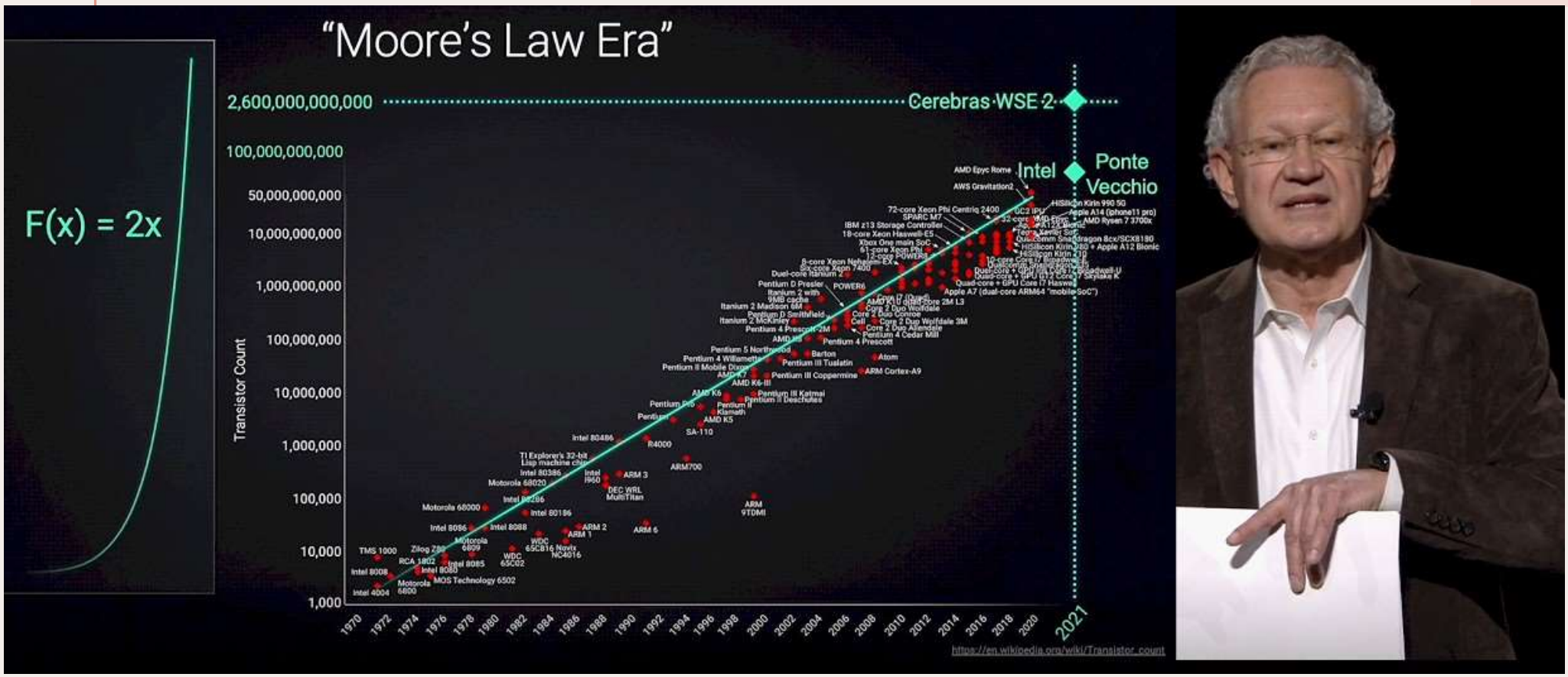
ESD protection on 3D IC

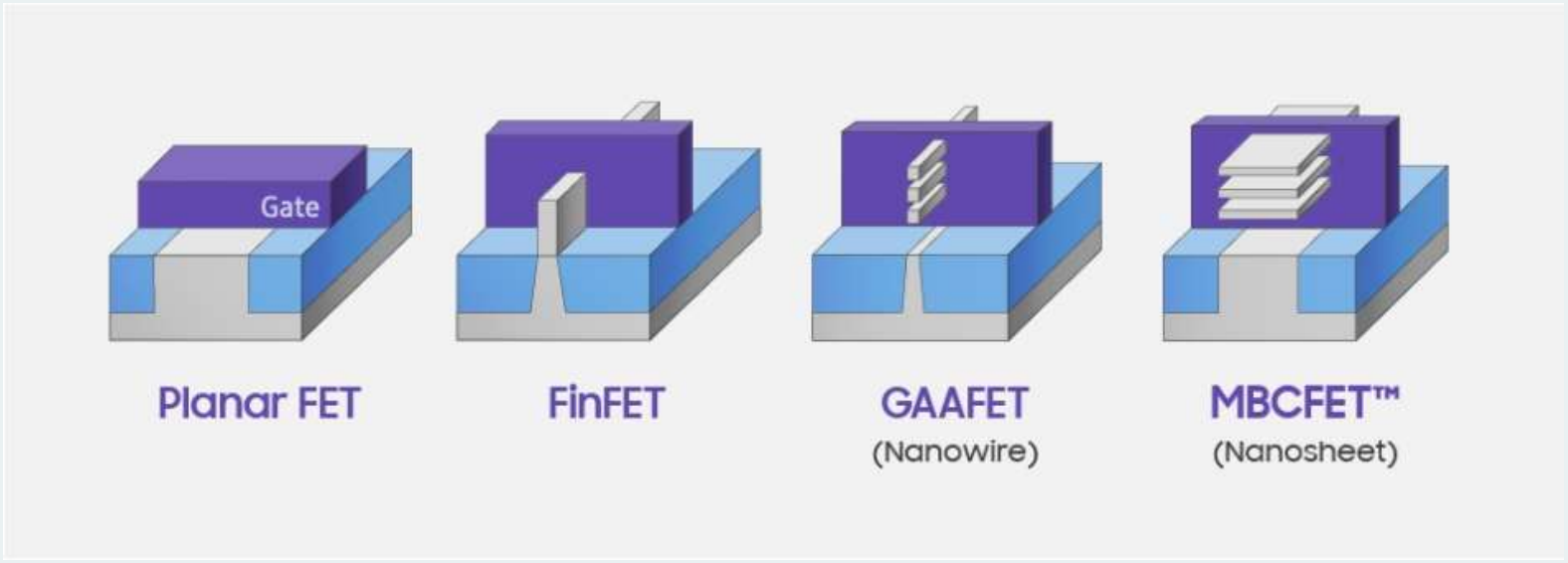
- Abner Huang
- Ph.D. of CS, NTHU
- Sr. Staff Engineer of Synopsys
- DRC/PERC, IC Validator

三維積體電路

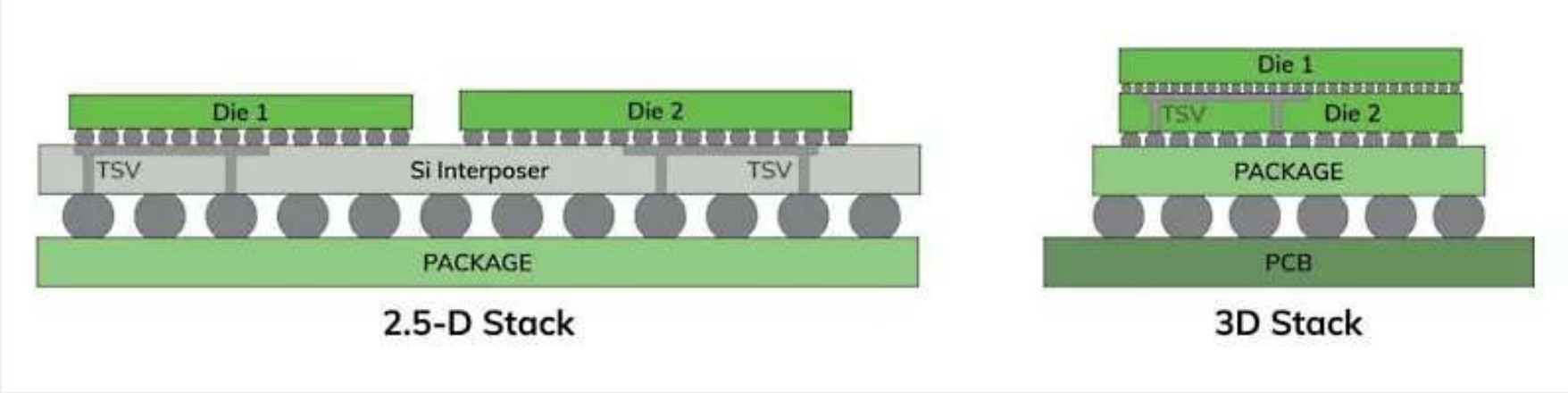


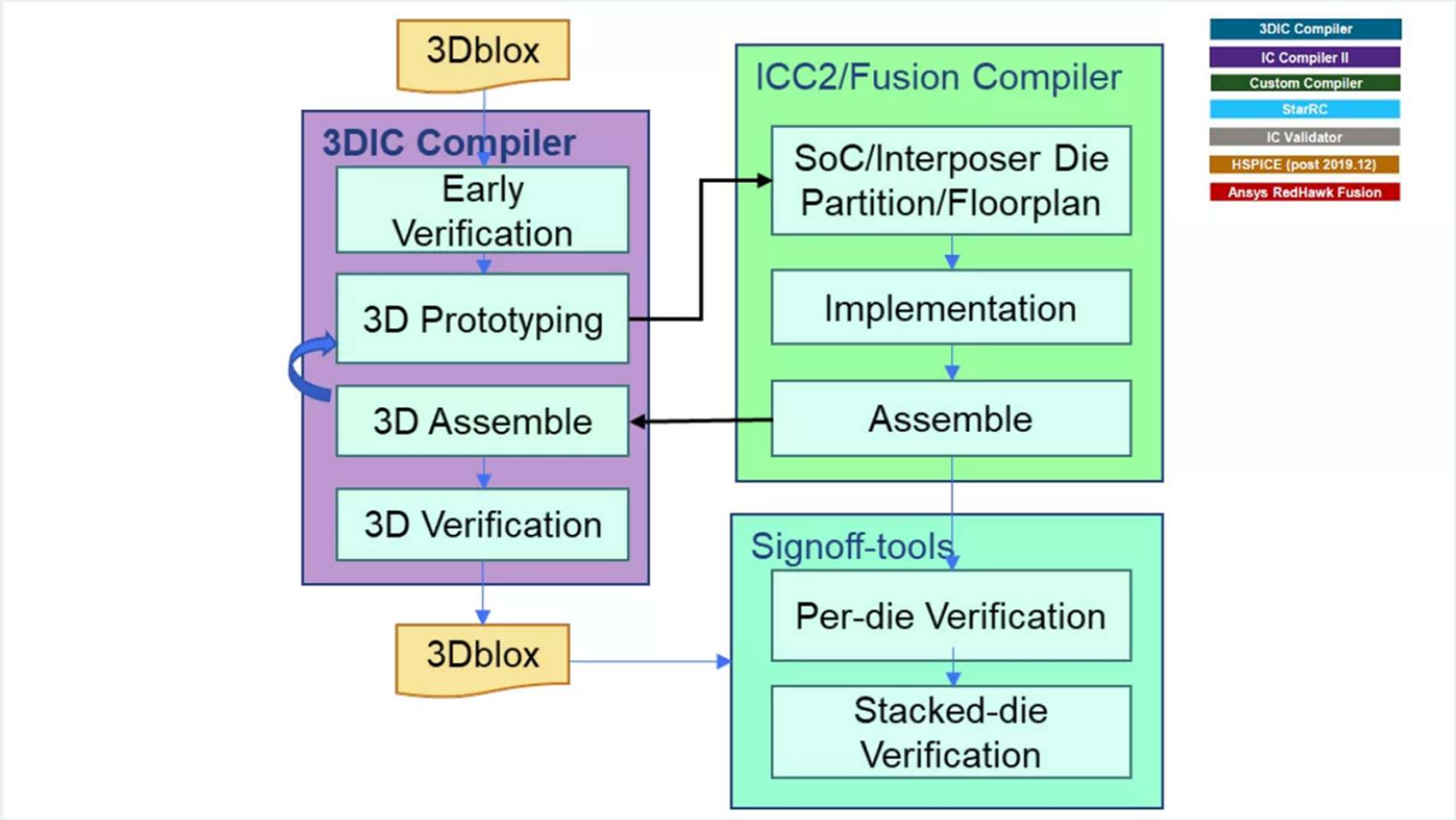

"Moore's Law Era"
F(x) = 2x
2,600,000,000,000
Cerebras WSE 2
100,000,000,000
50,000,000,000
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
Transistor Count
Intel
Ponte Vecchio
2021
1970
1972
1974
1976
1978
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000
2002
2004
2006
2008
2010
2012
2014
2016
2018
2020
AMD Epyc Rome
AWS Gravitation2
72-core Xeon Phi Centriq 2400
SPARC M7
IBM z13 Storage Controller
18-core Xeon Haswell-E5
Xbox One main SoC
61-core Xeon Phi
12-core POWER8
8-core Xeon Nehalem-EX
Six-core Xeon 7400
Dual-core Itanium 2
Pentium D Presler
Itanium 2 with 9MB cache
Itanium 2 Madison 6M
Pentium D Smithfield
Itanium 2 McKinley
Pentium 4 Prescott-2M
AMD K8
Pentium 5 Northwood
Pentium 4 Willamette
Pentium II Mobile Dixon
AMD K7
AMD K6-III
AMD K6
Pentium Pro
Pentium
Pentium
AMD K5
SA-110
Intel 80486
R4000
TI Explorer's 32-bit Lisp machine chip
Intel 80386
Intel i960
ARM 3
Motorola 68020
DEC WRL MultiTitan
Intel 80286
Motorola 68000
Intel 80186
ARM700
ARM 9TDMI
Intel 8086
Intel 8088
ARM 2
ARM 1
ARM 6
Motorola 6809
WDC 65C816
Novix NC4016
TMS 1000
Zilog Z80
RCA 1802
WDC 65C02
Intel 8085
Intel 8080
Intel 8008
Motorola 6800
MOS Technology 6502
Intel 4004
Pentium III Tualatin
Barton
Pentium III Coppermine
Pentium III Katmai
Pentium II Deschutes
Pentium 4 Prescott
Pentium 4 Cedar Mill
Core 2 Duo Allendale
Core 2 Duo Wolfdale 3M
Cell
Core 2 Duo Conroe
Core 2 Duo Wolfdale
AMD K10 quad-core 2M L3
POWER6
Apple A7 (dual-core ARM64 "mobile-SoC")
Quad-core + GPU Core i7 Haswell
Dual-core + GPU Core i7 Broadwell-U
Quad-core + GPU Core i7 Skylake K
Atom
ARM Cortex-A9
Apple A14 (iphone11 pro)
AMD Ryzen 7 3700x
https://en.wikipedia.org/wiki/Transistor_count

MOSFET to FINFET

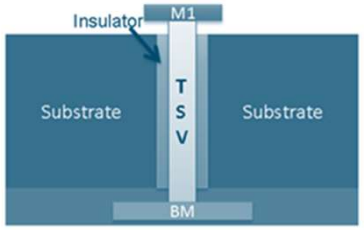


2.5D IC and 3D IC



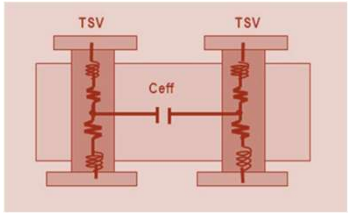

3Dblox
3DIC Compiler
Early Verification
3D Prototyping
3D Assemble
3D Verification
3Dblox
ICC2/Fusion Compiler
SoC/Interposer Die Partition/Floorplan
Implementation
Assemble
Signoff-tools
Per-die Verification
Stacked-die Verification
3DIC Compiler
IC Compiler II
Custom Compiler
StarRC
IC Validator
HSPICE (post 2019.12)
Ansys RedHawk Fusion

Thru Silicon Via



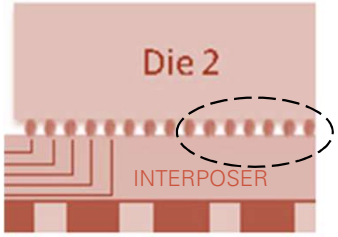
Need to Model TSV Parasitics accurately

TSV Coupling



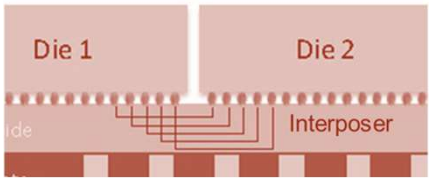
Extract TSV to TSV Coupling in floating substrate

Micro-Bump



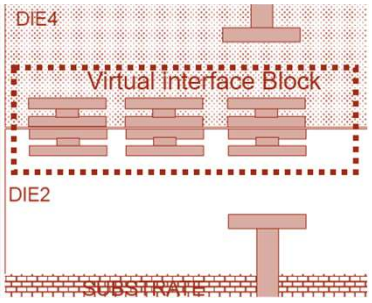
Resistance of Micro bumps needs to extract

Interposer



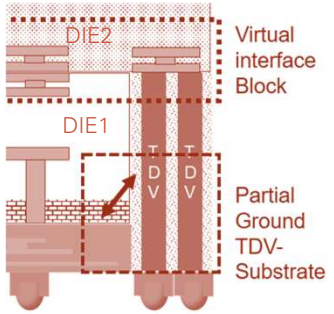
High speed Interposer interconnect parasitic needs to be extracted

Multi-Die Stacking

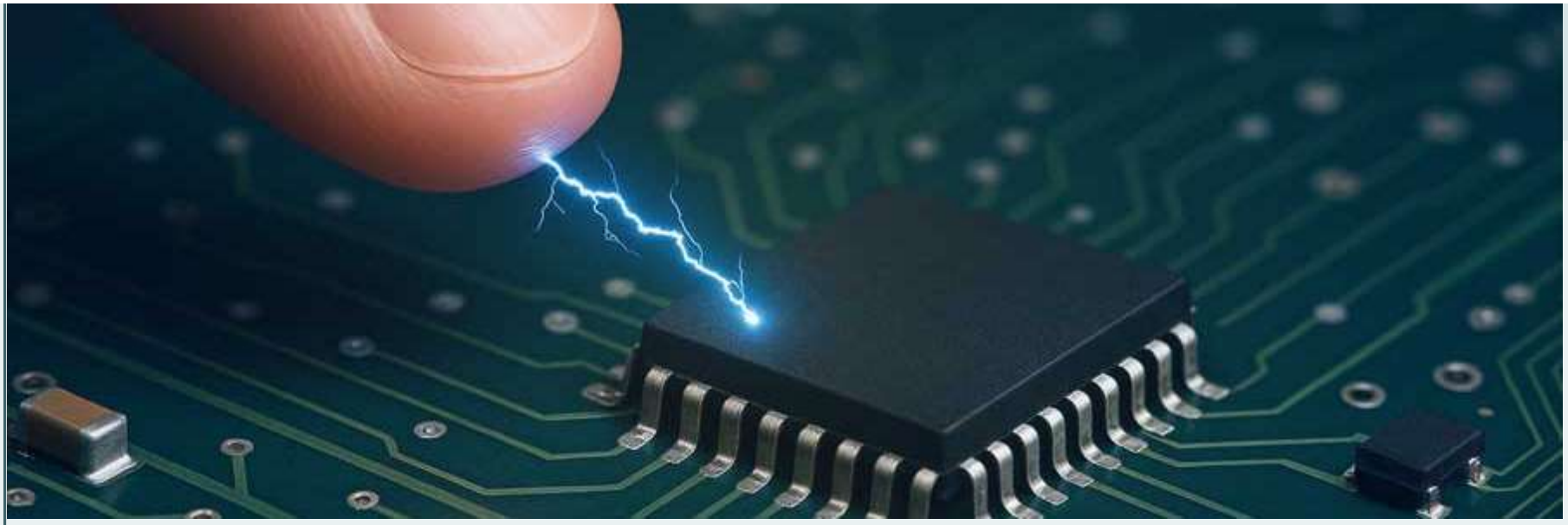


Hybrid Bond Link allows multi-die stacking – Extract Die-to-Die coupling

SOIC-Thru Dielectric Via



Tall TDV is needed for connecting to top Die – TDV parasitics needs to be extracted



靜電放電保護

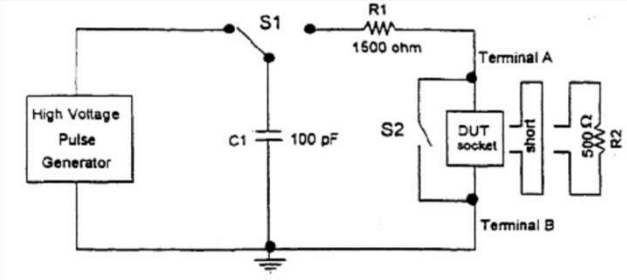
ElectroStatic Discharge

ESD Models

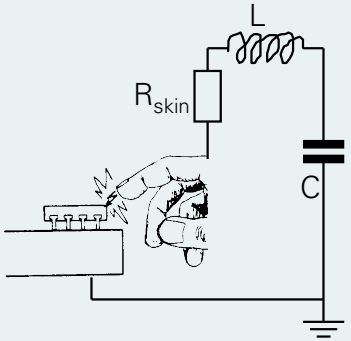
- The model used to simulate when a person comes into contact with an ESDS device is the Human Body Model (HBM).
- MM is designed to simulate a machine discharging through a device to ground. Failure modes in MM testing are similar to those in HBM testing.
- CDM (Charged Device Model) simulates an integrated circuit becoming charged and discharging to a grounded metal surface.
- In 3D IC, ESD in manufacturing is getting attentions.

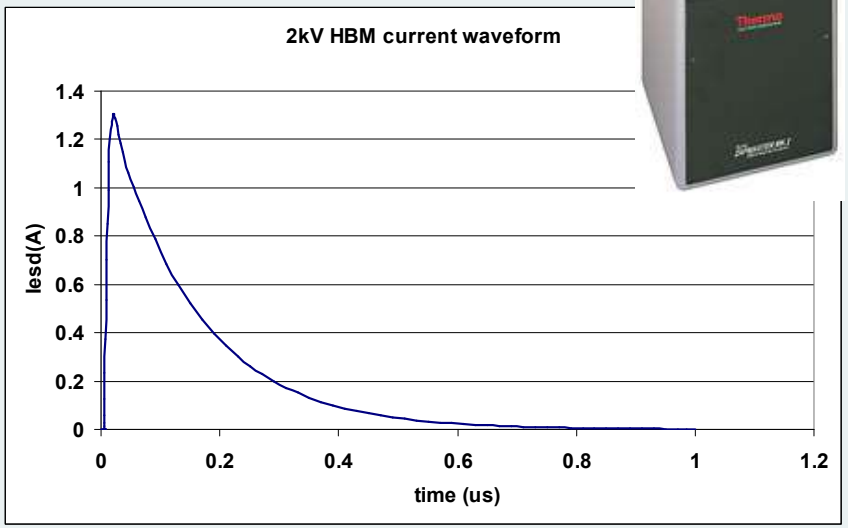
HBM

Attempts to model the ESD event which occurs when a charged person touches a device



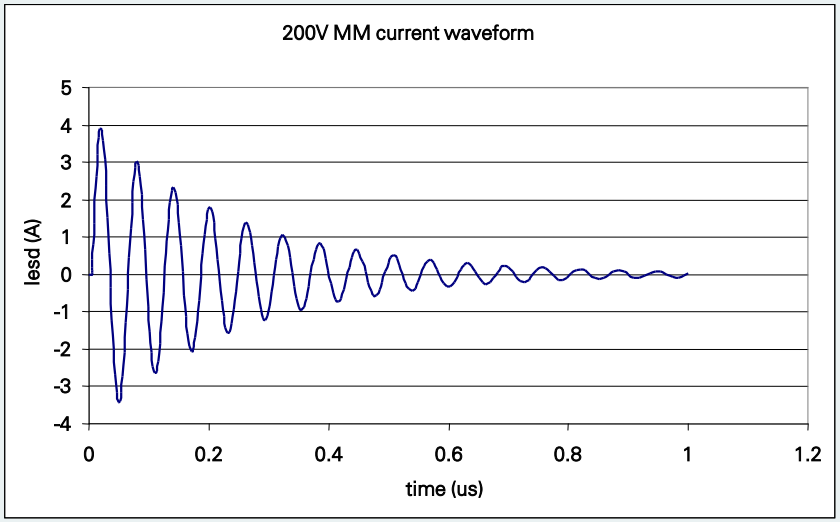
- R= 1500 Ω, C= 100 pF, L= 7.5 μH
- Maximum peak current 1.3 Amp @ **2.0 kV**
- Rise time 2..10ns





MM

Aimed at simulating abrupt discharges which are caused by contact with charged equipment

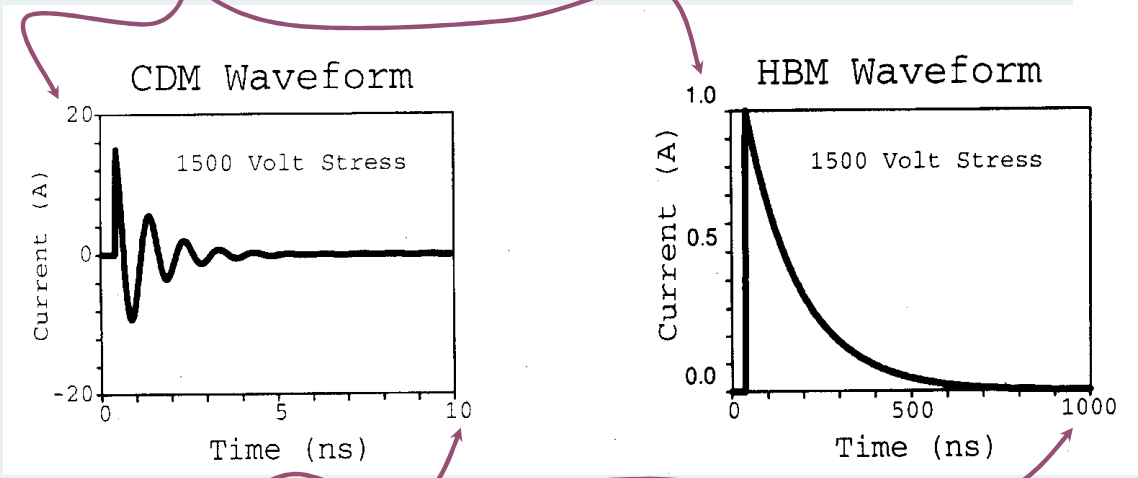


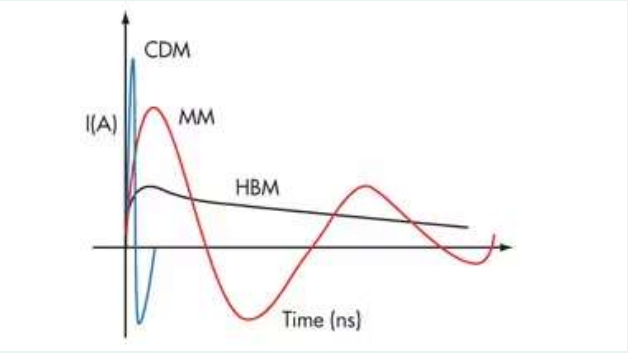
- Equivalent circuit diagram:
  - R = 0 Ω
  - C = 200 pF
  - L = 0.75 µH
- Max peak current 3.8 Amp @ 200 V and oscillation frequency specified
- Higher currents, lower voltages as compared to HBM
- Waveform is/can be alternating current

CDM

Models the discharge of a charged IC to a grounded surface

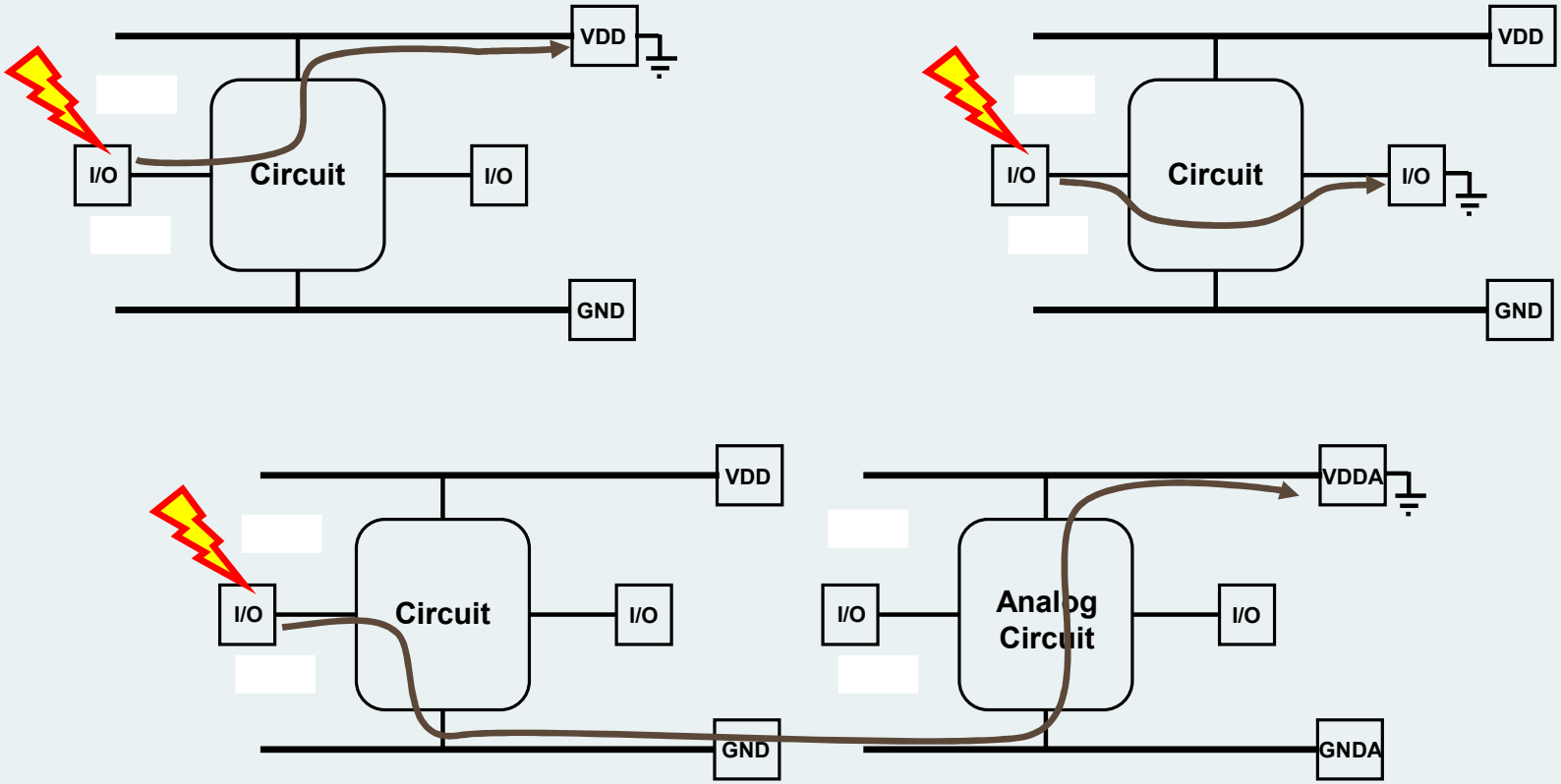
Much larger current peaks than other models



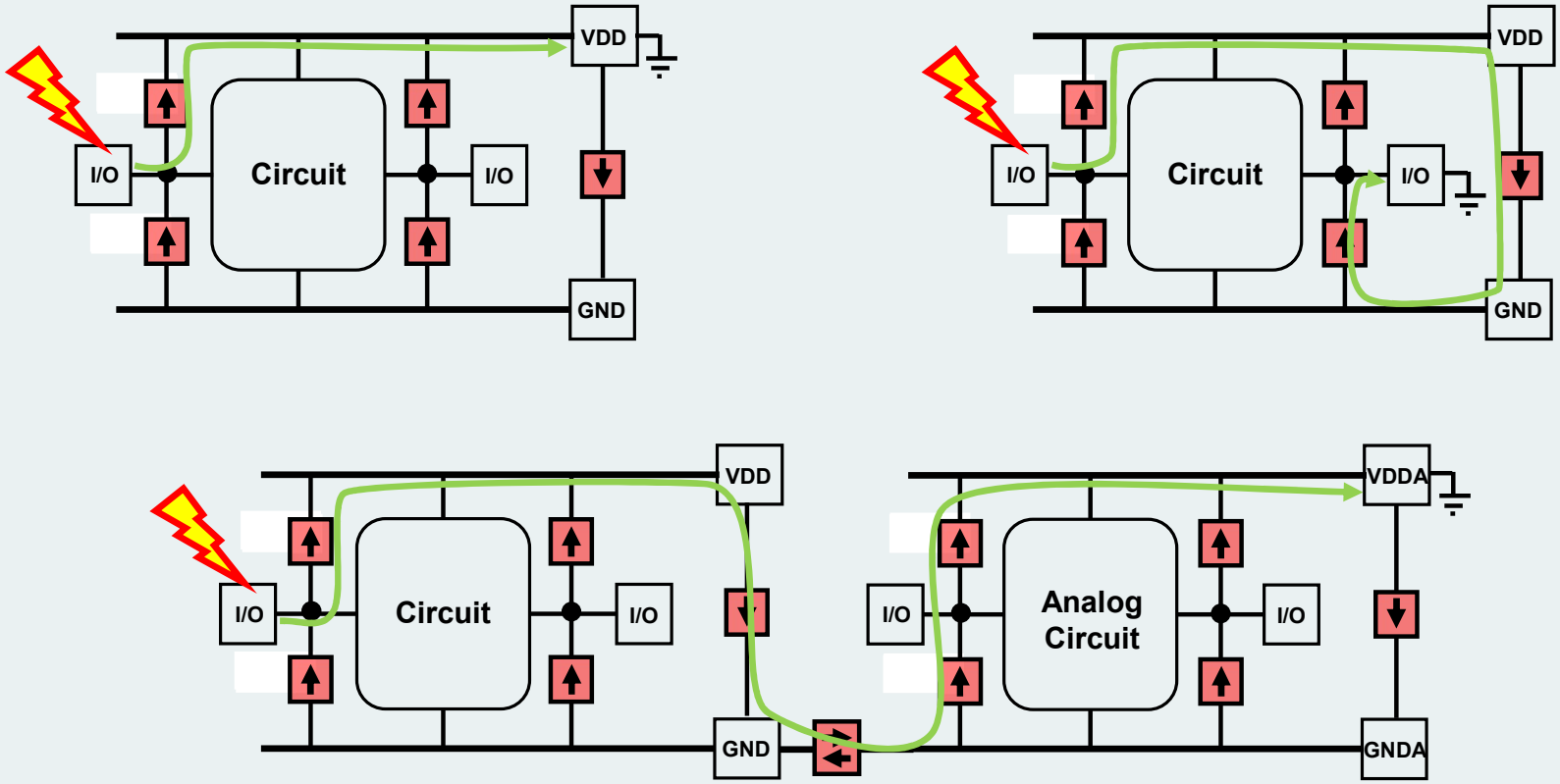


Much smaller typical times than other models

The Problem – Illustrated using HBM



The Solution – Illustrated using HBM

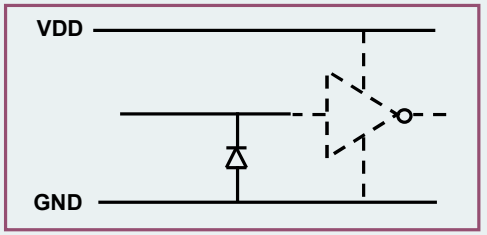


Some CDM Clamps

Single diode

Properties:

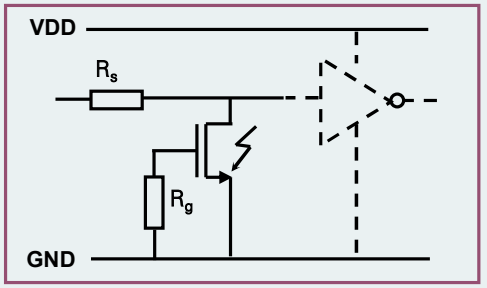
- Provides direct protection to invertor NMOS
- In reverse by avalanche current only



Single ggNMOS with / without R_S

Properties:

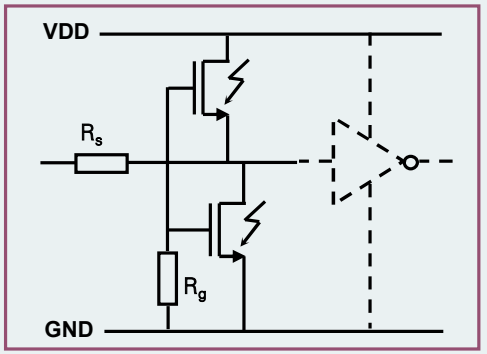
- Provides 2-way, direct protection to invertor NMOS
- Optional series resistors limits current through clamp and transistors of driving invertor: More robust solution



Double ggNMOS with / without R_S

Properties:

- Provides direct two-way protection to invertor NMOS and PMOS
- Additional series resistors limits current through clamp and transistors of driving invertor: More robust solution
- Relatively large due to the double ggNMOS's and resistor



可程式電汽規則分析

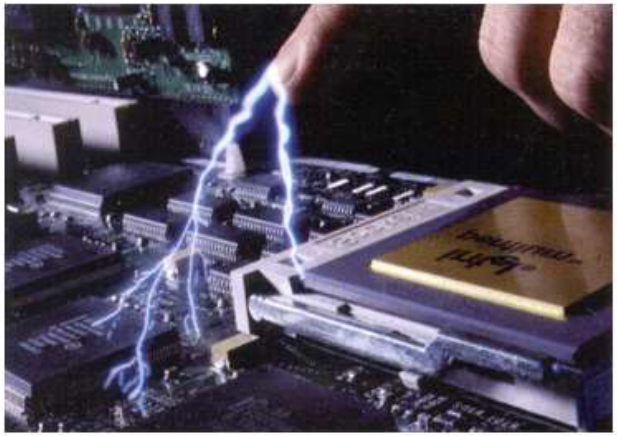
Programmable Electrical Rules Checking (PERC)

Physical Verification

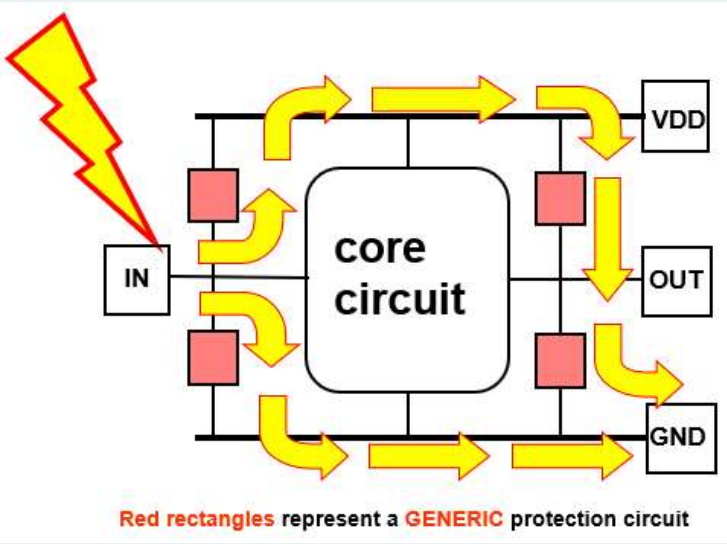
- Layout Versus Schematic
  - Text short and open
  - Device extraction error
  - Missing device terminal
  - etc
- Design Rule Checking
  - Minimum width
  - Minimum spacing
  - Minimum area
  - etc

What is PERC?

- PERC = Programmable Electrical Rule Check



static charge builds up on a person or on equipment and discharges to a device (IC, PCB, product)



Red rectangles represent a GENERIC protection circuit

- How would you program a rule which says

" Max. resistance (Rvdd1+Rvdd2 and Rvss1+Rvss2) of metal bus from IO power clamp group to the closest power clamp group ≤ X. Check needs to connect all power clamp groups like a tree"

Checks for ESD protections

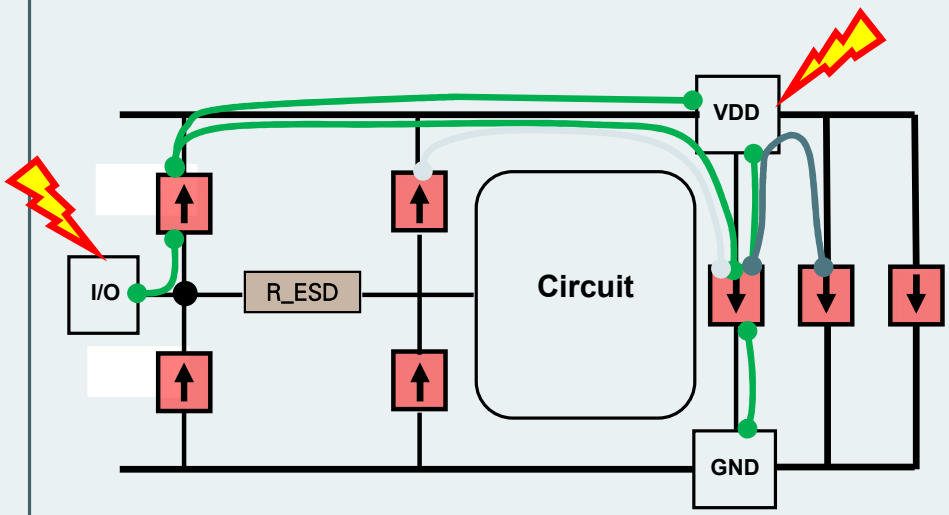
- There must be ESD devices to allow an ESD protected path from every IO/PG to every other IO/PG (existence check)
- The ESD devices need to be able to handle the ESD current; in others words … BIG (property check)
- The routing along the ESD path must be wide to handle all the current (current density check)
- The routing along the ESD path must be low resistance, so that the current chooses the desired path (P2P resistance check)

Converting the Checks into an EDA problem

- Given a netlist, find all clamp devices between P/G
- Find out “close enough” devices in the netlist, that make distributed clamping “units”
- Calculate size of clamps based on technology dependent formula
- Connect up each distributed clamp pair with a minimum-spanning tree
- …

Static P2P / CD checking in PERC

- HBM & CDM



ESD protection

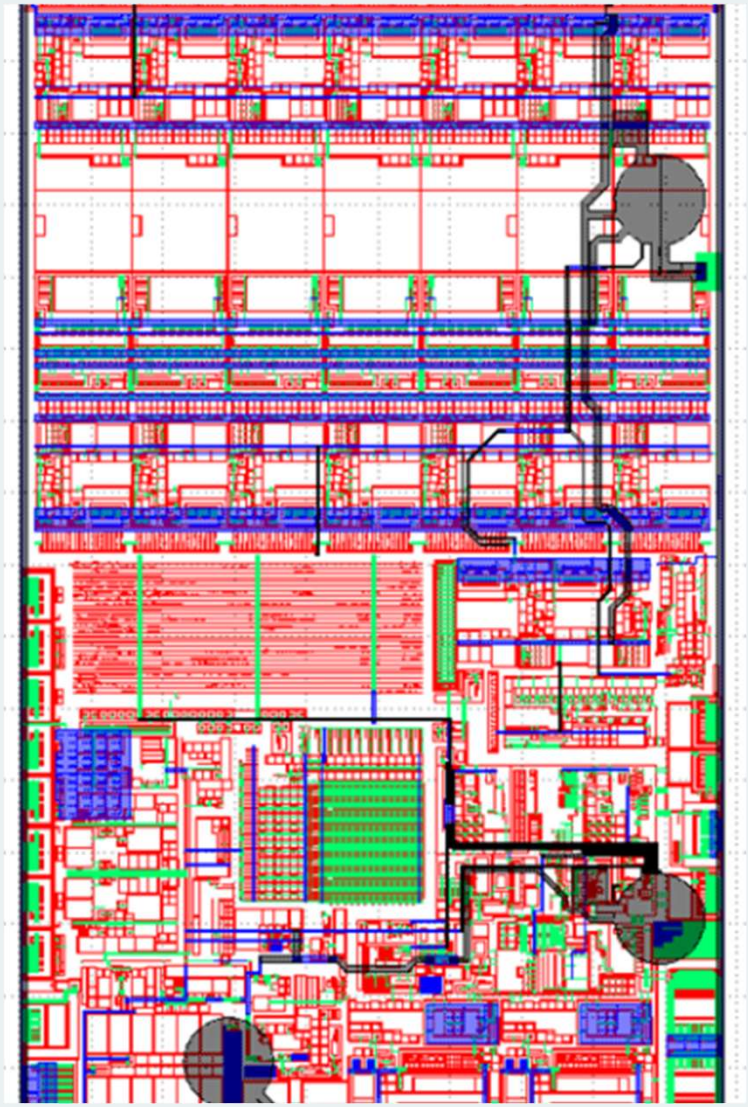
In PERC static checks, there is always a source and sink forming a path. Each source / sink can be made up of multiple devices, cell pins, or bumps. Path can be single net or multi-net

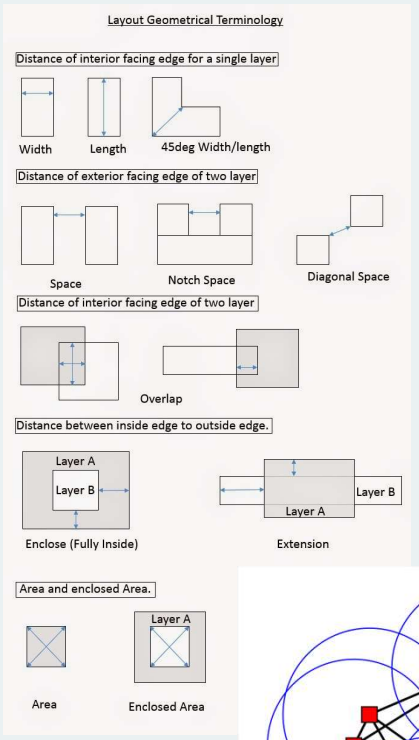
CDM problems are also checked in a "HBM-like" manner by making sure there are low res paths all through the interconnect network between ESD protections

ESD protections are identified in topological checking. They always have to exist and meet size criteria

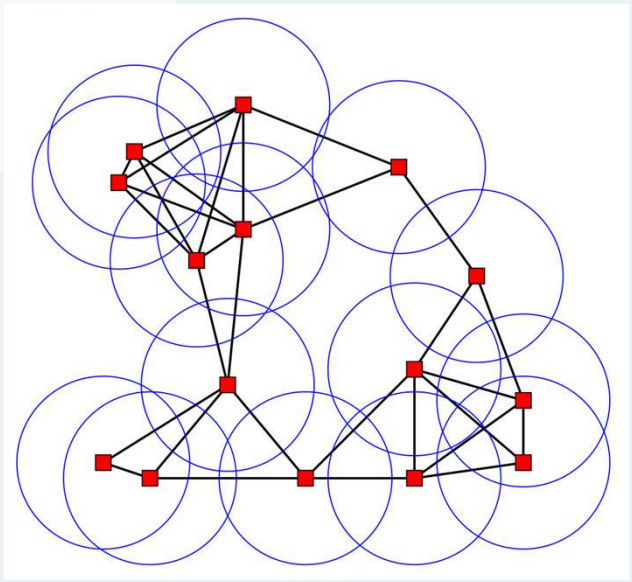
This means that for P2P / CD, we expect that design will always have ESD protection and PERC will check res on ESD interconnect.

In other words, we only really care about ESD devices and maybe a few more devices (ESD victims on I/O nets)

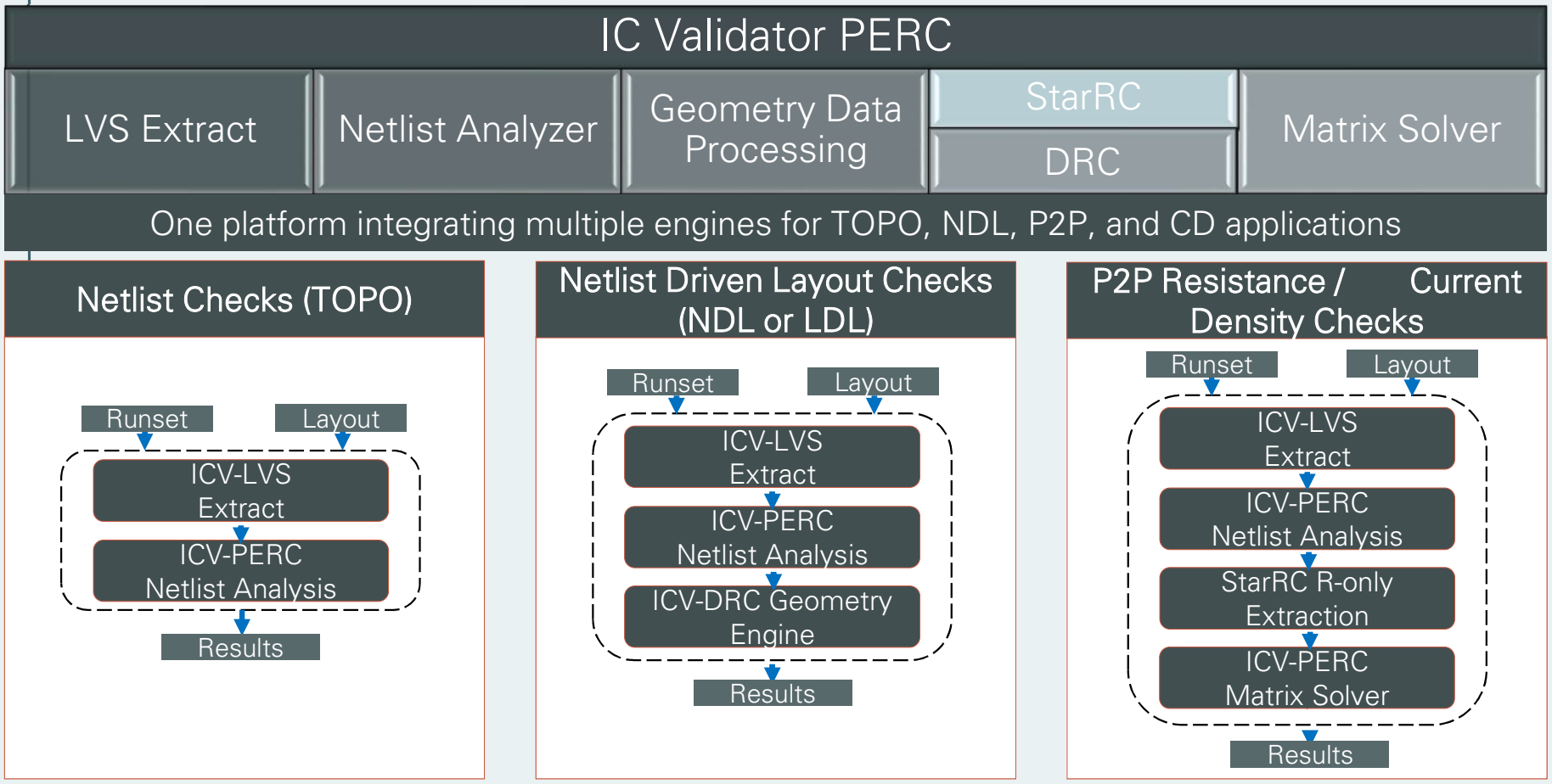




How to check all devices are protected by power clamps?



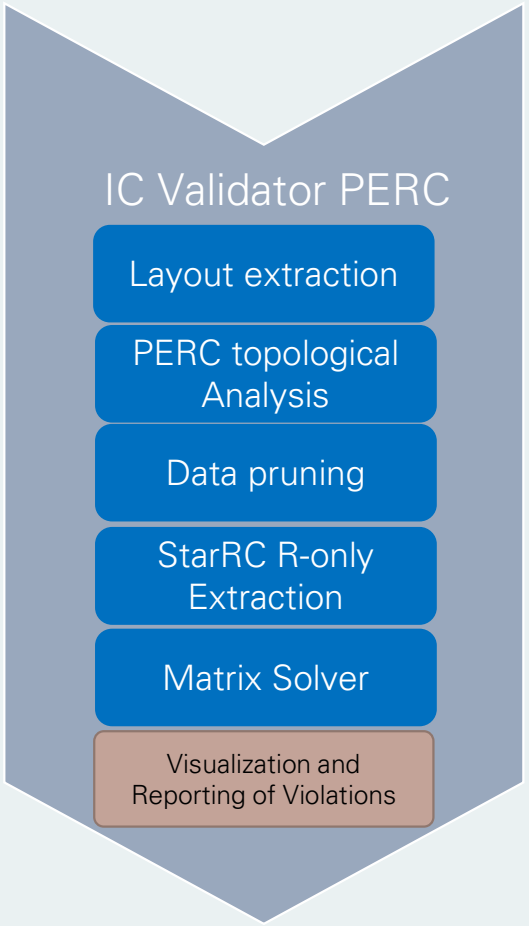
ICV PERC flows


IC Validator PERC
LVS Extract
Netlist Analyzer
Geometry Data Processing
StarRC
DRC
Matrix Solver
One platform integrating multiple engines for TOPO, NDL, P2P, and CD applications
Netlist Checks (TOPO)
Runset
Layout
ICV-LVS Extract
ICV-PERC Netlist Analysis
Results
Netlist Driven Layout Checks (NDL or LDL)
Runset
Layout
ICV-LVS Extract
ICV-PERC Netlist Analysis
ICV-DRC Geometry Engine
Results
P2P Resistance / Current Density Checks
Runset
Layout
ICV-LVS Extract
ICV-PERC Netlist Analysis
StarRC R-only Extraction
ICV-PERC Matrix Solver
Results

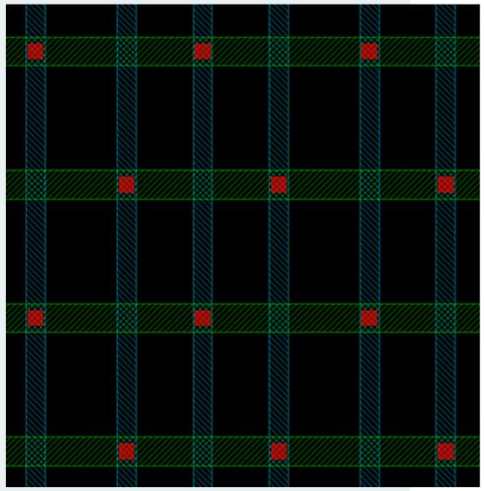
P2P flow

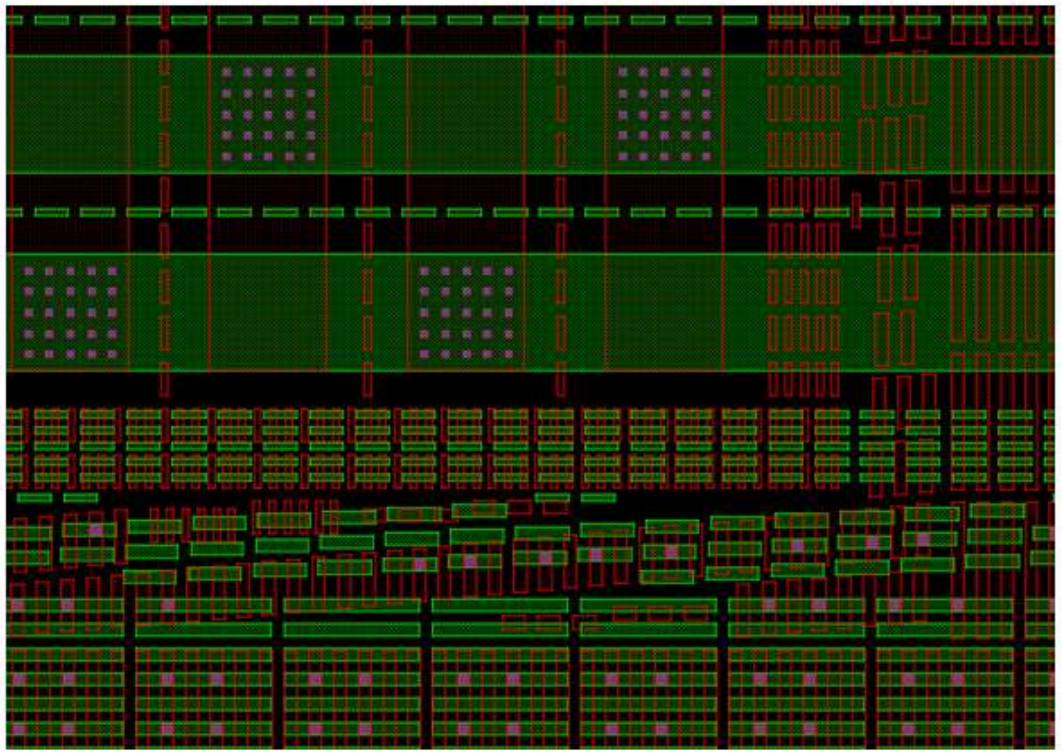
- ICV PERC is a full chip static ESD solution
- We rely on ESD circuitry definitions / descriptions (from customers or foundries), and find that circuitry in the design
- Focus on current flowing through the ESD devices → large sections of the design are irrelevant and can be pruned away
- The idea is that we focus on the ESD circuits and associated interconnects, that form source / sink pairs. This is the cornerstone of the pruning methodology

- Data pruning plays a critical role for full chip SoC closure



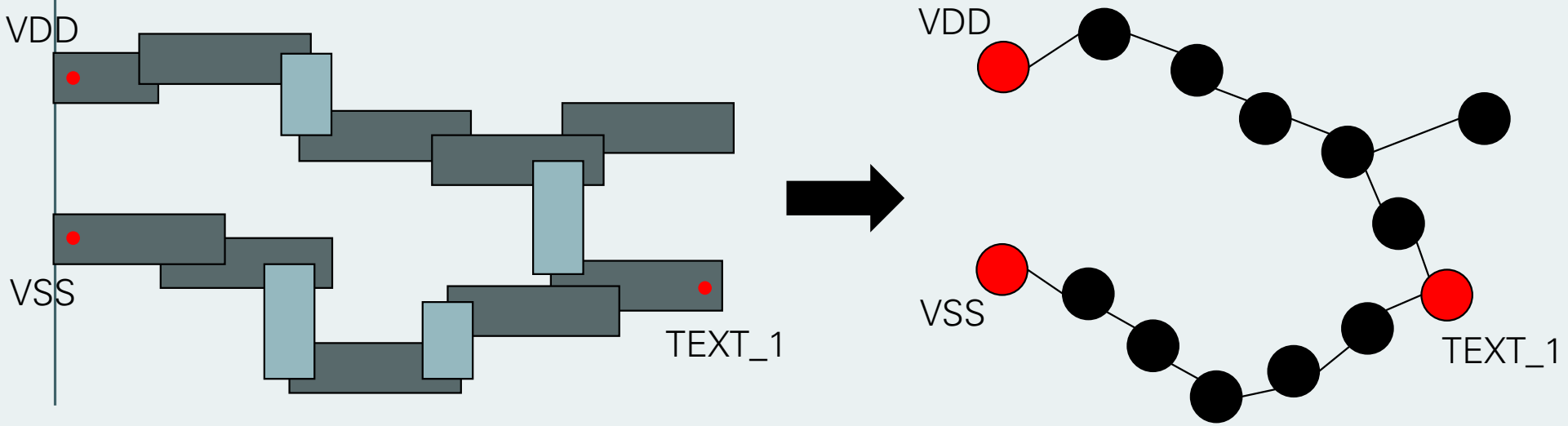
VIA reductions



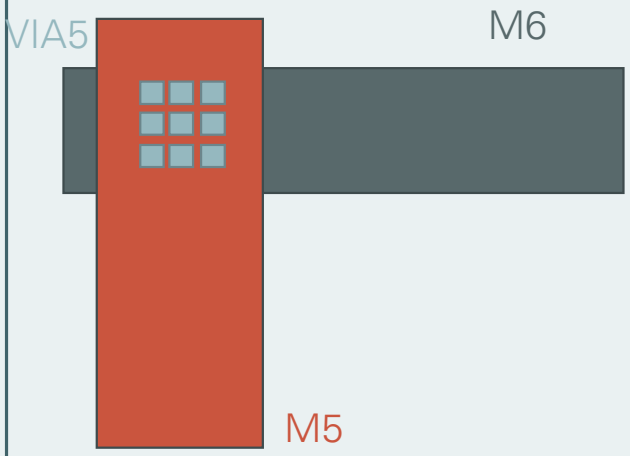


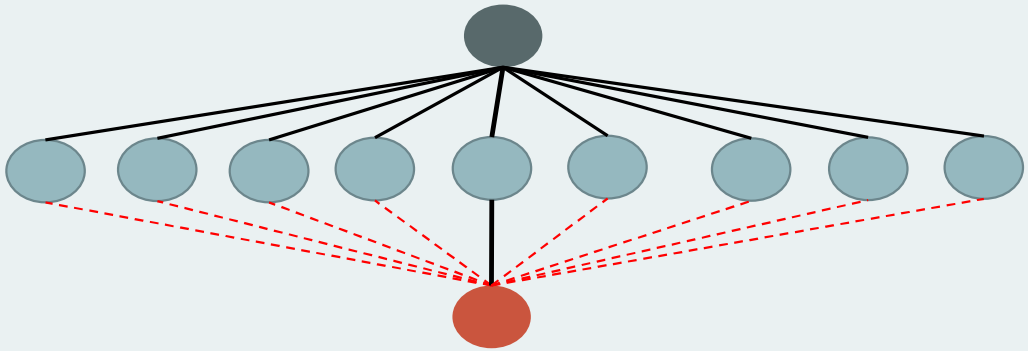
Circuit Graph

- A graph
  - Node represents polygons in the short net
  - Edge represents the polygon interactions
  - Node with text will become start/end of a path



VIA ARRAY in Graph

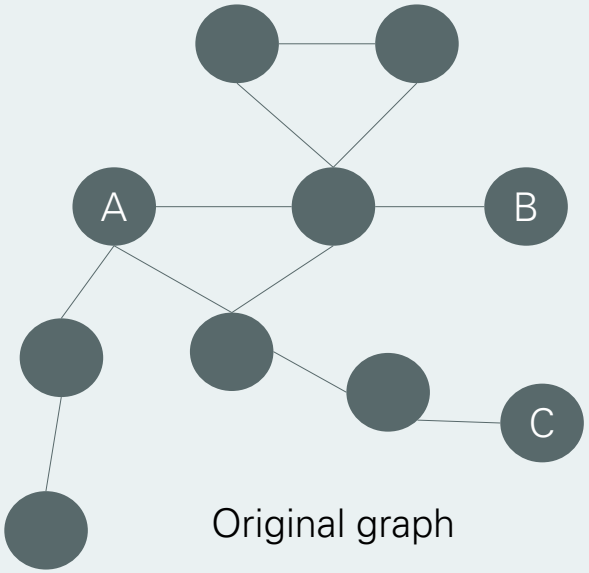




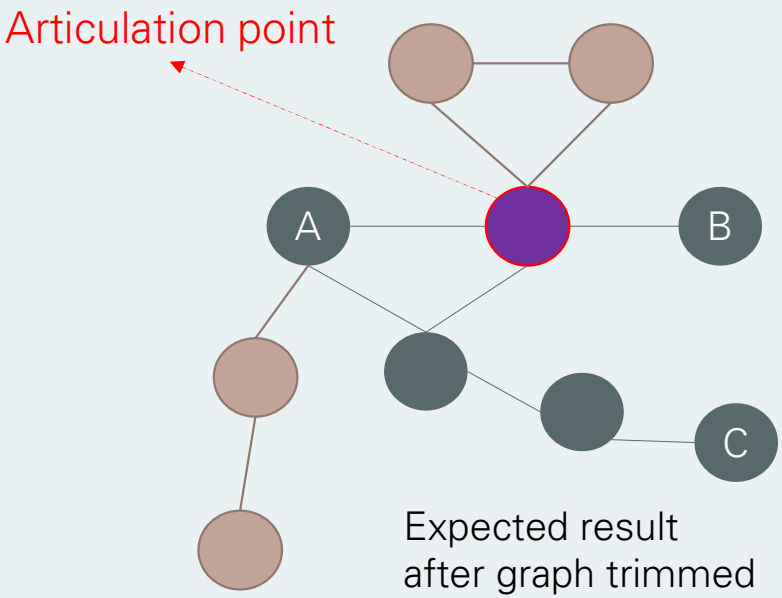
- Process as generating edges
- Reduce the graph pattern

Graph Trimming

- Given a graph, remove the nodes that are not part of the path from any text to another different text

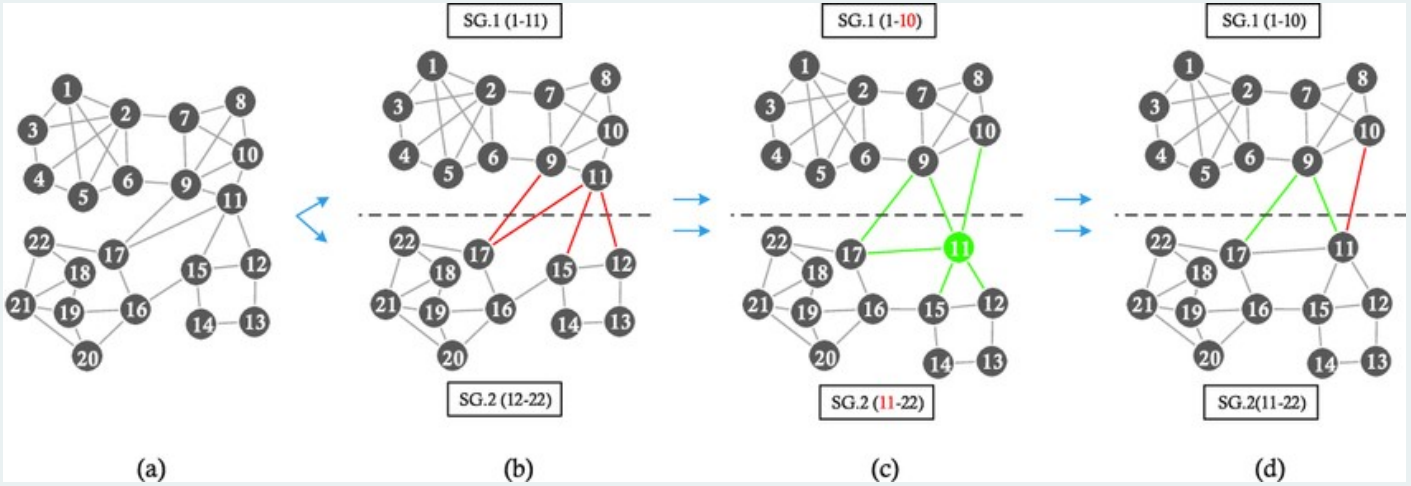


Original graph



Expected result
after graph trimmed

Flat network partition



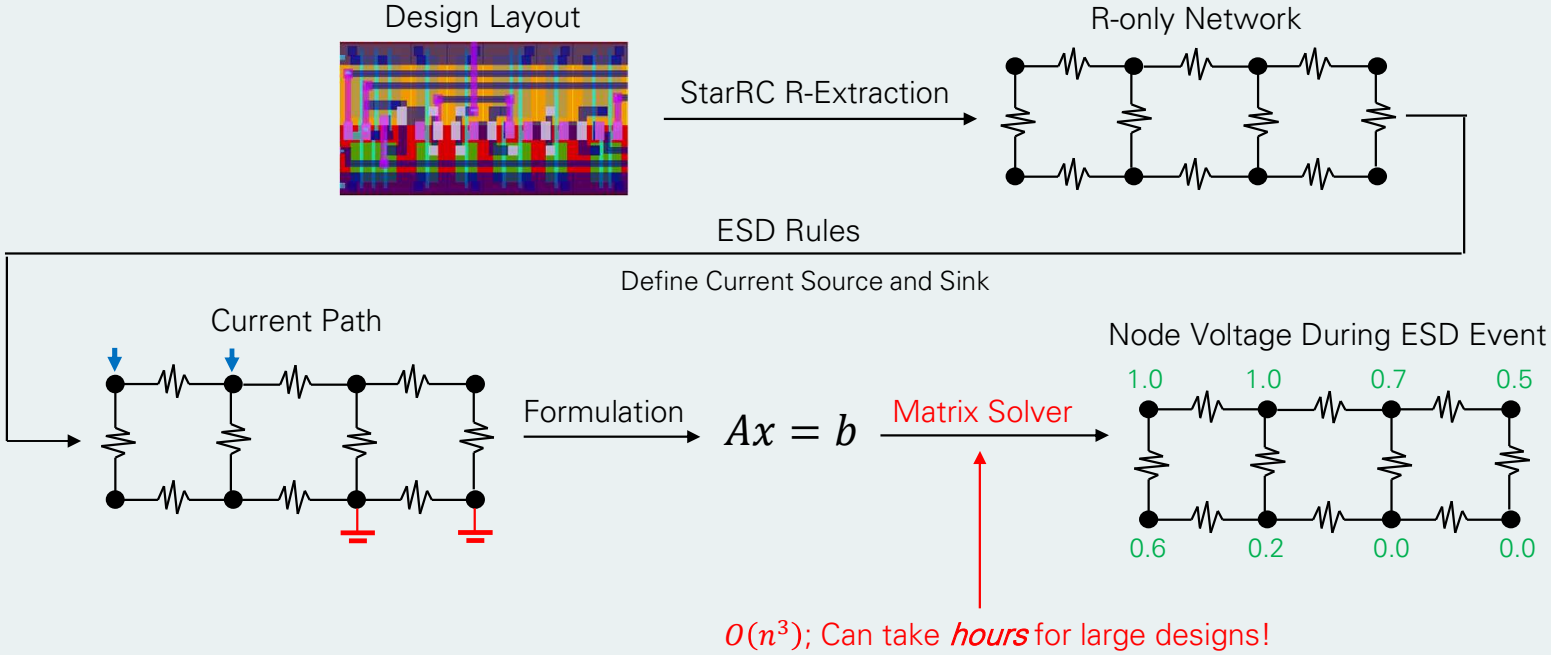
Pruning Solution for full chip static ESD checking

- ✓Good accuracy-performance balance
- ✓Pass the requirement of 20% resistance difference with reference tool (Calibre) from foundry
- ✓Runtime from days to hours

	Before pruning	After pruning
Graph node count (based on polygon connectivity, pre-parasitic-extract)	Case A: 3.5B Case B: 1.6B	Case A: 419M (-88%) Case B: 177M (-89%)
Runtime	Case A: DNF in StarRC Case B: DNF in StarRC	Case A: < 1 day Case B: < 1 day

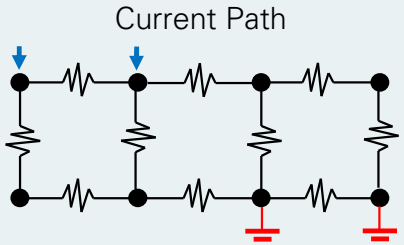
Matrix solving

- Static simulation of ESD event



Nodal Analysis and Direct Solver

- Nodal analysis
  - For each node, total inbound current equals total outbound current (Kirchhoff's current law)
- Direct solver (Gaussian elimination)
  1. Reordering (75% time)
  2. Factorization (20% time)
  3. Solving (5% time)



Nodal analysis → $Ax = b$

$$Ax = b \xrightarrow{\text{Reordering}} A_p x_p = b_p \xrightarrow[A_p = LL^T]{\text{Factorization}} A_p x_p = LL^T x_p = b_p \xrightarrow{\text{Solving}} x_p = L^{T^{-1}} L^{-1} b_p$$

(Finding the optimal elimination order)

(Eliminating variables)

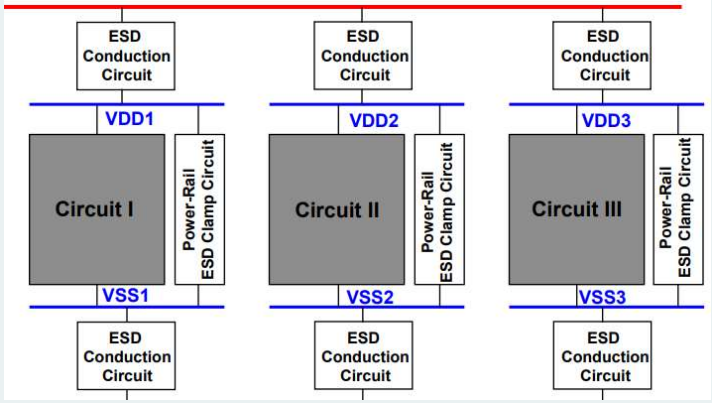
(Eliminating variables)

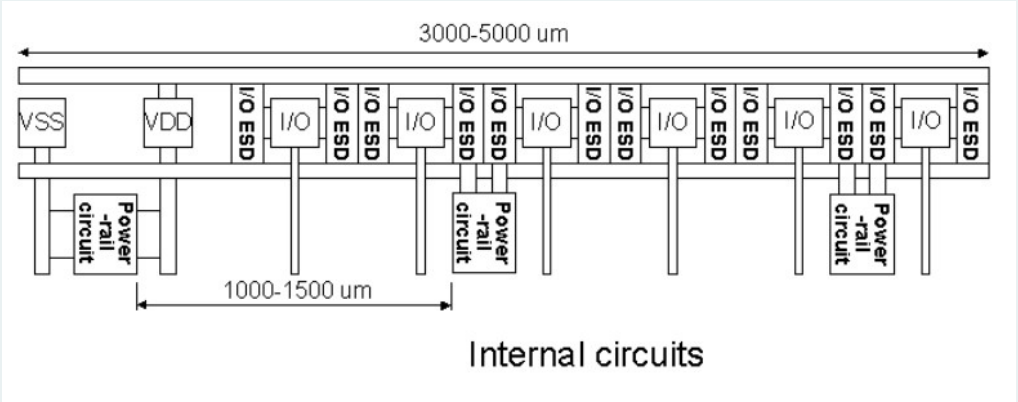
Current Density Check

- Check the point-to-point resistances of paths
- Check current densities of polygons of the paths.

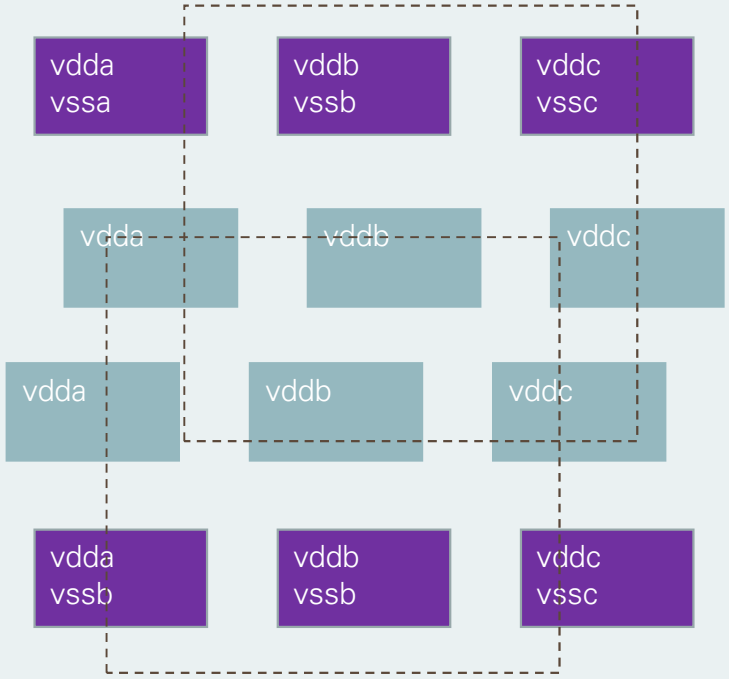
Large distance enclosure check for grouping data

- Foundry's LDL ESD rules
  - For every MOS connected directly to power/ground, there must be a corresponding power clamp
    - Deal with grouping data for applications with mixed supply voltage
    - Long distance check





Large distance enclosure check for grouping data



- Grouping data by property values, e.g.,
  - 3 power nets: vdda, vddb and vddc.

    In DRC: Property vdd has three values a, b and c.
  - 3 ground nets: vssa, vssb and vssc.

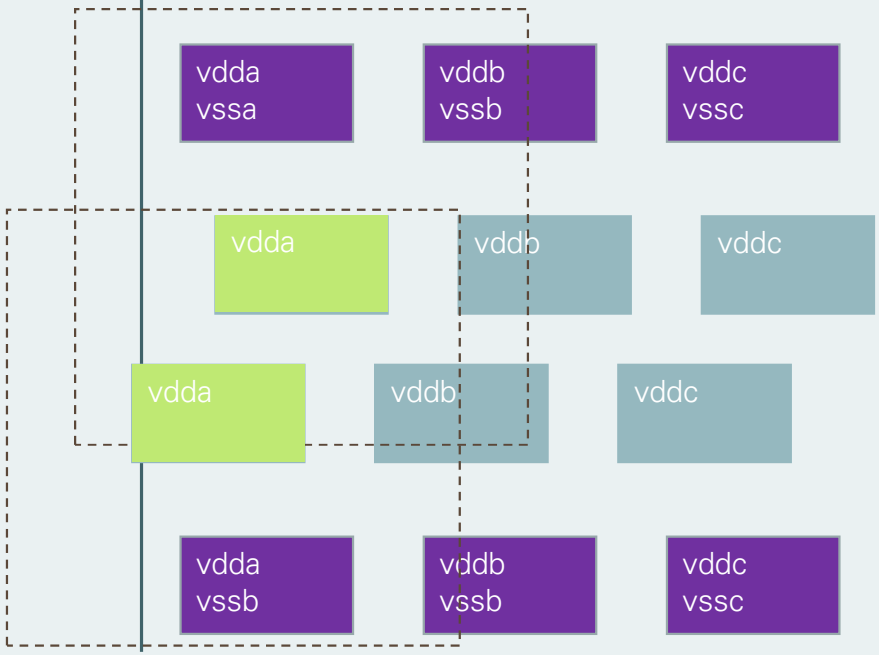
    In DRC: Property vss has three values a, b and c.

- Want to ask

  Select the gate connecting to net vddb which have no power clamp connecting to net vddb within distance D?

Select the gray vddb polygons which have no purple vddb polygon within distance D?

Large distance enclosure check for grouping data



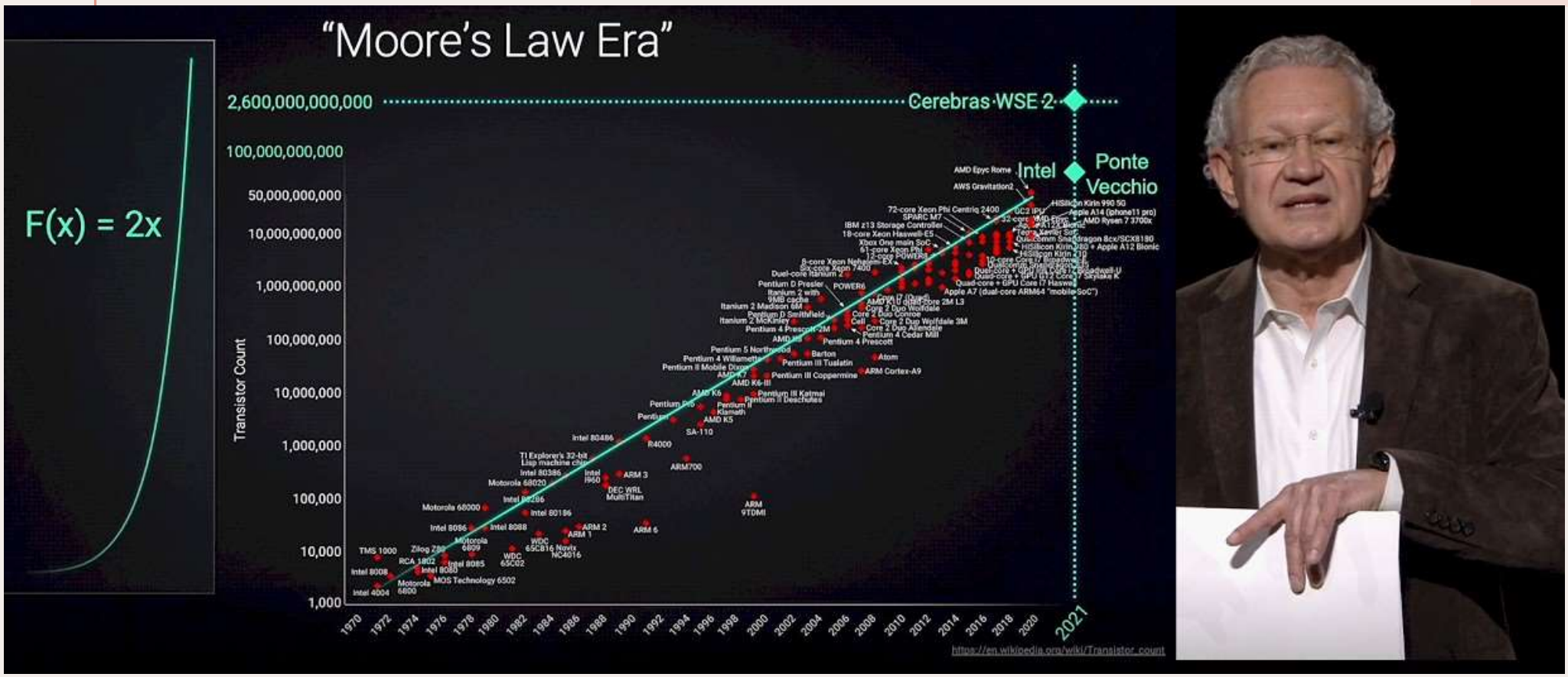
- Take power and ground nets into account together.

What are the gray vdda polygons which have no purple vdda polygon within distance D?

(vdda, vssa) and (vdda, vssb) will be considered as different groups when we take 2 types of nets (2 properties) into account together.

It means that green gates are not fully protected by two groups of power clamps

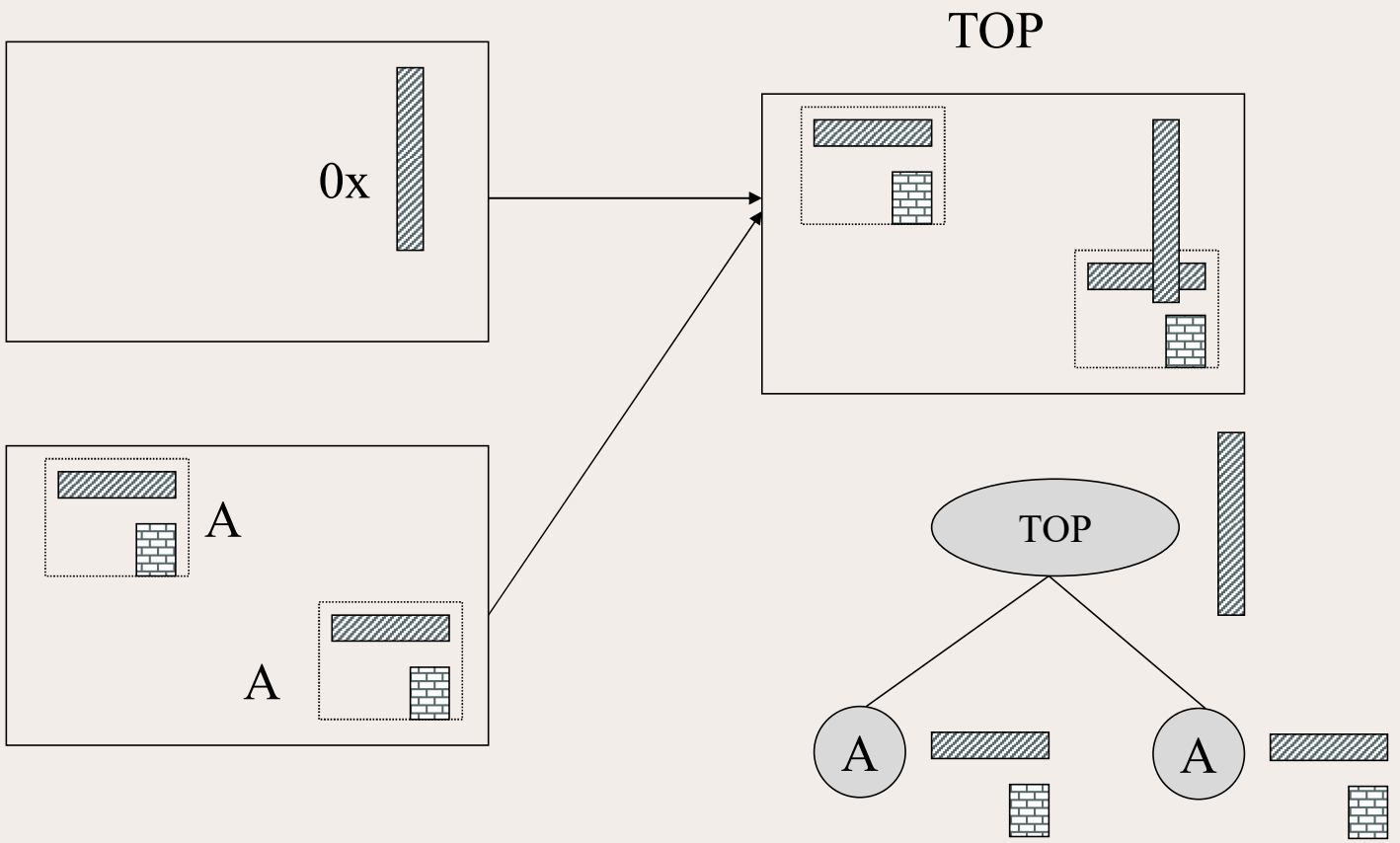
3DIC PERC 在資訊工程上的挑戰


"Moore's Law Era"
F(x) = 2x
2,600,000,000,000
Cerebras WSE 2
100,000,000,000
50,000,000,000
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
Transistor Count
Intel
Ponte Vecchio
2021
1970
1972
1974
1976
1978
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000
2002
2004
2006
2008
2010
2012
2014
2016
2018
2020
AMD Epyc Rome
AWS Gravitation2
72-core Xeon Phi Centriq 2400
SPARC M7
IBM z13 Storage Controller
18-core Xeon Haswell-E5
Xbox One main SoC
61-core Xeon Phi
12-core POWER8
8-core Xeon Nehalem-EX
Six-core Xeon 7400
Dual-core Itanium 2
Pentium D Presler
Itanium 2 with 9MB cache
Itanium 2 Madison 6M
Pentium D Smithfield
Itanium 2 McKinley
Pentium 4 Prescott-2M
AMD K8
Pentium 5 Northwood
Pentium 4 Willamette
Pentium II Mobile Dixon
AMD K7
AMD K6-III
AMD K6
Pentium Pro
Pentium
Pentium
AMD K5
SA-110
Intel 80486
R4000
TI Explorer's 32-bit Lisp machine chip
Intel 80386
Intel i960
ARM 3
Motorola 68020
DEC WRL MultiTitan
Intel 80286
Motorola 68000
Intel 80186
ARM700
ARM 9TDMI
Intel 8086
Intel 8088
ARM 2
ARM 1
ARM 6
Motorola 6809
WDC 65C816
Novix NC4016
TMS 1000
Zilog Z80
RCA 1802
WDC 65C02
Intel 8085
Intel 8080
Intel 8008
Motorola 6800
MOS Technology 6502
Intel 4004
Pentium III Tualatin
Barton
Pentium III Coppermine
Pentium III Katmai
Pentium II Deschutes
Pentium 4 Prescott
Pentium 4 Cedar Mill
Core 2 Duo Allendale
Core 2 Duo Wolfdale 3M
Cell
Core 2 Duo Conroe
Core 2 Duo Wolfdale
AMD K10 quad-core 2M L3
POWER6
Apple A7 (dual-core ARM64 "mobile-SoC")
Quad-core + GPU Core i7 Haswell
Dual-core + GPU Core i7 Broadwell-U
Quad-core + GPU Core i7 Skylake K
Atom
ARM Cortex-A9
Apple A14 (iphone11 pro)
AMD Ryzen 7 3700x
https://en.wikipedia.org/wiki/Transistor_count

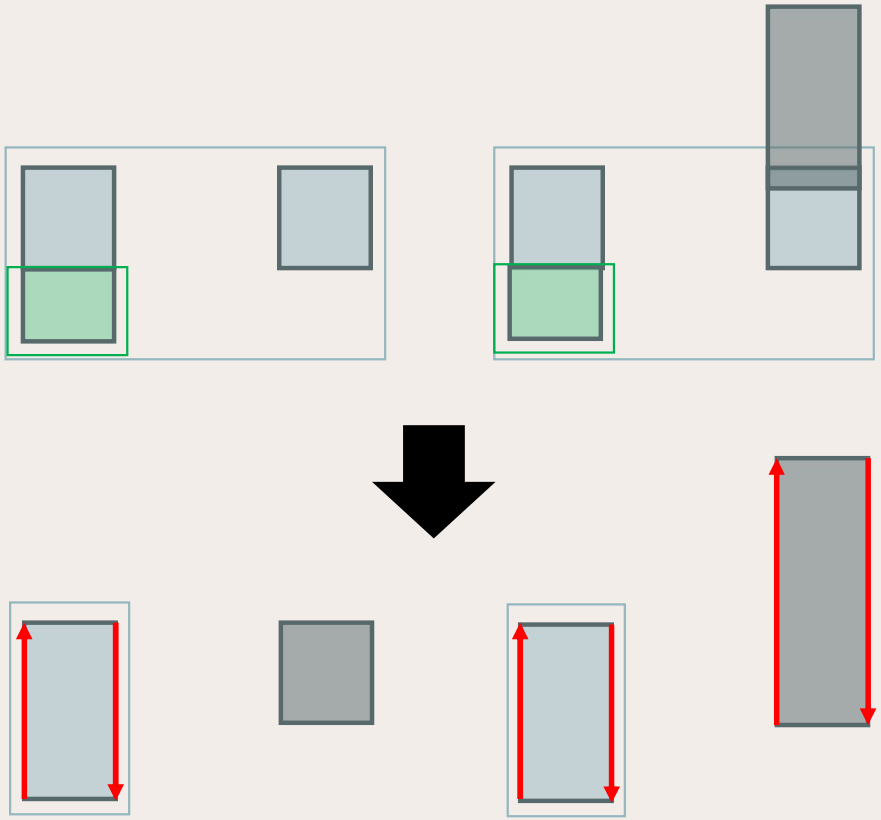
How to handle large layout Data?

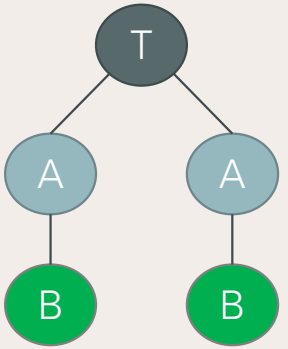
Cell Hierarchy

- Reduce runtime.
  - Avoid doing duplicate work for the same cell.
    - It applies to both the current command and the next command which takes this command's output as input.
- The most important thing to keep in mind:
  - Each cell can be placed many times but there's only one place to store each cell's results.


TOP
0x
A
A
TOP
A
A

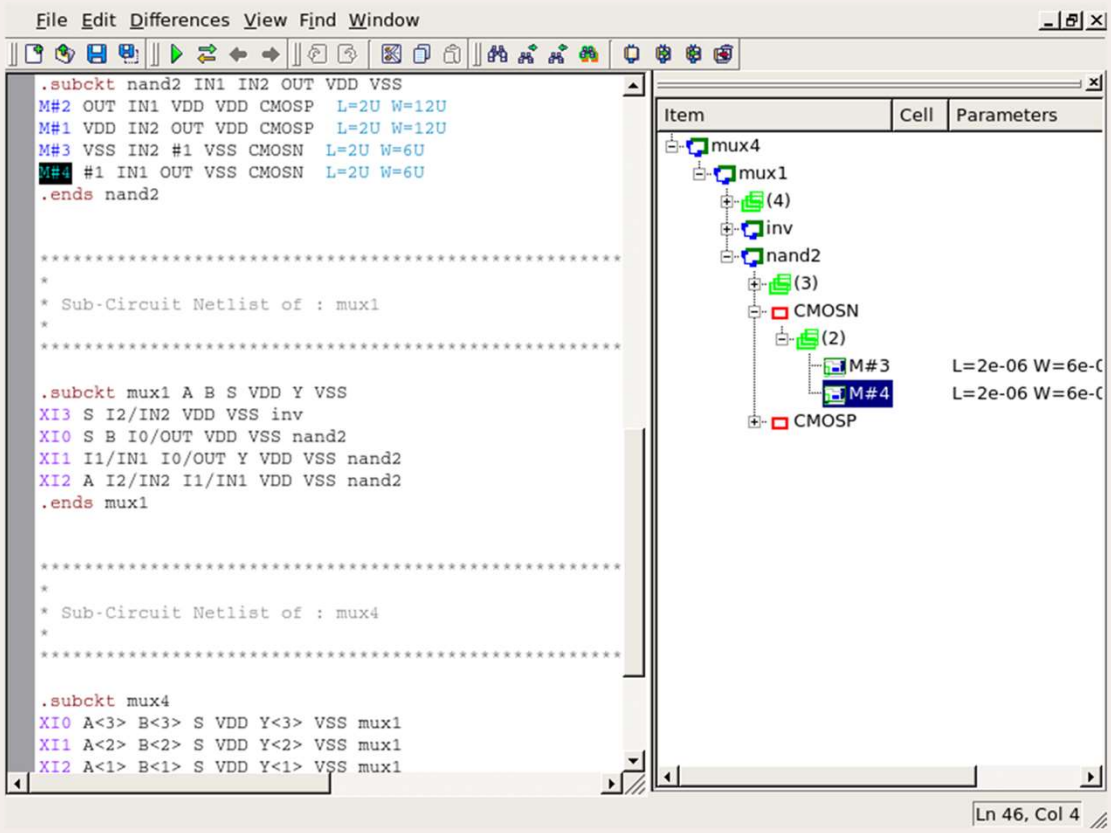
Example: Calculate Polygon Length in Hierarchy



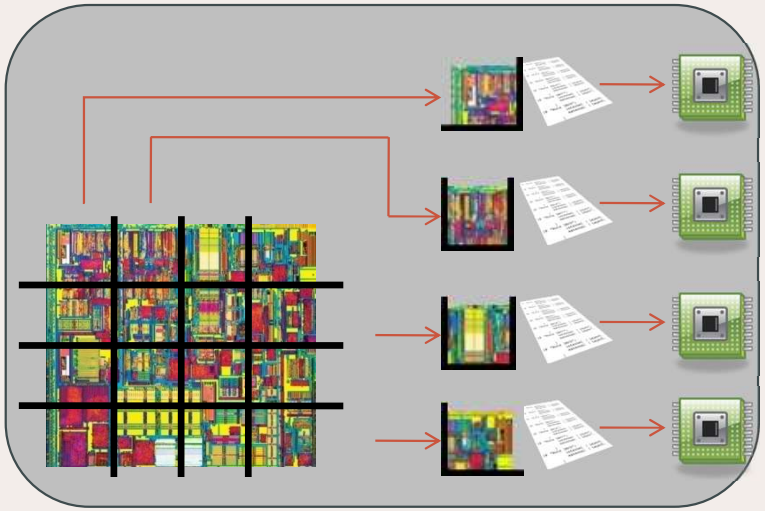


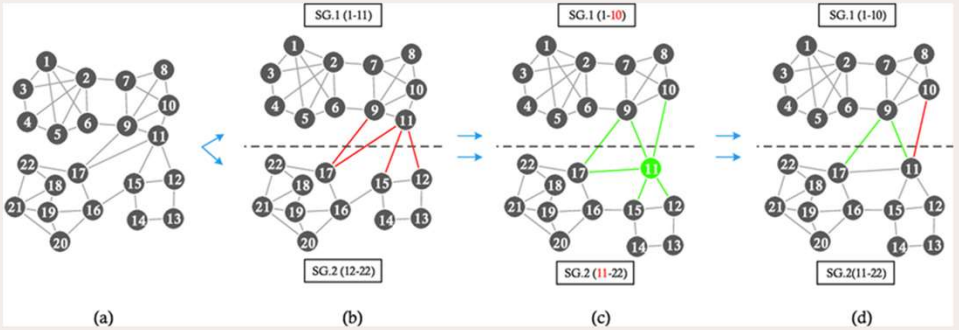
Cell B becomes an empty cell.

SPICE Netlist is Also Hierarchical



Flat Data Partition



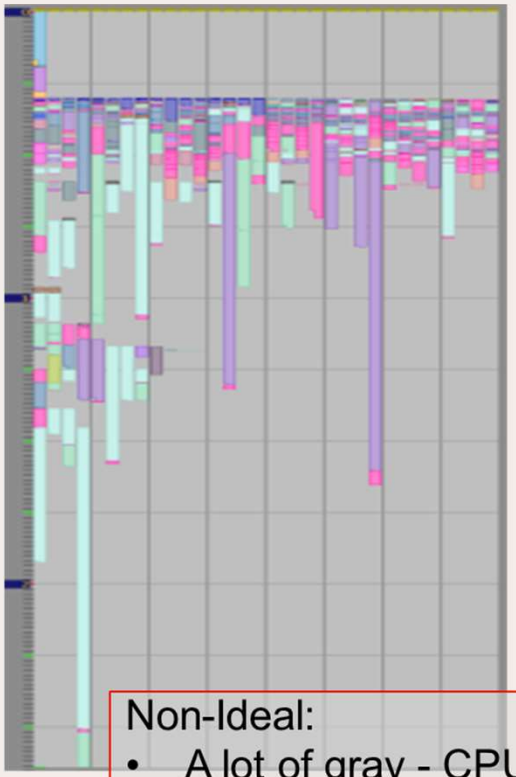


Transistor-Level to Cell-Level

Parallel computing

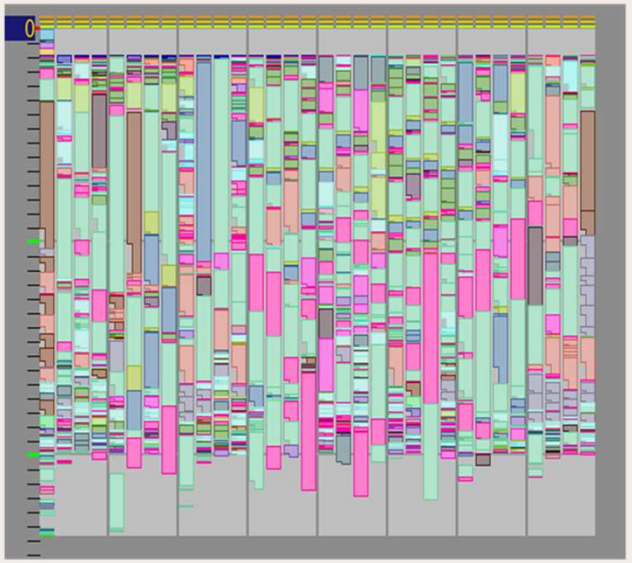
- Threading & OpenMP
- MPI
- Cloud Computing
- GPU CUDA
- …

LSF + NFS + Pthread + OpenMP



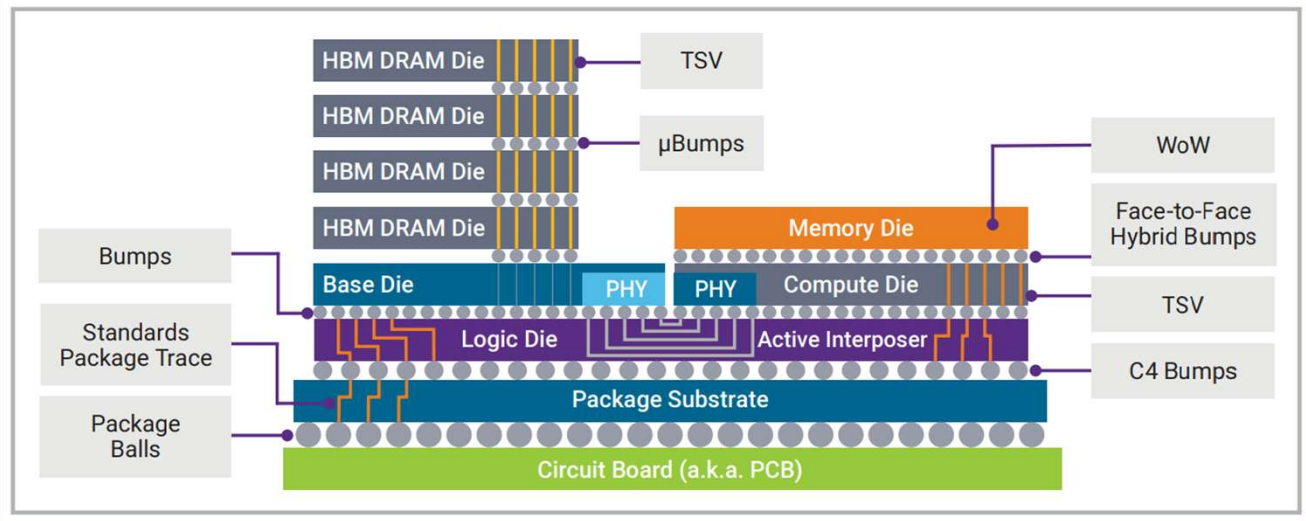
Non-Ideal:
- A lot of gray - CPUs sitting idle
- A few long running commands limit performance

Ideal:
- Does not have many gray areas—All CPUS being used
- No long serial chains



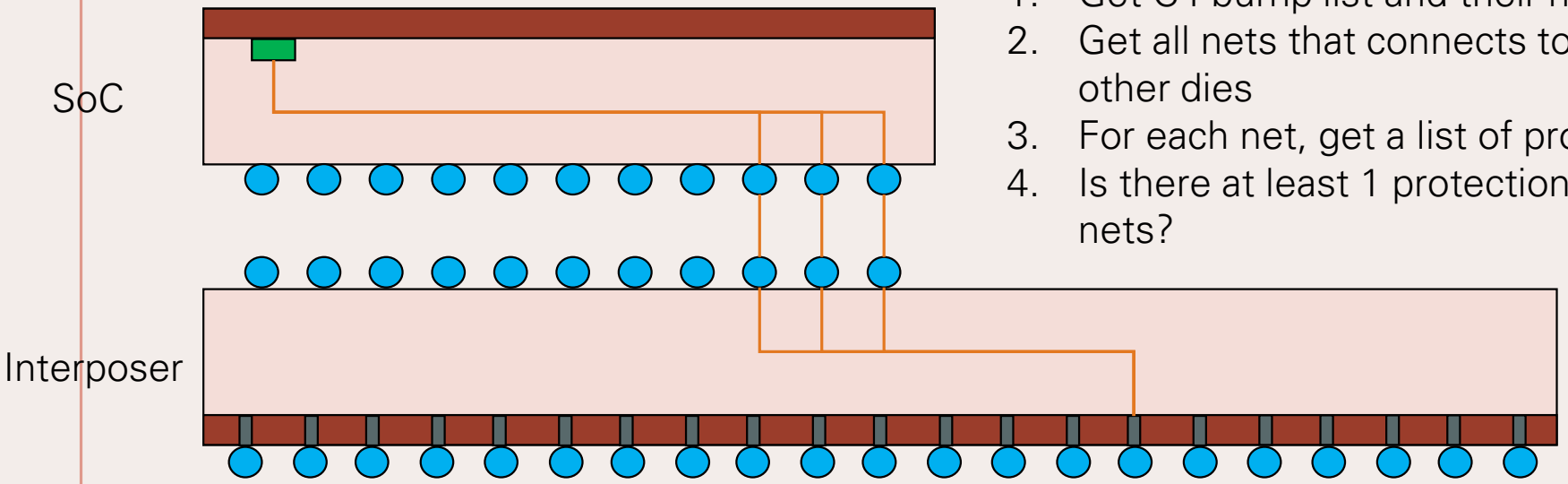
Reuse 2D (IP block) results

- Cross-Die CD/P2PR
- Cross-Die Netlist and Layout Check



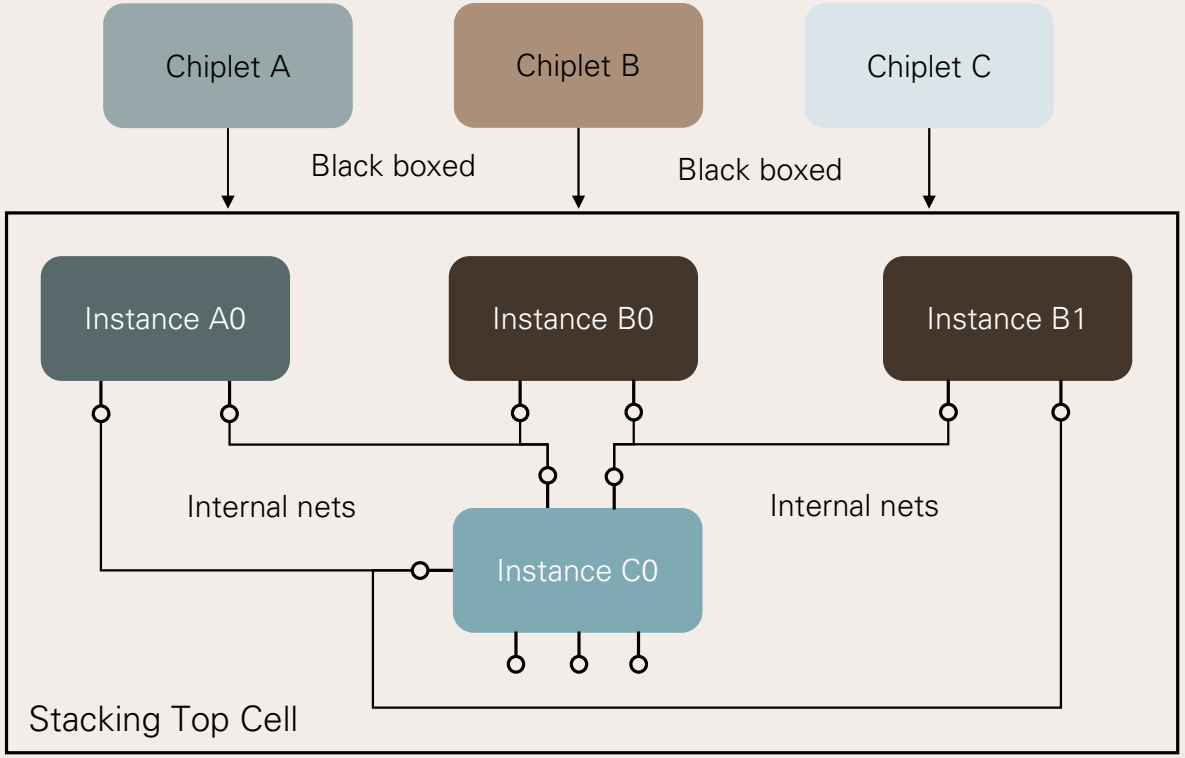
TOPO Flow Walkthrough

- For each C4 bump, a protection must be present



1. Get C4 bump list and their net
2. Get all nets that connects to C4 bump on other dies
3. For each net, get a list of protections on it
4. Is there at least 1 protection on any of the nets?

Stacking Netlist



3DIC Rule Checks

more data, larger hierarchy, and more checks

- How to calculate cross-die P2PR?
- How to calculate cross-die large distance coverage of power clamps?
- How to merge and query cross-die netlists

VUE for ICV PERC – Debug for Huge Data

Overview of IO/PG ESD Design

Summary of Clamp Network

Power	Ground	Clamp Type	Width (um)
VDDQ	VSS	Single	14288.16
VDDQLP	VSS	Single, Cascoded	14420.06

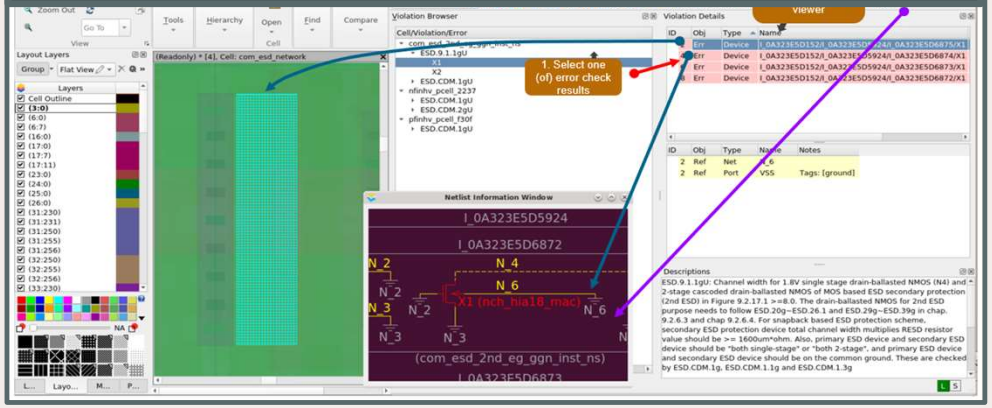
Summary of I/O ESD Network

I/O	Power	Ground	Primary Up	Primary Down	Secondary Up	Secondary Down	Clamp Type	Width (um)
BP_DAT0	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT1	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT10	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT2	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT3	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT4	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT5	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT6	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT7	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT8	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16
BP_DAT9	VDDQ	VSS	PRIMARYUPDIO	PRIMARYDOWNDIO	SECONDARYUPDIO	SECONDARYDOWNDIO	Single	14288.16

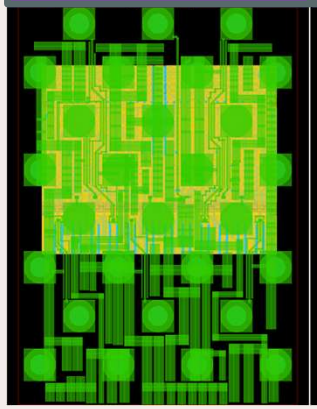
Summary of Power / Ground / IO Nets

Design Power Net definition(s) -> [VDD, VDDQ, VDDQLP]
Design Ground Net definition(s) -> [VSS]
Design I/O Net definition(s) -> [BP_DAT0, BP_DAT1, BP_DAT10, BP_DAT2, BP_DAT3, BP_DAT4, BP_DAT5, BP_DAT6, BP_DAT7, BP_DAT8, BP_DAT9]

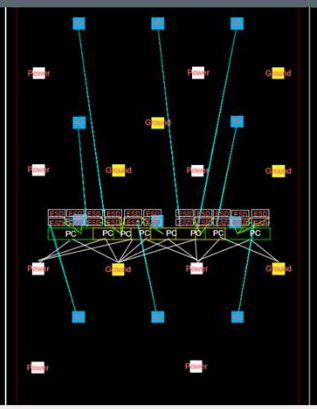
Topological / Layout ESD Error Debug



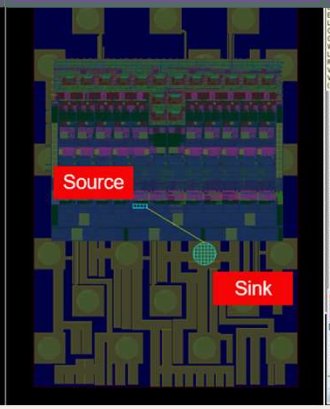
Layout View



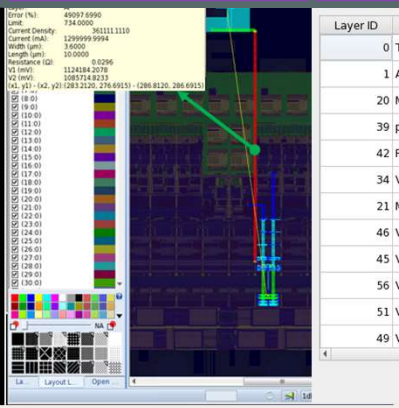
ESD Network Vis (UD)



Single ESD Path View



P2P/CD Heatmap View



Resistance Contribution by Layer

Layer ID	Name	Type	Contribution (%)	R (Ω)
0	Total		100.000000	1.281428
1	AP	Conducting	80.904368	1.036731
20	M14	Conducting	6.760593	0.086632
39	p_odtap_io	Via	3.604074	0.046184
42	RV	Via	1.587084	0.020337
34	VD_MD_OD_P_IO	Via	1.029957	0.013198
21	M15	Conducting	0.552552	0.007081
46	VIA3	Via	0.528281	0.006770
45	VIA2	Via	0.528186	0.006768
56	VIA13	Via	0.380978	0.004882
51	VIA8	Via	0.373326	0.004784
49	VIA6	Via	0.372906	0.004779

Close

EDA 產業的發展方向

Buzz words

- Cloud Computing
- IOT
- GPU
- AUTOMOBILE
- Cypto
- BlockChain
- AI – Deep Learning
- AI – GenAI
- 3D-IC


tsmc

Buzz words

- Cloud Computing
- IOT
- GPU
- AUTOMOBILE
- Cypto
- BlockChain
- AI – Deep Learning
- AI – GenAI
- 3D-IC

Buzz words in EDA

- Cloud Computing
  - Only a few customers adopt this. Safety is the concern.
- GPU
  - Only a few customers adopt this. C/P ratio is the concern.
- AI – GenAI
  - Synopsys DSO.ai
  - Huge data, small number of cases
- 3D-IC
  - CoWoS (2012), InFO (2016), SoIC (~)
  - N5, N3, N2, A16

EDA 業界的工作日常

工作機會

- MTK, Qualcomm, TSMC, Google, 其他EDA公司和 IC 設計公司.
- EDA 背景的學生少 (EDA 無聊?)
- 敝公司的工程師有EDA背景的也不多

EE or CS ?

- 電子學知識是加分但非必要
- 效能改進
- 系統整合
- 掌握新技術

Thank you