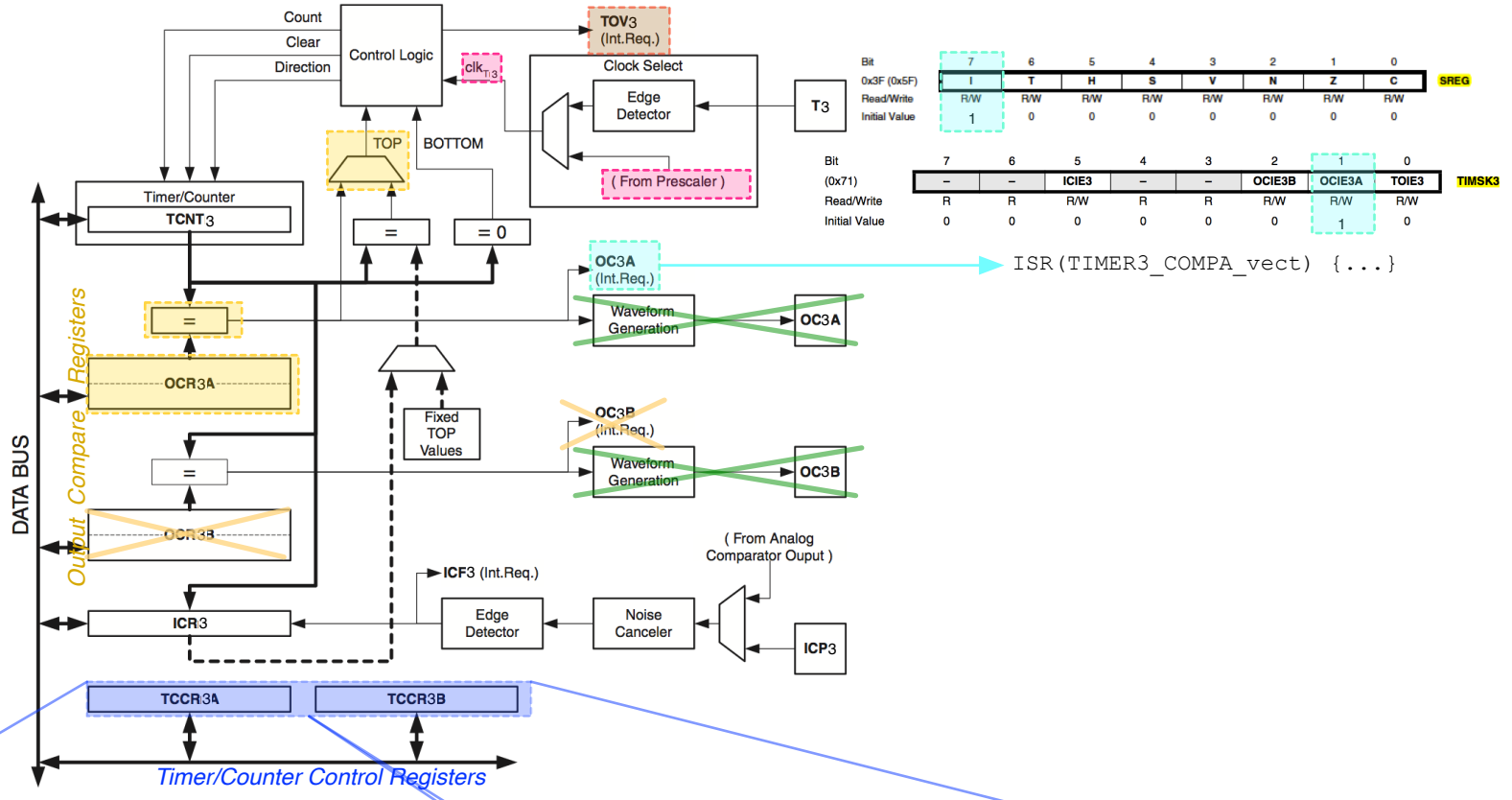
Scheduling an Interrupt Service Routine on Timer3

SEng 5832 minilab

Figure 16-1. 16-bit Timer/Counter block diagram (Note:).



Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0	
(0x71)	–	–	ICIE3	–	–	OCIE3B	OCIE3A	TOIE3	TIMSK3
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	1	0	

Bit	7	6	5	4	3	2	1	0
(0x80)	COM3A1	COM3A0	COM3B1	COM3B0	–	–	WGM31	WGM30
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ICNC3	ICES3	–	WGM33	WGM32	CS32	CS31	CS30
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	1	1	0	1

Table 16-2. Compare Output mode, non-PWM.

COMnA1/COMnB1	COMnA0/COMnB0	Description
0	0	Normal port operation, OCnA/OCnB disconnected.
0	1	Toggle OCnA/OCnB on Compare Match.
1	0	Clear OCnA/OCnB on Compare Match (Set output to low level).
1	1	Set OCnA/OCnB on Compare Match (Set output to high level).

Table 16-5. Waveform Generation mode bit description (1).

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter mode of operation	TOP	Update of OCR3x at	TOVn flag set on
4	0	1	0	0	CTC	OCR3A	Immediate	MAX

Table 16-6. Clock Select bit description.

CSn2	CSn1	CSn0	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$clk_{I/O}$/1 (No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)