High-Speed Ring Oscillator based Sensors for Remote Side-Channel Attacks on FPGAs

Joseph GRAVELLIER (EMSE)
Jean-Max DUTERTRE (EMSE)
Yannick TEGLIA (THALES)
Philippe LOUBET-MOUNDI (THALES)

Laboratoire de Sécurité des Architectures et des Systèmes,
F-13541 Gardanne France
Thales - 13600 La Ciotat, France

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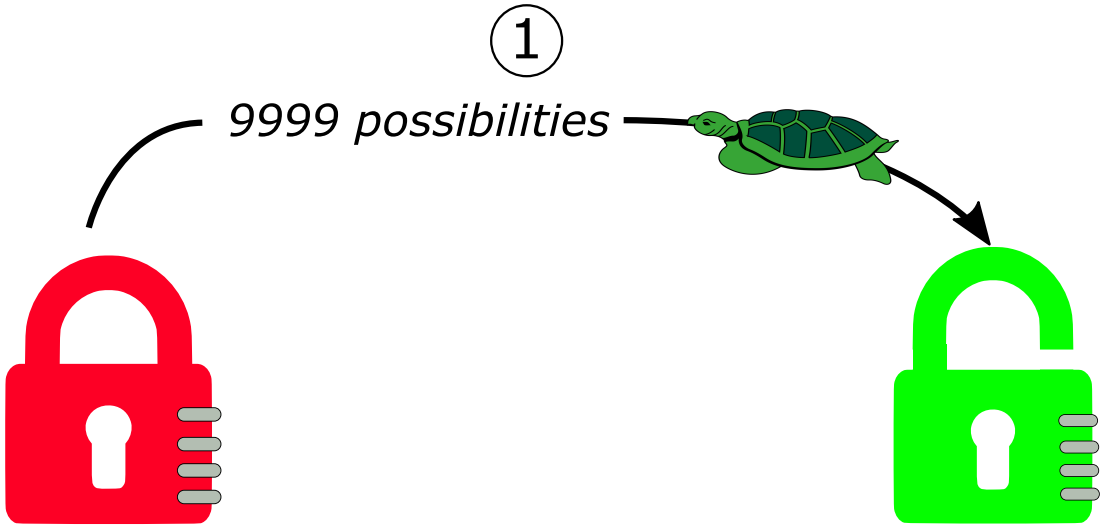
Context: What is side-channel ?

Example: Padlock

- Two ways to crack the padlock:
  1. Brute Force all the combinations.
  2. Listen to padlock clicks.



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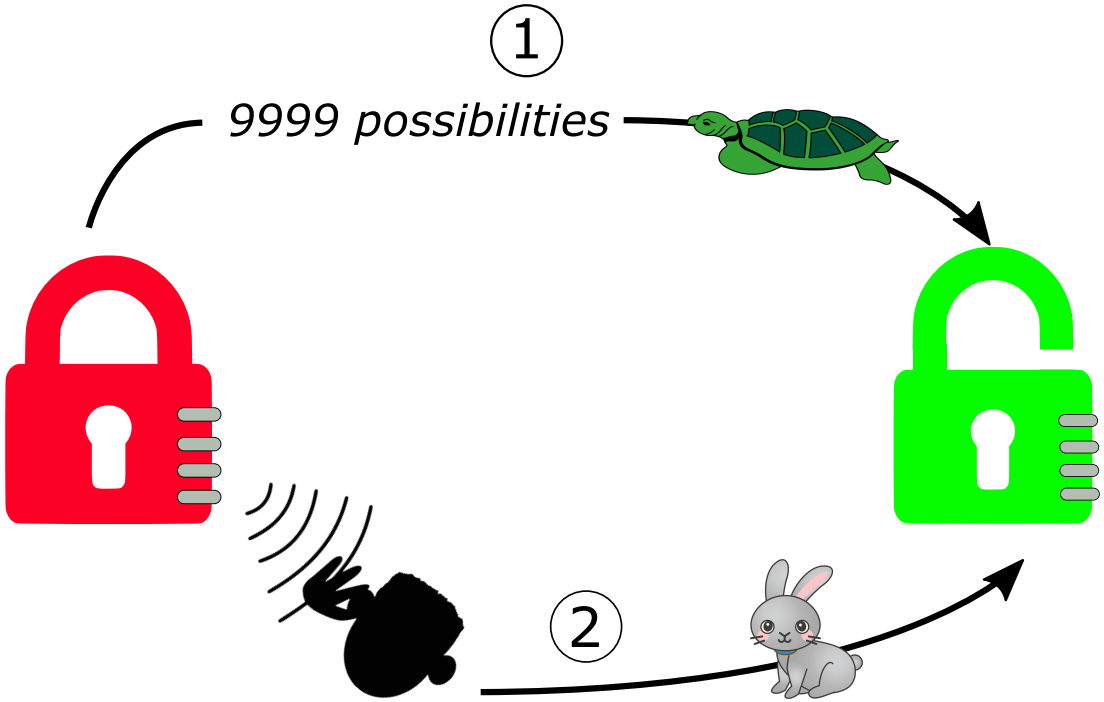

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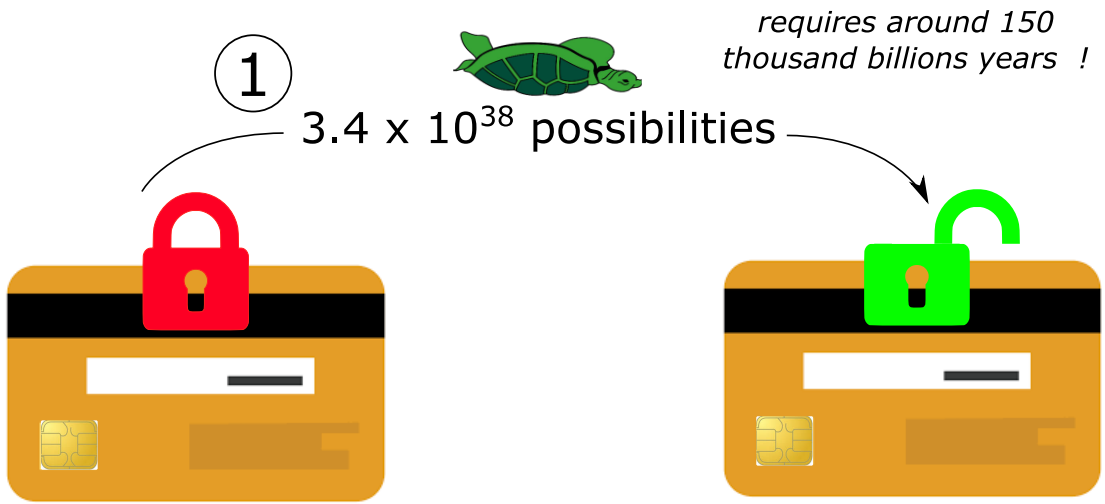
Use case: Smart Card

- Retrieve a credit card secret key ? :
  1. Using Brute Force → impossible.
  2. Using power measurement → Yes, because the secret leaks !



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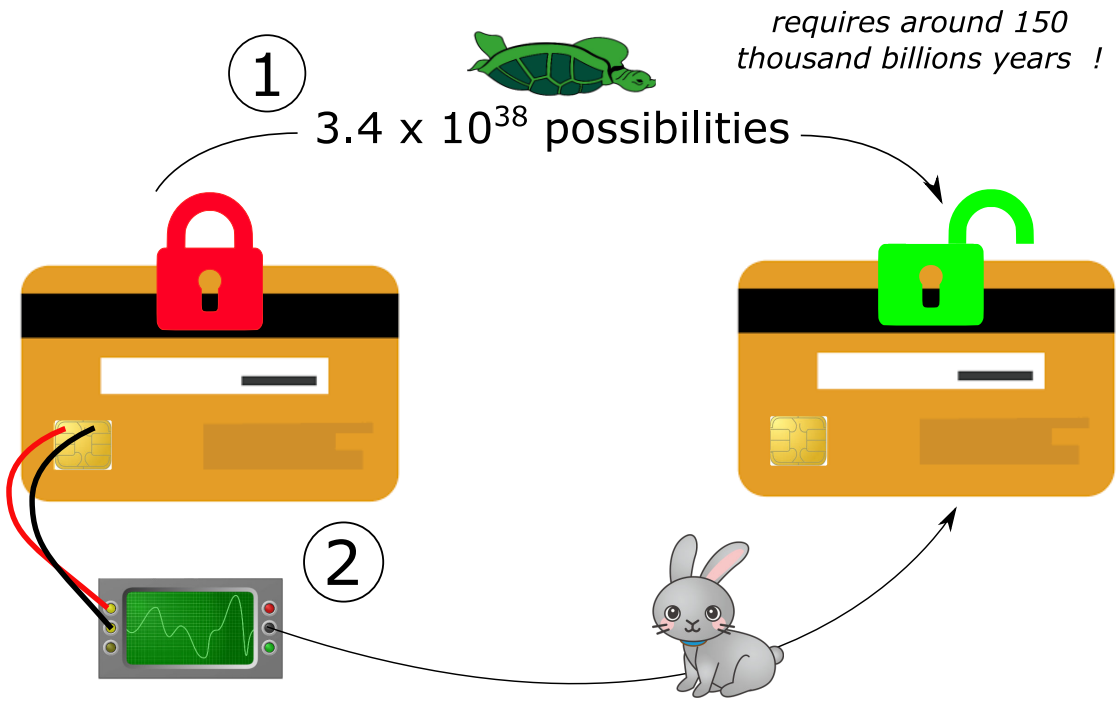

Context: What is side-channel ?

Application: Power side-channel on RSA

- Example on RSA algorithm: *if* $(Key[\mathrm{i}] = 1)$ $\{do\ something\}$.
- Attacker measures RSA power consumption.
- Knowing RSA algorithm & RSA power consumption, the attacker deduces RSA key bits.

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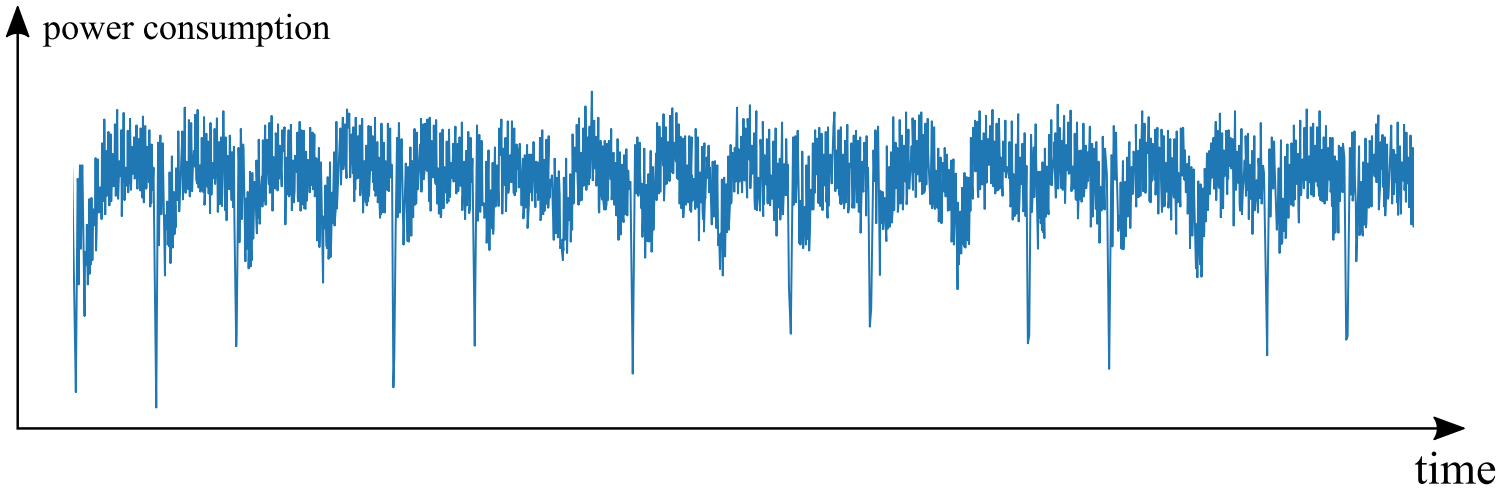

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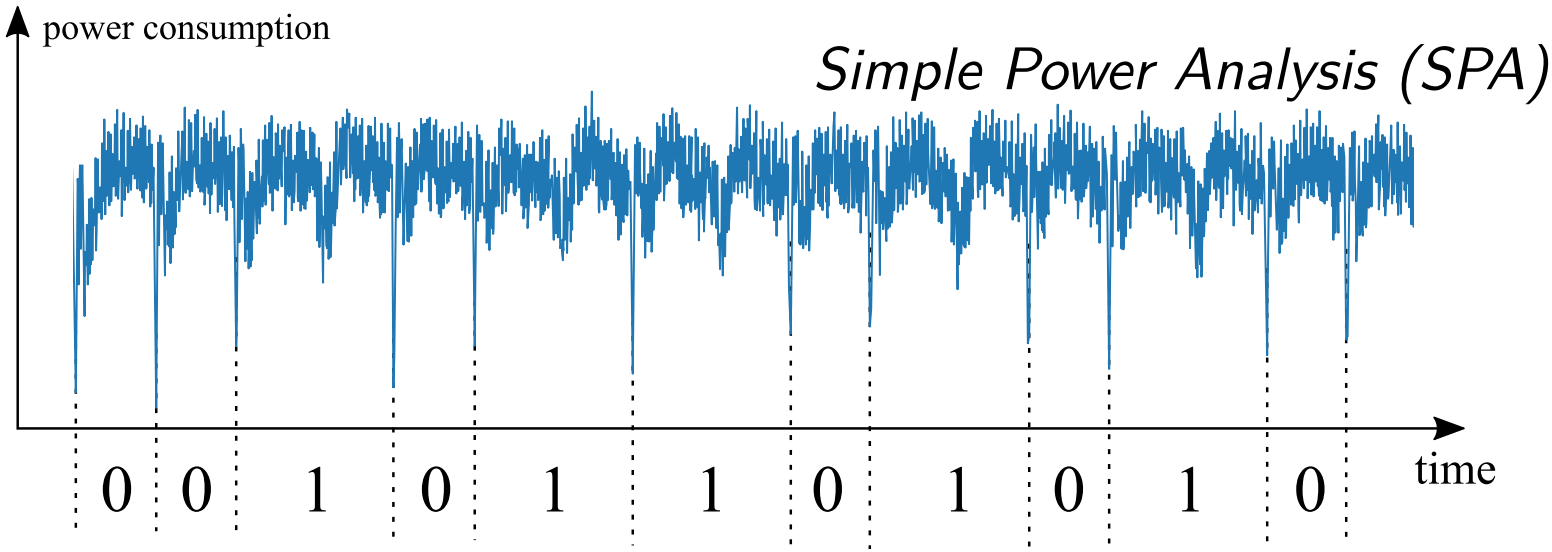
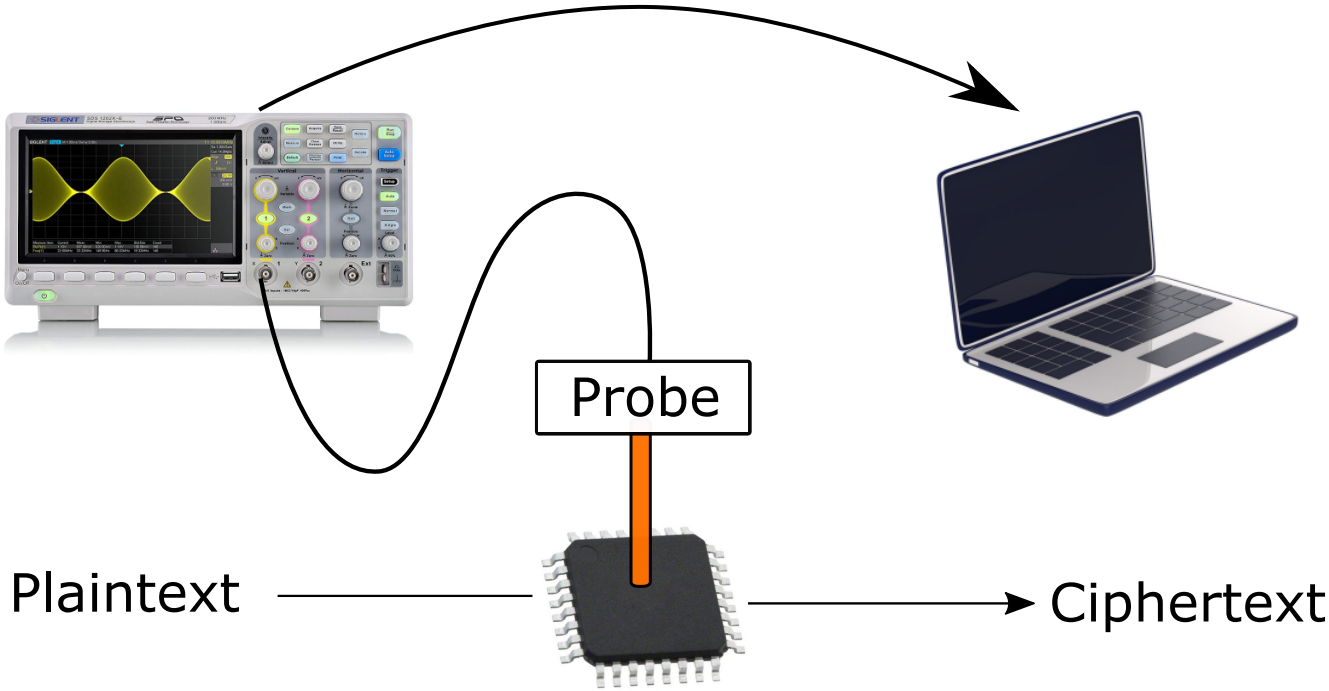
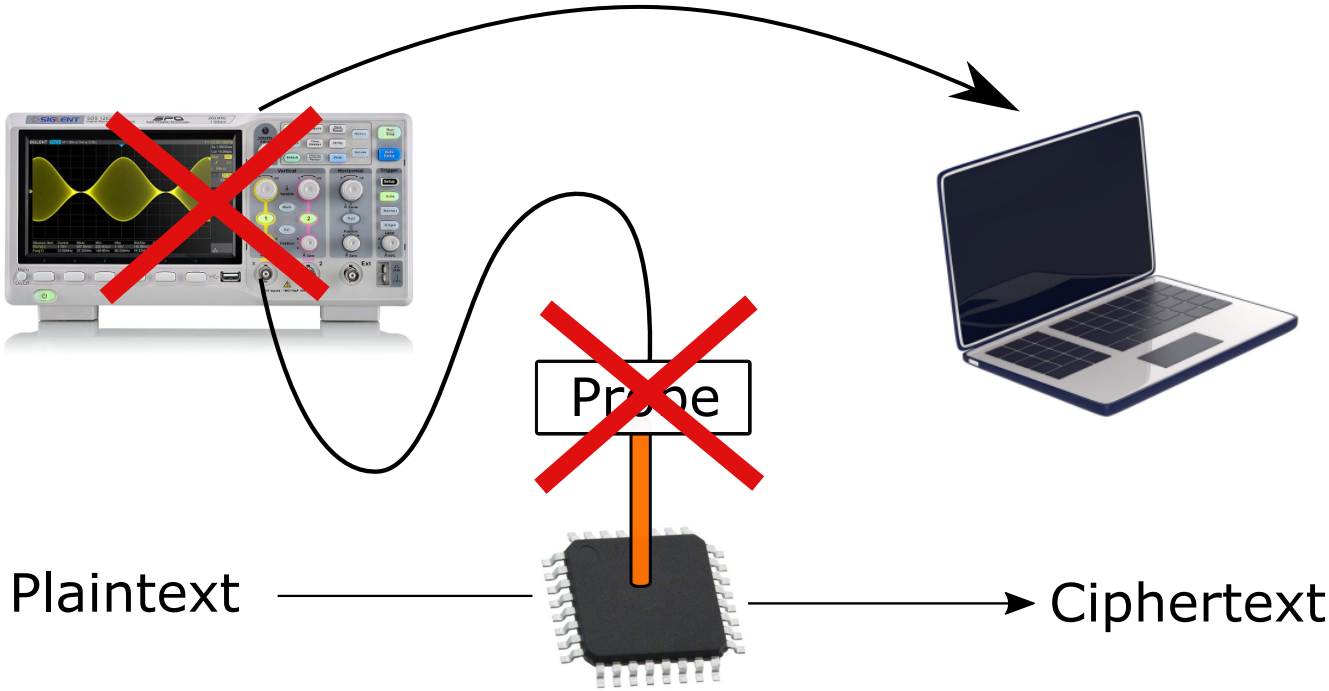


- Type: fault injection attack (FIA) & side-channel attack (SCA).
- Target: smart cards, microcontrollers, system on chip...
- Means: oscilloscope, power & EM probe...
- Range: **local**, direct physical access required.



Context: What is remote side-channel ?

- Type: fault injection attack (FIA) & side-channel attack (SCA).
- Range: **remote, access to a network required.**
- Target: connected devices (IoT), data centers...
- Means: **resources available within the target**.



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2. Presentation of the proposed **RO-based sensor design**.
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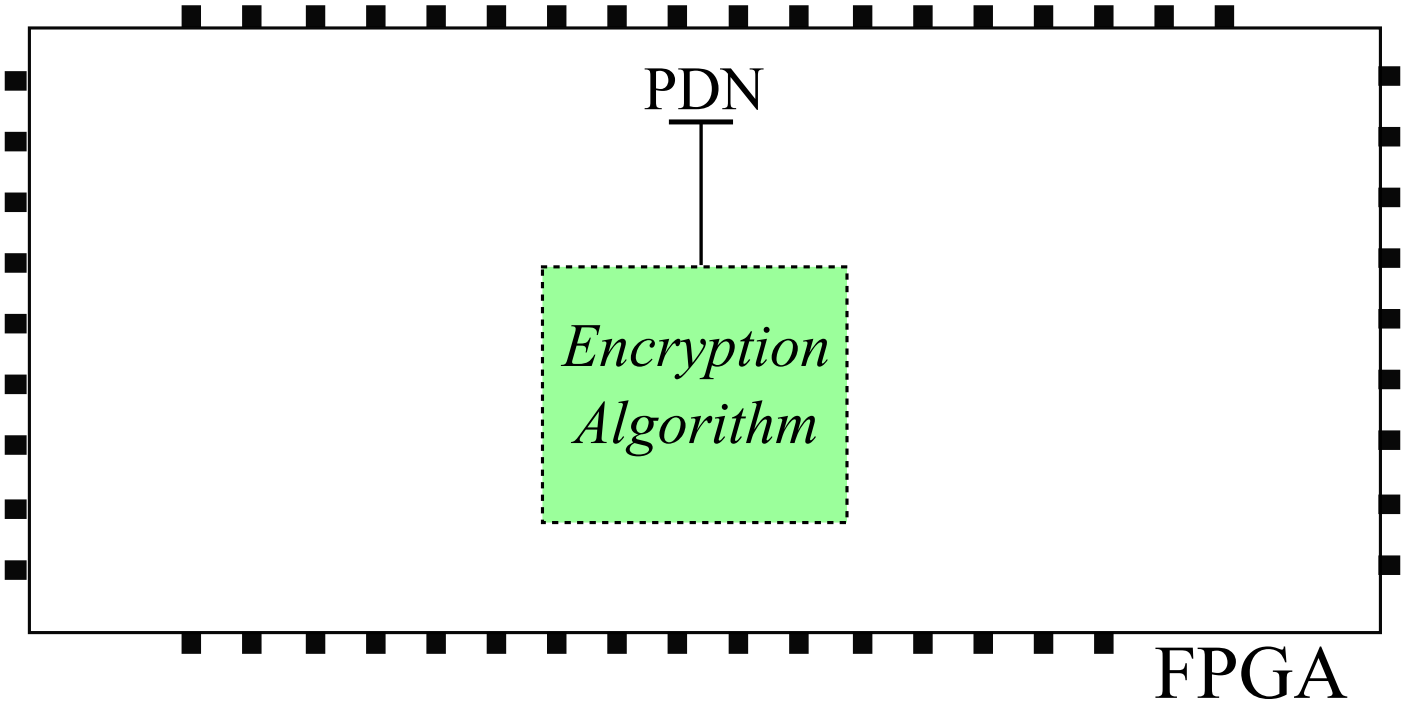

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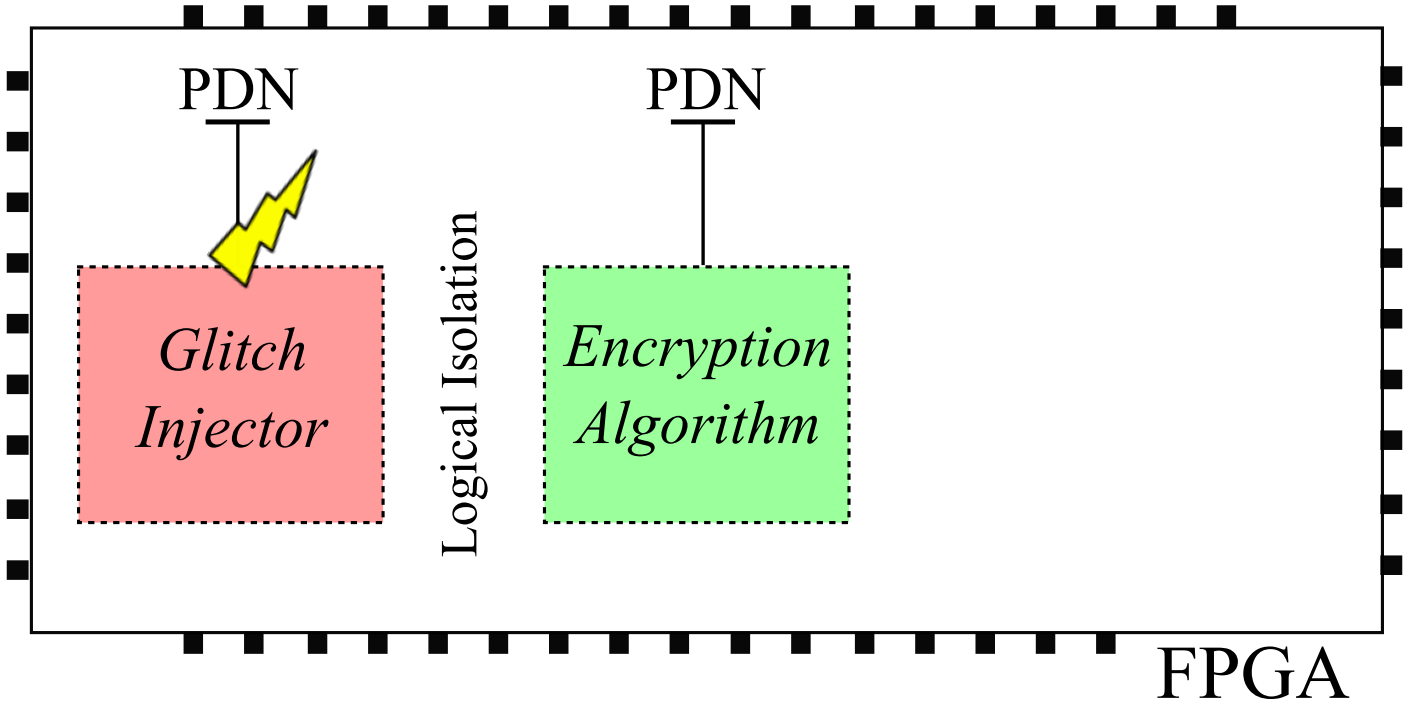

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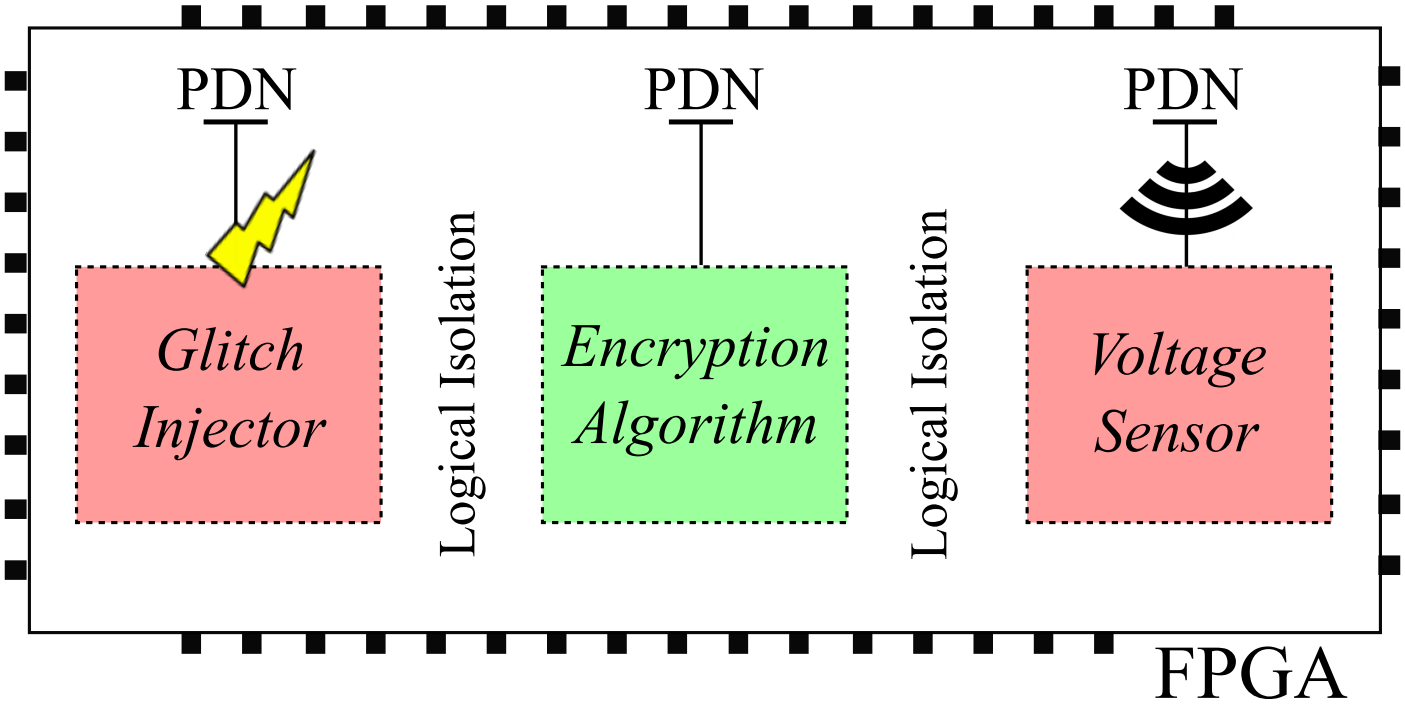

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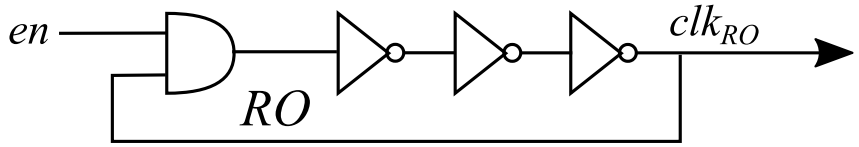

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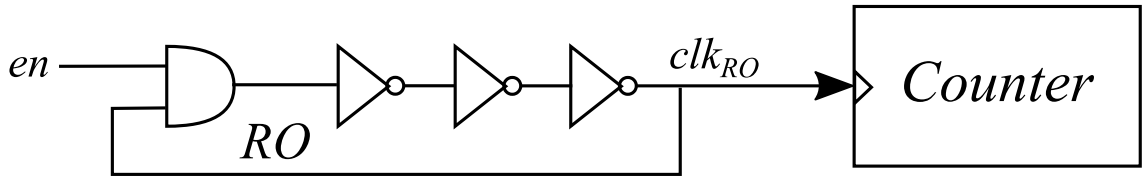

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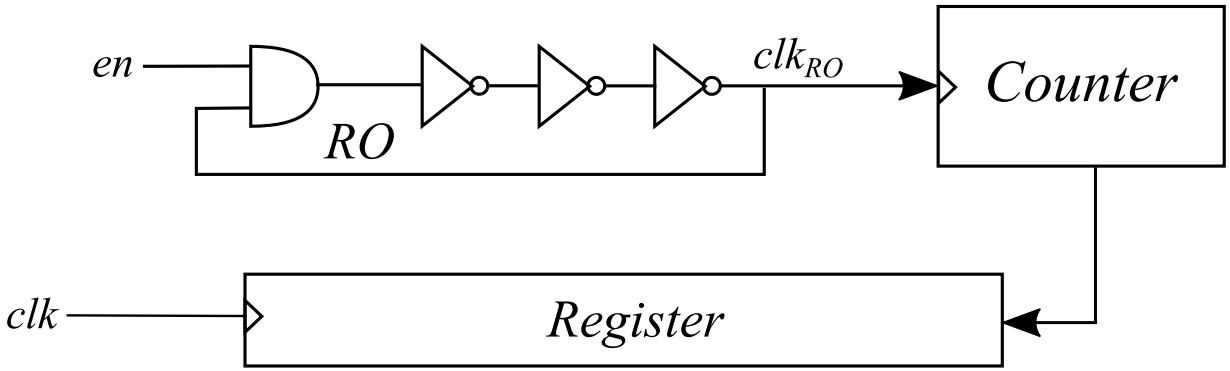

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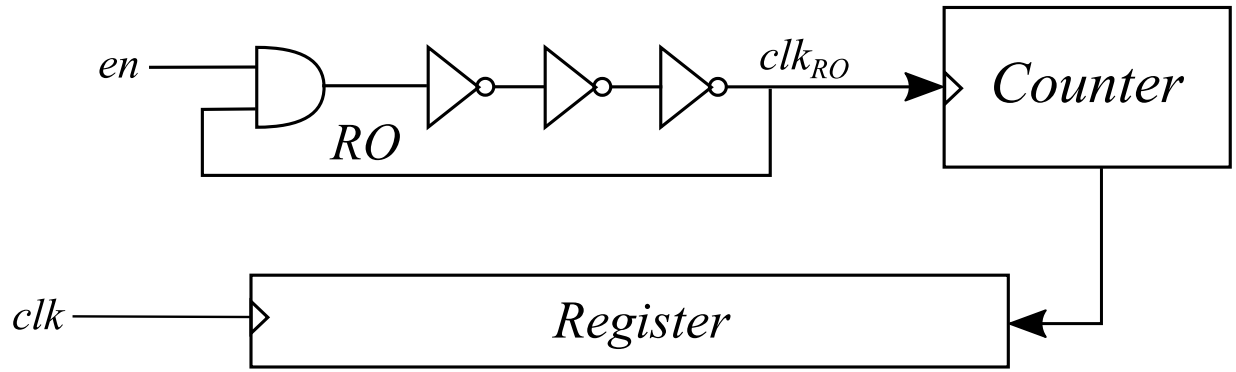
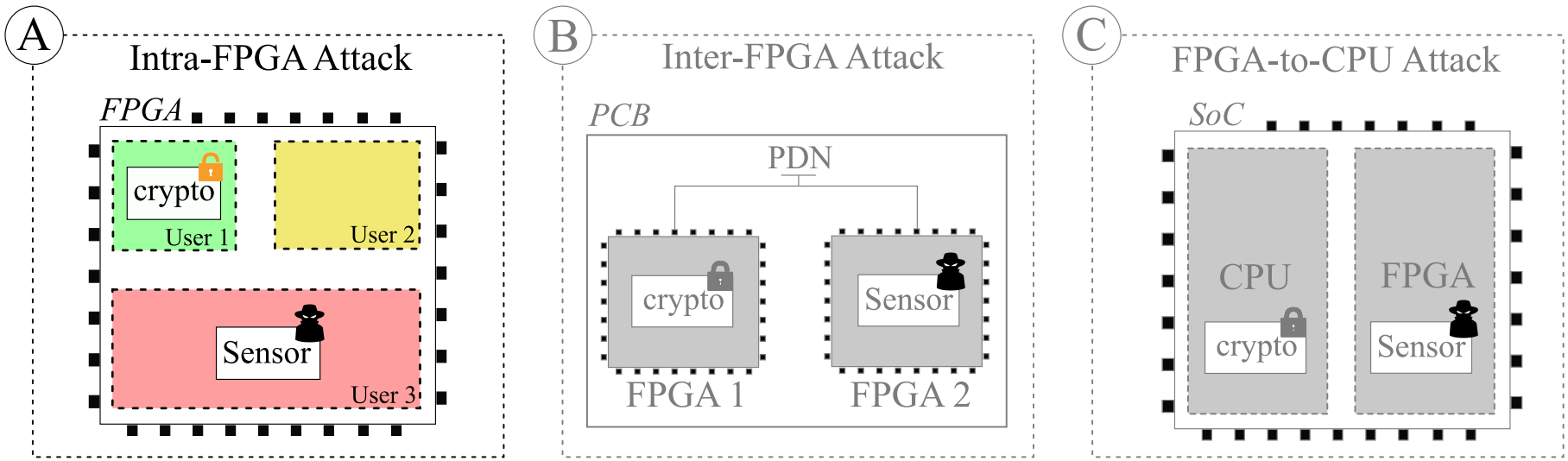


- f_{RO} fluctuates with temperature and voltage variations.
  - if $V \nearrow$ or $T \searrow$ then $f_{RO} \nearrow$: bigger values are sampled
  - if $V \searrow$ or $T \nearrow$ then $f_{RO} \searrow$: smaller values are sampled

- Target: connected devices that embeds FPGAs.
  - A Multi-user FPGAs in **cloud datacenters** (Schellenberg et al).
  - B Printed circuit boards **PCB** (Schellenberg et al).
  - C **Heterogeneous** connected **SoCs** (Zhao et al).



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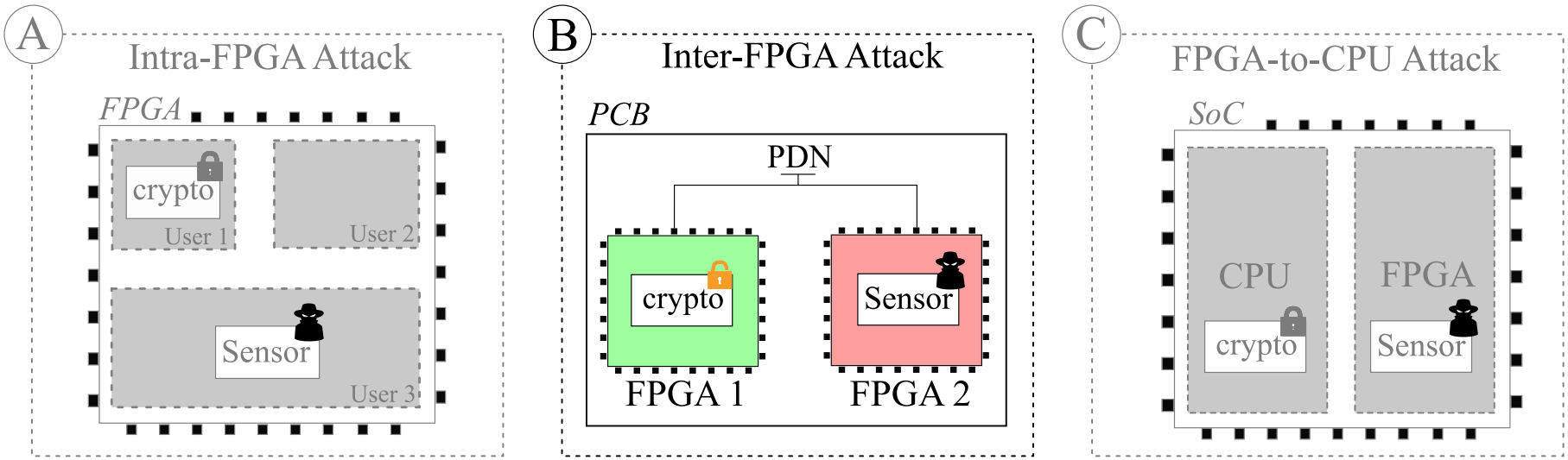

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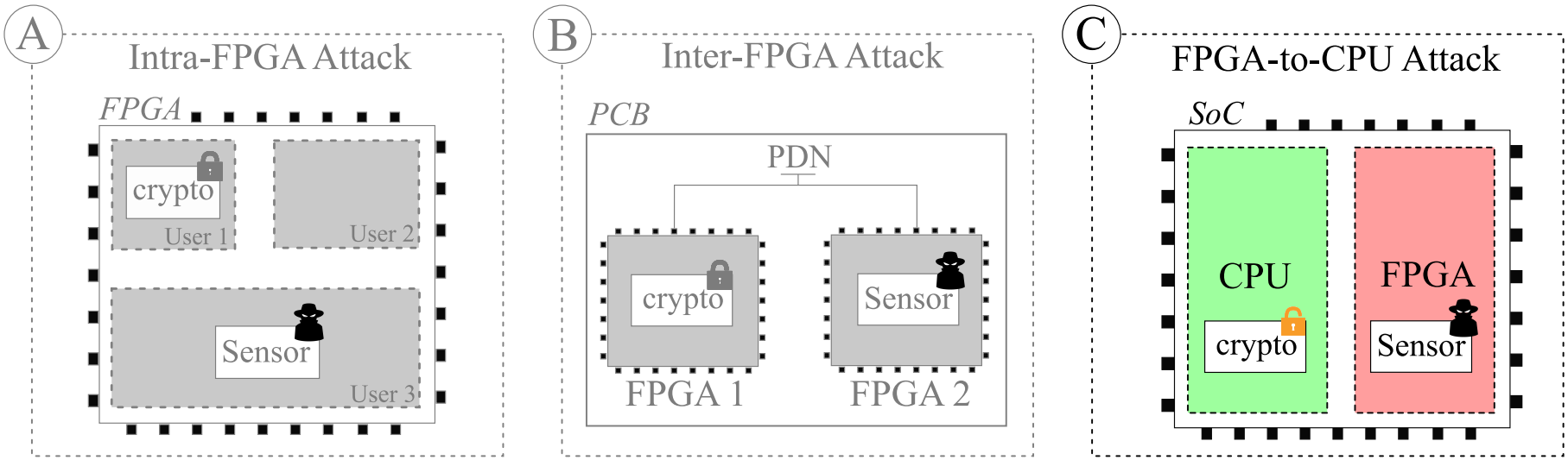

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  "The measurement through ROs requires a counting mechanism. Because of that, even with multiple ROs, a sampling rate of only 8 MHz was achieved [...], making them too slow to sense variations at circuit speed" (Gnad et al. 2018)

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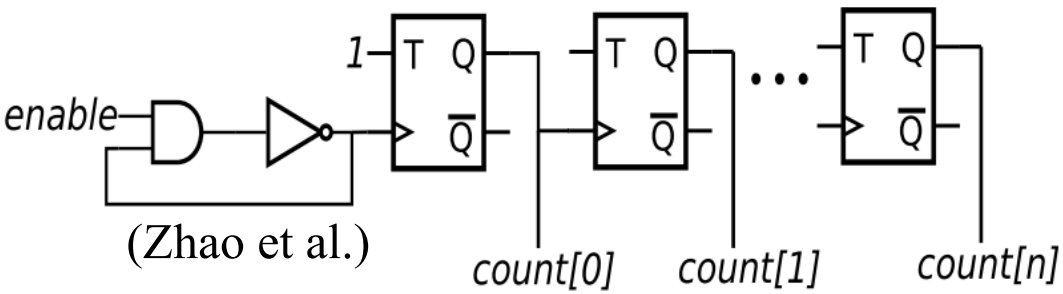

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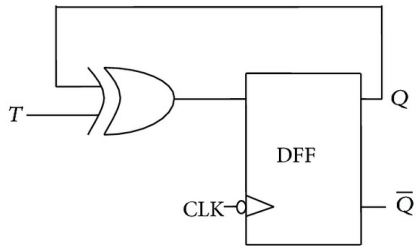

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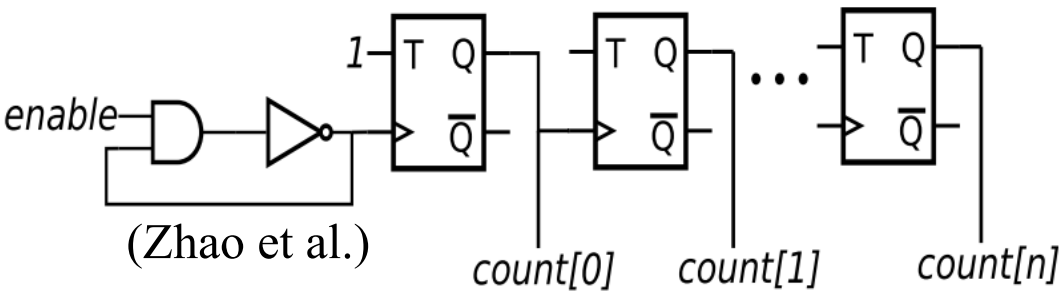

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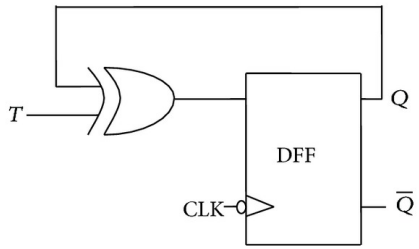

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  - A unique NAND gate for the **RO**.(1 LUT)
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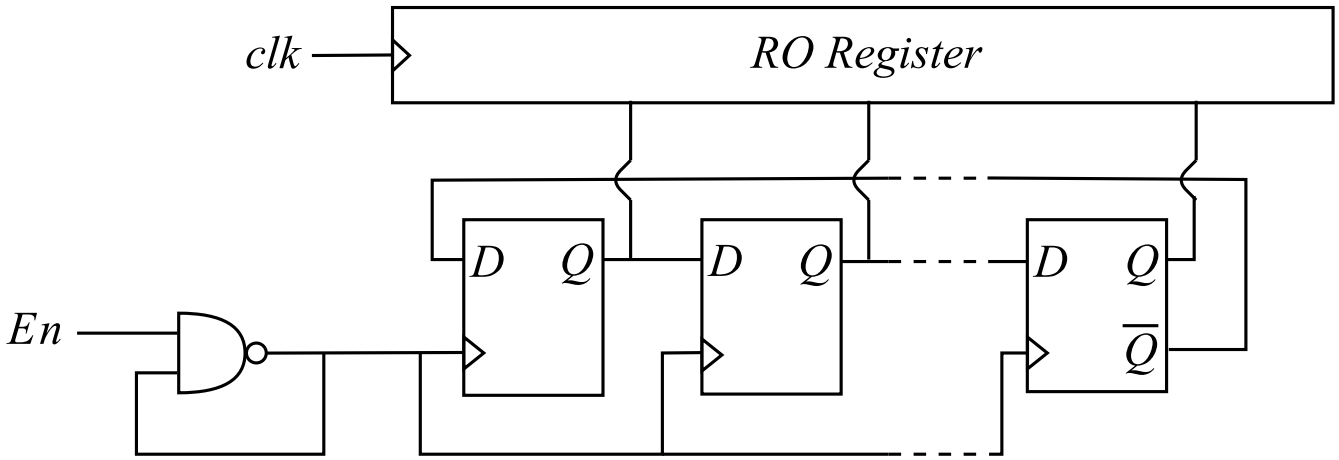

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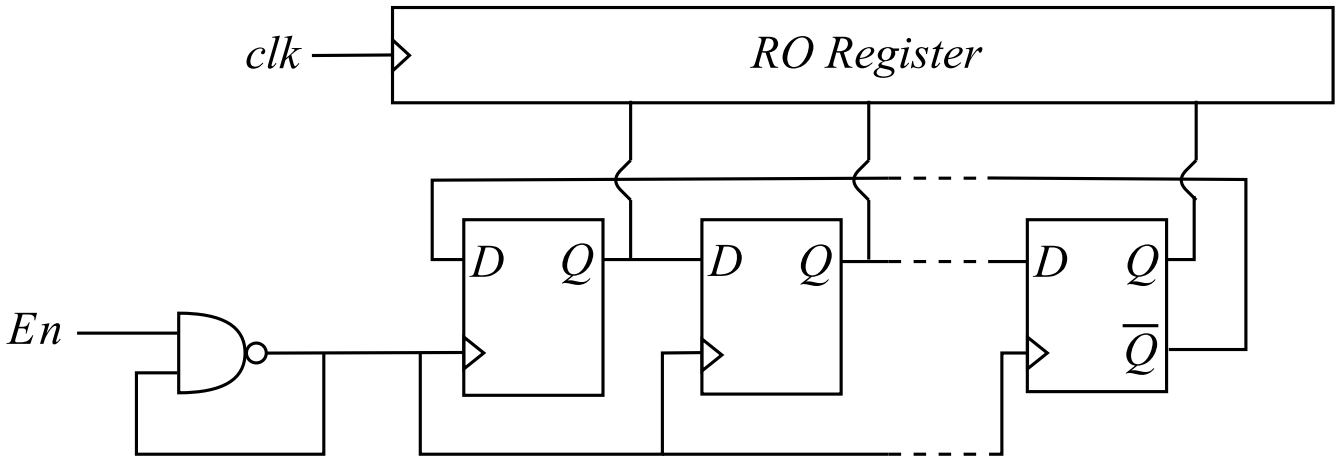

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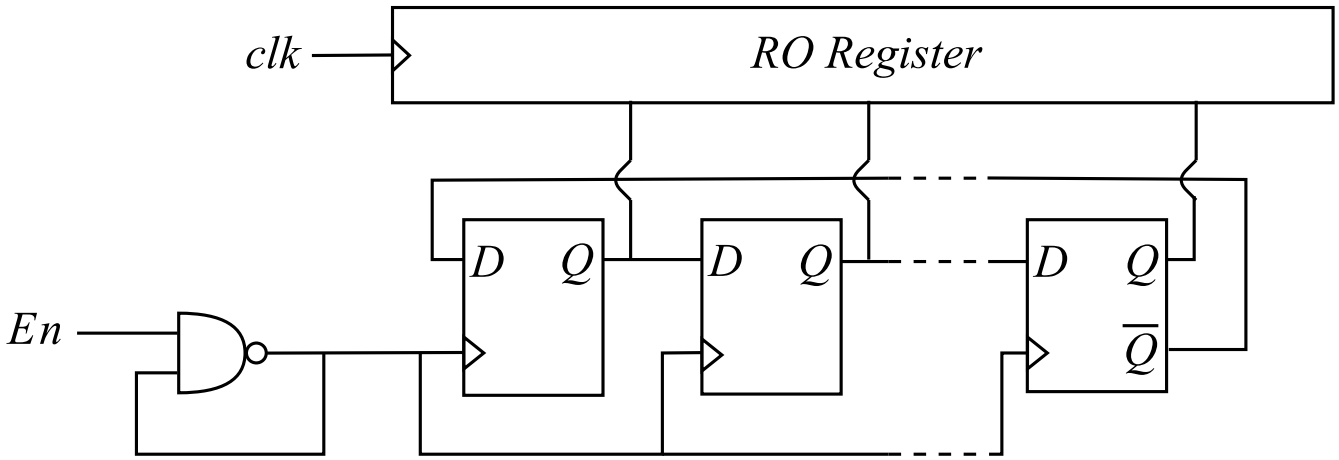

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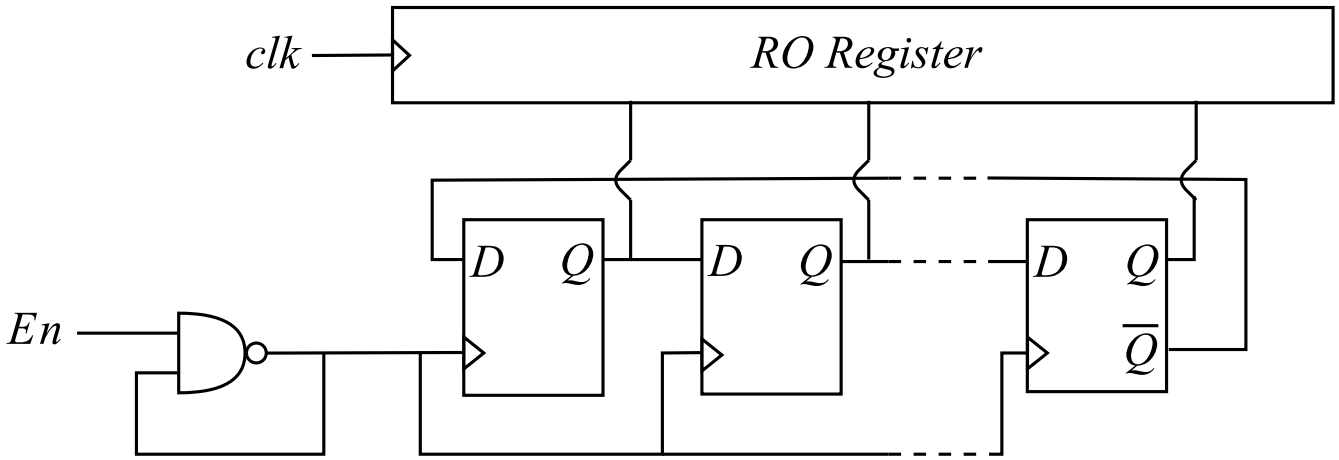
- The overall sensor consumes 2 Artix-7 slices.



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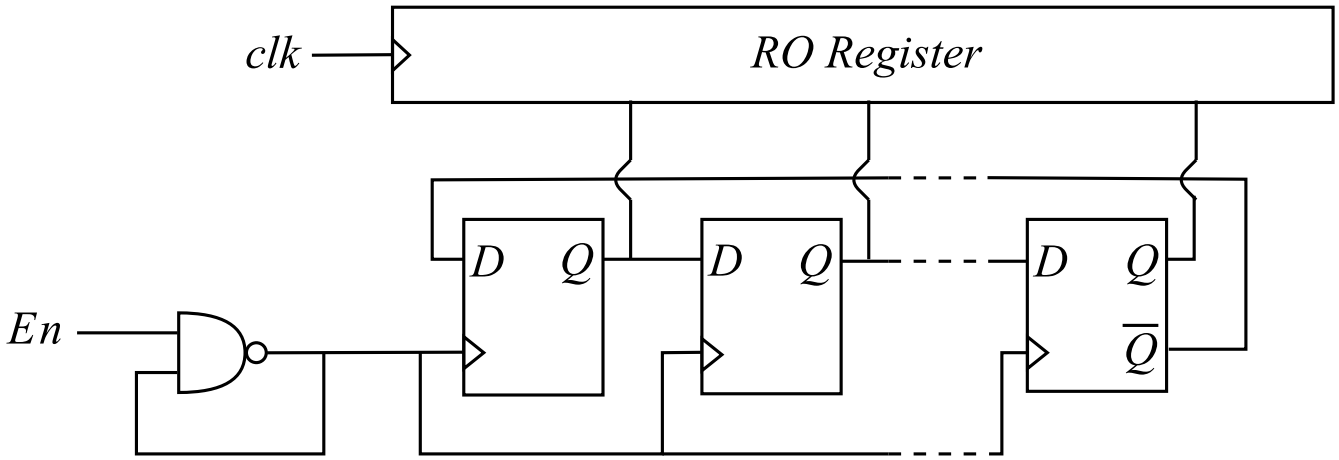
  - RO frequency reaches around **1.2 GHz**.
  - Johnson Ring-Counter provides **16 distinct states**.
  - Sampling register is cadenced at **250 MHz**



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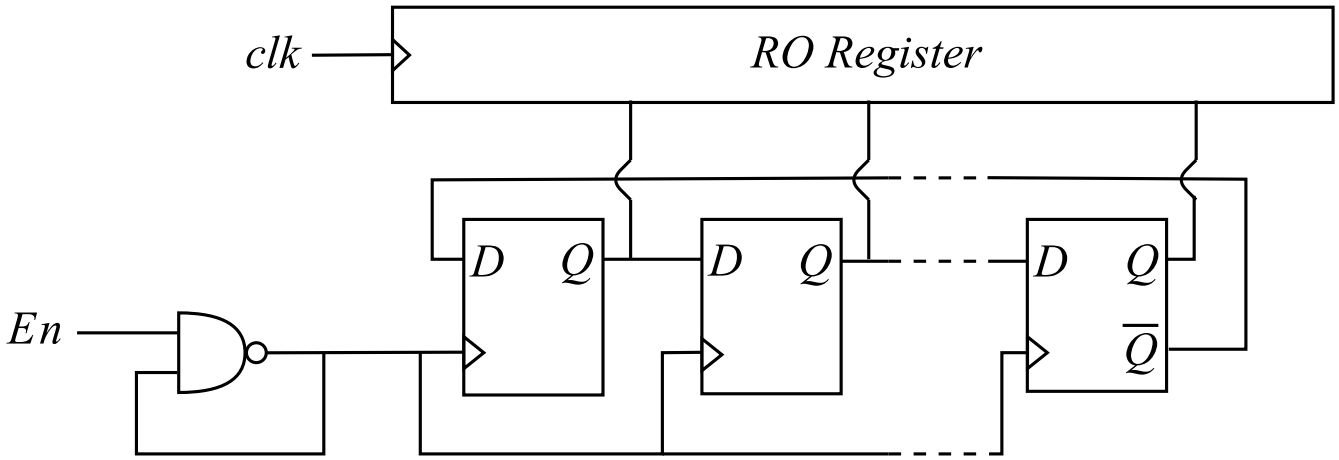

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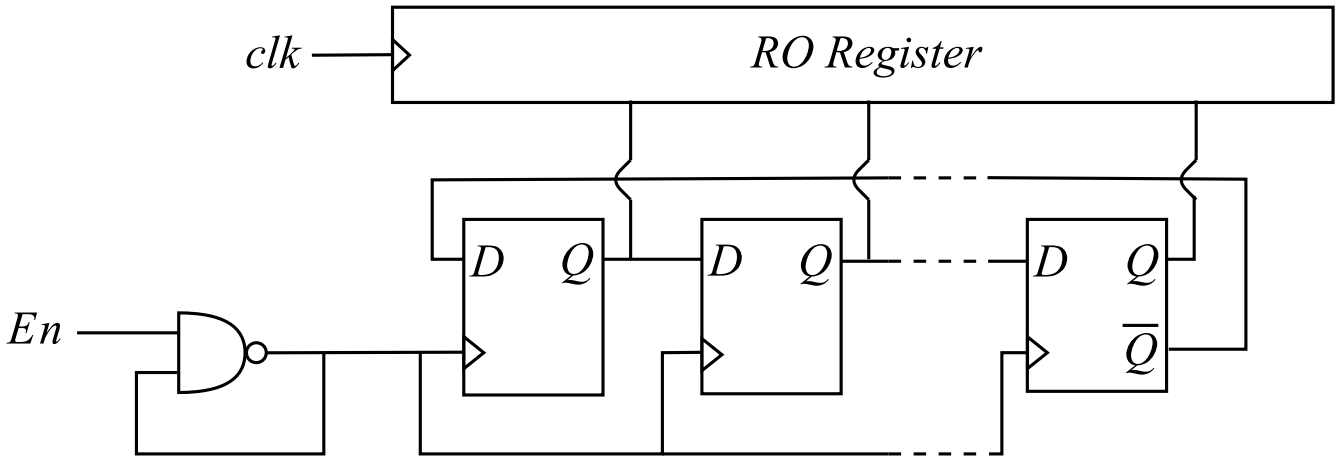

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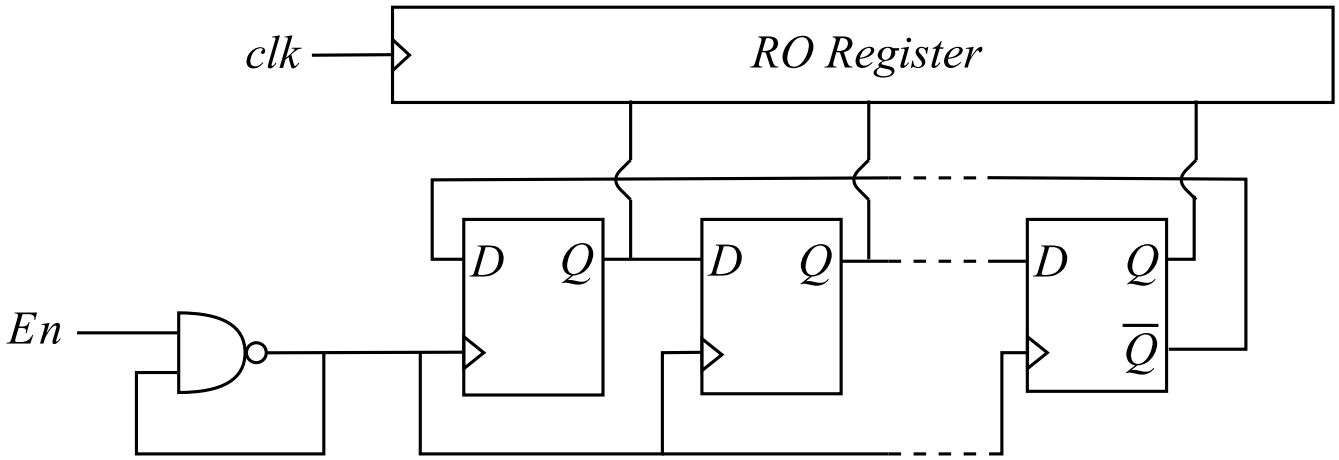
- Only 4-5 counter increments between each sampling !



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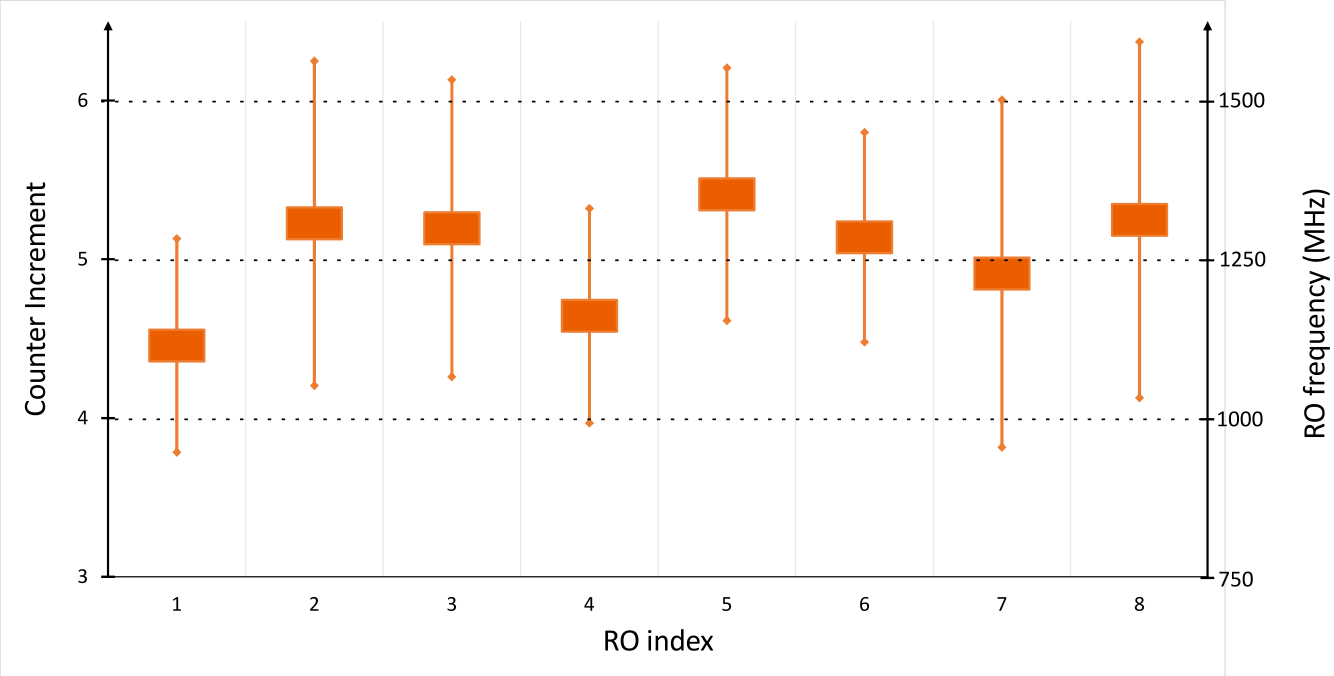

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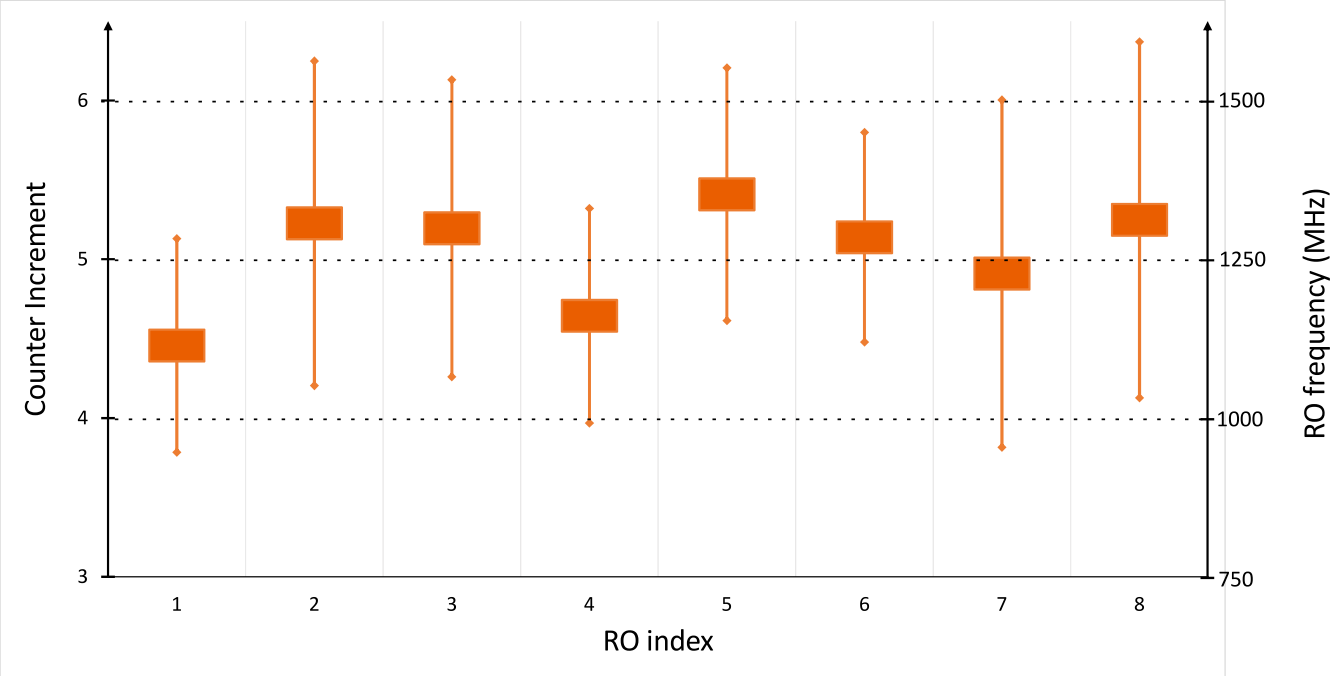

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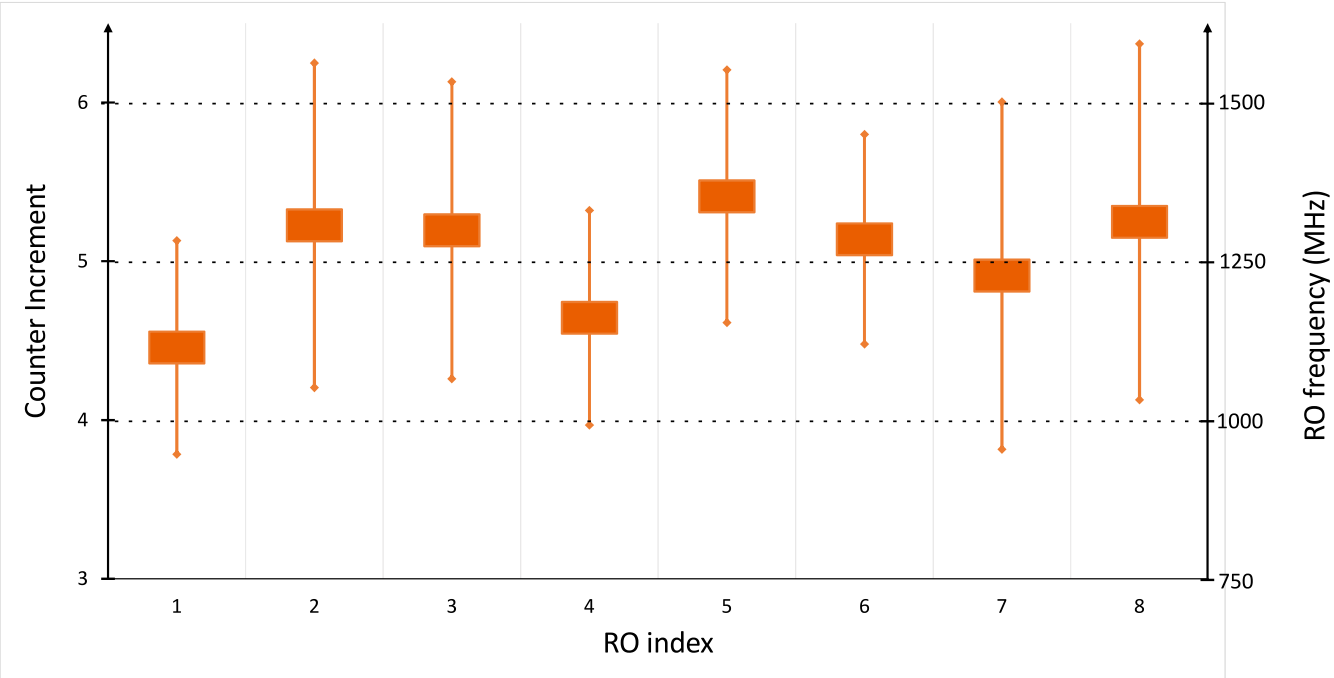
  - **Multiplying ROs** enhances the **overall granularity**.



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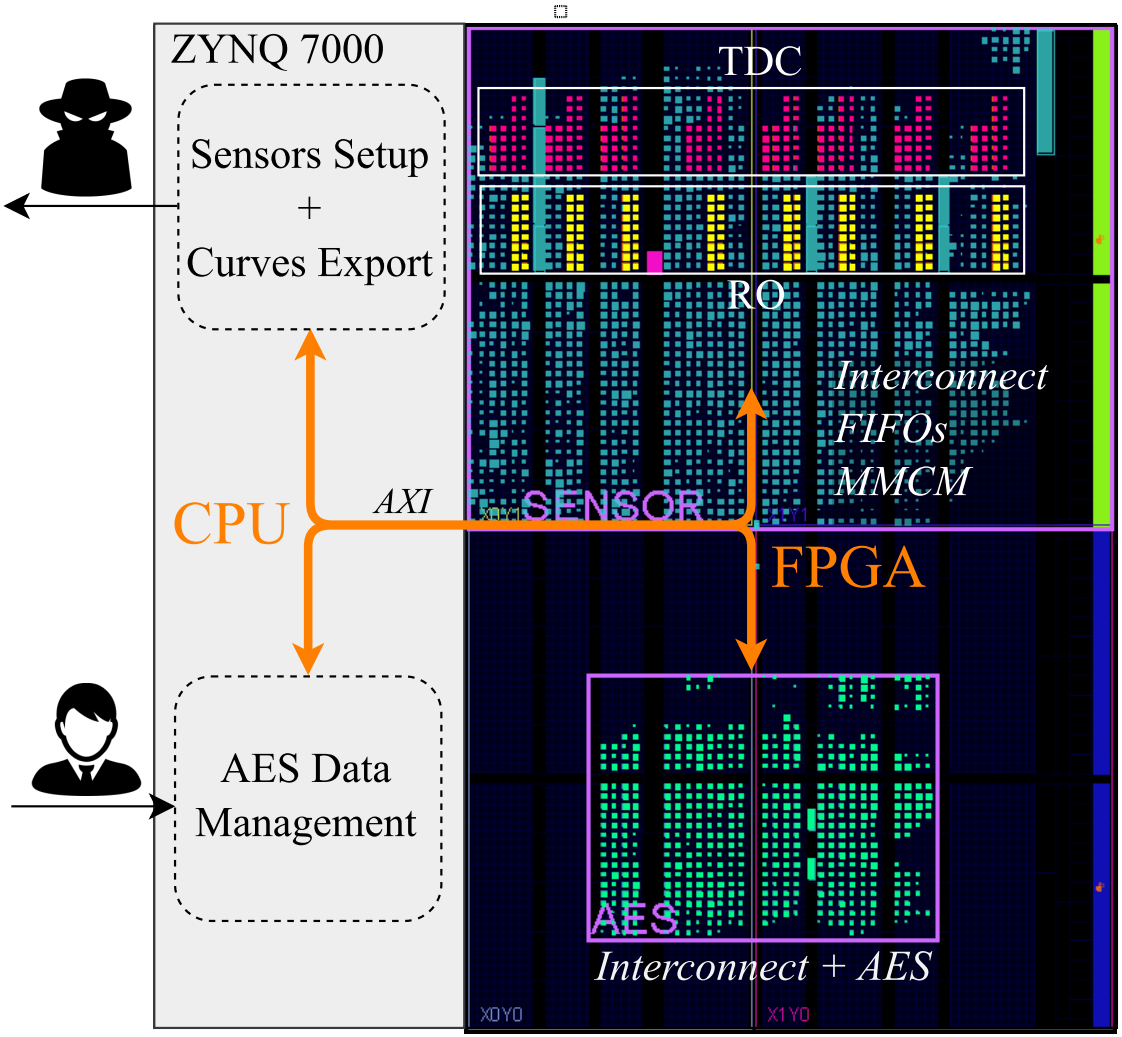
- Target: Xilinx Zynq 7000 heterogeneous SoC
- FPGA (Xilinx Artix-7): 64 RO-based sensors and AES algorithm
- CPU (ARM Cortex-A9): Traces export and AES management



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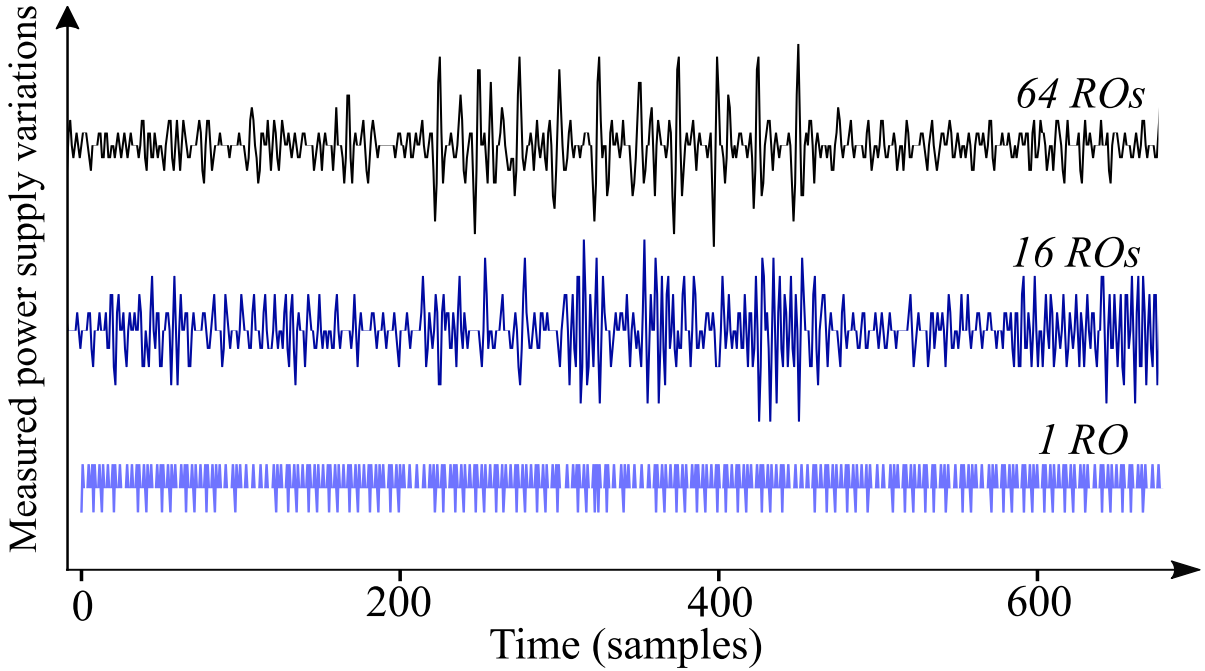

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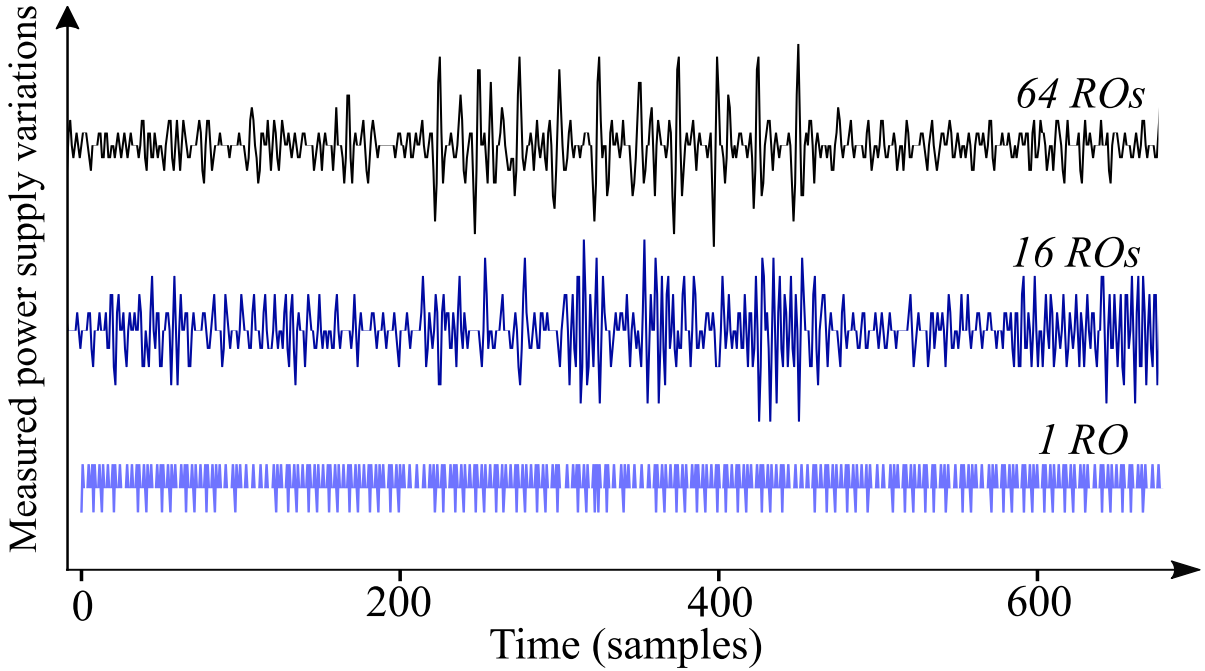

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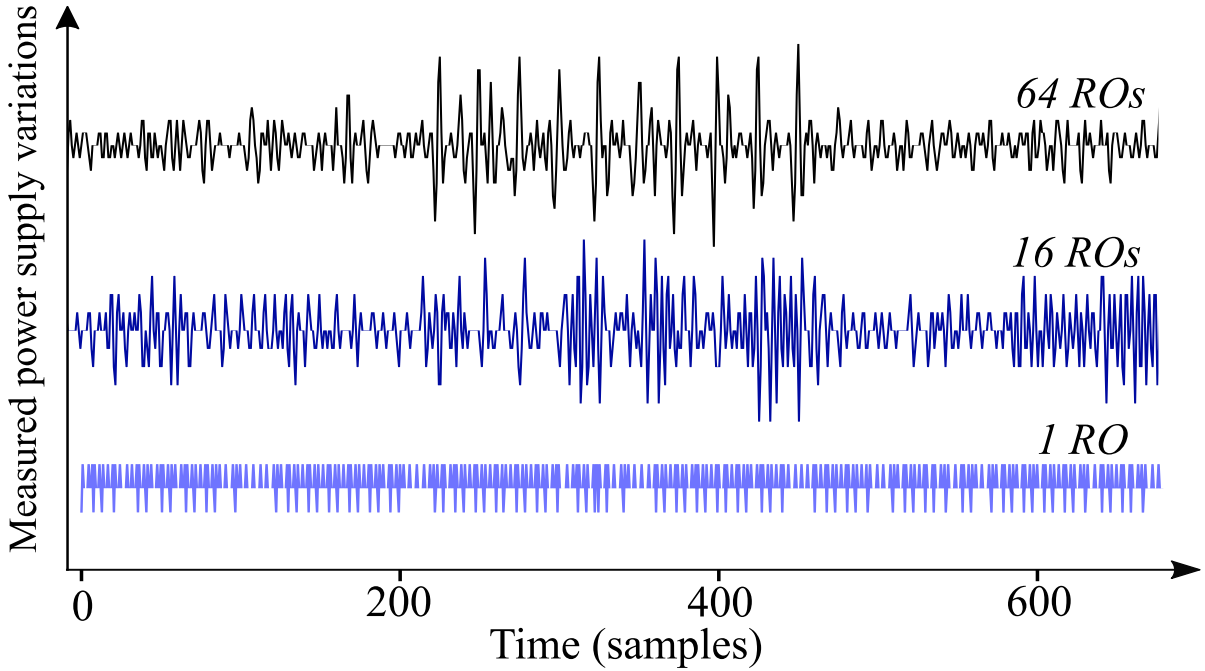
  - RO contributions are **summed** and **averaged**.
  - The 10 AES rounds **gradually** appears.



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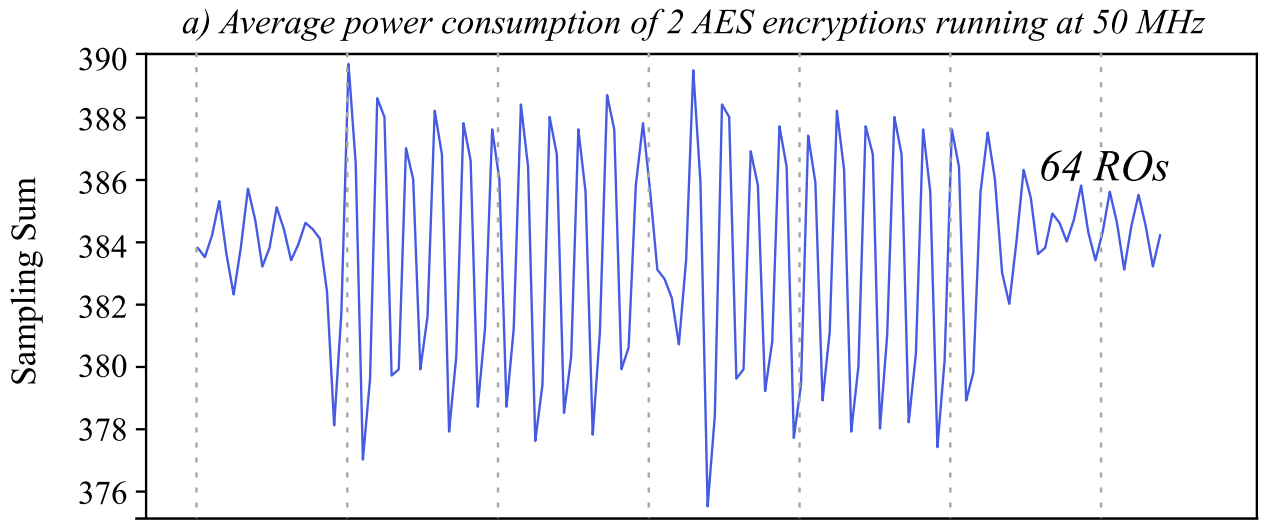

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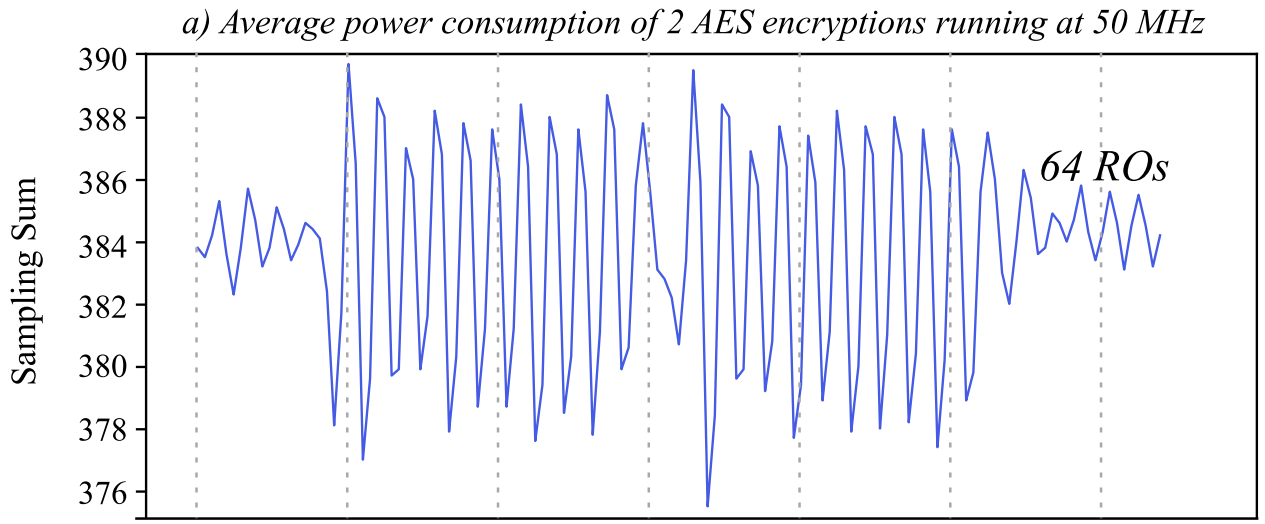

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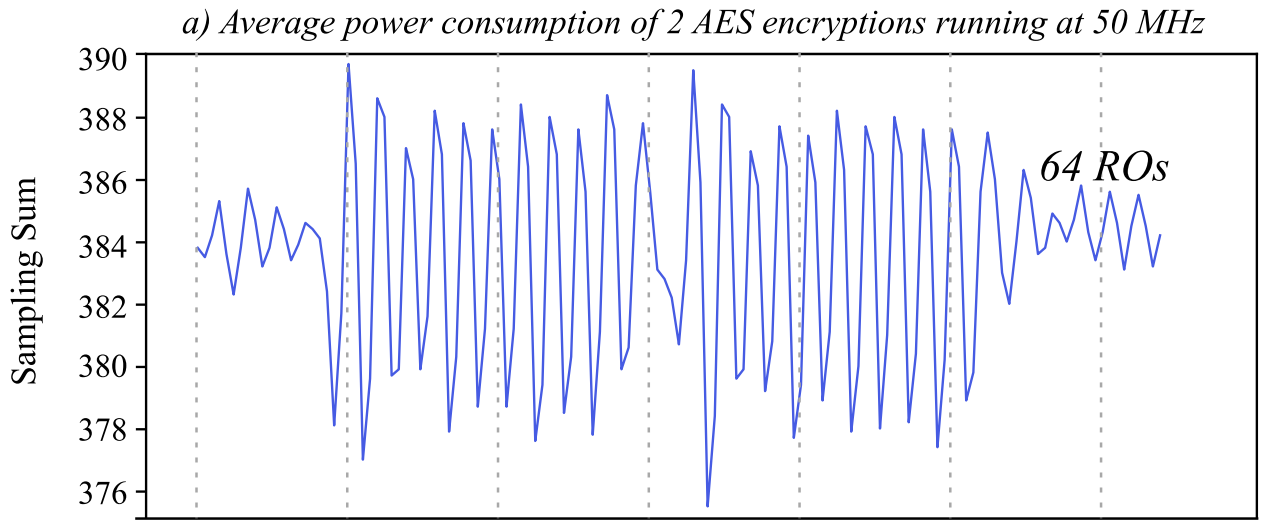

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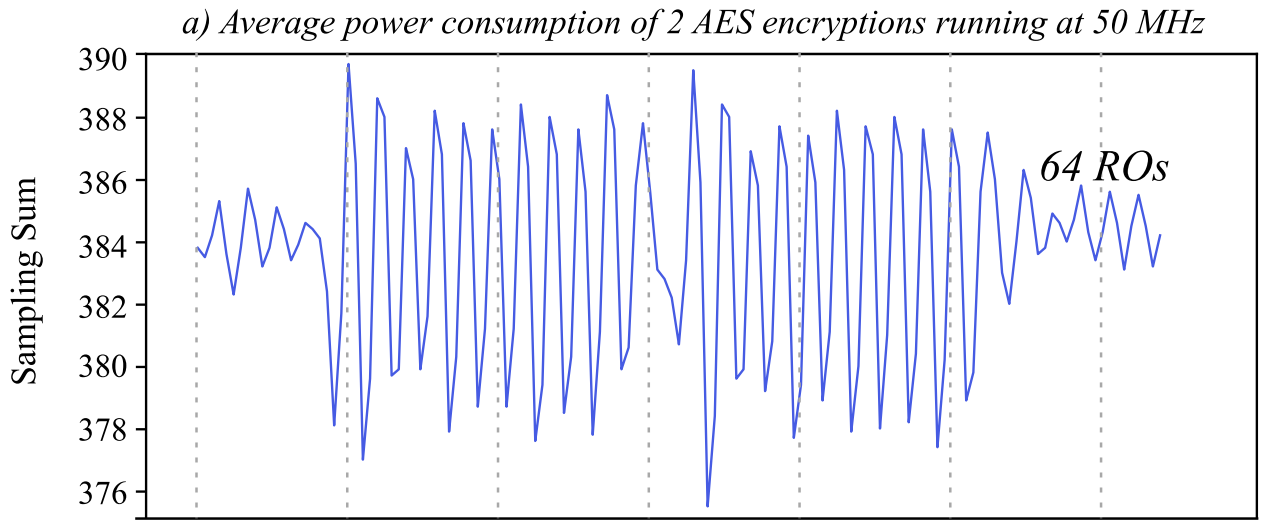

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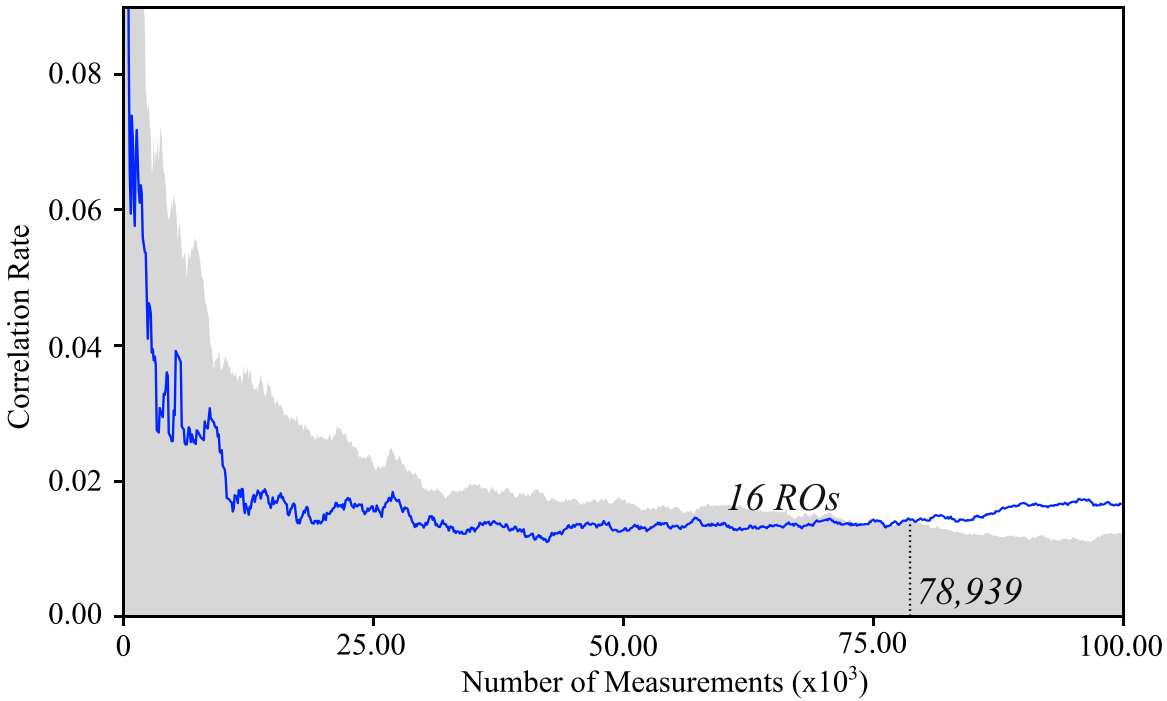
  - Using **16 ROs** $\rightarrow$ **78,939 traces** per AES key byte



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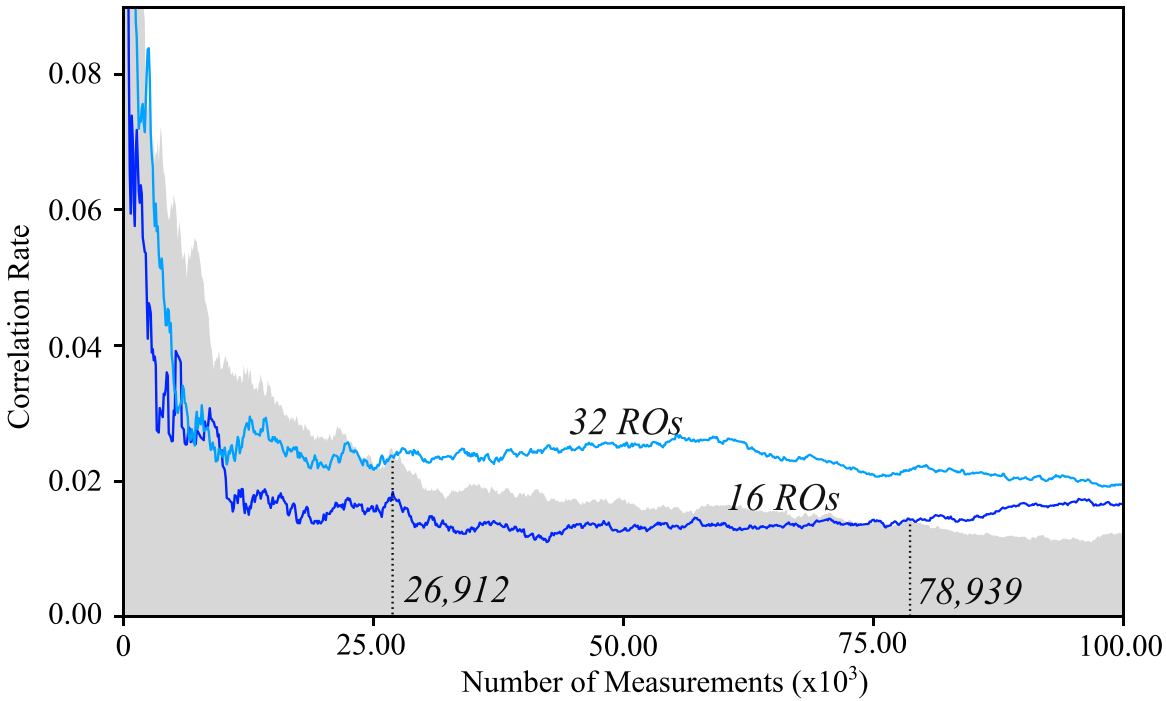

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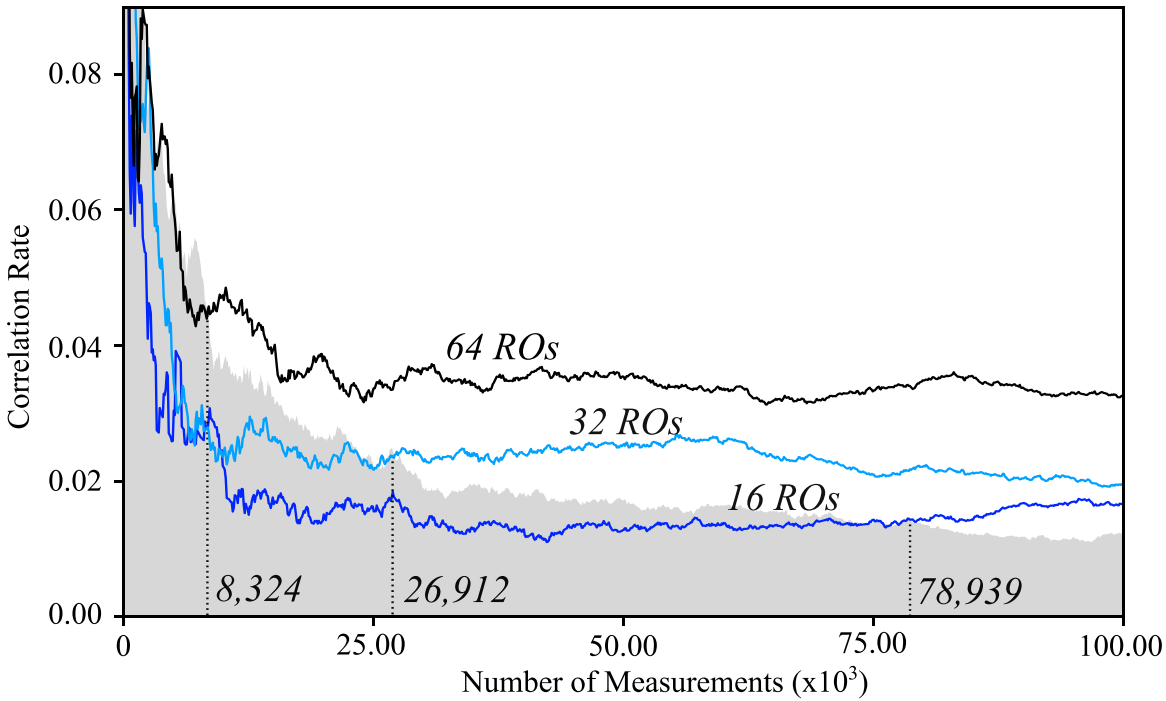
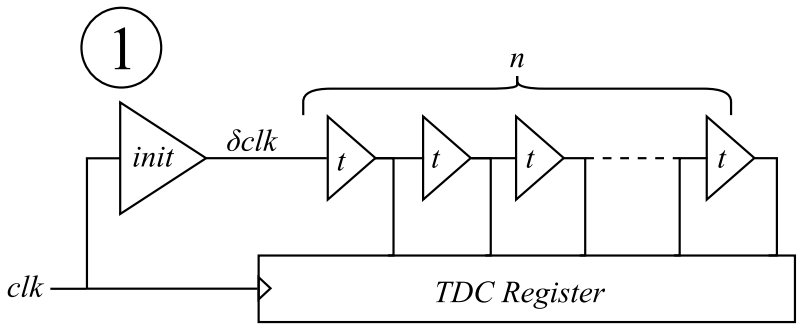
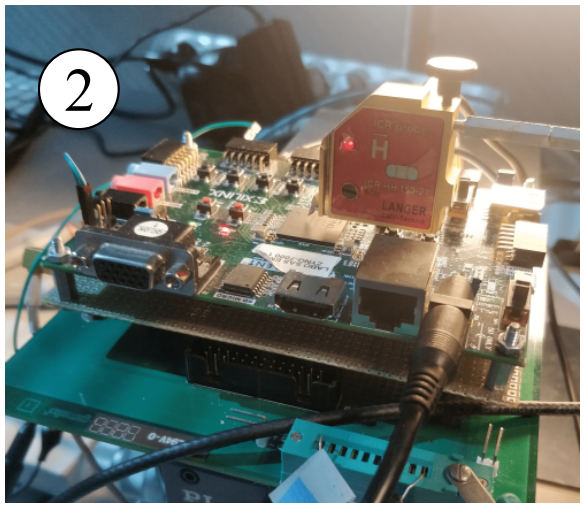


1. **Introduction** to remote FPGA-based hardware attacks.
2. Presentation of the proposed **RO-based sensor design**.
3. Experimental validation and SCA.
4. Comparison with other **SCA setups**.

- Goal: **challenge** our sensor results regarding other SCA setups.
- Experimental Setup ① (internal remote):
  - Time-to-digital converter (delay line)
  - TDC Sampling Rate: **250MHz**
- Experimental Setup ② (external local):
  - EM Probe: Langer ICR HH 150
  - Oscilloscope Sampling Rate: **5GS/s**



Time-to-Digital Converter



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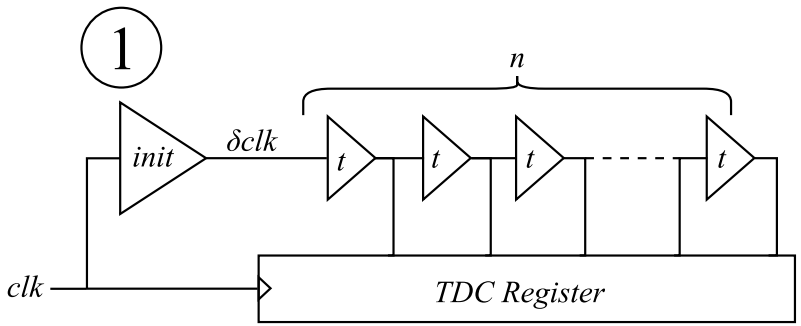

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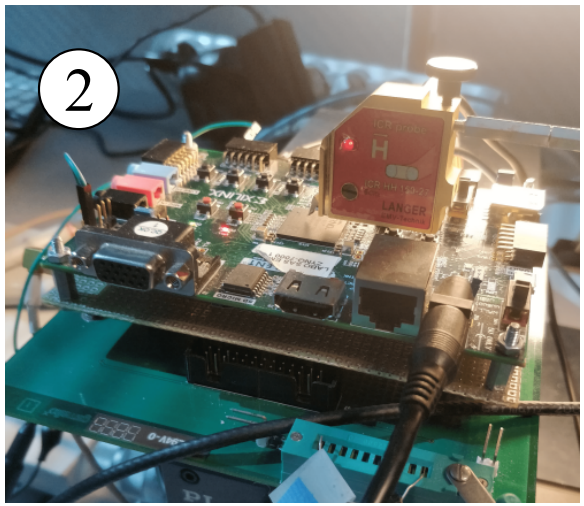

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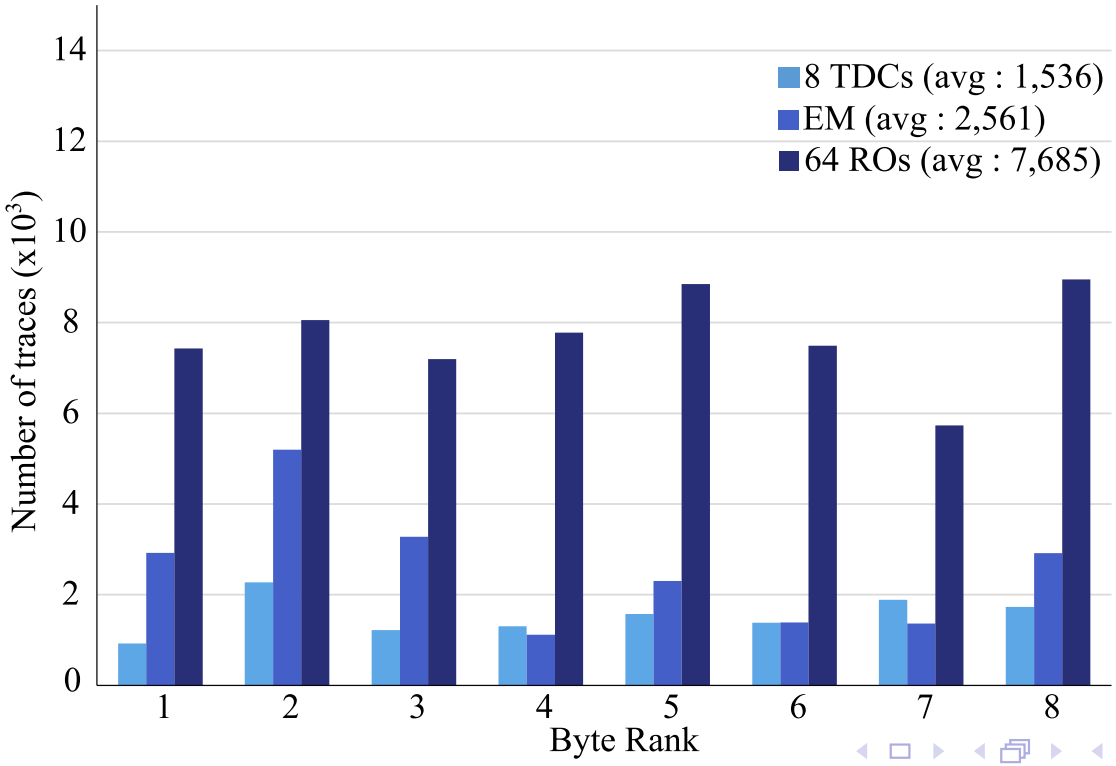

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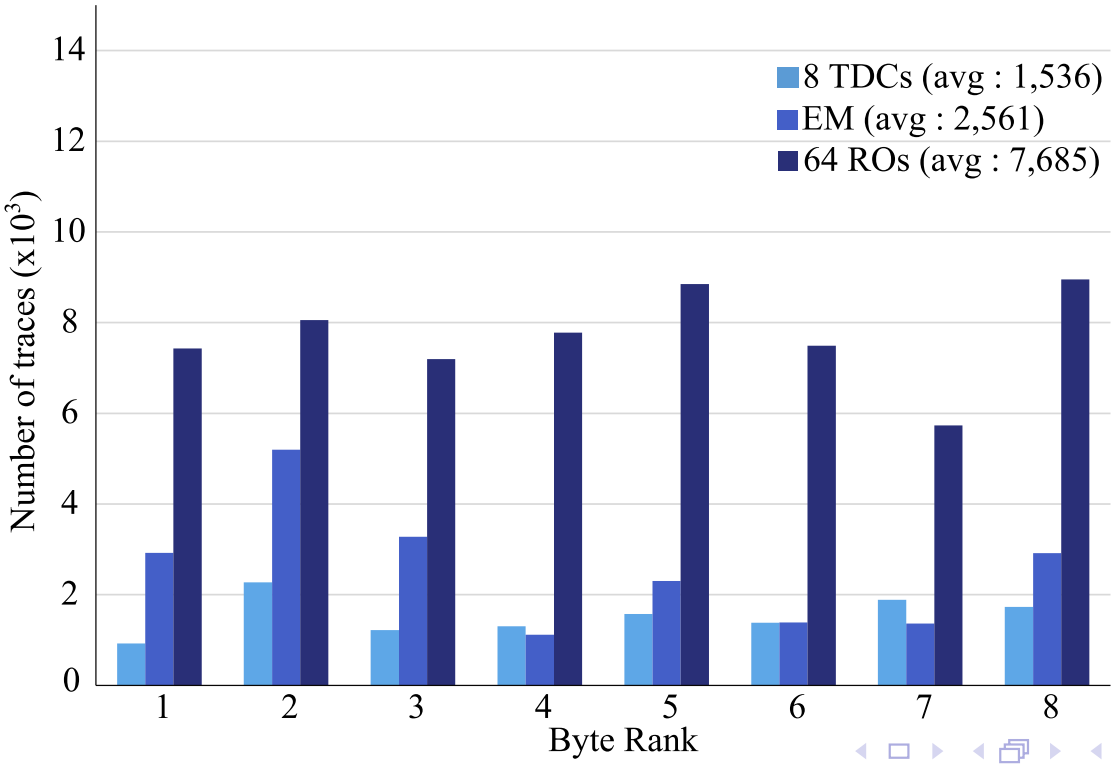

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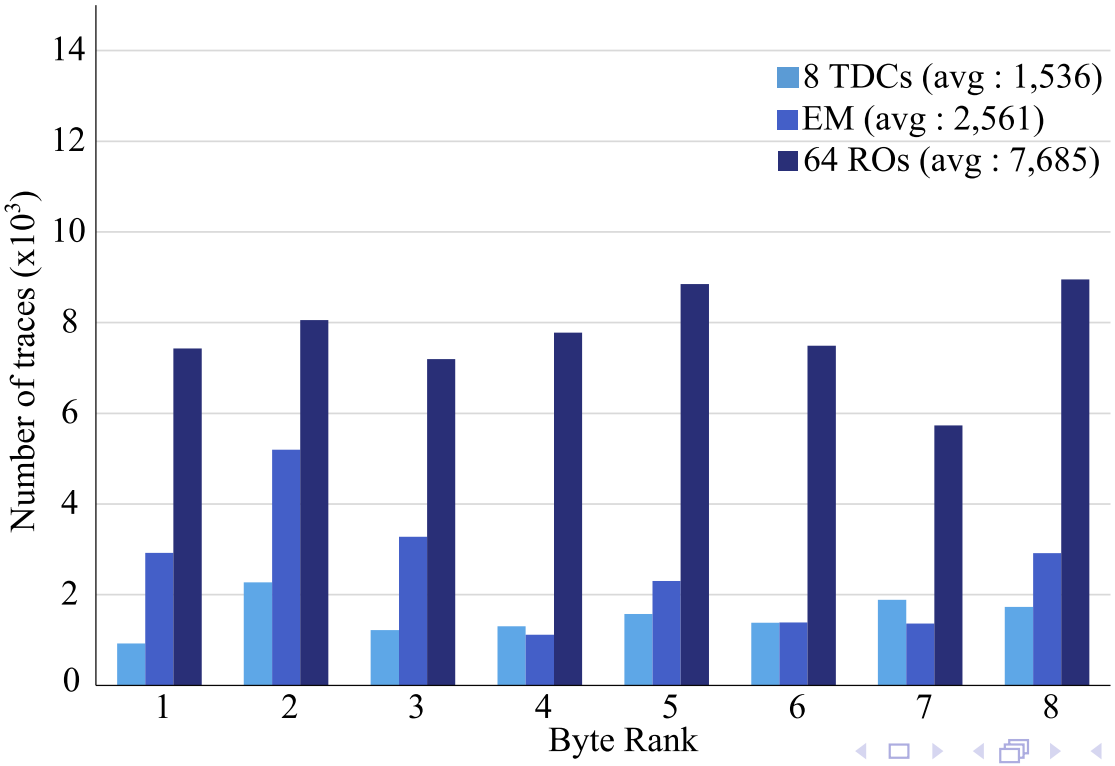

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  - Reaching **high sampling frequencies** with decent resolution.
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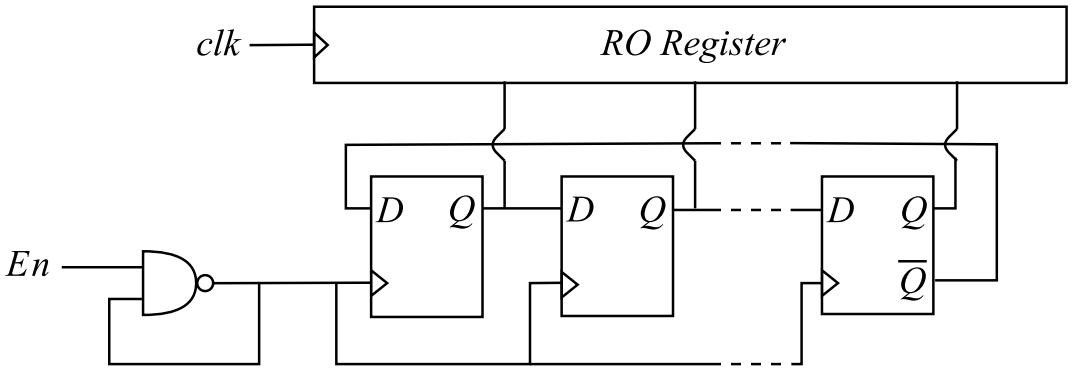
- It's an ideal alternative for monitoring fine-grained high-speed voltage fluctuations in SoCs



Thank you! Questions?

joseph.gravellier@emse.fr